An EMC/EMI system-design and testing methodology for FPD-Link III SerDes

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High Speed Data and Clocks

Introduction

Automotive electromagnetic compatibility (EMC) tests are broadly classified into two areas: 1) Radiated emissions tests that analyze the electromagnetic interference (EMI) or noise generated by the system as an "aggressor", and 2) System electrostatic-discharge (ESD) and bulk-current injection (BCI) tests that measure the "immunity" of the system as a "victim" to ambient emissions. In order to pass these tests, designers should follow best practices for power-supply layout, grounding, high-speed guidelines, and cable and connector shielding.

This article presents system-design guidelines that aid in EMI/EMC system design and the testing of FPD-Link III high-speed serializers and deserializers (SerDes) as shown in Figure 1.

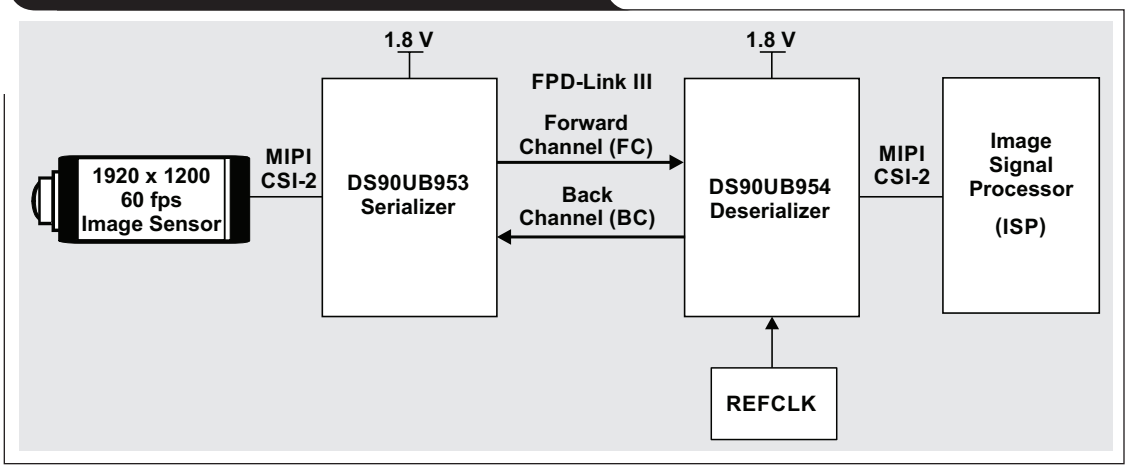
EMI/EMC testing

Signals propagate as electromagnetic waves that can cause electromagnetic interference (EMI). EMI tests are typically performed according to Comité International Spécial des Perturbations Radioélectriques (CISPR) 25, the automotive EMI standard that original-equipment manufacturers (OEMs) use as basis for their testing requirements. CISPR 25 defines the maximum limits of emissions that a system can create so as not to act as an aggressor and interfere with other systems operating within the same bands. OEMs may have their own limits that differ from CISPR 25; however, the testing methodology remains the same.

Radiated emissions are emitted as electromagnetic waves and can be picked up by unintentional antennas present in the system. The subsystem, or device under test (DUT), is placed in an isolated room/chamber and set up in a well-defined, reproducible electrical arrangement. All other possible emitters are removed from the chamber, and the DUT is turned on and allowed to operate normally. The DUT is powered through an artificial network, or line-impedance stabilization network (LISN), and loaded according to its normal operation. Putting a capacitor at the LISN output pins for the power supply to make the test setup completely stable can help. Measuring the noise across the 50-Ω impedance in the LISN can provide information about the ambient noise.

A spectrum analyzer measures the emissions across different frequencies (either through the LISN or from an antenna) for comparison against the CISPR 25 limits. Both the peak and average measured values of the emissions must be within the limits for "pass." The level of passing falls into several categories or classes that have different limits. The emission measurements are broken down into different sections, each tested with a different type of antenna appropriate for the band. The official CISPR 25 documentation explains the test setup for CISPR 25 radiated emissions testing and defines the limits.

Figure 1. FPD-Link III system block diagram



Identifying the EMI/EMC source

Identifying the noise source in a system is a critical step toward system compliance. Noise can be the result of intermodulation or harmonic content of the fundamental frequencies.

Table 1 captures this methodology in a step-by-step procedure and described as follows:

1. Capture the ambient noise, including the noise associated with the power-over-cable (PoC) switching circuitry.
2. Capture the serializer noise by itself.
3. Capture the deserializer noise by itself.
4. Capture the imager noise by itself; disable the forward channel, and keep the back channel on.
5. Slow down the REFCLK clock rise and fall time. Also, disable REFCLK on the deserializer and try using the internal clock.
6. Shield the camera serializer board and connect the shield to a solid ground
7. Change the cable to a better-shielded coaxial cable, such as DACAR 302 instead of DACAR 462.
8. Change the forward-channel data rate by changing the back-channel reference clock (REFCLK in Figure 1) applied to the deserializer.

Once the sources of noise source have been identified, the following checklist will help implement a design.

Design guidelines/checklist

PCB board stack-up

- Select a printed circuit board (PCB) with at least four layers for FPD-Link construction, with the four layers consisting of two signal and two power or ground planes.
- Use dedicated ground and power planes: power/ground planes make an excellent high-frequency capacitor and act as an additional high-frequency bypassing capacitor in complement with traditional (discrete) components. The use of a solid ground plane is highly recommended. A solid plane minimizes inductance, which is a desirable trait for high-speed signals (both analog and digital signals) and also acts as low-impedance path for return current.
- Keep the power and ground plane surface area equivalent in size/shape.
- Keep the power and ground shapes on top of each other for optimal board capacitance.
- Use ground pours on the top and bottom layers. Use evenly-spaced ground pores around differential traces.

Table 1. Example step-by-step methodology to identify the root causes of EMI

Step No.	Imager	Serializer	Deserializer	Other System Components	Comments
1	Off	Off	Off	On	Captures ambient noise, including PoC switching noise
2	Off	On	Off	Off	953 by itself
3	Off	Off	On	Off	954 by itself
4	On	Forward driver disabled	On	Off	Imager by itself – everything is on except for the forward channel; the back channel is on
5	On	On	On	On	Slow down reference-clock rise and fall times by putting capacitance at the clock pin
6	On	On	On	On	Shield the camera serializer board, connect the shield to a solid ground
7	On	On	On	On	Change to a better-shielded coaxial cable such as DACAR 302 instead of DACAR 462
8	On	On	On	On	Change the forward-channel speed by changing the back-channel reference clock

Interfaces

- The geometry of copper determines the characteristic impedance (Z_O) of the signal trace. The trace Z_O depends on its mutual inductance and capacitance, as determined by its dimensions and the PCB dielectric (ε_r). Keep the impedance matched across transitions such as connectors. Use a time-domain reflectometer (TDR) to verify.
- Keep single-ended inputs/outputs away from differential traces—at least 2× the trace width.
- A 50-Ω impedance for single-ended signal traces is recommended.
- Power/ground traces should be wide to provide a low impedance path. Do not route power/ground traces as 50-Ω traces.

FPD-Link differential high-speed signal traces

- Route high-speed FPD-Link signals with the most direct route and minimum trace length to the connector.
- Minimize stub lengths: they are the most critical and sensitive links in the system.
- Maintain a 100-Ω (±5% total) differential impedance of microstrip or stripline: A microstrip line is on either the top or bottom layer of a PCB. Microstrip construction consists of a differential pair and a single reference layer (typically ground). In contrast, striplines are embedded between two reference layers, which results in a higher capacitance versus microstrip lines (when comparing identical geometries). There are generally longer propagation delays compared to microstrip lines. Also, striplines require an additional layer, which may increase cost. On the other hand, striplines usually have better EMI and EMC performance.
- Avoid routing high-speed frequency traces through the vias. PCB via capacitance and inductance are dictated by the via's geometry. The parasitic-capacitance of vias often limit their impedance to a range between 20 and 30 Ω. The impedance mismatch between vias and signal traces can cause transmission-line reflections. As an example, a 0.4-mm via in a 1.6-mm thick PCB can have 1.2 nH of inductance, and a 1.6-mm clearance hole around a 0.80-mm pad on FR-4 can have 0.4 pF of capacitance.
- Bury longer high-speed traces in an inner signal layer. For example, in a four-layer PCB board, the high-speed trace can be on either the second or third layer. Construct high-speed vias with controlled impedance.
- Keep signals within a differential pair closely coupled to minimize the noise injection and radiated electromagnetic field from other signals.
- Minimize intrapair skew; keep differential skew to ±30 ps. Avoid serpentining one side of the differential pair to match skew. Phase differences between the differential lines increase radiation and decrease the eye opening. Trace layout, connectors or cable wires can cause skew, while strong coupling within differential pairs reduces it. If using a shielded twisted-pair (STP) cable, keep the intrapair skew associated with STP cables in mind.
- Minimize stubs and junction taps in order to avoid reflections.
- Use a continuous ground plane underneath the traces.
- 45-degree corners are acceptable, but rounded corners are best. Avoid asymmetric meanders. Do not route traces at right angles to component pins or other traces. Avoid right-angle traces, as they are known to cause more radiation.
- Use small-sized AC-coupling capacitors (0603 or smaller) to minimize pad discontinuity. Also, 0201 decoupling filter capacitors can be used.

Power and grounding

- Use a solid ground plane and avoid vias with transmission lines.
- Separate digital and analog power supplies with filtering and bypassing.
- Put the largest-value filter capacitors near power-connector and supply inputs.
- Place high-quality X7R decoupling capacitors close to device pins. Use multiple capacitors (such as 0.1 µF, 0.01 µF, 1 µF) in parallel to offer low impedance over higher frequency ranges.
- Place the smallest-value capacitors closest to the power pin.
- Use a ferrite bead to decouple the integrated circuit (IC) power from the rest of the supply system.
- Keep the traces from decoupling caps to ground as short and wide as possible. Connect power and ground as soon as possible to the power and ground planes, using multiple vias to reduce inductance.
- Ensure that bypass capacitors are on the same layer as the device for best results; do not place capacitors on the opposite side of the board.
- Do not make ground or power connections with controlled impedance traces. Use wide, low-impedance traces for power and ground.
- Use an inductor or ferrite beads to split power and minimize noise coupling.
- Do not place vias between bypass capacitors and the IC.
- More vias means lower inductance. The use of multiple vias for both power and ground connections is highly recommended.
- Minimize current loops. The return current takes the lowest impedance path. At high frequencies, the return current tends to flow directly beneath the signal path. Current loops in the layout generate noise; this noise can be minimized by keeping loops as small as possible to improve both EMI and ESD performance. A solid ground plane provides a continuous, low-impedance path for return currents of high-speed signals.

Connectors and cables

- Keep differential pairs close and monitor their electrical length.
- Use shielded high-speed connectors that have complete shielding around the connector interface, such as Rosenberger high-speed data (HSD)-type connectors (D4S20A-40ML5-Z or D4S10A-400L5-Y) or equivalent. Coax and STP connectors are acceptable.

Conclusion

Designers should follow the best practices listed in this article to simplify the emissions testing process. If issues are encountered, consider following the step-by-step testing methodology listed in Table 1 to help pinpoint sources of emissions. Explore TI's FPD-Link III SerDes products to simplify your system design process to operate reliably without EMI issues.

References

1. Ankur Verma and Brian Rodriguez, "Electrical design considerations for industrial resolver sensing applications," TI White Paper (SLYY100), June 2016.
2. Ankur Verma, "How to reduce total harmonic distortion to below 10%," TI E2E™ Community Power House blog, May 28, 2013.
3. Ankur Verma and Anand Chellamuthu, "Design considerations for resolver-to-digital converters in electric vehicles," Texas Instruments Analog Applications Journal (SLYT661), 1Q 2016.
4. Mark Sauerwald, "Ten tips for successfully designing with automotive EMC/EMI requirements," Texas Instruments Analog Applications Journal (SLYT636), 3Q 2015.
5. "MSP430™ System-Level ESD Considerations," Texas Instruments Application Report (SLAA530), March 2012.
6. CISPR 25 specification, ANSI eStandards Store

Related Web sites

Product information:
FPD-Link III SerDes products
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