Maximizing the dynamic range of analog front ends having a transimpedance amplifier

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Introduction

Optical-pulsed time-of-flight (ToF) systems find wide usage in robotic vision, laser-distance measurement, light detection and ranging (LIDAR), and position and proximity sensing. Maximizing the analog front-end's signal-to-noise ratio (SNR) increases the system's dynamic range, which can result in improved target resolution, a lower variance in the target's absolute position, and the ability to "see" farther. To produce a best-in-class system, the primary goals are to optimize the optics, the analog front-end, and the digital post-processing subsystems.

The analog front-end subsystem typically consists of three components:

- The transimpedance amplifier (TIA), which converts the output current from a photodiode (PD) or avalanche photodiode (APD) into a voltage.
- A differential amplifier, which converts the single-ended output of a TIA into a differential output and adjusts the common-mode output voltage to match the subsequent analog-to-digital converter's (ADC) common-mode input range.
- An ADC, which digitizes the analog output of the amplifier front end.

This article describes various factors that should be considered when setting various DC bias levels in a pulsed ToF system to maximize the signal's dynamic range.

PD and bias configurations

High-speed optical signal chains can have their PD or APD configured in two different ways:

- A PD cathode biased to a positive voltage relative to the anode, which is tied to the TIA inverting terminal, as shown in Figure 1. In this configuration, the PD will source an output current.
- A PD anode biased to a negative voltage relative to the cathode, which is tied to the TIA inverting terminal, as shown in Figure 2. In this configuration, the PD will sink an output current.

In both Figures 1 and 2, the interface between the PD and the TIA can be DC coupled or it can be AC coupled to eliminate the DC offset due to ambient light. Irrespective of whether the interface between the PD and the TIA is AC or DC coupled, the common-mode output voltage of the TIA stage is set to its noninverting bias voltage (V_{CM_TIA}).

Figure 1. Analog front-end for optical signal chain with cathode bias

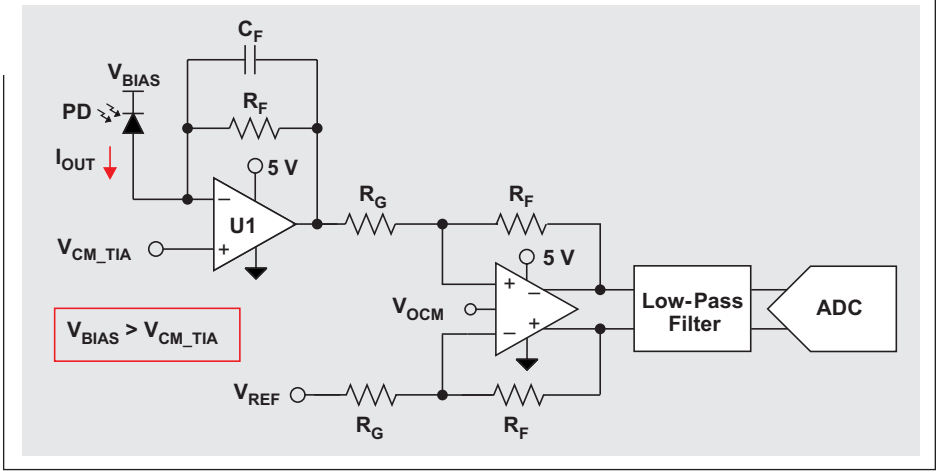
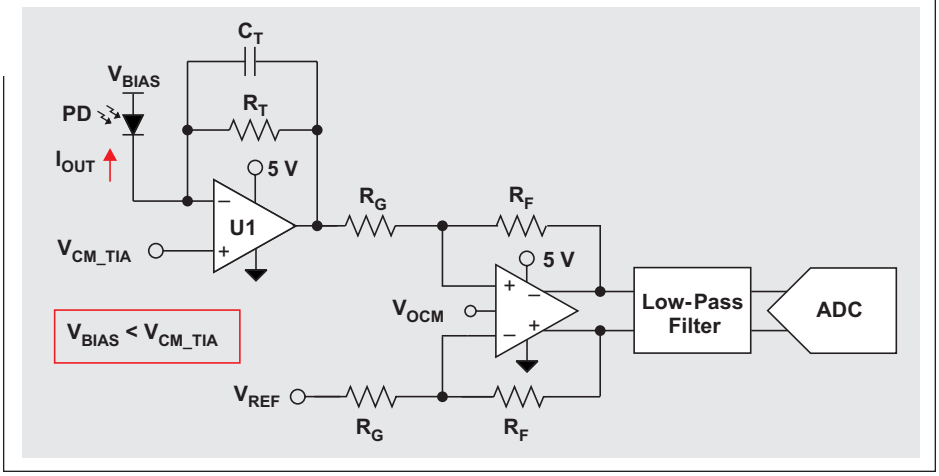


Figure 2. Analog front-end for optical signal chain with anode bias



TIA common-mode configurations

With the PD configured as shown in Figure 3, the output of the TIA will swing in a negative direction relative to V_{CM_TIA}. To maximize the output swing of the TIA, set V_{CM_TIA} at the lower compliance limit of the TIA's positive common-mode input voltage and its most positive output swing.

For example, in the case of the Texas Instruments (TI) OPA855, V_{CM_TIA} should be set to 3.95 V when the amplifier is configured with a 5-V positive supply and a 0-V negative supply. See Tables 1 and 2. In this case, the maximum output swing is 3.95 V – 1.15 V = 2.8 V.

When configuring the PD as shown in Figure 4, the output of the TIA will swing in a positive direction relative to V_{CM_TIA}. To maximize the output swing of the TIA, set V_{CM_TIA} at the higher compliance limit of its negative common-mode input voltage and the TIAs most negative output swing.

For example, for the OPA855 (see Tables 1 and 2), V_{CM_TIA} should be set to 1.3 V when the amplifier's supplies are at 5 V and ground. In this case, the maximum output swing is 4.1 V – 1.3 V = 2.8 V.

Add sufficient guardband when setting V_{CM_TIA} to account for amplifier process and temperature variances. In addition, if V_{CM_TIA} is set with a resistive divider between the voltage supplies, be sure to account for any resistor tolerances as well as voltage-supply variance and drift. If a resistive divider is used to set V_{CM_TIA}, add a noise bypass capacitor (C_{BYP}) to ground on the amplifier's noninverting input to bypass the high-frequency noise generated by the resistors.

Differential amplifier to ADC interface

For the remainder of this discussion, assume that the PD is configured as shown in Figure 3. Also assume that the TI THS4541 is used as the differential amplifier configured in a gain of 2 V/V, and the TI ADC32J23 is the ADC.

Figure 3. TIA configuration with cathode bias

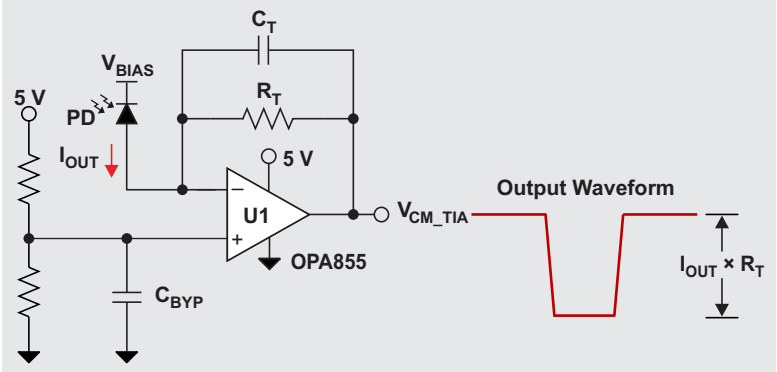


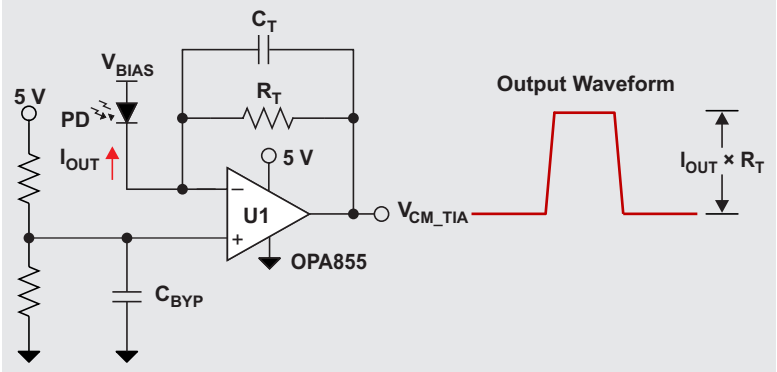
Table 1. OPA855 common-mode input range

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input					
V_{IH}, the common-mode voltage range (high)	Common-mode rejection ratio (CMRR) > 80 dB	4.4	4.6		V
V_{IL}, the common-mode voltage range (low)	CMRR > 80 dB		1.1	1.3	V

Table 2. OPA855 output swing range

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output					
V_{OH}, the output voltage (high)	T_A = 25°C	3.95	4.1		V
V_{OL}, the output voltage (low)	T_A = 25°C		1.05	1.15	V

Figure 4. TIA configuration with anode bias



The ADC32J23's common-mode input is specified at 0.95 V and its differential input signal range is 2 V_{PP}. Under these conditions, the linear input range of each ADC input is 0.95 V ± 0.5 V = 1.45 V and 0.45 V, as shown in Figure 5.

To level-translate the common-mode output voltage of the differential amplifier stage to match the ADC's required common-mode input range, simply set the V_{OCM} pin of the THS4541 to 0.95 V.

When converting a single-ended bipolar input to a differential output, the common-mode input voltage for each half of the differential amplifier stage should be equal. In Figure 5, V_{ICM} should be equal to V_{REF}.

As stated earlier, the output of a TIA is unipolar with respect to V_{CM_TIA}. This is because the output of a PD is unipolar. When no light is incident on the PD, it generates zero output current. When light is incident on the PD, it generates a proportional output current depending on its reverse bias configuration

If the differential amplifier were configured such that $V_{CM\_TIA} = V_{REF}$, then the resulting output pulse of the THS4541 will be as shown in Figure 6. When no light is incident on the PD, each output of the THS4541 will be at midscale, or in other words, the V_{OCM} voltage (0.95 V). When light is incident on the PD, each output of the THS4541 will move in opposite directions such that the instantaneous average voltage of the two outputs is always at V_{OCM}.

If the ADC digitizes the THS4541's output, then under no-light conditions, the ADC32J23 output will be at midscale. When a large optical pulse is incident on the PD, the output will be at positive full scale. In Figure 6, the circuit uses only half the dynamic range of the ADC; the red signal never goes below 0.95 V and the green signal never goes above 0.95 V. In other words, the ADC bits between midscale and negative full-scale are never exercised in this configuration. This is akin to losing 1 bit of ADC resolution.

Figure 5. Interface of differential amplifier to the ADC

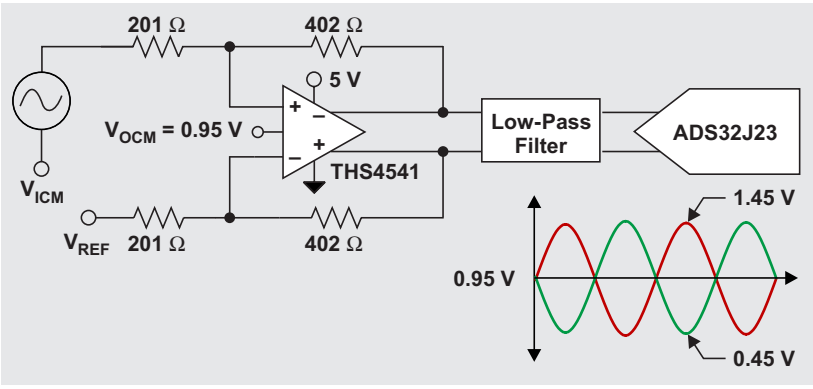
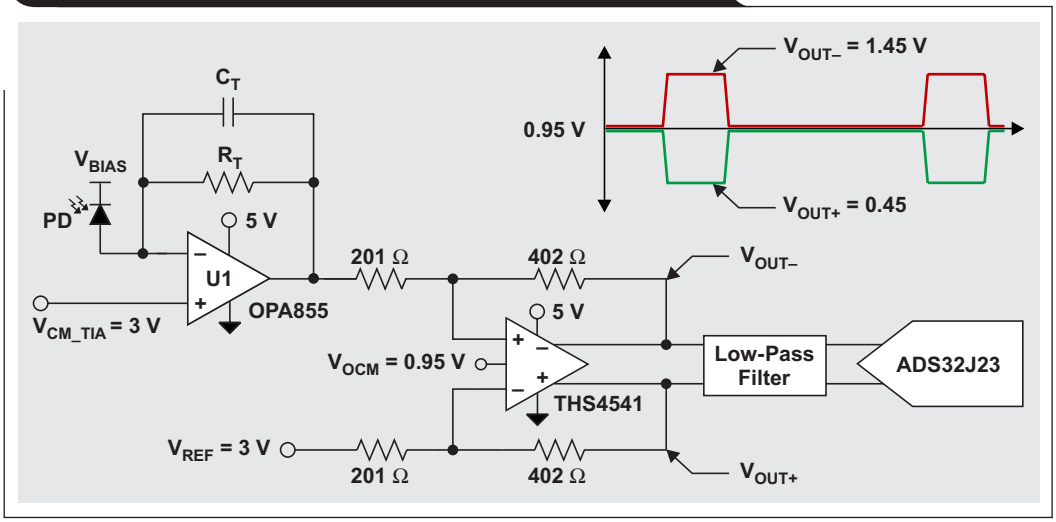


Figure 6. Signal-chain performance with $V_{CM\_TIA} = V_{REF}$



To recover the lost ADC bit, the THS4541 can be configured such that under no-light conditions, its individual outputs are offset so as to produce a negative full-scale output from the ADC32J23, as shown in Figure 7. Under these conditions, the output of the THS4541 now has 2x the linear swing range compared to Figure 6, thus improving the signal-to-noise ratio (SNR) of the system by 6 dB.

To achieve the differential output shown in Figure 7, the DC bias on the non-signal side (V_{REF}) of the THS4541 should be offset versus V_{CM_TIA}. This relationship is used to calculate V_{REF}.

With $\left(V_{CM\_TIA} - V_{REF}\right) \times G = \frac{\text{ADC full-scale range}}{2}$,

then $$V_{REF} = V_{CM\_TIA} - \left(\frac{\text{ADC full-scale range}}{2 \times G}\right) \quad (1)$$

where the differential amplifier gain,
$G = R_F / R_G = 402\ \Omega / 201\ \Omega = 2$ V/V.

When the PD is biased as shown in Figure 4, Equation 2 sets V_{REF}.

$$V_{REF} = V_{CM\_TIA} + \left(\frac{\text{ADC full-scale range}}{2 \times G}\right) \quad (2)$$

Returning to the example using Equation 1, if the THS4541 is configured in a gain of 2 V/V and V_{CM_TIA} = 3 V, then:

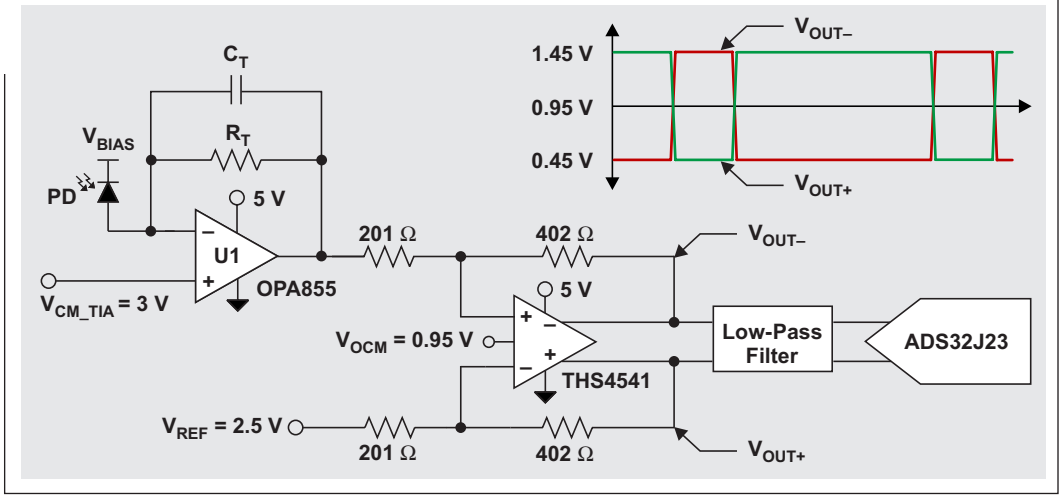
$$V_{REF} = 3\ V - \left(\frac{2\ V_{PP}}{2 \times 2}\right) = 2.5\ V$$

The offset voltage is not affected by the differential amplifier's V_{OCM} settings as long as the voltage is within the THS4541's input and output compliance limits.

Configuring the V_{REF} buffer circuit

A buffered resistor-divider can be used to set V_{REF}. The closed-loop bandwidth of the circuit used to set V_{REF} should be approximately 10x greater than the closed-loop bandwidth of the TIA. The V_{REF} circuit that sets the DC offset of the signal chain should have low output impedance across the frequency range of interest to minimize balance and gain errors. Using the same amplifier for both the transimpedance stage, as well as the DC offset stage, typically ensures low output impedance across frequency.

Figure 7. Signal-chain performance with offset differential-amplifier outputs under no-light conditions



To save power, an amplifier with lower bandwidth can be used to set the DC bias. However, to ensure low impedance across frequency, it's best to use an AC bypass capacitor, as shown in Figure 8. Since most operational amplifiers cannot directly drive large capacitors, a series isolation resistor will be required to maintain stability. The circuit shown in Figure 8 ensures stability and balance.

The amplifier used to set the DC offset will also introduce noise. The appropriate noise analysis should be performed to ensure that the added buffer does not degrade the overall system SNR. The total noise in optical signal chains is typically dominated by the TIA stage, and the noise added in the buffer and differential amplifier stage is relatively minor.

AC coupling between the TIA and differential amplifier stages

If the signal path between the TIA and differential amplifier stages is AC coupled, the differential output offset of the THS4541 is 0 V, and the system will lose 1 bit of ADC resolution. To regain the lost bit, use the circuit shown in Figure 9, where V_{B1} and V_{B2} are two DC bias voltages. These voltages, along with R_{G2}, recreate the differential offset at the THS4541's outputs.

Figure 8. V_{REF} drive circuit using a low-bandwidth U2 buffer

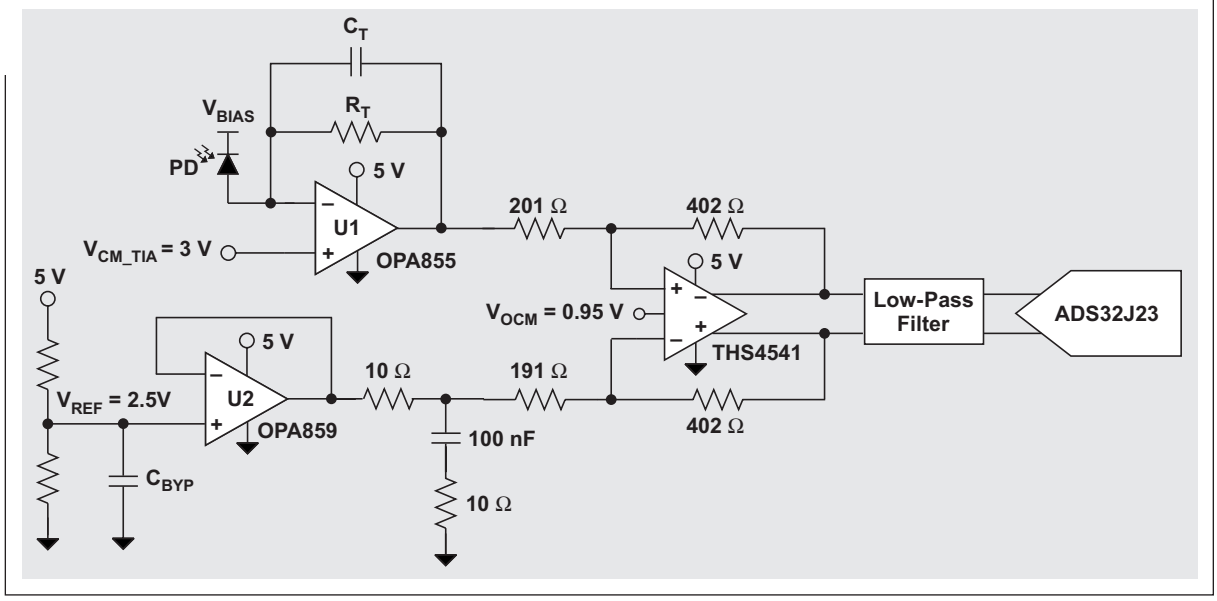
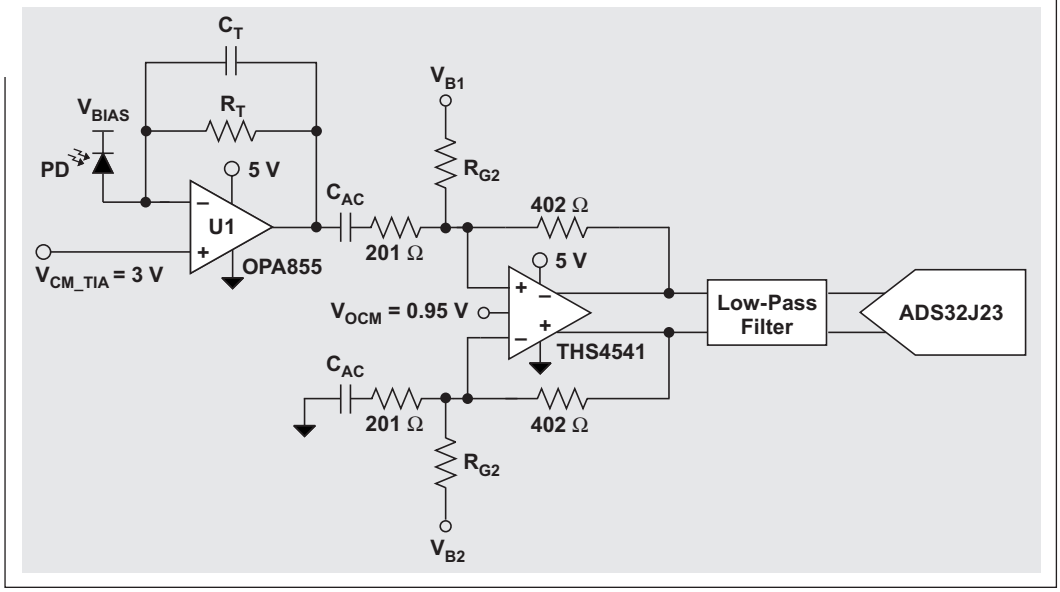


Figure 9. DC offset circuit with AC coupling between the TIA and the differential-amplifier



The V_{B1} and V_{B2} voltages can usually be set to the supply voltage and ground respectively, and adjust R_{G2} accordingly to create the specified DC offset. For example, if $V_{B1} = V_{CC} = 5$ V and $V_{B2} = 0$ V, then R_{G2} can be calculated.

$$\text{With} \quad \left(V_{B1} - V_{B2}\right) \times \left(\frac{R_F}{R_{G2}}\right) = \frac{\text{ADC full-scale range}}{2},$$

$$\text{then} \quad R_{G2} = \frac{\left(V_{B1} - V_{B2}\right) \times R_F}{\left(\frac{\text{ADC full-scale range}}{2}\right)} \quad (3)$$

$$= \frac{\left(5\,\text{V} - 0\,\text{V}\right) \times 402\ \Omega}{\left(\frac{2\,V_{PP}}{2}\right)} = 2010\ \Omega$$

When the PD is biased as shown in Figure 4, set $V_{B2} = V_{CC} = 5$ V and V_{B1} = ground.

If the path between the THS4541 output and the ADC input is AC coupled, the signal chain will still lose 1 bit of resolution. It is generally not recommended to AC couple the final stage between the amplifier and the ADC. If AC coupling between the differential amplifier and the ADC is inevitable, pull-up and pull-down resistors (R_{G2}) similar to Figure 9 can be used at the ADC inputs to create a DC offset.

Conclusion

This article provided qualitative analysis and theoretical equations on setting the DC bias levels at the different amplifier stages in an optical signal chain to maximize the ADC dynamic range. Here are some key takeaways:

- Account for resistor and voltage-supply tolerances when setting DC bias levels and set guardbands accordingly to prevent saturation in any of the analog stages.
- Similarly, the TIA and differential-amplifier offset voltage, bias current and DC drift performance should be accounted for when setting the DC bias.
- Pay careful attention to the various error sources and set the DC bias levels accordingly. This will result in properly utilizing all the ADC bits without saturating the signal chain due to temperature and part-to-part variations.

Related Web sites

Product information:
OPA855, THS4541, ADC32J23

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