Texas
Instruments
Incorporated

UC1846-SP
5962-8680603V2A
5962-8680603VEA

Radiation Test Report

5962-8680603VEA (UC1846J-SP) Radiation Testing

Note: The following radiation test results are provided for information only, as these devices are not Radiation Hardness Assured (RHA) at this time.

Samples of the 5962-8680603VEA, UC1846J-SP, device have been evaluated to determine performance effects after Total Ionizing Dose (TID) radiation exposure. The initial radiation test plan for this device involved testing 40 units at a dose rate of 10 mrad/second, with samples pulled at various total dose intervals. Twenty samples were exposed under unbiased conditions, and 20 samples were exposed under biased conditions. For the biased samples, the bias conditions were the same as the circuit used for burn-in.

The TID samples were pulled from the initial qualification lot after completing normal class-V processing (assembly, burn-in, full-temp testing), and serialized datalogs were collected at 25C before and after radiation exposure. The electrical testing results are included in the release documentation. The test results are summarized below.

Device Traceability Information Confirmed By: Date:	 Kevin Treece 10/20/2008
Full Device Name:	5962-8680603VEA
Datecode or Lot Trace Code:	0827A
A/T Lot #:	8020888ALP
Full Die Name (Alias with Die Rev):	SMATRC1843VS
Die Lot #:	8124614SHE
Sample Size:	235

Summary: Units pass up to 40 krad(Si)

Dose rate requirement: 10 mrad(Si)/sec

Exposure groups by S/N:

Control – SN 230 (no radiation exposure)

Biased samples:
10krad(Si) – SN 251, 252*, 253, 254, 255
20krad(Si) – SN 256, 257, 258, 259, 260
30krad(Si) – SN 261*, 262, 263, 264, 265*
40krad(Si) – SN 266, 267, 268, 269, 270

Uniased samples:
10krad(Si) – SN 231, 232, 233, 234, 235
20krad(Si) – SN 236, 237, 238, 239, 240
30krad(Si) – SN 241, 242, 243, 244, 245
40krad(Si) – SN 246, 247, 248, 249, 250

*** Note:** Unit #252, from the 10krad sample, and unit #s 261 and 265, from the 30krad sample, failed post radiation electrical testing with several gross parametric test failures. Failure analysis results showed the failures were due to electrical overstress. These devices were removed from the electrical test data.

prerad

Units: 38

Parameter		Cpk (LL)	Lower Limit	-6 Sigma	Min	Ave	Max	Sigma	Skew	Kurt	+6 Sigma	Upper Limit	Cpk (UL)
25'C QA				27	27	27	27	0	#DIV/0!	#DIV/0!	27		
Standby Supply Current; Vin15V	m a			12.2944238	12.7178	13.0214763	13.2336	0.12117542	-0.32	-0.2426	13.7485288	20.6	20.847252
Reference Output Voltage; Il1mA	v	1.79663777	5.05	5.04153127	5.0997	5.12481842	5.1499	0.01388119	-0.1273	-0.8888	5.20810557	5.15	0.604693
Reference Line Reg; Vin8-40V	m v	9.18070464	-19	-0.0289658	3.8863	5.25492632	7.7574	0.88064868	1.1549	1.0576	10.5388184	19	5.20263224
>Reference Load Reg; Il1-10mA	m v	11.9620708	-14	-4.0116628	-2.5399	-2.0063895	-1.377	0.33421221	0.093	-1.1136	-0.0011162		
Reference Short Circuit Current	m a	97.7713812	-147	-47.041565	-45.5928	-44.954126	-44.1371	0.34790642	0.0871	-0.1373	-42.866688	-13	30.6156335
*Oscillator Discharge Current	m a	15.0292177	3.02	7.70798836	8.1365	8.4276	8.7671	0.11993527	-0.0902	1.6989	9.14721164	17.98	26.5487646
INITIAL READING	k hz	2.51551009	39.25	40.5280435	41.9372	45.4864079	46.4201	0.82639407	-3.2352	11.798	50.4447723	46.75	0.50968101
Oscillator Accuracy; 10K, 4.7nF	k hz	2.51551009	39.25	40.5280435	41.9372	45.4864079	46.4201	0.82639407	-3.2352	11.798	50.4447723	46.75	0.50968101
Oscillator Voltage Stab; Vin8-40V	%	15.6427767	-1.94	0.85781969	0.9947	1.26797368	1.3877	0.068359	-2.0335	7.1359	1.67812768	1.94	3.27694632
*Ct Leakage; Ct2.5V, RtVref	u a	40.0132726	-19	-0.524435	0.0255	0.44762368	0.7045	0.16200977	-0.6972	-0.0426	1.41968233	19	38.1713109
SYNC Output High Level; Il-1.3mA	v	9.07652926	3.91	4.19677222	4.2551	4.27782105	4.303	0.01350814	-0.0264	-0.9065	4.35886989	5.09	20.0417185
SYNC Output Low Level; Il0mA	v			2.13119422	2.177	2.20202368	2.2276	0.01180491	-0.1958	-0.1283	2.27285315	2.48	7.84917196
SYNC Input Current; 5.25V,RTVREF,CT0	m a			1.15417357	1.1821	1.20272368	1.2169	0.00809169	-0.5665	0.2144	1.2512738	1.49	11.8342186
*SYNC Leakage Current; 0.5V,Vref0	m a	546.563279	-1.5	0.04128149	0.0452	0.04694211	0.0486	0.00094344	0.0416	-0.9503	0.05260272	1.49	509.859064
SYNC In High/Low Thresh.; CT0	v	15.4154324	2.51	2.92838431	2.9716	2.99075789	3.0197	0.0103956	0.9032	1.0389	3.05313148	3.89	28.834068
E/A Input Offset Voltage	m v	3.67109191	-4.9	-3.0559285	-2.0028	-0.8489026	0.1206	0.36783764	-0.6183	3.661	1.35812322	4.9	5.20963779
E/A Avol; Vout1.2-3V, Vcm2V	db	5.94123747	82	99.2161063	105.2635	107.952503	112.9897	1.45606606	0.8003	2.654	116.688899		
E/A PSRR; Vin8-40V	db	7.7252204	82	91.041986	93.0707	94.2006368	95.4462	0.5264418	-0.1426	0.0089	97.3592877		
E/A CMRR; Vcm0-38; Vin40V	db	1.95359104	77	75.9408425	108.8924	121.585374	140.0091	7.60742187	0.8312	0.9474	167.229905		
E/A Input Bias Current	u a	74.6889438	-0.98	0.13507454	0.1565	0.16575526	0.1815	0.00511345	0.8595	1.3614	0.19643598	0.98	53.0785948
E/A Input Offset Current	n a	85.6344626	-245	-4.5511009	-0.6091	1.19889474	3.2889	0.95833261	0.4297	-0.1209	6.94889041	245	84.8004482
E/A Output Sink Current; COMP1.2V	m a	10.0685679	2.04	7.72440032	8.6403	9.13342368	9.826	0.23483723	0.252	1.2502	10.542447		
E/A Output Source Current; COMP2.5V	m a			-0.5989772	-0.5705	-0.5573842	-0.532	0.00693216	1.1283	3.6817	-0.5157912	-0.408	7.18314606
E/A Output High Level; Rl15K	v	11.1371905	4.31	4.64261183	4.6942	4.71541579	4.7357	0.01213399	-0.1016	-0.9846	4.78821975		
E/A Output Low Level; Rl15K	v			0.70836228	0.7284	0.73893421	0.7491	0.00509532	0.0685	-0.3358	0.76950615	0.97	15.1162031
C/L ADJ Offset Voltage	v	3.57298515	0.453	0.4710025	0.4863	0.49389211	0.5041	0.00381493	0.3753	0.2883	0.51678171	0.547	4.64035094
C/L ADJ Input Bias Current; 0V	u a	40.5605722	-29.4	-7.995952	-7.348	-6.8858	-6.4298	0.18502533	0.0894	0.8061	-5.775648	29.4	65.3708686
*C/L ADJ Input Bias Current; 5V	u a	1120.76129	-29.4	0.33672938	0.3725	0.38988947	0.4069	0.00886002	0.0834	-0.5421	0.44304957	29.4	1091.42429
*PWM Latch Test Output A	%			7.37111171	7.6271	8.31366316	8.4779	0.15709191	-3.4762	13.012	9.25621461	25	35.4067394
*PWM Latch Test Output B	%			7.39632857	7.6751	8.32487105	8.4906	0.15475708	-3.2705	11.641	9.25341354	25	35.9167819
C/S AMP Input Offset Voltage	m v	4.00777591	-23.4	-13.068784	-7.1147	-2.7775789	0.4822	1.71520078	-0.4886	0.2011	7.51362571	23.4	5.08736923
C/S AMP CMRR; Vcm1-12V	db	11.0837491	63	80.5613304	83.241	84.4278684	86.0034	0.644423	0.2116	-0.0494	88.2944064		
C/S AMP PSRR; Vin8-40V	db	3.24042251	63	73.2854175	84.6105	89.86915	95.4058	2.76395541	0.0885	-0.702	106.452882		
C/S AMP Input Bias Current	u a	134.916263	-9.7	0.81175263	0.9177	0.96992368	1.0415	0.02636184	0.3774	0.5711	1.12809474	9.7	110.387788
C/S AMP Input Offset Current	u a	23.667744	-0.7	-0.0719114	-0.0418	-0.0139368	0.0095	0.00966242	-0.1971	1.325	0.04403769	0.7	24.6293278
C/S AMP Gain	v	3.40229826	2.515	2.6137844	2.7061	2.75467368	2.8013	0.02348155	-0.0143	-0.2858	2.89556297	2.985	3.26960728
C/S AMP Max Diff Input	v	3.6352269	1.12	1.18266578	1.2355	1.25931053	1.2842	0.01277412	-0.035	-0.6479	1.33595528		
Shutdown Threshold Voltage	m v	7.75732204	254	333.370044	347.3827	360.941905	370.674	4.59531029	-0.0493	1.3218	388.513767	396	2.54303428
Shutdown Latching Voltage; 3mA	v			0.08685957	0.1115	0.12321579	0.1365	0.00605937	0.1959	-0.105	0.15957201	1.995	102.969139
Shutdown NonLatching Volt; 0.8mA	v	1161.70976	5.01	6.08746552	6.0884	6.08932368	6.0899	0.00030969	-0.2513	0.487	6.09118185	7	980.189333
*Shutdown Input Bias Current; 0V	m a	326.1506	-1	-0.0190367	-0.0151	-0.0129842	-0.0114	0.00100875	-0.1319	-0.8632	-0.0069317	0.99	331.427223
*Shutdown Input Bias Current; 15V	m a	32.4016184	1	2.57222739	2.6401	2.67565789	2.7163	0.01723842	-0.3081	-0.1162	2.7790884	4.99	44.7516346
Collector Leakage Current; Vc40V	u a			77.5299437	82.7425	86.7353105	88.9072	1.53422781	-0.7245	-0.0173	95.9406774	170	18.0904663
Output A Low; Il20mA	v			0.09259894	0.1239	0.14047105	0.1592	0.00797868	0.0724	0.3182	0.18834316	0.392	10.5083714

prerad

Units: 38

Parameter		Cpk (LL)	Lower Limit	-6 Sigma	Min	Ave	Max	Sigma	Skew	Kurt	+6 Sigma	Upper Limit	Cpk (UL)
>Output A Low; Il100mA	v			0.54188164	0.6647	0.73418421	0.8035	0.03205043	0.1097	0.2569	0.92648679	2.09	14.1008594
>Output B Low; Il100mA	v			0.55395454	0.6628	0.72352368	0.8252	0.02826152	1.0724	3.766	0.89309283	2.09	16.1170396
Output B Low; Il20mA	v			0.09564839	0.1232	0.13785789	0.1594	0.00703492	0.6573	1.7632	0.1800674	0.392	12.0419364
Output B High; Il-20mA	v	44.9076241	13.045	13.5155158	13.5266	13.5374474	13.5469	0.00365526	-0.1341	1.8104	13.5593789		
>Output B High; Il-100mA	v	68.0950089	12.03	13.3063954	13.3344	13.3450184	13.3595	0.00643717	0.3079	-0.6303	13.3836415		
Output A High; Il-20mA	v	33.5626948	13.045	13.5056698	13.5224	13.5348605	13.5474	0.00486513	0.0081	0.9671	13.5640513		
>Output A High; Il-100mA	v	29.4418096	12.03	13.2433434	13.2898	13.3317737	13.3616	0.01473838	-0.4417	0.7381	13.420204		
*PWM Output A Minimum Duty Cycle	%			0	0	0	0	0	#DIV/0!	#DIV/0!	0	0.001	Infinite
*PWM Output B Minimum Duty Cycle	%			0	0	0	0	0	#DIV/0!	#DIV/0!	0	0.001	Infinite
*PWM Output A Maximum Duty Cycle	%	9.68803602	45.05	46.9496736	47.3273	47.4438632	47.7567	0.08236493	2.5079	8.1548	47.9380527		
*PWM Output B Maximum Duty Cycle	%	8.440662	45.05	46.8637218	47.282	47.4269316	47.7782	0.09386829	2.165	6.7555	47.9901413		
UVLO Start-up Threshold	v	28.9899421	6.01	7.69286528	7.7646	7.81756842	7.8551	0.02078386	-0.0866	0.0084	7.94227156	7.99	2.76547291
UVLO Threshold Hysterisis	v	66.6898401	0.11	0.80238323	0.8155	0.82378947	0.8315	0.00356771	0.1862	0.2228	0.84519572	2	109.894156

post10krad

Units: 9

Parameter		Cpk (LL)	Lower Limit	-6 Sigma	Min	Ave	Max	Sigma	Skew	Kurt	+6 Sigma	Upper Limit	Cpk (UL)
25'C QA				27	27	27	27	0	#DIV/0!	#DIV/0!	27		
Standby Supply Current; Vin15V	m a			12.5829155	12.9062	13.0610111	13.1375	0.0796826	-0.9608	0.1708	13.5391067	20.6	31.5375806
Reference Output Voltage; Il1mA	v	1.66559973	5.05	5.0344605	5.104	5.1274	5.1552	0.01548992	0.3326	0.0886	5.2203395	5.15	0.48633791
Reference Line Reg; Vin8-40V	m v	22.4017106	-19	2.51345867	4.1541	4.62244444	5.271	0.35149763	0.6233	-0.269	6.73143021	19	13.6345686
>Reference Load Reg; Il1-10mA	m v	10.4054153	-14	-4.400653	-2.5399	-2.1165667	-1.4995	0.38068105	0.6495	-1.2918	0.16751964		
Reference Short Circuit Current	m a	105.542367	-147	-46.865115	-45.4223	-44.930933	-44.5831	0.32236365	-0.4857	-1.4573	-42.996751	-13	33.0175086
*Oscillator Discharge Current	m a	25.1741555	3.02	8.02007808	8.3724	8.4516	8.5923	0.07192032	1.0772	0.4637	8.88312192	17.98	44.1618351
INITIAL READING	k hz	6.7233453	39.25	43.8781676	45.399	45.8378667	46.5242	0.32661651	1.1896	1.8306	47.7975657	46.75	0.93089124
Oscillator Accuracy; 10K, 4.7nF	k hz	6.7233453	39.25	43.8781676	45.399	45.8378667	46.5242	0.32661651	1.1896	1.8306	47.7975657	46.75	0.93089124
Oscillator Voltage Stab; Vin8-40V	%	59.4626427	-1.94	1.16574819	1.243	1.27384444	1.2964	0.01801604	-0.2724	-0.7167	1.3819407	1.94	12.3252293
*Ct Leakage; Ct2.5V, RtVref	u a	61.3131257	-19	-0.1859852	0.2891	0.44841111	0.6287	0.10573272	0.1477	-0.4709	1.08280745	19	58.4858009
SYNC Output High Level; Il-1.3mA	v	6.95448356	3.91	4.17124285	4.2572	4.2767	4.3133	0.01757619	1.0104	1.3475	4.38215715	5.09	15.4242746
SYNC Output Low Level; Il0mA	v			2.12269869	2.1827	2.20894444	2.2285	0.01437429	-0.7267	-0.0085	2.2951902	2.48	6.28565569
SYNC Input Current; 5.25V,RTVREF,CT0	m a			1.18121514	1.1986	1.20585556	1.2099	0.00410674	-1.0846	-0.2459	1.23049597	1.49	23.063285
*SYNC Leakage Current; 0.5V,Vref0	m a	486.034882	-1.5	0.0403797	0.0457	0.04674444	0.0485	0.00106079	0.7541	-1.2254	0.05310919	1.49	453.515476
SYNC In High/Low Thresh.; CT0	v	25.1446221	2.51	2.94550037	2.9758	2.98313333	2.9923	0.00627216	0.2476	-1.8087	3.0207663	3.89	48.1953353
E/A Input Offset Voltage	m v	2.74173853	-4.9	-3.8358984	-1.8455	-0.9666889	-0.4992	0.47820158	-1.2695	0.2523	1.90252061	4.9	4.08941132
E/A Avol; Vout1.2-3V, Vcm2V	db	9.34055679	82	103.020902	107.1346	108.748233	110.3286	0.95455528	-0.071	-0.0303	114.475565		
E/A PSRR; Vin8-40V	db	8.15804093	82	90.946065	93.0632	93.8515556	94.6871	0.48424843	-0.1083	0.27	96.7570461		
E/A CMRR; Vcm0-38; Vin40V	db	2.50148487	77	84.8284905	107.8349	116.049733	126.6494	5.20354048	0.6804	1.822	147.270976		
E/A Input Bias Current	u a	79.3808356	-0.98	0.16872105	0.1912	0.19841111	0.2041	0.00494834	-0.5459	-1.3338	0.22810118	0.98	52.6498592
E/A Input Offset Current	n a	56.8238065	-245	-7.2792716	-1.2171	1.3929	3.773	1.44536193	-0.2305	0.6515	10.0650716	245	56.1813376
E/A Output Sink Current; COMP1.2V	m a	12.8959703	2.04	8.09614715	8.9168	9.20777778	9.5209	0.18527177	0.22	-0.1544	10.3194084		
E/A Output Source Current; COMP2.5V	m a			-0.5794119	-0.5608	-0.5545889	-0.5487	0.00413716	0.1321	-0.5826	-0.5297659	-0.408	11.8107438
E/A Output High Level; Rl15K	v	9.84798528	4.31	4.63506958	4.6983	4.71791111	4.7402	0.01380692	0.2294	-0.5861	4.80075265		
E/A Output Low Level; Rl15K	v			0.71927134	0.7325	0.73654444	0.7425	0.00287885	0.8549	1.6784	0.75381754	0.97	27.0311119
C/L ADJ Offset Voltage	v	4.83165616	0.453	0.47583042	0.4883	0.49195556	0.4963	0.00268752	0.2266	-0.7394	0.50808069	0.547	6.82716048
C/L ADJ Input Bias Current; 0V	u a	26.6275569	-29.4	-9.2248229	-7.9331	-7.5864	-7.1993	0.27307049	-0.0026	-1.4545	-5.9479771	29.4	45.1487819
*C/L ADJ Input Bias Current; 5V	u a	669.254569	-29.4	0.30216092	0.3664	0.39118889	0.4127	0.014838	-0.4181	-0.4977	0.48021686	29.4	651.67857
*PWM Latch Test Output A	%			7.97825361	8.3455	8.40175556	8.553	0.07058366	1.5738	1.7938	8.8252575	25	78.3856817
*PWM Latch Test Output B	%			8.14570575	8.3659	8.40894444	8.5075	0.04387312	1.5416	2.8432	8.67218314	25	126.053319
C/S AMP Input Offset Voltage	m v	5.68600278	-23.4	-9.5785263	-4.0956	-2.0790889	-0.1567	1.24990624	-0.0499	-0.4762	5.42034857	23.4	6.79493336
C/S AMP CMRR; Vcm1-12V	db	7.63032927	63	79.2107951	83.5648	84.9691778	86.3668	0.95973044	-0.095	-1.2006	90.7275604		
C/S AMP PSRR; Vin8-40V	db	4.63090138	63	77.7292142	86.4968	88.9263	91.7242	1.86618096	0.0867	-1.4497	100.123386		
C/S AMP Input Bias Current	u a	120.085264	-9.7	1.05788354	1.1947	1.24008889	1.2896	0.03036756	-0.0784	-0.1287	1.42229424	9.7	92.8612805
C/S AMP Input Offset Current	u a	25.728726	-0.7	-0.0859656	-0.0427	-0.0342111	-0.021	0.00862575	0.6633	-1.6256	0.01754341	0.7	28.3728323
C/S AMP Gain	v	3.96751057	2.515	2.63416611	2.7289	2.7553	2.7917	0.02018898	0.5768	-0.4643	2.87643389	2.985	3.79249762
C/S AMP Max Diff Input	v	4.07906909	1.12	1.19091515	1.239	1.25913333	1.275	0.0113697	-0.4933	-0.2629	1.32735151		
Shutdown Threshold Voltage	m v	16.6857979	254	347.659127	358.0354	360.414189	364.6823	2.12584357	1.1225	0.8943	373.16925	396	5.57987294
Shutdown Latching Voltage; 3mA	v			0.09855349	0.1159	0.1204	0.1269	0.00364109	0.4167	-0.4264	0.14224651	1.995	171.615512
Shutdown NonLatching Volt; 0.8mA	v	662.366514	5.01	6.10857284	6.1112	6.1119	6.1131	0.00055453	0.9896	2.6675	6.11522716	7	533.848535
*Shutdown Input Bias Current; 0V	m a	461.549241	-1	-0.0167901	-0.0135	-0.0125111	-0.0113	0.00071317	0.4185	-0.8893	-0.0082321	0.99	468.570581
*Shutdown Input Bias Current; 15V	m a	55.0236649	1	2.62057357	2.6626	2.6817	2.6954	0.01018774	-0.8896	0.3836	2.74282643	4.99	75.525436
Collector Leakage Current; Vc40V	u a			68.665374	81.9039	86.5309889	90.9806	2.97760248	-0.0676	-0.9455	104.396604	170	9.3440961
Output A Low; Il20mA	v			0.10129469	0.1296	0.13573333	0.1437	0.00573977	0.5905	-1.7015	0.17017197	0.392	14.8825075

post10krad

Units: 9

Parameter		Cpk (LL)	Lower Limit	-6 Sigma	Min	Ave	Max	Sigma	Skew	Kurt	+6 Sigma	Upper Limit	Cpk (UL)
>Output A Low; Il100mA	v			0.5755435	0.6891	0.71401111	0.7489	0.02307794	0.7777	-1.183	0.85247872	2.09	19.8745231
>Output B Low; Il100mA	v			0.56962508	0.6974	0.72088889	0.7693	0.02521063	1.1227	0.2307	0.8721527	2.09	18.1022958
Output B Low; Il20mA	v			0.09870029	0.1296	0.13654444	0.1487	0.00630736	1.039	0.2439	0.1743886	0.392	13.5003972
Output B High; Il-20mA	v	30.4040176	13.045	13.4876746	13.512	13.5188444	13.527	0.00519498	-0.1864	-1.0116	13.5500143		
>Output B High; Il-100mA	v	53.0580879	12.03	13.2760893	13.3129	13.3249	13.3351	0.00813511	-0.3848	-1.4815	13.3737107		
Output A High; Il-20mA	v	28.1526867	13.045	13.485729	13.5126	13.5194333	13.5291	0.00561738	0.3545	-0.7125	13.5531376		
>Output A High; Il-100mA	v	42.4969559	12.03	13.2661509	13.3094	13.3272	13.3384	0.01017485	-1.0225	-0.0816	13.3882491		
*PWM Output A Minimum Duty Cycle	%			0	0	0	0	0	#DIV/0!	#DIV/0!	0	0.001	Infinite
*PWM Output B Minimum Duty Cycle	%			0	0	0	0	0	#DIV/0!	#DIV/0!	0	0.001	Infinite
*PWM Output A Maximum Duty Cycle	%	16.097677	45.05	47.1417686	47.339	47.4385222	47.5015	0.04945894	-0.952	0.8343	47.7352759		
*PWM Output B Maximum Duty Cycle	%	21.9311709	45.05	47.1833505	47.339	47.3974222	47.4564	0.03567863	-0.0999	-0.2304	47.611494		
UVLO Start-up Threshold	v	28.9273449	6.01	7.69764113	7.7955	7.82298889	7.862	0.02089129	0.5416	-0.111	7.94833665	7.99	2.66476427
UVLO Threshold Hysterisis	v	113.049145	0.11	0.81299459	0.8233	0.82565556	0.8294	0.00211016	0.6007	-0.8733	0.83831652	2	185.506329

post20krad

Units: 10

Parameter		Cpk (LL)	Lower Limit	-6 Sigma	Min	Ave	Max	Sigma	Skew	Kurt	+6 Sigma	Upper Limit	Cpk (UL)
25'C QA				27	27	27	27	0	#DIV/0!	#DIV/0!	27		
Standby Supply Current; Vin15V	m a			12.2388969	12.8573	13.04353	13.2323	0.13410552	0.0469	-1.6192	13.8481631	20.6	18.7823982
Reference Output Voltage; Il1mA	v	1.57554658	5.05	5.03211987	5.0997	5.11637	5.1412	0.01404169	0.5563	-0.5611	5.20062013	5.15	0.79833707
Reference Line Reg; Vin8-40V	m v	12.9763041	-19	1.0094451	3.7047	4.65538	5.7867	0.60765582	0.4168	0.1474	8.3013149	19	7.86882948
>Reference Load Reg; Il1-10mA	m v	19.2900864	-14	-3.3910513	-2.457	-2.16388	-1.9059	0.20452855	-0.1182	-1.6266	-0.9367087		
Reference Short Circuit Current	m a	91.9684513	-147	-47.11568	-45.4815	-44.89525	-44.4872	0.37007165	-0.5681	-1.3523	-42.67482	-13	28.728896
*Oscillator Discharge Current	m a	16.5960099	3.02	7.71636628	8.1689	8.35988	8.5056	0.10725229	-0.3788	-0.7762	9.00339372	17.98	29.8987255
INITIAL READING	k hz	12.7542844	39.25	44.6003353	45.3816	45.59535	45.9764	0.16583578	1.2848	2.5656	46.5903647	46.75	2.32087032
Oscillator Accuracy; 10K, 4.7nF	k hz	12.7542844	39.25	44.6003353	45.3816	45.59535	45.9764	0.16583578	1.2848	2.5656	46.5903647	46.75	2.32087032
Oscillator Voltage Stab; Vin8-40V	%	27.8956548	-1.94	1.0318268	1.22	1.26135	1.3491	0.03825387	1.3596	2.4199	1.4908732	1.94	5.91356338
*Ct Leakage; Ct2.5V, RtVref	u a	47.3129934	-19	-0.4448088	0.207	0.37417	0.5942	0.13649647	0.6253	-0.3682	1.19314883	19	45.4854981
SYNC Output High Level; Il-1.3mA	v	8.67607247	3.91	4.18421223	4.2513	4.26636	4.2888	0.01369129	0.5777	-0.8971	4.34850777	5.09	20.0526443
SYNC Output Low Level; Il0mA	v			2.16569212	2.1872	2.19533	2.1997	0.00493965	-0.6651	-1.5563	2.22496788	2.48	19.2098753
SYNC Input Current; 5.25V,RTVREF,CT0	m a			1.15417531	1.194	1.20409	1.2163	0.00831911	0.0988	-1.5125	1.25400469	1.49	11.4559468
*SYNC Leakage Current; 0.5V,Vref0	m a	565.919496	-1.5	0.04239972	0.0457	0.04787	0.0487	0.00091171	-1.8322	3.1839	0.05334028	1.49	527.259707
SYNC In High/Low Thresh.; CT0	v	16.6567645	2.51	2.92626785	2.9676	2.98307	3.003	0.00946702	0.6344	1.6669	3.03987215	3.89	31.9329474
E/A Input Offset Voltage	m v	5.53774705	-4.9	-2.2672223	-1.1521	-0.77883	-0.291	0.24806538	0.4051	0.5482	0.70956229	4.9	7.63082427
E/A Avol; Vout1.2-3V, Vcm2V	db	5.30988048	82	97.895077	105.5324	107.4997	110.6309	1.60077049	0.638	-0.0683	117.104323		
E/A PSRR; Vin8-40V	db	10.7127313	82	92.0107101	93.6969	94.30866	94.8969	0.38299165	-0.2229	-0.9121	96.6066099		
E/A CMRR; Vcm0-38; Vin40V	db	1.75528151	77	70.5478489	110.187	123.27906	140.0091	8.78853519	0.6488	0.1216	176.010271		
E/A Input Bias Current	u a	46.291582	-0.98	0.171714	0.2067	0.22372	0.2362	0.00866767	-0.5918	0.3051	0.275726	0.98	29.0843366
E/A Input Offset Current	n a	57.2475622	-245	-7.2958643	-1.3396	1.30919	3.2273	1.43417571	-0.3739	-0.4436	9.91424428	245	56.6389943
E/A Output Sink Current; COMP1.2V	m a	13.8819548	2.04	8.26479682	9.06	9.31257	9.6337	0.17462886	0.3257	-0.2973	10.3603432		
E/A Output Source Current; COMP2.5V	m a			-0.6173928	-0.5704	-0.55568	-0.5311	0.01028546	1.4083	3.826	-0.4939672	-0.408	4.78604472
E/A Output High Level; Rl15K	v	10.3264918	4.31	4.62982011	4.6904	4.70664	4.7257	0.01280332	0.5195	-1.1806	4.78345989		
E/A Output Low Level; Rl15K	v			0.71190526	0.729	0.73458	0.7418	0.00377912	0.7049	0.3714	0.75725474	0.97	20.7649536
C/L ADJ Offset Voltage	v	3.43648283	0.453	0.46919369	0.4839	0.49174	0.4962	0.00375772	-1.0754	0.8605	0.51428631	0.547	4.90191123
C/L ADJ Input Bias Current; 0V	u a	14.5878151	-29.4	-11.096336	-8.8269	-8.18818	-7.5313	0.48469264	-0.1073	-1.799	-5.2800241	29.4	25.8501825
*C/L ADJ Input Bias Current; 5V	u a	830.918023	-29.4	0.32380289	0.3813	0.39552	0.4127	0.01195285	0.4571	-1.3823	0.46723711	29.4	808.858015
*PWM Latch Test Output A	%			8.11055352	8.3131	8.36594	8.4521	0.04256441	0.7079	0.3856	8.62132648	25	130.265782
*PWM Latch Test Output B	%			8.1768455	8.3333	8.37938	8.4236	0.03375575	-0.1891	-1.8265	8.5819145	25	164.126309
C/S AMP Input Offset Voltage	m v	4.96145189	-23.4	-10.520738	-3.8353	-1.8228	1.0968	1.4496563	0.7478	0.5948	6.87513782	23.4	5.79971955
C/S AMP CMRR; Vcm1-12V	db	12.7072177	63	81.257166	83.6007	84.66742	85.5132	0.56837567	-0.5387	-0.0138	88.077674		
C/S AMP PSRR; Vin8-40V	db	3.65016489	63	74.8429018	85.9523	89.1965	94.216	2.39226636	0.6884	1.2777	103.550098		
C/S AMP Input Bias Current	u a	58.6341803	-9.7	1.07405124	1.3785	1.45453	1.5517	0.06341313	0.5228	-1.1866	1.83500876	9.7	43.3426038
C/S AMP Input Offset Current	u a	18.4715787	-0.7	-0.1178726	-0.061	-0.04719	-0.0239	0.01178044	0.8819	0.0592	0.02349264	0.7	21.142107
C/S AMP Gain	v	3.33357034	2.515	2.6125144	2.7103	2.75876	2.7929	0.02437427	-0.4281	0.8264	2.9050056	2.985	3.09397339
C/S AMP Max Diff Input	v	3.1112888	1.12	1.16779777	1.2356	1.25382	1.2817	0.01433704	0.6081	0.2378	1.33984223		
Shutdown Threshold Voltage	m v	6.79542713	254	329.385494	350.8312	360.82607	369.6337	5.24009593	-0.1864	0.6552	392.266646	396	2.23748639
Shutdown Latching Voltage; 3mA	v			0.09865384	0.1157	0.11958	0.1255	0.00348769	1.0021	-0.2871	0.14050616	1.995	179.241712
Shutdown NonLatching Volt; 0.8mA	v	634.56163	5.01	6.10854667	6.1109	6.11202	6.1127	0.00057889	-0.4547	0.128	6.11549333	7	511.313802
*Shutdown Input Bias Current; 0V	m a	332.544321	-1	-0.0178327	-0.0143	-0.01189	-0.0109	0.00099045	-1.7325	3.7656	-0.0059473	0.99	337.181923
*Shutdown Input Bias Current; 15V	m a	24.374066	1	2.5387797	2.6379	2.67633	2.7107	0.02292505	-0.5065	-0.4129	2.8138803	4.99	33.6410762
Collector Leakage Current; Vc40V	u a			69.0105901	83.1805	88.95183	93.6143	3.32353998	-0.6959	-0.3081	108.89307	170	8.12869916
Output A Low; Il20mA	v			0.10464725	0.1278	0.13358	0.1427	0.00482212	0.8714	-0.1261	0.16251275	0.392	17.863494

post20krad

Units: 10

Parameter		Cpk (LL)	Lower Limit	-6 Sigma	Min	Ave	Max	Sigma	Skew	Kurt	+6 Sigma	Upper Limit	Cpk (UL)
>Output A Low; Il100mA	v			0.60224382	0.6853	0.70757	0.7427	0.01755436	0.9668	0.3042	0.81289618	2.09	26.2504538
>Output B Low; Il100mA	v			0.61149343	0.6841	0.70274	0.7277	0.01520776	0.6736	-0.6029	0.79398657	2.09	30.4068426
Output B Low; Il20mA	v			0.10783144	0.1274	0.13199	0.1396	0.00402643	0.769	-0.2623	0.15614856	0.392	21.52529
Output B High; Il-20mA	v	66.2355173	13.045	13.5091388	13.5188	13.52359	13.5274	0.00240853	-0.3539	0.8722	13.5380412		
>Output B High; Il-100mA	v	89.3627333	12.03	13.305451	13.3251	13.33465	13.343	0.0048665	-0.2203	1.0806	13.363849		
Output A High; Il-20mA	v	40.2505211	13.045	13.4988211	13.5123	13.52255	13.5277	0.00395481	-2.0687	6.1767	13.5462789		
>Output A High; Il-100mA	v	37.4519537	12.03	13.260076	13.3009	13.32947	13.3413	0.01156566	-1.8527	4.1841	13.398864		
*PWM Output A Minimum Duty Cycle	%			0	0	0	0	0	#DIV/0!	#DIV/0!	0	0.001	Infinite
*PWM Output B Minimum Duty Cycle	%			0	0	0	0	0	#DIV/0!	#DIV/0!	0	0.001	Infinite
*PWM Output A Maximum Duty Cycle	%	11.6098277	45.05	47.0034644	47.2588	47.41002	47.4948	0.06775926	-1.1491	1.9673	47.8165756		
*PWM Output B Maximum Duty Cycle	%	14.6026827	45.05	47.0649368	47.2817	47.3847	47.4721	0.05329386	-0.3566	0.5695	47.7044632		
UVLO Start-up Threshold	v	30.5648143	6.01	7.689554	7.7854	7.80715	7.8456	0.01959933	0.9764	0.0382	7.924746	7.99	3.10979956
UVLO Threshold Hysterisis	v	113.963749	0.11	0.80904305	0.8178	0.82153	0.8254	0.00208116	0.1069	0.8453	0.83401695	2	188.752209

post30krad

Units: 8

Parameter		Cpk (LL)	Lower Limit	-6 Sigma	Min	Ave	Max	Sigma	Skew	Kurt	+6 Sigma	Upper Limit	Cpk (UL)
25'C QA				27	27	27	27	0	#DIV/0!	#DIV/0!	27		
Standby Supply Current; Vin15V	m a			12.3487228	12.8032	12.9695875	13.1379	0.10347746	-0.059	0.0971	13.5904522	20.6	24.5799511
Reference Output Voltage; Il1mA	v	2.08530587	5.05	5.05283544	5.1032	5.1193125	5.135	0.01107951	-0.123	-1.235	5.18578956	5.15	0.92325084
Reference Line Reg; Vin8-40V	m v	22.7735311	-19	2.19561344	3.9119	4.23625	4.93	0.34010609	1.3042	1.6679	6.27688656	19	14.4697496
>Reference Load Reg; Il1-10mA	m v	21.2335466	-14	-3.3001375	-2.4344	-2.1875125	-1.9062	0.1854375	0.5694	-0.715	-1.0748875		
Reference Short Circuit Current	m a	109.518552	-147	-46.720812	-45.1825	-44.855475	-44.2799	0.31088957	0.812	0.2274	-42.990138	-13	34.1551883
*Oscillator Discharge Current	m a	14.3984759	3.02	7.62855569	8.2531	8.3719625	8.6359	0.12390113	1.5594	2.636	9.11536931	17.98	25.8486669
INITIAL READING	k hz	11.982857	39.25	44.5777356	45.4368	45.6451125	45.9526	0.17789615	0.6087	-0.356	46.7124894	46.75	2.07028554
Oscillator Accuracy; 10K, 4.7nF	k hz	11.982857	39.25	44.5777356	45.4368	45.6451125	45.9526	0.17789615	0.6087	-0.356	46.7124894	46.75	2.07028554
Oscillator Voltage Stab; Vin8-40V	%	36.5905312	-1.94	1.08198355	1.1949	1.2567125	1.2785	0.02912149	-1.7	2.5037	1.43144145	1.94	7.82111391
*Ct Leakage; Ct2.5V, RtVref	u a	52.2420103	-19	-0.3926585	0.1978	0.34805	0.5751	0.12345141	0.6403	0.6238	1.08875848	19	50.3624584
SYNC Output High Level; Il-1.3mA	v	10.1914587	3.91	4.19565532	4.2479	4.2654	4.2791	0.01162411	-0.504	-1.332	4.33514468	5.09	23.6462489
SYNC Output Low Level; Il0mA	v			2.15267264	2.1827	2.19785	2.208	0.00752956	-0.957	2.0889	2.24302736	2.48	12.4907684
SYNC Input Current; 5.25V,RTVREF,CT0	m a			1.14520961	1.1852	1.1994125	1.2132	0.00903382	-0.038	-0.409	1.25361539	1.49	10.7222137
*SYNC Leakage Current; 0.5V,Vref0	m a	609.648845	-1.5	0.04355708	0.0473	0.0486375	0.0495	0.00084674	-0.502	-1.455	0.05371792	1.49	567.418123
SYNC In High/Low Thresh.; CT0	v	17.7154091	2.51	2.92956689	2.968	2.9829625	2.997	0.00889927	-0.15	0.2309	3.03635811	3.89	33.9742377
E/A Input Offset Voltage	m v	4.69962702	-4.9	-2.541028	-1.174	-0.7934	-0.1952	0.29127134	1.1668	2.3283	0.95422805	4.9	6.51557407
E/A Avol; Vout1.2-3V, Vcm2V	db	5.53988686	82	98.0934275	105.2242	107.18605	109.088	1.51543709	0.1799	-1.828	116.278673		
E/A PSRR; Vin8-40V	db	6.10799419	82	90.2596285	93.3765	94.280875	95.5198	0.67020774	0.5969	0.6472	98.3021215		
E/A CMRR; Vcm0-38; Vin40V	db	1.99642157	77	76.9206849	109.3247	121.250188	132.9697	7.38825043	0.1068	-0.038	165.57969		
E/A Input Bias Current	u a	69.0005047	-0.98	0.20903178	0.2319	0.244525	0.249	0.00591554	-1.731	2.6071	0.28001822	0.98	41.4431279
E/A Input Offset Current	n a	96.2937814	-245	-3.6209731	0.7304	1.49875	3.4692	0.85328719	2.1602	5.1276	6.61847313	245	95.1228197
E/A Output Sink Current; COMP1.2V	m a	19.7451168	2.04	8.54171122	9.1085	9.2745	9.471	0.12213146	0.4403	-0.6	10.0072888		
E/A Output Source Current; COMP2.5V	m a			-0.5826459	-0.561	-0.555925	-0.5484	0.00445349	0.5838	-0.879	-0.5292041	-0.408	11.0718415
E/A Output High Level; Rl15K	v	12.6153754	4.31	4.6452495	4.6936	4.7084125	4.7238	0.01052717	-0.022	-1.183	4.7715755		
E/A Output Low Level; Rl15K	v			0.72110301	0.7318	0.7343125	0.7383	0.00220158	0.924	0.0784	0.74752199	0.97	35.6845632
C/L ADJ Offset Voltage	v	4.08181577	0.453	0.47204295	0.4842	0.4903375	0.4941	0.00304909	-1.04	1.7771	0.50863205	0.547	6.19446632
C/L ADJ Input Bias Current; 0V	u a	28.8161079	-29.4	-10.300574	-9.1908	-8.8761	-8.4663	0.23741235	0.4932	-0.299	-7.4516259	29.4	53.7406744
*C/L ADJ Input Bias Current; 5V	u a	597.681889	-29.4	0.29638199	0.3764	0.3960875	0.4169	0.01661758	0.0979	-2.183	0.49579301	29.4	581.791593
*PWM Latch Test Output A	%			8.11469624	8.309	8.3812375	8.4438	0.04442354	-0.129	-0.418	8.64777876	25	124.69936
*PWM Latch Test Output B	%			8.13813381	8.3374	8.3874	8.4604	0.04154437	0.7411	-0.194	8.63666619	25	133.292043
C/S AMP Input Offset Voltage	m v	5.78285761	-23.4	-8.9920387	-2.9425	-1.3745375	1.1088	1.26958354	0.9005	1.2098	6.24296374	23.4	6.50463629
C/S AMP CMRR; Vcm1-12V	db	7.15454727	63	78.6479317	83.3289	84.7194375	86.3855	1.01191763	0.5877	-0.274	90.7909433		
C/S AMP PSRR; Vin8-40V	db	8.08428826	63	82.851484	87.4396	89.376975	90.7579	1.08758183	-0.453	0.0517	95.902466		
C/S AMP Input Bias Current	u a	151.376306	-9.7	1.5094294	1.6192	1.6595125	1.7005	0.02501385	0.0401	0.1909	1.8095956	9.7	107.147142
C/S AMP Input Offset Current	u a	5.01928161	-0.7	-0.31928	-0.1245	-0.0670875	-0.0169	0.04203208	-0.246	-1.747	0.18510496	0.7	6.08334988
C/S AMP Gain	v	2.67580004	2.515	2.57314562	2.7006	2.745225	2.7793	0.0286799	-0.359	-1.207	2.91730438	2.985	2.78679533
C/S AMP Max Diff Input	v	3.62939493	1.12	1.18264452	1.2398	1.2595375	1.2798	0.0128155	0.0897	-0.389	1.33643048		
Shutdown Threshold Voltage	m v	16.2814119	254	347.529467	357.6518	360.627538	363.6703	2.18301169	-0.019	-1.393	373.725608	396	5.40117164
Shutdown Latching Voltage; 3mA	v			0.09979636	0.1147	0.1188375	0.1238	0.00317352	0.7977	-0.327	0.13787864	1.995	197.064097
Shutdown NonLatching Volt; 0.8mA	v	1364.39532	5.01	6.06765985	6.0689	6.0692125	6.0694	0.00025877	-0.644	-2.24	6.07076515	7	1198.96821
*Shutdown Input Bias Current; 0V	m a	197.650418	-1	-0.0244103	-0.0165	-0.0144375	-0.0122	0.00166213	0.289	-1.306	-0.0044647	0.99	201.43572
*Shutdown Input Bias Current; 15V	m a	33.8425951	1	2.56475677	2.6397	2.6630375	2.6907	0.01638012	-0.041	0.3428	2.76131823	4.99	47.3533819
Collector Leakage Current; Vc40V	u a			69.6708445	80.7761	86.603325	88.6403	2.82208009	-1.482	1.7264	103.535806	170	9.85049708
Output A Low; Il20mA	v			0.10416647	0.1272	0.1328375	0.1403	0.0047785	0.8037	-0.751	0.16150853	0.392	18.0783541

post30krad

Units: 8

Parameter		Cpk (LL)	Lower Limit	-6 Sigma	Min	Ave	Max	Sigma	Skew	Kurt	+6 Sigma	Upper Limit	Cpk (UL)
>Output A Low; Il100mA	v			0.59950663	0.6863	0.70835	0.7362	0.01814056	0.3979	-1.09	0.81719337	2.09	25.3878569
>Output B Low; Il100mA	v			0.57770154	0.6864	0.713575	0.7557	0.02264558	0.9309	0.4722	0.84944846	2.09	20.2603952
Output B Low; Il20mA	v			0.09858105	0.1266	0.13335	0.144	0.00579483	1.1359	0.417	0.16811895	0.392	14.8782168
Output B High; Il-20mA	v	19.5477684	13.045	13.4556467	13.484	13.50245	13.5093	0.00780055	-2.338	6.0784	13.5492533		
>Output B High; Il-100mA	v	43.2188048	12.03	13.2506592	13.2917	13.3098875	13.3241	0.00987138	-0.614	0.784	13.3691158		
Output A High; Il-20mA	v	18.7568844	13.045	13.4546783	13.484	13.503575	13.509	0.00814945	-2.52	6.6304	13.5524717		
>Output A High; Il-100mA	v	39.7994615	12.03	13.2500701	13.2896	13.314625	13.3229	0.01075915	-2.215	5.3637	13.3791799		
*PWM Output A Minimum Duty Cycle	%			0	0	0	0	0	#DIV/0!	#DIV/0!	0	0.001	Infinite
*PWM Output B Minimum Duty Cycle	%			0	0	0	0	0	#DIV/0!	#DIV/0!	0	0.001	Infinite
*PWM Output A Maximum Duty Cycle	%	17.7106961	45.05	47.0968454	47.2914	47.3574125	47.4305	0.04342785	0.4442	0.2563	47.6179796		
*PWM Output B Maximum Duty Cycle	%	21.0001113	45.05	47.1324238	47.2921	47.351625	47.4043	0.03653354	-0.331	-0.426	47.5708262		
UVLO Start-up Threshold	v	23.1177695	6.01	7.65643375	7.7821	7.8123625	7.8606	0.02598813	0.652	0.5151	7.96829125	7.99	2.27844442
UVLO Threshold Hysterisis	v	42.6756248	0.11	0.78984725	0.8168	0.823275	0.8315	0.00557129	0.3553	-1.623	0.85670275	2	70.4040862

post40krad

Units: 11

Parameter		Cpk (LL)	Lower Limit	-6 Sigma	Min	Ave	Max	Sigma	Skew	Kurt	+6 Sigma	Upper Limit	Cpk (UL)
25'C QA				27	27	27	27	0	#DIV/0!	#DIV/0!	27		
Standby Supply Current; Vin15V	m a			12.1013306	12.718	13.0004636	13.1996	0.14985551	-0.446	-0.443	13.8995967	20.6	16.9041423
Reference Output Voltage; Il1mA	v	1.33056456	5.05	5.01570085	5.0911	5.11817273	5.1492	0.01707865	-0.099	-0.119	5.22064461	5.15	0.62119036
Reference Line Reg; Vin8-40V	m v	6.7019687	-19	-2.3508125	3.6669	4.73098182	8.0534	1.18029905	2.5852	7.5313	11.8127761	19	4.02977483
>Reference Load Reg; Il1-10mA	m v	32.6088927	-14	-3.0189695	-2.488	-2.3014636	-2.1129	0.11958432	0.2814	-0.47	-1.5839577		
Reference Short Circuit Current	m a	108.741371	-147	-46.574559	-45.1825	-44.6929	-44.2596	0.31360987	-0.073	-1.16	-42.811241	-13	33.6861214
*Oscillator Discharge Current	m a	15.9808551	3.02	7.55013366	8.0032	8.19818182	8.3701	0.10800803	-0.373	-0.226	8.84622997	17.98	30.1885535
INITIAL READING	k hz	4.36475439	39.25	42.7031987	44.8709	45.6237545	46.6012	0.48675931	0.2936	0.7847	48.5443104	46.75	0.77125417
Oscillator Accuracy; 10K, 4.7nF	k hz	4.36475439	39.25	42.7031987	44.8709	45.6237545	46.6012	0.48675931	0.2936	0.7847	48.5443104	46.75	0.77125417
Oscillator Voltage Stab; Vin8-40V	%	8.26650201	-1.94	0.5018619	1.1684	1.2812	1.6502	0.12988968	2.6409	7.959	2.0605381	1.94	1.69066544
*Ct Leakage; Ct2.5V, RtVref	u a	55.2462226	-19	-0.3203685	0.2732	0.38126364	0.5751	0.1169387	0.7458	-0.831	1.08289581	19	53.0726413
SYNC Output High Level; Il-1.3mA	v	5.96693881	3.91	4.14561212	4.2407	4.2644	4.3149	0.01979798	1.608	4.2836	4.38318788	5.09	13.9004082
SYNC Output Low Level; Il0mA	v			2.08708818	2.1662	2.19412727	2.2297	0.01783985	0.2137	0.4829	2.30116636	2.48	5.34146414
SYNC Input Current; 5.25V,RTVREF,CT0	m a			1.15067062	1.1837	1.20347273	1.2139	0.00880035	-1.164	1.3001	1.25627483	1.49	10.8528726
*SYNC Leakage Current; 0.5V,Vref0	m a	515.085224	-1.5	0.04275002	0.0467	0.04876364	0.0501	0.00100227	-0.679	0.1896	0.05477726	1.49	479.323984
SYNC In High/Low Thresh.; CT0	v	12.094725	2.51	2.91142325	2.972	2.99095455	3.0115	0.01325522	0.0216	-0.941	3.07048584	3.89	22.6085971
E/A Input Offset Voltage	m v	3.64860907	-4.9	-3.0765224	-1.3478	-0.8643818	0.1269	0.36869011	2.0584	6.0051	1.34775881	4.9	5.21158713
E/A Avol; Vout1.2-3V, Vcm2V	db	4.9004958	82	97.0925615	105.0581	107.499445	110.8835	1.73448065	1.1727	1.0656	117.906329		
E/A PSRR; Vin8-40V	db	8.14649402	82	91.3436806	93.3303	94.3840091	95.0956	0.50672142	-0.746	0.5857	97.4243376		
E/A CMRR; Vcm0-38; Vin40V	db	1.7694379	77	71.6312891	100.6087	118.201918	127.5928	7.76177152	-1.018	1.6326	164.772547		
E/A Input Bias Current	u a	14.4190063	-0.98	0.07747351	0.1659	0.24777273	0.2711	0.0283832	-2.813	8.6457	0.41807194	0.98	8.59930298
E/A Input Offset Current	n a	19.6750373	-245	-23.040688	-1.6433	2.07488182	13.9986	4.18592823	2.6871	8.0645	27.1904512	245	19.3445838
E/A Output Sink Current; COMP1.2V	m a	6.06499938	2.04	6.77283207	8.096	9.10140909	9.5003	0.38809617	-1.905	4.4739	11.4299861		
E/A Output Source Current; COMP2.5V	m a			-0.6006461	-0.5654	-0.5547091	-0.5452	0.00765617	-0.094	-1.668	-0.5087721	-0.408	6.38740295
E/A Output High Level; Rl15K	v	7.93096218	4.31	4.60715118	4.6851	4.70735455	4.7448	0.01670056	0.8358	1.5657	4.80755791		
E/A Output Low Level; Rl15K	v			0.67971708	0.731	0.73854545	0.7669	0.00980473	2.8477	8.758	0.79737383	0.97	7.86880581
C/L ADJ Offset Voltage	v	2.55914221	0.453	0.46151309	0.4864	0.49196364	0.506	0.00507509	2.3417	6.91	0.52241418	0.547	3.6148033
C/L ADJ Input Bias Current; 0V	u a	8.32076206	-29.4	-13.891733	-9.8234	-8.9846455	-6.8568	0.81784795	1.892	4.6261	-4.0775578	29.4	15.6445729
*C/L ADJ Input Bias Current; 5V	u a	951.018772	-29.4	0.34171204	0.3909	0.40439091	0.4193	0.01044648	0.0803	-1.651	0.46706978	29.4	925.211611
*PWM Latch Test Output A	%			7.73329062	8.233	8.37679091	8.6284	0.10725005	1.1719	2.3326	9.0202912	25	51.6649621
*PWM Latch Test Output B	%			7.87654165	8.233	8.37957273	8.5329	0.08383851	-0.021	0.3143	8.8826038	25	66.0811154
C/S AMP Input Offset Voltage	m v	2.43139925	-23.4	-19.701278	-10.7187	-2.5537182	0.1811	2.8579266	-2.688	8.2445	14.5938414	23.4	3.02710342
C/S AMP CMRR; Vcm1-12V	db	6.30615721	63	78.1537186	83.9945	85.1918818	88.0975	1.1730272	1.5803	3.2089	92.230045		
C/S AMP PSRR; Vin8-40V	db	2.58341993	63	68.7177048	79.776	88.3183545	93.1414	3.26677495	-1.728	5.3446	107.919004		
C/S AMP Input Bias Current	u a	14.6163814	-9.7	0.14042026	0.9801	1.70036364	1.8891	0.25999056	-2.443	6.812	3.26030701	9.7	10.2563163
C/S AMP Input Offset Current	u a	2.43412337	-0.7	-0.5875234	-0.2377	-0.0693455	0.1051	0.08636299	0.059	1.6834	0.44883251	0.7	2.9694256
C/S AMP Gain	v	3.68814747	2.515	2.62321804	2.7139	2.75142727	2.7944	0.0213682	0.3578	0.9057	2.8796365	2.985	3.64361798
C/S AMP Max Diff Input	v	3.68950789	1.12	1.18180286	1.2336	1.25496364	1.2733	0.01219346	-0.366	-0.742	1.32812442		
Shutdown Threshold Voltage	m v	3.95706496	254	308.576191	356.0438	364.3497	390.9681	9.29558491	2.7088	8.3562	420.123209	396	1.13495817
Shutdown Latching Voltage; 3mA	v			0.04495323	0.1172	0.12487273	0.1635	0.01331992	2.8972	8.8678	0.20479223	1.995	46.8002744
Shutdown NonLatching Volt; 0.8mA	v	742.986075	5.01	6.06593175	6.0682	6.06878182	6.0692	0.00047501	-0.478	-1.964	6.07163189	7	653.469988
*Shutdown Input Bias Current; 0V	m a	162.453105	-1	-0.0272253	-0.018	-0.0151	-0.0126	0.00202089	0.0609	-1.567	-0.0029747	0.99	165.784969
*Shutdown Input Bias Current; 15V	m a	32.3695272	1	2.56749034	2.6373	2.67071818	2.6864	0.01720464	-1.519	1.1297	2.77394602	4.99	44.9352001
Collector Leakage Current; Vc40V	u a			76.8048047	84.1254	86.6342545	89.2318	1.63824165	0.202	-0.957	96.4637044	170	16.9624438
Output A Low; Il20mA	v			0.10024118	0.1296	0.13625455	0.1486	0.00600223	1.0394	0.0676	0.17226791	0.392	14.2028095

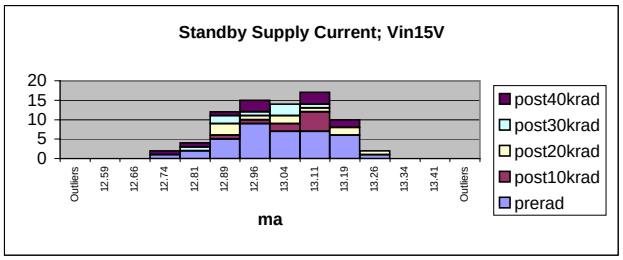
post40krad

Units: 11

Parameter		Cpk (LL)	Lower Limit	-6 Sigma	Min	Ave	Max	Sigma	Skew	Kurt	+6 Sigma	Upper Limit	Cpk (UL)
>Output A Low; Il100mA	v			0.57451232	0.69	0.71964545	0.7598	0.02418886	0.7059	-1.098	0.86477859	2.09	18.8841035
>Output B Low; Il100mA	v			0.49522148	0.6979	0.73512727	0.8389	0.0399843	1.893	4.5042	0.97503307	2.09	11.2950396
Output B Low; Il20mA	v			0.09247266	0.1304	0.13850909	0.1556	0.00767274	1.1809	1.2144	0.18454552	0.392	11.0126228
Output B High; Il-20mA	v	21.6059353	13.045	13.4555474	13.4889	13.4974273	13.5118	0.00697998	0.6643	0.1494	13.5393072		
>Output B High; Il-100mA	v	53.184466	12.03	13.2532741	13.2877	13.3010727	13.3124	0.00796644	-0.03	-0.968	13.3488714		
Output A High; Il-20mA	v	20.2983974	13.045	13.4530217	13.4879	13.4976182	13.512	0.00743274	0.5017	-0.261	13.5422146		
>Output A High; Il-100mA	v	34.4631518	12.03	13.2290127	13.2813	13.3028818	13.3191	0.01231152	-0.345	-0.861	13.376751		
*PWM Output A Minimum Duty Cycle	%			0	0	0	0	0	#DIV/0!	#DIV/0!	0	0.001	Infinite
*PWM Output B Minimum Duty Cycle	%			0	0	0	0	0	#DIV/0!	#DIV/0!	0	0.001	Infinite
*PWM Output A Maximum Duty Cycle	%	13.199297	45.05	47.008994	47.2356	47.3588364	47.4614	0.05830705	-0.409	1.4783	47.7086787		
*PWM Output B Maximum Duty Cycle	%	17.5490334	45.05	47.0863791	47.2809	47.3483091	47.4084	0.043655	-0.011	-1.404	47.6102391		
UVLO Start-up Threshold	v	26.5606525	6.01	7.66538228	7.7694	7.80018182	7.8343	0.02246659	0.057	-1.172	7.93498135	7.99	2.81630319
UVLO Threshold Hysterisis	v	51.3863162	0.11	0.7926283	0.8119	0.82027273	0.8269	0.00460741	-0.956	0.3514	0.84791716	2	85.3500865

Standby Supply Current; Vin15V

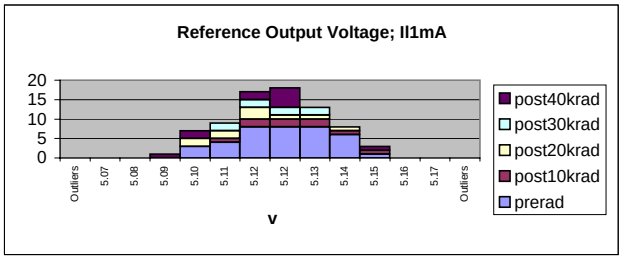
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
12.59	0	0	0	0	0
12.66	0	0	0	0	0
12.74	1	0	0	0	1
12.81	2	0	0	1	1
12.89	5	1	3	2	1
12.96	9	1	1	1	3
13.04	7	2	2	3	0
13.11	7	5	1	1	3
13.19	6	0	2	0	2
13.26	1	0	1	0	0
13.34	0	0	0	0	0
13.41	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	-	-	12.718	13.021	13.234	0.121	20.6	20.847
post10krad	-	-	12.906	13.061	13.137	0.080	20.6	31.538
post20krad	-	-	12.857	13.044	13.232	0.134	20.6	18.782
post30krad	-	-	12.803	12.970	13.138	0.103	20.6	24.580
post40krad	-	-	12.718	13.000	13.200	0.150	20.6	16.904

Reference Output Voltage; Il1mA

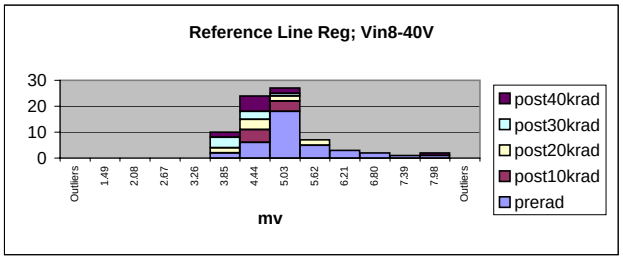
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
5.07	0	0	0	0	0
5.08	0	0	0	0	0
5.09	0	0	0	0	1
5.10	3	0	2	0	2
5.11	4	1	2	2	0
5.12	8	2	3	2	2
5.12	8	2	1	2	5
5.13	8	2	1	2	0
5.14	6	1	1	0	0
5.15	1	1	0	0	1
5.16	0	0	0	0	0
5.17	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	1.797	5.05	5.100	5.125	5.150	0.014	5.15	0.605
post10krad	1.666	5.05	5.104	5.127	5.155	0.015	5.15	0.486
post20krad	1.576	5.05	5.100	5.116	5.141	0.014	5.15	0.798
post30krad	2.085	5.05	5.103	5.119	5.135	0.011	5.15	0.923
post40krad	1.331	5.05	5.091	5.118	5.149	0.017	5.15	0.621

Reference Line Reg; Vin8-40V

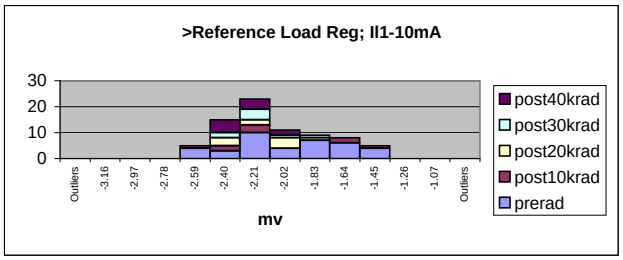
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
1.49	0	0	0	0	0
2.08	0	0	0	0	0
2.67	0	0	0	0	0
3.26	0	0	0	0	0
3.85	2	0	2	4	2
4.44	6	5	4	3	6
5.03	18	4	2	1	2
5.62	5	0	2	0	0
6.21	3	0	0	0	0
6.80	2	0	0	0	0
7.39	1	0	0	0	0
7.98	1	0	0	0	1
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	9.181	-19	3.886	5.255	7.757	0.881	19	5.203
post10krad	22.402	-19	4.154	4.622	5.271	0.351	19	13.635
post20krad	12.976	-19	3.705	4.655	5.787	0.608	19	7.869
post30krad	22.774	-19	3.912	4.236	4.930	0.340	19	14.470
post40krad	6.702	-19	3.667	4.731	8.053	1.180	19	4.030

>Reference Load Reg; Il1-10mA

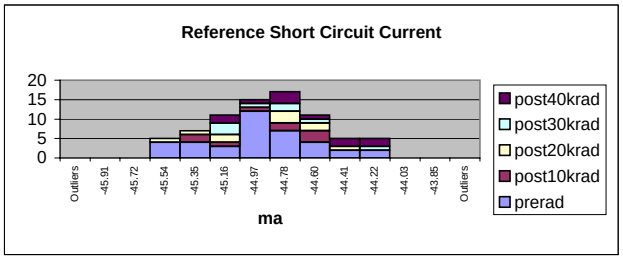
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
-3.16	0	0	0	0	0
-2.97	0	0	0	0	0
-2.78	0	0	0	0	0
-2.59	4	1	0	0	0
-2.40	3	2	3	2	5
-2.21	10	3	2	4	4
-2.02	4	0	4	1	2
-1.83	7	0	1	1	0
-1.64	6	2	0	0	0
-1.45	4	1	0	0	0
-1.26	0	0	0	0	0
-1.07	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	11.962	-14	-2.540	-2.006	-1.377	0.334	-	-
post10krad	10.405	-14	-2.540	-2.117	-1.500	0.381	-	-
post20krad	19.290	-14	-2.457	-2.164	-1.906	0.205	-	-
post30krad	21.234	-14	-2.434	-2.188	-1.906	0.185	-	-
post40krad	32.609	-14	-2.488	-2.301	-2.113	0.120	-	-

Reference Short Circuit Current

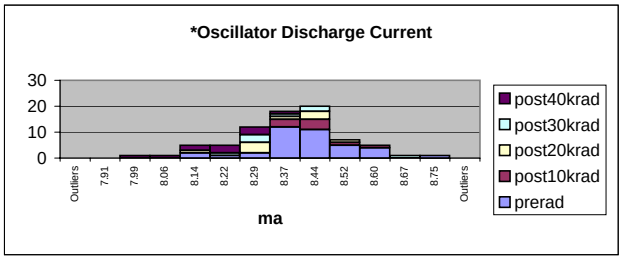
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
-45.91	0	0	0	0	0
-45.72	0	0	0	0	0
-45.54	4	0	1	0	0
-45.35	4	2	1	0	0
-45.16	3	1	2	3	2
-44.97	12	1	0	1	1
-44.78	7	2	3	2	3
-44.60	4	3	2	1	1
-44.41	2	0	1	0	2
-44.22	2	0	0	1	2
-44.03	0	0	0	0	0
-43.85	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	97.771	-147	-45.593	-44.954	-44.137	0.348	-13	30.616
post10krad	105.542	-147	-45.422	-44.931	-44.583	0.322	-13	33.018
post20krad	91.968	-147	-45.481	-44.895	-44.487	0.370	-13	28.729
post30krad	109.519	-147	-45.182	-44.855	-44.280	0.311	-13	34.155
post40krad	108.741	-147	-45.182	-44.693	-44.260	0.314	-13	33.686

***Oscillator Discharge Current**

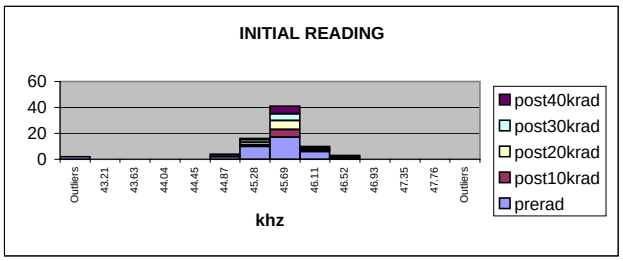
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
7.91	0	0	0	0	0
7.99	0	0	0	0	1
8.06	0	0	0	0	1
8.14	2	0	1	0	2
8.22	1	0	0	1	3
8.29	2	0	4	3	3
8.37	12	3	1	1	1
8.44	11	4	3	2	0
8.52	5	1	1	0	0
8.60	4	1	0	0	0
8.67	0	0	0	1	0
8.75	1	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	15.029	3.02	8.137	8.428	8.767	0.120	17.98	26.549
post10krad	25.174	3.02	8.372	8.452	8.592	0.072	17.98	44.162
post20krad	16.596	3.02	8.169	8.360	8.506	0.107	17.98	29.899
post30krad	14.398	3.02	8.253	8.372	8.636	0.124	17.98	25.849
post40krad	15.981	3.02	8.003	8.198	8.370	0.108	17.98	30.189

INITIAL READING

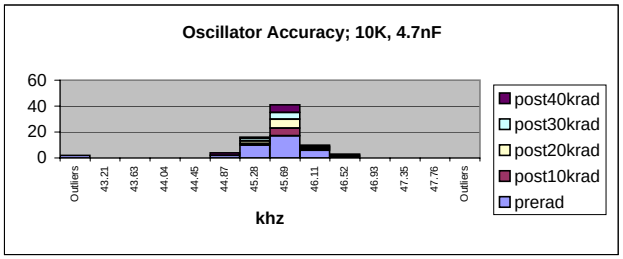
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	2	0	0	0	0
43.21	0	0	0	0	0
43.63	0	0	0	0	0
44.04	0	0	0	0	0
44.45	0	0	0	0	0
44.87	2	0	0	0	2
45.28	10	1	2	2	1
45.69	17	6	7	5	6
46.11	6	1	1	1	1
46.52	1	1	0	0	1
46.93	0	0	0	0	0
47.35	0	0	0	0	0
47.76	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	2.516	39.25	41.937	45.486	46.420	0.826	46.75	0.510
post10krad	6.723	39.25	45.399	45.838	46.524	0.327	46.75	0.931
post20krad	12.754	39.25	45.382	45.595	45.976	0.166	46.75	2.321
post30krad	11.983	39.25	45.437	45.645	45.953	0.178	46.75	2.070
post40krad	4.365	39.25	44.871	45.624	46.601	0.487	46.75	0.771

Oscillator Accuracy; 10K, 4.7nF

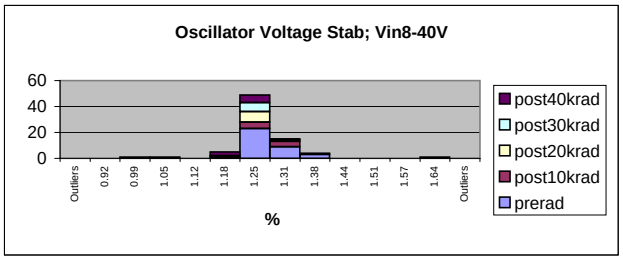
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	2	0	0	0	0
43.21	0	0	0	0	0
43.63	0	0	0	0	0
44.04	0	0	0	0	0
44.45	0	0	0	0	0
44.87	2	0	0	0	2
45.28	10	1	2	2	1
45.69	17	6	7	5	6
46.11	6	1	1	1	1
46.52	1	1	0	0	1
46.93	0	0	0	0	0
47.35	0	0	0	0	0
47.76	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	2.516	39.25	41.937	45.486	46.420	0.826	46.75	0.510
post10krad	6.723	39.25	45.399	45.838	46.524	0.327	46.75	0.931
post20krad	12.754	39.25	45.382	45.595	45.976	0.166	46.75	2.321
post30krad	11.983	39.25	45.437	45.645	45.953	0.178	46.75	2.070
post40krad	4.365	39.25	44.871	45.624	46.601	0.487	46.75	0.771

Oscillator Voltage Stab; Vin8-40V

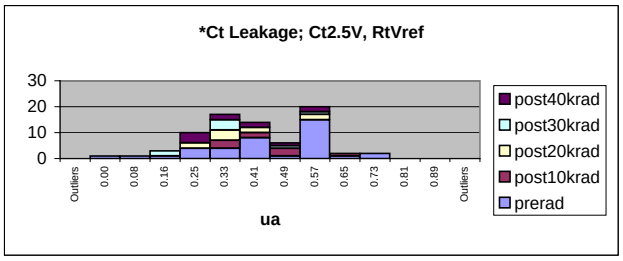
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
0.92	0	0	0	0	0
0.99	1	0	0	0	0
1.05	1	0	0	0	0
1.12	0	0	0	0	0
1.18	1	0	0	1	3
1.25	23	5	8	7	6
1.31	9	4	1	0	1
1.38	3	0	1	0	0
1.44	0	0	0	0	0
1.51	0	0	0	0	0
1.57	0	0	0	0	0
1.64	0	0	0	0	1
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	15.643	-1.94	0.995	1.268	1.388	0.068	1.94	3.277
post10krad	59.463	-1.94	1.243	1.274	1.296	0.018	1.94	12.325
post20krad	27.896	-1.94	1.220	1.261	1.349	0.038	1.94	5.914
post30krad	36.591	-1.94	1.195	1.257	1.278	0.029	1.94	7.821
post40krad	8.267	-1.94	1.168	1.281	1.650	0.130	1.94	1.691

***Ct Leakage; Ct2.5V, RtVref**

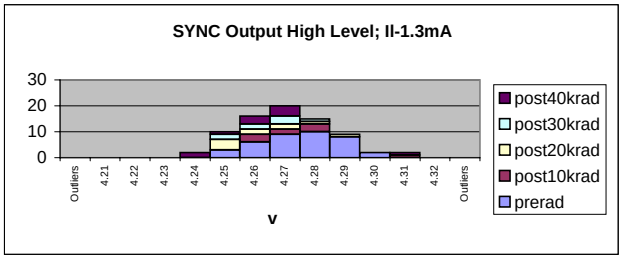
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
0.00	1	0	0	0	0
0.08	1	0	0	0	0
0.16	1	0	0	2	0
0.25	4	0	2	0	4
0.33	4	3	4	4	2
0.41	8	2	2	0	2
0.49	1	3	0	1	1
0.57	15	0	2	1	2
0.65	1	1	0	0	0
0.73	2	0	0	0	0
0.81	0	0	0	0	0
0.89	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	40.013	-19	0.025	0.448	0.705	0.162	19	38.171
post10krad	61.313	-19	0.289	0.448	0.629	0.106	19	58.486
post20krad	47.313	-19	0.207	0.374	0.594	0.136	19	45.485
post30krad	52.242	-19	0.198	0.348	0.575	0.123	19	50.362
post40krad	55.246	-19	0.273	0.381	0.575	0.117	19	53.073

SYNC Output High Level; Il-1.3mA

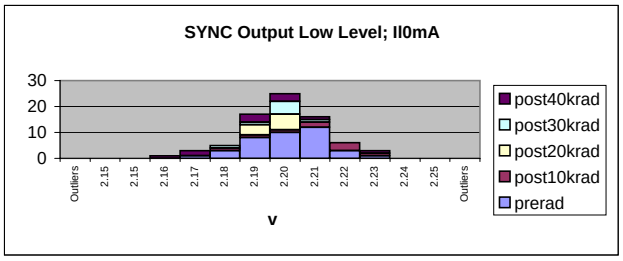
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
4.21	0	0	0	0	0
4.22	0	0	0	0	0
4.23	0	0	0	0	0
4.24	0	0	0	0	2
4.25	3	0	4	2	1
4.26	6	3	2	2	3
4.27	9	2	2	3	4
4.28	10	3	1	1	0
4.29	8	0	1	0	0
4.30	2	0	0	0	0
4.31	0	1	0	0	1
4.32	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	9.077	3.91	4.255	4.278	4.303	0.014	5.09	20.042
post10krad	6.954	3.91	4.257	4.277	4.313	0.018	5.09	15.424
post20krad	8.676	3.91	4.251	4.266	4.289	0.014	5.09	20.053
post30krad	10.191	3.91	4.248	4.265	4.279	0.012	5.09	23.646
post40krad	5.967	3.91	4.241	4.264	4.315	0.020	5.09	13.900

SYNC Output Low Level; Il0mA

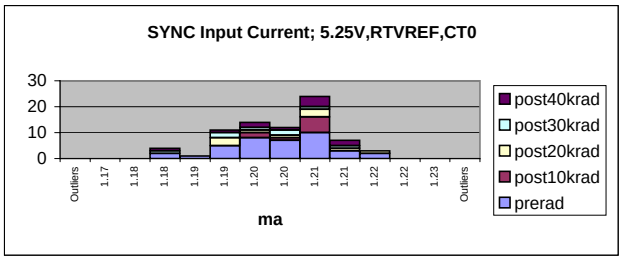
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
2.15	0	0	0	0	0
2.15	0	0	0	0	0
2.16	0	0	0	0	1
2.17	1	0	0	0	2
2.18	3	1	0	1	0
2.19	8	1	4	1	3
2.20	10	1	6	5	3
2.21	12	2	0	1	1
2.22	3	3	0	0	0
2.23	1	1	0	0	1
2.24	0	0	0	0	0
2.25	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	-	-	2.177	2.202	2.228	0.012	2.48	7.849
post10krad	-	-	2.183	2.209	2.228	0.014	2.48	6.286
post20krad	-	-	2.187	2.195	2.200	4.94E-03	2.48	19.210
post30krad	-	-	2.183	2.198	2.208	7.53E-03	2.48	12.491
post40krad	-	-	2.166	2.194	2.230	0.018	2.48	5.341

SYNC Input Current; 5.25V,RTVREF,CT0

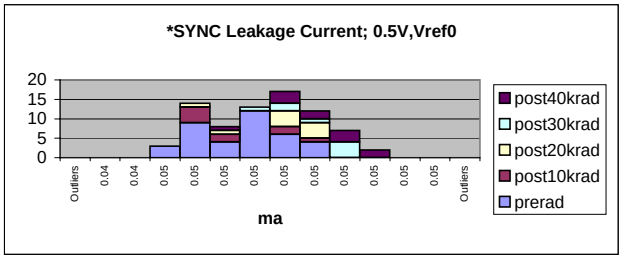
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
1.17	0	0	0	0	0
1.18	0	0	0	0	0
1.18	2	0	0	1	1
1.19	1	0	0	0	0
1.19	5	0	3	2	1
1.20	8	2	1	1	2
1.20	7	1	1	2	1
1.21	10	6	3	1	4
1.21	3	0	1	1	2
1.22	2	0	1	0	0
1.22	0	0	0	0	0
1.23	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	-	-	1.182	1.203	1.217	8.09E-03	1.49	11.834
post10krad	-	-	1.199	1.206	1.210	4.11E-03	1.49	23.063
post20krad	-	-	1.194	1.204	1.216	8.32E-03	1.49	11.456
post30krad	-	-	1.185	1.199	1.213	9.03E-03	1.49	10.722
post40krad	-	-	1.184	1.203	1.214	8.80E-03	1.49	10.853

***SYNC Leakage Current; 0.5V,Vref0**

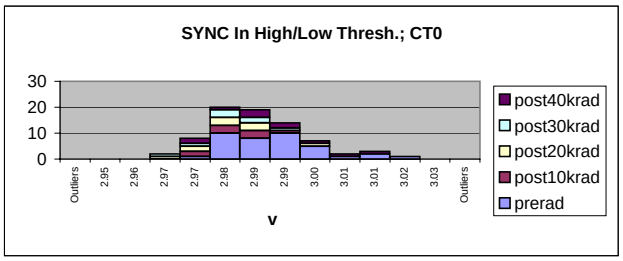
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
0.04	0	0	0	0	0
0.04	0	0	0	0	0
0.05	3	0	0	0	0
0.05	9	4	1	0	0
0.05	4	2	1	0	1
0.05	12	0	0	1	0
0.05	6	2	4	2	3
0.05	4	1	4	1	2
0.05	0	0	0	4	3
0.05	0	0	0	0	2
0.05	0	0	0	0	0
0.05	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	546.563	-1.5	0.045	0.047	0.049	9.43E-04	1.49	509.859
post10krad	486.035	-1.5	0.046	0.047	0.049	1.06E-03	1.49	453.515
post20krad	565.919	-1.5	0.046	0.048	0.049	9.12E-04	1.49	527.260
post30krad	609.649	-1.5	0.047	0.049	0.049	8.47E-04	1.49	567.418
post40krad	515.085	-1.5	0.047	0.049	0.050	1.00E-03	1.49	479.324

SYNC In High/Low Thresh.; CT0

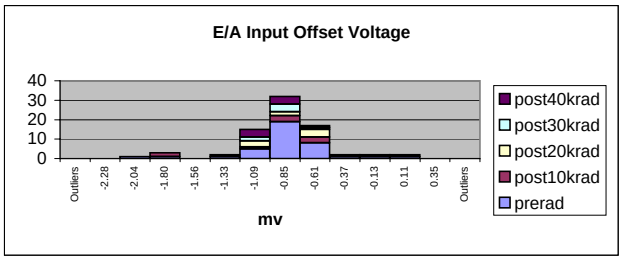
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
2.95	0	0	0	0	0
2.96	0	0	0	0	0
2.97	0	0	1	1	0
2.97	1	2	2	1	2
2.98	10	3	3	3	1
2.99	8	3	3	2	3
2.99	10	1	0	1	2
3.00	5	0	1	0	1
3.01	1	0	0	0	1
3.01	2	0	0	0	1
3.02	1	0	0	0	0
3.03	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	15.415	2.51	2.972	2.991	3.020	0.010	3.89	28.834
post10krad	25.145	2.51	2.976	2.983	2.992	6.27E-03	3.89	48.195
post20krad	16.657	2.51	2.968	2.983	3.003	9.47E-03	3.89	31.933
post30krad	17.715	2.51	2.968	2.983	2.997	8.90E-03	3.89	33.974
post40krad	12.095	2.51	2.972	2.991	3.011	0.013	3.89	22.609

E/A Input Offset Voltage

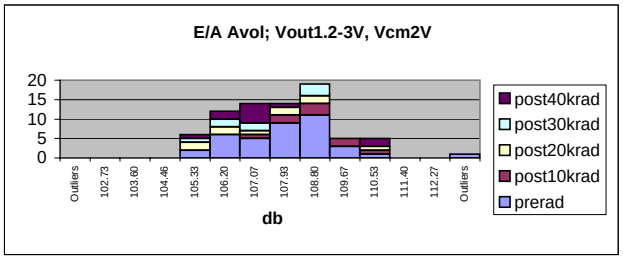
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
-2.28	0	0	0	0	0
-2.04	1	0	0	0	0
-1.80	1	2	0	0	0
-1.56	0	0	0	0	0
-1.33	1	0	0	0	1
-1.09	5	1	3	2	4
-0.85	19	3	2	4	4
-0.61	8	3	4	1	1
-0.37	1	0	1	0	0
-0.13	1	0	0	1	0
0.11	1	0	0	0	1
0.35	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	3.671	-4.9	-2.003	-0.849	0.121	0.368	4.9	5.210
post10krad	2.742	-4.9	-1.845	-0.967	-0.499	0.478	4.9	4.089
post20krad	5.538	-4.9	-1.152	-0.779	-0.291	0.248	4.9	7.631
post30krad	4.700	-4.9	-1.174	-0.793	-0.195	0.291	4.9	6.516
post40krad	3.649	-4.9	-1.348	-0.864	0.127	0.369	4.9	5.212

E/A Avol; Vout1.2-3V, Vcm2V

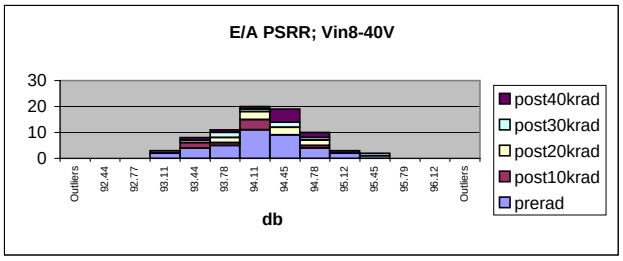
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
102.73	0	0	0	0	0
103.60	0	0	0	0	0
104.46	0	0	0	0	0
105.33	2	0	2	1	1
106.20	6	0	2	2	2
107.07	5	1	1	2	5
107.93	9	2	2	0	1
108.80	11	3	2	3	0
109.67	3	2	0	0	0
110.53	1	1	1	0	2
111.40	0	0	0	0	0
112.27	0	0	0	0	0
Outliers	1	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	5.941	82	105.263	107.952	112.990	1.456	-	-
post10krad	9.341	82	107.135	108.748	110.329	0.955	-	-
post20krad	5.310	82	105.532	107.500	110.631	1.601	-	-
post30krad	5.540	82	105.224	107.186	109.088	1.515	-	-
post40krad	4.900	82	105.058	107.499	110.883	1.734	-	-

E/A PSRR; Vin8-40V

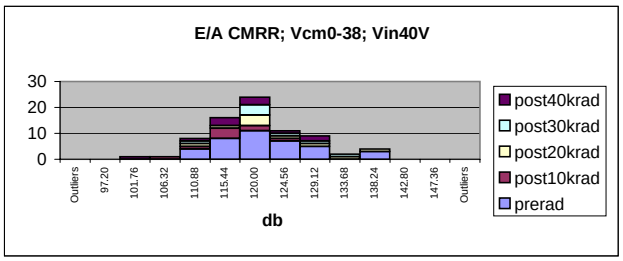
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
92.44	0	0	0	0	0
92.77	0	0	0	0	0
93.11	2	1	0	0	0
93.44	4	2	0	1	1
93.78	5	1	2	2	1
94.11	11	4	3	1	1
94.45	9	0	3	2	5
94.78	4	1	2	1	2
95.12	2	0	0	0	1
95.45	1	0	0	1	0
95.79	0	0	0	0	0
96.12	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	7.725	82	93.071	94.201	95.446	0.526	-	-
post10krad	8.158	82	93.063	93.852	94.687	0.484	-	-
post20krad	10.713	82	93.697	94.309	94.897	0.383	-	-
post30krad	6.108	82	93.377	94.281	95.520	0.670	-	-
post40krad	8.146	82	93.330	94.384	95.096	0.507	-	-

E/A CMRR; Vcm0-38; Vin40V

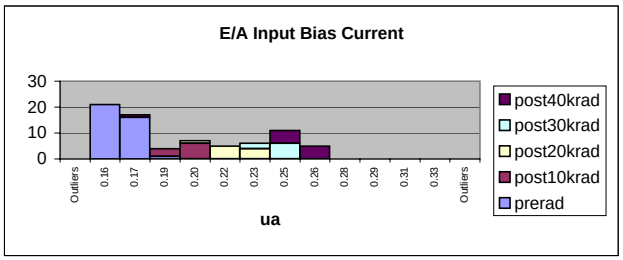
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
97.20	0	0	0	0	0
101.76	0	0	0	0	1
106.32	0	1	0	0	0
110.88	4	1	1	1	1
115.44	8	4	1	0	3
120.00	11	2	4	4	3
124.56	7	1	1	1	1
129.12	5	0	1	1	2
133.68	0	0	1	1	0
138.24	3	0	1	0	0
142.80	0	0	0	0	0
147.36	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	1.954	77	108.892	121.585	140.009	7.607	-	-
post10krad	2.501	77	107.835	116.050	126.649	5.204	-	-
post20krad	1.755	77	110.187	123.279	140.009	8.789	-	-
post30krad	1.996	77	109.325	121.250	132.970	7.388	-	-
post40krad	1.769	77	100.609	118.202	127.593	7.762	-	-

E/A Input Bias Current

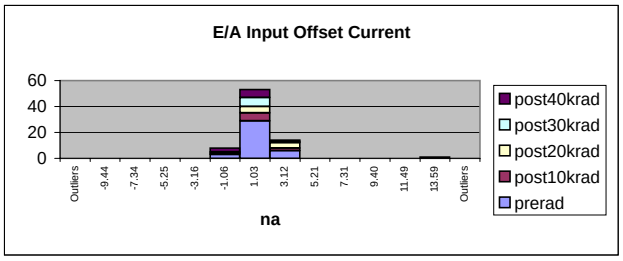
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
0.16	21	0	0	0	0
0.17	16	0	0	0	1
0.19	1	3	0	0	0
0.20	0	6	1	0	0
0.22	0	0	5	0	0
0.23	0	0	4	2	0
0.25	0	0	0	6	5
0.26	0	0	0	0	5
0.28	0	0	0	0	0
0.29	0	0	0	0	0
0.31	0	0	0	0	0
0.33	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	74.689	-0.98	0.156	0.166	0.182	5.11E-03	0.98	53.079
post10krad	79.381	-0.98	0.191	0.198	0.204	4.95E-03	0.98	52.650
post20krad	46.292	-0.98	0.207	0.224	0.236	8.67E-03	0.98	29.084
post30krad	69.001	-0.98	0.232	0.245	0.249	5.92E-03	0.98	41.443
post40krad	14.419	-0.98	0.166	0.248	0.271	0.028	0.98	8.599

E/A Input Offset Current

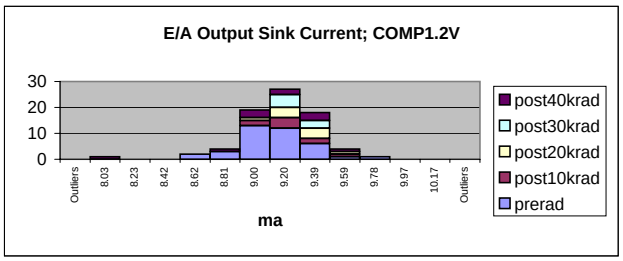
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
-9.44	0	0	0	0	0
-7.34	0	0	0	0	0
-5.25	0	0	0	0	0
-3.16	0	0	0	0	0
-1.06	3	1	1	0	3
1.03	29	6	5	7	6
3.12	6	2	4	1	1
5.21	0	0	0	0	0
7.31	0	0	0	0	0
9.40	0	0	0	0	0
11.49	0	0	0	0	0
13.59	0	0	0	0	1
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	85.634	-245	-0.609	1.199	3.289	0.958	245	84.800
post10krad	56.824	-245	-1.217	1.393	3.773	1.445	245	56.181
post20krad	57.248	-245	-1.340	1.309	3.227	1.434	245	56.639
post30krad	96.294	-245	0.730	1.499	3.469	0.853	245	95.123
post40krad	19.675	-245	-1.643	2.075	13.999	4.186	245	19.345

E/A Output Sink Current; COMP1.2V

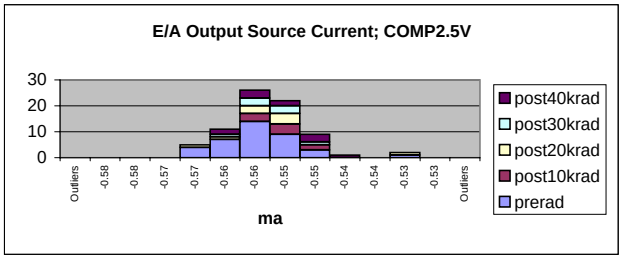
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
8.03	0	0	0	0	1
8.23	0	0	0	0	0
8.42	0	0	0	0	0
8.62	2	0	0	0	0
8.81	3	0	0	0	1
9.00	13	2	1	0	3
9.20	12	4	4	5	2
9.39	6	2	4	3	3
9.59	1	1	1	0	1
9.78	1	0	0	0	0
9.97	0	0	0	0	0
10.17	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	10.069	2.04	8.640	9.133	9.826	0.235	-	-
post10krad	12.896	2.04	8.917	9.208	9.521	0.185	-	-
post20krad	13.882	2.04	9.060	9.313	9.634	0.175	-	-
post30krad	19.745	2.04	9.108	9.274	9.471	0.122	-	-
post40krad	6.065	2.04	8.096	9.101	9.500	0.388	-	-

E/A Output Source Current; COMP2.5V

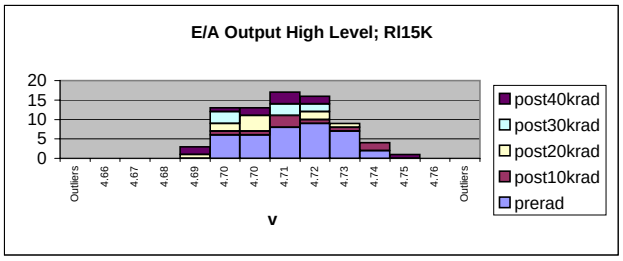
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
-0.58	0	0	0	0	0
-0.58	0	0	0	0	0
-0.57	0	0	0	0	0
-0.57	4	0	1	0	0
-0.56	7	0	1	1	2
-0.56	14	3	3	3	3
-0.55	9	4	4	3	2
-0.55	3	2	0	1	3
-0.54	0	0	0	0	1
-0.54	0	0	0	0	0
-0.53	1	0	1	0	0
-0.53	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	-	-	-0.571	-0.557	-0.532	6.93E-03	-0.408	7.183
post10krad	-	-	-0.561	-0.555	-0.549	4.14E-03	-0.408	11.811
post20krad	-	-	-0.570	-0.556	-0.531	0.010	-0.408	4.786
post30krad	-	-	-0.561	-0.556	-0.548	4.45E-03	-0.408	11.072
post40krad	-	-	-0.565	-0.555	-0.545	7.66E-03	-0.408	6.387

E/A Output High Level; Rl15K

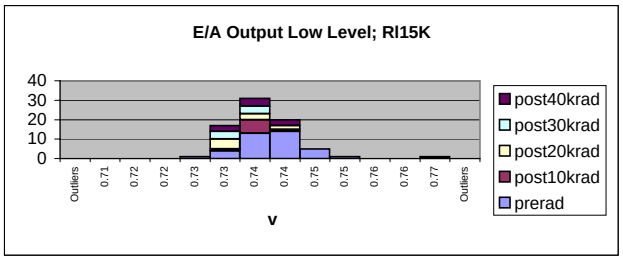
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
4.66	0	0	0	0	0
4.67	0	0	0	0	0
4.68	0	0	0	0	0
4.69	0	0	1	0	2
4.70	6	1	2	3	1
4.70	6	1	4	0	2
4.71	8	3	0	3	3
4.72	9	1	2	2	2
4.73	7	1	1	0	0
4.74	2	2	0	0	0
4.75	0	0	0	0	1
4.76	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	11.137	4.31	4.694	4.715	4.736	0.012	-	-
post10krad	9.848	4.31	4.698	4.718	4.740	0.014	-	-
post20krad	10.326	4.31	4.690	4.707	4.726	0.013	-	-
post30krad	12.615	4.31	4.694	4.708	4.724	0.011	-	-
post40krad	7.931	4.31	4.685	4.707	4.745	0.017	-	-

E/A Output Low Level; RI15K

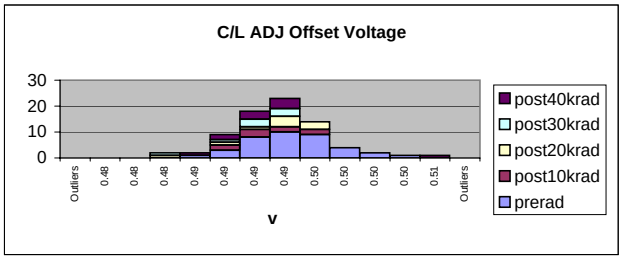
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
0.71	0	0	0	0	0
0.72	0	0	0	0	0
0.72	0	0	0	0	0
0.73	1	0	0	0	0
0.73	4	1	5	4	3
0.74	13	7	3	4	4
0.74	14	1	2	0	3
0.75	5	0	0	0	0
0.75	1	0	0	0	0
0.76	0	0	0	0	0
0.76	0	0	0	0	0
0.77	0	0	0	0	1
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	-	-	0.728	0.739	0.749	5.10E-03	0.97	15.116
post10krad	-	-	0.733	0.737	0.743	2.88E-03	0.97	27.031
post20krad	-	-	0.729	0.735	0.742	3.78E-03	0.97	20.765
post30krad	-	-	0.732	0.734	0.738	2.20E-03	0.97	35.685
post40krad	-	-	0.731	0.739	0.767	9.80E-03	0.97	7.869

C/L ADJ Offset Voltage

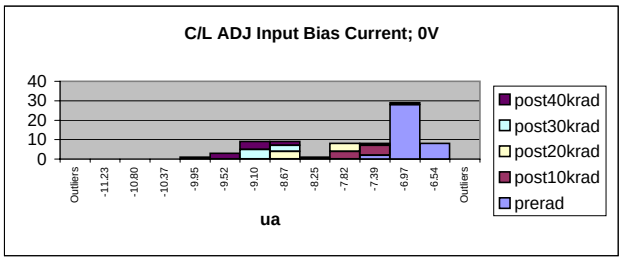
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
0.48	0	0	0	0	0
0.48	0	0	0	0	0
0.48	0	0	1	1	0
0.49	1	0	0	0	1
0.49	3	2	1	1	2
0.49	8	3	1	3	3
0.49	10	2	4	3	4
0.50	9	2	3	0	0
0.50	4	0	0	0	0
0.50	2	0	0	0	0
0.50	1	0	0	0	0
0.51	0	0	0	0	1
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	3.573	0.453	0.486	0.494	0.504	3.81E-03	0.547	4.640
post10krad	4.832	0.453	0.488	0.492	0.496	2.69E-03	0.547	6.827
post20krad	3.436	0.453	0.484	0.492	0.496	3.76E-03	0.547	4.902
post30krad	4.082	0.453	0.484	0.490	0.494	3.05E-03	0.547	6.194
post40krad	2.559	0.453	0.486	0.492	0.506	5.08E-03	0.547	3.615

C/L ADJ Input Bias Current; 0V

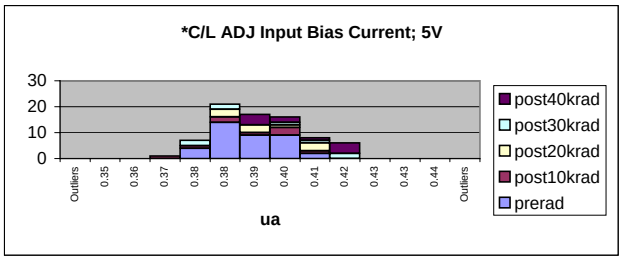
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
-11.23	0	0	0	0	0
-10.80	0	0	0	0	0
-10.37	0	0	0	0	0
-9.95	0	0	0	0	1
-9.52	0	0	0	0	3
-9.10	0	0	0	5	4
-8.67	0	0	4	3	2
-8.25	0	0	1	0	0
-7.82	0	4	4	0	0
-7.39	2	5	1	0	0
-6.97	28	0	0	0	1
-6.54	8	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	40.561	-29.4	-7.348	-6.886	-6.430	0.185	29.4	65.371
post10krad	26.628	-29.4	-7.933	-7.586	-7.199	0.273	29.4	45.149
post20krad	14.588	-29.4	-8.827	-8.188	-7.531	0.485	29.4	25.850
post30krad	28.816	-29.4	-9.191	-8.876	-8.466	0.237	29.4	53.741
post40krad	8.321	-29.4	-9.823	-8.985	-6.857	0.818	29.4	15.645

***C/L ADJ Input Bias Current; 5V**

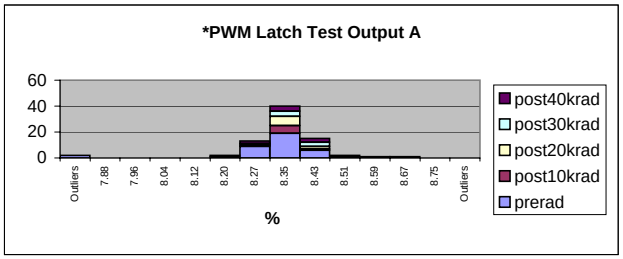
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
0.35	0	0	0	0	0
0.36	0	0	0	0	0
0.37	0	1	0	0	0
0.38	4	1	0	2	0
0.38	14	2	3	2	0
0.39	9	1	3	0	4
0.40	9	3	1	1	2
0.41	2	1	3	1	1
0.42	0	0	0	2	4
0.43	0	0	0	0	0
0.43	0	0	0	0	0
0.44	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	1120.761	-29.4	0.373	0.390	0.407	8.86E-03	29.4	1091.424
post10krad	669.255	-29.4	0.366	0.391	0.413	0.015	29.4	651.679
post20krad	830.918	-29.4	0.381	0.396	0.413	0.012	29.4	808.858
post30krad	597.682	-29.4	0.376	0.396	0.417	0.017	29.4	581.792
post40krad	951.019	-29.4	0.391	0.404	0.419	0.010	29.4	925.212

***PWM Latch Test Output A**

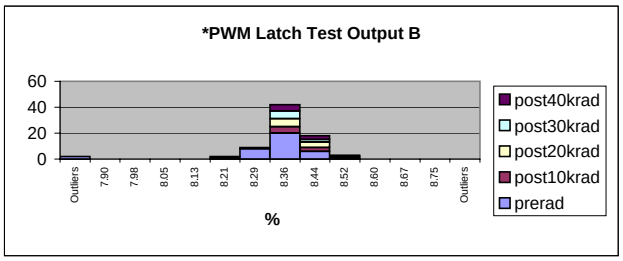
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	2	0	0	0	0
7.88	0	0	0	0	0
7.96	0	0	0	0	0
8.04	0	0	0	0	0
8.12	0	0	0	0	0
8.20	1	0	0	0	1
8.27	9	0	1	1	2
8.35	19	6	7	4	4
8.43	6	1	2	3	3
8.51	1	1	0	0	0
8.59	0	1	0	0	0
8.67	0	0	0	0	1
8.75	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	-	-	7.627	8.314	8.478	0.157	25	35.407
post10krad	-	-	8.345	8.402	8.553	0.071	25	78.386
post20krad	-	-	8.313	8.366	8.452	0.043	25	130.266
post30krad	-	-	8.309	8.381	8.444	0.044	25	124.699
post40krad	-	-	8.233	8.377	8.628	0.107	25	51.665

***PWM Latch Test Output B**

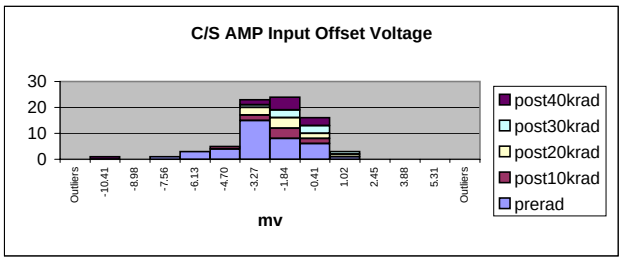
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	2	0	0	0	0
7.90	0	0	0	0	0
7.98	0	0	0	0	0
8.05	0	0	0	0	0
8.13	0	0	0	0	0
8.21	1	0	0	0	1
8.29	8	0	0	0	1
8.36	20	5	6	6	5
8.44	6	3	4	2	3
8.52	1	1	0	0	1
8.60	0	0	0	0	0
8.67	0	0	0	0	0
8.75	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	-	-	7.675	8.325	8.491	0.155	25	35.917
post10krad	-	-	8.366	8.409	8.507	0.044	25	126.053
post20krad	-	-	8.333	8.379	8.424	0.034	25	164.126
post30krad	-	-	8.337	8.387	8.460	0.042	25	133.292
post40krad	-	-	8.233	8.380	8.533	0.084	25	66.081

C/S AMP Input Offset Voltage

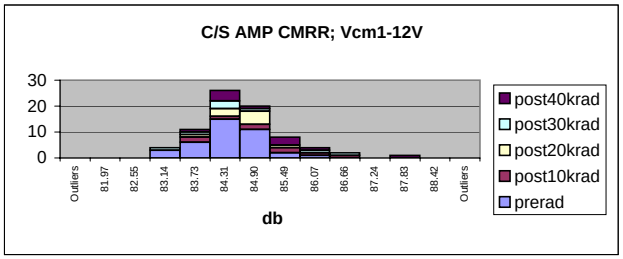
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
-10.41	0	0	0	0	1
-8.98	0	0	0	0	0
-7.56	1	0	0	0	0
-6.13	3	0	0	0	0
-4.70	4	1	0	0	0
-3.27	15	2	3	1	2
-1.84	8	4	4	3	5
-0.41	6	2	2	3	3
1.02	1	0	1	1	0
2.45	0	0	0	0	0
3.88	0	0	0	0	0
5.31	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	4.008	-23.4	-7.115	-2.778	0.482	1.715	23.4	5.087
post10krad	5.686	-23.4	-4.096	-2.079	-0.157	1.250	23.4	6.795
post20krad	4.961	-23.4	-3.835	-1.823	1.097	1.450	23.4	5.800
post30krad	5.783	-23.4	-2.943	-1.375	1.109	1.270	23.4	6.505
post40krad	2.431	-23.4	-10.719	-2.554	0.181	2.858	23.4	3.027

C/S AMP CMRR; Vcm1-12V

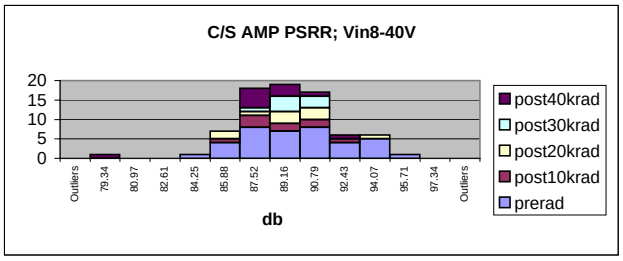
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
81.97	0	0	0	0	0
82.55	0	0	0	0	0
83.14	3	0	0	1	0
83.73	6	2	1	1	1
84.31	15	1	3	3	4
84.90	11	2	5	1	1
85.49	2	2	1	0	3
86.07	1	1	0	1	1
86.66	0	1	0	1	0
87.24	0	0	0	0	0
87.83	0	0	0	0	1
88.42	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	11.084	63	83.241	84.428	86.003	0.644	-	-
post10krad	7.630	63	83.565	84.969	86.367	0.960	-	-
post20krad	12.707	63	83.601	84.667	85.513	0.568	-	-
post30krad	7.155	63	83.329	84.719	86.385	1.012	-	-
post40krad	6.306	63	83.994	85.192	88.098	1.173	-	-

C/S AMP PSRR; Vin8-40V

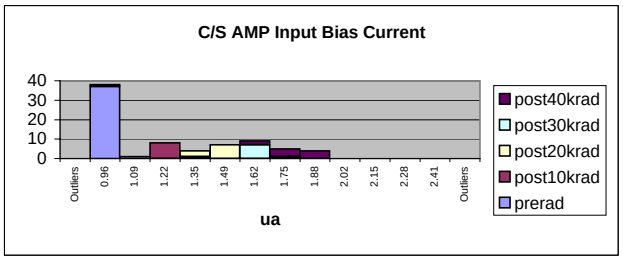
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
79.34	0	0	0	0	1
80.97	0	0	0	0	0
82.61	0	0	0	0	0
84.25	1	0	0	0	0
85.88	4	1	2	0	0
87.52	8	3	1	1	5
89.16	7	2	3	4	3
90.79	8	2	3	3	1
92.43	4	1	0	0	1
94.07	5	0	1	0	0
95.71	1	0	0	0	0
97.34	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	3.240	63	84.610	89.869	95.406	2.764	-	-
post10krad	4.631	63	86.497	88.926	91.724	1.866	-	-
post20krad	3.650	63	85.952	89.197	94.216	2.392	-	-
post30krad	8.084	63	87.440	89.377	90.758	1.088	-	-
post40krad	2.583	63	79.776	88.318	93.141	3.267	-	-

C/S AMP Input Bias Current

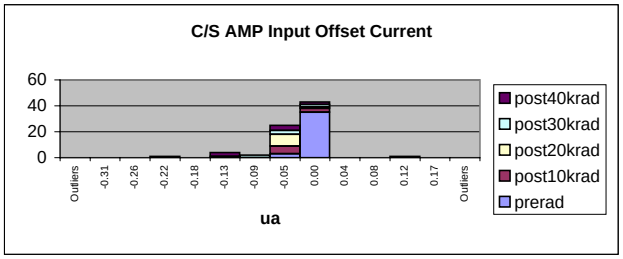
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
0.96	37	0	0	0	1
1.09	1	0	0	0	0
1.22	0	8	0	0	0
1.35	0	1	3	0	0
1.49	0	0	7	0	0
1.62	0	0	0	7	2
1.75	0	0	0	1	4
1.88	0	0	0	0	4
2.02	0	0	0	0	0
2.15	0	0	0	0	0
2.28	0	0	0	0	0
2.41	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	134.916	-9.7	0.918	0.970	1.041	0.026	9.7	110.388
post10krad	120.085	-9.7	1.195	1.240	1.290	0.030	9.7	92.861
post20krad	58.634	-9.7	1.378	1.455	1.552	0.063	9.7	43.343
post30krad	151.376	-9.7	1.619	1.660	1.701	0.025	9.7	107.147
post40krad	14.616	-9.7	0.980	1.700	1.889	0.260	9.7	10.256

C/S AMP Input Offset Current

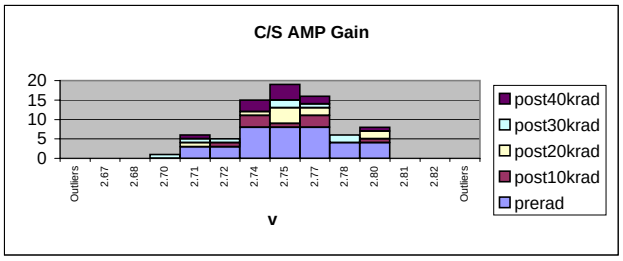
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
-0.31	0	0	0	0	0
-0.26	0	0	0	0	0
-0.22	0	0	0	0	1
-0.18	0	0	0	0	0
-0.13	0	0	0	1	3
-0.09	0	0	0	2	0
-0.05	3	6	9	3	4
0.00	35	3	1	2	2
0.04	0	0	0	0	0
0.08	0	0	0	0	0
0.12	0	0	0	0	1
0.17	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	23.668	-0.7	-0.042	-0.014	0.009	9.66E-03	0.7	24.629
post10krad	25.729	-0.7	-0.043	-0.034	-0.021	8.63E-03	0.7	28.373
post20krad	18.472	-0.7	-0.061	-0.047	-0.024	0.012	0.7	21.142
post30krad	5.019	-0.7	-0.124	-0.067	-0.017	0.042	0.7	6.083
post40krad	2.434	-0.7	-0.238	-0.069	0.105	0.086	0.7	2.969

C/S AMP Gain

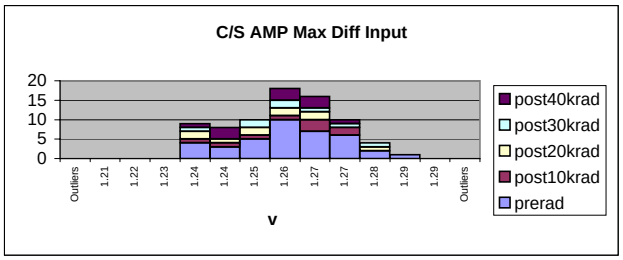
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
2.67	0	0	0	0	0
2.68	0	0	0	0	0
2.70	0	0	0	1	0
2.71	3	0	1	1	1
2.72	3	1	0	1	0
2.74	8	3	1	0	3
2.75	8	1	4	2	4
2.77	8	3	2	1	2
2.78	4	0	0	2	0
2.80	4	1	2	0	1
2.81	0	0	0	0	0
2.82	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	3.402	2.515	2.706	2.755	2.801	0.023	2.985	3.270
post10krad	3.968	2.515	2.729	2.755	2.792	0.020	2.985	3.792
post20krad	3.334	2.515	2.710	2.759	2.793	0.024	2.985	3.094
post30krad	2.676	2.515	2.701	2.745	2.779	0.029	2.985	2.787
post40krad	3.688	2.515	2.714	2.751	2.794	0.021	2.985	3.644

C/S AMP Max Diff Input

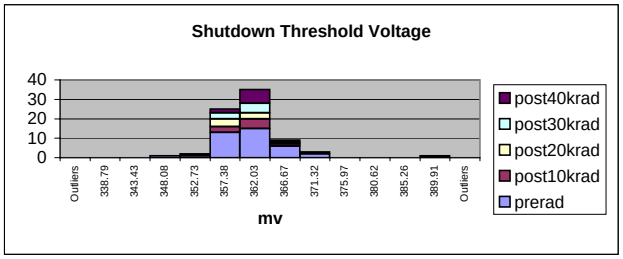
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
1.21	0	0	0	0	0
1.22	0	0	0	0	0
1.23	0	0	0	0	0
1.24	4	1	2	1	1
1.24	3	1	1	0	3
1.25	5	1	2	2	0
1.26	10	1	2	2	3
1.27	7	3	2	1	3
1.27	6	2	0	1	1
1.28	2	0	1	1	0
1.29	1	0	0	0	0
1.29	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	3.635	1.12	1.235	1.259	1.284	0.013	-	-
post10krad	4.079	1.12	1.239	1.259	1.275	0.011	-	-
post20krad	3.111	1.12	1.236	1.254	1.282	0.014	-	-
post30krad	3.629	1.12	1.240	1.260	1.280	0.013	-	-
post40krad	3.690	1.12	1.234	1.255	1.273	0.012	-	-

Shutdown Threshold Voltage

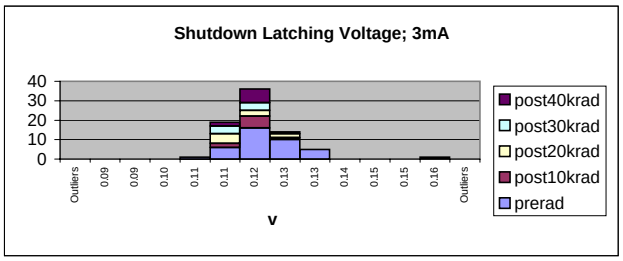
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
338.79	0	0	0	0	0
343.43	0	0	0	0	0
348.08	1	0	0	0	0
352.73	1	0	1	0	0
357.38	13	3	4	3	2
362.03	15	5	3	5	7
366.67	6	1	1	0	1
371.32	2	0	1	0	0
375.97	0	0	0	0	0
380.62	0	0	0	0	0
385.26	0	0	0	0	0
389.91	0	0	0	0	1
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	7.757	254	347.383	360.942	370.674	4.595	396	2.543
post10krad	16.686	254	358.035	360.414	364.682	2.126	396	5.580
post20krad	6.795	254	350.831	360.826	369.634	5.240	396	2.237
post30krad	16.281	254	357.652	360.628	363.670	2.183	396	5.401
post40krad	3.957	254	356.044	364.350	390.968	9.296	396	1.135

Shutdown Latching Voltage; 3mA

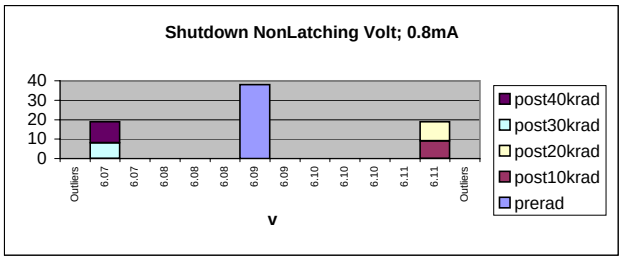
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
0.09	0	0	0	0	0
0.09	0	0	0	0	0
0.10	0	0	0	0	0
0.11	1	0	0	0	0
0.11	6	2	5	4	2
0.12	16	6	3	4	7
0.13	10	1	2	0	1
0.13	5	0	0	0	0
0.14	0	0	0	0	0
0.15	0	0	0	0	0
0.15	0	0	0	0	0
0.16	0	0	0	0	1
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	-	-	0.112	0.123	0.137	6.06E-03	1.995	102.969
post10krad	-	-	0.116	0.120	0.127	3.64E-03	1.995	171.616
post20krad	-	-	0.116	0.120	0.125	3.49E-03	1.995	179.242
post30krad	-	-	0.115	0.119	0.124	3.17E-03	1.995	197.064
post40krad	-	-	0.117	0.125	0.163	0.013	1.995	46.800

Shutdown NonLatching Volt; 0.8mA

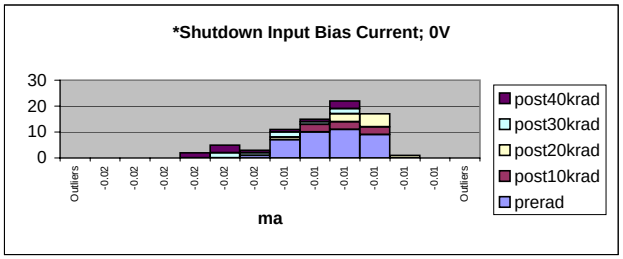
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
6.07	0	0	0	8	11
6.07	0	0	0	0	0
6.08	0	0	0	0	0
6.08	0	0	0	0	0
6.08	0	0	0	0	0
6.09	38	0	0	0	0
6.09	0	0	0	0	0
6.10	0	0	0	0	0
6.10	0	0	0	0	0
6.10	0	0	0	0	0
6.11	0	0	0	0	0
6.11	0	9	10	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	1161.710	5.01	6.088	6.089	6.090	3.10E-04	7	980.189
post10krad	662.367	5.01	6.111	6.112	6.113	5.55E-04	7	533.849
post20krad	634.562	5.01	6.111	6.112	6.113	5.79E-04	7	511.314
post30krad	1364.395	5.01	6.069	6.069	6.069	2.59E-04	7	1198.968
post40krad	742.986	5.01	6.068	6.069	6.069	4.75E-04	7	653.470

***Shutdown Input Bias Current; 0V**

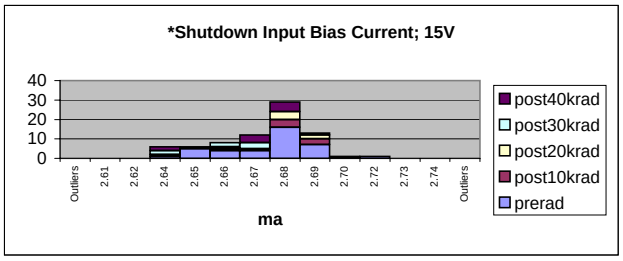
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
-0.02	0	0	0	0	0
-0.02	0	0	0	0	0
-0.02	0	0	0	0	0
-0.02	0	0	0	0	2
-0.02	0	0	0	2	3
-0.02	1	0	0	1	1
-0.01	7	0	1	2	1
-0.01	10	3	0	1	1
-0.01	11	3	3	2	3
-0.01	9	3	5	0	0
-0.01	0	0	1	0	0
-0.01	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	326.151	-1	-0.015	-0.013	-0.011	1.01E-03	0.99	331.427
post10krad	461.549	-1	-0.014	-0.013	-0.011	7.13E-04	0.99	468.571
post20krad	332.544	-1	-0.014	-0.012	-0.011	9.90E-04	0.99	337.182
post30krad	197.650	-1	-0.016	-0.014	-0.012	1.66E-03	0.99	201.436
post40krad	162.453	-1	-0.018	-0.015	-0.013	2.02E-03	0.99	165.785

***Shutdown Input Bias Current; 15V**

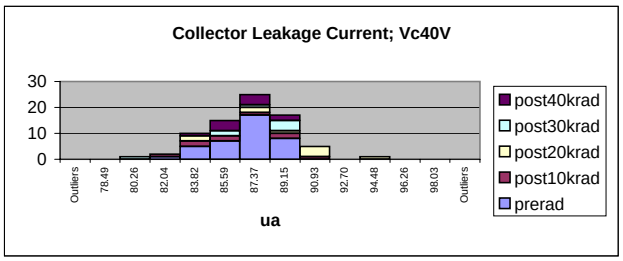
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
2.61	0	0	0	0	0
2.62	0	0	0	0	0
2.64	1	0	1	2	2
2.65	5	0	1	0	0
2.66	4	1	1	2	0
2.67	4	1	0	3	4
2.68	16	4	4	0	5
2.69	7	3	2	1	0
2.70	0	0	1	0	0
2.72	1	0	0	0	0
2.73	0	0	0	0	0
2.74	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	32.402	1	2.640	2.676	2.716	0.017	4.99	44.752
post10krad	55.024	1	2.663	2.682	2.695	0.010	4.99	75.525
post20krad	24.374	1	2.638	2.676	2.711	0.023	4.99	33.641
post30krad	33.843	1	2.640	2.663	2.691	0.016	4.99	47.353
post40krad	32.370	1	2.637	2.671	2.686	0.017	4.99	44.935

Collector Leakage Current; Vc40V

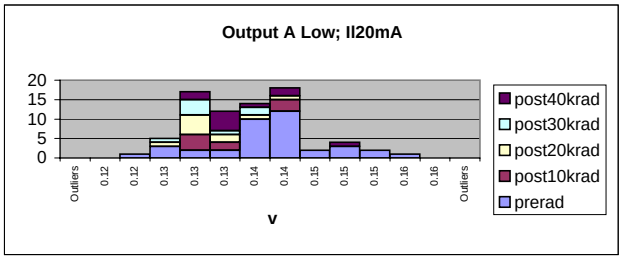
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
78.49	0	0	0	0	0
80.26	0	0	0	1	0
82.04	1	1	0	0	0
83.82	5	2	2	0	1
85.59	7	2	0	2	4
87.37	17	1	2	1	4
89.15	8	2	1	4	2
90.93	0	1	4	0	0
92.70	0	0	0	0	0
94.48	0	0	1	0	0
96.26	0	0	0	0	0
98.03	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	-	-	82.743	86.735	88.907	1.534	170	18.090
post10krad	-	-	81.904	86.531	90.981	2.978	170	9.344
post20krad	-	-	83.180	88.952	93.614	3.324	170	8.129
post30krad	-	-	80.776	86.603	88.640	2.822	170	9.850
post40krad	-	-	84.125	86.634	89.232	1.638	170	16.962

Output A Low; Il20mA

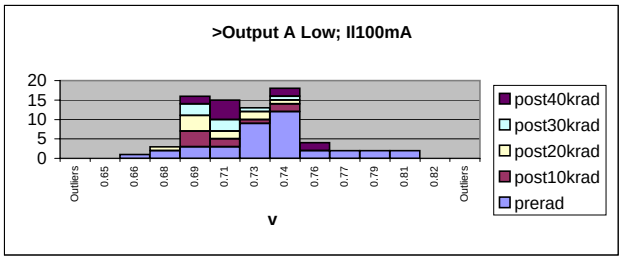
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
0.12	0	0	0	0	0
0.12	1	0	0	0	0
0.13	3	0	1	1	0
0.13	2	4	5	4	2
0.13	2	2	2	1	5
0.14	10	0	1	2	1
0.14	12	3	1	0	2
0.15	2	0	0	0	0
0.15	3	0	0	0	1
0.15	2	0	0	0	0
0.16	1	0	0	0	0
0.16	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	-	-	0.124	0.140	0.159	7.98E-03	0.392	10.508
post10krad	-	-	0.130	0.136	0.144	5.74E-03	0.392	14.883
post20krad	-	-	0.128	0.134	0.143	4.82E-03	0.392	17.863
post30krad	-	-	0.127	0.133	0.140	4.78E-03	0.392	18.078
post40krad	-	-	0.130	0.136	0.149	6.00E-03	0.392	14.203

>Output A Low; Il100mA

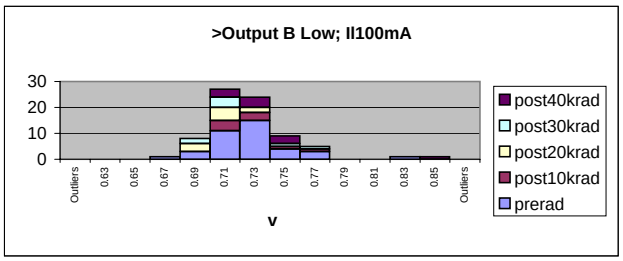
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
0.65	0	0	0	0	0
0.66	1	0	0	0	0
0.68	2	0	1	0	0
0.69	3	4	4	3	2
0.71	3	2	2	3	5
0.73	9	1	2	1	0
0.74	12	2	1	1	2
0.76	2	0	0	0	2
0.77	2	0	0	0	0
0.79	2	0	0	0	0
0.81	2	0	0	0	0
0.82	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	-	-	0.665	0.734	0.803	0.032	2.09	14.101
post10krad	-	-	0.689	0.714	0.749	0.023	2.09	19.875
post20krad	-	-	0.685	0.708	0.743	0.018	2.09	26.250
post30krad	-	-	0.686	0.708	0.736	0.018	2.09	25.388
post40krad	-	-	0.690	0.720	0.760	0.024	2.09	18.884

>Output B Low; Il100mA

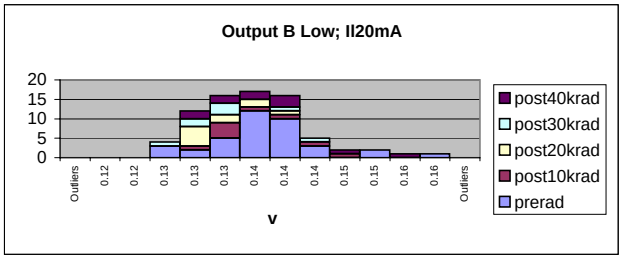
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
0.63	0	0	0	0	0
0.65	0	0	0	0	0
0.67	1	0	0	0	0
0.69	3	0	3	2	0
0.71	11	4	5	4	3
0.73	15	3	2	0	4
0.75	4	1	0	1	3
0.77	3	1	0	1	0
0.79	0	0	0	0	0
0.81	0	0	0	0	0
0.83	1	0	0	0	0
0.85	0	0	0	0	1
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	-	-	0.663	0.724	0.825	0.028	2.09	16.117
post10krad	-	-	0.697	0.721	0.769	0.025	2.09	18.102
post20krad	-	-	0.684	0.703	0.728	0.015	2.09	30.407
post30krad	-	-	0.686	0.714	0.756	0.023	2.09	20.260
post40krad	-	-	0.698	0.735	0.839	0.040	2.09	11.295

Output B Low; Il20mA

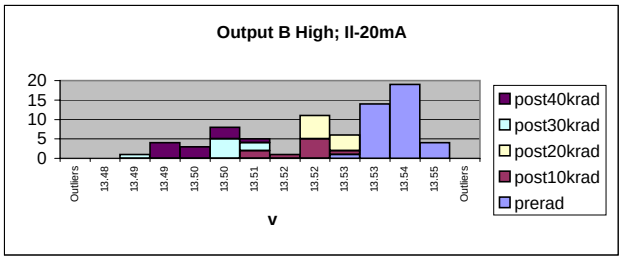
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
0.12	0	0	0	0	0
0.12	0	0	0	0	0
0.13	3	0	0	1	0
0.13	2	1	5	2	2
0.13	5	4	2	3	2
0.14	12	1	2	0	2
0.14	10	1	1	1	3
0.14	3	1	0	1	0
0.15	0	1	0	0	1
0.15	2	0	0	0	0
0.16	0	0	0	0	1
0.16	1	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	-	-	0.123	0.138	0.159	7.03E-03	0.392	12.042
post10krad	-	-	0.130	0.137	0.149	6.31E-03	0.392	13.500
post20krad	-	-	0.127	0.132	0.140	4.03E-03	0.392	21.525
post30krad	-	-	0.127	0.133	0.144	5.79E-03	0.392	14.878
post40krad	-	-	0.130	0.139	0.156	7.67E-03	0.392	11.013

Output B High; Il-20mA

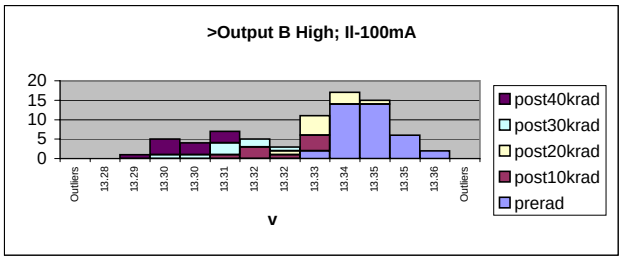
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
13.48	0	0	0	0	0
13.49	0	0	0	1	0
13.49	0	0	0	0	4
13.50	0	0	0	0	3
13.50	0	0	0	5	3
13.51	0	2	0	2	1
13.52	0	1	0	0	0
13.52	0	5	6	0	0
13.53	1	1	4	0	0
13.53	14	0	0	0	0
13.54	19	0	0	0	0
13.55	4	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	44.908	13.045	13.527	13.537	13.547	3.66E-03	-	-
post10krad	30.404	13.045	13.512	13.519	13.527	5.19E-03	-	-
post20krad	66.236	13.045	13.519	13.524	13.527	2.41E-03	-	-
post30krad	19.548	13.045	13.484	13.502	13.509	7.80E-03	-	-
post40krad	21.606	13.045	13.489	13.497	13.512	6.98E-03	-	-

>Output B High; Il-100mA

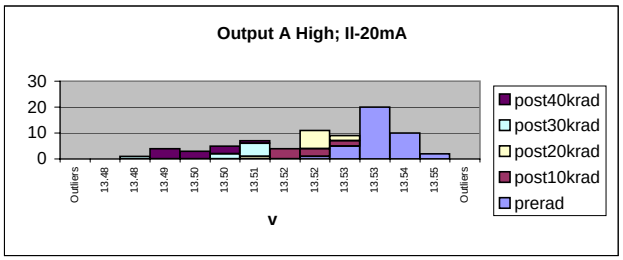
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
13.28	0	0	0	0	0
13.29	0	0	0	0	1
13.30	0	0	0	1	4
13.30	0	0	0	1	3
13.31	0	1	0	3	3
13.32	0	3	0	2	0
13.32	0	1	1	1	0
13.33	2	4	5	0	0
13.34	14	0	3	0	0
13.35	14	0	1	0	0
13.35	6	0	0	0	0
13.36	2	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	68.095	12.03	13.334	13.345	13.359	6.44E-03	-	-
post10krad	53.058	12.03	13.313	13.325	13.335	8.14E-03	-	-
post20krad	89.363	12.03	13.325	13.335	13.343	4.87E-03	-	-
post30krad	43.219	12.03	13.292	13.310	13.324	9.87E-03	-	-
post40krad	53.184	12.03	13.288	13.301	13.312	7.97E-03	-	-

Output A High; Il-20mA

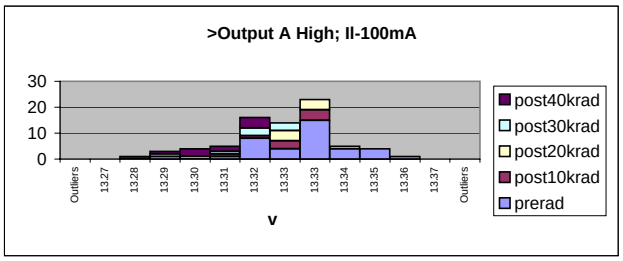
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
13.48	0	0	0	0	0
13.48	0	0	0	1	0
13.49	0	0	0	0	4
13.50	0	0	0	0	3
13.50	0	0	0	2	3
13.51	0	0	1	5	1
13.52	0	4	0	0	0
13.52	1	3	7	0	0
13.53	5	2	2	0	0
13.53	20	0	0	0	0
13.54	10	0	0	0	0
13.55	2	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	33.563	13.045	13.522	13.535	13.547	4.87E-03	-	-
post10krad	28.153	13.045	13.513	13.519	13.529	5.62E-03	-	-
post20krad	40.251	13.045	13.512	13.523	13.528	3.95E-03	-	-
post30krad	18.757	13.045	13.484	13.504	13.509	8.15E-03	-	-
post40krad	20.298	13.045	13.488	13.498	13.512	7.43E-03	-	-

>Output A High; Il-100mA

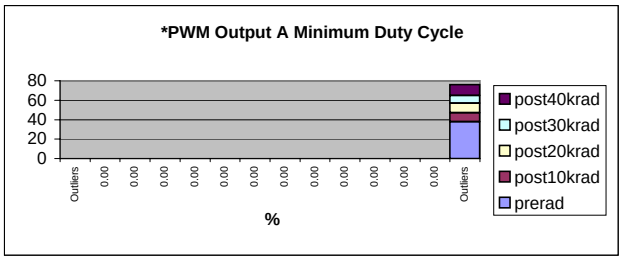
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
13.27	0	0	0	0	0
13.28	0	0	0	0	1
13.29	1	0	0	1	1
13.30	0	0	1	0	3
13.31	1	1	0	1	2
13.32	8	1	0	3	4
13.33	4	3	4	3	0
13.33	15	4	4	0	0
13.34	4	0	1	0	0
13.35	4	0	0	0	0
13.36	1	0	0	0	0
13.37	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	29.442	12.03	13.290	13.332	13.362	0.015	-	-
post10krad	42.497	12.03	13.309	13.327	13.338	0.010	-	-
post20krad	37.452	12.03	13.301	13.329	13.341	0.012	-	-
post30krad	39.799	12.03	13.290	13.315	13.323	0.011	-	-
post40krad	34.463	12.03	13.281	13.303	13.319	0.012	-	-

***PWM Output A Minimum Duty Cycle**

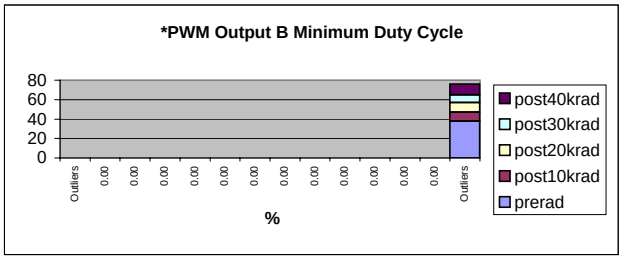
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
Outliers	38	9	10	8	11



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	-	-	0.000	0.000	0.000	0.00E+00	0.001	Infinite
post10krad	-	-	0.000	0.000	0.000	0.00E+00	0.001	Infinite
post20krad	-	-	0.000	0.000	0.000	0.00E+00	0.001	Infinite
post30krad	-	-	0.000	0.000	0.000	0.00E+00	0.001	Infinite
post40krad	-	-	0.000	0.000	0.000	0.00E+00	0.001	Infinite

***PWM Output B Minimum Duty Cycle**

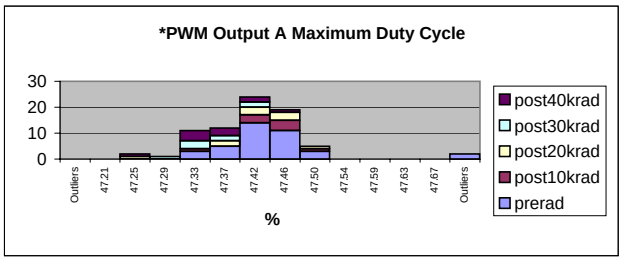
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
0.00	0	0	0	0	0
Outliers	38	9	10	8	11



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	-	-	0.000	0.000	0.000	0.00E+00	0.001	Infinite
post10krad	-	-	0.000	0.000	0.000	0.00E+00	0.001	Infinite
post20krad	-	-	0.000	0.000	0.000	0.00E+00	0.001	Infinite
post30krad	-	-	0.000	0.000	0.000	0.00E+00	0.001	Infinite
post40krad	-	-	0.000	0.000	0.000	0.00E+00	0.001	Infinite

***PWM Output A Maximum Duty Cycle**

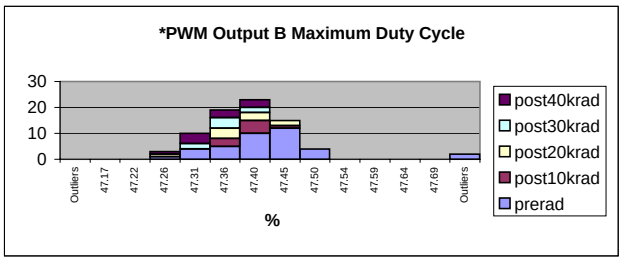
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
47.21	0	0	0	0	0
47.25	0	0	1	0	1
47.29	0	0	0	1	0
47.33	3	1	0	3	4
47.37	5	0	2	2	3
47.42	14	3	3	2	2
47.46	11	4	3	0	1
47.50	3	1	1	0	0
47.54	0	0	0	0	0
47.59	0	0	0	0	0
47.63	0	0	0	0	0
47.67	0	0	0	0	0
Outliers	2	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	9.688	45.05	47.327	47.444	47.757	0.082	-	-
post10krad	16.098	45.05	47.339	47.439	47.501	0.049	-	-
post20krad	11.610	45.05	47.259	47.410	47.495	0.068	-	-
post30krad	17.711	45.05	47.291	47.357	47.431	0.043	-	-
post40krad	13.199	45.05	47.236	47.359	47.461	0.058	-	-

***PWM Output B Maximum Duty Cycle**

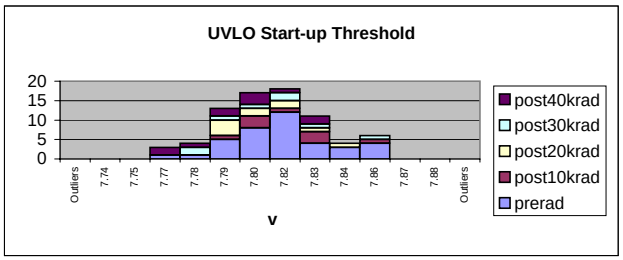
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
47.17	0	0	0	0	0
47.22	0	0	0	0	0
47.26	1	0	1	0	1
47.31	4	0	0	2	4
47.36	5	3	4	4	3
47.40	10	5	3	2	3
47.45	12	1	2	0	0
47.50	4	0	0	0	0
47.54	0	0	0	0	0
47.59	0	0	0	0	0
47.64	0	0	0	0	0
47.69	0	0	0	0	0
Outliers	2	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	8.441	45.05	47.282	47.427	47.778	0.094	-	-
post10krad	21.931	45.05	47.339	47.397	47.456	0.036	-	-
post20krad	14.603	45.05	47.282	47.385	47.472	0.053	-	-
post30krad	21.000	45.05	47.292	47.352	47.404	0.037	-	-
post40krad	17.549	45.05	47.281	47.348	47.408	0.044	-	-

UVLO Start-up Threshold

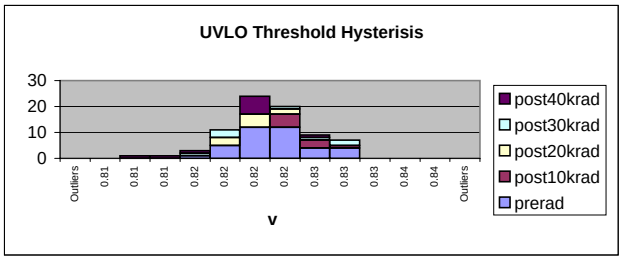
Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
7.74	0	0	0	0	0
7.75	0	0	0	0	0
7.77	1	0	0	0	2
7.78	1	0	0	2	1
7.79	5	1	4	1	2
7.80	8	3	2	1	3
7.82	12	1	2	2	1
7.83	4	3	1	1	2
7.84	3	0	1	0	0
7.86	4	1	0	1	0
7.87	0	0	0	0	0
7.88	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	28.990	6.01	7.765	7.818	7.855	0.021	7.99	2.765
post10krad	28.927	6.01	7.795	7.823	7.862	0.021	7.99	2.665
post20krad	30.565	6.01	7.785	7.807	7.846	0.020	7.99	3.110
post30krad	23.118	6.01	7.782	7.812	7.861	0.026	7.99	2.278
post40krad	26.561	6.01	7.769	7.800	7.834	0.022	7.99	2.816

UVLO Threshold Hysterisis

Bin	prerad	post10krad	post20krad	post30krad	post40krad
Outliers	0	0	0	0	0
0.81	0	0	0	0	0
0.81	0	0	0	0	1
0.81	0	0	0	0	1
0.82	1	0	0	1	1
0.82	5	0	3	3	0
0.82	12	0	5	0	7
0.82	12	5	2	1	0
0.83	4	3	0	1	1
0.83	4	1	0	2	0
0.83	0	0	0	0	0
0.84	0	0	0	0	0
0.84	0	0	0	0	0
Outliers	0	0	0	0	0



	Cpk(LL)	LL	Min	Avg	Max	Sigma	UL	Cpk(UL)
prerad	66.690	0.11	0.816	0.824	0.831	3.57E-03	2	109.894
post10krad	113.049	0.11	0.823	0.826	0.829	2.11E-03	2	185.506
post20krad	113.964	0.11	0.818	0.822	0.825	2.08E-03	2	188.752
post30krad	42.676	0.11	0.817	0.823	0.831	5.57E-03	2	70.404
post40krad	51.386	0.11	0.812	0.820	0.827	4.61E-03	2	85.350

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