

From 112G/224G PAM4 SerDes Outputs

156.25 MHz, LVPECL, PHY Recovered

25 MHz, LVDS, PHY Recovered or Local

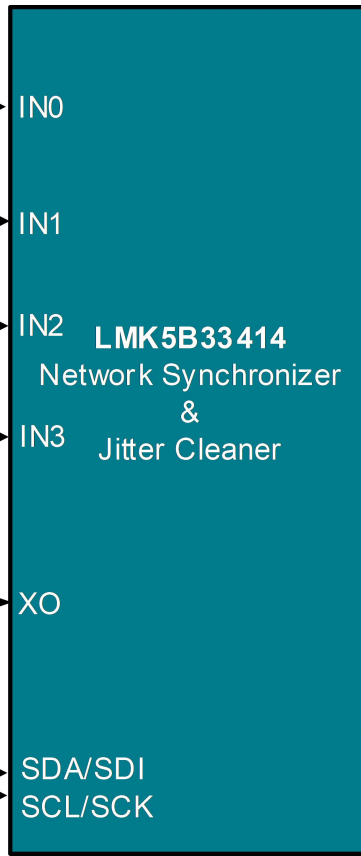
100MHz, LVDS, PHY Backup

1PPS, LVCMOS

48 MHz, LVCMOS

LMK6CE4800x

I2C/SPI



156.25/312.5 MHz, HSDS, Network
156.25 MHz, LVDS, Mgmt. Reference

50 MHz, HSDS, Core

25 MHz, LVDS, Sync

1-PPS, 1.8-V LVCMOS, Test

1-PPS, 1.8-V LVCMOS, IEEE-1588 CPU Sync

25 MHz, HSDS, IEEE-1588 CPU Sync

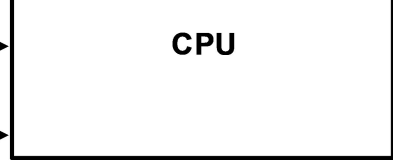


25 MHz, LVDS, IEEE-1588 Sync PLL

25 MHz, LVDS, IEEE-1588 Sync PLL

25 MHz, LVDS, IEEE-1588 TimeStamp PLL

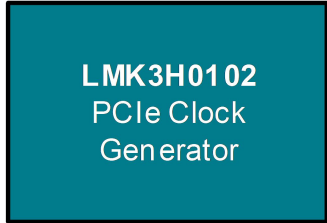
25 MHz, LVDS, IEEE-1588 Test



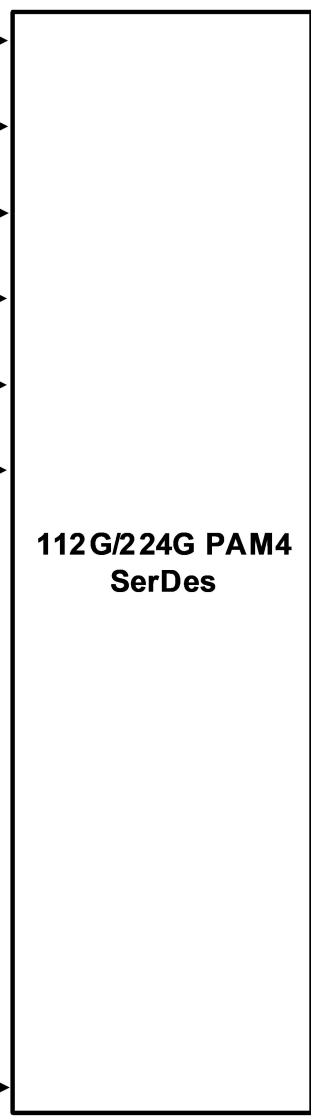
25 MHz, LVCMOS, CPLD

100 MHz, LP-HCSL, PCIe

100 MHz, LP-HCSL, PCIe



4x to 10x



156.25 MHz, LVPECL, PHY Recovered

25 MHz, LVDS, PHY Recovered or Local

To LMK5B33216 DPLL Inputs

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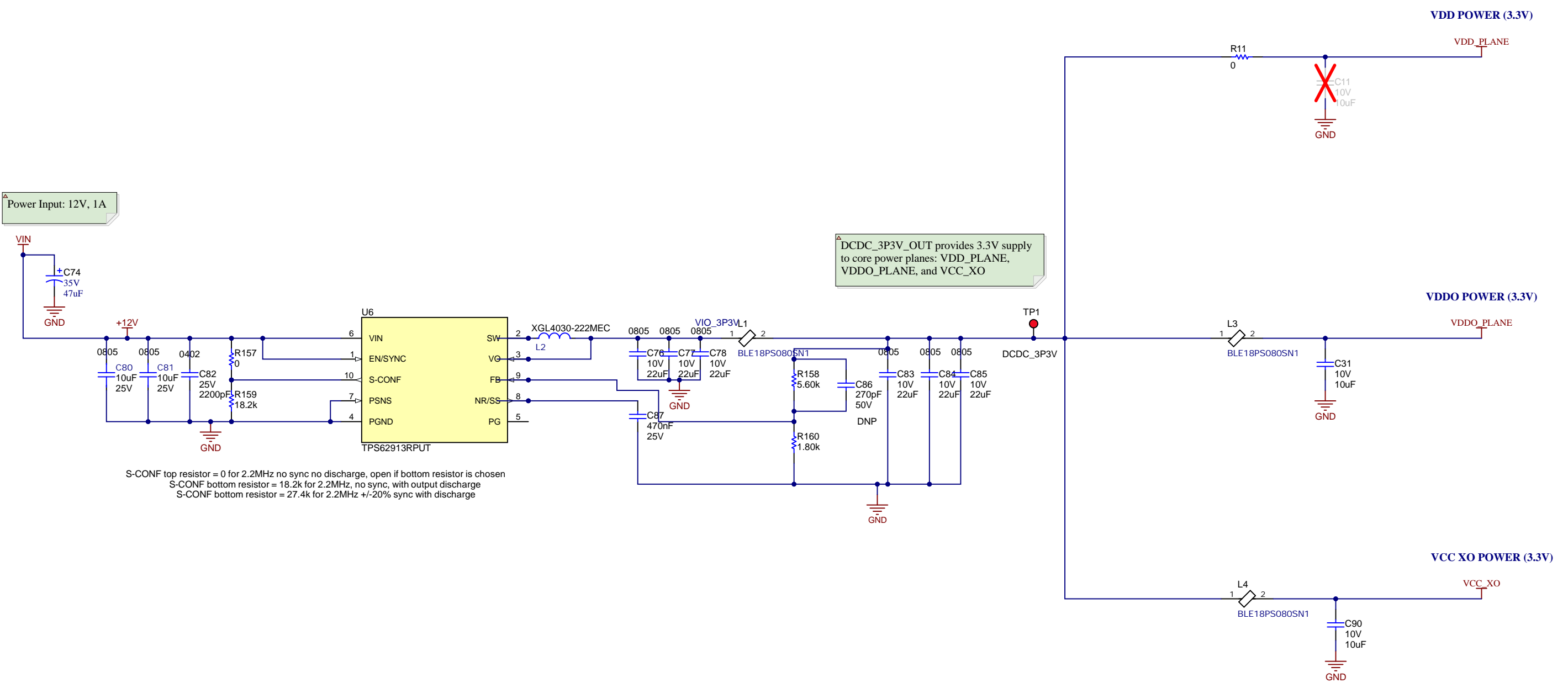
Orderable: Multi EVMs	Designed for: Public Release	Mod. Date: 9/23/2024
TID #: N/A	Project Title: Tomahawk 5 Network Switch Reference Design	
Number: N/A	Rev: A	Sheet Title: Network Switch Block Diagram
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 1 of 7
Drawn By: Riley Nguyen	File: Network Switch Block Diagram.SchDoc	Size: B
Engineer: Riley Nguyen	Contact: https://e2e.ti.com/	

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Power Input: 12V, 1A

DCDC_3P3V_OUT provides 3.3V supply to core power planes: VDD_PLANE, VDDO_PLANE, and VCC_XO

S-CONF top resistor = 0 for 2.2MHz no sync no discharge, open if bottom resistor is chosen
 S-CONF bottom resistor = 18.2k for 2.2MHz, no sync, with output discharge
 S-CONF bottom resistor = 27.4k for 2.2MHz +/-20% sync with discharge



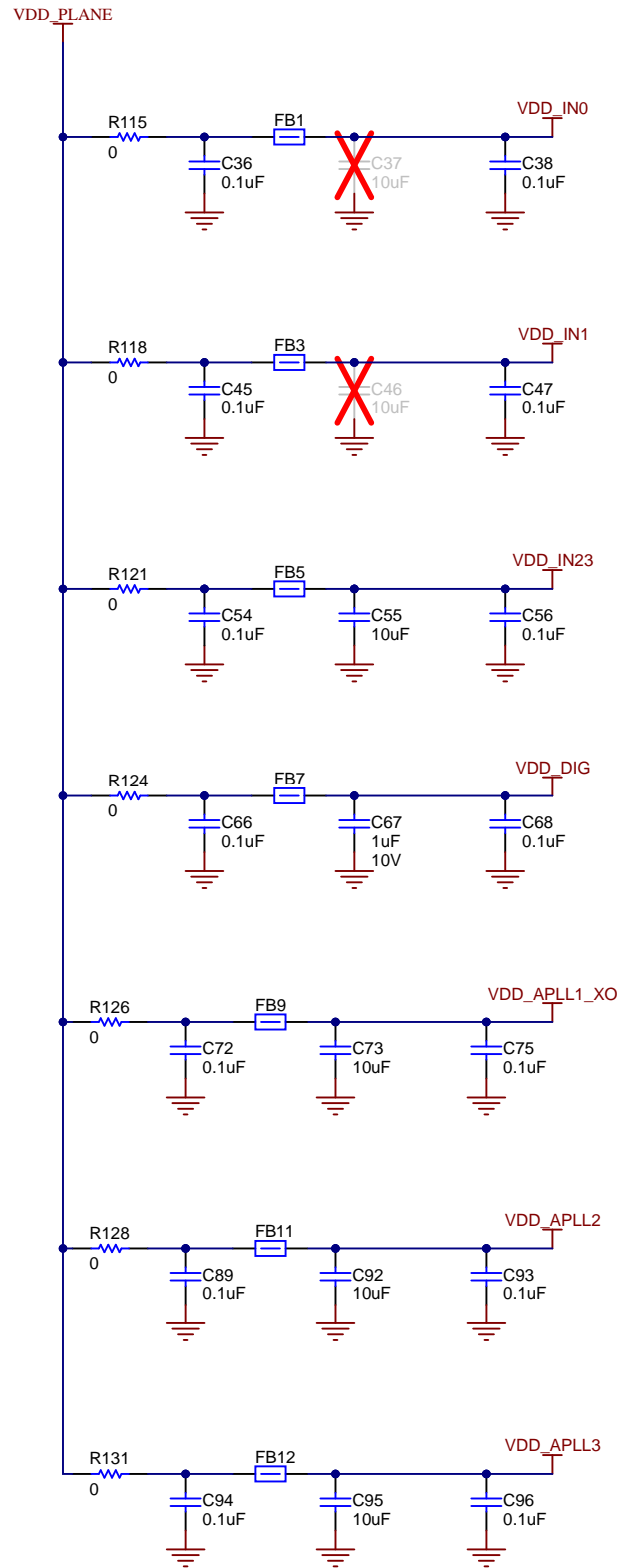
Orderable: Multi EVMs	Designed for: Public Release	Mod. Date: 9/23/2024
TID #: N/A	Project Title: Tomahawk 5 Network Switch Reference Design	
Number: N/A	Rev: A	Sheet Title: Power Supply
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 2 of 7
Drawn By: Riley Nguyen	File: Power_Supply_SchDoc	Size: B
Engineer: Riley Nguyen	Contact: https://e2e.ti.com/	

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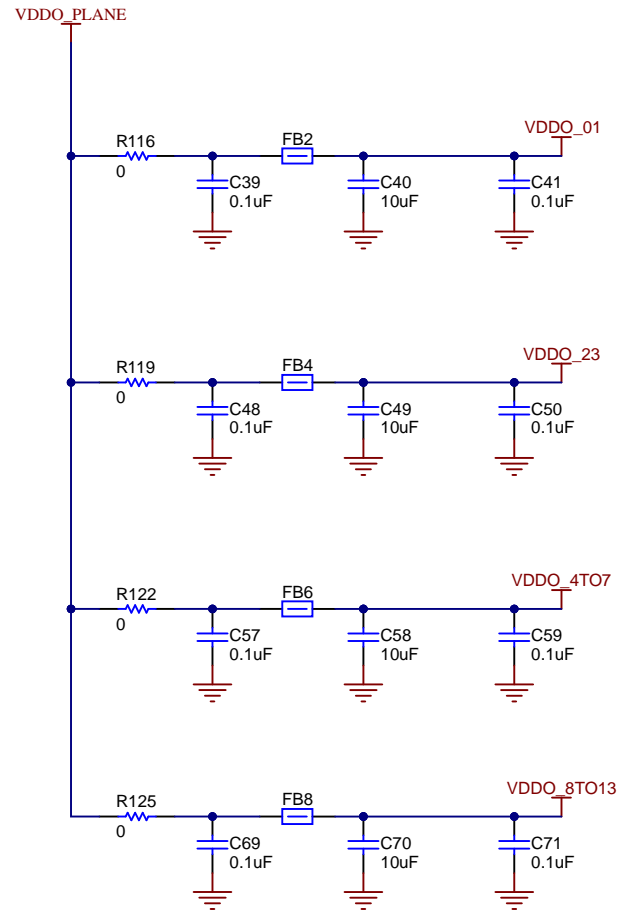


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LMK5B33414 VDD CORE SUPPLY

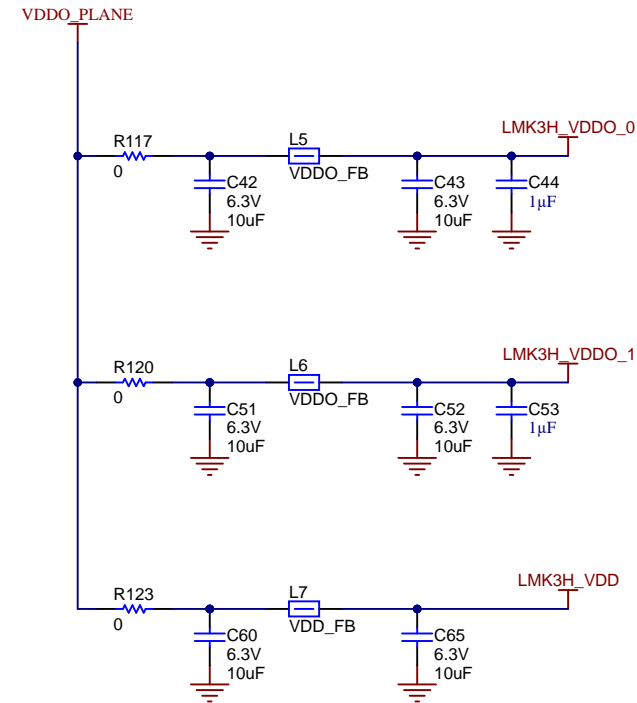


LMK5B33414 VDDO OUTPUT SUPPLY



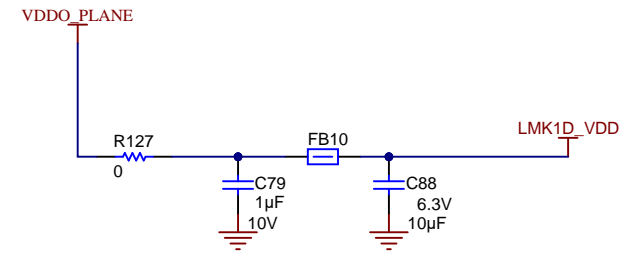
Place C38, C47, C56, C68, C75, C93, C96, C41, C50, C59, C71 close to LMK3B33414

LMK3H0102 VDD & VDDO SUPPLY

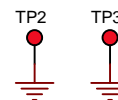


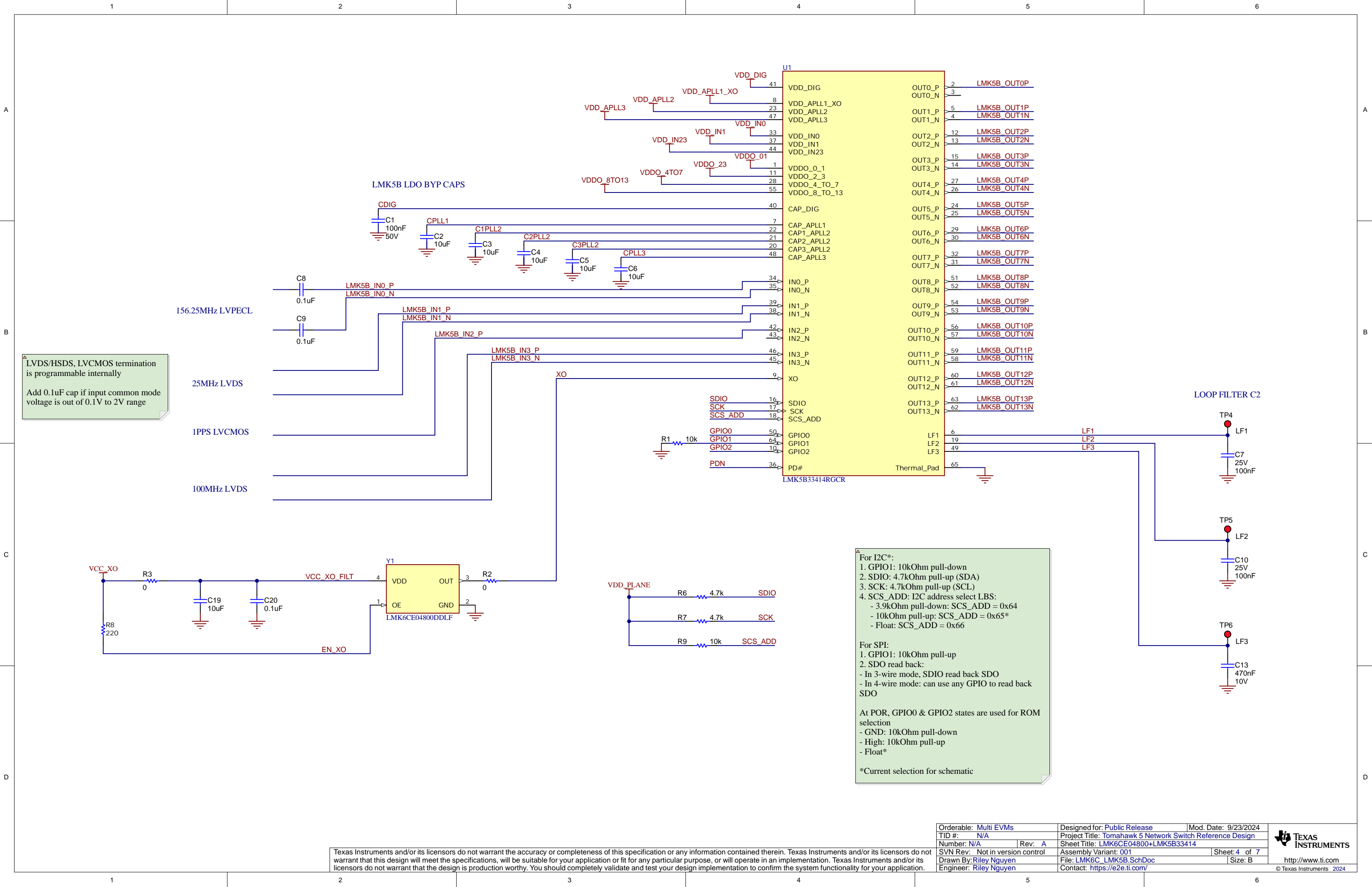
Place C44, C53 close to LMK3H0102

LMK1D1204 LDD SUPPLY



GND TEST POINTS





LVDS/HSDS, LVCMOS termination is programmable internally
 Add 0.1uF cap if input common mode voltage is out of 0.1V to 2V range

For I2C*:
 1. GPIO1: 10kOhm pull-down
 2. SDIO: 4.7kOhm pull-up (SDA)
 3. SCK: 4.7kOhm pull-up (SCL)
 4. SCS_ADD: I2C address select LBS:
 - 3.9kOhm pull-down: SCS_ADD = 0x64
 - 10kOhm pull-up: SCS_ADD = 0x65*
 - Float: SCS_ADD = 0x66

For SPI:
 1. GPIO1: 10kOhm pull-up
 2. SDO read back:
 - In 3-wire mode, SDIO read back SDO
 - In 4-wire mode: can use any GPIO to read back SDO

At POR, GPIO0 & GPIO2 states are used for ROM selection
 - GND: 10kOhm pull-down
 - High: 10kOhm pull-up
 - Float*

*Current selection for schematic

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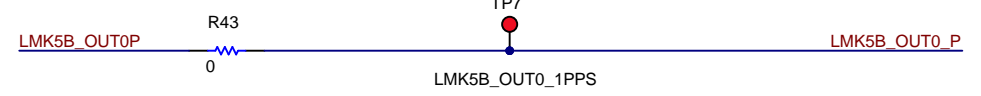
Orderable: Multi EVMs	Designed for: Public Release	Mod. Date: 9/23/2024
TID #: N/A	Project Title: Tomahawk 5 Network Switch Reference Design	
Number: N/A	Rev: A	Sheet Title: LMK6CE04800+LMK5B33414
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 4 of 7
Drawn By: Riley Nguyen	File: LMK6C_LMK5B_SchDoc	Size: B
Engineer: Riley Nguyen	Contact: https://e2e.ti.com/	



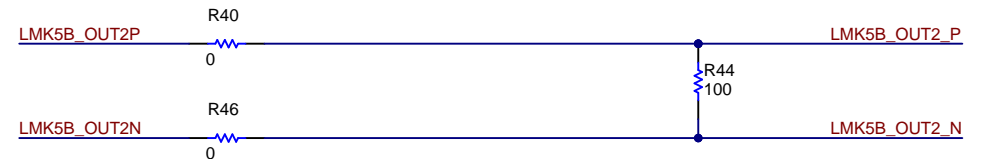
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1. 100Ohm load is not present internally
Place external 100Ohm load close to receiver side

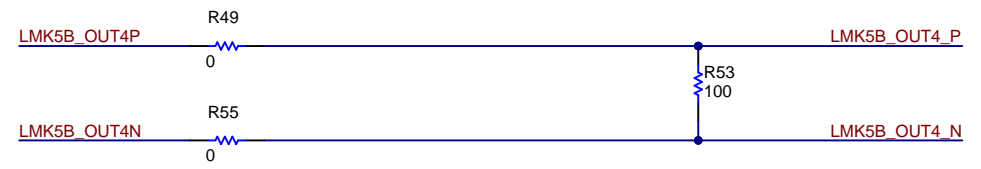
2. Termination on OUT3 is placed close to LMK1D1204 IN0



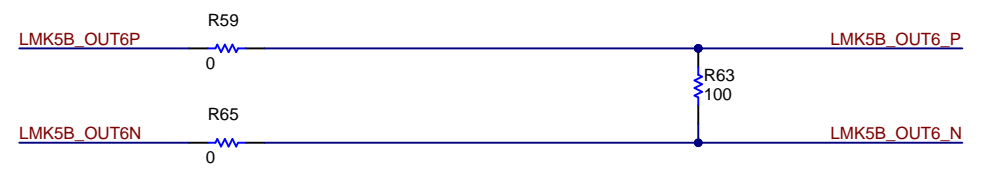
1PPS LVCMOS
To CPU



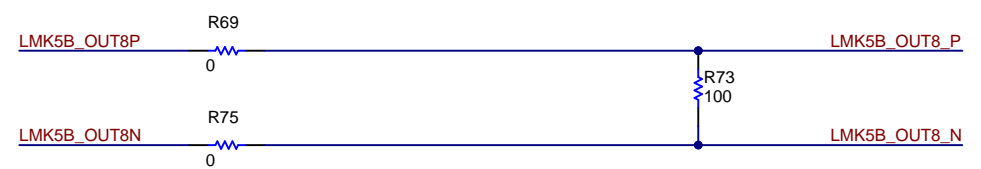
25MHz LVDS
To CPU



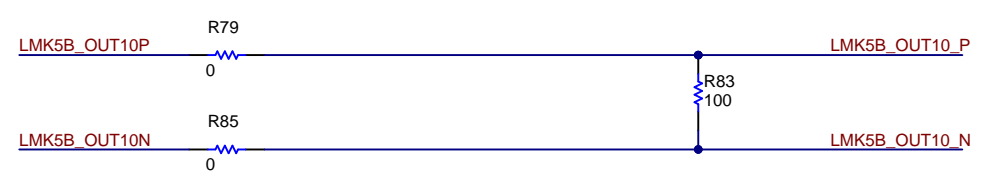
312.5MHz HSDS
To 112G/224G PAM4 SerDes



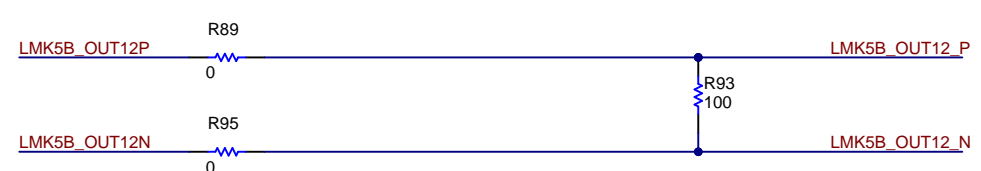
312.5MHz HSDS
To 112G/224G PAM4 SerDes



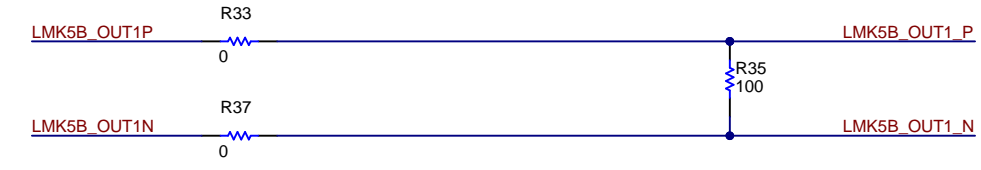
156.25MHz LVDS
To 112G/224G PAM4 SerDes



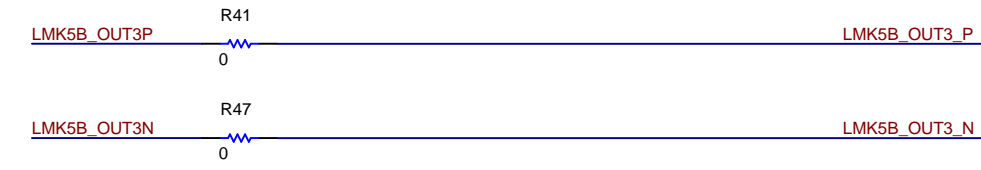
156.25MHz HSDS
To 112G/224G PAM4 SerDes



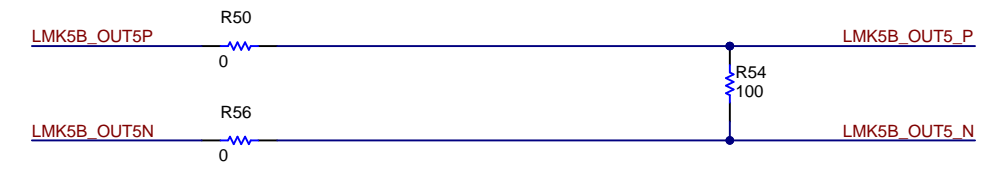
156.25MHz HSDS
To 112G/224G PAM4 SerDes



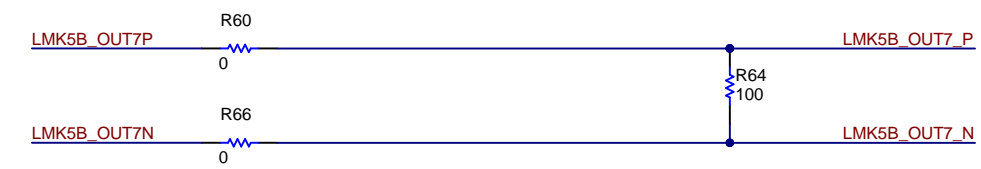
50MHz HSDS
To 112G/224G PAM4 SerDes



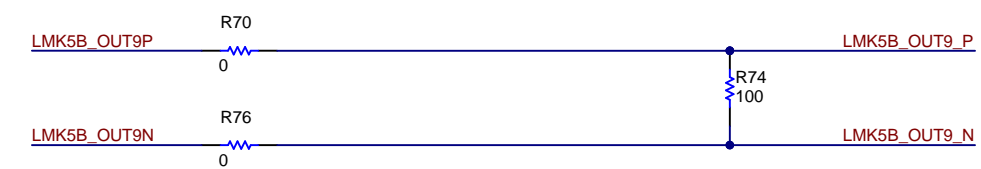
25MHz LVDS
To LMK1D IN0



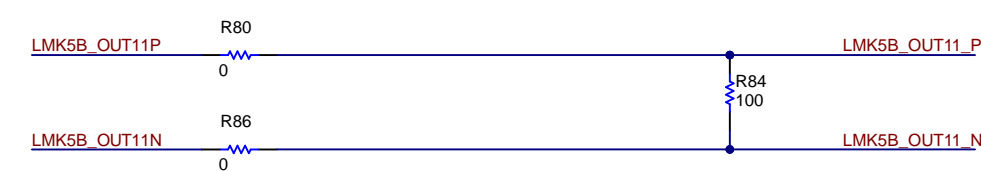
312.5MHz HSDS
To 112G/224G PAM4 SerDes



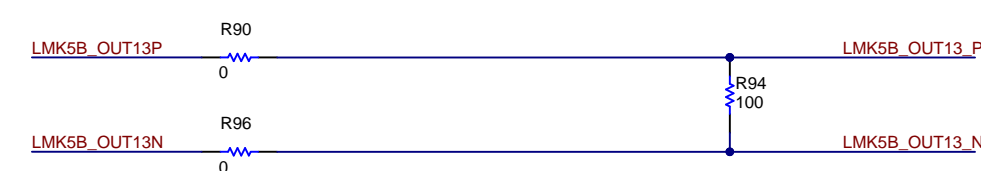
312.5MHz HSDS
To 112G/224G PAM4 SerDes



156.25MHz HSDS
To 112G/224G PAM4 SerDes



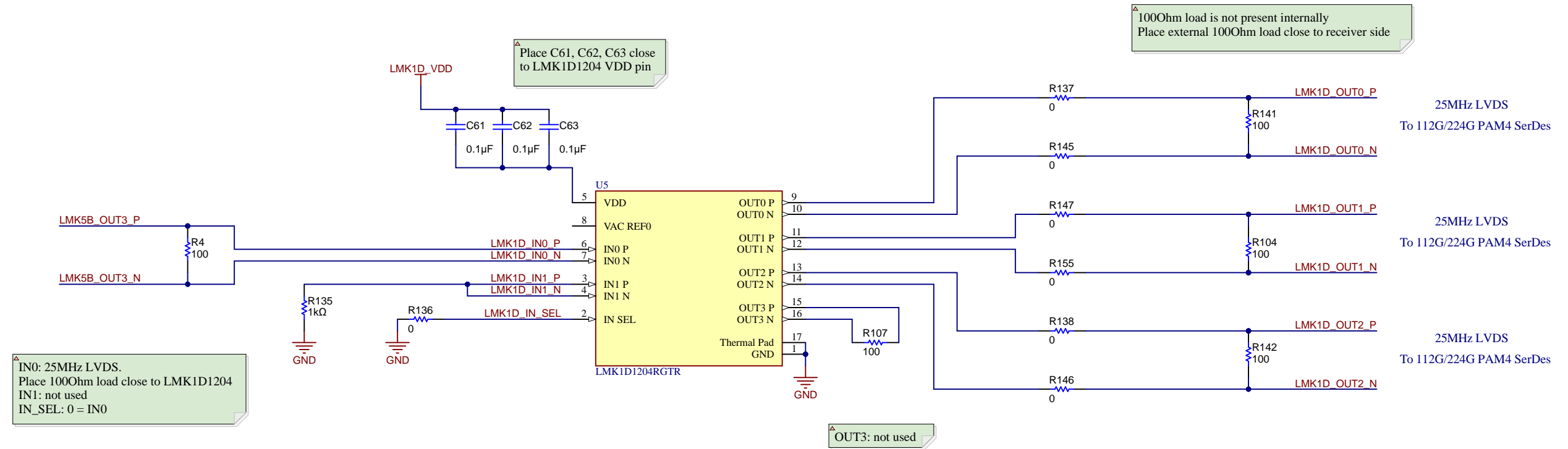
156.25MHz HSDS
To 112G/224G PAM4 SerDes



156.25MHz HSDS
To 112G/224G PAM4 SerDes

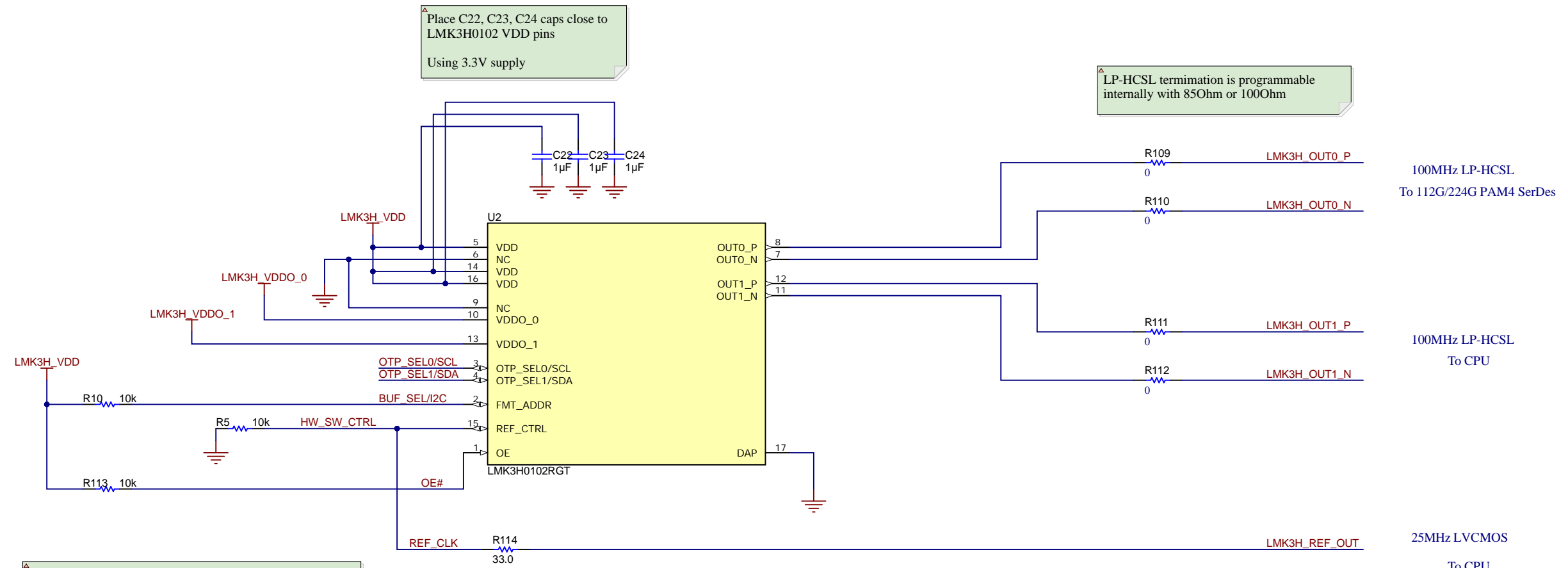
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Orderable: Multi EVMs	Designed for: Public Release	Mod. Date: 9/23/2024	TEXAS INSTRUMENTS
TID #: N/A	Project Title: Tomahawk 5 Network Switch Reference Design	Sheet Title: LMK5B33414 Outputs	
Number: N/A	Rev: A	Assembly Variant: 001	Sheet: 5 of 7
Drawn By: Riley Nguyen	File: LMK5B_Outputs.SchDoc	Size: B	http://www.ti.com
Engineer: Riley Nguyen	Contact: https://e2e.ti.com/		© Texas Instruments 2024



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TID #: N/A	Project Title: Tomahawk 5 Network Switch Reference Design	Sheet Title: LMK1D1204	
Number: N/A	Rev: A	Assembly Variant: 001	Sheet: 6 of 7
SVN Rev: Not in version control	File: LMK1D.SchDoc	Contact: https://e2e.ti.com/	Size: B
Drawn By: Riley Nguyen	Engineer: Riley Nguyen		http://www.ti.com
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Place C22, C23, C24 caps close to LMK3H0102 VDD pins
Using 3.3V supply

LP-HCSL termination is programmable internally with 850Ohm or 1000Ohm

For I2C:
 1. REF_CTRL: 10kOhm pull-up*
 2. FMT_ADDR: I2C address
 - 3.9kOhm pull-down: 0x68
 - 10kOhm pull-up: 0x69*
 - Tied to SDA: 0x6A
 - Tied to SCL: 0x6B
 3. OTP_SEL0/SCL and OTP_SEL1/SDA: I2C SCL and SDA

For OTP (one time programming):
 1. REF_CTRL: 10kOhm pull-down
 2. FMT_ADDR: ignored by default or can be used to control output format by overriding OUT_FMT_SRC_SEL = 1
 3. OTP_SEL0/SCL and OTP_SEL1/SDA: use for OTP page selection

OE:
 1. 10kOhm pull-up: enable all outputs*
 2. 3.9kOhm pull-down: disable all outputs

After POR: REF_CLK is used as CMOS output*

*Current selection for schematic

Place R114 close to REF_CTRL pin for LVCMOS termination

100MHz LP-HCSL
To 112G/224G PAM4 SerDes

100MHz LP-HCSL
To CPU

25MHz LVCMOS
To CPU

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