EVM User's Guide: LMKDB1108EVM

LMKDB1108 Evaluation Module

Description

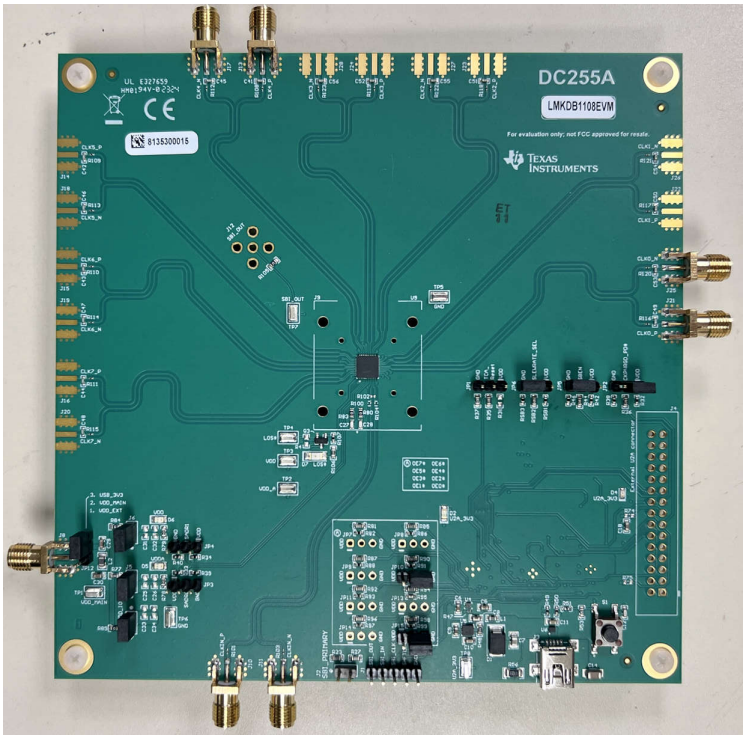
The LMKDB1108 Evaluation Module (EVM) is designed to provide a quick setup to evaluate the LMKDB1108 LP-HCSL buffer that supports PCIe Gen 1 to Gen 6 and is DB2000QL compliant. The printed circuit board (PCB) contains several jumpers and a USB connection to enable the LMKDB1108 with desired user programming and setup. The evaluation module provides flexibility for compliance testing, system prototyping and performance evaluation of the LMKDB1108 device.

Features

- PCIe Gen 1 to Gen 6 and DB2000QL compliant buffer
- External and USB power supply options
- Programmability through TICS Pro Software GUI graphical user interface (GUI)
- On-board input / output expander for output enable / disable through pin controls

Applications

- High performance computing
- Server motherboard
- NIC/SmartNIC
- Hardware accelerator



LMKDB1108 EVM Default Settings

1 Evaluation Module Overview

1.1 Introduction

The EVM can be configured through an on-board USB microcontroller (MCU) interface using a PC with TI's TICS Pro Software GUI. TICSPro can also be used to import and export register data for flexible programming of device. Input and outputs of LMKDB1108 can be interfaced with external system for evaluating compatibility and performance through coaxial cable. On-board LDOs give user an option to use the USB as power supply to minimize the number of test equipment needed. Side Band Interface (SBI) header pins can be used to daisy chain or control the outputs of LMKDB1108 for fast switching.

1.2 Kit Contents

LMKDB1108EVM box contains:

- One LMKDB1108EVM board (DC255A).
- 3-ft mini-USB cable (MPN 3021003-03).

1.3 Specification

Some key specifications for LMKDB1108 buffer and EVM are noted in Table 1-1.

Table 1-1. LMKDB1108 Key Parameters

Parameter	Value
Ambient Temperature	-40 to 105 ºC
Power Supply	1.8 V ± 10%, 3.3 V ± 10%
Operating Frequency	1 MHz to 400 MHz. ("automatic output disable" (AOD) disabled)
	25 MHz to 400 MHz. ("automatic output disable" (AOD) enabled)
Output Format	LP-HCSL

1.4 Device Information

The LMKDB1108 is a high performance LP-HCSL buffer that supports PCIe Gen 1 to Gen 6 and is DB2000QL compliant. LMKDB1108 has extremely low additive jitter, fail safe inputs, flexible power-up sequence, individual output enable pins, loss of input signal detection, and 3-wire or 4-wire SBI and SMBUs interface. The EVM has integrated LDOs for excellent power supply noise suppression with operating supply voltage of 3.3-V.

2 Hardware

2.1 EVM Quick Start

Table 2-1 describes the default jumper configuration of the EVM to power the device from an on-board 3.3-V LDO with USB supply option. Configure the EVM as specified in Table 2-1 for initial bring up. The EVM can also be configured to use an external power supply by changing the position of jumper JP12 as described in Table 2-1.

Table 2-1. Default Jumper Configuration

Category	Reference Designator	Default Position	Description
Power	J5	1-2	Connect USB or external supply to VDDA of device.
	J6	1-2	Connect USB or external supply to output bank and digital supply of the chip (VDD).
	J7	1-2	Connect USB or external supply to IO pins on board (VDD_IO).
	JP12	2-3	Choose between USB power supply and external. Current configuration is for USB option. To change to external supply, change jumper position to 1-2.
Output enable control pins	JP10, JP15	2-3	Pull down to GND to enable output (OE#0, OE#4) with pin control option.
	JP7, JP8, JP9, JP11, J13, JP14	-	Not populated on the EVM. If additional outputs are needed, these jumpers need to be soldered onto the EVM as well as their respective output edge SMA headers.
SMBus address control pins	JP3, JP4	-	Refer to Table 2-8 for selecting SMBus address.
Digital pins	JP1, JP2	1-2	TCA Reset and CLKPWRGD_PD# pulled high.
	JP5	1-3	SBEN pin = GND.
	J2	-	SN74LVC125 buffer enable control pin. Default pull down to GND.
	JP6	2-3	Slew Rate SEL Pin pulled Low by default.

2.1.1 Hardware Setup

Figure 1-1 shows default jumper configuration for the EVM. Make sure to adjust the jumpers as shown for initial boot-up using USB power supply option.

To begin using the LMKDB1108EVM, follow the steps below.

1. Verify the EVM default jumper as described in Table 2-1 and Figure 1-1.
2. Connect the USB cable to USB port at J3.
3. Connect 100 MHz reference clock to CLKIN_P/N. Refer to Table 2-9 for different input reference configurations.

2.1.2 EVM Measurements

Measurements can now be made on the clock outputs using an oscilloscope or a phase noise analyzer.

2.2 Device Operation Modes

The LMKDB1108 can be configured to start up in one of two modes during power-on/reset (POR). SBEN enable pin determines the mode of operation during power supply ramp up. Below are both the modes for the device:

1. **SMBus Mode Only** (EVM default): When SBEN pin is set to low during the power up. SBI interface is disabled, output enable (OE) control is only accessible through the SMBus and OE control pins.
2. **SBI Mode**: When SBEN pin is set to high during power up, SBI interface is enabled and the outputs can be controlled through SBI interface, as well as SMBus and OE control pins.

2.3 EVM Configuration

The LMKDB1108EVM can be configured for multiple modes using on board MCU and external power supply options. The following sections describes power, logic, clock input and output interfaces on the EVM and how to configure the EVM accordingly.

Some of the key components and their reference designator are noted in Table 2-2.

Table 2-2. Key Components Reference Designator and Descriptions

Item No.	Reference Designators	Description
1	U9	LMKDB1108.
2A	J8	External VDD option through SMA Port.
2B	JP12	Jumper header to select between external or on-board 3.3-V USB supply option.
3	J10, J11	SMA Ports for Clock Input (CLKIN_P, CLKIN_N).
4	J13 through J28	SMA Ports for Clock Outputs (CLKXX_P, CLKXX_N).
5	JP3, JP4	SADR0_tri and SADR1_tri jumper header option to select different address as defined in Table 2-8.
6	JP5	SBEN pin header jumper to enable or disable SBI interface during power-up.
7	JP1	TCA_RESET pin header jumper for Input / Output (IO) Expander needs to be pulled-up for proper operation. Default configuration is set to pull-up (header connected to 1-2).
8	JP2	CLKPWRGD_PD# pin header jumper to enable or disable the LMKDB1108.
9	JP6	SLEWRATE_SEL pin header jumper to select fast or slow slew rate option.
10A	J1	SBI Connector header jumper for daisy chain option.
10B	J2	SBI_PRIMARY header jumper option to disable the U3A, U3B, U3C, U3D buffer part of the EVM.
11	U4	USB power option LDO.
12	U1A, U1B, U1C, U1D	Hi-Z buffer part used on SBI lines for daisy chain configuration.
13	U3	MUX part to choose between MCU and IO expander option on OE#0, OE#1, and OE#4 pins.
14	U2	IO Expander used for all OE# pin controls.
15	U8	MSP430F5529IPN MCU.

2.3.1 Power Supply

The LMKDB1108 has VDDA and VDD supply pins that operate from 1.8-V ± 10% and 3.3-V ± 10%.

For 3.3-V supply option, EVM has an on-board LDO which is selected by default to reduce the need for external power supply and operate the EVM using USB cable with a PC.

To use 1.8-V ± 10% supply on the EVM, J8 can be used to force external supply voltage. The EVM has two different method of supplying power to the device as listed in Table 2-3.

Table 2-3. EVM Power Modes

EVM Power Mode	Designator	Position	Supply Voltage	Description
External	J8	External Supply	1.8-V ± 10% or 3.3-V ± 10%	External supply option is selected.
	JP12	1-2		
USB	J8	Not Connected	3.3-V ± 10%	USB 3.3-V supply option is selected.
	JP12	2-3		

2.3.2 Logic Input and Outputs

The logic input and output pins on LMKDB1108 provides option for selecting different device modes, output enable / disable control, loss of signal (LOS) detection, and different device address selection. The following section describes the function of different input and output logic pins. Voltage levels for input pins can be set through TICSPro GUI or using on-board jumper as specified in Table 2-2.

Table 2-4. Device Start-Up Modes

SBEN_EN Input Level	Start-up Mode
Low	SBI disabled
High	SBI enabled

Table 2-5. Output Enable Pin Control

OE0# to OE7# INPUT LEVEL	OUTPUT STATUS
Low	Enabled
High	Disabled

Table 2-6. Loss of Signal Detection (LOS)

LOSb OUTPUT LEVEL (Status pin)	LOS STATUS
Low	Detected
High	Not detected

Table 2-7. SLEWRATE_SEL

SLEWRATE_SEL	OUTPUT SLEW RATE
Low	Slow
High	Fast

Table 2-8. SMBus Address Decode

Address Selection		Binary Value								Hex Value	
SADR1_tri	SADR0_tri	7	6	5	4	3	2	1	Rd/Wrt	Without Rd/Wrt	With Rd/Wrt
0	0	1	1	0	1	1	0	0	0	6C	D8
	M	1	1	0	1	1	0	1	0	6D	DA
	1	1	1	0	1	1	1	1	0	6F	DE
M	0	1	1	0	0	0	0	1	0	61	C2
	M	1	1	0	0	0	1	0	0	62	C4
	1	1	1	0	0	0	1	1	0	63	C6
1	0	1	1	0	0	1	0	1	0	65	CA
	M	1	1	0	0	1	1	0	0	66	CC
	1	1	1	0	0	1	1	1	0	67	CE

Note

SMBus address for the device is Bits[7:1]. Often Rd/Wrt bit is included in the hex value depending on the different vendors. *With **Rd/Wrt*** column shows hex value when Rd/Wrt value is considered 0, while *Without **Rd/Wrt*** is the SMBus address.

2.3.3 Clock Input

LMKDB1108 can support different input interfaces depending on the input swing and common mode voltage. There are four input interfaces type that can be configured on LMKDB1108 using external components and internal termination schemes as shown in Figure 2-1. If using signal generator, then make sure to populate *R34* with a *100*-Ω resistor or use internal / external 50-Ω termination to ground.

1. DC Coupled HCSL / LP HCSL Input.
2. DC Coupled LVDS Input.
3. External AC Coupled Input.
4. Internal 50-Ω to ground terminations.

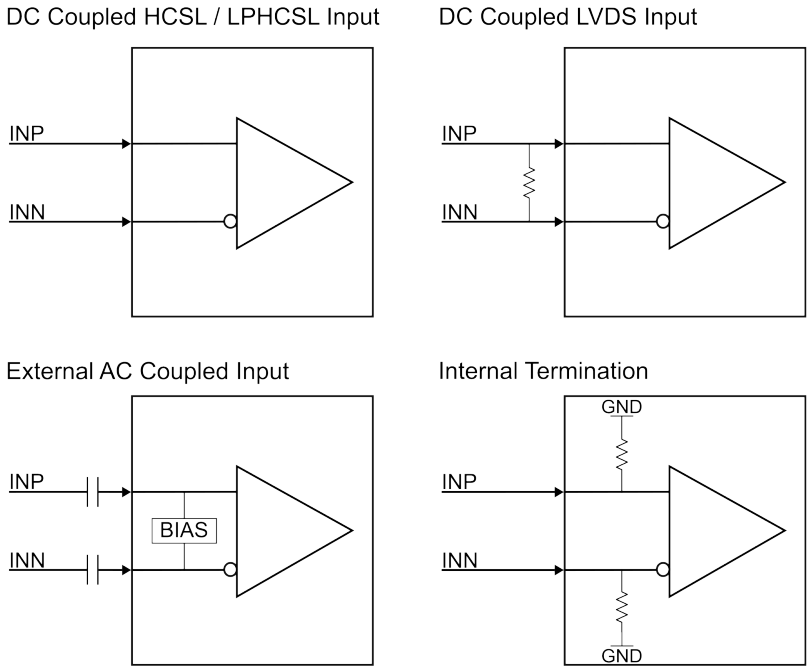


Figure 2-1. Input Interfaces

Table 2-9 outlines how to setup all different interfaces supported by LMKDB1108.

Table 2-9. Input Interfaces

Input Interface	Configuration
DC coupled HCSL / LPHCSL	This is default EVM and device configuration. *R101* and *R103* values are ***0-Ω*** and *Input Interface Type* on *Input* page is selected to *DC Coupled*.
DC coupled LVDS input	Populate *R102* with a ***100-Ω*** resistor and set *Input Interface Type* on *Input* page to *DC Coupled*.
External AC coupled input	Replace *R101* and *R103* with ***0.1 uF*** capacitor and set *Input Interface Type* on *Input* page to *AC Coupled*.
Internal termination	To enable internal 50-Ω to ground terminations. Set the *Input Termination* on *Input* page to *Enabled*.

2.3.4 Clock Outputs

LMKDB1108 has eight differential clock outputs (CLK[0:7]_P/N).

All the outputs are DC coupled with a capacitive load of 2-pF. CLK0_P/N and CLK4_P/N have SMA ports populated on the EVM for measurements. To evaluate all other outputs, SMA ports need to be soldered to connect outputs to measurement instrument.

WARNING

DC-coupled clocks must not be directly connected to RF equipment which cannot accept DC voltages greater than 0-V, such as spectrum analyzers and phase noise analyzers.

2.3.5 Status Outputs, LEDs and Test Points

LMKDB1108EVM have status output signal from LMKDB1108, LEDs and testpoints to monitor signal / supply voltage on the board. Table 2-10 summarizes all the status signals / testpoints on the board.

Table 2-10. Status Output, LEDs and Test Points

Function / Test Signal	Status Pin / LED Designator	Description
LOSb	TP4	Test point to monitor LOSb status.
	D7	LED status light for LOSb detection.
SBI OUT	J12	SMA Port for SBI OUT pin.
	TP7	Additional test point for SBI OUT pin.
	J1	Jumper header for SBI OUT, SBI_IN, SBI_DATA, and SHFT_LD# pins to connect all signals needed for daisy chain in one place.
VDDA	D5	LED status light for VDDA supply pin.
	TP2	Test point for VDDA supply pins.
VDD	D6	LED status light for VDD supply pins.
	TP3	Test point for VDD supply pins.
VDD_MAIN	TP1	Test Point to measure the VDD supply selected from USB option or External option through JP17.
GND	TP5, TP6	Test points for GND reference on the board.
USB LED	D4	USB LED status light to verify USB2ANY communication to board.
U2A_3V3	D2	USB2ANY LDO supply status LED.
	TP8	Test point for USB2ANY LDO supply pin.

3 Software

3.1 Software Installation

3.1.1 Software Setup

1. If not already installed, then install TICS Pro software from TI website: TICS Pro Software GUI.
2. Start TICS Pro software.
3. Select the LMKDB1108 profile from *Select Device* → *Clock Distribution with Divider* → *LMKDB1108*.
4. Confirm communication with the board as follows:
   a. Click *USB Communication* from the menu bar.
   b. Click *Interface* to launch the *Communication Setup* pop-up window.
   c. Confirm following field the *Communication Setup* pop-up window:
      i. Make sure *USB2ANY* is selected as the interface.
      ii. In case of multiple USB2ANY, select desired interface. If a USB2ANY is currently in use in another TICS Pro, then the user must release that interface by changing the interface setting to *DemoMode*.
      iii. Click *Identify* to blink LED shown in Figure 3-1. After clicking the *Identify* button, the LED flashes quickly at about 0.5 second on, 0.5 second off for about 5 seconds. This confirms the connection to the board. However, be aware that USB2ANY devices connected to the PC, but not attached to a TICS Pro instance, can blink at a slow rate of 1 second on, 1 second off continuously.
   d. Confirm all the fields match the ones shown in Figure 3-2.

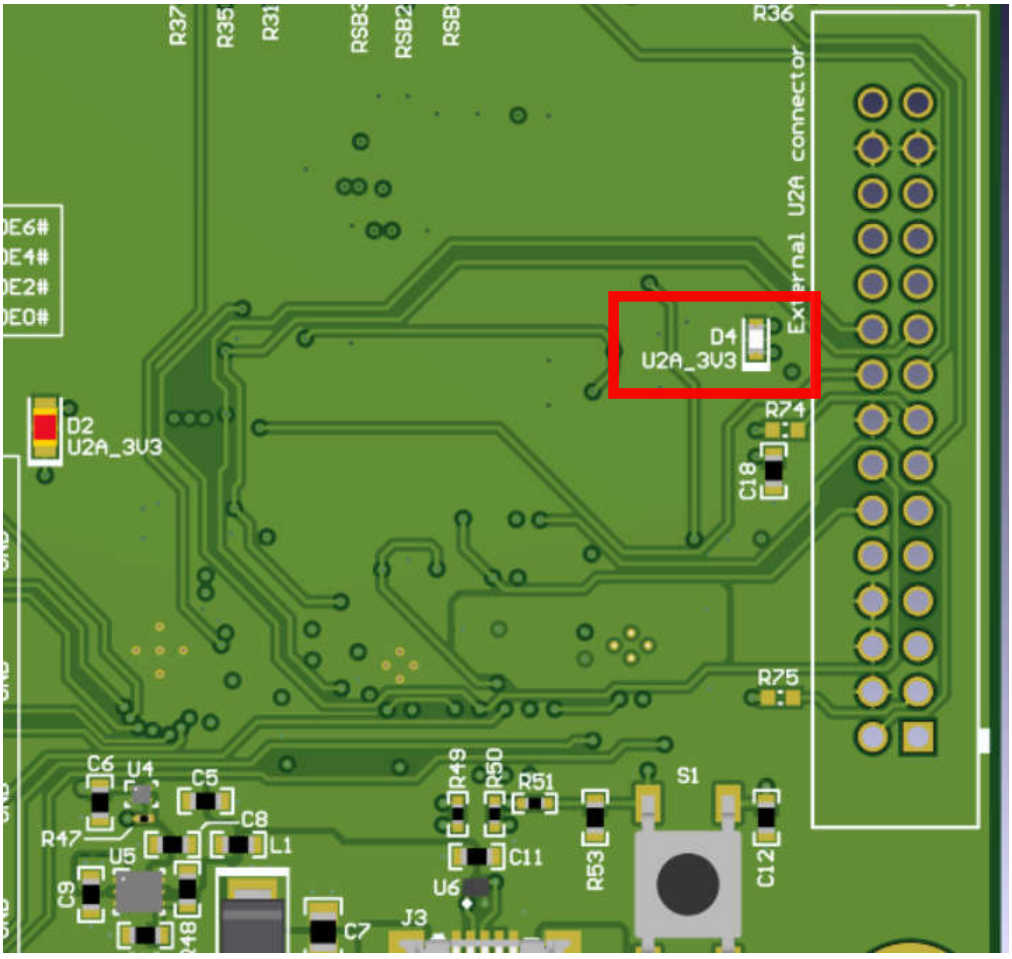


Figure 3-1. USB LED

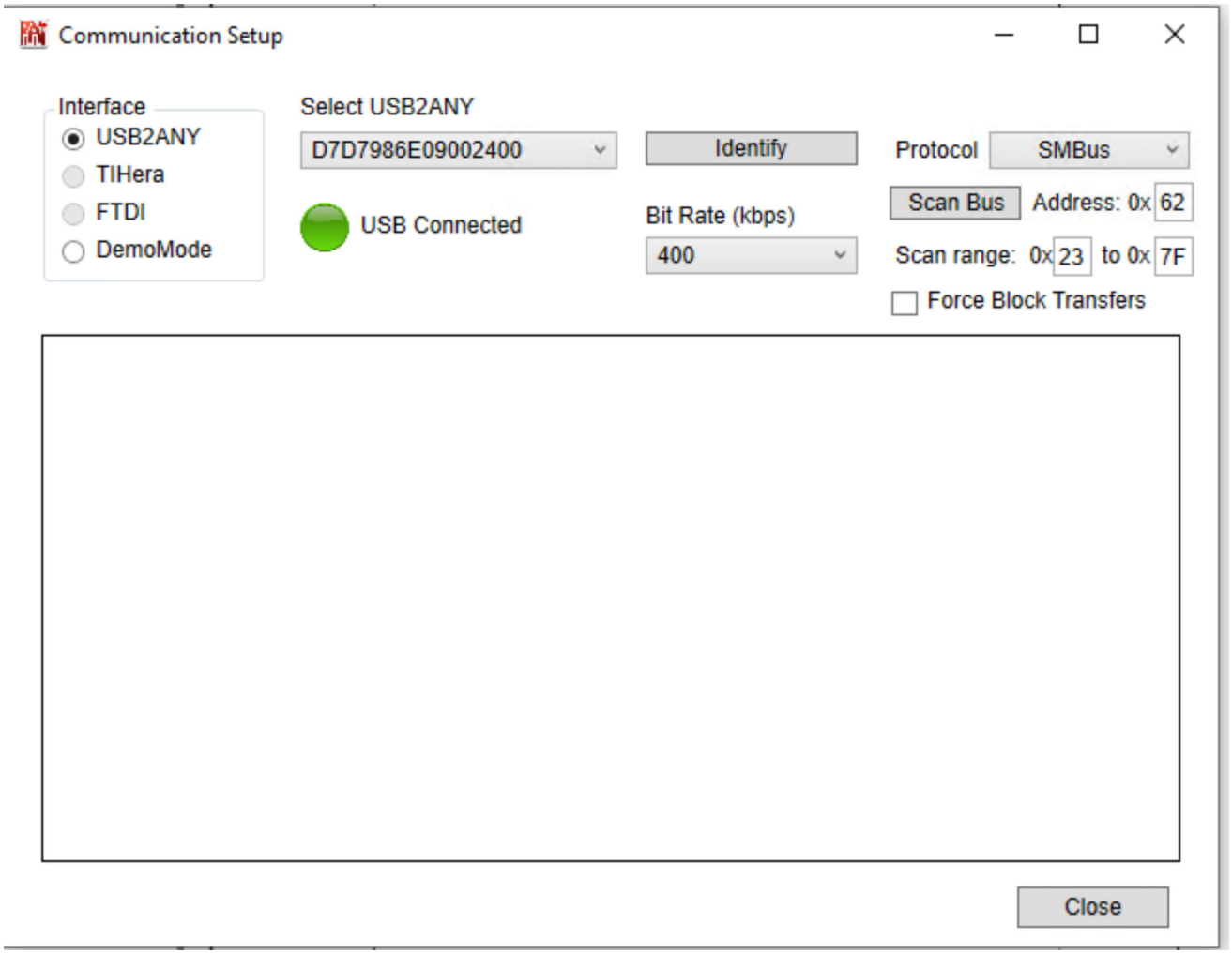


Figure 3-2. Communication Setup

3.1.2 Program and Setup

By default, the LMKDB1108 and the GUI are started with the default configuration. When using the on-board USB supply option, the following steps can be followed to avoid any improper power up sequence issue when plugging in the USB cable to the EVM.

1. After all the steps above, toggle the *USB 3V3 Supply* pin *Low* → *High* for power reset. This step is not necessary but recommended if there are any issues with readback or improper start up on EVM.
2. Click on *Scan Bus* in the *Communication Setup* window to find and update device address.
3. Click on *Read All Regs* to update the register readback from the device.

3.2 TICS Pro LMKDB1108 Software

LMKDB1108 TICS Pro GUI provides full functionality to interact with the device through SMBus, SBI, and OE pin option to interact with the device. TI recommends to use GUI interface while evaluating LMKDB1108EVM to fully utilize all the functionalities of the EVM. The GUI interface consists of *User Controls* and *Raw Register* page to write directly into each register bit or field values. The GUI interface also has *Input*, *Device Info*, and *Output* pages, which can be used to evaluate functions available on the device. The following sections describe the details of each page.

3.2.1 Input

Input page provides access to configure different input modes and read back live status for loss of signal (LOSb) as shown in Figure 3-3

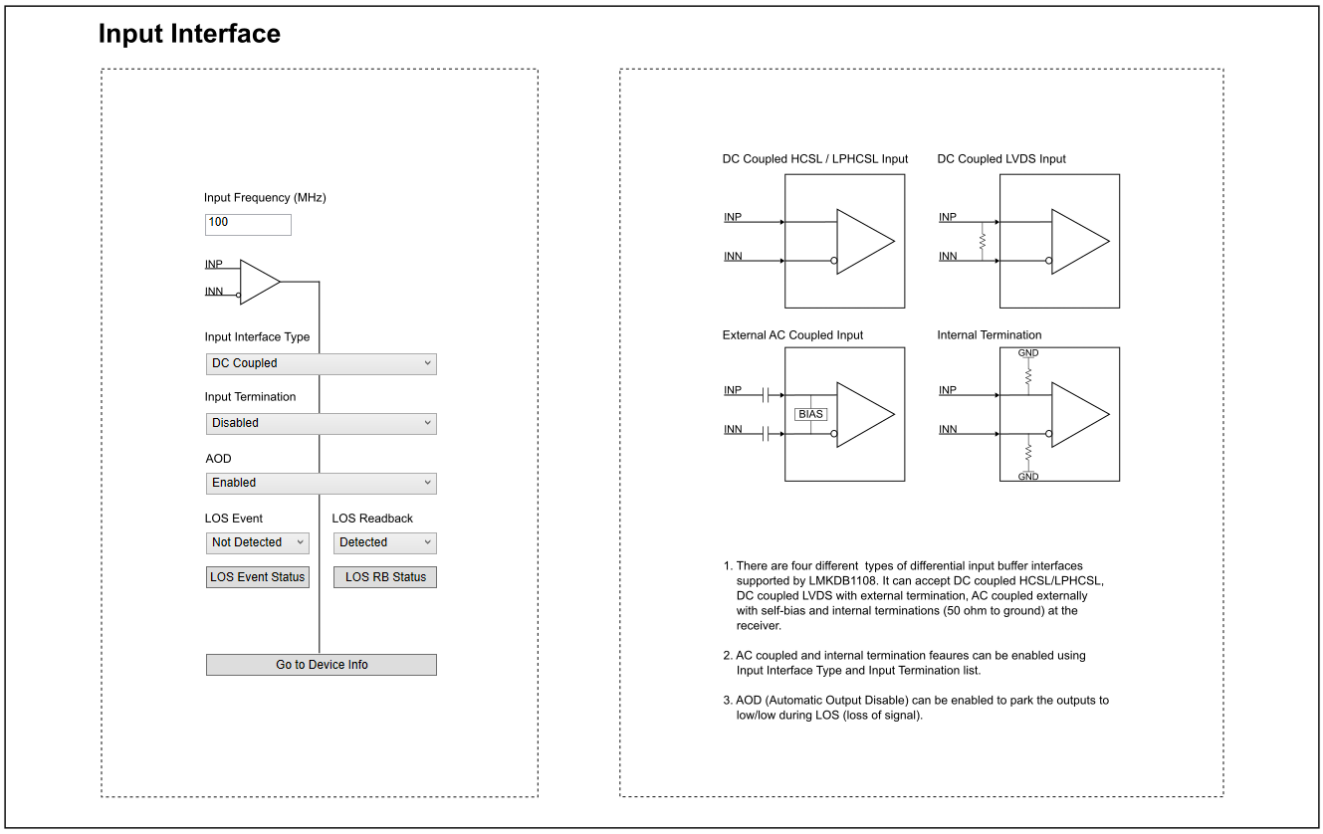


Figure 3-3. Input Interface

3.2.1.1 Input Interface Type

Input interface type can configured as AC Coupled or DC coupled. AC coupled option provides internal bias to the clock inputs connected.

3.2.1.2 Input Termination

Internal 50-Ω to ground terminations can be enabled or disabled using the *Input Termination* drop-down menu.

3.2.1.3 Auto Output Disable (AOD)

Automatic output disable (AOD) can be enabled or disabled using this control. AOD is enabled by default on LMKDB1108. AOD disables the outputs when low when there is a loss of signal (LOS) detected on the input. When AOD is disabled, outputs follow the input clock in DC state.

3.2.1.4 LOS Event

LOS Event Status gives information when there is loss of signal (LOS) event that occurs and can be cleared by writing 1.

3.2.1.5 LOS Readback

LOS Readback provide live status of loss of signal detection.

3.2.2 Device Info

Device Info page contains three different sections and the LMKDB1108EVM information.

This section contains following information related to device which can be read back using *Read Device Info* button.

1. Vendor ID
2. Device ID
3. Rev ID

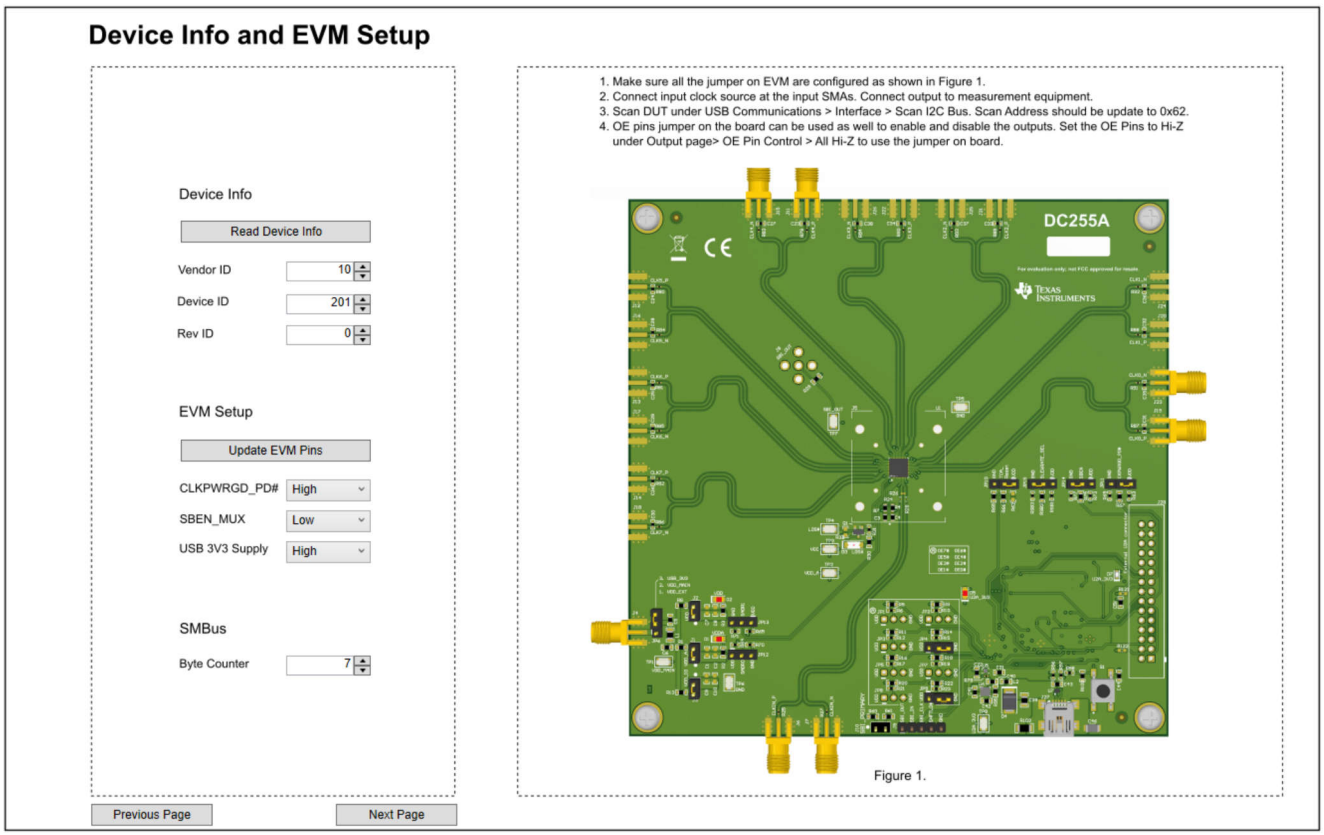


Figure 3-4. Device Info

3.2.2.1 EVM Setup

EVM setup has key pins to configure device. Below tables outlines usage of each pin option.

Table 3-1. CLKPWRGD_PD#

Pin Level	Function
Low	LMKDB1108 power down mode.
High	LMKDB1108 normal operation mode (default).
Hi-Z	When Hi-Z is selected, on-board header jumper can be used to force external voltages on the pin.

Table 3-2. SBEN_MUX

Pin Level	Function
Low	SBEN MUX (U3) configured to OE option for pin OE0#, OE1# and OE4# through IO expander (default).
High	SBEN MUX (U3) switches to USB2ANY MCU for SBI_IN, SBI_DATA, and SHFT_LD#. SBI becomes availabe after power reset in this setting on the device. Output page have *Enable SBI Control* button to configure all the setting automatically.
Hi-Z	When Hi-Z is selected, on-board header jumper can be used to force external voltages on the pin.

3.2.2.2 SMBus

Byte counter value determines the number of register readback during block read operation.

3.2.3 Output

The output page in TICS Pro has controls for clock outputs through SMBus, OE pins, and SBI.

3.2.3.1 SMBus

SMBus can be used to control the following parameters on the outputs:

1. Global Output Amplitude: To program output VOD from 600-mV to 975-mV with a step size of 25-mV.
2. SMBus Output Control: To enable or disable CLK0 through CLK7 via register bits.
3. Output Slew Rate Control: To program slow or fast setting for an output slew rate.
4. SBI Mask Register: To enable or disable SBI mask bits. When a mask bit is enabled, an output is controlled through SMBus and SBI control doesn't have any affect on the output. This is used when critical outputs needs to stay on.
5. OE# Pin Readback: To read status of OE# pins.

3.2.3.2 OE Pin Control

LMKDB1108EVM has on-board IO expander to provide output enable / disable controls for OE# pins. Low and High voltage level can be set on all the pins using GUI without the need of on-board headers. If on-board header are used, set all the OE# pins to Hi-Z using *All Hi-Z* button under the OE Pin Control on output page.

3.2.3.3 Side Band Interface (SBI)

Side band interface can be evaluated using controls available on the output page. There are two methods that can be used to enable SBI on the LMKDB1108.

1. Automated: When using on-board USB power supply option on the EVM, clicking once on the *Enable SBI Control* button configures the LMKDB1108 into SBI mode.
2. Manual: This method requires to set the *Set Pin SBEN* to *High* followed with a power cycle on the board. This is needed when using external supply option or when not using the *Enable SBI Control* button. SBI is enabled on LMKDB1108 after the restart.

After using any of the methods above, press *Read SBEN* to verify status of SBI mode on the device. Use check boxes for CLK0 through CLK7 to enable (checked) or disable (unchecked) the desired outputs. Once selected, click on *SBI Latch Enable* to load data into shift register.

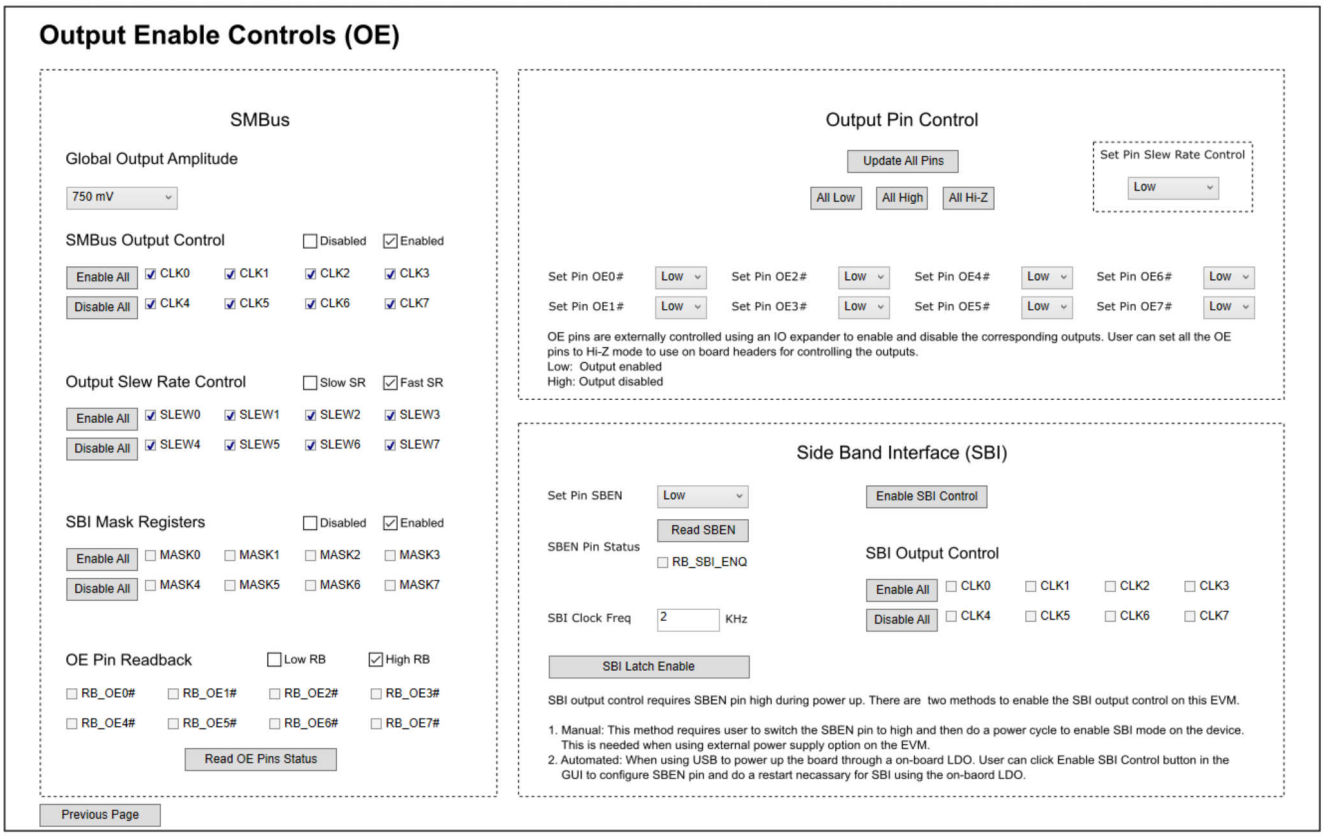


Figure 3-5. Output Enable Controls

4 Implementation Results

4.1 Typical Phase Noise Characteristic

Figure 4-1 shows a typical phase noise performance for 156.25 MHz reference clock input from the SMA100B.

LMKDB1108EVM was configured in cascade mode to get these measurements, which were obtained by following these steps:

1. SMA100B → LMKDB1108EVM input. Then, LMKDB1108EVM to secondary LMKDB1108 EVM. This was done to get good slew rate at the input. Other methods like clipping a circuit can be used to get a desired slew rate and square wave form as well outputted from the SMA100B.
2. Outputs phase noise is measured through a Balun to the differential waveform from the LMKDB1108 into a single-ended waveform for the phase noise analyzer.

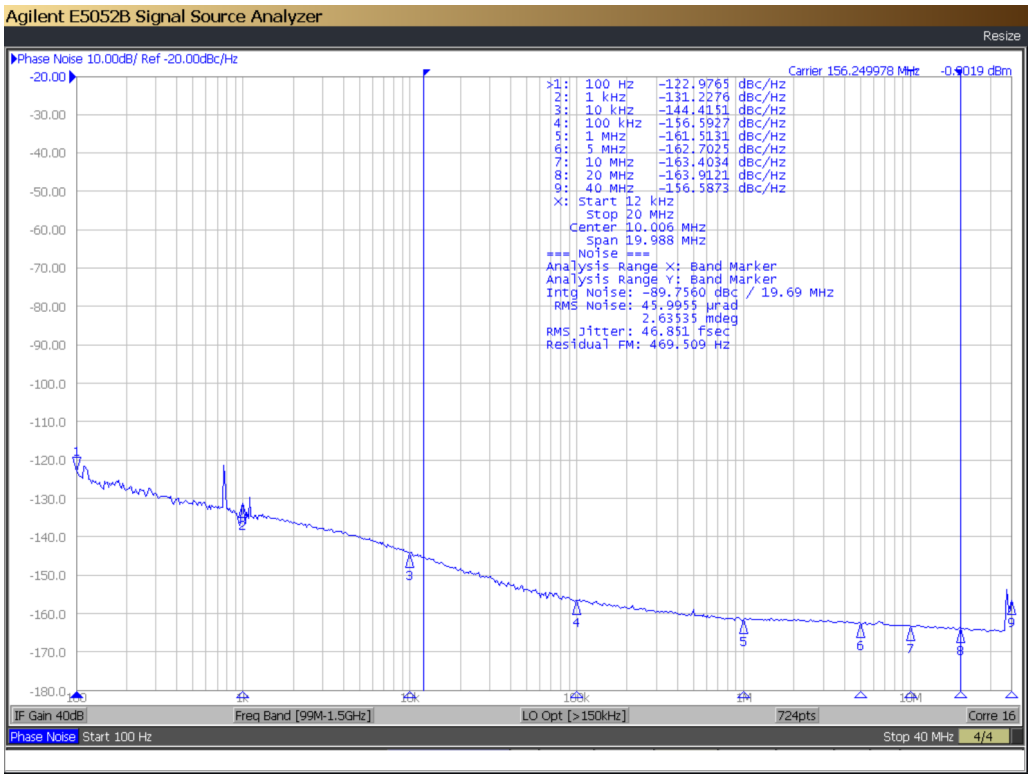


Figure 4-1. LMKDB1108 Output Clock Phase Noise

5 Hardware Design Files

5.1 Schematics

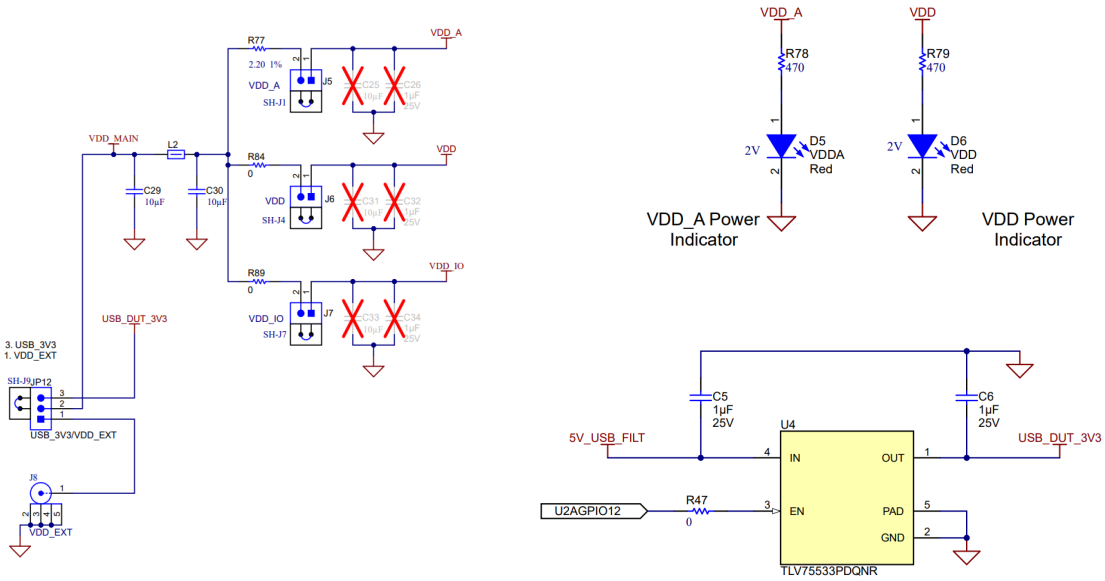


Figure 5-1. Power Supply (External and USB option)

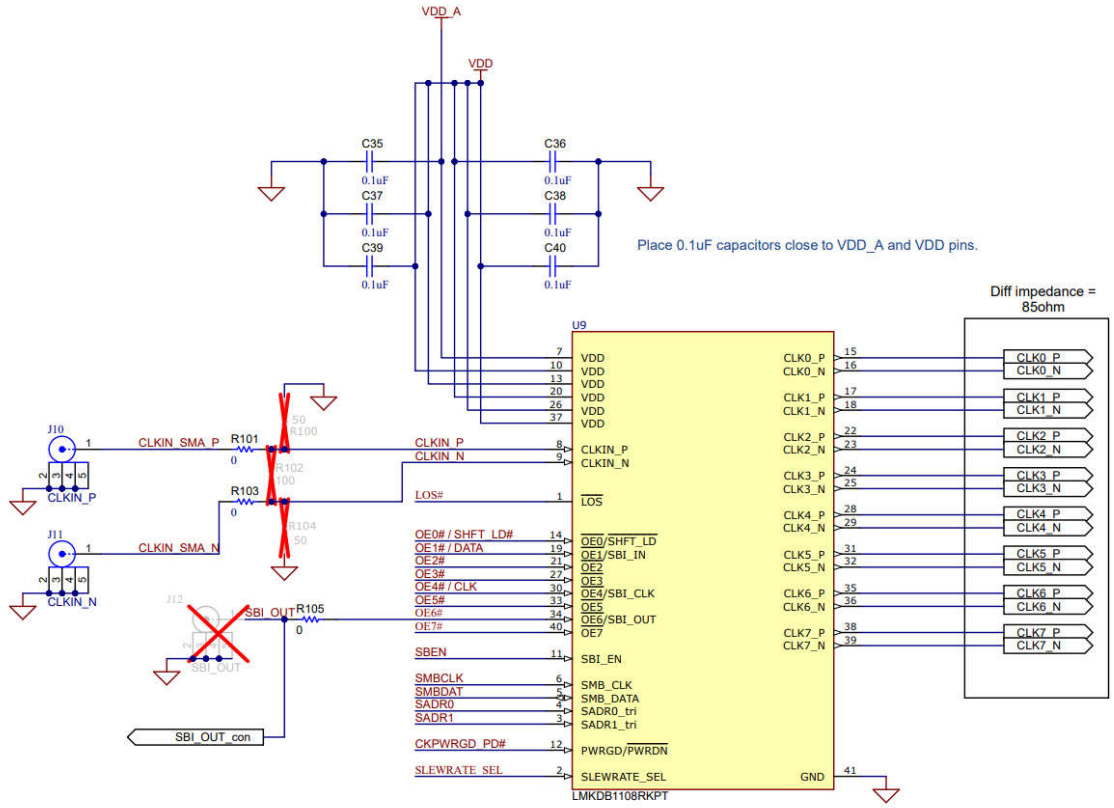


Figure 5-2. LMKDB1108 Device and CLKIN_P/N Reference

1. Differential impedance is 85 ohms.
2. Trace length should be matched with in +/- 2 MILS
3. Place load capacitor 2pF close to SMA connectors.

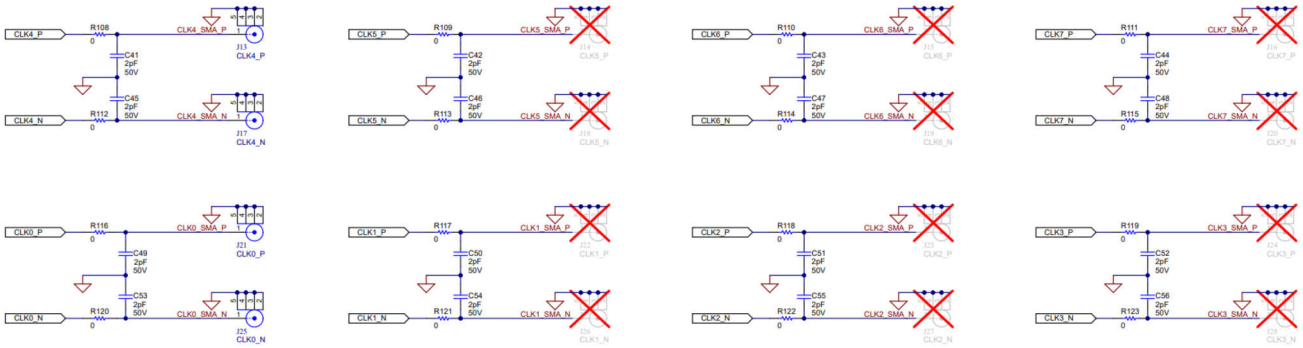


Figure 5-3. Clock Outputs CLK0 to CLK7

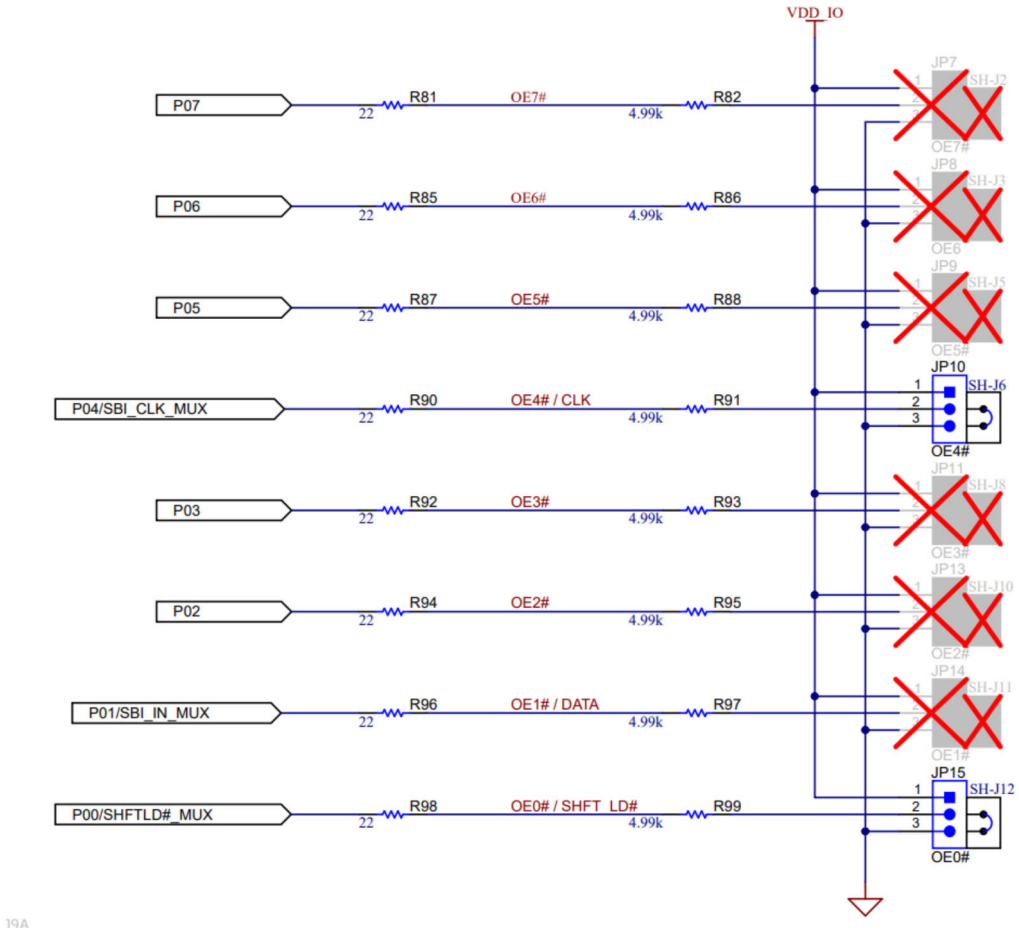


Figure 5-4. Output Enable Pins (OE#)

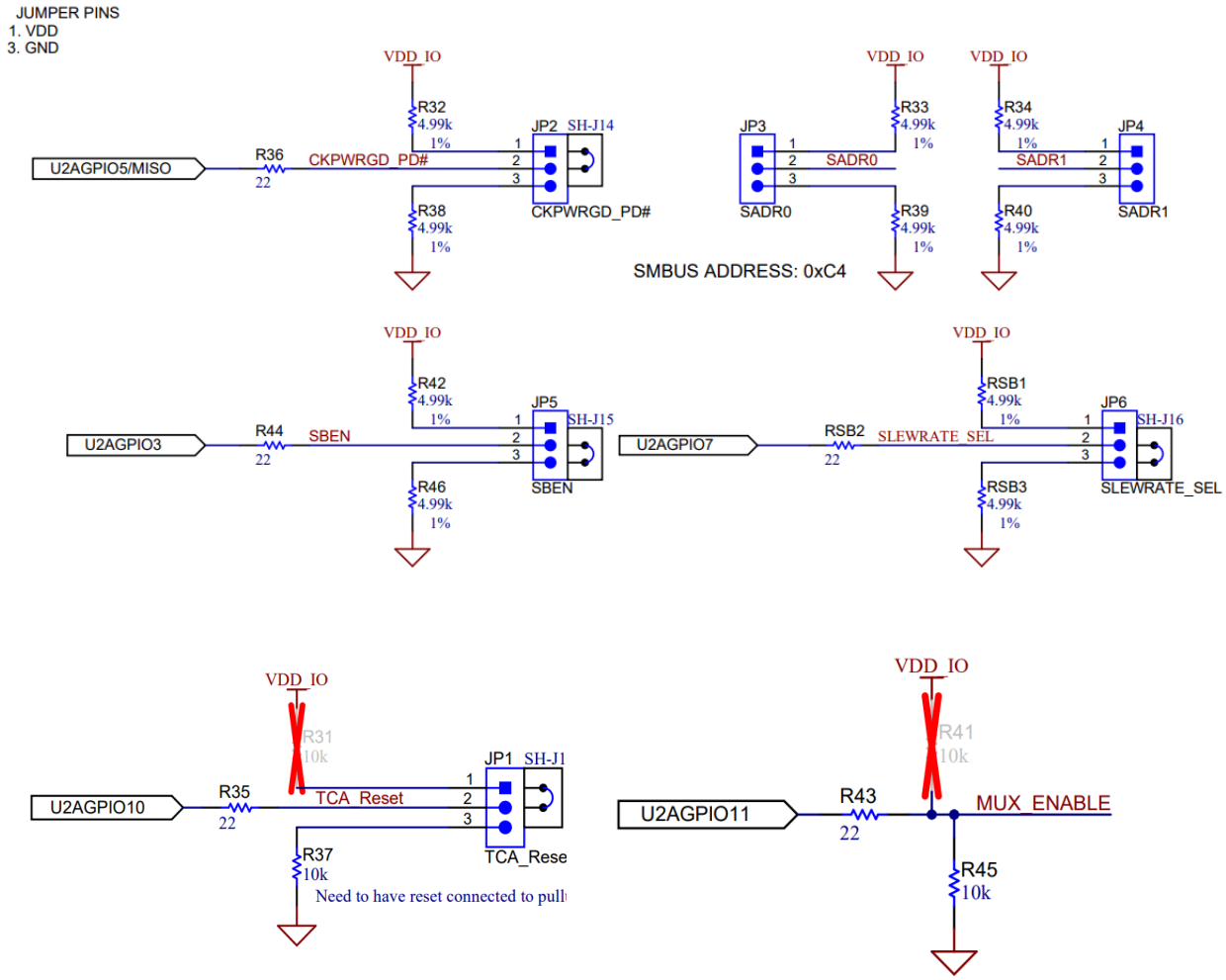


Figure 5-5. Logic I/O Jumpers

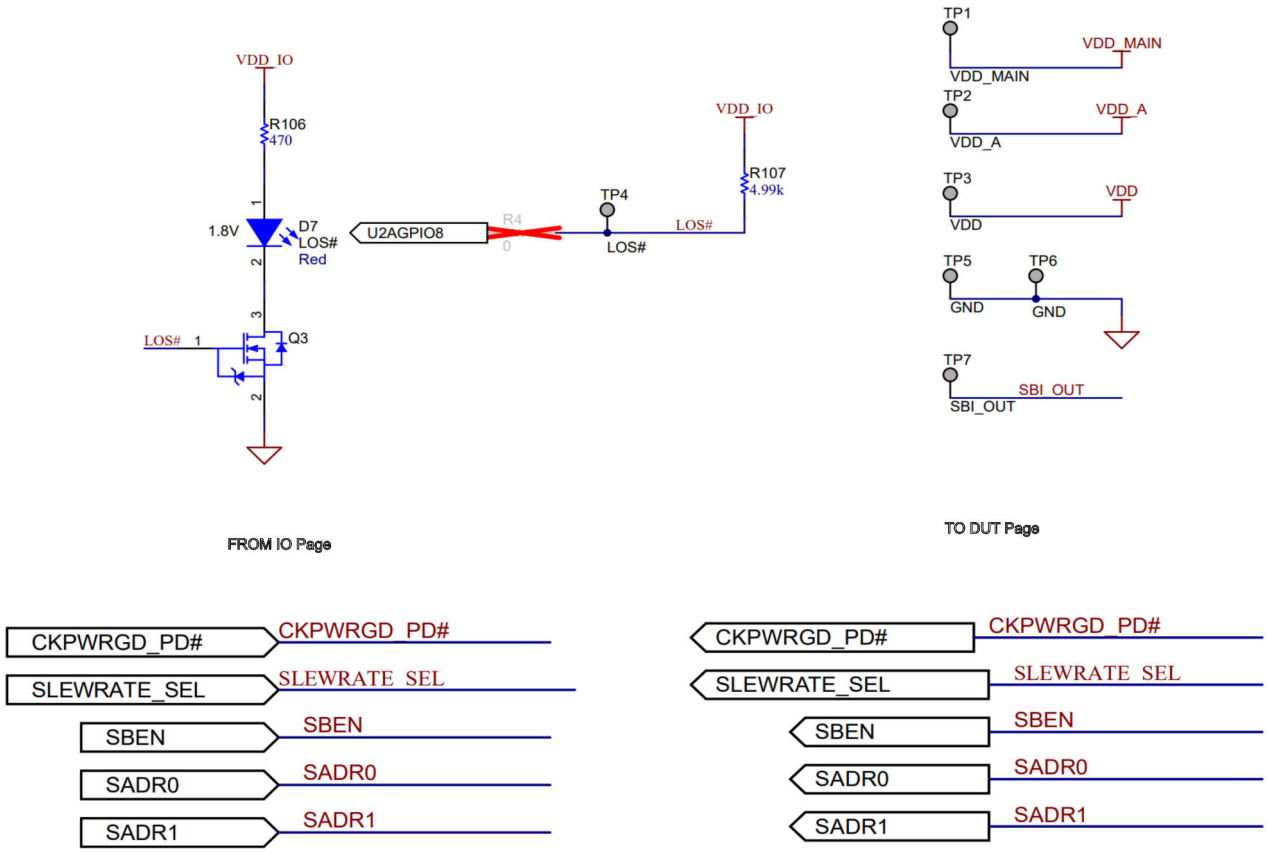


Figure 5-6. Status LEDs and Test Points

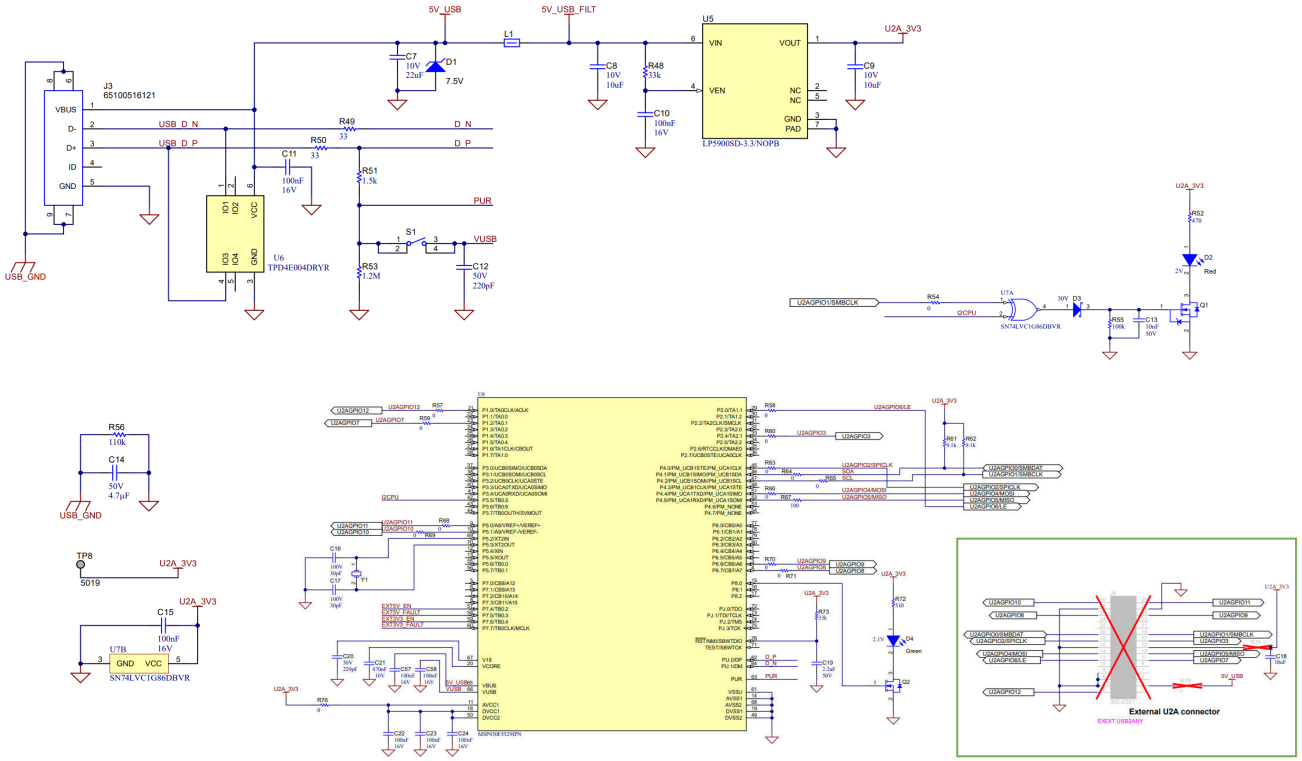


Figure 5-7. USB Schematic

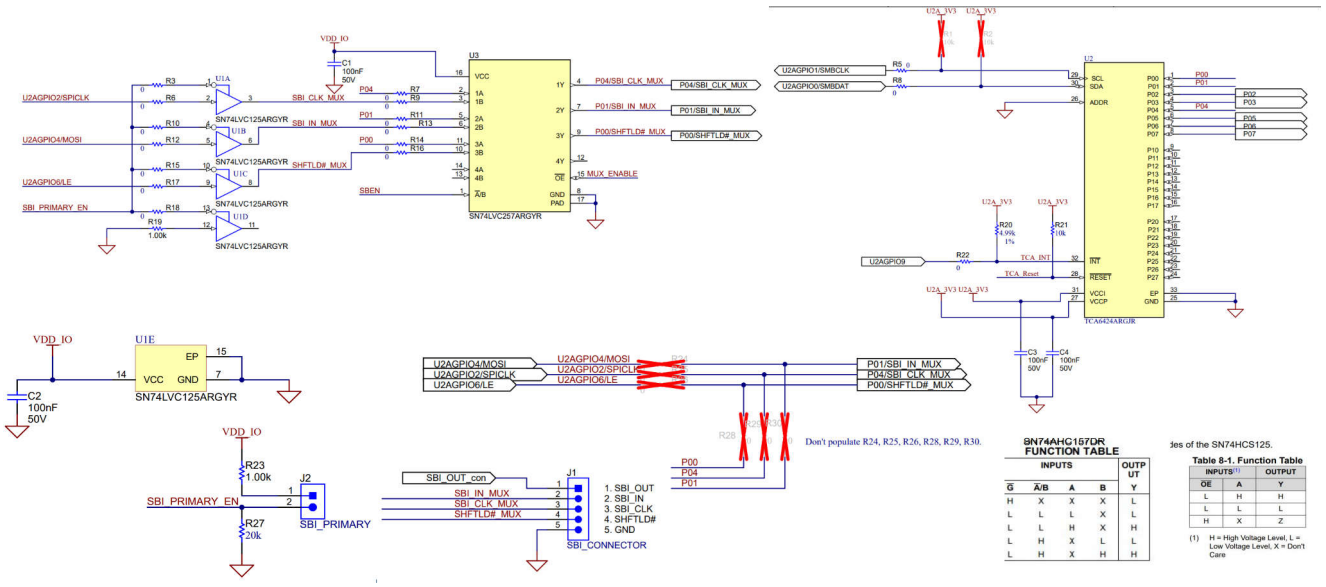


Figure 5-8. I/O Expander, MUX, and Buffer Used for SBI and OE Pin Control

5.2 PCB Layouts

Layer Stackup :

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.80mil	3.5	
1	Top Layer	Copper	2.10mil		
	Dielectric 1	FR-4 High Tg	6.00mil	4.2	
2	GND 1	Copper	1.40mil		
	Dielectric 2	FR-4 High Tg	10.00mil	4.2	
3	Signal-1	Copper	1.40mil		
	Dielectric 3	FR-4 High Tg	18.60mil	4.2	
4	PWR	Copper	1.40mil		
	Dielectric 4	FR-4 High Tg	10.00mil	4.2	
5	GND 2	Copper	1.40mil		
	Dielectric 5	FR-4 High Tg	6.00mil	4.2	
6	Bottom Layer	Copper	2.10mil		
	Bottom Solder	Solder Resist	0.80mil	3.5	
	Bottom Overlay				

Figure 5-9. Layer Stackup

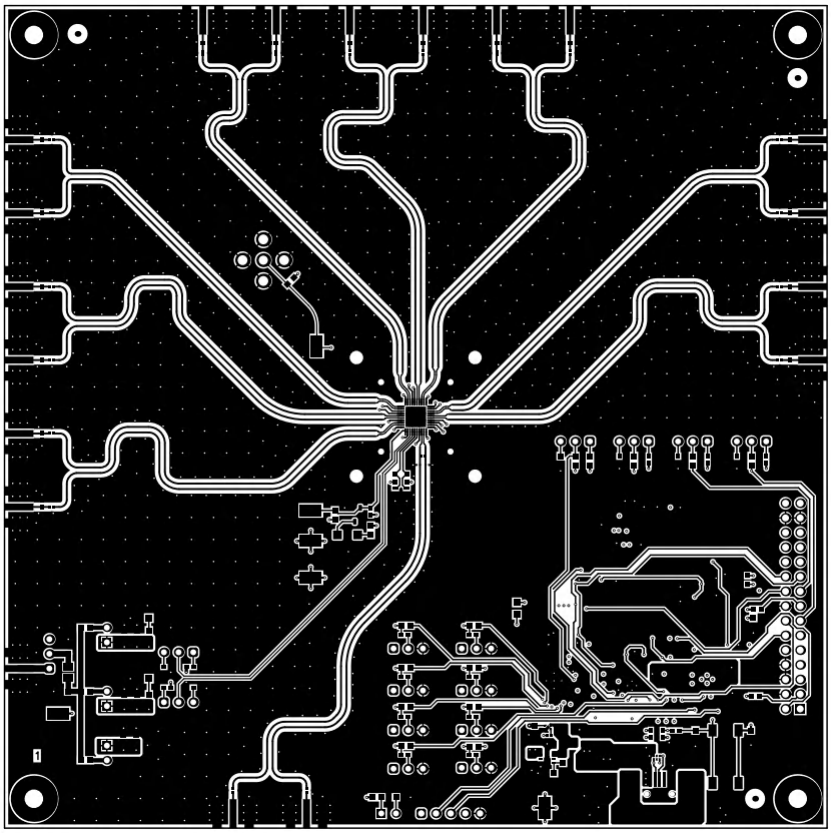


Figure 5-10. Top Layer (CLKIN / CLKOUT Signals)

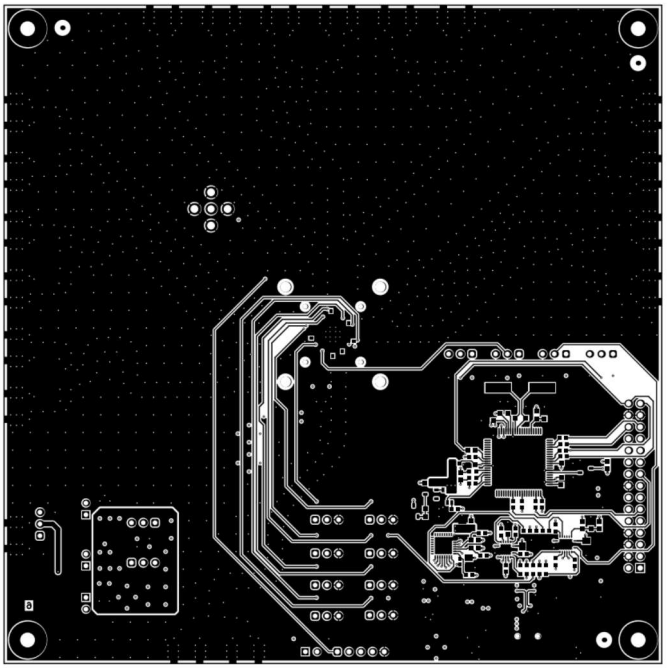


Figure 5-11. Bottom Layer

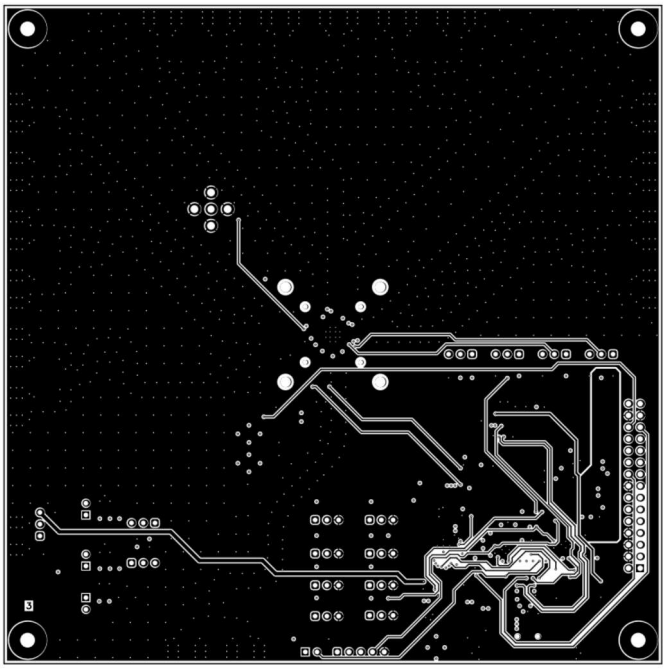


Figure 5-12. Signal 1 Layer

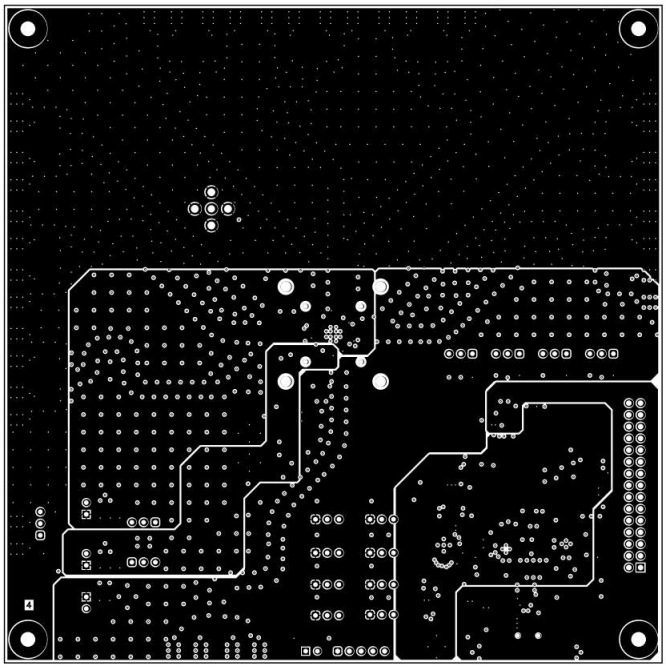


Figure 5-13. PWR Layer

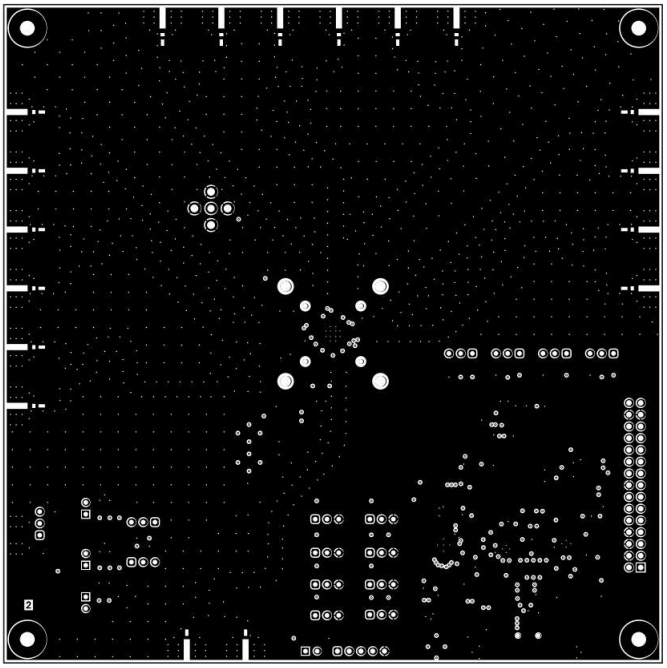


Figure 5-14. GND 1 Layer

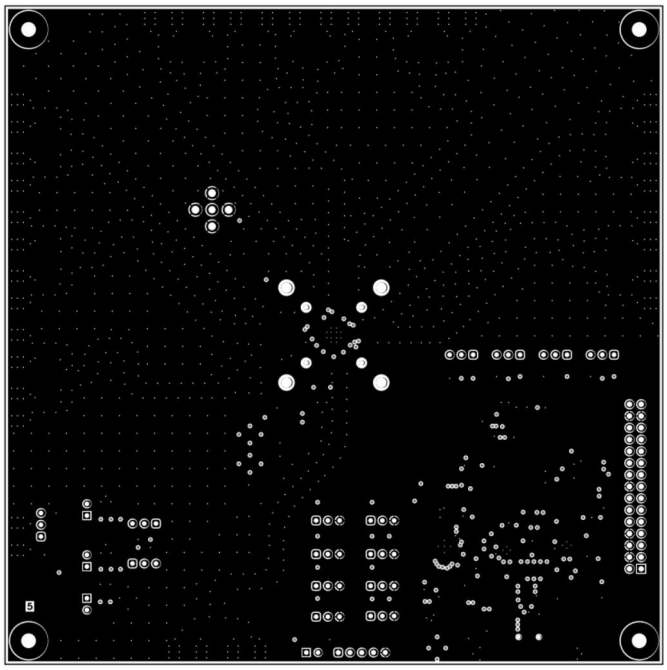


Figure 5-15. GND 2 Layer

5.3 Bill of Materials (BOM)

Table 5-1. Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		DC255	Any
C1, C2, C3, C4	4	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 20%, X7R, 0805	0805	08055C104MAT2A	AVX
C5, C6	2	1uF	CAP, CERM, 1 µF, 25 V,+/- 20%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E1X7R1E105M080AC	TDK
C7	1	22uF	CAP, CERM, 22 uF, 10 V, +/- 20%, X5R, 0805	0805	LMK212BJ226MG-T	Taiyo Yuden
C8, C9, C18	3	10uF	CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0603	0603	C1608X5R1A106M080AC	TDK
C10, C11, C15, C22, C23, C24, C57, C58	8	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 5%, X7R, 0603	0603	C0603C104J4RACTU	Kemet
C12, C20	2	220 pF	CAP, CERM, 220 pF, 50 V, +/- 1%, C0G/NP0, 0603	0603	06035A221FAT2A	AVX
C13	1	0.01uF	CAP, CERM, 0.01 uF, 50 V, +/- 5%, X7R, 0603	0603	C0603C103J5RACTU	Kemet
C14	1	4.7uF	CAP, CERM, 4.7 µF, 50 V,+/- 10%, X7R, 1206	1206	C3216X7R1H475K160AE	TDK
C16, C17	2	30 pF	CAP, CERM, 30 pF, 100 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C2A300JA01D	MuRata
C19	1	2200 pF	CAP, CERM, 2200 pF, 50 V, +/- 10%, X7R, 0603	0603	C0603C222K5RACTU	Kemet
C21	1	0.47uF	CAP, CERM, 0.47 uF, 10 V, +/- 10%, X7R, 0603	0603	GRM188R71A474KA61D	MuRata
C27, C28	2	33 pF	CAP, CERM, 33 pF, 100 V, +/- 5%, C0G/NP0, 0603	0603	06031A330JAT2A	AVX
C29, C30	2	10uF	CAP, CERM, 10 µF, 16 V,+/- 20%, X6S, 0603	0603	GRM188C81C106MA73D	MuRata
C35, C36, C37, C38, C39, C40	6	0.1uF	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X7R, 0402	0402	GRM155R71A104KA01D	MuRata
C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56	16	2 pF	CAP, CERM, 2 pF, 50 V, +/- 5%, C0G/NP0, 0402	0402	GRM1555C1H2R0CA01D	MuRata
D1	1	7.5V	Diode, Zener, 7.5 V, 550 mW, SMB	SMB	1SMB5922BT3G	ON Semiconductor
D2, D5, D6	3	Red	LED, Red, SMD	Red 0805 LED	LTST-C170KRKT	Lite-On
D3	1	30 V	Diode, Schottky, 30 V, 0.2 A, SOT-23	SOT-23	BAT54-7-F	Diodes Inc.
D4	1	Green	LED, Green, SMD	1.6x0.8x0.8mm	LTST-C190GKT	Lite-On
D7	1	Red	LED, Red, SMD	1206	LTST-C150CKT	Lite-On
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1	1		Header, 2.54mm, 5x1, Gold, TH	Header, 2.54mm, 5x1, TH	61300511121	Wurth Elektronik
J2, J5, J6, J7	4		Header, 100mil, 2x1, Gold, TH	Header, 2x1, 100mil	5-146261-1	TE Connectivity

Table 5-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
J3	1		Connector, Receptacle, USB Mini B 2.0, SMT	Connector, Receptacle, USB Mini B 2.0, 5 Position, SMT	65100516121	Wurth Elektronik
J8, J10, J11, J13, J17, J21, J25	7		CONN SMA JACK STR EDGE MNT	CONN_JACK	CON-SMA-EDGE-S	RF Solutions Ltd.
JP1, JP2, JP3, JP4, JP5, JP6, JP10, JP12, JP15	9		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
L1	1	60 ohm	Ferrite Bead, 60 ohm @ 100 MHz, 3.5 A, 0603	0603	MPZ1608S600ATAH0	TDK
L2	1	330 ohm	Ferrite Bead, 330 ohm @ 100 MHz, 2 A, 0805	0805	742792037	Wurth Elektronik
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
Q1, Q3	2	25 V	MOSFET, N-CH, 25 V, 0.22 A, SOT-23	SOT-23	FDV301N	Fairchild Semiconductor
Q2	1	50 V	MOSFET, N-CH, 50 V, 0.22 A, SOT-23	SOT-23	BSS138	Fairchild Semiconductor
R3, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R22, R54, R57, R58, R59, R60, R63, R64, R65, R66, R68, R69, R70, R71, R76, R80, R83, R84, R89, R105	35	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R19, R23	2	1.00k	RES, 1.00 k, 0.5%, 0.1 W, 0603	0603	RT0603DRE071KL	Yageo America
R20, R32, R33, R34, R38, R39, R40, R42, R46, R82, R86, R88, R91, R93, R95, R97, R99, R107, RSB1, RSB3	20	4.99k	RES, 4.99 k, 1%, 0.063 W, 0402	0402	RC0402FR-074K99L	Yageo America
R21, R27, R37, R45	4	10k	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K0JNEA	Vishay-Dale
R35, R36, R43, R44, R81, R85, R87, R90, R92, R94, R96, R98, RSB2	13	22	RES, 22, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060322R0JNEA	Vishay-Dale
R47, R101, R103, R108, R109, R110, R111, R112, R113, R114, R115, R116, R117, R118, R119, R120, R121, R122, R123	19	0	RES, 0, 5%, .05 W, AEC-Q200 Grade 0, 0201	0201	ERJ-1GN0R00C	Panasonic

Table 5-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
R48, R73	2	33k	RES, 33 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060333K0JNEA	Vishay-Dale
R49, R50	2	33	RES, 33, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040233R0JNED	Vishay-Dale
R51	1	1.5k	RES, 1.5 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K50JNED	Vishay-Dale
R52, R78, R79, R106	4	470	RES, 470, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603470RJNEA	Vishay-Dale
R53	1	1.2Meg	RES, 1.2 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031M20JNEA	Vishay-Dale
R55	1	100k	RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KJNEA	Vishay-Dale
R56	1	110k	RES, 110 k, 1%, 0.25 W, 1206	1206	RC1206FR-07110KL	Yageo America
R61, R62	2	9.1k	RES, 9.1 k, 5%, 0.1 W, 0603	0603	RC0603JR-079K1L	Yageo
R67	1	100	RES, 100, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100RJNEA	Vishay-Dale
R72	1	510	RES, 510, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603510RJNEA	Vishay-Dale
R77	1	2.2	RES, 2.20, 1%, 0.1 W, 0603	0603	ERJ-3RQF2R2V	Panasonic
S1	1		Switch, Tactile, SPST-NO, 0.05A, 12 V, SMT	SW, SPST 6x6 mm	FSM4JSMA	TE Connectivity
SH-J1, SH-J4, SH-J6, SH-J7, SH-J9, SH-J12, SH-J13, SH-J14, SH-J15, SH-J16, SH-J17, SH-J18, SH-J19	13	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	8		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
U1	1		Quadruple Bus Buffer Gate With 3-State Outputs, RGY0014A, LARGE T&R	RGY0014A	SN74LVC125ARGYR	Texas Instruments
U2	1		Low-Voltage 24-Bit I2C and SMBus I/O Expander, 24 Outputs, 1.65 to 5.5 V, -40 to 85 degC, 32-pin UQFN (RGJ), Green (RoHS & no Sb/Br)	RGJ0032A	TCA6424ARGJR	Texas Instruments
U3	1		Quadruple 2-Line To 1-Line Data Selector/Multiplexer With 3-State Outputs, RGY0016A (VQFN-16)	RGY0016A	SN74LVC257ARGYR	Texas Instruments
U4	1		500-mA, Low IQ, Small Size, Low Dropout Regulator, DQN0004A (X2SON-4)	DQN0004A	TLV75533PDQNR	Texas Instruments
U5	1		150-mA Ultra-Low Noise LDO for RF and Analog Circuits Requires No Bypass Capacitor, NGF0006A (WSON-6)	NGF0006A	LP5900SD-3.3/NOPB	Texas Instruments
U6	1		4-Channel ESD Protection Array for High-Speed Data Interfaces, DRY0006A (USON-6)	DRY0006A	TPD4E004DRYR	Texas Instruments
U7	1		Single 2-Input Exclusive-OR Gate, DBV0005A (SOT-23-5)	DBV0005A	SN74LVC1G86DBVR	Texas Instruments

Table 5-1. Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
U8	1		25 MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br)	PN0080A	MSP430F5529IPN	Texas Instruments
U9	1		PCIe Gen 1 to Gen 6 Ultra Low Jitter 1:8 LP-HCSL Clock Buffer and Clock MUX	VQFN40	LMKDB1108RKPT	Texas Instruments
Y1	1		Crystal, 24.000 MHz, 20 pF, SMD	Crystal, 11.4x4.3x3.8mm	ECS-240-20-5PX-TR	ECS Inc.
C25, C31, C33	0	10uF	CAP, CERM, 10 µF, 16 V,+/- 20%, X6S, 0603	0603	GRM188C81C106MA73D	MuRata
C26, C32, C34	0	1uF	CAP, CERM, 1 µF, 25 V,+/- 20%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E1X7R1E105M080AC	TDK
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J4	0		Header(shrouded), 2.54mm, 15x2, Gold, TH	Header(shrouded), 2.54mm, 15x2, TH	302-S301	On-Shore Technology
J9	0		SCKT, 40PQFN05-0.40, HIN	SOCKET_QFN40	106458-0037	Ironwood Electronics
J12	0		Connector, SMA, TH	SMA	142-0701-201	Cinch Connectivity
J14, J15, J16, J18, J19, J20, J22, J23, J24, J26, J27, J28	0		CONN SMA JACK STR EDGE MNT	CONN_JACK	CON-SMA-EDGE-S	RF Solutions Ltd.
JP7, JP8, JP9, JP11, JP13, JP14	0		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
R1, R2, R31, R41	0	10k	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310K0JNEA	Vishay-Dale
R4, R24, R25, R26, R28, R29, R30, R74, R75	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R100, R104	0	49.9	49.9 Ohms ±1% 0.05W, 1/20W Chip Resistor 0201 (0603 Metric) Automotive AEC-Q200 Thick Film	0201	ERJ-1GNF49R9C	Panasonic Electronic Components
R102	0	100	RES, 100, 5%, 0.05 W, 0201	0201	RC0201JR-07100RL	Yageo America
SH-J2, SH-J3, SH-J5, SH-J8, SH-J10, SH-J11	0	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec

6 Compliance Information

6.1 Compliance and Certifications

Refer to *LMKDB1108EVM EU Declaration of Conformity (DoC)*.

7 References

For additional information on LMKDB1108, refer to *LMKDB1120/1108/1104/1102/1204/1202 PCIe Gen 1 to Gen 6 Ultra Low Jitter 1:20, 1:8, 1:4, 1:2, 2:4, 2:2 LP-HCSL Clock Buffer and Clock MUX*.

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