Application Report
SNLA128B–July 2010–Revised April 2013

AN-2068 DS90UR241/124 Spread Spectrum Tolerance Support

ABSTRACT

Compliance to EMI limits is often a challenge. Spread spectrum clocking is commonly used to minimize EMI. The effect of modulating periodic signals, both clock and data, reduces the peak emissions by spreading the energy over a range of frequencies. The DS90UR241 and DS90UR124 chipset allows the use of spread spectrum clock and data inputs. The following is a discussion of spread spectrum clock characteristics and the interaction with DS90UR241/124 chipset.

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1 Spread Spectrum Modulation

Three key parameters, frequency deviation, modulation frequency and modulation profile, are used to define a spread spectrum output. Most spread spectrum generators will modulate the fundamental clock frequency by several percent. This modulation may be “center spread” or “down spread”. The rate of this frequency change, modulation frequency, is often quite slow in comparison to the fundamental clock frequency - typically in the 10’s of kHz range.

Table 1 provides guidance for the frequency deviation and modulation frequencies supported by the DS90UR241/124 chipset. This data is based on testing with an ideal source. The input clock signal was modulated by the triangle output of an arbitrary waveform generator. There was a direct connection between serializer and deserializer (no cable). No effects of additional jitter or cable length are included.

Additional factors associated with spread spectrum operation must also be considered. A modulated clock output may contain additional higher frequency jitter components beyond the modulation frequency. It is important that this additional jitter not exceed the input jitter tolerance of the downstream device. Per the DS90UR241 specification, the input jitter tolerance is ±100ps (200ps pk-pk) at the maximum operating frequency of 43 MHz. This value scales with input clock period. For example, at 33 MHz, the recommended input clock jitter maximum increases to 260 ps pk-pk. For a description of measuring peak-to-peak jitter, see the Appendix A.

The frequency profile of the modulated signal is also important. There are two common modulation profiles: triangle and Lexmark (“Hershey Kiss”). Both apply a fixed modulation rate to the clock signal, and are proven to effectively reduce EMI. The DS90UR241/124 is targeted to support these two profiles. Note that some other profiles do exist, with slightly different behavior (varying the modulation rate over a range of frequencies). The DS90UR241/124 is not guaranteed to operate properly with these alternative modulation profiles.

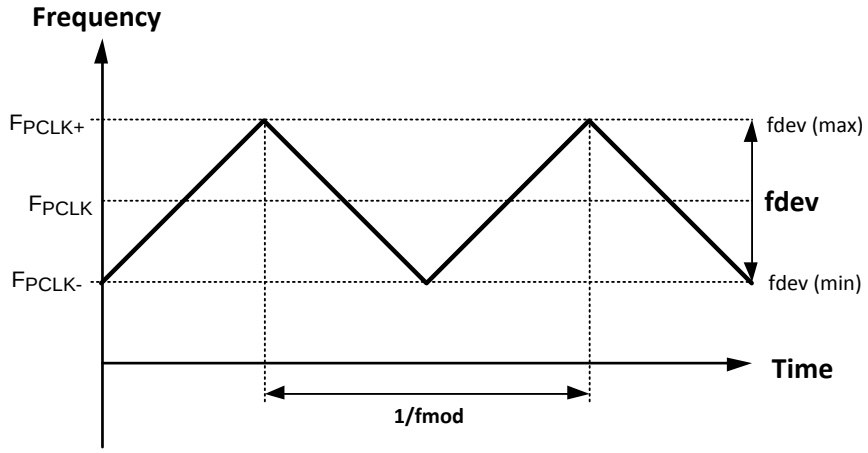

Figure 1. SSC Triangle Modulation

Table 1. Frequency and Modulation Frequencies for SSC (Triangle Modulation Profile)

Maximum f_{dev}	Maximum f_{mod}	
	PCLK = 33 MHz	PCLK = 8 MHz
±4% center spread (8% total)	20 kHz	5 kHz
±2% center spread (4% total)	50 kHz	25 kHz

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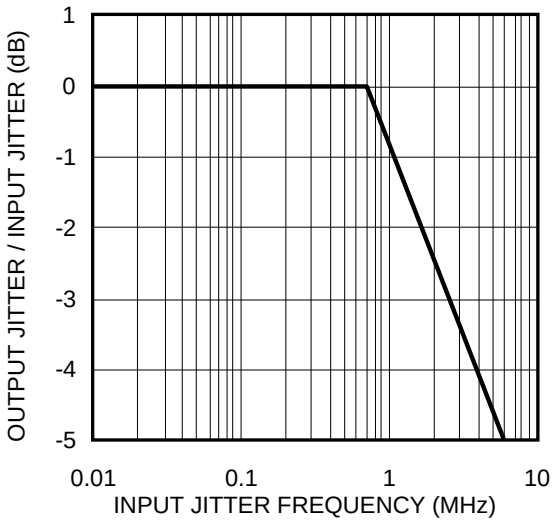

Figure 2. Example of PLL Jitter Transfer (Theoretical)

When viewing the frequency spectra, the energy should be spread evenly across a range as defined by the frequency deviation. Outside of the specified range, the energy should quickly reduce to baseline levels. Additional “peaks” outside the desired deviation range are undesirable, resulting in a high frequency component that the phased-locked loop (PLL) will not track.

2 Theory of Operation: Serializer and Deserializer PLL Response to Jitter

The bandwidth of the device PLL determines its fundamental response to jitter. Input jitter with a frequency below the bandwidth of the PLL, “low frequency jitter”, will be tracked and passed to the output of the PLL. As frequencies increase above the PLL bandwidth, “high frequency” jitter begins to be attenuated as per the jitter transfer curve. Maximum attenuation is achieved beyond the 6dB point. A typical PLL jitter transfer curve is shown in Figure 2. This illustrates gain (ratio of PLL input to output jitter) vs. the frequency of the jitter.

At the serializer input, jitter frequencies below the serializer bandwidth will be tracked by the PLL, and passed along the serial link to the downstream deserializer. Jitter with a frequency above the serializer bandwidth will be attenuated to some degree as defined by the PLL’s jitter transfer curve.

As with the serializer, any jitter below the deserializer bandwidth will be tracked by the PLL and passed to the deserializer’s outputs. Frequencies above the deserializer bandwidth are not tracked, and must be considered with respect to the receiver’s input jitter tolerance specification. For the DS90UR241/124 to operate properly, the deserializer's input jitter tolerance specification (RxINTOL) must be satisfied. High frequency jitter at frequencies >2 MHz will not be tracked and must remain below 0.5UI.

The purpose of the serializer's input jitter specification is to ensure that jitter contributed by the serializer output is limited such that deserializer's RxINTOL can be satisfied by the system. When a typical SSC modulation profile is applied (triange, Lexmark profile), the behavior of the serializer PLL is predictable and follows the PLL jitter transfer curve. At frequencies above the serializer bandwidth (2.6MHz), the input jitter will be attenuated. Therefore, it is critical to limit the jitter at frequencies in the range of 2 - 2.6MHz. This is the range in which the serializer maximum input jitter specification of 0.25UI must be applied. At input jitter frequencies above 2.6 MHz, the magnitude of jitter should remain below 0.4UI.

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Table 2. Serializer Input Jitter Across TCLK Frequency

TCLK Frequency (MHz)	Jitter Frequency (MHz)	Maximum Jitter pk-pk(ps)
43	2 - 2.6	200
	> 2.6	300
33	2 - 2.6	260
	> 2.6	400
25	2 - 2.6	340
	> 2.6	550

3 Alternate Modulation Profiles

The supported modulation profiles, triangle and Lexmark, modulate the clock at a single frequency and do not generate abrupt frequency steps. Some alternative SSC modulation profiles have been shown to exhibit abrupt frequency steps and are not recommended. The instantaneous frequency step results in a frequency error, appearing as excessive jitter at the output of the serializer PLL. Under these conditions the serializer input jitter specification cannot be used to predict the behavior of the serializer output and assure link performance. If an alternate modulation profile is employed, you must assure system operation by measuring the jitter at the receiver input to ensure the RxINTOL specification is satisfied.

4 Response to SSC Source

Spread spectrum clock sources modulate at frequencies well below the bandwidth of the PLLs. This low frequency modulation is easily tracked by the PLLs, and passes along cleanly to the output of the deserializer. However, the generated SSC signal will have additional frequency components, some of which may appear as high frequency jitter or frequency discontinuities. Depending upon the frequency and magnitude of these additional jitter components, input jitter tolerance may be violated and potentially impact the ability to accurately recover serialized data. Therefore, the quality of the SSC generated output is important in the selection of an SSC device. SSC sources with triangle or Lexmark modulation profiles should be used. It is recommended that you select the minimum spread spectrum f_{dev} and f_{mod} necessary to achieve EMC compliance.

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Appendix A Jitter Measurements

It is important to understand the high frequency jitter contribution of a spread spectrum clock source. The high frequency peak-to-peak jitter can be measured using a real-time scope combined with jitter analysis software. When analyzing the peak-to-peak jitter, high-pass and band-pass filters are applied. This focuses the analysis on the specified high-frequency jitter components, and ignores the intentional low frequency modulation of the spread spectrum device. The following section provides specific guidance to measure jitter at the DS90UR241 (serializer) and DS90UR124 (deserializer) inputs.

A number of platforms and tools are available for measurement and analysis of jitter. This section describes the use of Tektronix digital sampling scope and DPOJET jitter analysis tool.

Serializer input jitter should be measured as close as possible to the serializer's TCLK input pin. This is an LVCMOS input signal, switching at a frequency between 10 MHz and 43 MHz. A low capacitance probe with a bandwidth of 1GHz is sufficient for measuring this input signal.

In DPOJET (Jitter and Eye Diagram Analysis Tools) click on:

1. Select → Jitter → **TJ@BER**
2. Configure → Edges → (*under* Signal Type) *select* **Clock**
3. Configure → Clock Recovery → (*under* Method) *select* **Constant Clock – Mean** and (*under* Auto Calc) *select* **Every Acq**
4. Configure → RjDj → In the Data Signal Settings (*under* Pattern Type) *select* **Repeating**, (*under* Pattern Length) *enter* **2** for UI, and (*under* Jitter Target BER) *enter* **12** for BER = 1E-
5. Configure → Filters: (*under* Filter Spec) *select* **2nd Order** and (*under* **High Pass (F1)**) *enter* **2 MHz** for Freq and (*under* **Low Pass (F2)**) *select* **2nd Order** and *enter* **2.6 MHz** for Freq
6. To measure TJ >2.6 MHz remove the **Low Pass (F2)** *select* **No Filter**) and (*under* **High Pass (F1))** *enter* **2.6 MHz** for Freq
7. Results → Single (for Population = 1) or Run (for Population > 1)

The deserializer input is a high-speed differential serial stream. As such, this should be measured across the deserializer input termination resistor using a low capacitance, high-bandwidth (>3GHz) differential probe. Zoom in on the serial stream and look at the rising and falling edges. Make sure the edges are monotonic in nature and have no reflections showing on the edges. If there is a reflection, then the jitter measurements will be larger than if there were no reflection.

1. In DPOJET (Jitter and Eye Diagram Analysis Tools) click on:
2. Select → Jitter → **TJ@BER**
3. Configure → Edges → (*under* Signal Type) *select* **Data**
4. Configure → Clock Recovery → (*under* Method) *select* **PLL — Custom**, (*under* PLL Model) *select* **Type II**, (*under* Damping) *enter* **1.07** and (*under* Loop BW) *enter* **2 MHz**
5. Configure → RjDj → In the Data Signal Settings (*under* Pattern Type) *select* **Arbitrary**, (*under* Window Length) *enter* **5UI** , (*under* Population) *enter* **28**, and (*under* Jitter Target BER) *enter* **12** for BER = 1E-
6. No filter(s) should be used with this measurement
7. Results → Single (for Population = 1) or Run (for Population > 1)

A.1 Equipment

1. Tektronix DSA71604 16 GHz 50GS/s Digital Serial Analyzer with DPOJET software
2. Tektronix P7330 3.5 GHz Differential Probe
3. Tektronix P6247 1GHz Differential Probe

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A.2 Measurement in “UI”

The jitter specification for the receiver input (RxINTOL) is given in terms of unit interval (“UI”). The jitter measurements provided by the jitter analysis tools are commonly presented in terms of time units (picoseconds). This measured time-based value needs to be converted to UI terms for comparison with the 0.5 UI specification. If the input clock rate (TCLK) is known, it is simple to convert from a time-based jitter measurement to jitter in terms of UI.

A unit interval (“UI”) is the time duration of 1 bit in the serialized differential data stream. For every TCLK input clock period, 28 serialized bits are transferred over the differential link. Therefore, UI is defined as: UI = TCLK period (ps) / 28 bits

The conversion from measured jitter (time-based) to “UI” is: jitter (ps) / UI (ps) = jitter (UI)

Here is an example for a system with input clock (TCLK) of 33 MHz, and a measured jitter of 200ps.

- TCLK input clock period =
- UI = 30303 ps / 28 = 1082 ps
- jitter (UI) = 200 ps / 1082ps = 0.18 UI

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