CLC001,DS90CP22,DS90LV001

Making the Most of Your LVDS - 5 Tips for Buffering Signal Integrity Headaches

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Technology Edge

Making the Most of Your LVDS
5 Tips for Buffering Signal Integrity Headaches

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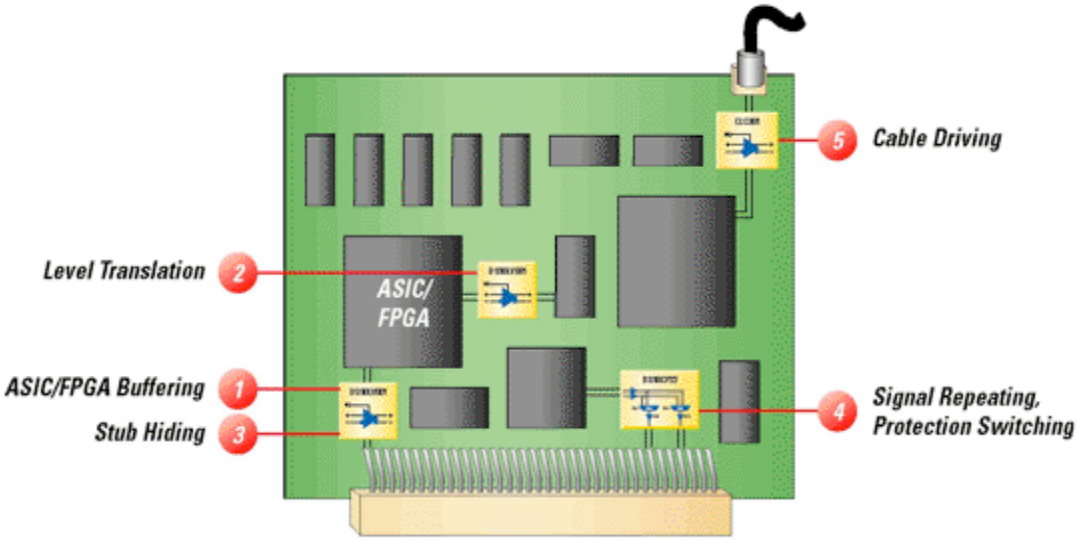
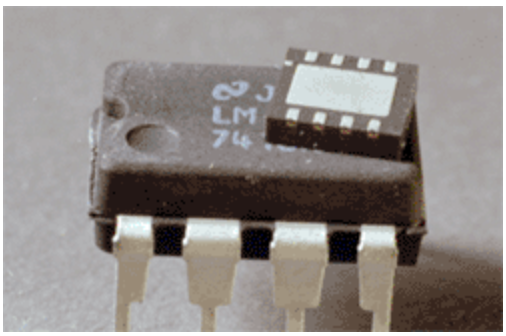
The Low Voltage Differential Signaling (LVDS) standard TIA/EIA-644 has become widely popular and is available on most ASICs and FPGAs as well as on hundreds of standard devices. Thousands of systems have successfully implemented high speed interconnect using LVDS. All LVDS I/Os are not alike, however. Some ASIC and FPGA LVDS I/O may not be as suited to driving off board as LVDS I/O in standard devices. Even standard devices with well-designed I/O may give poor signal quality due to board layout issues. For example, it may not be possible to put the device close to the connector, creating long stubs and reflections. To help cure these interconnect woes, National Semiconductor has recently introduced some small buffers like the DS90LV001, CLC001, and DS92CP22. The following paragraphs describe a few useful applications.



Boosting FPGAs and ASICs

Almost all advanced ASICs and FPGAs include LVDS I/O. Sometimes the design of these LVDS cells do not take full account of the analog nature of high speed signalling. Operating at megabits or gigabits per second requires fast edge rates and precise circuit timing. The bus or cable to be driven is modelled as a transmission line not a lumped load at these speeds. Driving off the printed circuit board (PCB) with these digital LVDS I/O may result in poor signal quality, requiring an LVDS-to-LVDS buffer to boost the signal. The DS90LV001 is an 800 Mbps Single LVDS/LVPECL to LVDS Buffer and is available in a 3 x 3 mm package. Its small size allows it to be added dense PCBs to fix signal integrity issues without a major re-layout of the PCB, making it a useful last minute fix.

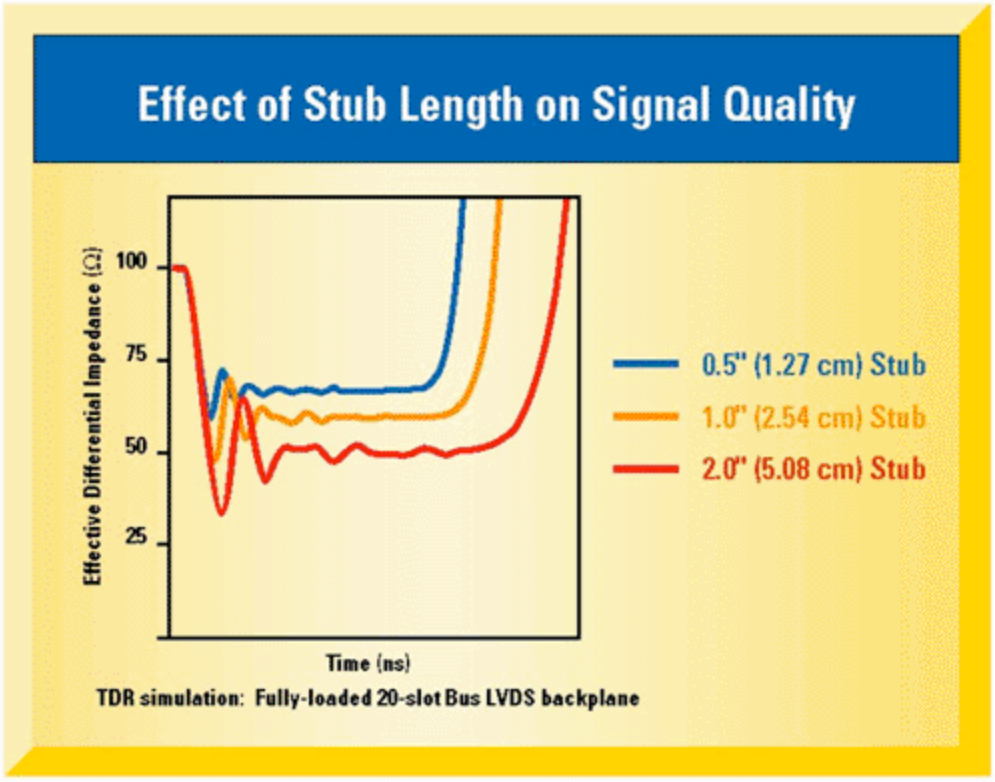


Translating LVDS

Many older high speed ASICs and standard devices use LVPECL signalling. LVPECL I/O have great signalling characteristics, but are not compatible with today s CMOS circuits. Therefore, a system design may be a mix of older Bipolar/BiCMOS LVPECL and newer CMOS LVDS devices, resulting in the need to translate between LVPECL and LVDS. For translating from LVPECL to LVDS, the DS90LV001 directly accepts LVPECL signals providing a clean LVDS output. For LVDS to LVPECL translation, the CLC001 622Mbps Single LVDS/LVPECL to Adjustable Output Buffer translates from LVDS to 800mV levels into 70 ohms (see the CLC001 datasheet for more possibilities).

Hiding Stubs

Even if you ve design in the world s best LVDS device, you may not be able to place it close to the connector. In multidrop and multipoint system topologies, short stub lengths are necessary to minimize reflections. In these systems, stub length has large impact on signal quality and often is the main factor determining top bus speed. When running at 200 Mbps, edge rates will be fast enough to require stubs less than 2-3 cm.



Source: NESA Technical DesignCon99 Whitepaper: Signal Integrity and Validation of National's Bus LVDS Technology in Heavily Loaded Backplanes, www.national.com/lvds

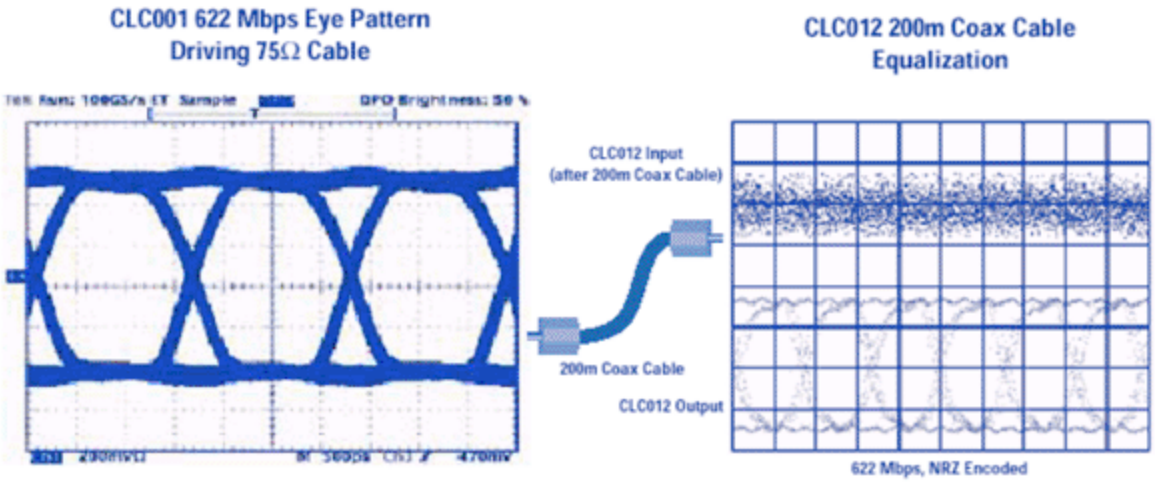
The DS90LV001 Stub-Hider device can be placed within millimetres of the connector, reducing a potentially 3-5 cm stub to less than 2 cm and greatly improving signal quality. As an added benefit, the Stub Hider allows more placement flexibility of the LVDS source/destination chips, mitigating other PCB layout headaches.

Switching and Splitting Signals

Many communications systems require protection switching where a redundant backup serial stream can be switched in to replace a faulty serial stream. National s 800Mbps/Channel DS90CP22 2x2 LVDS Switch can be used as a 2:1 or 1:2 mux to perform this operation. The DS90CP22 can also be used as a signal splitter for clock or data as well as a full 2x2 non-blocking switch. Due to its low 75 ps typical peak-to-peak jitter, it can be used to either fanout or daisy-chain a serial stream to multiple cards without adding excessive cumulative jitter.

Driving Long Cables

LVDS technology drives cables up to about 15 meters depending on data rate, cable quality, and common mode voltage. To drive longer distances, many designers use special electrical or optical transceivers. With the CLC001, this is not necessary. By feeding the CLC001 with a DC balanced serial LVDS stream, it can drive up to 200 m of cable. At the other end of the cable, National s CLC012 Adaptive Equalizer will equalize the signal automatically and recover clock and data. The CLC001/CLC012 chipset can extend the reach of your LVDS signals from ASICs, FPGAs, and standard devices.



Conclusion

New National Semiconductor LVDS buffers are useful tools in the battle for signal integrity, capable of performing a host of tasks such as:

- Hiding long stubs
- Buffering ASIC/FPGA signals
- Translating between LVPECL and LVDS
- Signal splitting
- Protection switching
- Signal repeating
- Driving LVDS streams onto long cables

For more information on these and other LVDS tools, visit www.national.com/lvds.

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