LMH0040,LMH0041,LMH0050,LMH0051,LMH0070, LMH0071,LMH0340,LMH0341,LMH1981

A 3 Gbps SDI Connectivity Solution Supporting Uncompressed 1080p60 Video

Literature Number: SNLA210

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No. 113

A 3 Gbps SDI Connectivity Solution Supporting Uncompressed 1080p60 Video

— By Mark Sauerwald, SDI Applications Engineer, National Semiconductor / Bob Feng, Spartan Applications Engineer, Xilinx

National Semiconductor's Serial Digital Interface (SDI) Smart SerDes combined with the Xilinx Spartan-3 FPGAs and the Xilinx protocol stack, provide a high-performance, cost-effective solution for broadcast for Standard-Definition (SD), High-Definition (HD), and Three-Gigabit SDI (3G-SDI).

Today's high-speed video system designers are faced with significant challenges in addressing both the digital IP and analog physical interface requirements of their products. Because digital and analog components often have very different requirements, supporting both fuctions in a single, ASSP chip often compromises the quality or cost-effectiveness of the solution. It can also be difficult to find a solution that has exactly the right IP and physical interface without waste in area or flexibility to meet the requirements of multiple standards.

A new chip set offered by National Semiconductor and Xilinx combines the best of the digital and analog worlds into one highly integrated solution. The digital heavy lifting, including the protocol IP stack, is handled by the Spartan™-3E or Spartan-3A FPGA silicon. The high-performance analog section is handled by National Semiconductor's family of SDI products to deliver the greatest signal integrity, with the lowest jitter. The highly optimized, combined solution enables faster time to market and increases flexibility for professional audio/video broadcast (AVB) system developers to differential their product offering through IP implemented in the FPGA.

SDI Video Standards

SDI [SMPTE-259M], is a widely adopted broadcast industry standard supporting the transmission of uncompressed SD video signals over a single coaxial cable. By definition, standard definition SDI typically supports data rates of 270 Mbps to cover screen formats of 480i at 60 Hz (480i60).

HD SDI, or HD-SDI [SMPTE-292M], boosts the bit rate up to 1.485 Gbps to support high-definition formats such as 720p60 and 1080i60.

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3G-SDI [SMPTE-424M], further extends the serial digital throughput up to 2.97 Gbps in order to carry the highest screen resolution: 1080p60.

SDI

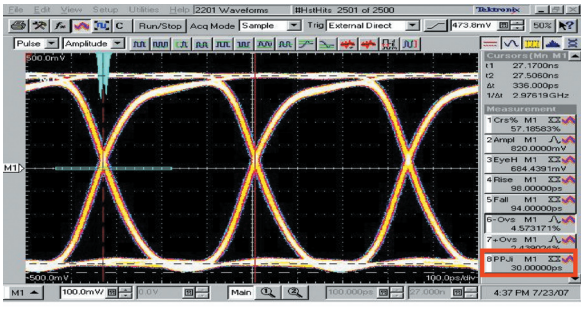
National Semiconductor offers a complete portfolio of products supporting the physical layer transmission for SDI applications and associated video clocks (timing). National's Smart SerDes is a new family of SDI serializers and deserializers with speed grade options supporting SD SMPTE 259M at 270 Mbps, HD SMPTE 292M at 1.485 Gbps, and the new 3 Gbps standard (3G-SDI) SMPTE 424M at 2.97 Gbps (***Table 1***).

Table 1. National Semiconductor's Smart SerDes Family

Product ID	Description	Max Data Rate	Data Rates Supported	SMPTE Standards Supported
LMH0340	Serializer and Driver	3G	2.97G 1.485G 270M	424M 292M 259M
LMH0341	Reclocking Deserializer	3G	2.97G 1.485G 270M	424M 292M 259M
LMH0040	Serializer and Driver	HD	1.485G 270M	292M 259M
LMH0041	Reclocking Deserializer	HD	1.485G 270M	292M 259M
LMH0050	Serializer	HD	1.485G 270M	292M 259M
LMH0051	Deserializer	HD	1.485G 270M	292M 259M
LMH0070	Serializer and Driver	SD	270M	259M
LMH0071	Reclocking Deserializer	SD	270M	259M

National's LMH0340 and LMH0341 deliver industry-leading analog performance:

- Ultra-low output jitter: 50 ps typical at HD and 3 Gbps rates (***Figure 1***)
- Exceptional input jitter tolerance: 0.6 UI minimum (***Figure 2***)



Equipment: Tektronix CSA8000 sampling scope with 20 GHz sampling heads

Input Signal: PRBS 2^{15} -1 Data Rate: 2.97 Gbps

Figure 1. 3 Gbps Output Alignment Jitter from LMH0340: 30 ps

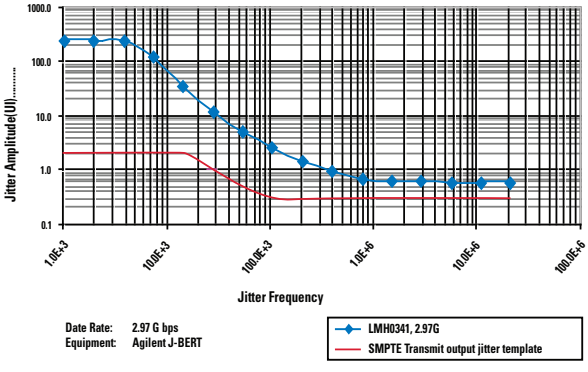


Figure 2. LMH0341 Input Jitter Tolerance

- Integrated, high-precision PLL for serial clock reference and data recovery
- Integrated cable driver in LMH0340 transmitter
- Integrated serial re-clocked loop through and driver
- Low power consumption
- TX: 420 mW
- RX: 515 mW
- No external VCOs or clock cleaning required

In addition to leading-edge analog performance, National's Smart SerDes family reduces the traditional parallel bus between the PHY (serializer or deserializer) and the host FPGA from a 20-bit, single-ended interface to a five-channel Low-Voltage Differential Signaling (LVDS) interface. This innovative narrow differential bus reduces EMI and simplifies board layout by reducing the number of

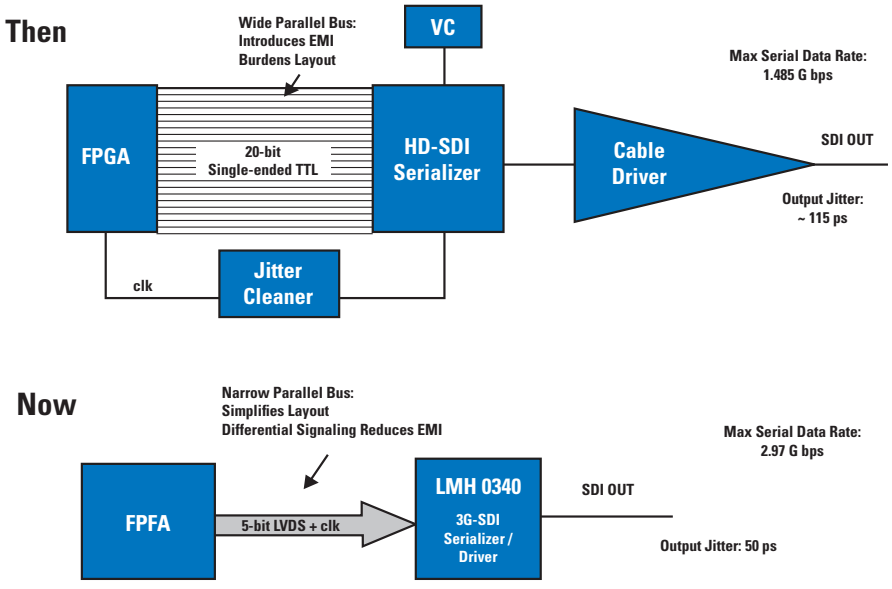


Figure 3. SDI Bill of Materials Reduction

traces on the interface and using fewer pins on the host FPGA. Additionally, National's discrete serializers and deserizlizers do not require any external VCOs or jitter-reducing PLLs (***Figure 3***).

The combined National/Xilinx Spartan solution enables low-cost FPGAs into the high-end AVB market supporting SD, HD, and 3 Gbps data rates for professional video applications.

Spartan Features for Video Applications

The Spartan-3E and Spartan-3A FPGA families suit many aspects of video applications by offering high performance, high density (logic and I/O), great flexibility, and scalability with unique, cost-effective features such as:

- 50,000 to 1.6 million system gates
- True LVDS differential I/O drivers at more than 666 Mbps, with internal termination on receiver for direct chip-to-chip communication
- Double Data Rate (DDR) I/O registers at more than 300 MHz to increase effective bandwidth beyond 600 Mbps
- 18-Kb dual-port block RAMs at more than 200 MHz for FIFOs and data buffering
- Dedicated 18 x 18 multipliers at more than 200 MHz for high-speed digital signal processing
- Digital clock managers (DCMs)
- Clock deskew
- Frequency synthesis
- High-resolution phase shifting
- Wide frequency range (5 MHz to more than 300 MHz)
- Full programmability to easily modify the design during development or in the field, or to support multiple standards in a single solution
- Software and IP to quickly implement key features of video applications
- Design examples and reference boards to get started quickly

By using FPGAs, you can be compliant to industry standards while differentiating yourself from your competitors. Such differentiation may be too difficult to find using an ASSP solution and too expensive to address with an ASIC. The flexibility of a programmable solution provides faster time to market, while field updates provide longer time in market. Numerous standards (and versions) cause uncertainty, so designs need flexibility in transmission schemes, MPEG profiles, display formats, and color correction.

Ultra Low-Jitter Sync Separator for SD/HD Video

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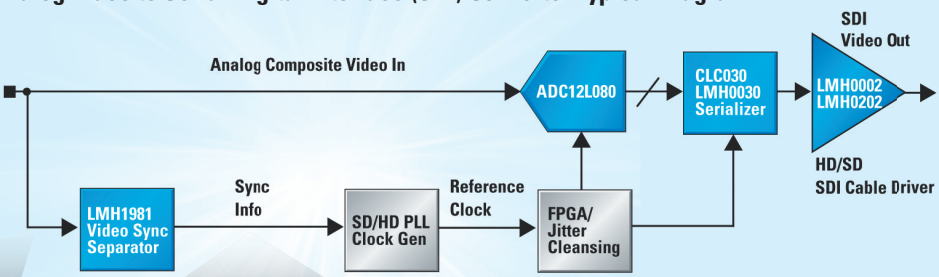
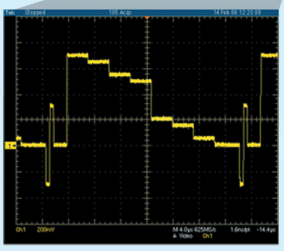
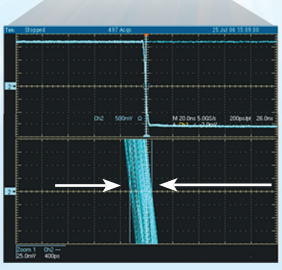
LMH1981 Features 50% Sync Slicing for Precise Output Timing

Analog Video to Serial Digital Interface (SDI) Converter Typical Diagram





720p/60 Tri-Level Input



350 ps_{p-p}

720p/60 H-Sync Output

LMH1981 in TSSOP-14 packaging
Shown at actual size 4.40 x 5.00 x 0.90 mm

AVAILABLE LEAD-FREE

LMH1981 Features

- 50% sync slicing
- Low-jitter horizontal sync outputs
- Supports NTSC, PAL, SECAM, 480i, 480p, 576i, 576p, 720p, 1080i, and 1080p
- Accepts video signals from .05 V_{P-P} to 2 V_{P-P}
- No external programming with µC required
- Horizontal sync output propagation delay <50 ns
- 3.3V or 5V single supply operation

LMH1981 Outputs

- Horizontal sync
- Vertical sync
- Odd/Even field
- Burst/back porch clamp
- Composite sync
- Video format (horizontal lines/field)

Applications

Ideal for use in sync separation, A/V clock generation, video genlock, back porch clamp generator, video format detection circuit, and analog-to-SDI converter applications

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Interconnect Soft SERDES and Protocol IP Stack

While the National Semiconductor Smart SerDes, equalizer and cable driver take care of the SDI physical interface, the FPGA plays an essential role in supporting all digital functions in the protocol IP stack, including:

- 20:5/5:20 LVDS soft serialization and de-serialization (SERDES)
- SMPTE scrambling/descrambling
- Video framer/de-framer
- CRC and line number insertion
- Rasterization
- ANC insertion
- Video standard detection and flywheel

The FPGA design is effectively divided into two frequency domains: "soft SERDES" and "pixel processing," as illustrated in ***Table 2***. The clock frequency used in the soft SERDES is typically only half of the serialization bit rate, by leveraging the DDR technique. On the other hand, the pixel processing clock frequency is determined by the relevant video transmission format: 74.25 MHz for 720p60 and 148.5 MHz for 1080p60.

Table 2. FPGA Design Frequency Domains

	Soft SERDES	Pixel Processing
SD-SDI	27 MHz	27 MHz
HD-SDI	148.5 MHz	74.25 MHz
3G-SDI	297 MHz	148.5 MHz

The timing closure challenge is mainly on the soft SERDES side, as 297 MHz operation is required to achieve 594 Mbps across all of the differential channels. The Xilinx® Spartan applications team has been offering this soft SERDES reference design in a beta version since May 2007. Since then, Xilinx and National Semiconductor have conducted extensive testing. All three data rates have passed BERT test suites developed by Xilinx. ***Figure 4*** illustrates the basic SERDES construct.

Xilinx has a long history of supporting SDI interfaces in the Virtex™ family of FPGAs. XAPP514, "Audio/Video Connectivity Solutions for the Broadcast Industry," is a video connectivity IP and reference design book that details all aspects of the protocol stack: SDI, HD-SDI, DVB-ASI, SDTV/

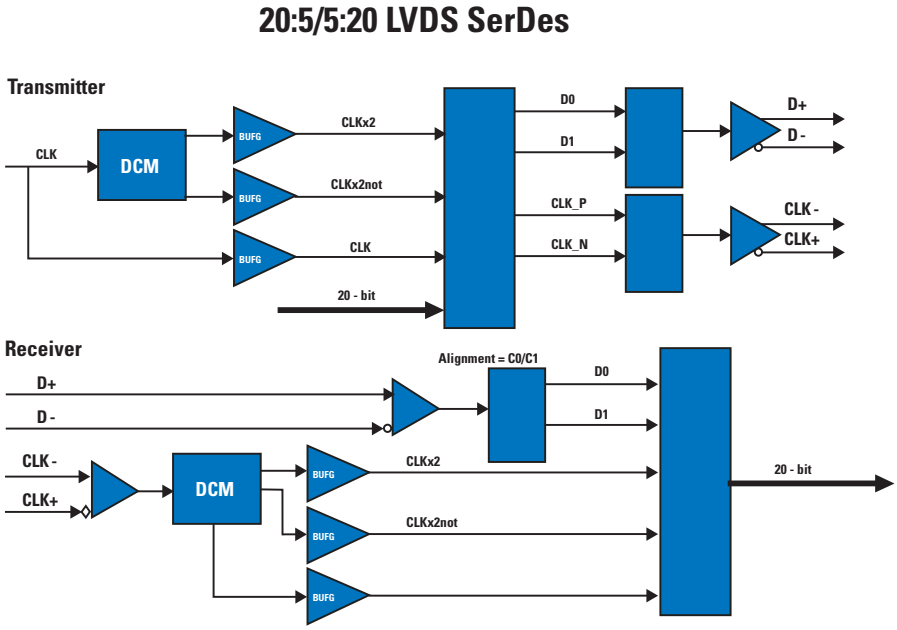

Figure 4. Basic Soft SERDES Construct in Spartan-3E FPGAs

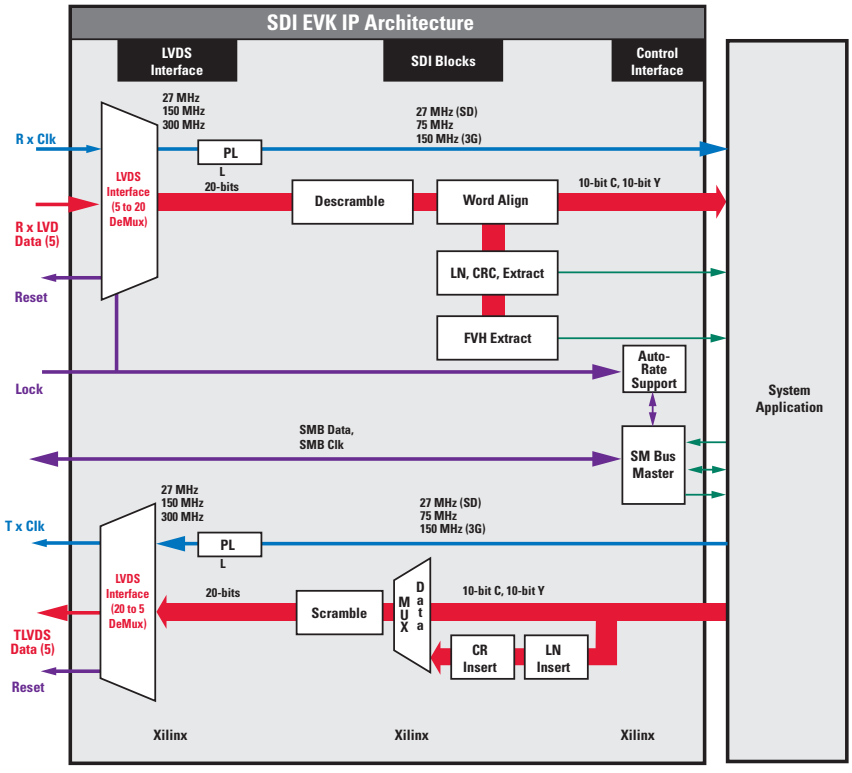

Figure 5. Successfully Ported Reference Blocks from XAPP514

HDTV test pattern generation, and even embedded audio. Xilinx and National Semiconductor are actively working to port these highly valuable reference designs into Spartan-3E and Spartan-3A FPGAs. ***Figure 5*** illustrates a list of successfully ported reference blocks used for demonstration purposes based on an internal evaluation board.

Target Applications

Xilinx low-cost Spartan-3 generation FPGAs have proven track records in a wide range of consumer and professional video applications. The combination of the Spartan FPGA as the digital logic and National Semiconductor Smart SerDes as the analog interface opens up new possibilities in high-end applications in professional video, broadcasting, and digital cinema. Applicable products include high-definition video cameras, digital video recorders, video editors, and display monitors.

Conclusion

The power of Xilinx Spartan-3E and Spartan-3A FPGAs, combined with National's proven SD/HD/3G-SDI Smart SerDes and the XAPP514 protocol IP, delivers a cost-effective solution to the ever-increasing data throughput requirements of broadcast video applications. The complete hardware solution is available today and a complete SDI evaluation kit will be offered by Xilinx's distribution partner Avnet in the first quarter of 2008.

Take the Next Step

- To learn more about SDI resources, visit www.national.com/sdi
- Download XAPP514, "Audio/Video Connectivity Solutions for the Broadcast Industry." ■

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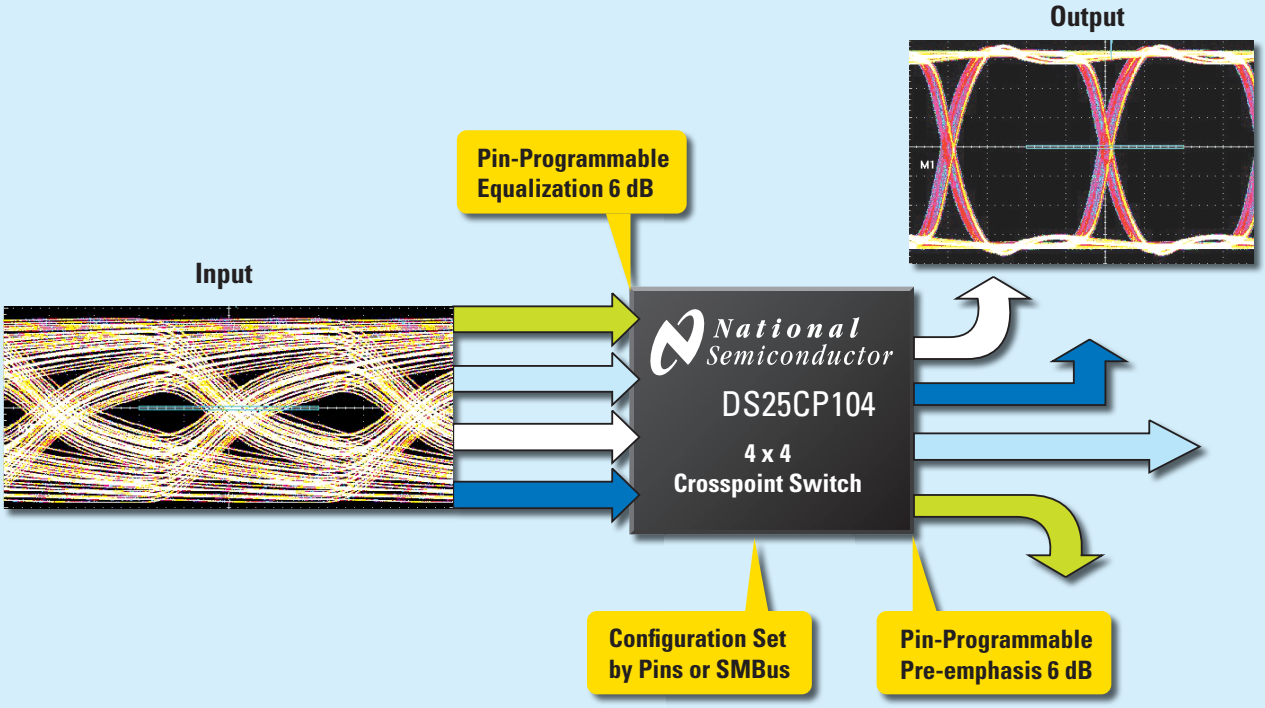

DS25CP104 Features

- 3.125 Gbps max data rate
- 10 ps typ jitter
- I_{CC} 37 mA per channel (typ)
- 6 dB pin-programmable equalization compensates for lossy cables, backplanes
- 6 dB pin-programmable pre-emphasis for improved cable driving
- Crosspoint configurable using external pins or SMBus
- Available in LLP-40 packaging

LVDS Crosspoint Switches

Product ID	Function	Max Datarate	Features	Power
DS25CP152	2 x 2	3.125 Gbps	Pre-emphasis, 8 KV ESD, Equalizatin	211 mW
DS25CP104	4 x 4	3.125 Gbps	Pre-emphasis, SM Bus, Equalization	495 mW

Applications

Ideal for use in communication switches, routers, and muxes, also in video routers and switches, and automated test equipment

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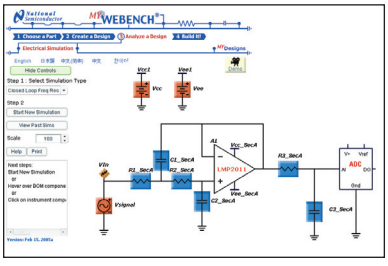
Design Tools



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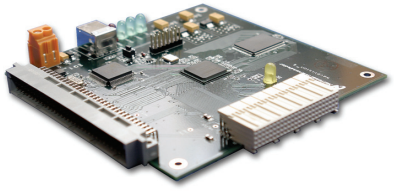

Features and benefits:

- Plug-n-play ADC evaluation board
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- PC-based data capture
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- Highlighted harmonic and SFDR frequencies
- Easy waveform examination
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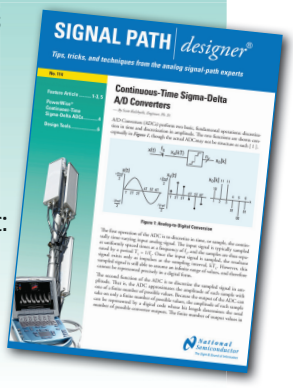

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