DS110DF111EVM Evaluation Board

User's Guide

Literature Number: SNLU142A
May 2014–Revised January 2016

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DS110DF111EVM Evaluation Board

1 Overview

The DS110DF111EVM – SMA evaluation kit provides a complete high band-width platform to evaluate the signal integrity and signal conditioning features of the Texas Instruments signal conditioning products – with Equalization and De-emphasis.

SMA edge launch connectors are used as the input and the output connections for this evaluation board. Commercially available adaptor boards can be purchased to facilitate connection to cables or backplane interconnects.

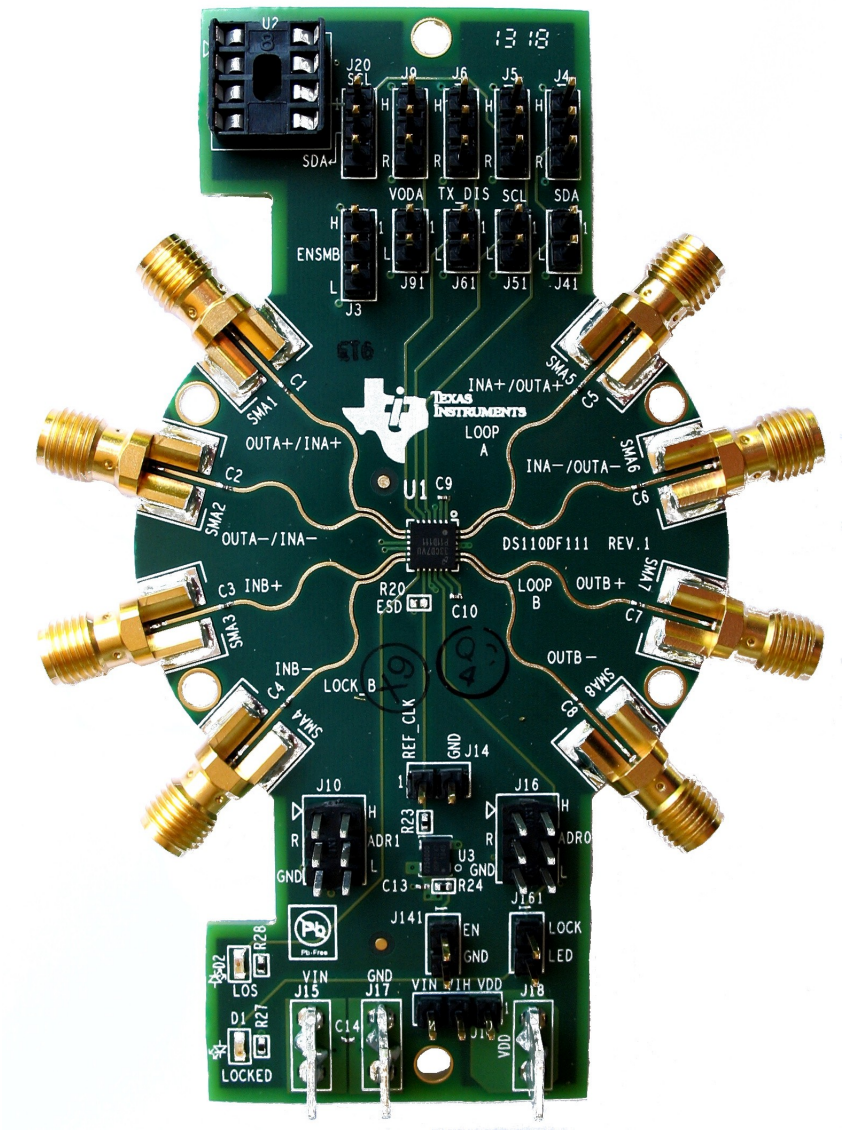


Figure 1. DS110DF111EVM

2 Features

- Fully Adaptive CTLE up to 34 dB Boost
- Self-tuning 5-tap DFE
- Adjustable Receive Equalization
- Raw Equalized and Re-timed Data Loopback
- Adjustable Transmit VOD: 600 – 1300 mVp-p
- Settable Transmit De-emphasis Driver to -12 dB
- Low Power Consumption: 200 mW/Channel
- Locks to Half/Quarter/Eighth Data Rates for Legacy Support
- On-chip Eye Monitor (EOM), PRBS Generator
- Input Signal Detection, CDR Lock Detection/Indicator
- Programmable via Pin Selection or SMBus Interface
- Single Supply Operation: VIN = 3.3 V±10% or V_{DD} = 2.5 V ±5%
- -40°C to +85°C Operation
- High Speed Signal Flow–thru Pin-out Package – RTW: 24-pin QFN (4 mm x 4 mm, 0.5 mm Pitch)

3 Applications

- Front Port Optical Interconnects
- SFF-8431
- 10G/1G Ethernet
- CPRI

4 Ordering Information

EVM ID	DEVICE ID	DEVICE PACKAGE
DS110DF111EVM	DS110DF111SQ	24WQFN

5 Setup

This section describes the jumpers and connectors on the EVM, as well and how to properly connect, set up and use the DS110DF111EVM.

The DS110DF111EVM – SMA evaluation kit can be used in three different modes.

1. Pin Control Mode – provides access to selected signal integrity settings.
2. SMBus Slave Mode – full access to signal integrity and control settings.
3. EEPROM Mode – full access to signal integrity and control settings. EEPROM mode is a convenient method of programming one or more DS110DF111 devices on system power-up when a SMBus master (micro-controller or similar) is unavailable in the design.

This EVM and documentation focus on Pin Control and SMBus Slave Mode to highlight the ease-of-use and excellent low-jitter performance of the DS110DF111.

5.1 Pin Control Mode

In Pin Control Mode, the external control pins on the DS110DF111 are used to configure the signal integrity and control settings of the device. In this mode only a subset of the VOD and de-emphasis (DEMA/B) levels are available. Due to the limited number of control pins, a limited bandwidth 4-level input scheme has been implemented across the control pin interface. This allows for improved DE and VOD control with fewer physical pins.

The 4 levels are defined below:

Table 1. Four-Level Logic Settings

Level	Input Pin Setting
Low - 0	1 kΩ to GND
Resistor - R	20 kΩ to GND
Float - F	Open
High - 1	1 kΩ to V_{DD}

The EVM interfaces to this 4-level IO using the setup below. Only one shunt connection is required to access any of the 4 levels. This methodology minimizes the risk of improper connections that could damage the board or board power supply.

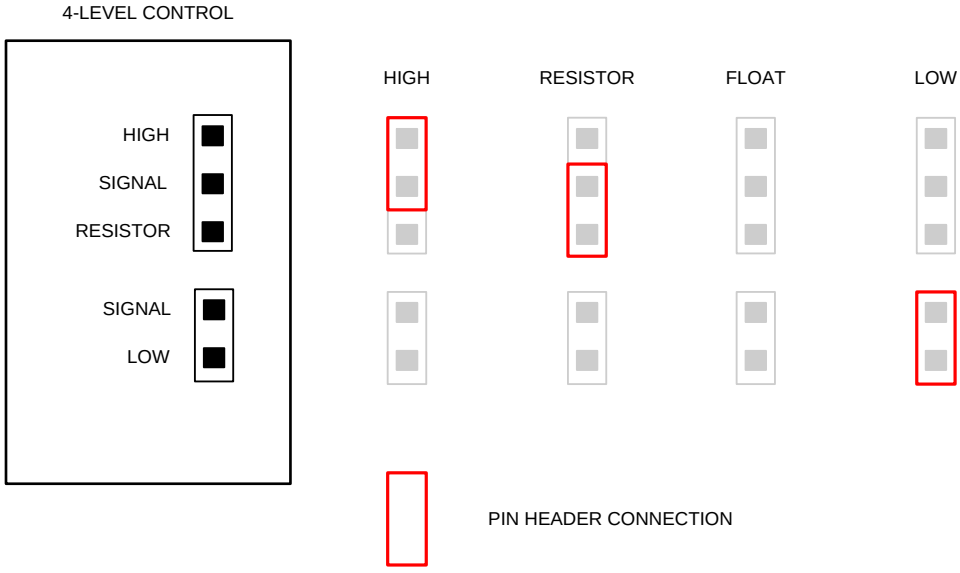


Figure 2. 4-Level IO Control on EVM

5.1.1 Pin Control Mode Configuration

The DS110DF111EVM is shipped ready to use in pin control mode. The EVM will require the following power supply inputs and jumpers.

1. J17 - GND
2. J19 – V_{IN} to V_{IH} : 3.3 V supply operation, 2.5 V internal regulator is enabled
3. J15 – V_{IN} = 3.3 V: Use internal regulator to convert 3.3 V supply to internal supply level of 2.5 V

NOTE: The 2.5 V level may be observed on J18 (V_{DD}) or the device V_{DD} pins. While in 3.3 V mode, J18 (V_{DD}) is a regulated output voltage. Do not connect a 2.5 V supply to this pin.

4. J3 – ENSMB = 1 kΩ to GND (L): Pin Control Mode
5. J6 - Loopback = 1 kΩ to V_{IN} (H): Normal operation, INA - to - OUT A and INB - to - OUT B
6. J91 - VODA = 1 kΩ to GND (L): 600 mV output VOD on OUT A
7. J10 - VODB = 1 kΩ to GND (L): 600 mV output VOD on OUT B
8. J41 - DEMA = 1 kΩ to GND (L): 0 dB De-emphasis on OUT A
9. J51 - DEMB = 1 kΩ to GND (L): 0 dB De-emphasis on OUT B
10. J161 - LOCK: With shunt installed LOCK LED will light Green when DS110DF111 CDR is in the locked state

5.1.2 VOD and De-Emphasis

The DS110DF111 silicon uses pin strapping to define the VOD and DE level of the outputs. See Table 2 and Table 3 for a complete list of VOD and DE settings.

Table 2. DS110DF111 VOD Levels

VODA/B	Bit 2, sel_vod[2]	Bit 1, sel_vod[1]	Bit 0, sel_vod[0]	Output VOD (mVppd)
0	0	0	0	600
R	0	0	1	700
	0	1	0	800
	0	1	1	900
F	1	0	0	1000
1	1	0	1	1100
	1	1	0	1200
	1	1	1	1300

Table 3. DS110DF111 DEM Levels

DEMA/B	Reg 0x15 Bit [2]	Reg 0x15 Bit [1]	Reg 0x15 Bit [0]	Reg 0x15 Bit [6]	De-Emphasis (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6

Table 3. DS110DF111 DEM Levels (continued)

DEMA/B	Reg 0x15 Bit [2]	Reg 0x15 Bit [1]	Reg 0x15 Bit [0]	Reg 0x15 Bit [6]	De-Emphasis (dB)
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-9.0
	1	1	1	0	-12.0

5.1.3 Equalization

There are no pin control settings for the input Equalization. The DS110DF111 input equalization will automatically adapt for divide ratios 1 and 2. For divide ratios 4 and 8 a pre-set equalization level is used.

5.1.4 Loopback

J6 and J61 control the DS110DF111EVM loopback function according to Table 4.

Table 4. DS110DF111 Loopback Control

Loopback	Mode of Operation	IN A	IN B
0	Loopback	Output B	Output A
R	Fanout Input A	Output A	Output A
F	Fanout Input B	Output B	Output B
1	Normal Operation	Output A	Output B

5.1.5 LOS and LOCK

- LOS Function: The LOS function monitors the Input of Channel A for a valid signal. When there is a valid signal on Input A the LED will light up. Channel B does not have any effect on the LOS output signal.
- LOCK Function: The LOCK function monitors both Channel A and Channel B for a valid Lock condition. If either channel has a valid Lock the LED will light up.

5.2 SMBus Slave Mode

The SMBus can also be used to control DS110DF111 devices. This method has the advantage of independent channel control and finer signal conditioning granularity.

1. J17 – GND
2. J19 – V_{IN} to V_{IH}: 3.3 V supply operation (2.5 V internal regulator is enabled)
3. J15 – V_{IN} = 3.3V: Use internal regulator to convert 3.3 V supply to internal supply level of 2.5 V

NOTE: The 2.5V level may be observed on J18 (V_{DD}) or the device V_{DD} pins. While in 3.3 V mode, J18 (V_{DD}) is a regulated output voltage. Do not connect a 2.5V supply to this pin.

4. Floating the AD[1:0] inputs will result in an SMBus Address = 00 = 30'h
5. J3 – ENSMB = H: SMBus Slave Mode
6. Connect the board signals SDA, SCL, and GND on J20 to a DPS-DONGLE-EVM or an equivalent USB2ANY device. A pull-up resistor is needed on the SMBus clock and data signals; place jumpers on pins 1-2 of J4 and J5 to connect a 1 kΩ pull-up resistor to SCL and SDA. The address line settings on J16 (ADR0) and J10 (ADR1) are pin strap settings which get latched on power up and retain their value until the DS110DF111 is power cycled.
7. The DS110DF111's control and signal integrity settings are programmable with SigCon Architect, a GUI which supports full register access through SMBus communication. An example of a DS1xxDF111EVM connected to a PC through a DPS-DONGLE-EVM is shown in Figure 3 and Figure 4. The possible SMBus address settings are shown in Table 5. For more information about SigCon Architect, reference the "SigCon Architect: Installation and Starter's Guide" (SNLU178).

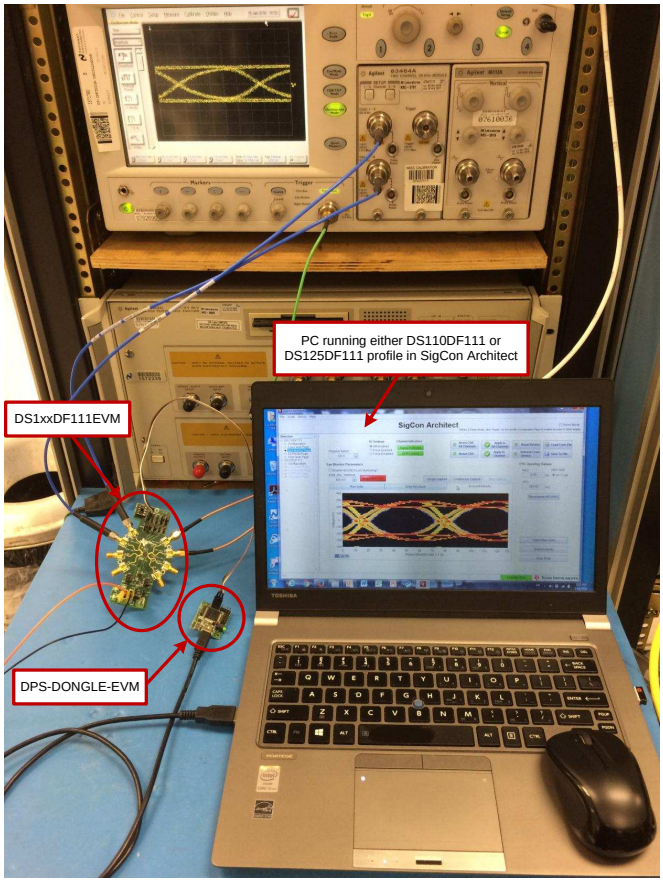


Figure 3. DS1xxDF111EVM Slave Mode Full Setup

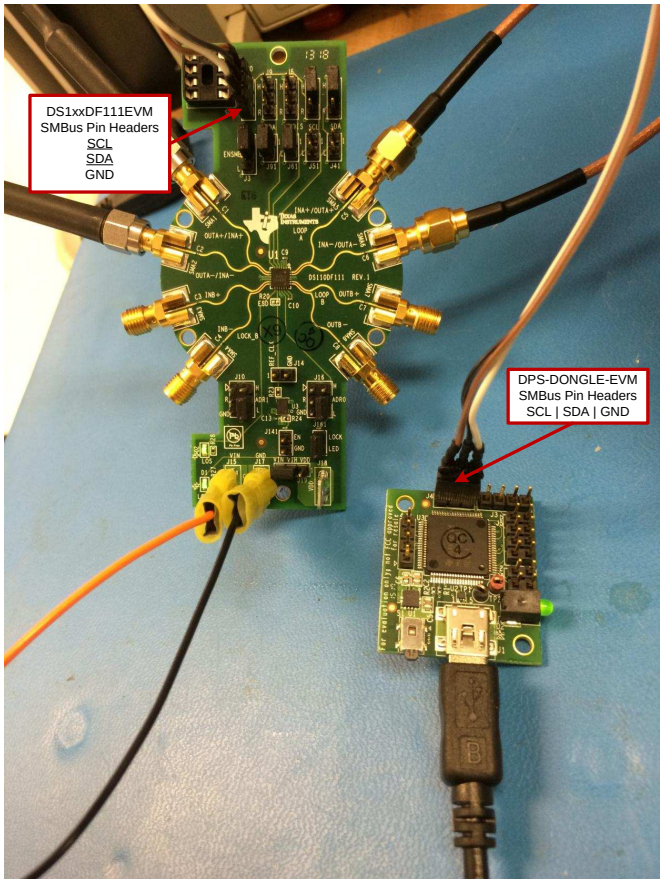


Figure 4. DS1xxDF111EVM Slave Mode Close-Up

Table 5. SMBus Write Address Assignment(1)

ADDR1	ADDR0	SMBus Write	SMBus Read
0	0	0x30	0x31
0	1	0x32	0x33
1	0	0x34	0x35
1	1	0x36	0x37

(1) A floating ADDR[1:0] pin at power-up will be interpreted as a logic 0.

5.2.1 Register Architecture and Bit Fields

There are two types of device registers in the DS110DF111. These are the Control/Share Registers and the Channel Registers. The Control/Share Registers control or allow observation of settings which affect the operation of all channels of the DS110DF111. They are also used to select which channel of the device is to be the target channel for reads from and writes to the Channel Registers.

The Channel Registers are used to set all the configuration settings of the DS110DF111. They provide independent control for each channel of the DS110DF111 for all the configurable device characteristics. Any registers not described in the datasheet tables should be treated as Reserved. The user should not try to write new values to these registers. The user-accessible registers described in the datasheet provide a complete capability for customizing the operation of the DS110DF111 on a channel-by-channel basis.

Many of the registers in the DS110DF111 are divided into bit fields. This allows a single register to serve multiple purposes, which may be unrelated. Often configuring the DS110DF111 requires writing a bit field that makes up only part of a register value while leaving the remainder of the register value unchanged.

5.2.2 Using SigCon Architect

SigCon Architect can be used to program the DS110DF111EVM. In order to use SigCon Architect for SMBus Slave Mode access control, a DPS-DONGLE-EVM (see SNLU184) or USB2ANY equivalent adapter board must be used. This adapter board serves as an interface board to allow SMBus communication between the PC and the DS110DF111 retimer. The SigCon Architect GUI features high level control, low level register bit level control, and an Eye Monitor page to program the device. Examples of these pages are shown in the following figures.

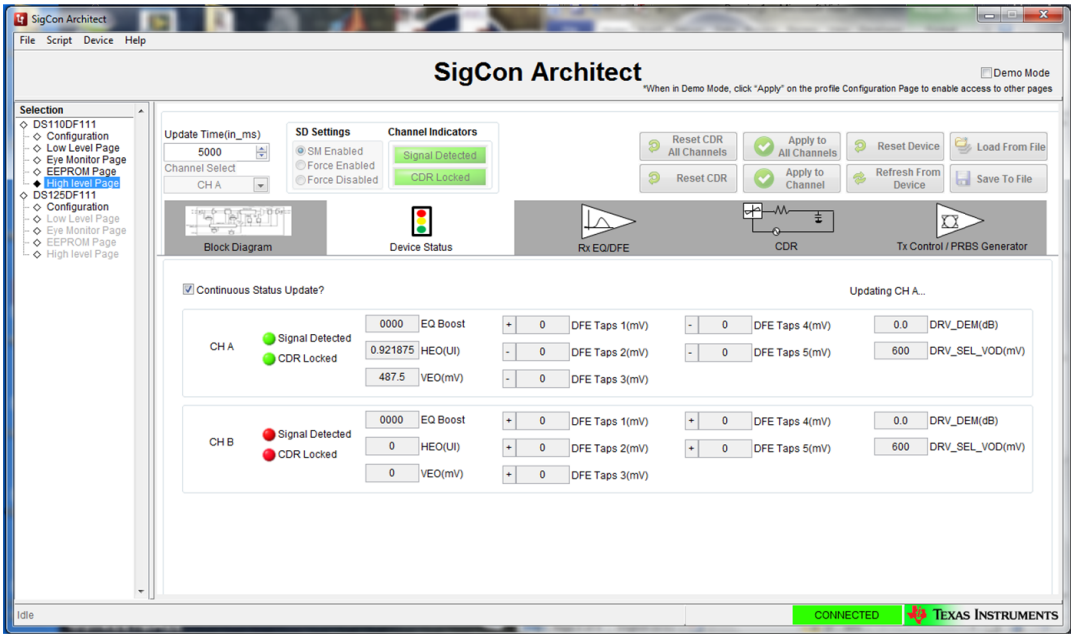


Figure 5. DS110DF111 High Level Page

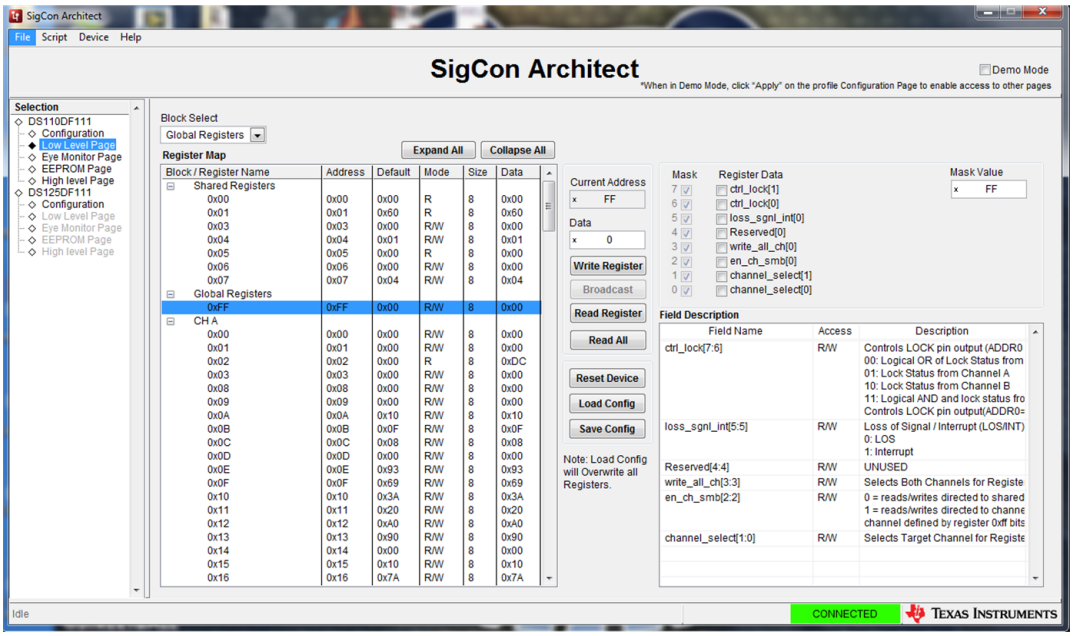


Figure 6. DS110DF111 Low Level Page

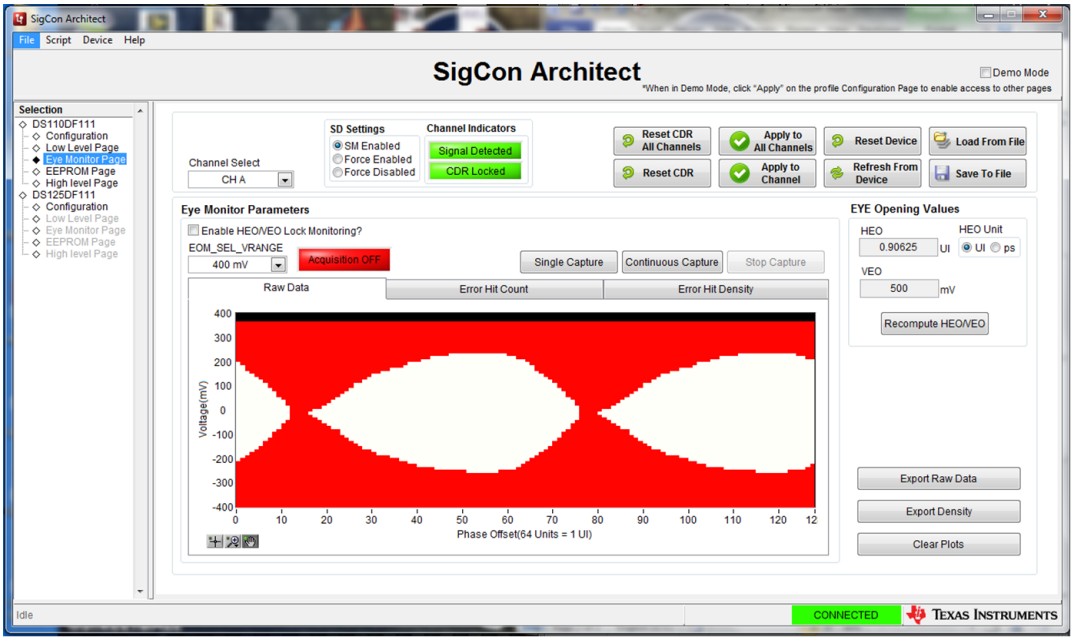


Figure 7. DS110DF111 Eye Monitor Page

For more information about functions about SigCon Architect and the retimer profiles, please reference the "SigCon Architect: Installation and Starter's Guide" (SNLU178) and the "DS110DF410EVK, DS110DF410EVK, and DS125DF410EVM Evaluation Board Software Installation, Setup, and Operating Guide" (SNLU126).

5.3 EEPROM Mode

A serial EEPROM may also be used to configure one or more DS110DF111 devices. This configuration mode is accessed by setting ENSMB = FLOAT. When the DS110DF111 is placed in EEPROM Mode, the DS110DF111 will attempt to load its startup settings from a programmed EEPROM in the 8-pin DIP socket (U2). SigCon Architect can be used to generate an EEPROM Hex file by configuring the EEPROM page settings.

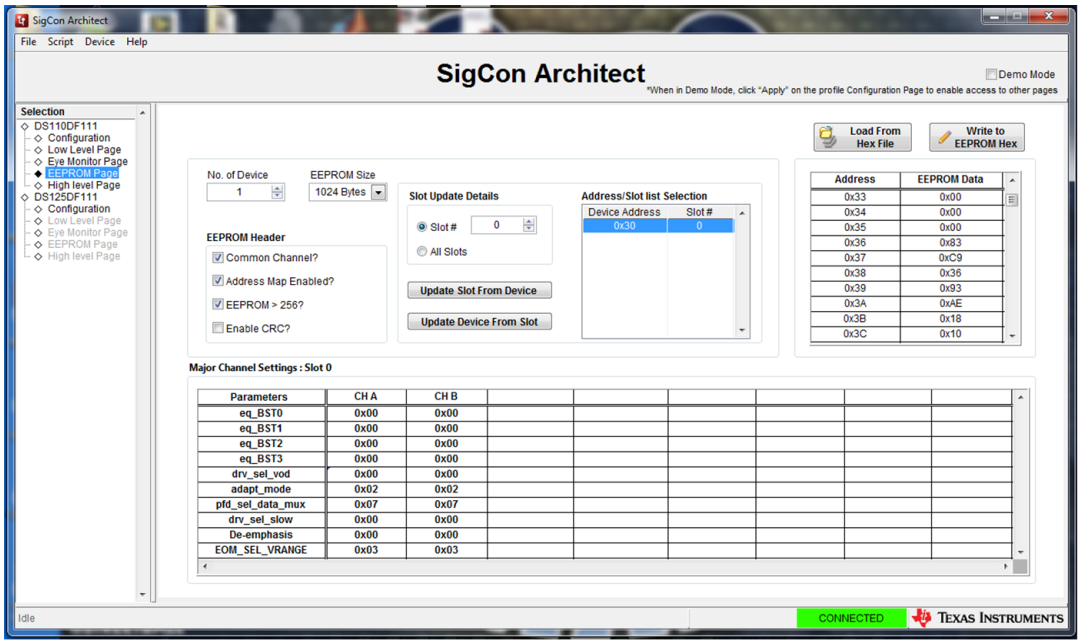


Figure 8. DS110DF111 EEPROM Hex File Generation Page

SigCon Architect cannot directly program the EEPROM. A third-party tool must be used to write the EEPROM hex file into a valid EEPROM. For details about EEPROM hex file generation, please reference "Understanding EEPROM Programming for 10G to 12.5G Retimers" (SNLA245) and the "DS110DF410EVK, DS110DF410EVK, and DS125DF410EVM Evaluation Board Software Installation, Setup, and Operating Guide" (SNLU126).

6 EVM Layout

Figure 9 and Figure 10 show the board layout for the DS110DF111EVM. The EVM uses simple 100 mil headers to control the output signal integrity functions. The DS110DF111EVM is very compact and low power, the board traces have been designed for connection to standard 50 Ω test equipment and cables. The QFN package offers an exposed thermal pad to enhance electrical and thermal performance (this pad must be soldered to the copper landing on the PCB).

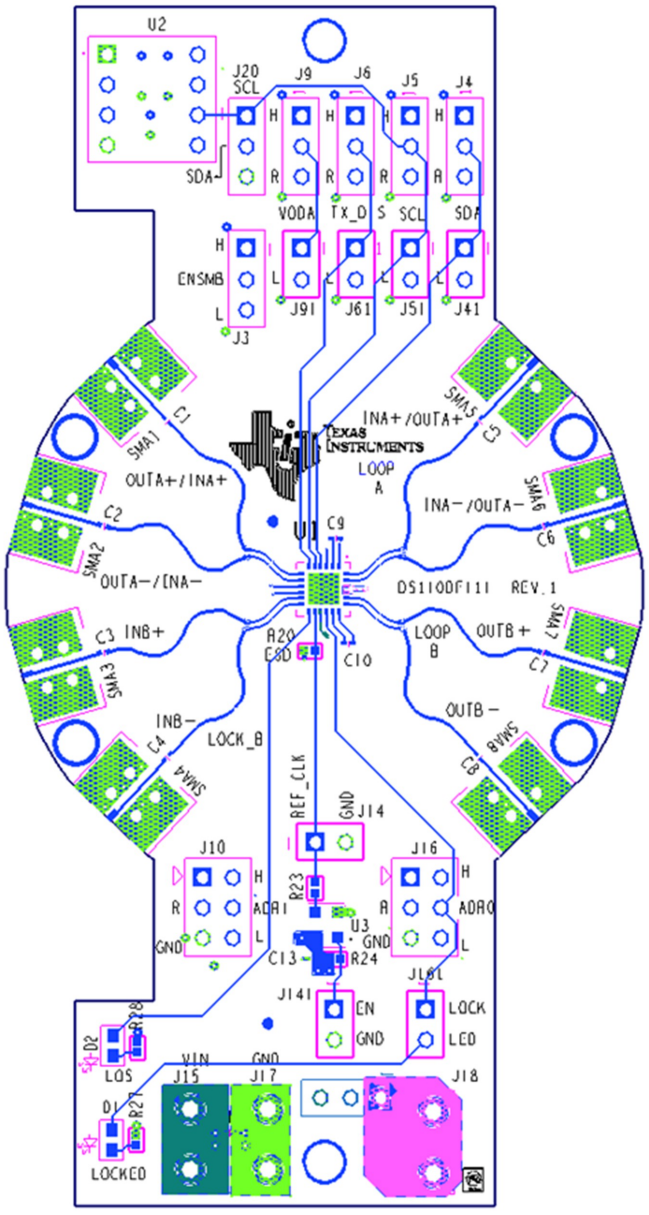


Figure 9. Top Assembly Layer

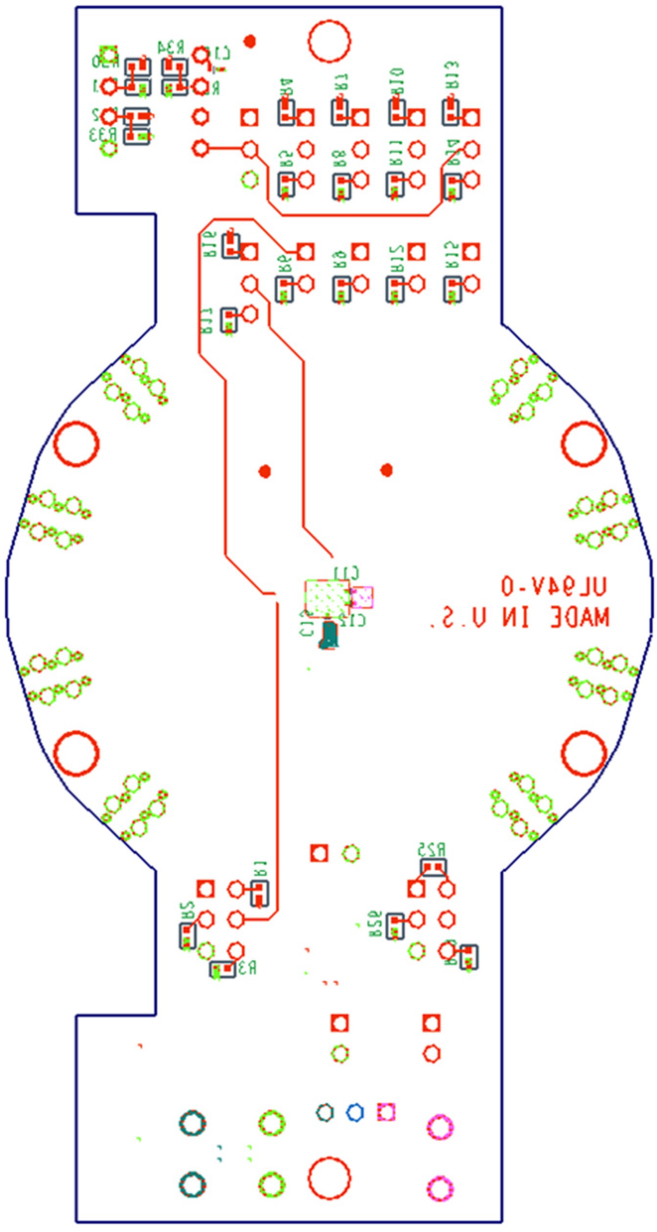
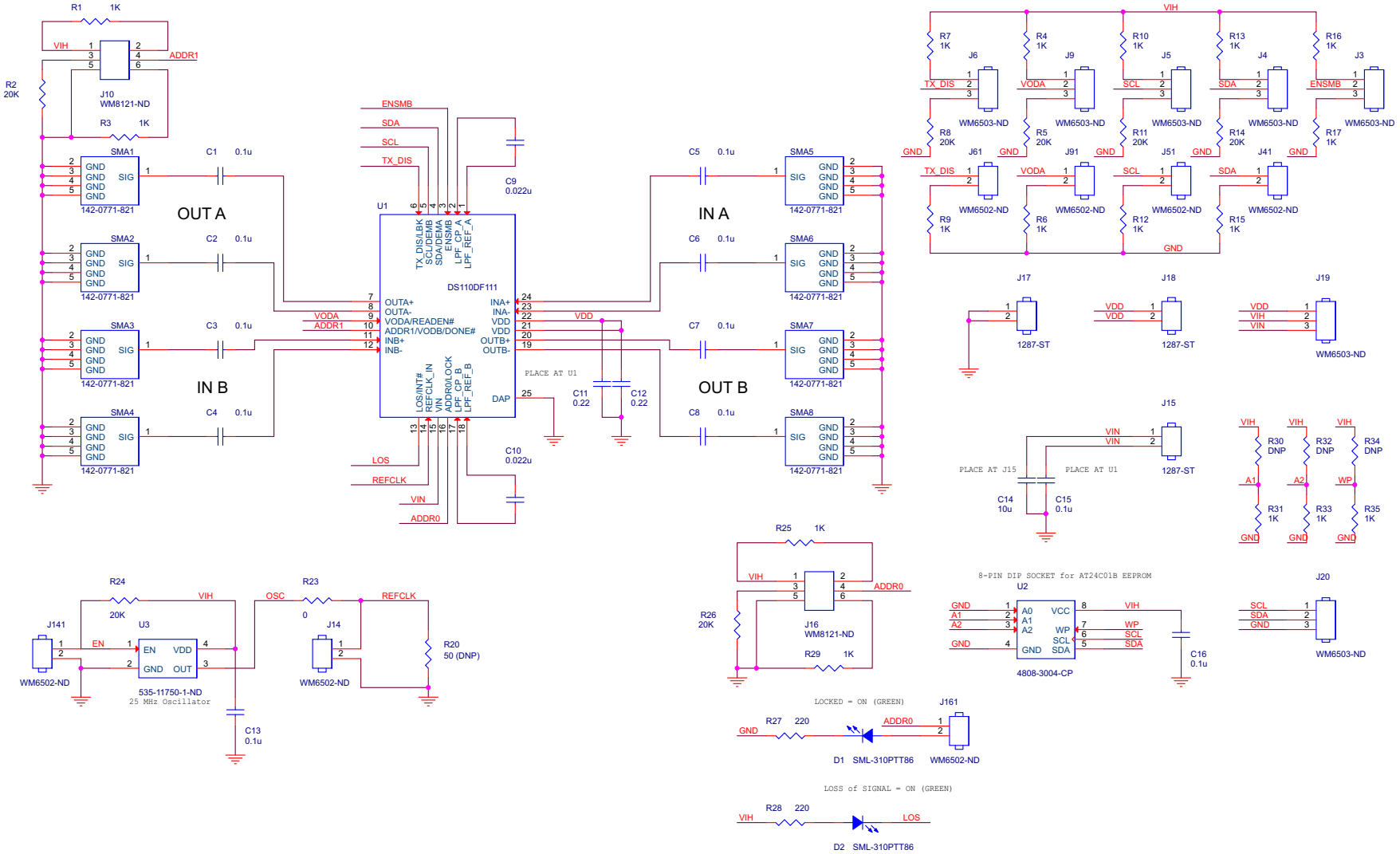


Figure 10. Bottom Assembly Layer

7 Schematic



8 Bill of Materials

COUNT	REF DES	DESCRIPTION	SIZE	MFR	PART NUMBER
11	C1, C2, C3, C4, C5, C6, C7, C8, C13, C15, C16	CAP CERAMIC .10UF 10V X5R	0201	Taiyo Yuden	LMK063BJ104KP-F
2	C9, C10	CAP CERAMIC .022UF 6.3V X5R	0201	TDK	C0603X5R0J223K030BC
2	C11, C12	CAP CERAMIC .22UF 6.3V X5R	0201	Taiyo Yuden	LMK063BJ224MP-F
1	C14	CAP CERAMIC 10UF 6.3V X5R	0603	TDK	C1608X5R0J106M080AB
2	D1, D2	GRN LED	0603	Rohm	SML-310PTT86
8	SMA1,SMA2, SMA3,SMA4, SMA5,SMA6, SMA7,SMA8	CONN JACK SMA 50 OHMS PC MOUNT		Emerson	142-0761-881
3	J15, J17, J18	TERM QF .052"DIA .250" STURDY MT		Keystone	1287-ST
7	J3, J4, J5, J6, J9, J19, J20	CONN HEADER 3-POS 0.100 VERT GOLD		Molex	WM50016-03-ND
7	J14, J41, J51, J61, J91, J141, J161	CONN HEADER 2-POS 0.100 VERT GOLD		Molex	WM50016-02-ND
2	J10, J16	CONN HEADER 6-POS 0.100 VERT GOLD		Molex	WM8121-ND
17	R1, R3, R4, R6, R7, R9, R10, R12, R13, R15, R16, R17, R25, R29, R31, R33, R35	RES 1.0K OHM 1/10W 5%	0402	Rohm	MCR01MZPJ102
7	R2, R5, R8, R11, R14, R24, R26	RES 20.0K OHM 1/10W 1%	0402	Panasonic	ERJ-2GEJ203X
1	R23	RES 0.0 OHM 1/10W 5%	0402	Panasonic	ERJ-2GE0R00X
2	R27, R28	RES 220 OHM 1/10W 5%	0402	Rohm	MCR01MZPJ221
1	U1	DS110DF111SQ (24-QFN - 4x4mm, 0.5mm pitch)		TI	DS110DF111SQ
1	U2	SOCKET IC OPEN FRAME 8-POS 0.3"		3M	4808-3004-CP
1	U3	OSC MEMS 25.000 MHZ SMD		Abracon Corporation	ASEMB-25.000MHZ-LC-T
1	R20	(DNP) RES 50 OHM	0402	Rohm	MCR01MZPF49R9
3	R30, R32, R34	(DNP) RES 1K OHM	0402	Rohm	MCR01MZPJ102
1	-	PCB, 0.062 inch		Any	DS110DF111EVM, Rev 1

9 Example Waveforms

With the default power up configuration, the DS110DF111 is designed to LOCK to 10.3125 Gbps or 1.25 Gbps encoded data. The results in Figure 11 and Figure 12 are typical when measured and observed via test equipment attached to the EVM with matched SMA coaxial cables.

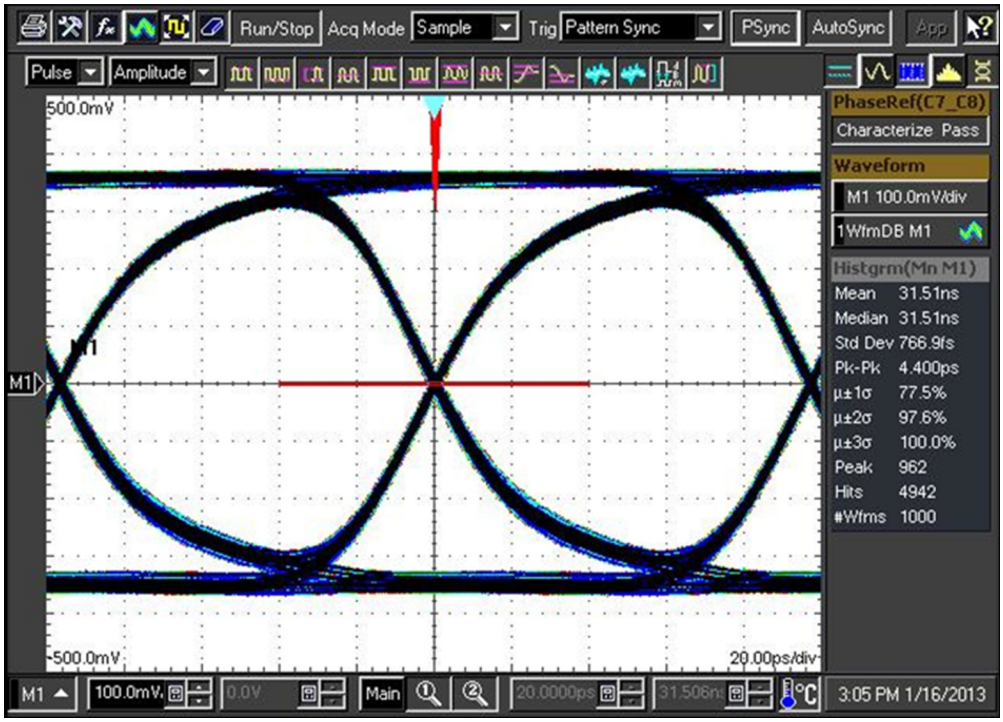


Figure 11. 10.3125 Gbps Output Waveform

Data Source: MATH1	Data Rate: 10.3125 Gbps	Filter: False
SSC: Off	Pattern: 127 bits	Channel: False
Phase Reference: 10.3125 GHz	Sample Count: 52.70 k	Equalizer: None

Jitter (Decision Threshold: 4.55 mV)			**Noise** (Sampling Phase: 0 UI)		
Random Jitter			**Random Noise**		
RJ (RMS)	=	323.07 fs	RN (RMS)	=	874.00 uV
RJ(h) (RMS)	=	317.70 fs	RN(v) (RMS)	=	873.98 uV
RJ(v) (RMS)	=	58.65 fs	RN(h) (RMS)	=	6.24 uV
Deterministic Jitter			**Deterministic Noise**		
DJ	=	3.82 ps	DN	=	80.04 mV
DDJ	=	2.43 ps	DDN	=	78.79 mV
DCD	=	712.28 fs	DDN(level 1)	=	72.46 mV
DDPWS	=	2.15 ps	DDN(level 0)	=	85.54 mV
PJ	=	580.52 fs	PN	=	1.48 mV
PJ(h)	=	572.01 fs	PN(v)	=	1.48 mV
PJ(v)	=	99.06 fs	PN(h)	=	11.23 uV
Total Jitter @ BER			**Total Noise @ BER**		
TJ (1E-12)	=	7.52 ps	TN (1E-12)	=	100.44 mV
Eye Opening (1E-12)	=	89.44 ps	Eye Opening (1E-12)	=	559.04 mV
			Eye Amplitude	=	659.48 mV
Dual Dirac			**SSC Modulation**		
RJ(d-d)	=	366.18 fs	Magnitude	=	0 ppm
DJ(d-d)	=	2.36 ps	Frequency	=	0 Hz

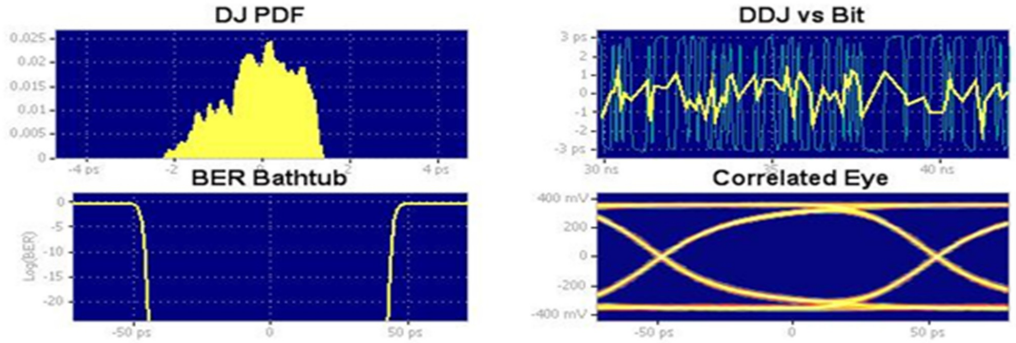


Figure 12. 10.3125 Gbps RjDj Jitter Decomposition

Revision History

Changes from Original (May 2014) to A Revision **Page**

- Added Features, Applications, and Ordering Information contents 5
- Changed source formatting of Pin Control descriptions 6
- Deleted DS110DF111 pin map from "Pin Control Mode Configuration" subsection 7
- Changed connection to reflect operation with SigCon Architect through the DPS-DONGLE-EVM adapter board 9
- Added new subsections for register archtiecture and SigCon Architect basics 10
- Added detailed description about operation in EEPROM mode 12
- Changed display format of EVM layout 13

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms and conditions that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.

   2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY WRITTEN DESIGN MATERIALS PROVIDED WITH THE EVM (AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

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7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS AND CONDITIONS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

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9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

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