DS160PR410 Programming Guide

This document provides a programming reference for the DS160PR410 Quad-Channel PCI-Express Gen-4 Linear Redriver. It contains detailed information related to the DS160PR410 advanced configuration options. The intended audience includes software engineers working on system diagnostics and control software.

TI recommends that the reader be familiar with the DS160PR410 data sheet (SNLS645). This document and all other collateral data related to the DS160PR410 redriver (application notes, models, and so forth) are available to download from the TI website. Alternatively, contact your local Texas Instruments field sales representative.

Topic **Page**

1 Access Methods

There are two ways the designer can access the DS160PR410. The methods are:

- Register control through the Serial Management Bus (SMBus)
- Automatic configuration through an external EEPROM

In a typical system, SMBus access is used to configure the device and monitor the device status. An EEPROM can also be used to configure the device initially, with the SMBus used to monitor its status. Rarely is the EEPROM method used without using the SMBus to monitor the device status.

1.1 Register Programming Through SMBus

The DS160PR410 internal registers can be accessed through standard SMBus protocol. The SMBus slave address is determined at power up based on the configuration of the EQ1_ADDR1 and EQ0_ADDR0 pins. The pin state is read on power up, after the internal power-on reset signal is deasserted.

The EQ1_ADDR1 and EQ0_ADDR0 pins along with GAIN, VOD, EN_SMB, and RX_DET pins are 4-level input pins that are used to control the configuration of the device. These 4-level inputs use a resistor divider to help set the four valid levels as shown in Table 1.

Table 1. DS160PR410 4-Level Control Pin Settings

Pin Level	Pin Setting
L0	1 kΩ to GND
L1	13 kΩ to GND
L2	Float
L3	59 kΩ to GND

There are 16 unique SMBus slave addresses that can be assigned to the device by placing external resistor straps on the EQ0_ADDR0 and EQ1_ADDR1 pins as shown in Table 2. When multiple DS160PR410 devices are on the same SMBus interface bus, each device must be configured with a unique SMBus slave address.

Table 2. DS160PR410 SMBus Address Map

EQ1_ADDR1 Pin Level	EQ0_ADDR0 Pin Level	7-Bit Address [HEX]	8-Bit Write Address [HEX]
L0	L0	0x18	0x30
L0	L1	0x19	0x32
L0	L2	0x1A	0x34
L0	L3	0x1B	0x36
L1	L0	0x1C	0x38
L1	L1	0x1D	0x3A
L1	L2	0x1E	0x3C
L1	L3	0x1F	0x3E
L2	L0	0x20	0x40
L2	L1	0x21	0x42
L2	L2	0x22	0x44
L2	L3	0x23	0x46
L3	L0	0x24	0x48
L3	L1	0x25	0x4A
L3	L2	0x26	0x4C
L3	L3	0x27	0x4E

1.2 Device Configuration Through External EEPROM

The DS160PR410 can automatically read its initial configuration from the EEPROM at power up. Many of the key configuration bits in the register map are mapped to the EEPROM, as indicated by the “EEPROM” column in the register map. Detailed information on EEPROM hex file generation for this device is provided in the *Understanding EEPROM Programming for DS160PR410 PCI-Express Gen-4 Redriver* application report (SNLA320).

2 Register Types

The DS160PR410 has two types of registers:

- **Share Registers** – These registers can be accessed at any time and are used to select individual channel registers, device-level configuration, status read back, control, or to read back the device ID information.
- **Channel Registers** – These registers are used to control and configure specific features for each individual channel. All channels have the same channel register set and can be configured independent of each other.

2.1 Channel Control Share Registers

There are two share registers for the DS160PR410 channel control:

- **0xFC** – This registers is used for channel selection.
- **0xFF** – This register is used to select between the channel and share register sets. This register can also be used to enable broadcast writes to quickly configure settings that are common to all channels.

Register 0xFC is used to select which channel register sets are later written to. To select a channel register set, write a 1 to its corresponding bit in this global register. Note that more than one channel may be written to by setting multiple bits in register 0xFC. When performing an SMBus read transaction, however, only one channel can be selected at a time. If multiple channels are selected when attempting to perform an SMBus read, the device will return 0xFF. This functionality is important to note when using read-modify-write transactions.

Table 3. Channel Select Control Register Definition

Global Register	Bit	Description
0xFC	7	Reserved
	6	Reserved
	5	Reserved
	4	Reserved
	3	Select register set for channel 3.
	2	Select register set for channel 2.
	1	Select register set for channel 1.
	0	Select register set for channel 0.

Register 0xFF bit 0 is used to select the Channel Register Page for the channels selected in Register 0xFC.

Table 4. Register Page Select Register Definition

Global Register	Bit	Description
0xFF	7:2	Reserved
	1	1: Broadcast write to all channels, 0xFF [0] must be set to 1. Select a single channel in 0xFC. 0: Normal operation, select channel register as defined in 0xFC.
	0	1: Select Channel Registers. 0: Deselect Channel Registers. Select Share Register Page.

3 Example Programming Sequences

The DS160PR410 is highly programmable and customizable for multiple applications. The following sections provide guidance for programming the DS160PR410 for certain common applications.

The following information is provided in each sequence:

- **Step**: Many sequences contain several steps. The order in which actions are to be taken is indicated by the step number.
- **Register Type**: Actions are intended for either the Shared or Channel register. For channel register actions, it is necessary to select the target channel first.
- **Operation**: Read or Write. If it is a Read operation, a register value or write mask is not associated.
- **Register Address**: Select the register to write to.
- **Register Value**: Value to write to register address.
- **Write Mask**: Unless the write mask is 0xFF, all writes should be performed as a read/modify/write operation. Only the bits identified by the mask should be modified.

3.1 Single Channel Write Selection

Select a specific channel as the target for subsequent channel register accesses.

Table 5. Sequence to Select a Target Channel

Step	Register Set	Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]	Comment
1	Share	Write	0xFF	0x01	0x01	Enables Channel Register Page access
2	Share	Write	0xFC	0x08	0xFF	Select register set for channel 3
				0x04	0xFF	Select register set for channel 2
				0x02	0xFF	Select register set for channel 1
				0x01	0xFF	Select register set for channel 0

3.2 Broadcast Write Selection

Register 0xFF[1] is used to perform broadcast register writes to all channels. Users can perform single-channel read-modify-broadcast-write commands by setting register 0xFF to 0x03 and selecting a single channel in the 0xFC register. All reads will be from the channel selected in register 0xFC. If more than one channel is selected in register 0xFC, then reads are invalid.

Table 6 shows how to configure the device to read back values from Channel 0 and then broadcast write to all channels. TI highly recommends to select only one channel for read back when simultaneously enabling broadcast writes.

Table 6. Sequence to Implement a Broadcast Write

Step	Register Set	Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]	Comment
1	Share	Write	0xFF	0x03	0xFF	Enable Channel Register Page access and broadcast mode.
2	Share	Write	0xFC	0x01	0xFF	Select only register set channel 0 for read back.

3.3 Set CTLE Gain Level

The DS160PR410 requires manual CTLE tuning. The CTLE gain level can be changed by modifying the value of each CTLE stage (EQ1 and EQ2) or by bypassing the EQ1 stage. The CTLE level may be set individually for each channel or broadcast to all channels. Table 7 shows an example sequence to set the CTLE gain level to 5.7 dB at 8 GHz (CTLE Index 2: EQ1 = 001'b; EQ2 = 000'b).

Table 7. Sequence to Set CTLE Level

Step	Register Set	Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]	Comment
1	Share	Write	0xFF	0x03	0xFF	Select channel registers and enable broadcast write to all channels.
2	Share	Write	0xFC	0x01	0xFF	Select only register set channel 0 for read back.
3	Channel	Write	0x04	0x00	0x01	Disable EQ1 bypass.
4	Channel	Write	0x03	0x01	0x07	Set EQ1 to Index 1.
5	Channel	Write	0x03	0x00	0x38	Set EQ2 to Index 0.

Table 8 gives a sub-sequence (Steps 3 - 5) to set a range of CTLE gain levels (CTLE Index 0 - 15). The sub-sequence should be preceded with the steps 1 and 2 as described in Table 7.

Table 8. Sub-Sequence to Set CTLE Level as a Function of CTLE Index

CTLE Index	CTLE Gain at 4 GHz (dB)	CTLE Gain at 8 GHz (dB)	Step / Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]
0	-0.3	-0.8	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x01 0x00 0x00	0x01 0x07 0x38
1	0.4	1.3	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x01 0x00 0x18	0x01 0x07 0x38
2	3.3	5.7	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x01 0x00	0x01 0x07 0x38
3	3.8	7.1	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x01 0x10	0x01 0x07 0x38
4	4.9	8.4	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x02 0x08	0x01 0x07 0x38
5	5.2	9.1	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x02 0x10	0x01 0x07 0x38
6	5.4	9.8	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x02 0x18	0x01 0x07 0x38
7	6.5	10.7	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x03 0x10	0x01 0x07 0x38
8	6.7	11.3	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x03 0x18	0x01 0x07 0x38
9	7.7	12.6	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x04 0x18	0x01 0x07 0x38
10	8.7	13.6	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x05 0x18	0x01 0x07 0x38
11	9.1	14.4	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x05 0x20	0x01 0x07 0x38
12	9.4	15.0	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x05 0x28	0x01 0x07 0x38
13	10.3	15.9	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x06 0x28	0x01 0x07 0x38
14	10.6	16.5	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x06 0x30	0x01 0x07 0x38
15	11.8	17.8	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x07 0x38	0x01 0x07 0x38

Table 9 gives a sub-sequence (Steps 3 - 5) to set a range of CTLE gain levels with finer steps (CTLE Fine Index 0 - 29). The sub-sequence should be preceded with the steps 1 and 2 as described in Table 7.

Table 9. Sub-Sequence to Set CTLE Level as a Function of CTLE Fine Index

CTLE Fine Index	CTLE Gain at 4 GHz (dB)	CTLE Gain at 8 GHz (dB)	Step / Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]
0	0.1	0.6	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x01 0x00 0x10	0x01 0x07 0x38
1	0.4	1.3	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x01 0x00 0x18	0x01 0x07 0x38
2	0.8	2.0	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x01 0x00 0x20	0x01 0x07 0x38
3	1.0	2.6	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x01 0x00 0x28	0x01 0x07 0x38
4	1.4	3.2	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x01 0x00 0x30	0x01 0x07 0x38
5	1.7	3.7	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x01 0x00 0x38	0x01 0x07 0x38
6	2.1	4.5	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x00 0x10	0x01 0x07 0x38
7	2.3	5.2	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x00 0x18	0x01 0x07 0x38
8	2.7	6.0	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x00 0x20	0x01 0x07 0x38
9	3.5	6.3	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x01 0x08	0x01 0x07 0x38
10	3.8	7.1	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x01 0x10	0x01 0x07 0x38
11	4.0	7.7	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x01 0x18	0x01 0x07 0x38
12	4.4	8.5	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x01 0x20	0x01 0x07 0x38
13	5.2	9.1	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x02 0x10	0x01 0x07 0x38
14	5.4	9.8	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x02 0x18	0x01 0x07 0x38
15	5.8	10.5	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x02 0x20	0x01 0x07 0x38
16	6.5	10.7	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x03 0x10	0x01 0x07 0x38
17	6.7	11.3	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x03 0x18	0x01 0x07 0x38

Table 9. Sub-Sequence to Set CTLE Level as a Function of CTLE Fine Index (continued)

CTLE Fine Index	CTLE Gain at 4 GHz (dB)	CTLE Gain at 8 GHz (dB)	Step / Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]
18	7.4	11.9	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x04 0x10	0x01 0x07 0x38
19	7.7	12.6	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x04 0x18	0x01 0x07 0x38
20	8.4	12.9	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x05 0x10	0x01 0x07 0x38
21	8.7	13.6	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x05 0x18	0x01 0x07 0x38
22	9.1	14.4	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x05 0x20	0x01 0x07 0x38
23	9.4	15.0	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x05 0x28	0x01 0x07 0x38
24	9.7	15.5	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x05 0x30	0x01 0x07 0x38
25	10.3	15.9	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x06 0x28	0x01 0x07 0x38
26	10.6	16.5	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x06 0x30	0x01 0x07 0x38
27	10.9	17.0	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x06 0x38	0x01 0x07 0x38
28	11.4	17.2	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x07 0x30	0x01 0x07 0x38
29	11.8	17.8	3 / Write 4 / Write 5 / Write	0x04 0x03 0x03	0x00 0x07 0x38	0x01 0x07 0x38

3.4 Set CTLE DC Gain Level

The CTLE DC Gain value may be set individually for each channel or broadcast to all channels.

Table 10. Sequence to Set DC Gain Level

Step	Register Set	Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]	Comment
1	Share	Write	0xFF	0x03	0xFF	Select channel registers and enable broadcast write to all channels.
2	Share	Write	0xFC	0x01	0xFF	Select only register set channel 0 for read back.
3	Channel	Write	0x04	0x00	0x20	Set DC Gain to: 0 dB (Default)
				0x80	0xC0	Set DC Gain to: 3.5 dB

3.5 Set VOD Level

The DS160PR410 driver differential output voltage can be modified, if needed.

Table 11. Sequence to Set VOD Level

Step	Register Set	Operation	Register Address [HEX]	Register Value [HEX]	Write Mask [HEX]	Comment
1	Share	Write	0xFF	0x03	0xFF	Select channel registers and enable broadcast write to all channels.
2	Share	Write	0xFC	0x01	0xFF	Select only register set channel 0 for read back.
3	Channel	Write	0x06	0x00	0xC0	Set VOD to: -6 dB
				0x40	0xC0	Set VOD to: -3.5 dB
				0x80	0xC0	Set VOD to: -1.6 dB
				0xC0	0xC0	Set VOD to: 0 dB (Default)

4 Share Registers

Table 12 lists the Share registers. All register offset addresses not listed in Table 12 should be considered as reserved locations and the register contents should not be modified.

Table 12. Share Registers

Address	Acronym	Register Name	Section
0x4	General_1		Go
0xB	EE_Status		Go
0xF1	Full_Device_ID		Go
0xFC	Channel_Control_1		Go
0xFF	Channel_Control_2		Go

Complex bit access types are encoded to fit into small table cells. Table 13 shows the codes that are used for access types in this section.

Table 13. Share Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
WSC	WSC	Write / Self-Clearing
Reset or Default Value		
-n		Value after reset or the default value

4.1 General_2 Register (Address = 0x4) [reset = 0x1]

General_2 is shown in Table 14.

Return to the Summary Table.

Table 14. General_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	1b0	Reserved
6	rst_i2c_regs	R/W	1b0	Device Reset Control: Reset all I2C registers to default values (self-clearing).
5	rst_i2c_mas	R/WSC	1b0	Reset I2C master (self-clearing).
4 - 0	RESERVED	R/W	1b0001	Reserved

4.2 EE_Status Register (Address = 0xB) [reset = 0x0]

EE_Status is shown in Table 15.

Return to the Summary Table.

Table 15. EE_Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	eecfg_cmplt	R	1b0	EEPROM Load Status: 11: Not valid 10: EEPROM load completed successfully 01: EEPROM load failed after 64 attempts 00: EEPROM load in progress
6	eecfg_fail	R	1b0	
5	eecfg_atmpt_5	R	1b0	Number of attempts made to load EEPROM image.
4	eecfg_atmpt_4	R	1b0	
3	eecfg_atmpt_3	R	1b0	
2	eecfg_atmpt_2	R	1b0	
1	eecfg_atmpt_1	R	1b0	
0	eecfg_atmpt_0	R	1b0	

4.3 Full_Device_ID Register (Address = 0xF1) [reset = 0x26]

Full_Device_ID is shown in Table 16.

Return to the Summary Table.

Table 16. Full_Device_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DEVICE_ID_7	R	1b0	Device ID: 0010 0110: DS160PR410
6	DEVICE_ID_6	R	1b0	
5	DEVICE_ID_5	R	1b1	
4	DEVICE_ID_4	R	1b0	
3	DEVICE_ID_3	R	1b0	
2	DEVICE_ID_2	R	1b1	
1	DEVICE_ID_1	R	1b1	
0	DEVICE_ID_0	R	1b0	

4.4 Channel_Control_1 Register (Address = 0xFC) [reset = 0x0]

Channel_Control_1 is shown in Table 17.

Return to the Summary Table.

Table 17. Channel_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 4	RESERVED	R/W	1b0000	Reserved
3	en_q0c3	R/W	1b0	Enable Channel 3 register access
2	en_q0c2	R/W	1b0	Enable Channel 2 register access
1	en_q0c2	R/W	1b0	Enable Channel 1 register access
0	en_q0c2	R/W	1b0	Enable Channel 0 register access

4.5 Channel_Control_2 Register (Address = 0xFF) [reset = 0x0]

Channel_Control_2 is shown in Table 18.

Return to the Summary Table.

Table 18. Channel_Control_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 2	RESERVED	R/W	1b0000000	Reserved
1	write_all_ch	R/W	1b0	Enable Broadcast Write: 0: Broadcast write disabled 1: Broadcast write enabled Set en_ch_SMB (Reg 0xFF[0]) = 1 to use this function. Otherwise, the write_all_ch bit is invalid. Read-back will only occur based on the selected channel register page in Reg 0xFC.
0	en_ch_SMB	R/W	1b0	Register Access Control: 1: Enable register access to one of the channels specified in Reg 0xFC[3:0]. 0: Enable Share register access.

5 Channel Registers

Table 19 lists the Channel registers. All register offset addresses not listed in Table 19 should be considered as reserved locations and the register contents should not be modified.

Table 19. Channel Registers

Address	Acronym	Register Name	Section
0x0	reg_00		Go
0x1	reg_01		Go
0x3	reg_03		Go
0x4	reg_04		Go
0x6	reg_06		Go
0xD	reg_0D		Go

Complex bit access types are encoded to fit into small table cells. Table 20 shows the codes that are used for access types in this section.

Table 20. Channel Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

5.1 *reg_00 Register (Address = 0x0) [reset = 0x0]*

reg_00 is shown in Table 21.

Return to the Summary Table.

Table 21. reg_00 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 3	RESERVED	R/W	1b00000	Reserved
2	rst_regs	R/W	1b0	Channel Reset Control: Reset channel registers to default values (self-clearing)
1 - 0	RESERVED	R/W	1b00	Reserved

5.2 reg_01 Register (Address = 0x1) [reset = 0x0]

reg_01 is shown in Table 22.

Return to the Summary Table.

Table 22. reg_01 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	rx_det_comp_p	R	1b0	Rx Detect Positive Polarity Status: 0: Not detected 1: Detected The value is latched.
6	rx_det_comp_n	R	1b0	Rx Detect Negative Polarity Status: 0: Not detected 1: Detected The value is latched.
5 - 0	RESERVED	R	1b000000	Reserved

5.3 reg_03 Register (Address = 0x3) [reset = 0x80]

reg_03 is shown in Table 23.

Return to the Summary Table.

Table 23. reg_03 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	eq_bw_1	R/W	1b1	CTLE Bandwidth Control: 00: Lowest 01: Intermediate 10: Recommended 11: Highest
6	eq_bw_0	R/W	1b0	See MSB
5	eq_bst2_2	R/W	1b0	CTLE Boost Stage 2 Control.
4	eq_bst2_1	R/W	1b0	See MSB
3	eq_bst2_0	R/W	1b0	See MSB
2	eq_bst1_2	R/W	1b0	CTLE Boost Stage 1 Control.
1	eq_bst1_1	R/W	1b0	See MSB
0	eq_bst1_0	R/W	1b0	See MSB

5.4 reg_04 Register (Address = 0x4) [reset = 0x16]

reg_04 is shown in Table 24.

Return to the Summary Table.

Table 24. reg_04 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	1b0	Reserved
6	eq_term_en	R/W	1b0	Enable CTLE Termination (active if reg_06[5]=1)
5	eq_hi_gain	R/W	1b0	Set CTLE DC Gain: 0: 0 dB (Recommended) 1: 3.5 dB
4	eq_en_dc_off	R/W	1b1	Enable CTLE DC Offset Correction: 0: DC offset correction disabled 1: DC offset correction enabled (recommended)
3	eq_en	R/W	1b0	Enable CTLE (active if reg_06[5]=1)
2 - 1	RESERVED	R/W	1b11	Reserved
0	eq_en_bypass	R/W	1b0	Enable CTLE Stage 1 Bypass: 0: Bypass disabled 1: Bypass enabled

5.5 reg_06 Register (Address = 0x6) [reset = 0xC0]

reg_06 is shown in Table 25.

Return to the Summary Table.

Table 25. reg_06 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	drv_sel_vod_1	R/W	1b1	TX VOD Select: 00: - 6 dB 01: -3.5 dB 10: -1.6 dB 11: 0 dB (Recommended)
6	drv_sel_vod_0	R/W	1b1	See MSB
5	drv_eq_en_override	R/W	1b0	Enable overrides for driver and equalizer enables.
4	drv_en_pre	R/W	1b0	Enable Pre-driver. (active if reg_06[5]=1)
3	drv_en	R/W	1b0	Enable Driver. (active if reg_06[5]=1)
2	drv_en_cm_loop	R/W	1b0	Enable CM Loop. (active if reg_06[5]=1)
1 - 0	RESERVED	R/W	1b00	Reserved

5.6 reg_0D Register (Address = 0xD) [reset = 0x0]

reg_0D is shown in Table 26.

Return to the Summary Table.

Table 26. reg_0D Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	1b0	Reserved
6	mr_rx_det_man	R/W	1b0	Manual override of rx_detect_p/n decision to always return valid.
5	en_rx_det_count	R/W	1b0	Enable RX detect valid counter
4	sel_rx_det_count	R/W	1b0	Select valid RX detect count before enable 0: 2x consecutive valid detections 1: 3x consecutive valid detections
3	mr_rx_det_rst	R/W	1b0	RX Detect state machine reset
2 - 0	RESERVED	R/W	1b000	Reserved

6 References

1. Texas Instruments, *DS160PR410 4-Channel PCI-Express Gen-4 Linear Redriver* data sheet (SNLS645)
2. Texas Instruments, *Understanding EEPROM Programming for DS160PR410 PCI-Express Gen-4 Redriver* application report (SNLA320)

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