Application Report
SNOA491C–September 2007–Revised May 2013

AN-1639 LMP7300 Single Precision Comparator With Reference Evaluation Boards (SOIC and VSSOP)

ABSTRACT

The following evaluation boards are designed to demonstrate the LMP7300 micropower precision comparator, with precision voltage reference. Texas Instruments recommends the use of these boards as an aid in the evaluation and characterization of the LMP7300.

- -551013114 - For the LMP7300 MO8A Evaluation (SOIC pkg)
- -551013115 - For the LMP7300 MUA8A Evaluation (VSSOP pkg)

The boards have identical circuit configurations and layouts. All components are surface mount 0805 except the test points for supply and voltage measurement. The layout input and output will accommodate either BNC or SMA connectors.

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1 Basic Configuration as Threshold Detector

The LMP7300 evaluation boards are designed to provide maximum flexibility while investigating different circuit configurations. The values chosen are for micropower precision level threshold applications where supply noise is at a minimum. If supply noise is present, provision has been made to add decoupling as needed. While most component values are shown, some are application specific and should be defined by you. For example, the bridge gain can be changed with R1, R2, and R4, while supply line decoupling can be improved with C2 and C6. The potentiometers, R6 and R7, can be used to quickly trim the trip points.

As shown in Figure 1, the input signal, V_{IN}, is brought onto the board through a BNC or SMA connector and divided by the bridge gain. If the desired V_{IN} trigger level is set to twice V_{REF}, the comparator will trip around V_{REF}. The signal path is connected via jumper JP1 to the comparator's inverting input and JP2 for the non-inverting input. The bridge gain is set to ~ 1/2 with R1 and R2 both stuffed as 1 MΩ and R4 set to 0 Ω for initial setup, then trimmed for high or low threshold detection. There is a provision for a resistor R3 to be placed between the input pins for large hysteresis levels.

2 Hysteresis

The hysteresis for the LMP7300, unlike most comparators, is totally independent of the supply, the input conditions, or the output connections. The part design allows for five hysteresis settings: asymmetric, symmetric, positive only, negative only, or none. The hysteresis is easily determined by two resistors in a voltage divider format with the precision 2.048 V voltage reference tied to the top resistor and ground set to the bottom. The center voltage tap is connected to device pin HYSTP, or HYSTN to fix the hysteresis at 1 mV/mV. Trim potentiometers R6 and R7 are provided for quick and easy resolution of the proper hysteresis. Resistors R5 and R10 are set to 1 MΩ to establish ~2 µA current through the divider to ground. The hysteresis is the voltage measured across the trim potentiometer resistance or V_{REF} - the voltage at the voltage divider center tap. A maximum of 100 to 130 mV is recommended.

3 Reconfigure Application with Jumper Pins

- For negative threshold detection: The input signal V_{IN} is normally above the threshold, dropping below the threshold. Connect V_{IN} to the non-inverting input with JP2, and V_{REF} to the inverting input with JP3
- For positive threshold detection: The input signal V_{IN} is normally below the threshold, rising above the threshold. Connect V_{IN} to the inverting input with JP1, and V_{REF} to the non-inverting input with JP4.
- Use JP5 for split supply.
- Use JP6 for single supply.

4 Bypassing the Voltage Reference

In noisy supply line applications, bypassing the voltage reference to improve line regulation with respect to supply line transients is recommended. The reference output can drive a bypass capacitance of 0.05 µF, with minimum peaking and no oscillation. For larger capacitors, add a small value of resistance in series with the capacitor. A 190 Ω resistor in series with a 5 µF ceramic capacitor is recommended.

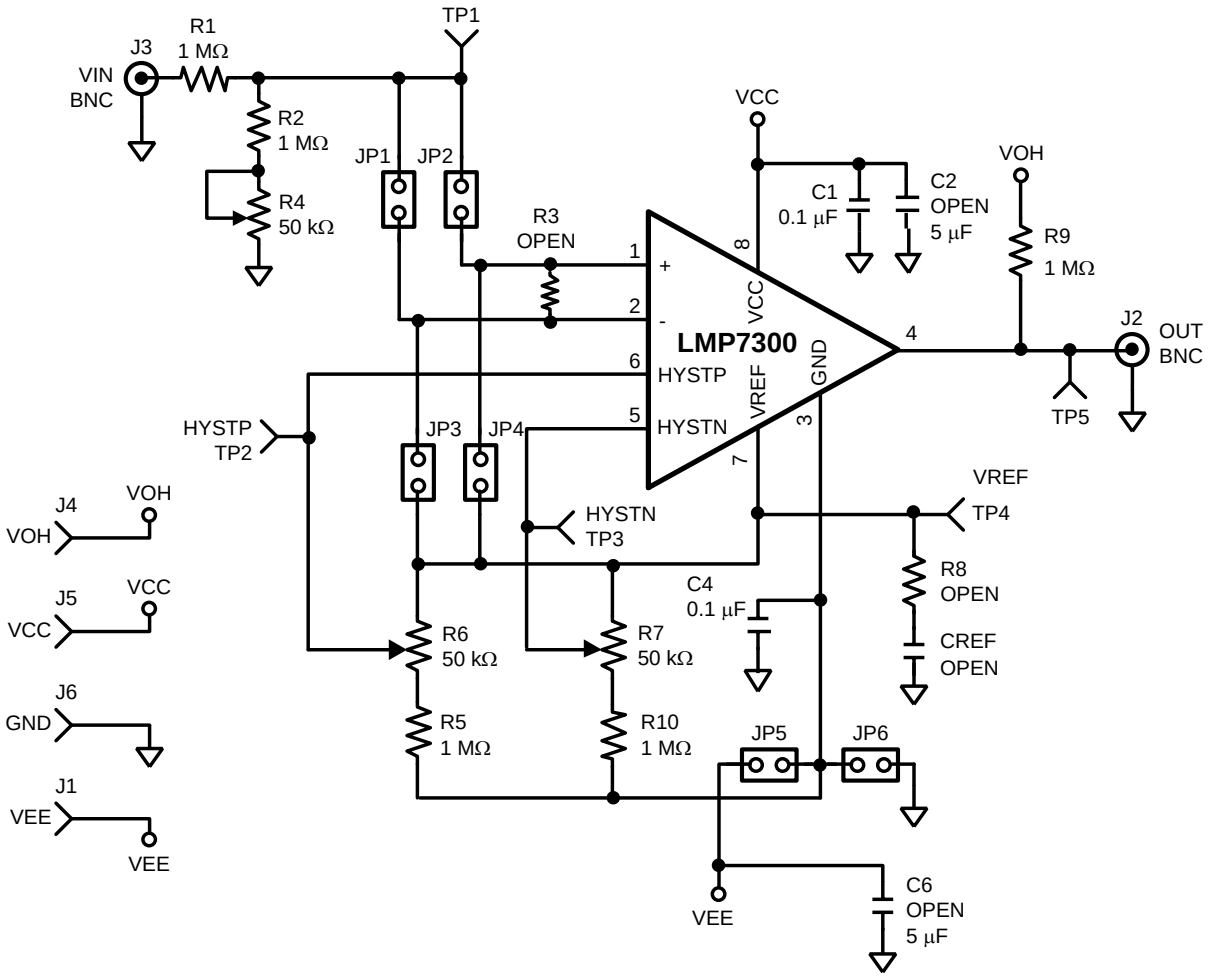

Figure 1. Evaluation Board Schematic

5 Output Stage

The comparator employs an open collector output stage that can drive both voltage and current loads, such as solenoids, lamps, heater, and so forth. Since the pull-up resistor can be taken to any voltage between 0.5 V and 12 V, independent of the comparator supply voltage, interfacing with mixed voltage systems is straight forward. The open collector design also permits wired-OR connection to the multiple comparator outputs. This output stage easily interfaces with various logic inputs, such as TTL and CMOS. When the positive input is above the negative input, the output is in an off or high state. The output voltage high level is determined by the pull-up supply. For the reverse condition, when the positive input is below the negative input, the output is in an on or low state. The maximum load current is around 10 mA for a low state.

Table 1. Bill of Materials (BOM)

ID	Part Number	Type	Size	Parameters	Qty	Vendor
U1	LMP7300	Comparator	8-Pin SOIC/VSSOP		1	TI
R8	P191CCT-ND	Resistor	805	190 Ω, 1%, 1/8W, Open	1	Digi-Key
R1, R2, R5, R9, R10	P100MCCT-ND	Resistor	805	1.00 MΩ, 1%, 1/8W	5	Digi-Key
R4, R6, R7	3299Y-503LF-ND	Potentiometer		50 kΩ, 1/2W	3	Digi-Key
JP1 - JP6	929450-01-36-ND	Header	2-pin, 0.1"		6	Digi-Key
C1, C4	PCC1828CT-ND	Capacitor	805	0.1 µF, X7R, 10%, 25 V	2	Digi-Key
C2, C6, CREF		Capacitor		5 µF, X7R, 10%, 25 V, Open	3	Digi-Key
J2,J3	22C4690	BNC		PCB Edge Mount	2	Newark
J1	5009K-ND	LG Test Point		Yellow	1	Digi-Key
J4	5007K-ND	LG Test Point		White	1	Digi-Key
J5	5005K-ND	LG Test Point		Red	1	Digi-Key
J6	5006K-ND	LG Test Point		Black	1	Digi-Key
TP1 – TP5	5004K-ND	Test Point		Black	5	Digi-Key
Jumper Shunt	5900D	Short	2 pin, 0.1”	0 Ω Black		Digi-Key

6 Connection Diagram

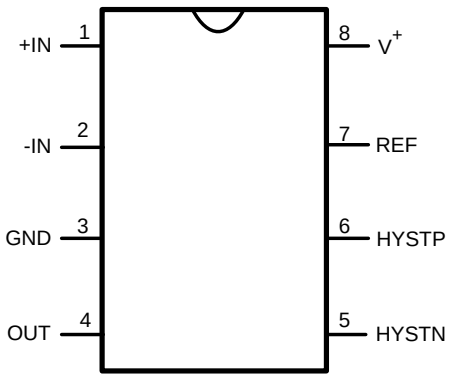

Figure 2. 8-Pin VSSOP/SOIC Top View

7 Pin Descriptions

Table 2. Pin Descriptions

+IN	Non-Inverting Comparator Input	The +IN has a common-mode voltage range from 1 V above the negative rail to, and including, the positive rail. Internal ESD diodes, connected from the +IN pin to the rails, protect the input stage from overvoltage. If the input voltage exceeds the rails, the diodes turn on and clamp the input to a safe level.
−IN	Inverting Comparator Input	The −IN has a common-mode voltage range from 1 V above the negative rail to, and including, the positive rail. Internal ESD diodes, connected from the −IN pin to the rails, protects the input stage from overvoltage. If the input voltage exceeds the rails, the diodes turn on and clamp the input to a safe level.
GND	Ground	This pin can be connected to a negative DC voltage source for applications requiring a dual supply. If connected to a negative supply, decouple this pin with 0.1 µF ceramic capacitor to ground. The internal reference output voltage is referenced to this pin. GND is the die substrate connection.
OUT	Comparator Output	The output is an open-collector. It can drive voltage loads by using a pullup resistor, drive current loads by sinking a maximum output current. This pin can be taken to maximum of +12 V with respect to the ground pin, irrespective of supply voltage.
HYSTN	Negative Hysteresis Pin	This pin sets the lower trip voltage V_{IL}. The common mode range is from 1 V above the negative rail to V_{CC}. The input signal must fall below V_{IL} for the comparator to switch from high to low state.
HYSTP	Positive Hysteresis pin	This pin sets the upper trip voltage V_{IH}. The common mode range is from 1 V above the negative rail to V_{CC}. The input signal must rise above V_{IH} for the comparator to switch from low to high state.
REF	Reference Voltage Output Pin	This is the output pin of a 2.048 V band gap precision reference.
V^+	Positive Supply Terminal	The supply voltage range is 2.7 V to 12 V. Decouple this pin with 0.1 µF ceramic capacitor to ground.

8 Board Layout

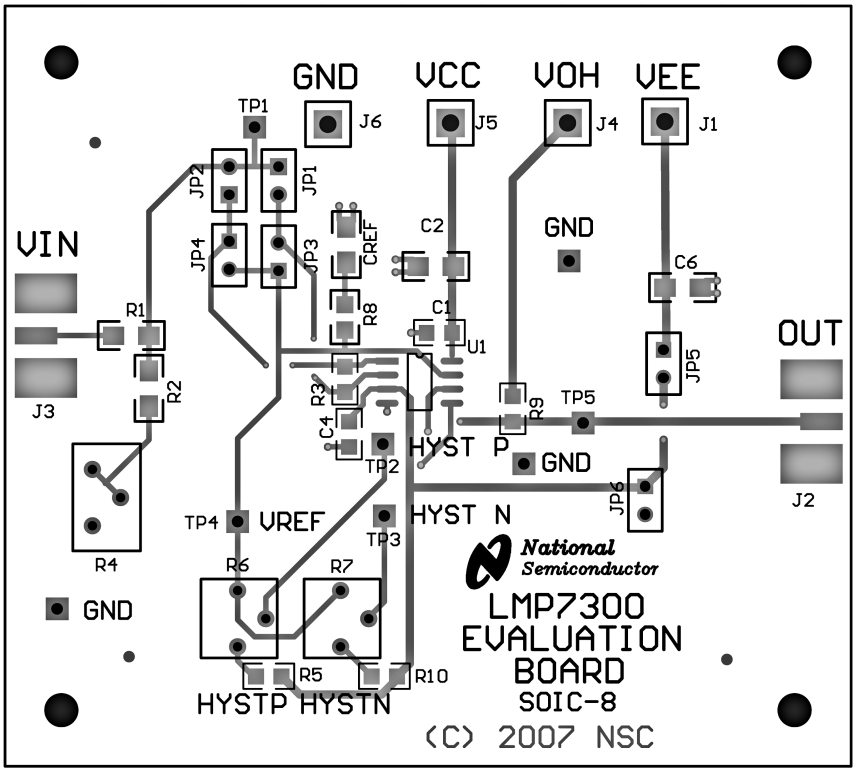

Figure 3. SOIC Top Layer

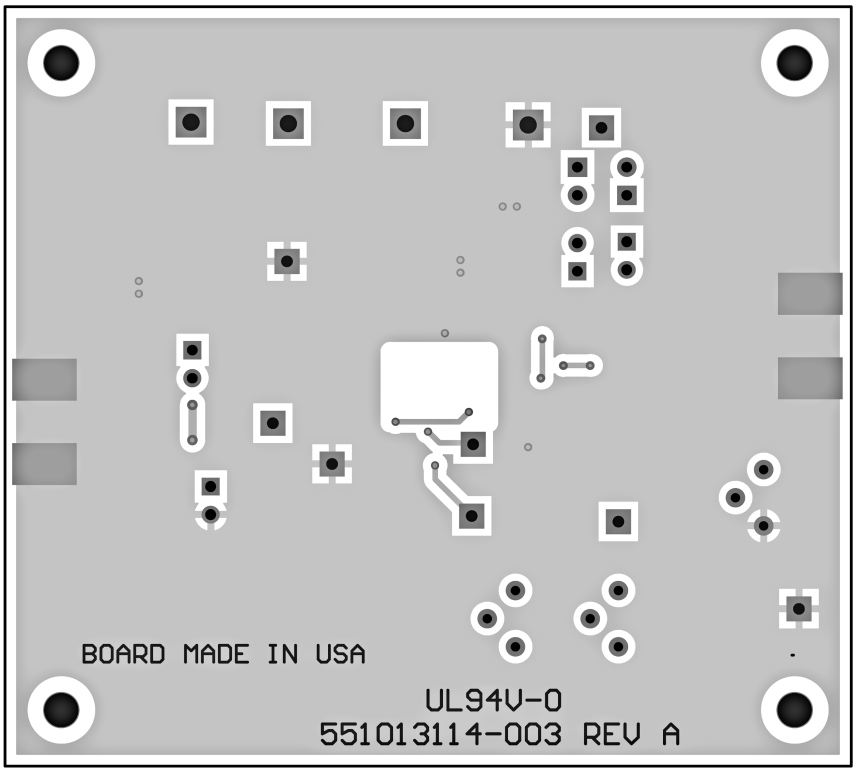

Figure 4. Bottom Layer

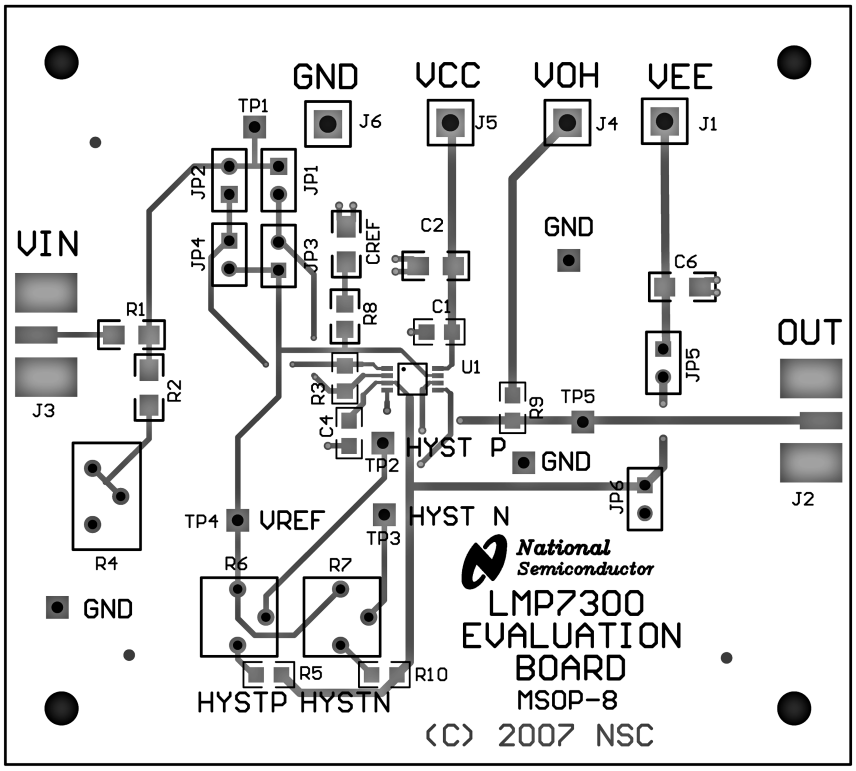

Figure 5. VSSOP Top Layer

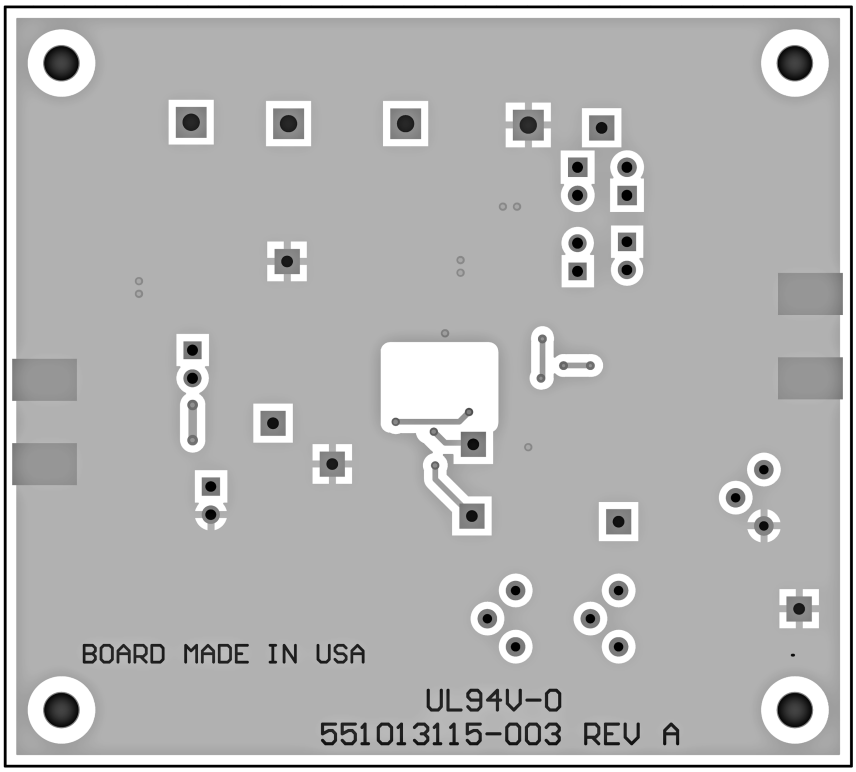

Figure 6. Bottom Layer

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