Application Note

How to Design a Boost Converter Using LM5123

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ABSTRACT

The LM5123 device is a wide input range, synchronous boost controller with envelope tracking capability. The device also integrates several features to meet system design requirements including precision enable, programmable UVLO, programmable soft-start, programmable switching frequency and adjustable control loop compensation. This application note details how to design a boost controller with a dynamically programmable output voltage. The results of this design are measured on the LM5123EVM-BST evaluation module and the results are presented in *LM5123EVM-BST User's Guide*. The basic concept and operation of a boost converter can be found in *Understanding Boost Power Stages in Switchmode Power Supplies*.

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1 Design Example

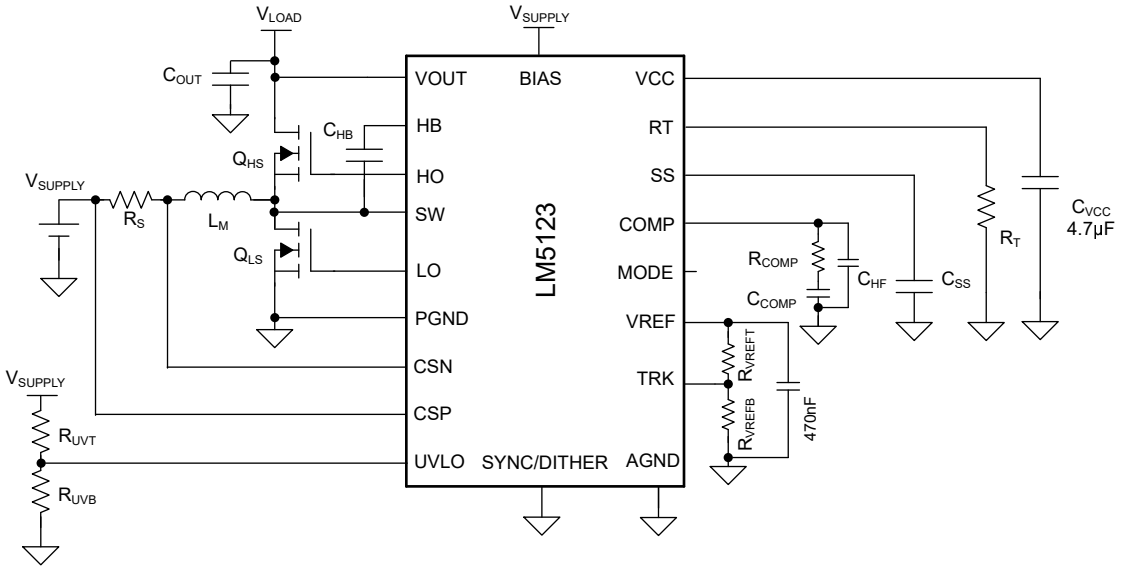

Figure 1-1. Typical Application

This design example produces a variable load voltage boost. Applications such as Class H audio amplifiers, and LED drivers require a variable output voltage from a boost regulator to greatly improve the system efficiency. The load voltage range for this design is 24 V to 33 V and provides a maximum power of 200 W from a standard 12 V automotive battery. The output voltage is adjusted using the TRK pin of the device. The detailed parameters are presented in Table 1-1 and the component selection is discussed in Section 2.

Table 1-1. Design Parameters

PARAMETER	Test Conditions		MIN	TYP	MAX	UNIT
INPUT VOLTAGE CHARACTERISITCS						
Input Voltage Range	Operation		8	14	18	V
	Input UVLO levels	Turn-off		5.2		V
		Turn-on		6.2		V
OUTPUT CHARACTERISITCS						
Load Voltage	VTRK = 400 mV ($V_{LOADmin}$)			24		V
	VTRK = 583 mV ($V_{LOADmax}$)			35		V
P_{OUTmax}	V_{SUPPLY}= 8 V to 18 V			200 W		W
SYSTEM CHARACTERISITCS						
f_{SW}				440		kHz

2 Calculations and Component Selection

The calculations specific to the LM5123 are provided to implement a boost converter operating in the continuous conduction mode (CCM) at full output power. The component calculations are based on the design parameters in Table 1-1. This procedure details how to design for a variable output voltage application, but are still valid for a fixed output voltage application. For a fixed output voltage design the $V_{LOADmin}$ parameter can be simply set equal to $V_{LOADmax}$.

2.1 Switching Frequency

With the given design parameters, selecting the proper switching frequency is an key step for any design. In general, a higher switching frequency yields a smaller solution size at the cost of a higher switching loss and lower efficiency. Therefore, the final selection of the switching frequency is a trade-off between the power density and efficiency based on the specific requirement of the application. Harmonics of the switching frequency should be considered in designs to strict EMC requirements. The required frequency set resistor for the internal oscillator is given in Equation 1.

$$R_T = \frac{2.21 \times 10^{10}}{f_{sw}} - 955 = \frac{2.21 \times 10^{10}}{440\text{KHz}} - 955 = 49.2\text{k}\Omega \quad (1)$$

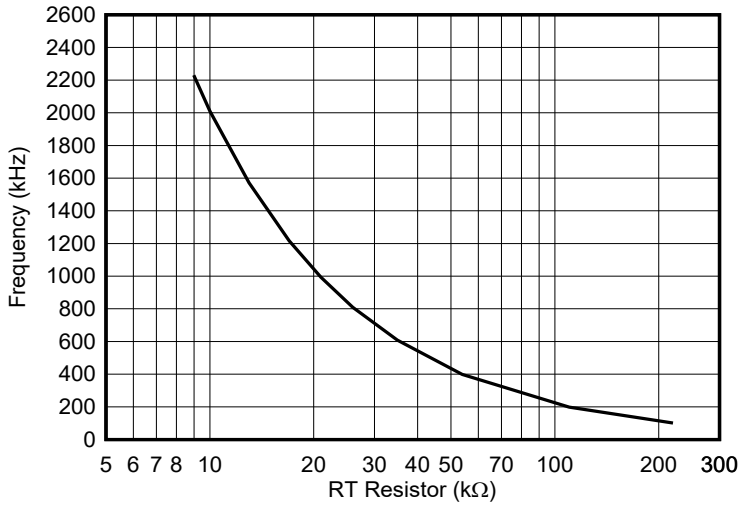

Figure 2-1. Frequency vs RT

The example application is selected to have a switching frequency of 440 kHz, and the standard value of 49.9kΩ with 1% tolerance is chosen for R_T. 440 kHz is selected as it provides a well balanced solutions between power density and efficiency and avoids the AM band (530 kHz to 1.8 MHz) where conducted emissions are greatly limited.

The internal oscillator of the device can be synchronized to an external clock as described in the data sheet. The LM5123 has a maximum duty cycle limit that is frequency dependent, which is also characterized in the data sheet.

2.2 Initial Inductor Calculation

The inductance value of the boost regulator is calculated with respect to the inductor current ripple ratio (RR). The ripple ratio is defined as the peak to peak ripple current over the average inductor current. In a boost topology the average inductor current is equal to the average input current. There are three main considerations guiding the selection of the inductance value: the inductor power loss, the falling slope of the inductor current and the right-half plane (RHP) zero frequency (ω_{Z_RHP}) of the control loop.

- As the inductance value increases the ripple ratio decreases so does inductor core loss and the RMS current but the losses due to the DCR of the inductor increase. Inductor selection effects the power losses of the regulator and should be considered to optimize the efficiency of the design.
- The inductance value should be large enough to prevent the sub-harmonic oscillation when they duty cycle is greater than approximately 50%. The LM5123 implements a fixed internal slope compensation of 45 mV

referenced to the current sense amplifier input. Additional slope compensation is required in peak current mode control architectures to prevent sub-harmonic oscillation.

- The RHP zero frequency is a limiting factor for the maximum control loop bandwidth. Therefore, the RHP zero frequency should be high enough to maximize the crossover frequency of the control loop. As the relative inductance value decreases the RHP zero frequency increases. Note, decreasing the inductance value increases the ripple ratio. As the relative control loop bandwidth increases the required output capacitance for a given load step reduces.

A maximum ripple ratio between 30% and 60% yields a balanced compromise among the above considerations. In this example, the maximum ripple ratio of the inductor current is selected to be 60%. The ripple ratio is calculated at the maximum output voltage ($V_{LOADmax}$) and maximum output power (P_{OUTmax}) to properly select the inductance value. In continuous conduction mode the duty cycle is estimated using Equation 2. The ripple ratio is calculated using Equation 3.

$$D = 1 - \frac{V_{SUPPLY}}{V_{LOAD}} \tag{2}$$

$$RR = \frac{{V_{SUPPLY}}^2 \cdot D}{I_{LOAD} \cdot L_M \cdot V_{LOAD} \cdot f_{SW}} \tag{3}$$

where

- V_{SUPPLY} is the voltage supplied to the input of the power stage
- V_{LOAD} is the target voltage regulation
- I_{LOAD} is the output current
- L_M is the magnetizing inductance of the inductor
- f_{SW} is the switching frequency

Locating the operating point at which the maximum ripple ratio is dependent on the duty cycle range. In CCM operation the maximum ripple ratio typically occurs at 33% duty cycle. When the duty cycle at the maximum input voltage is greater than 33% the maximum ripple ratio occurs at $V_{SUPPLYmax}$. When the duty cycle at the minimum input voltage is less than 33% the maximum ripple ratio occurs at $V_{SUPPLYmin}$.

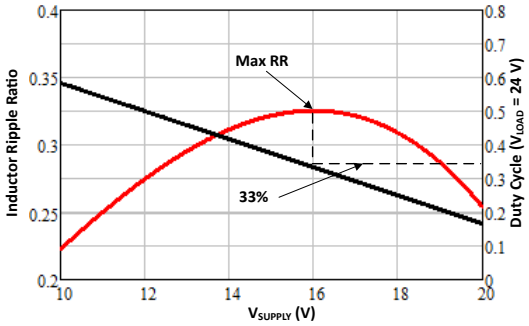

Figure 2-2. Ripple Ratio vs V_{SUPPLY}

Leveraging Equation 2, the duty cycle at the maximum input voltage is calculated to be 48.6% when the output voltage is set to $V_{LOADmax}$. The maximum ripple ratio occurs when V_{SUPPLY} is at the maximum specified value. If the design operates at 33% duty, Equation 4 is used to back calculate the supply voltage at given duty cycle.

$$V_{SUPPLY\_\Delta ILmax} = V_{LOAD} \cdot \left(1 - D_{\Delta ILmax}\right) \tag{4}$$

where

- $D_{\Delta ILmax}$ is equal to 33%

For this design example $V_{SUPPLY\_\Delta ILmax}$ is equal to 18 V. Knowing maximum ripple ratio operating point, the desired ripple ratio, load current and the switching frequency, the inductance is calculated using Equation 5

$$L_{M\_calc} = \frac{V_{SUPPLY}{}^2 \cdot D}{I_{LOAD} \cdot RR \cdot V_{LOAD} \cdot f_{SW}} = \frac{18V^2 \cdot 0.486}{5.71A \cdot 0.6 \cdot 35V \cdot 440kHz} = 2.98\ \mu H \quad (5)$$

A standard inductance of 2.6 µH is selected to satisfy the design criteria.

The maximum peak inductor current occurs at the minimum supply voltage, V_{SUPPLY_min}, and the maximum load current $I_{LOADmax}$. The peak inductor current is the sum of the average input current and half of the inductor peak-peak ripple, and is calculated using Equation 6.

$$IL_{PEAKmax} = \frac{V_{LOAD} \cdot I_{LOAD}}{V_{SUPPLY}} + \frac{1}{2} \cdot \frac{V_{SUPPLY} \cdot D}{L_M \cdot f_{SW}} = \frac{35V \cdot 5.71A}{8V} + \frac{1}{2} \cdot \frac{8V \cdot 0.771}{2.6\mu H \cdot 440kHz} = 27.67A \quad (6)$$

2.3 Current Sense Resistor Selection

The LM5123 has a fixed internal slope compensation ramp of 45 mV and a sensed peak current limit of 60 mV referenced to the input of the current sense amplifier. The current sense resistor is sized to prevent sub-harmonic oscillation as the slope compensation is a fixed value and to allow maximum power delivery. The selection process is an iterative process. Analyzing these two separate boundary conditions allow for the correct resistor value to be calculated.

The maximum current sense resistor value is calculated based on the adequate slope compensation to prevent sub-harmonic oscillation in Equation 7. The maximum current sense resistor value is calculated at the maximum duty cycle which occurs at the minimum supply voltage, and the maximum target load voltage.

$$R_{CSslope} \leq \frac{1.5 \cdot L_M \cdot V_{SL} \cdot f_{SW}}{(V_{LOAD} - V_{SUPPLY})} = \frac{1.5 \cdot 2.6\mu H \cdot 45mV \cdot 440kHz}{(35V - 8V)} = 2.86\ m\Omega \quad (7)$$

Based on the calculation, the final selection of the current sense resistor must be less than 2.86 mΩ to prevent sub-harmonic oscillation at the highest duty cycle. Note the R_{CSmax} value is proportional to the selected inductance value.

The peak inductor current calculated in Section 2.2, is used to size the current sense resistor for maximum output power. Due to component tolerances and power loss, the peak current limit is selected with some margin above the calculated peak inductor current. Typically, a range of 5% to 20% is used. In this example, a margin of 20% is selected. The calculated peak inductor current limit is estimated using Equation 8.

$$IL_{PEAKlimitset} = (1 + M_{LIMIT}) \cdot IL_{PEAKmax} = (1 + 0.2) \cdot 27.67A = 33.2A \quad (8)$$

where

- M_{LIMIT} is the select margin above the calculated peak inductor current

The minimum peak current limit set by the current sense resistor must be greater than 33.2 A. The ideal resistor value is calculated using Equation 9

where

$$R_{CSpower} \leq \frac{V_{CL}}{IL_{PEAKlimitset}} = \frac{60mV}{33.2A} = 1.8\ m\Omega \quad (9)$$

- V_{CL} is the fixed 60 mV current limit of the device.

To allow for maximum power the resistor value must be less than 1.8 mΩ.

Sub-harmonic oscillation can occur in a design where the $R_{CSslope}$ value is greater then than the $R_{CSpower}$ value. If this condition occurs, the ripple ratio of the inductor needs to be decreased and the procedure in Section 2.2 should be revisited. By decreasing the ripple ratio the effective slope compensation is increased. The slope compensation is adequate for this design example, and current sense resistor value is selected as a standard value of 1.5 mΩ. Rearranging Equation 9 to Equation 10, the peak inductor current limit is calculated.

$$IL_{PEAKlimit} = \frac{V_{CL}}{R_{CS}} = \frac{60mV}{1.5m\Omega} = 40\ A \quad (10)$$

The selected value of 1.5 mΩ, results in a peak inductor current limit of 40 A.

2.4 Inductor Selection

The inductor is selected according to three main parameters: calculated inductance value (L_M), RMS inductor current and the maximum peak inductor current ($IL_{PEAKlimit}$).

- The inductance is selected to be 2.6 µH. This value is a standard inductance value supplied by many magnetic vendors.
- The inductor RMS current is approximated by the average supply current at the minimum supply voltage, maximum load target voltage and maximum output power, 25 A. The inductor RMS current rating should be higher than the estimated RMS current and keep the inductor temperature to suitable level based on the application.
- The saturation current of the inductor should be larger than the maximum peak inductor current limit, 40A. The magnetic material and constructions of the inductor dictate the saturation profile. A hard saturation profile has a dramatic decrease in inductance when the inductor becomes saturated, while a softer saturation profile has a slower roll off. Check the inductor data sheet to ensure the saturation is above the peak inductor current limit.

For this design example, the inductor is selected to have an inductance value of 2.6 µH, a saturation current limit of 50 A, and a 30°C temperature rise at 25 A RMS.

2.5 Output Capacitor Selection

The output capacitor is required to smooth the load voltage ripple, provides an energy source during load transients. The output capacitor bank and the control loop bandwidth impact the dynamic load transient response of the regulator. The output capacitor delivers energy to the load until the control loop can adjust to the new operating point. The control loop crossover frequency is estimated to approximately 1/8 the right-half plan zero of the boost plant transfer function using Equation 11.

$$f_{CROSSest} = \frac{\omega_{RHP}}{2\pi \cdot 8} = \frac{{V_{SUPPLY}}^2}{2\pi \cdot 8 \cdot P_{OUTmax} \cdot L_M} = \frac{8{V}^2}{2\pi \cdot 8 \cdot 200W \cdot 2.6\mu H} = 2.45kHz \quad (11)$$

The estimated control loop crossover frequency estimated to be 2.45 kHz. Note that the minimum right-half plane zero frequency occurs at the minimum input voltage and maximum output power.

With the target crossover frequency selected, the minimum output capacitance is calculated based on the transient response for a given loaded step using Equation 12. In a variable output voltage design the maximum load step occurs at the minimum target load voltage and the output capacitance is sized accordingly.

$$C_{OUTest} \geq \frac{\Delta I_{LOAD}}{2\pi \cdot \Delta V_{LOAD} \cdot f_{CROSSest}} = \frac{4.167A}{2\pi \cdot 360mV \cdot 2.45kHz} = 752\mu F \quad (12)$$

where

- ΔI_{LOAD} is the given load step. For this example is from half load to full load.
- ΔV_{LOAD} is the load voltage undershoot caused by the load transient. For this example the value is 1.5% of the target load voltage.

The calculated output capacitance is 752 µF, and for this design is selected to be 900 µF.

The output capacitor must be rated to handle the RMS current during the off time of the low-side switch. The maximum output ripple current is estimated using Equation 13.

$$I_{COUTrms} = \sqrt{(1-D)\left[{I_{LOAD}}^2 \cdot \frac{D}{{(1-D)}^2} + \frac{{\Delta I_L}^2}{12}\right]} = \sqrt{(1-0.667)\left[{8.33A}^2 \cdot \frac{0.667}{{(1-0.667)}^2} + \frac{{4.66A}^2}{12}\right]} = 11.82\ A \quad (13)$$

where

- ΔI_L is the peak to peak ripple of the

The estimated RMS current of the output capacitor bank is 11.82 A. Note the highest output capacitor RMS current occurs at the worst case operating condition, minimum supply voltage, maximum load voltage and full

power. The output capacitor bank is comprised of both electrolytic capacitors and ceramic capacitors. Each chemistry benefits the design. Electrolytic capacitors provide a large bulk capacitance for low frequency energy storage to handle load transient demands, in a relatively small footprint. Ceramic capacitors provide a low ESR and low ESL decoupling path to minimize switching noise being coupled to the load voltage. Ceramic capacitor typically has very high RMS current rating. Due to the benefits of each chemistry the output capacitor bank is comprised of both electrolytic and ceramic capacitors.

2.6 Input Capacitor Selection

The input capacitor determines the supply ripple voltage. For this design an input capacitance of 220 µF is selected using low ESR ceramic capacitors. Equation 14 is used to calculate the maximum supply voltage ripple.

$$\Delta V_{\text{SUPPLY}} = \frac{V_{\text{LOAD}}}{32 \times L_M \times C_{\text{IN}} \times {f_{\text{sw}}}^2} = \frac{24V}{32 \times 2.6\mu\text{H} \times 220\mu\text{F} \times 440K\text{Hz}^2} = 6.7\text{mV} \quad (14)$$

2.7 Feedback Resistor Selection

The LM5123 controls the load voltage by the voltage on the TRK pin. The TRK pin is the reference voltage to the internal error amplifier. There are two output voltage ranges, a low range which allows for an output voltage range from 5-V and 20-V, and a high range which allows for an output voltage range from 20-V to 57-V. The range is selected by the resistance connected from the VREF pin to AGND. The VREF pin is a 1 V reference and is used to set a fixed load voltage through a resistor divider to the TRK pin. Table 2-1 shows the resistor range to select the voltage range. It is recommend to place a 470 pF capacitor from VREF to ANGD.

Table 2-1. V_{LOAD} Range selection

Voltage Range	Minimum resistance	Maximum resistance	K_{FB} (1)
Low range (5 V - 15V)	75 kΩ	100 kΩ	20
High range (20 V - 57 V)	20 kΩ	35 kΩ	60

(1) K_{FB} is the feedback attenuation from VOUT/SENSE pin to the internal error amplifier

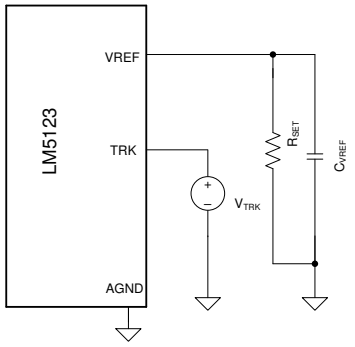

Figure 2-3. Variable load voltage configuration

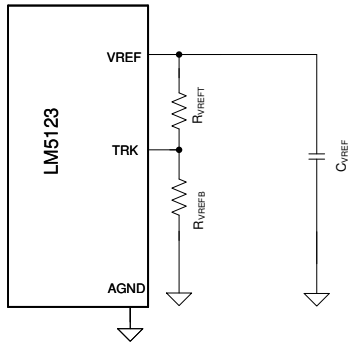

Figure 2-4. Fixed load voltage configuration

For a variable load voltage the TRK pin voltage is set by an external source as shown in Figure 2-3.

The R_{SET} resistance value is selected based on the require load voltage range. See Table 2-1 to select R_{SET}. The TRK pin voltage for a given load voltage target is calculated using Equation 15.

$$V_{TRK} = \frac{V_{LOAD}}{K_{FB}} \quad (15)$$

To configure a fixed load voltage a resistor divider is connected from the VREF pin to the TRK pin as shown in Figure 2-4.

R_{VREFT} is should be selected between the values calculated in Equation 16.

$$\frac{R_{VREFmin} \cdot \left(V_{REF} - \frac{V_{LOAD}}{K_{FB}}\right)}{V_{REF}} \le R_{VREFT} \le \frac{R_{VREFmax} \cdot \left(V_{REF} - \frac{V_{LOAD}}{K_{FB}}\right)}{V_{REF}} \quad (16)$$

$$\frac{20k\Omega \cdot \left(1V - \frac{24V}{60}\right)}{1V} \le R_{VREFT} \le \frac{35k\Omega \cdot \left(1V - \frac{24V}{60}\right)}{1V}$$

Assuming the target load voltage is 24 V, R_{VREFT} must be between 12 kΩ and 21 kΩ. R_{VREFT} is selected to be 21 kΩ. The value for RVREFB is calculated using Equation 17.

$$R_{VREFB} = \frac{\frac{V_{LOAD}}{K_{FB}} \cdot R_{VREFT}}{V_{REF} - \frac{V_{LOAD}}{K_{FB}}} = \frac{\frac{24V}{60} \cdot 21k\Omega}{1 - \frac{24V}{60}} = 14\ k\Omega \quad (17)$$

R_{VREFB} is selected to be 14 kΩ.

2.8 UVLO Resistor Selection

The external under voltage lockout (UVLO) resistors set the minimum operating voltage of the regulator. Two levels must be specified: the desired start-up voltage of the converter ($V_{SUPPLY(ON)}$) and the desired turn-off voltage of the converter ($V_{SUPPLY(OFF)}$). In this example, $V_{SUPPLY(ON)}$ voltage is 6.2 V and the $V_{SUPPLY(OFF)}$ is 5.2 V. Using Equation 18, the top UVLO resistor (R_{UVT}) is calculated.

$$R_{UVT} = \frac{0.977 \cdot V_{SUPPLYon} - V_{SUPPLYoff}}{I_{UVLO-HYST}} = \frac{0.967 \cdot 6.2V - 5.2V}{10\mu A} = 85.9\ k\Omega \quad (18)$$

where

- $I_{UVLO-HYST}$ is the current sunk by the EN/UVLO pin in standby mode.

A standard value of 86.6 kΩ is selected for R_{UVT}. Using Equation 19, the bottom UVLO resistor (R_{UVB}) is calculated.

$$R_{UVB} = \frac{1.1V \cdot R_{UVLOt}}{V_{SUPPLYon} - 1.1V} = \frac{1.1V \cdot 86.6\ k\Omega}{6.2V - 1.1V} = 18.68\ k\Omega \quad (19)$$

A standard value of 18.7 kΩ is selected for R_{UVB}.

2.9 Soft-Start Capacitor Selection

The soft-start capacitor eliminates the overshoot of the load voltage and minimizes the inrush current during the start-up of the regulator when properly selected. The minimum recommended soft-start capacitor value is calculated using Equation 20.

$$C_{SSmin} = \frac{I_{SS} \cdot V_{LOAD} \cdot C_{OUT}}{V_{TRK} \cdot I_{LOAD}} = \frac{20\mu A \cdot 35V \cdot 900\mu F}{583mV \cdot 5.71A} = 189\ nF \quad (20)$$

where

- I_{SS} is the current sourced from the SS pin
- V_{LOAD} is the maximum target load voltage
- V_{TRK} is the voltage on the TRK pin to set V_{LOAD}
- I_{LOAD} is the maximum load current at V_{LOAD}

The soft-start capacitor should be larger than 189 nF to eliminate overshoot on the load voltage during start-up.

In this design, for a given soft-start time of 7 ms at the minimum input voltage of 8 V, the soft-start capacitor can be calculated using Equation 21.

$$C_{SS} = \frac{t_{SS} \cdot I_{SS}}{V_{TRK} \cdot \left(1 - \frac{V_{SUPPLYmin}}{V_{LOADmax}}\right)} = \frac{7ms \cdot 20\mu A}{583mV \cdot \left(1 - \frac{8V}{35V}\right)} = 313\ nF \quad (21)$$

For this design a C_{SS} value of 330nF is selected.

2.10 Control Loop Compensation

Type II compensation network is adequate to stabilize the control loop for a peak current mode architecture. A generic technique for selecting the crossover frequency and placement of the error amplifier the pole and zero resulting in a stable system in CCM is presented. The detailed models of the control loop are presented in Section 4. The following section guides the reader through the process of selecting the control loop compensation components; R_{COMP}, C_{COMP} and C_{HF} as shown in Figure 2-5. Figure 2-6 shows the type II response of the compensation network. G_{Mea} and R_{COMP} sets the mid band gain (g_{MID}) of the compensation network. The zero frequency f_{Zea} is set by the combination R_{COMP} and C_{COMP}. The pole is set by the combination of R_{COMP} and C_{HF}.

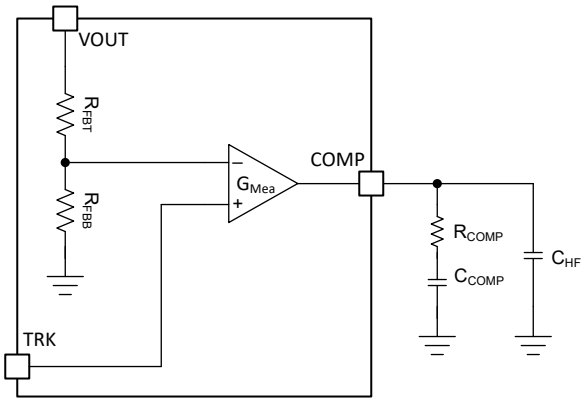

Figure 2-5. Control loop compensation network

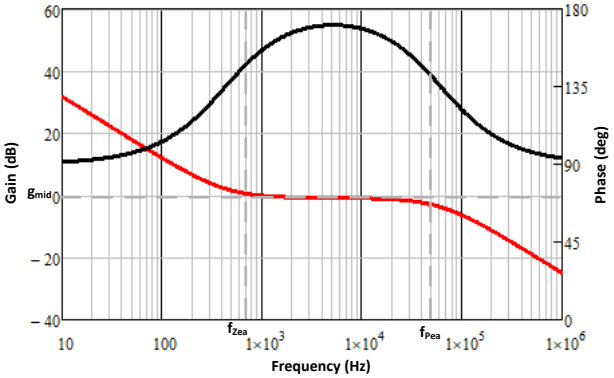

Figure 2-6. Type 2 Compensation

2.10.1 Crossover Frequency (f_{cross}) Selection

The crossover frequency of the control loop is selected to be less than the RHP zero of the modulator small signal model to ensure stability and simplify the compensation component calculations. The control loop crossover frequency is selected to be 1/8 the RHP zero frequency. The crossover frequency can be increased based on the application requirements but it is not recommended to exceed 1/5 the RHP zero frequency for wide supply voltage ranges. Equation 22 calculates the crossover frequency at the worst case operating condition.

$$f_{CROSS} = \frac{1}{8} \cdot \frac{\frac{V_{LOAD}}{I_{LOAD}} \cdot D'^2}{2\pi \cdot L_M} = \frac{1}{8} \cdot \frac{\frac{35V}{5.71A} \cdot \left(\frac{8V}{35V}\right)^2}{2\pi \cdot 2.6\mu H} = 2.45\ kHz \quad (22)$$

where

- D' is (1 -D) at the minimum supply voltage

The target crossover frequency at the worst case operating condition is selected to be 2.45kHz. Note this is the same value used to calculate the minimum output capacitance in Section 2.5.

2.10.2 R_{COMP} Selection

The R_{COMP} values is directly proportional to the mid-band gain of the control loop compensation, g_{MID} and the crossover frequency. Increasing R_{COMP} increases the mid-band gain and thus the crossover frequency is increased. Knowing the desired crossover frequency, R_{COMP} is estimated using Equation 23.

$$R_{COMP} = \frac{2\pi \cdot A_{CS} \cdot K_{FB} \cdot R_{CS} \cdot C_{OUT} \cdot V_{LOADmax} \cdot f_{CROSS}}{V_{SUPPLYmin} \cdot g_{Mea}} = \frac{2\pi \cdot 10 \cdot 60 \cdot 1.5m\Omega \cdot 900\mu A \cdot 35V \cdot 2.45kHz}{8V \cdot 1\frac{mA}{V}} = 54.5\ k\Omega \quad (23)$$

where

- g_{Mea} is the transconductance of the internal error amplifier and is 1 mA/V.
- K_{FB} is the attenuation factor of the internal feedback resistors dependent on the selected output voltage range.

R_{COMP} is selected to be 54.9 kΩ.

2.10.3 C_{COMP} Selection

The R_{COMP} resistor and C_{COMP} capacitor set the zero frequency of the compensation network. The zero of the compensation network provides a phase boost to stabilize the control loop. To provide adequate phase margin the zero frequency is placed at the geometric mean of the crossover frequency (f_{CROSS}) and the low frequency pole of the plant (f_{Plf}). The low frequency pole of the modulator and the zero frequency of the compensation network are estimated using Equation 24and Equation 25, respectively

$$f_{Plf} = \frac{I_{LOAD}}{\pi \cdot C_{OUT} \cdot V_{LOAD}} = \frac{5.71A}{\pi \cdot 900\mu F \cdot 35V} = 57Hz \quad (24)$$

$$f_{Zea} = \sqrt{f_{CROSS} \cdot f_{Plf}} = \sqrt{2.45kHz \cdot 57Hz} = 373\ Hz \quad (25)$$

The the zero frequency of the compensation network estimated to be approximately 373 Hz. Knowing the target frequency, C_{COMP} is calculate using Equation 26.

$$C_{COMP} = \frac{1}{2\pi \cdot f_{Zea} \cdot R_{COMP}} = \frac{1}{2\pi \cdot \sqrt{2.45kHz \cdot 57Hz} \cdot 54.9k\Omega} = 7.76nF \quad (26)$$

C_{COMP} is calculated to be 7.7 nF. Selecting the nearest standard value C_{COMP} is selected to be 6.8 nF.

2.10.4 C_{HF} Selection

The C_{HF} capacitor sets the high frequency pole of the compensation network. The high frequency pole aids in attenuating high frequency noise due to the switching frequency and assuring enough gain margin. It is recommended to set the pole frequency between the minimum RHP zero (f_{RHPz}) and one-half the switching frequency (f_{SW}). The pole location is set at the geometric mean of the RHP zero and one-half the switching frequency using Equation 27.

$$f_{Pea} = \sqrt{f_{RHPz} \cdot \frac{f_{sw}}{2}} = \sqrt{19.5kHz \cdot \frac{440kHz}{2}} = 65.5\ kHz \quad (27)$$

The pole of the compensation network is selected to be approximately 65.5 kHz. CHF is calculated using Equation 28.

$$C_{HF} = \frac{C_{COMP}}{2\pi \cdot C_{COMP} \cdot R_{COMP} \cdot f_{Pea} - 1} = \frac{6.8nF}{2\pi \cdot 6.8nF \cdot 54.9k\Omega \cdot 65.5\ kHz - 1} = 44.6\ pF \quad (28)$$

C_{HF} is estimated to be 44.6 pF. Selecting the nearest standard value, C_{HF} is selected to be 47 pF.

2.11 MOSFET selection

The selection of the power MOSFETs has a significant impact on the DC-DC controllers performance. A MOSFET with low on-state resistance, R_{DSon}, reduces conduction losses, where as low parasitic capacitance and low gate charge parameters reduces the switching losses. Normally, the R_{DSon} and gate charge are inversely proportional. For relatively higher switching frequencies, MOSFET switching losses dominate. For relatively lower switching frequencies conduction losses dominate.

The main parameters affecting MOSFET selection for the LM5123 are as follows:

- $R_{DS(on)}$ at V_{GS} of 5 V.
- Drain to source voltage rating, BV_{DSS}, depending on the load voltage range.
- Gate charge parameters at V_{GS} of 5 V
- Body diode reverse recovery charge, Q_{RR}, of the high-side MOSFET.

The MOSFET related power losses are summarized in Table 2-2. The influence of inductor ripple is considered but second order affect such as switch node ringing and parasitic inductance are not modeled.

Table 2-2. Boost Regulator MOSFET Power Losses

	Low-Side MOSFET	High-side MOSFET
MOSFET conduction	$P_{CONDls} = D \cdot \left(\frac{{I_{LOAD}}^2}{(1-D)^2} + \frac{{\Delta I_L}^2}{12} \right) \cdot R_{DS(on)ls}$	$P_{CONDhs} = (1-D) \cdot \left(\frac{{I_{LOAD}}^2}{(1-D)^2} + \frac{{\Delta I_L}^2}{12} \right) \cdot R_{DS(on)hs}$
MOSFET switching (2)	$P_{SWls} = \frac{V_{LOAD} \cdot f_{sw}}{2} \left[\left(I_{SUPPLY} + \frac{\Delta I_L}{2} \right) \cdot t_{rise} + \left(I_{SUPPLY} - \frac{\Delta I_L}{2} \right) \cdot t_{fall} \right]$	Negligible
Body diode conduction	N/A	$P_{CONDdhs} = \frac{V_{LOAD} \cdot f_{sw}}{2} \left[\left(I_{SUPPLY} + \frac{\Delta I_L}{2} \right) \cdot t_{d1} + \left(I_{SUPPLY} - \frac{\Delta I_L}{2} \right) \cdot t_{d2} \right]$
Body diode reverse recovery losses (1)	N/A	$P_{RRhs} = V_{LOAD} \cdot f_{SW} \cdot Q_{RRhs}$
Gate drive losses	$P_{GATEls} = V_{CC} \cdot f_{SW} \cdot Q_{Gls}$	$P_{GATEhs} = V_{CC} \cdot f_{SW} \cdot Q_{Ghs}$

(1) MOSFET body diode revere recover charge (Q_{RR}) depends on many parameters including forward current, current transition and speed

(2) t_{RISE} and t_{FALL} are the rise and fall time of the switch node. These values depend on many parameters such as total switch node capacitance. Layout of the switch node will impact these values.

3 Implementation Results

Please see the LM5123EVM-BST User's Guide for more testing results.

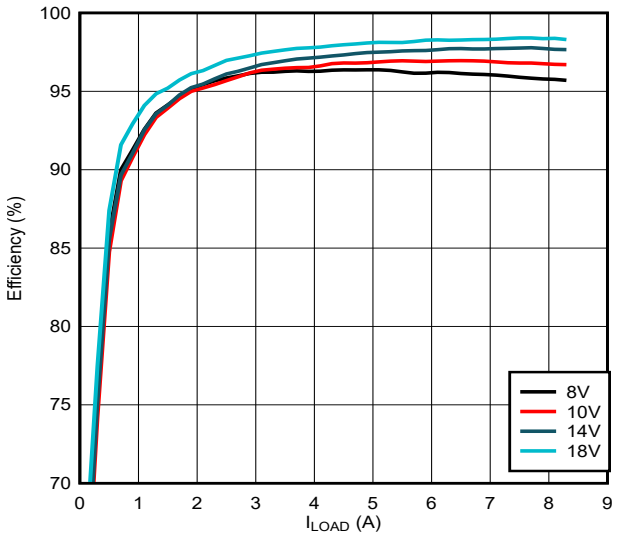

Figure 3-1. Efficiency V_{LOAD} = 24 V

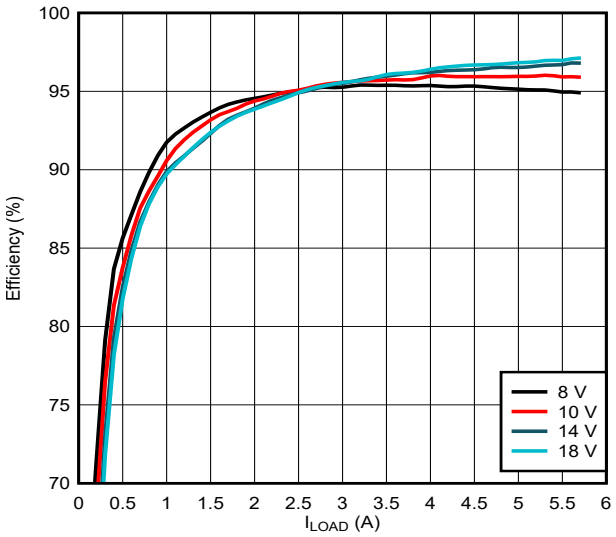

Figure 3-2. Efficiency V_{LOAD} = 35 V

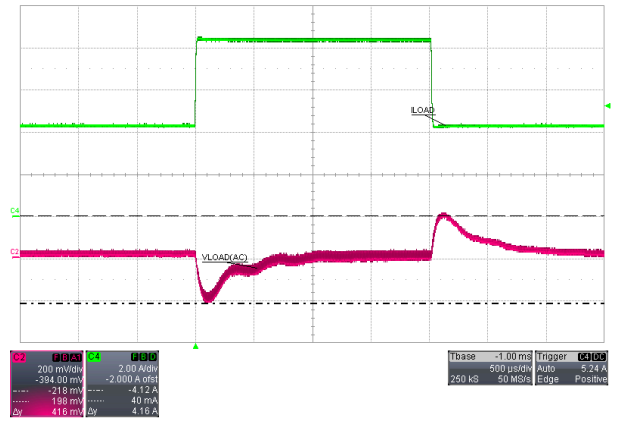

Figure 3-3. Load Transient V_{LOAD} = 24V, V_{SUPPLY} = 8 V

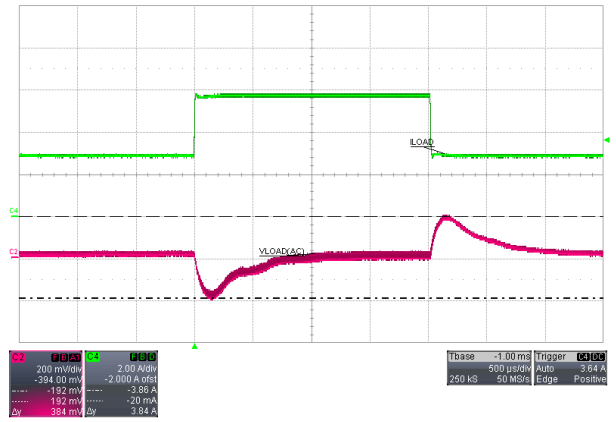

Figure 3-4. Load Transient V_{LOAD} = 35 V, V_{SUPPLY} = 8 V

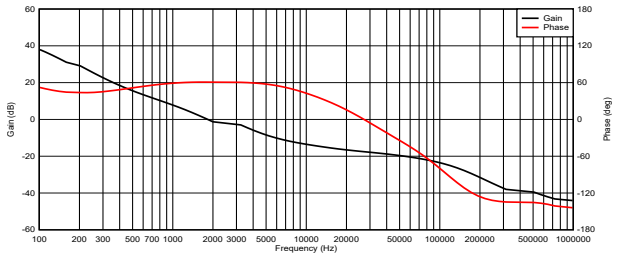

Figure 3-5. 35V Loop

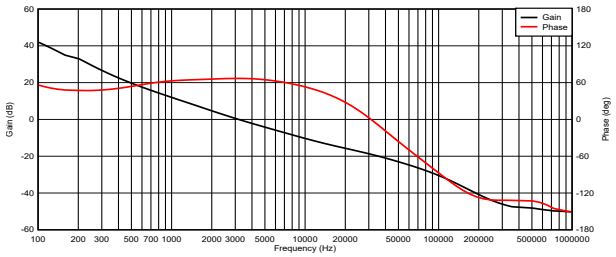

Figure 3-6. 24V Loop

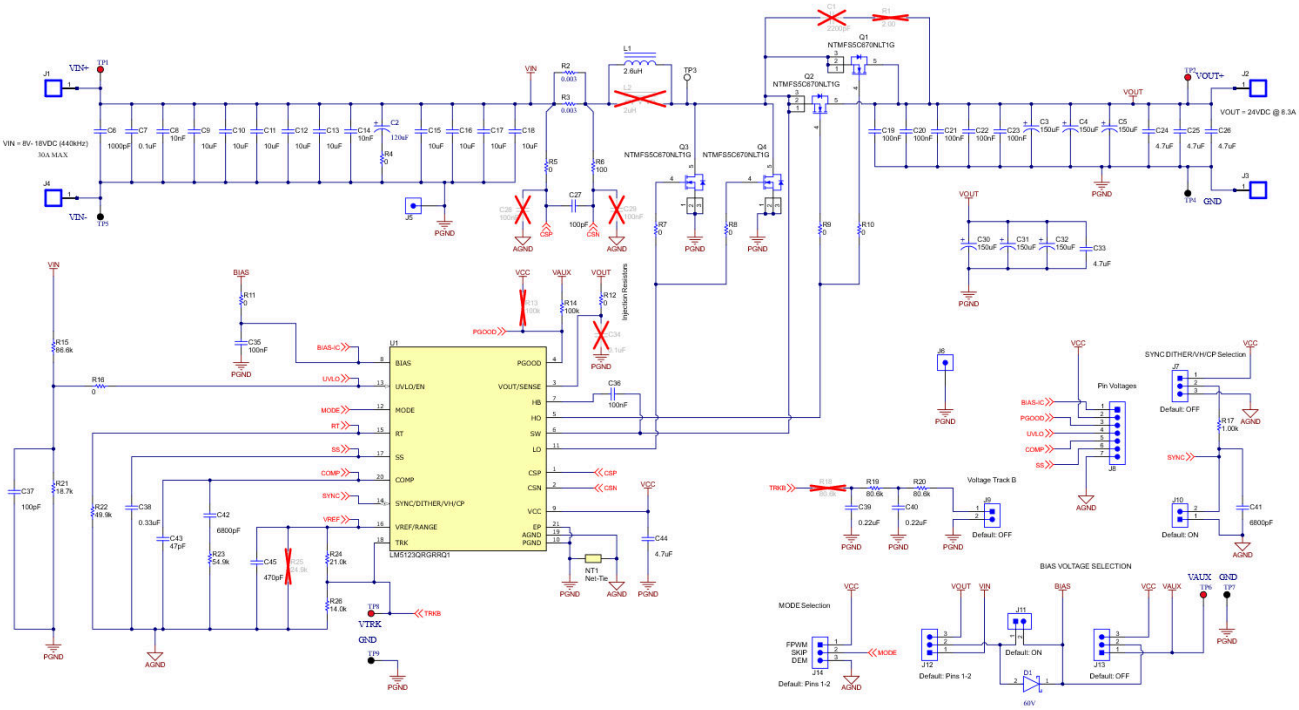

Figure 3-7. LM5123EVM-BST Schematic

Table 3-1. List of Materials

Reference Designator	QTY.	Specification	Manufacturer	Part Number
C2	1	Cap Aluminum Polymer 120uF 50VDC 20% (8 X 12mm) SMD 0.025 Ohm 2100mA 4000h 135C Automotive T/R	Nichicon	PCH1H121MCL2GS
C3, C4, C5, C30, C31, C32	6	150µF 50V Aluminum - Polymer Capacitors 17mOhm 4000 hrs @ 125°C	Panasonic	EEH-ZS1H151P
C6	1	CAP, CERM, 1000 pF, 50 V, +/- 10%, X7R, 0603	Kemet	C0603X102K5RACTU
C7	1	CAP, CERM, 0.1 uF, 50 V, ±10%, X7R, 0603	TDK	C1608X7R1H104K080AA
C8, C14	2	CAP, CERM, 0.01 µF, 100 V,+/- 10%, X7R, 0603	Wurth Elektronik	8.85012E+11
C9, C10, C11, C12, C13, C15, C16, C17, C18	9	CAP, CERM, 10 uF, 50 V, +/- 10%, X7R, 1210	MuRata	GRM32ER71H106KA12L
C19, C20, C21, C22, C23, C35, C36	7	CAP, CERM, 0.1 uF, 100 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	MuRata	GCJ188R72A104KA01D
C20, C21, C22	3	CAP, CERM, 4.7 uF, 100 V, ±10%, X7S, AEC-Q200 Grade 1, 1210	TDK	CGA6M3X7S2A475K200AB
C24, C25, C26, C33	4	CAP, CERM, 4.7 uF, 100 V, +/- 10%, X7S, AEC-Q200 Grade 1, 1210	TDK	CGA6M3X7S2A475K200AB
C27	1	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 0, 0603	TDK	CGA3E2NP01H101J080AA
C37	1	CAP, CERM, 100 pF, 50 V,+/- 1%, C0G/NP0, 0603	Kemet	C0603X103K5RACTU
C38	1	CAP, CERM, 0.33 uF, 10 V, +/- 10%, X5R, 0603	Kemet	C0603C334K8PACTU
C39, C40	2	CAP, CERM, 0.22 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E3X7R1H224K080AB
C41, C42	2	CAP, CERM, 6800 pF, 50 V,+/- 5%, C0G/ NP0, 0603	MuRata	GRM1885C1H682JA01D
C43	1	CAP, CERM, 47 pF, 100 V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603	Kemet	C0603C470J1GACAUTO
C44	1	CAP, CERM, 4.7 uF, 16 V, +/- 10%, X6S, 0603	TDK	C1608X6S1C475K080AC
C45	1	CAP, CERM, 470 pF, 50 V, +/- 5%, C0G/NP0, 0603	AVX	06035A471JAT2A
D1	1	Diode Schottky 60 V 1A Surface Mount SOD-123	Nexperia	PMEG6010CEGWX
H1, H2, H3, H4	4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH
H5, H6, H7, H8	4	Hex Standoff Threaded #4-40 Nylon 0.750" (19.05mm) 3/4" Natural	Keystone Electronics	1902D_Ndrill
J1, J2, J3, J4	4	TERMINAL SCREW PC 30AMP, TH	Keystone	8199
J5, J6	2	TEST POINT SLOTTED .118", TH	Keystone	1040
J7, J12, J13, J14	4	Header, 2.54 mm, 3x1, Gold, TH	Wurth Elektronik	61300311121
J8	1	Header, 100mil, 7x1, Gold, TH	Samtec	TSW-107-07-G-S
J9, J10, J11	3	Header, 2.54 mm, 2x1, Gold, TH	Wurth Elektronik	61300211121
L1	1	Inductor, Shielded Drum Core, WESuperflux200, 2.6 uH, 31.5 A, 0.0016 ohm, SMD	Wurth Elektronik	7443556260
Q1, Q2, Q3, Q4	4	MOSFET, N-CH, 60 V, 71 A, SO-8FL	ON Semiconductor	NTMFS5C670NLT1G
R2, R3	2	RES, 0.003, 1%, 3 W, AEC-Q200 Grade 0, 2512 WIDE	Susumu Co Ltd	KRL6432E-M-R003-F-T1
R4, R5, R7, R8, R9, R10, R11, R16	8	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Panasonic	ERJ-3GEY0R00V
R6	1	RES, 100, 1%, 0.1 W, 0603	Yageo	RC0603FR-07100RL
R12	1	RES, 0, 5%, 0.1 W, 0603	Yageo	RC0603JR-070RL
R14	1	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603100KFKEA
R15	1	RES, 86.6 k, 1%, 0.1 W, 0603	Yageo	RC0603FR-0786K6L
R17	1	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06031K00FKEA
R19, R20	2	RES, 80.6 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060321K0FKEA
R21	1	RES, 18.7 k, 1%, 0.1 W, 0603	Yageo	RT0603DRE0714KL

Table 3-1. List of Materials (continued)

Reference Designator	QTY.	Specification	Manufacturer	Part Number
R22	1	RES, 49.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Panasonic	ERJ-3EKF4992V
R23	1	RES, 54.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060354K9FKEA
R24	1	RES, 21.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060321K0FKEA
R26	1	RES, 14.0 k, 0.5%, 0.1 W, 0603	Yageo America	RT0603DRE0714KL
SH-J1, SH-J2, SH-J3, SH-J4	4	Single Operation 2.54mm Pitch Open Top Jumper Socket	Harwin	M7582-05
TP1, TP2, TP6, TP8	4	Test Point, Miniature, Red, TH	Keystone	5000
TP3	1	Test Point, Miniature, SMT	Keystone	5015
TP4, TP5, TP7, TP9	4	Test Point, Miniature, Black, TH	Keystone	5001
U1	1	2.2-MHz Wide VIN Low-IQ Synchronous Boost Controller with Tracking	Texas Instruments	LM5123QRGRRQ1
C1	0	CAP, CERM, 2200 pF, 100 V, +/- 10%, X7R, 0603	MuRata	GRM188R72A222KA01D
C28, C29	0	CAP, CERM, 0.1 uF, 100 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0603	MuRata	GCJ188R72A104KA01D
C34	0	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	TDK	C1608X7R1H104K080AA
FID1, FID2, FID3, FID4, FID5, FID6	0	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
L2	0	Inductor, Shielded, Composite, 2 uH, 39.9 A, 0.001909 ohm, SMD	Coilcraft	XAL1580-202MEB
R1	0	RES, 2.00, 1%, 0.5 W, AEC-Q200 Grade 0, 1210	Panasonic	ERJ-14BQF2R0U
R13	0	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603100KFKEA
R18	0	RES, 80.6 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060380K6FKEA
R25	0	RES, 24.9 k, 0.1%, 0.1 W, 0603	Yageo America	RT0603BRD0724K9L

4 Small Signal Frequency Modeling

This section provides all the equations for the control loop small signal model when the LM5123 is configured as a boost regulator in CCM operation. The simplified formulas allow for a quick evaluation of the control loop, but loose accuracy at high frequencies. The comprehensive formulas are more complex but provide better accuracy at high frequencies.

4.1 Boost Regulator Modulator Modeling

Table 4-1 includes equations model the plant (control-to-output) of a peak current mode boost regulator in continuous conduction mode.

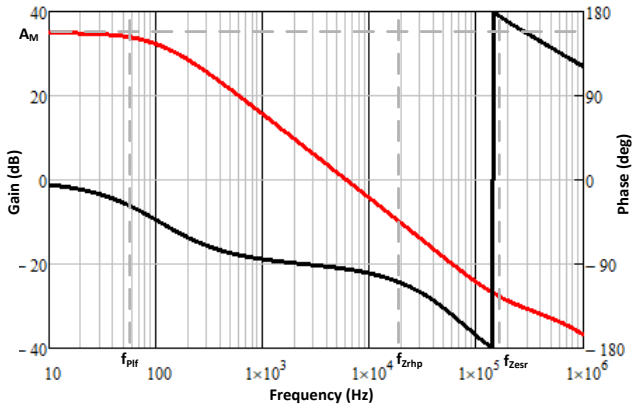

Figure 4-1. Modulator transfer function

Table 4-1. Power Plant Equations

	Simplified Formula	Comprehensive Formula
Modulator Equations		
Modulator Transfer Function	$\frac{\hat{v}_{LOAD}}{\hat{v}_{COMP}} = A_M \frac{\left(1+\frac{s}{\omega_{Zesr}}\right)\cdot\left(1-\frac{s}{\omega_{Zrhp}}\right)}{\left(1+\frac{s}{\omega_{Plf}}\right)}$	$\frac{\hat{v}_{LOAD}}{\hat{v}_{COMP}} = A_M \frac{\left(1+\frac{s}{\omega_{Zesr}}\right)\cdot\left(1-\frac{s}{\omega_{Zrhp}}\right)}{\left(1+\frac{s}{\omega_{Plf}}\right)\cdot\left(1+\frac{s}{Q\cdot\omega_n}+\frac{s^2}{\omega_n}\right)}$
Modulator DC Gain	$A_M = \frac{R_{LOAD}\cdot D'}{2\cdot R_{CS}\cdot A_{CS}}$ (1)	$A_M = \frac{R_{LOAD}\cdot D'}{K_D\cdot R_{CS}\cdot A_{CS}}$ (1)(3)
RHP Zero	$\omega_{Zrhp} = \frac{R_{LOAD}\cdot D'^2}{L_m}$	
ESR Zero	$\omega_{Zesr} = \frac{1}{C_{OUT}\cdot R_{ESR}}$	
Low Frequency Pole	$\omega_{Plf} = \frac{2}{C_{OUT}\cdot R_{LOAD}}$	$\omega_{Plf} = \frac{K_D}{C_{OUT}\cdot R_{LOAD}}$ (3)
Sub-Harmonic Double Pole	Not Considered	$\omega_n = \pi\cdot f_{SW}$
Quality Factor	Not Considered	$Q = \frac{1}{\pi\cdot\left[D'\left(1+\frac{s_e}{s_n}\right)-\frac{1}{2}\right]}$
Slope Compensation	Not Considered	$s_e = V_{SL}\cdot f_{SW}$ (1)
Sensed Rising Inductor Slope	Not Considered	$s_n = \frac{V_{SUPPLY}\cdot R_{CS}\cdot A_{CS}}{L_M}$ (2)
	Not Considered	$K_{EX} = \frac{R_{CS}\cdot A_{CS}\cdot D\cdot D'}{2\cdot L_M\cdot f_{SW}}$ (2)
	Not Considered	$K_M = \frac{1}{\left(\frac{1}{2}-D\right)\cdot\frac{R_{CS}\cdot A_{CS}}{L_M\cdot f_{SW}}+\frac{V_{SL}\cdot A_{CS}}{V_{LOAD}}}$ (1)(2)

Table 4-1. Power Plant Equations (continued)

Simplified Formula		Comprehensive Formula
Modulator Equations		
	Not Considered	$K_D = \frac{R_{LOAD} \cdot D'^2}{R_{CS} \cdot A_{CS}} \cdot \left[\left(\frac{1}{K_M}\right) + \left(\frac{K_{EX}}{D'}\right)\right]$ (2)(3)

(1) V_{SL} is the peak voltage of the internal slope compensation 45 mV
(2) A_{CS} is the gain of the current sense amplifier, 10 V/V.
(3) K_D is approximately equal to 2. This estimation simplifies the equation while still providing accurate high frequency modeling

4.2 Compensation Modeling

Table 4-2 includes equations model a type II compensation network implemented using a transconductance error amplifier.

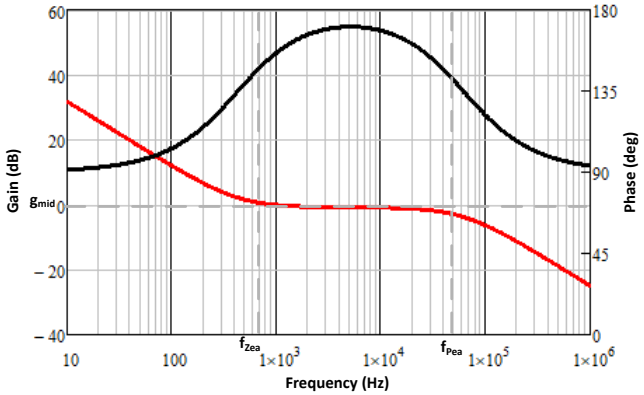

Figure 4-2. Compensation network transfer function

Table 4-2. Compensation Modeling Equations

	Simplified Formula	Comprehensive Formula
Feedback Equations		
Feedback Transfer Function	$\frac{\hat{v}_{COMP}}{\hat{v}_{LOAD}} = -A_{FB}\frac{\left(1+\frac{s}{\omega_{Zea}}\right)}{s\cdot\left(1+\frac{s}{\omega_{Pea}}\right)}$	
Feedback DC Gain	$A_{FB} = \frac{g_{Mea}}{K_{FB}\cdot C_{COMP}}$ (1)(2)	$A_{FB} = \frac{g_{Mea}}{K_{FB}\cdot(C_{COMP}+C_{HF})}$ (1)(2)
Low Frequency Zero	$\omega_{Zea} = \frac{1}{R_{COMP}\cdot C_{COMP}}$	
High Frequency Pole	$\omega_{Pea} = \frac{1}{R_{COMP}\cdot C_{HF}}$	$\omega_{Pea} = \frac{C_{COMP}+C_{HF}}{R_{COMP}\cdot C_{COMP}\cdot C_{HF}}$
Mid-band Gain	$g_{mid} = \frac{R_{COMP}\cdot g_{Mea}}{K_{FB}}$ (1)(2)	$g_{mid} = \frac{R_{COMP}\cdot g_{Mea}\cdot C_{COMP}}{K_{FB}\cdot(C_{COMP}+C_{HF})}$ (1)(2)

1. g_m is the transconductance of the error amplifier, 1 mA/V
2. K_{FB} is the attenuation factor of the internal feedback resistors. This is either 20 for the low load voltage range or 60 for the high voltage load range

4.3 Open Loop Modeling

These equations model the open loop transfer function of the control loop.

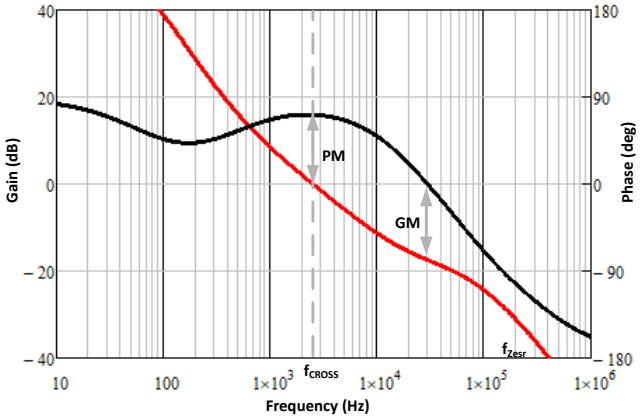

Figure 4-3. Open Loop Transfer function

Table 4-3. Open Loop Modeling Equations

Open Loop Equations		
	Simplified Formula	**Comprehensive Formula**
Open Loop Transfer Function	$T(s) = A_M \frac{\left(1+\frac{s}{\omega_{Zesr}}\right)\cdot\left(1-\frac{s}{\omega_{Zrhp}}\right)}{\left(1+\frac{s}{\omega_{Plf}}\right)} \cdot -A_{FB}\frac{\left(1+\frac{s}{\omega_{Zea}}\right)}{s\cdot\left(1+\frac{s}{\omega_{Pea}}\right)}$	$T(s) = A_M \frac{\left(1+\frac{s}{\omega_{Zesr}}\right)\cdot\left(1-\frac{s}{\omega_{Zrhp}}\right)}{\left(1+\frac{s}{\omega_{Plf}}\right)\cdot\left(1+\frac{s}{Q\cdot\omega_n}+\frac{s^2}{\omega_n}\right)} \cdot -A_{FB}\frac{\left(1+\frac{s}{\omega_{Zea}}\right)}{s\cdot\left(1+\frac{s}{\omega_{Pea}}\right)}$
Estimated crossover frequency	$f_{CROSS} = \frac{V_{SUPPLY}\cdot g_{Mea}\cdot R_{COMP}}{2\pi\cdot A_{CS}\cdot K_{FB}\cdot R_{CS}\cdot C_{OUT}\cdot V_{LOAD}}$	Use Bode Plot

5 Resources

- Texas Instruments, *LM5123-Q1 2.2-MHz Wide VIN Low-IQ Synchronous Boost Controller with VOUT Tracking*, data sheet
- Texas Instruments, *LM5123-Q1 Quick-Start Calculator*
- Texas Instruments, *LM5123-Q1 PSPICE model*
- Texas Instruments, *LM5123EVM-BST Evaluation Module*

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