TPS65313-Q1 Technical Reference Manual

This document provides the factory programmed EEPROM configuration settings and device ID register values (DEV_ID) for the orderable part number, 031310QRWGRQ1.

1 Introduction

This technical reference manual can be used as a reference for the TPS65313-Q1 default factory programmed EEPROM configuration settings for the given orderable part number. This technical reference manual does not provide information about the electrical characteristics, external components, package, or the functionality of the device. For this information and the full register map, refer to the TPS65313-Q1 Wide-VIN Power-Management IC for Automotive Applications Data Sheet.

Table 1 lists the register bits loaded from the EEPROM during device start-up.

Table 1. Main EEPROM Settings for TPS65313-Q1

Orderable Part Number	DEV_ID Register Value	BUCK1 Output Voltage Setting (BUCK1_CFG)	BUCK2 Output Voltage Setting (BUCK2_CFG)	Switching Regulator Clock and Modulation Source (SMPS_CLK_SRC)	External VMON1 Configuration at Power-Up (EXT_VMON1_CFG)	External VMON2 Configuration at Power-Up (EXT_VMON2_CFG)	NRES Extension Delay Configuration (NRES_EXT_DELAY)
O31310QRWGRQ1	0x10	3.3 V	1.2 V	Internal	No	No	Short

Figure 1 shows the typical power supply connections used with 031310QRWGRQ1 device for TI's single chip mmWave radar application.

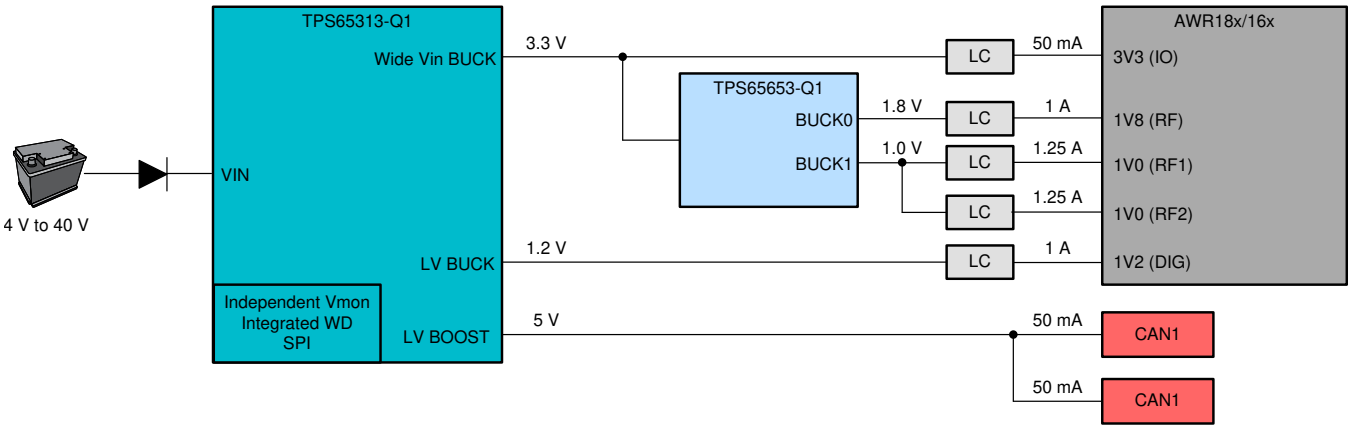

Figure 1. TPS65313-Q1 Power Supply Block Diagram for AWR16xx and AWR18xx Application

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2 Register Bits Loaded From EEPROM

The register bit values loaded from the EEPROM during device start-up.

Table 2. Summary of Register Bits

SPI COMMAND	REGISTER NAME	BIT	VALUE
RD_DEV_ID	DEV_ID	BIT [7] : SMPS_CLK_SRC	0b
RD_DEV_ID	DEV_ID	BIT[6] : EXT_VMON1_CFG	0b
RD_DEV_ID	DEV_ID	BIT [5] : EXT_VMON2_CFG	0b
RD_DEV_ID	DEV_ID	BIT [4] : NRES_EXT_DELAY	1b
RD_DEV_ID	DEV_ID	BIT [2:1] : BUCK2_CFG	00b
RD_DEV_ID	DEV_ID	BIT [0] : BUCK1_CFG	0b

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