TMS320VC5509 to TMS320VC5509A Migration

Muhammad Haque — *C5000 Hardware Applications*

ABSTRACT

This document provides a summary of the differences between the TMS320VC5509 and TMS320VC5509A. All efforts have been made to provide a comprehensive list of the differences between the two devices, this will be updated if additional changes are identified.

As the focus of this document is the differences between the two devices, the descriptions of the behavior and functions of the devices are explained only to the extent to illustrate the differences. This document does not cover the silicon exceptions that may be present on the device. Please consult the TMS320VC5509A Digital Signal Processor Silicon Errata (SPRZ200) for the list of silicon exceptions and the suggested workarounds.

All references in this document to 5509 refer to TMS320VC5509 and TMS320VC5509, unless otherwise specified. All references in this document to 5509A refer to TMS320VC5509A and TMS320VC5509A, unless otherwise specified.

For more detailed information on the TMS320VC5509A consult the references listed at the end of this document.

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1 Device Package and Pin-out

There are no changes to the device package. The following pin changes should not affect 5509-compatible code running on the 5509A.

Table 1. Pins With Added Functionality

GHH Ball No.	PGE Pin No.	5509	5509A
A3	142	GPIO4	GPIO4 This pin now can optionally control SDRAM CKE pin to enable SDRAM self-refresh mode
E14	101	XF	XF This pin now can optionally control SDRAM CKE pin to enable SDRAM self-refresh mode

Table 2. Pins With Changed Functionality

GHH Ball No.	PGE Pin No.	5509	5509A
G12	92	DVSS	USBPLLVSS, dedicated ground for USB PLL
G11	95	CVDD	USBPLLVDD, dedicated power for USB PLL

Table 3. Pins That are Now Fail-Safe†

GHH Ball No.	PGE Pin No.	5509A
H12	91	RESET‡
D6	135	DR0
G14	93	INT0‡
G13	94	INT1‡
G10	96	INT2‡
F14	97	INT3‡
F12	99	INT4‡

† The fail-safe buffers are able to survive the failure of any power supply indefinitely without causing a reliability or functionality hazard in the device on the failed supply, or any other devices that are still powered up.

‡ Fail-safe input buffer with hysteresis.

Table 4. Pin With Functionality Removed

GHH Ball No.	PGE Pin No.	5509A
H1	20	C3, Buskeeper removed

Table 5. Pins That Now Have Hysteresis

GHH Ball No.	PGE Pin No.	5509A
F3	12	GPIO0
E1	10	GPIO1
E2	9	GPIO2
B3	143	GPIO3
A3	142	GPIO4
C4	141	GPIO6
D1	6	GPIO7
J13	85	TCK†
H12	91	RESET†
G14	93	INT0†
G13	94	INT1†
G10	96	INT2†
F14	97	INT3†
F12	99	INT4†

† Fail-safe input buffer with hysteresis.
NOTE: GPIO5 has a buskeeper and therefore does not contain hysteresis.

2 Operating Voltage and CPU Speed

Table 6. Operating vs CPU Speed

CVdd (V) 5509 – 144 MHz			CVdd (V) 5509A – 108 MHz			CVdd (V) 5509A-144MHz			CVdd (V) 5509A – 200 MHz		
Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
1.52	1.6	1.68	1.14	1.2	1.26	1.28	1.35	1.42	1.55	1.6	1.65

IO supply voltage for the 5509 and 5509A remains unchanged.

3 Clock Generation

The recommended crystal parameters for generating system clock using on-chip oscillator have been changed due to upgrade in process technology.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

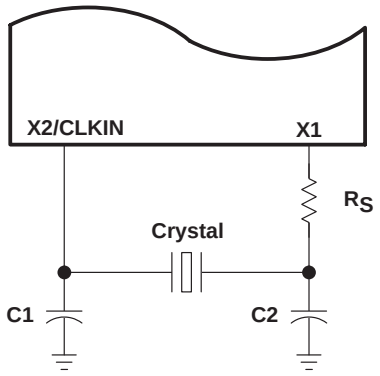


Figure 1. Internal System Oscillator With External Crystal

Table 7. Recommended Crystal Parameters

FREQUENCY RANGE (MHz)	MAX ESR (Ω)	TYP C_{LOAD} (pF)	MAX C_{SHUNT} (pF)	R_S (Ω)
20−15	20	10	7	0
15−12	30	16	7	0
12−10	40	16	7	100
10−8	60	18	7	470
8−6	80	18	7	1.5k
6−5	80	18	7	2.2k

4 CPU and Memory

The CPU on 5509A has been updated to meet 108, 144, and 200 MHz performance requirements. The 5509 CPU exceptions have been corrected by upgrading the core revision from 1.0 to 2.2. Consult the C55x DSP CPU Programmer's Reference Supplement (SPRU652) for the 5509A CPU exceptions.

The internal and external memory structure and organization remains unchanged.

5 Code Generation and Debug Tools

Full 5509A support is provided in CCS2.22 and later. The **−vcore:2.2** compiler/assembler option can be used for core version 2.2 specific code building until the **-v5509A** option is supported by the next tool revision. The DSP BIOS users should upgrade to the latest CCS version with 5509A support.

6 Peripherals

6.1 Universal Serial Bus (USB)

The USB module can be clocked from either an analog phase-locked loop (APLL) or a digital phase-locked loop (DPLL). The DPLL is the power-up default clock source for the USB module to maintain the backward compatibility with 5509. The APLL is the recommended USB clock source due to better noise tolerance and has less long-term jitter than the DPLL.

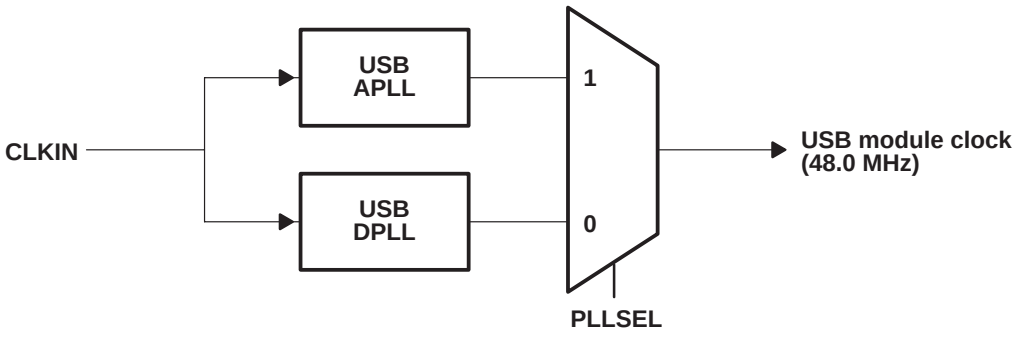


Figure 2. USB Clock Generation

15	3	2	1	0
Reserved		DPLLSTAT	APLLSTAT	PLLSEL
R−0000000000000		R−1	R−0	R/W−0

Figure 3. USB PLL Selection and Status Register (USBPLLSEL)
IO Address: 0x1E80

Table 8. USBPLLSEL Register Bit Descriptions

Bit No.	Bit Name	Reset Value	Function
15−3	Reserved	0	Reserved bits. Always write 0
2	DPLLSTAT	1	Status bit indicating if the DPLL is the source for USB module clock. • DPLLSTAT = 0 The DPLL is not the USB module clock source • DPLLSTAT = 1 The DPLL is the USB module clock source
1	APLLSTAT	0	Status bit indicating if the APLL is the source for USB module clock. • APLLSTAT = 0 The APLL is not the USB module clock source • APLLSTAT = 1 The APLL is the USB module clock source
0	PLLSEL	0	USB module clock source selection bit • PLLSEL = 0 DPLL is selected as USB module clock source • PLLSEL = 1 APLL is selected as USB module clock source

15 12	11	10 3	2	1	0
MULT	DIV	COUNT	ON	MODE	STAT
R/W−0000	R/W−0	R/W−00000000	R/W−0	R/W−0	R−0

Figure 4. USB APLL Control and Status Register (USBAPLL)
IO Address: 0x1F00

Table 9. USBAPLL Register Bit Descriptions

Bit No.	Bit Name	Reset Value	Function
15−12	MULT	0	PLL Multiply Factor K. Multiply Factor K combined with DIV and NDIV determine the final PLL output clock frequency. K = MULT[3:0]+1
11	DIV	0	PLL Divide Factor (D) selection bit for PLL multiply mode operation. DIV combined with K and NDIV determine the final PLL output clock frequency. When the PLL operating in multiply mode: • DIV = 0 PLL Divide Factor D = 1 • DIV = 1 PLL Divide Factor D = 2 if K is odd PLL Divide Factor D = 4 if K is even
10−3	COUNT	0	8-bit counter for PLL lock timer. When NDIV bit is set to 1 the COUNT field starts decrementing by 1 at the rate of CLKIN/16. When COUNT decrements to 0 the STAT bit is set to 1 and the PLL enabled clock is sourced to the USB module.
2	ON	0	PLL Voltage Controlled Oscillator (VCO) enable bit. This bit works in conjunction with NDIV to enable or disable the VCO. **ON / NDIV / VCO** 0 / 0 / OFF 1 / X / ON X / 1 / ON X = Don't care
1	MODE	0	PLL mode selection bit • MODE = 0 PLL operating in divide mode (VCO bypassed). When the PLL operating in DIV mode the PLL Divide Factor (D) is determined by the factor K. D = 2 if K = 1 to 15 D = 4 if K = 16 • MODE = 1 PLL operating in multiply mode (VCO on). The PLL multiply and divide factors are determined by DIV and K
0	STAT	0	PLL Lock Status bit • STAT = 0 PLL operating in divide mode (VCO bypassed) • STAT = 1 PLL operating in multiply mode (VCO on)

The DIV combined with MODE and K defines the final PLL multiplication ratio M/D as indicated below. The USB APLL clock frequency can be expressed by:

$$F_{USB\ APLL\ CLK} = F_{CLKIN} \times (M/D)$$

The multiplication factor M and the dividing factor D are defined in Table 10.

Table 10. Definition of Multiplication (M) and Dividing (D) Factors

MODE	DIV	K	M	D
0	X	1 to 15	1	2
0	X	16	1	4
1	0	1 to 15	K	1
1	0	16	1	1
1	1	Odd	K	2
1	1	Even	K−1	4

The USB clock generation and the PLL switching scheme are discussed in detail in The *TMS320VC5509 DSP Universal Serial Bus (USB) Module Reference Guide* (SPRU596).

6.2 External Memory Interface (EMIF)

Table 11. Asynchronous Mode

Issue	5509	5509A
Bus error generation on 8-bit asynchronous writes	Writes to memory configured as 8-bit asynchronous memory cause the EMIF to hang (5509 Exception EMIF_2)	Writes to memory configured as 8-bit asynchronous memory do not cause the EMIF to hang and generate a bus error. (8-bit asynchronous memory is read-only).
ARDY interaction with programmed HOLD timing	If HOLD is set to zero and ARDY is used to extend the strobe period, asynchronous accesses may operate incorrectly. (5509 Exception EMIF_3)	Corrected
ARDYOFF feature	Not available	ARDYOFF function added to EMIF Global Control Register bit 4. ARDYOFF provides the option to disable the use of hardware wait states on the asynchronous interface. If ARDY OFF is active, the ARDY is not sampled during asynchronous accesses and the access timing is only based on the programmed timings.

Table 12. SDRAM Mode

Issue	5509	5509A
Self-Refresh	Not supported	Either GPIO4 for XF pin can be programmed to drive SDRAM CKE pin. EBSR [11] is used to control SDRAM Self-Refresh mode
CLKMEM = 1/2 CPU	EBSR [11] must be set to 1	SDC3 [2] bit must be cleared to 0. EBSR[11] not used.
CLKMEM = 1/16 CPU	Not supported	Supported
CLKMEM = 1/4, 1/8, 1/16 CPU	SDC3 does not exist	SDC3 [2] bit must be cleared to 0

For detailed information on the 5509 and 5509A SDRAM interfaces consult the *TMS320VC5509 External Memory Interface (EMIF) Reference Guide* (SPRU670).

6.3 Enhanced Host Port Interface (EHPI)

The table concerns the migration issues associated with the EHPI. See the 5509A silicon errata for any specific exceptions associated with the EHPI.

Table 13. EHPI Migration Issues

Issue	5509	5509A
Delay from rising strobe (HDS1 or HDS2) to falling HRDY	Up to 3 CPU cycles	Static delay. See the 5509A data sheet for the specific value.
Initiating EHPI transactions (falling HDS1 or HDS2)	Does not allow a new transaction when HRDY is still low.	Allows a new transaction when HRDY is still low.
Byte Enable Support	No support	Supported
Data pre-fetch	Supported (MUX mode)	No support

6.3.1 Important Information about the EHPI Byte Enable Pins (HBE0/1)

The function of the EHPI byte enables (HBE0 and HBE1) is supported on 5509A. External pull-down resistors must be used to drive HBE [1:0] pins low all the time if the host processor does not drive these pins. When byte enable feature used with auto-increment (muxed EHPI) mode the HPIA register is incremented following high byte access (HBE1 driven low) only.

6.4 Inter-Integrated Circuit (I2C)

There have been multiple bug fixes to the I2C module; however, overall functionality has not been affected. Consult the *TMS320VC5501/5502/5509 DSP Inter-Integrated Circuit (I2C) Module Reference Guide* (SPRU146) and the 5509A silicon errata for details. Users may have to remove the I2c software workarounds while porting code for 5509A.

Table 14. 5509A I2C Idle Control

Issue	5509	5509A
Idling I2C module	I2CMDR [12] controls the I2C module idling feature	I2CMDR2 [0] controls the I2C module idling feature

6.5 Direct Memory Access (DMA) Controller

Table 15. DMA Controller for 5509 and 5509A

Issue	5509	5509A
Additional DMA power conservation feature	DMA are always running unless clock generator domain is in idle.	AUTOGATING_ON field added to DMA Global Control Register (DMA_GCR bit 3). When the DMA is not in idle mode and AUTOGATING_ON = 0, DMA clocks are always on whether the DMA is active or not. When the DMA is not in idle mode and AUTOGATING_ON = 1, DMA clocks are only on when the DMA is active. When the DMA is not active, the clocks to the DMA controller are turned off, conserving power.
Source/DestinationElement /Frame Index Support	The Element Index Register (DMA_CEI) and Frame Index Register (DMA_CFI) apply to both the source and destination.	Separate element and frame index registers are provided so that the source and destination addressing modes can be specified differently. New registers: • DMA_CSEI Channel Source Element Index • DMA_CSFI Channel Source Frame Index • DMA_CDEI Channel Destination Element Index • DMA_CDFI Channel Destination Frame Index
Software Compatibility for additional element / frame index support (above)	Not supported	DMA Software Compatibility Control Register (DMA_GSCR) added. See DMAGSCR detail below.
Ability to monitor source destination address status on an active channel.	There is no ability to monitor the current address on an active DMA channel.	The DMA Source Address Counter (DMA_CSAC) and the DMA Destination Address Counter (DMA_CDAC) have been added. The user can read these registers to monitor progress of the source/destination addresses in the DMA channel.
Added ability to enable/disable DMA timeout function for internal memory accesses.	Not supported	DMA Timeout Control Register (DMA_GTCR) added. See DMAGTCR detail below.

Table 16 shows a comparison of the 5509 and 5509A DMA registers. By default, the DMA will be code compatible with the 5509. See the Global Software Compatibility Register description to take advantage of these new 5509A DMA features

Table 16. Comparison of 5509 and 5509A DMA Registers

5509 Register Name	5509A Register Name	Description	Ch 0 Addr	Ch 1 Addr	Ch 2 Addr	Ch 3 Addr	Ch 4 Addr	Ch 5 Addr
DMA_GCR	DMA_GCR	Global Control Register	0E00	0E00	0E00	0E00	0E00	0E00
	DMA_GSCR	Global Software Compatibility Register	0E02	0E02	0E02	0E02	0E02	0E02
	DMA_GTCR	Global Timeout Control Register	0E03	0E03	0E03	0E03	0E03	0E03
DMA_CDSP	DMA_CDSP	Channel Source/Destination Parameters Register	0C00	0C20	0C40	0C60	0C80	0CA0
DMA_CCR	DMA_CCR	Channel Control Register	0C01	0C21	0C41	0C61	0C81	0CA1
DMA_CICR	DMA_CICR	Channel Interrupt Control Register	0C02	0C22	0C42	0C62	0C82	0CA2
DMA_CSR	DMA_CSR	Channel Status Register	0C03	0C23	0C43	0C63	0C83	0CA3
DMA_CSSA_L	DMA_CSSA_L	Channel SRC start Address (lower)	0C04	0C24	0C44	0C64	0C84	0CA4
DMA_CSSA_U	DMA_CSSA_U	Channel SRC start Address (upper)	0C05	0C25	0C45	0C65	0C85	0CA5
DMA_CDSA_L	DMA_CDSA_L	Channel SRC start Address (lower)	0C06	0C26	0C46	0C66	0C86	0CA6
DMA_CDSA_U	DMA_CDSA_U	Channel SRC start Address (upper)	0C07	0C27	0C47	0C67	0C87	0CA7
DMA_CEN	DMA_CEN	Channel Element Number	0C08	0C28	0C48	0C68	0C88	0CA8
DMA_CFN	DMA_CFN	Channel Frame Number	0C09	0C29	0C49	0C69	0C89	0CA9
DMA_CFI	DMA_CSFI	Channel Frame Index Channel Source Frame Index (5509A)	0C0A	0C2A	0C4A	0C6A	0C8A	0CAA
DMA_CEI	DMA_CSEI	Channel Element Index Channel Source Element Index (5509A)	0C0B	0C2B	0C4B	0C6B	0C8B	0CAB
	DMA_CSAC	Channel Source Address Counter	0C0C	0C2C	0C4C	0C6C	0C8C	0CAC
	DMA_CDAC	Channel Destination Address Counter	0C0D	0C2D	0C4D	0C6D	0C8D	0CAD
	DMA_CDEI	Channel Destination Element Index	0C0E	0C2E	0C4E	0C6E	0C8E	0CAE
	DMA_CDFI	Channel Destination Frame Index	0C0F	0C2F	0C4F	0C6F	0C8F	0CAF

15	1	0
Reserved		DINDXMD
R/W–000000000000000		R/W–0†

† When this bit is set to zero, the DMA is code compatible with the 5509. This bit must be set to one to take advantage of the additional 5509A DMA features.

Figure 5. Global Software Compatibility Register (DMA_GSCR)

Table 17. DMA_GSCR Register Bit Descriptions

Bit	Field	Value	Description
15−1	Reserved	000000000000000b	These bits are not available for your use.
0	DINDXMD		Destination Element and Frame Index Compatibility Mode. This bit determines which registers will be used to indicate the destination element and frame indexes.
		0b	One element index for both the source and destination is stored in the channel source element index register (DMACSEI). One frame index for both the source and destination is stored in the channel source frame index register (DMACSEI).
		1b	The source element index is stored in the channel source element index register (DMACSEI). The destination element index is stored in the channel destination element index register (DMACDEI). The source frame index is stored in the channel source frame index register (DMACSFI). The destination frame index is stored in the channel destination frame index register (DMACDFI).

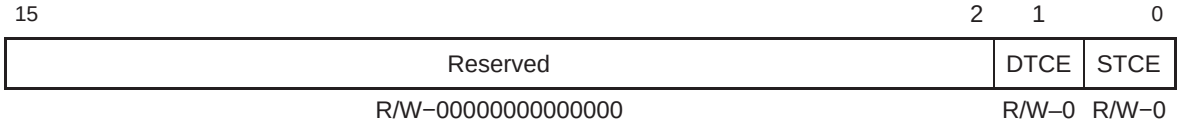


Figure 6. Global Timeout Control Register (DMA_GTCR)

Table 18. DMA_GTCR Register Bit Descriptions

Bit	Field	Value	Description
15−2	Reserved	0000000000 00000b	These bits are not available for your use.
1	DTCE		DARAM timeout counter enable. This bit enables/disables the timeout counter used to monitor delays on DMA requests to the DARAM port.
		0b	DARAM timeout counter disabled
		1b	DARAM timeout counter enabled
0	STCE		SARAM timeout counter enable. This bit enables/disables the timeout counter used to monitor delays on DMA requests to the SARAM port.
		0b	SARAM timeout counter disabled
		1b	SARAM timeout counter enabled

6.6 Multichannel Buffered Serial Port (McBSP)

The programming and operation of the McBSPs remain unchanged.

6.7 Timers

The programming and operation of the timers and the TIN/TOUT0 pin remains unchanged. However the shortest timer period is 4 CPU cycles for the 5509A. The shortest timer period supported by the 5509 is 3 CPU cycles.

6.8 General-Purpose I/O (GPIO, AGPIO, EHPI GPIO)

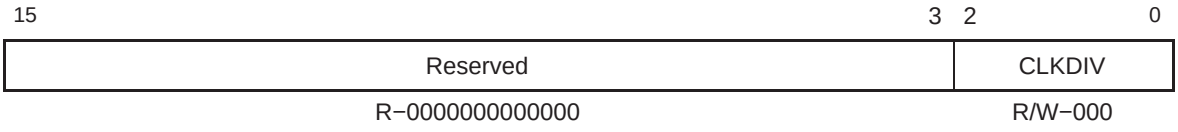
The programming and operation of the GPIO pins remain unchanged, with the exception of GPIO4.

GPIO4 can be used to control the SDRAM CKE pin. Consult the 5509A data sheet and the *TMS320VC5509 External Memory Interface (EMIF) Reference Guide* (SPRU670) for details.

7 System Register (SYSR)

The System Register is located at port address 0x07FD. The SYSR controls the CPU clock present at the CLKOUT pin. The SYSR was not supported on the 5509.

The contents of SYSR are shown in Figure 7.



Legend: R = Read, W = Write, −0 = after reset, −1 = 1 after reset

Figure 7. System Register (SYSR)

Table 19. SYSR Register Bit Descriptions

Bit No.	Bit Name	Reset Value	Function
15−3	Reserved	0	This bit is reserved and must be written as 0.
2−0	CLKDIV	000	CLKOUT Divide Factor Allows the clock present on the CLKOUT pin to be a divided-down version of the internal CPU clock. This field does not affect the programming of the PLL. • 000 = CLKOUT represents the CPU clock divided by 1 • 001 = CLKOUT represents the CPU clock divided by 2 • 010 = CLKOUT represents the CPU clock divided by 4 • 011 = CLKOUT represents the CPU clock divided by 6 • 100 = CLKOUT represents the CPU clock divided by 8 • 101 = CLKOUT represents the CPU clock divided by 10 • 110 = CLKOUT represents the CPU clock divided by 12 • 111 = CLKOUT represents the CPU clock divided by 14

8 Disabling the On-chip System Oscillator

The programming sequence for disabling the on-chip oscillator to attain maximum power saving remained unchanged except for the McBSP transmittal and the receiver must be disabled before initiating the oscillator disable sequence. For recommended programming steps for disabling on-chip oscillator, please review the application report *Disabling the Internal Oscillator on the TMS320VC5507/5509/5509A DSP (SPRA078)*.

9 Bootloader

The 5509A bootloader is always invoked after reset. The function of the bootloader is to transfer user code from an external source to the on-chip RAM or external memory. The 5509A supports several different bootmodes to download DSP code to accommodate varying system requirements. For details see the application report *Using the TMS320C5509/TMS320C5509A Bootloader* (SPRA375).

Table 20. Bootmodes Supported by 5509 and 5509A

BOOTM [3:0]	5509	5509A	Description
0000b	–	–	Reserved
0001b	Yes	Yes	Serial EEPROM (SPI – 24-bit address) boot from McBSP0
0010b	Yes	Yes	USB
0011b	No	Yes	I2C EEPROM
0100b	–	–	Reserved
0101b	Yes	Yes	EHPI (multiplexed mode) boot
0110b	Yes	Yes	EHPI (non-multiplexed mode) boot
0111b	–	–	Reserved
1000b	Yes	Yes	Execute from 16-bit external asynchronous memory
1001b	Yes	Yes	Serial EEPROM (SPI – 16-bit address) boot from McBSP0
1010b	No	Yes	Parallel EMIF boot (8-bit asynchronous memory)
1011b	Yes	Yes	Parallel EMIF boot (16-bit asynchronous memory)
1100b	–	–	Reserved
1101b	–	–	Reserved
1110b	Yes	Yes	Standard serial (16-bit data) boot from McBSP0
1111b	Yes	Yes	Standard serial (8-bit data) boot from McBSP0

10 References

1. *TMS320VC5509 Fixed-Point Digital Signal Processor Data Manual* (SPRS163)
2. *TMS320VC5509A Fixed-Point Digital Signal Processor Data Manual* (SPRS205)
3. *TMS320VC5509 DSP External Memory Interface (EMIF) Reference Guide* (SPRU670)
4. *TMS320VC5501/5502/5509 DSP Inter-Integrated Circuit (I2C) Module Reference Guide* (SPRU146)
5. *TMS320VC5509 DSP Universal Serial Bus (USB) Module Reference Guide* (SPRU596)
6. *TMS320VC5509/5510 DSP Direct Memory Access (DMA) Controller Reference Guide* (SPRU587)
7. *TMS320C55x DSP CPU Programmer's Reference Supplement* (SPRU652)
8. *Disabling the Internal Oscillator on the TMS320VC5507/5509/5509A DSP (SPRA078)*

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Post Office Box 655303 Dallas, Texas 75265