Application Report
SPRAAV7B—October 2009

TMS320TCI6484 and TMS320C6457 DSPs Hardware Design Guide

High-Performance and Multicore Processors

Randy Rosales

Abstract

This application note describes hardware system design considerations for the TMS320TCI6484 and TMS320C6457 DSPs.

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1 Introduction

1.1 Purpose & Scope

This application note is intended to aid in the hardware design and system implementation using theTMS320TCI6484 and TMS320C6457 DSPs.

The document should be used along with the device-specific data manual and relevant user guides, application reports, standards, and specifications (see "References" on page 1-45).

1.2 Terms & Abbreviations

Table 1 Terms and Abbreviations

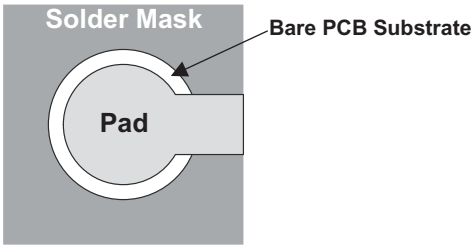
Abbreviation	Definition
BGA	Ball Grid Array
CML	Current Mode Logic, I/O type
DDR2	Double Data Rate 2 (SDRAM Memory)
EMIF	External Memory Interface
FC-BGA	Flip-chip BGA
GPIO	General-Purpose I/O
I^2C	Inter-IC Control bus
JEDEC	Joint Electron Device Engineering Council
LJCB	Low Jitter Clock Buffer: Differential clock input buffer type, compatible with LVDS and LVPECL
LVDS	Low Voltage Differential Swing, I/O type
LVPECL	Low Voltage Positive Emiiter-Coupled Logic, I/O type
McBSP	Multi-channel Buffered Serial Port
MDIO	Management Data Input/Output
NSMD	Non-Solder Mask Defined BGA land
PHY	Physical layer of the interface
SerDes	Serializer/De-serializer
SGMII	Serial Gigabit Media Independent Interface
SRIO	Serial RapidIO
SSTL_18	Stub Series Terminated Logic
TBD	To Be Determined. Implies something is currently under investigation and will be clarified in a later version of the document.
UI	Unit Interval
End of Table 1	

2 Mechanical

2.1 BGA Layout Guidelines

The BGA footprint and pin escapes can be laid-out as defined in the TI reference guide SPRU811, *Flip Chip Ball Grid Array Package*. If the DDR interface is used, there are specific recommendations for BGA pad and pin escape vias given in TI user guide *DSP DDR2 Memory Controller*. Given the 0.80-mm pitch, it is recommended that non-solder mask defined (NSMD) PCB lands be used for mounting the device to the board. With the NSMD method, the land area is etched inside the solder mask area (Figure 1).

Figure 1 Non-Solder-Mask Defined (NSMD) PCB Land



While the size control is dependent on copper etching and is not as accurate as the solder mask-defined (SMD) method, the overall pattern registration is dependent on the copper artwork, which is quite accurate. The tradeoff is between accurate dot placement and accurate dot size. NSMD lands are recommended for small-pitch BGA packages because more space is left between the copper lands for signal traces. Dimensioning for the pad and mask are provided in the TI reference guide SPRU811, *Flip Chip Ball Grid Array Package*. .

2.2 Thermal Issues

A proper understanding of the thermal characteristics of the device is critical for proper design of the board and system. The maximum case temperature of the device must not be exceeded, which requires adequate heat dispersion through a heat sink to be a part of the thermal design.

3 Device Configurations and Initialization

On the TMS320TCI6484 and TMS320C6457 DSP devices, bootmode and certain device configuration selections are determined at device reset based on the state (high or low) of certain GPIO pins. Peripheral usage (enabled/disabled) is determined by the Peripheral Configuration registers after the device reset. Most of the peripherals on the device are *enabled* after reset but some default to disabled. The basic information on configuration options, boot mode options, and use of the Power Configuration registers can be found in the device data manual.

3.1 Device Reset

There are several ways to reset the device and these are described in the data manual. The two external resets, $\overline{\text{POR}}$ and $\overline{\text{RESET}}$, need to be at valid logic levels at all times. $\overline{\text{POR}}$ must be asserted (low) on a power-up while the clocks and power planes become stable. $\overline{\text{RESET}}$ can be used after the powered up state to issue a warm reset, which performs the same as a $\overline{\text{POR}}$ except:

- Test and emulation logic are not reset
- Configuration strapping options (via GPIO pins) are not latched

If warm reset is not needed, $\overline{\text{RESET}}$ can be pulled up to DVDD_18.

The $\overline{\text{RESETSTAT}}$ signal indicates the internal reset state. The $\overline{\text{RESETSTAT}}$ is asserted (low) on power-on reset (issued by $\overline{\text{POR}}$), warm reset (issued by $\overline{\text{RESET}}$), max reset (issued by an emulator), or system reset (issued by emulator or SRIO peripheral). The only reset that does not cause $\overline{\text{RESETSTAT}}$ to be asserted is a CPU reset (issued by watchdog timers).

3.2 Device Configuration

The device configuration strapping options are multiplexed on the GPIO[15:0] pins. In addition to the multiplexed configuration pins, there are three dedicated configuration pins, CORECLKSEL, DDRCLKSEL, and DDRSLRATE. See the data manual for details on the configuration options. If the GPIO signals are not used, the internal pullups and pulldowns can be used to set the input level and an external pullup/down is needed only if the opposite setting is desired. If the GPIO pins are connected to other components, the internal pullup/pulldown resistor should not be relied upon. External 1-kΩ pullups and pulldowns are recommended for all desired settings.

The PLL multiplier can be set only by CPU register writes. The registers are not accessible through boot peripherals. For other boot modes, it is suggested to set the multiplier early in the boot process in order to reduce boot times.

For details on configuration of the PLL, see the *Software-Programmable Phase-Locked Loop (PLL) Controller* user's guide and the device data manual.

3.3 Peripheral Configuration

Other than the device reset configuration covered in "Device Reset" on page 1-5, all other configurations are done by register accesses. Peripherals that default to disabled can be enabled using the Peripheral Configuration registers. If the boot mode selection specifies a particular interface for boot, that peripheral is automatically enabled and configured. For more details on peripheral configuration see the Device Configuration section of the data manual.

For some peripherals, the peripheral operating frequency is dependent on the CPU core clock frequency. This should be accounted for when configuring the peripheral.

3.4 Configuration Tables in I^2C ROM

I^2C ROM contents can contain configuration tables that allow customer-defined memory map accesses during the I^2C boot mode. These accesses can be used to configure peripherals during the boot process. For details see the *Bootloader User's Guide*.

3.5 Boot Modes

The interfaces that support a boot loading process are: EMIF, HPI, I^2C, Serial RapidIO, and EMAC. For a summary of the boot modes supported see the data manual. For details regarding boot modes, see the *Bootloader User's Guide*.

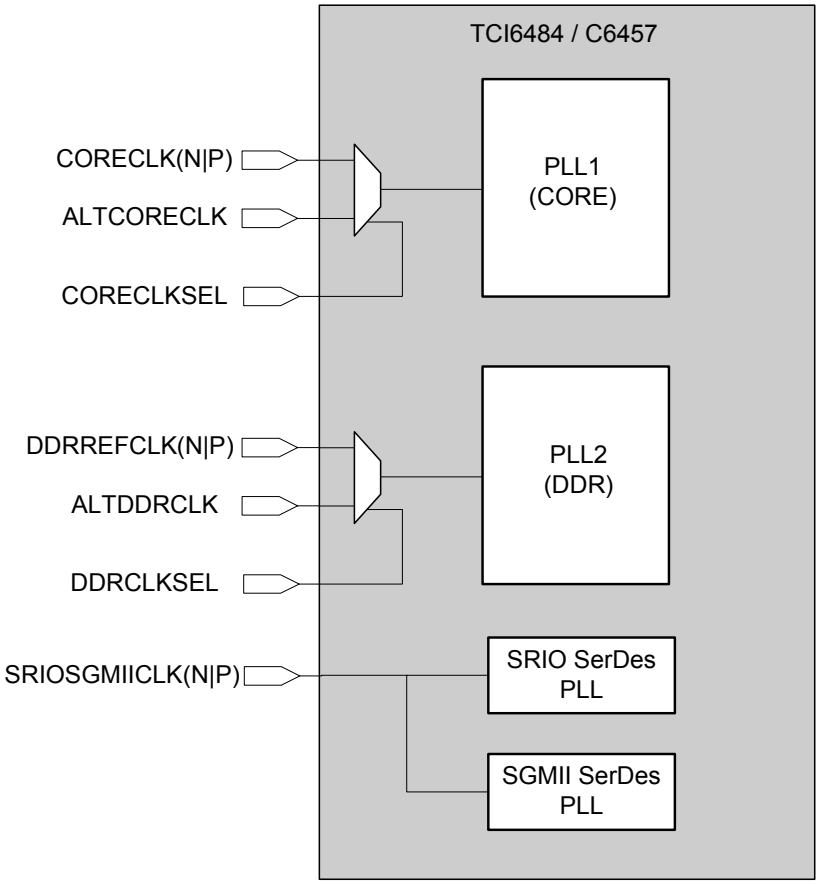
Regardless of the boot mode selected, an emulator connection can always reset the device to acquire control.

4 Clocking

4.1 PLL Reference Clock Solutions

This section describes the clock requirements and a system solution for the PLL reference clocks. There are two types of PLLs and each type has different requirements for its reference clocks. The core PLL and DDR PLL produce clocks for digital logic, whereas the SRIO and SGMII PLLs produce clocks for SERDES (serializer/deserializer) links. Figure 2 is a functional representation of how the reference clocks are connected inside the device.

Figure 2 TMS320TCI6484 and TMS320C6457 DSP Reference Clocks

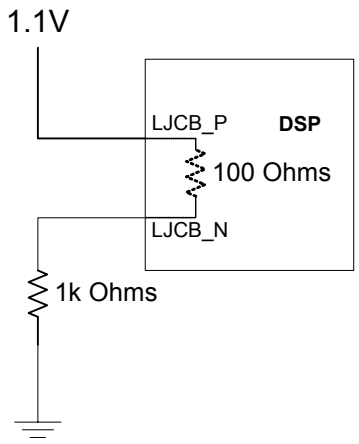


The core PLL can be configured with multiplier values from 1× to 32× and any integer value in between as long as the PLL output frequency does not violate the maximum operating frequency for the device. There are minimum core clock frequency requirements for some peripherals so the data sheet should be consulted to check for any limitations with the desired core clock frequency. The DDR PLL uses a fixed 10× multiplier. The SERDES PLL multipliers are covered in the peripherals section.

All differential clock input buffers are LJCBs (Low Jitter Clock Buffers). These input buffers include a 100-Ω termination (P to N) and a common mode biasing. Because the common mode biasing is included, the clock source must be AC-coupled. LVDS and LVPECL clock sources are compatible with the LJCBs.

Any unused LJCB inputs should be connected to produce a valid logic level. The recommended connections are shown in Figure 3. The 1-kΩ resistor is to reduce power.

Figure 3 Unused LJCB Connections



4.1.1 Clock Requirements

The clock requirements are shown in Table 2.

Table 2 PLL Reference Clock Requirements

Clock	Logic	Input Jitter[1]	T_{rise} and T_{fall} [2]	Duty Cycle	Stability	Frequency Range	Max PLL Frequency
CORECLKP/ CORELKN	LVDS or LVPECL	100 ps peak-to-peak	50 ps-350 ps	45/55%	± 100 PPM	50 MHz – 61.44 MHz	1.0 GHz
ALTCORECLK	1.8-V LVCMOS	100 ps peak-to-peak	50 ps-350 ps	45/55%	± 100 PPM	50 MHz – 61.44 MHz	1.0 GHz
DDRREFCLKP / DDRREFCLKN	LVDS or LVPECL	2.0% of DDRREFCLKP/N input period (peak-peak)[3]	50 ps-350 ps	45/55%	±100 PPM	40 MHz – 66 MHz	333 MHz
ALTDDRCLK	1.8-V LVCMOS	2.0% of DDRREFCLKP/N input period (peak-peak)	50 ps-350 ps	45/55%	±100 PPM	40 MHz – 66 MHz	333 MHz
RIOSGMIICLKP / RIOSGMIICLKN (if SRIO is used)	LVDS or LVPECL	4 ps RMS 56 ps pk-pk @ 1×10^{-12} BER	50 ps-350 ps	45/55%	±100 PPM	125 MHz, 156.25 MHz, 312.5 MHz	2.5 GHz or 3.125 GHz
RIOSGMIICLKP / RIOSGMIICLKN (if SRIO is notused)	LVDS or LVPECL	8ps RMS 112 ps pk-pk @ 1×10^{-12} BER	50 ps-350 ps	45/55%	± 100 PPM	125 MHz, 156.25 MHz, 312.5 MHz	2.5 GHz
End of Table 2							

1. Peak-to-peak jitter value for DDRREFCLK is measured at 10,000 sample points. Total RMS jitter values for RIOSGMIICLK are specified for a target BER for the associated SERDES interface.
2. T_{rise}/T_{fall} values are given for 10% to 90% of the voltage swing.
3. In example assuming a 66 MHz DDRREFCLK the total allowable jitter on the reference clock would be approximately 300ps peak-to-peak

The main concerns for the differential reference clocks are low jitter and proper termination. Either LVDS or LVPECL clock sources can be used but they require different terminations. The input buffer sets its own common mode voltage (CML) so AC coupling is necessary. It also includes a 100-Ω differential termination resistor, eliminating the need for an external 100-Ω termination when using an LVDS driver. For generation information on AC termination schemes, see the *AC-Coupling Between Differential LVPECL, LVDS, HSTL, and CML* application report.

4.1.2 Single Device Solution

It is assumed that the source clock is an oscillator on the same board as the TMS320TCI6484 and TMS320C6457 DSP device. Use of distributed clocks may require a jitter cleaner device such as the CDCL6010. If an on-board oscillator is used with one DSP device, no other components should be needed except for terminations.

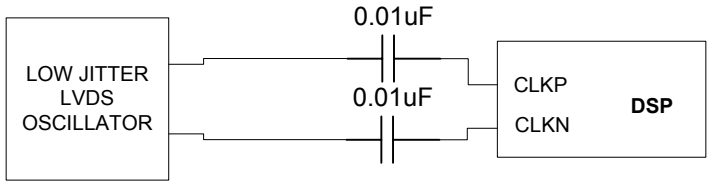
Examples of 3.3-V differential oscillators are:

- Pletronics oscillator: LVDS LV77D
- Pletronics oscillator: LVPECL PE77D

These oscillators have not been tested but are examples of oscillators that meet the specification requirements for all TMS320TCI6484 and TMS320C6457 DSP differential reference clocks. Note that these oscillators require 3.3 V. No availability of 1.8-V differential oscillators that meet the clocking requirements was found, although they may exist.

Figure 4 shows an LVDS based solution including terminations.

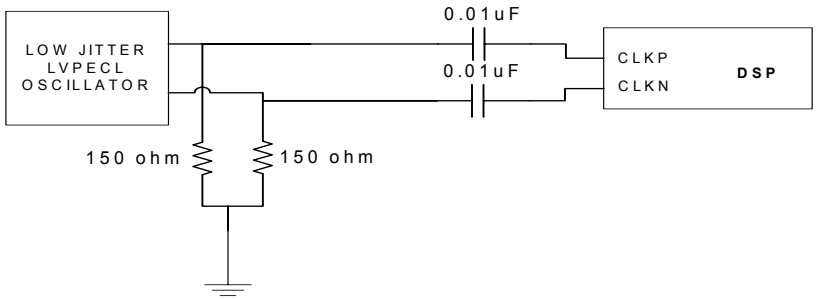
Figure 4 Differential Single Device LVDS Clock Solution



Note—The receiver is self-biasing and does not require the 10-kΩ pullup and pulldown shown in the referenced application note.

Figure 5 shows an LVPECL based solution including terminations.

Figure 5 Differential Single Device LVPECL Clock Solution



4.1.3 Multiple Device Fanout Solutions

For systems with multiple TMS320TCI6484 or TMS320C6457 DSP devices it may be preferred to use one oscillator and a fanout buffer instead of multiple oscillators. This would allow for fewer components as well as lower cost. The fanout buffer can increase the jitter at the clock input so care must be taken in selecting the combination of oscillator and fanout buffer.

In most cases, the same oscillators described in section 4.1 on page 1-7 can be used for the fanout case. The oscillator output specifications should be compared to the fanout buffer input specifications to make sure they are compatible.

If 3.3 V is available, there are many options for clock oscillators and fanout buffers. There are fewer options for 1.8-V fanout buffers but TI does offer one: the CDCL1810.

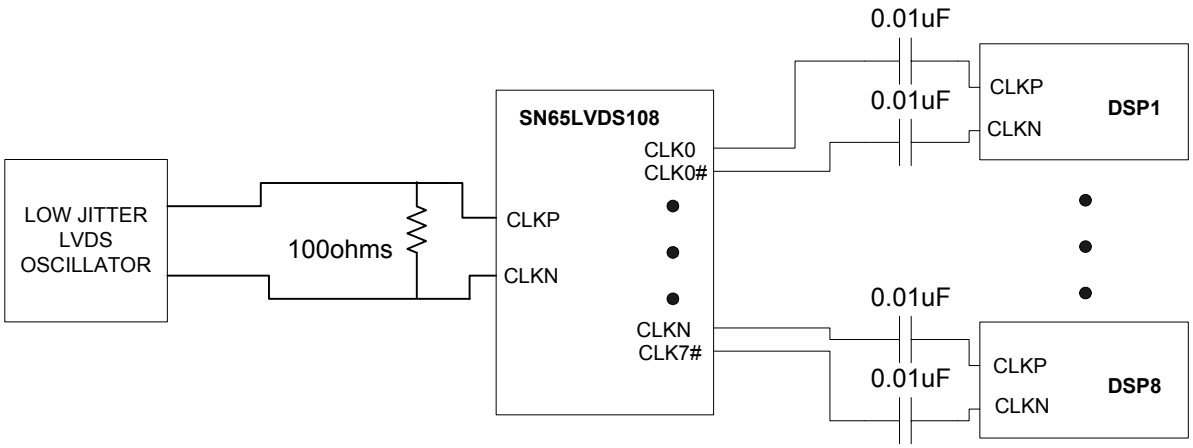
For an all 1.8-V solution, a 1.8-V single-ended oscillator can be used with the CDCL6010. Because the CDCL6010 is a jitter cleaner, the single-ended oscillator does not need to be low-jitter, which allows it to be lower in cost. Also, if a distributed clock with jitter exceeding the input jitter specification is the source (either single ended or differential), the CDCL6010 can be used for both jitter cleaning and distribution. The solution using the CDCL6010 is described in Section 4.1.3.2.

4.1.3.1 Fanout Solutions (No Jitter Cleaning)

Suggested 3.3-V fanout buffers are:

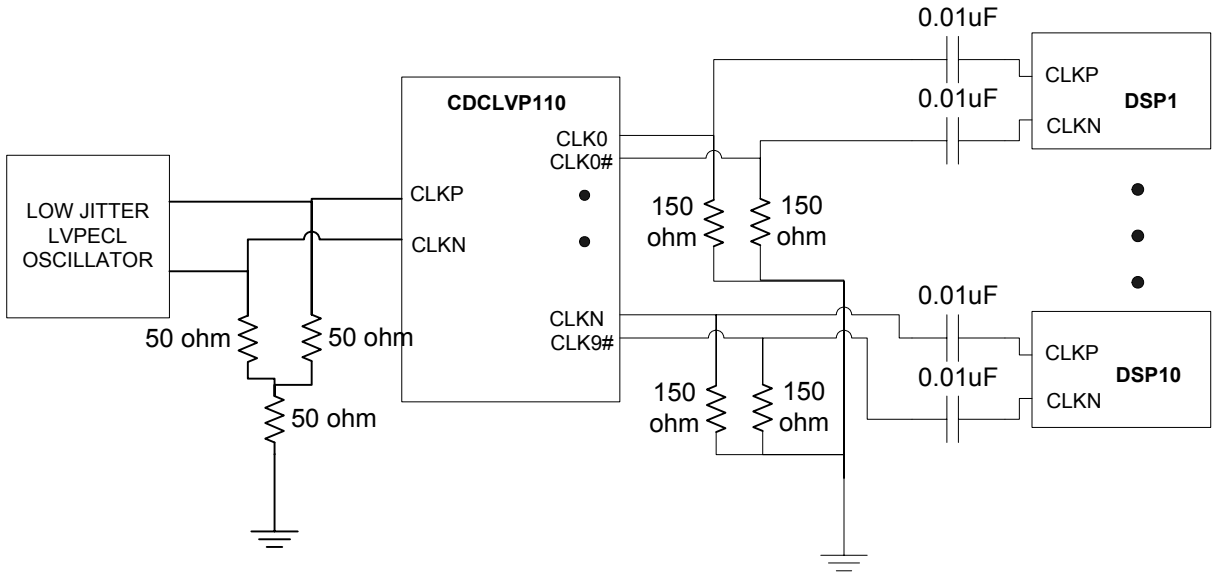
- TI SN65LVDS108 LVDS 1:8 clock fanout buffer
  - TI data sheet SLLS399, *SN65LVDS108 8-Port LVDS Repeater*
  - See Figure 6

Figure 6 Multiple Devices LVDS Clock Solution



- TI CDCLVP110 LVPECL 2:10 clock fanout buffer
  - TI data sheet SCAS683, *CDCLVP110 Low-voltage 1:10 LVPECL/HSTL With Selectable Input Clock Driver*
  - See Figure 7.

Figure 7 RIOCLK Multiple Devices LVPECL Clock Solution

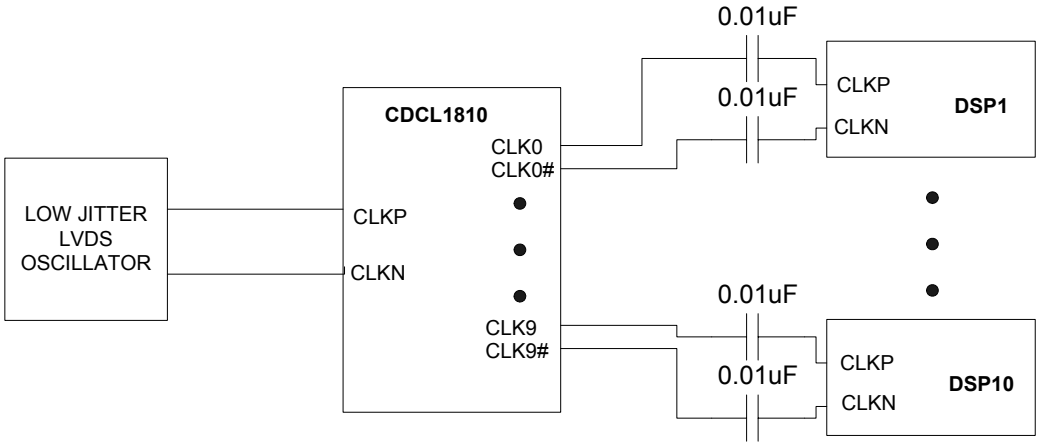


There are also 4-port and 16-port versions of the SN65LVDS108.

Texas Instruments also has a 1.8-V fanout buffer that includes some options for providing divided-down outputs. This is:

- TI CDCL1810 1:10 clock fanout buffer
  - New Product: see TI representative for details and availability
  - TI data sheet SLLS781, *CDCL1810 1.8V, 10 Output, High-Performance Clock Distributor*
  - See Figure 8.

Figure 8 Multiple Devices 1.8V LVDS Clock Solution



These buffers have not been tested but are examples of buffers that meet the specification requirements for all of the DSP differential clock inputs.

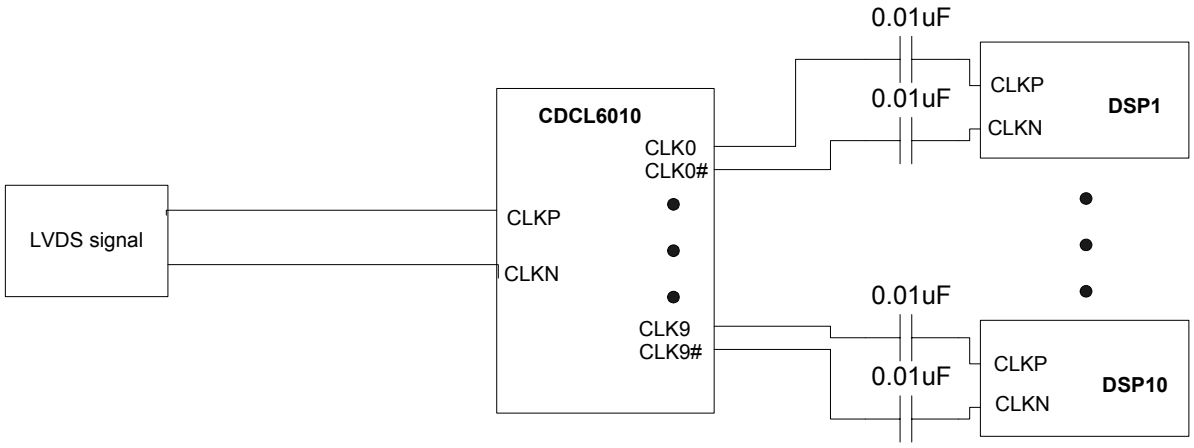
Jitter performance for the SN65LVDS108 is found in its data sheet. For the CDCLVP110, jitter characteristics can be found in TI application report SCAA068, *Advantage of Using TI's Lowest Jitter Differential Clock Buffer*.

The fanout buffer outputs should not be used to drive additional fanout buffers because the jitter will accumulate.

4.1.3.2 CDCL6010-Based Solutions (Jitter Cleaning)

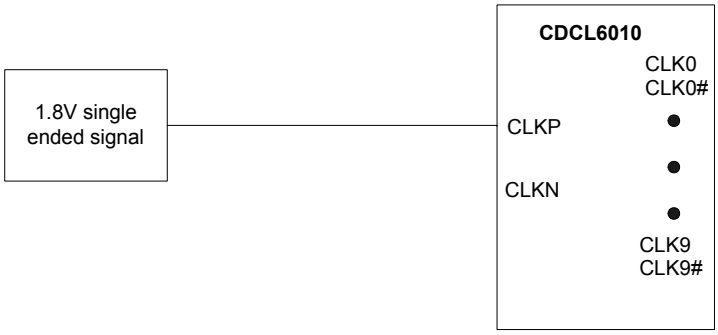
The CDCL6010 is a jitter cleaner and 1:10 fanout buffer that is well suited for use with the TMS320TCI6484 and TMS320C6457 DSPs. It operates from 1.8 V and meets the jitter requirements for all differential clock inputs on the device. An example of the connections when using an LVDS signal as the source is shown in Figure 9.

Figure 9 CDCL6010 Solution with LVDS Input



The connection of a single-ended input clock to CDCL6010 is shown in Figure 10. This source could be a 1.8-V source or, using a voltage divider, a 3.3-V source such as the CDCE706 or the CDCE906. TI application report SCAA080, *CDCx706/x906 Termination and Signal Integrity Guidelines* describes the interface between the CDCE706/CDCE906 and the CDCL6010 in detail.

Figure 10 CDCL6010 with Single-Ended Input



4.1.4 Layout Recommendations (LVDS and LVPECL)

4.1.4.1 Placement

- The oscillator, buffer, and DSPs should be placed as close to each other as practical.
- Fanout buffers should be placed in a central area to equalize the trace lengths to each DSP.
- AC coupling capacitors should be placed near the receivers.
- 50-Ω resistors used in LVPECL DC termination should be placed near the receiver.
- 150-Ω resistors used in LVPECL AC termination should be placed near the driver.

4.1.4.2 Trace Routing

- A GND plane should be placed below the oscillator.
- Digital signals should not be routed near or under the clock sources.
- Traces should be 100-Ω differential impedance and 50-Ω single-ended impedance.
- Clock traces should be routed as differential pairs with no more than two vias per connection (not counting pin escapes).
- The number of vias on each side of a differential pair should match.
- Differential clock traces must be matched in length to within 10 mils.
- Maintain at least 25-mil spacing to other traces.

4.2 Non-PLL Reference Clock Solutions

There are several peripherals that use reference clock inputs for operation. These, and their clocks, are:

- *EMIF64:* AECLKIN
- *UTOPIA:* UXCLK, URCLK
- *McBSP:* CLKS0, CLKS1
- *Timers:* TIMI0, TIMI1

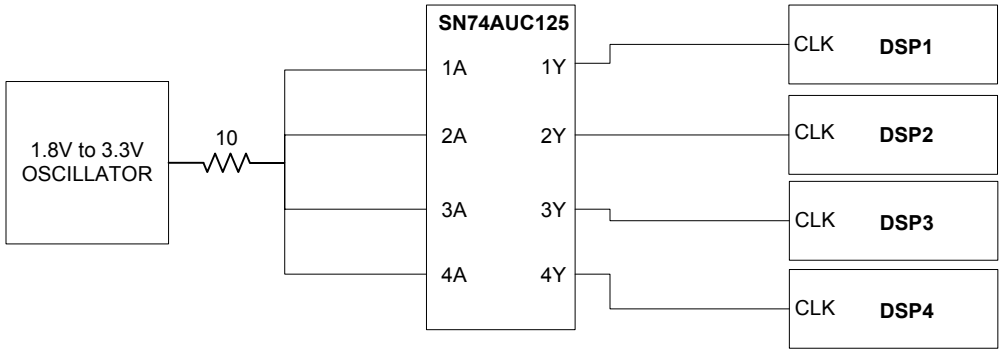
Table 3 shows all single-ended clocks with 1.8-V LVCMOS inputs. The specific requirements for these clocks are also shown in Table 2. Use of standard oscillators and buffers should be adequate for these clocks with the exception that they do require 1.8-V operation.

Table 3 Non-PLL Clock Requirements

Clock	Logic	Input Jitter	Duty Cycle	Stability	Frequency Range
AECLKIN	3.3-V LVCMOS	2.5% of input clock period	40/60%	Not specified	DC to 100 MHz
UXCLK, URCLK (UTOPIA)	3.3-V LVCMOS	2.5% of input clock period	40/60%	Not specified	DC to 50 MHz
CLKS0, CLKS1(McBSP)	1.8-V LVCMOS	Not specified	Not specified	Not specified	DC to 120 MHz
TIMI0, TIMI1(Timer)	1.8-V LVCMOS	Not specified	Not specified	Not specified	DC to 50 MHz
End of Table 3					

There are some 1.8-V LVCMOS oscillators and 1.8-V 1:N clock buffers available, although the selection is limited. One alternative is to have an oscillator supply multiple loads of a standard buffer. Typically oscillators are rated to drive 15-pF loads. The TI AUC buffers are typically rated around 3 pF per input, so an oscillator could drive five inputs of an AUC part. Because the AUC parts are 3.3-V tolerant, a standard 3.3-V oscillator could be used. See Figure 11 for one example of a solution.

Figure 11 LVCMOS Clock Buffer

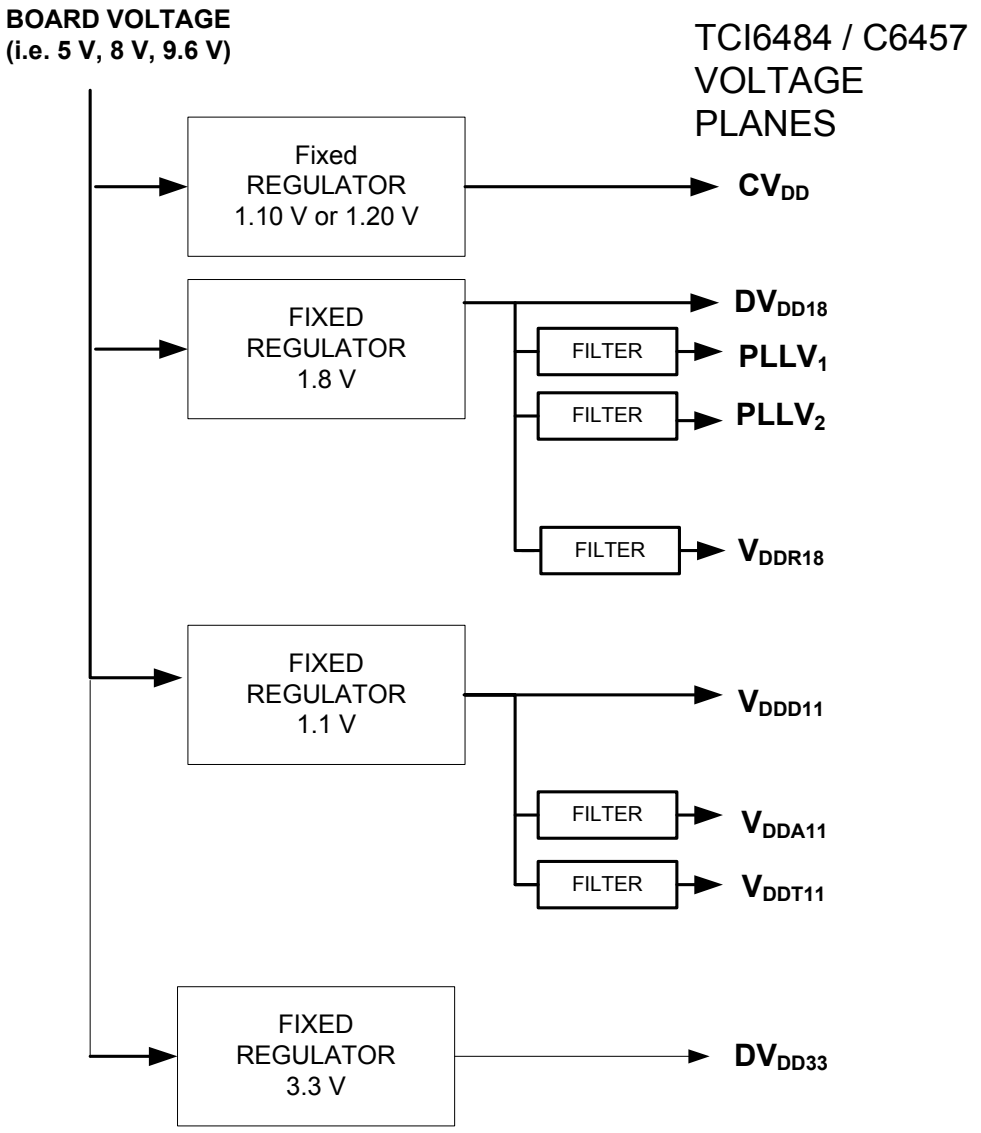


5 Power Supplies

5.1 Power Plane Generation

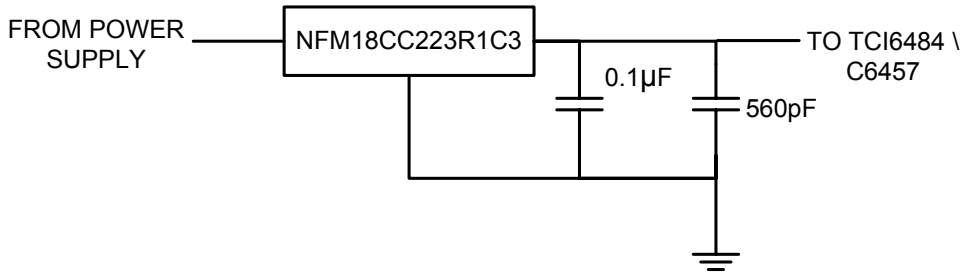
All power supplies may be generated from switching supplies. Filters are recommended for some power supplies. An overview of the recommended power supply generation architecture is shown in Figure 12. Additional information can be found in the TI application report SCAA048, *Filtering Techniques: Isolating Analog and Digital Power Supplies in TI's PLL-Based CDC Devices.*

Figure 12 TMS320TCI6484 and TMS320C6457 DSP Power Supplies



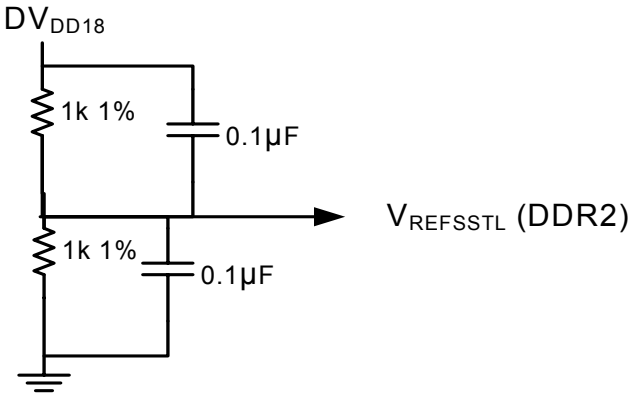
The recommended EMI filter circuit from Murata is shown in Figure 13. If the peripheral associated with the power supply is not used, it still needs to be powered but the filters are not required.

Figure 13 Recommended Power Supply Filter



A reference voltage is needed for the SSTL (DDR2) interface. This can be done through a simple voltage divider as shown in Figure 14. See Section 5.4 for additional details.

Figure 14 VREFSSTL Reference Voltage



5.2 Power Supply Sequencing

The required power supply sequence is defined by the following steps:

1. DV_{DD18}, $PLLV_1$, $PLLV_2$, and V_{DDR18} simultaneously ramp within 5 ms of each other
2. CV_{DD}, DV_{DD11}, V_{DDA11}, and V_{DDT11} simultaneously ramp within 5 ms of each other
3. DV_{DD33} ramps

100 µs after DV_{DD33} is stable, the $\overline{POR}$ signal can be brought high and device execution can begin.

The delay between steps should be a minimum of 500 µs and a maximum of 200 milliseconds.

See the device data manual for more details.

5.3 Voltage Plane Power Requirements

Power requirements are highly dependent on the usage of the device. This includes core voltage and operating frequency selected, peripheral utilization and case temperature. Table 4 shows estimated power numbers for a typical Pico Base Station system. The example was derived using the *Power Consumption Summary* application report and power spreadsheet.

Note—It is recommended that all system designers use the power spreadsheet to estimate their system power usage prior to designing a power distrubution system.

Depending on the specific design and usage, the worse-case transient conditions should be taken into account when evaluating power supplies and associated capacitors (Section 5.6.1 and Section 5.6.2). Designs outside of the approximate maximum values should re-examine power supply selection and design layout. These values should not be used to estimate thermal performance.

Table 4 Estimated Power Usage for a Typical Pico Base Station System Scenario[1]

Power Signal	Voltage	Estimated Power Usage	Peripheral Utilization[2]
CV_{DD}	1.1 V	2309.13 mW	• CPU Frequency - 1.0 GHz • CPU Utilization - 50%
DV_{DD33}	3.3 V	212.97 mW	• EMIFA Frequency - 100 MHz, EMIFA Utilization - 50%, EMIFA Switching - 50% • HPI Frequency - 50 MHz, HPI Utilization - 30%, HPI Switching - 50% • UTOPIA - Disabled
DV_{DD18}	1.8 V	363.93 mW	• DDR2 Frequency - 250 MHz, DDR2 Utilization - 60%, DDR2 Switching - 50% • McBSP0 - Disabled • McBSP1 - Disabled • SRIO Mode- 3 x1 lanes at 3.125 Gbps, SRIO Utilization - 15% • EMAC - Disabled
DV_{DD11}	1.1 V	377.28 mW	• SRIO Mode- 3 x1 lanes at 3.125 Gbps, SRIO Utilization - 15% • EMAC - Disabled
Total		3263.31 mW	
End of Table 4			

1. Please see the Power Spreadsheet and Application Report for more details about specific use-conditions and peripheral utilization termonology.
2. Many peripherals, such as SRIO and EMAC are powered from multiple voltage nets so their usage is noted under all applicable supplies

5.4 Power Supply Layout Recommendations

Core and I/O supply voltage regulators should be located close to the DSP device (or device array) to minimize inductance and resistance in the power delivery path. In addition, when designing for high-performance applications using the TMS320TCI6484 or TMS320C6457 DSPs platforms, the PCB should include separate power planes for core, I/O, and ground, all bypassed with high-quality, low-ESL/ESR capacitors.

For $V_{REFSSTL}$, one reference voltage divider should be used for both the DSPand the reference voltage input on the DDR-SDRAMs. The VREF resistor divider should be placed between the two devices and the routes made as directly as possible with a minimum 20-mil-wide trace. There should be a 2× trace width clearance between the routing of the reference voltage and any switching signals.

5.5 Voltage Tolerances, Noise, and Transients

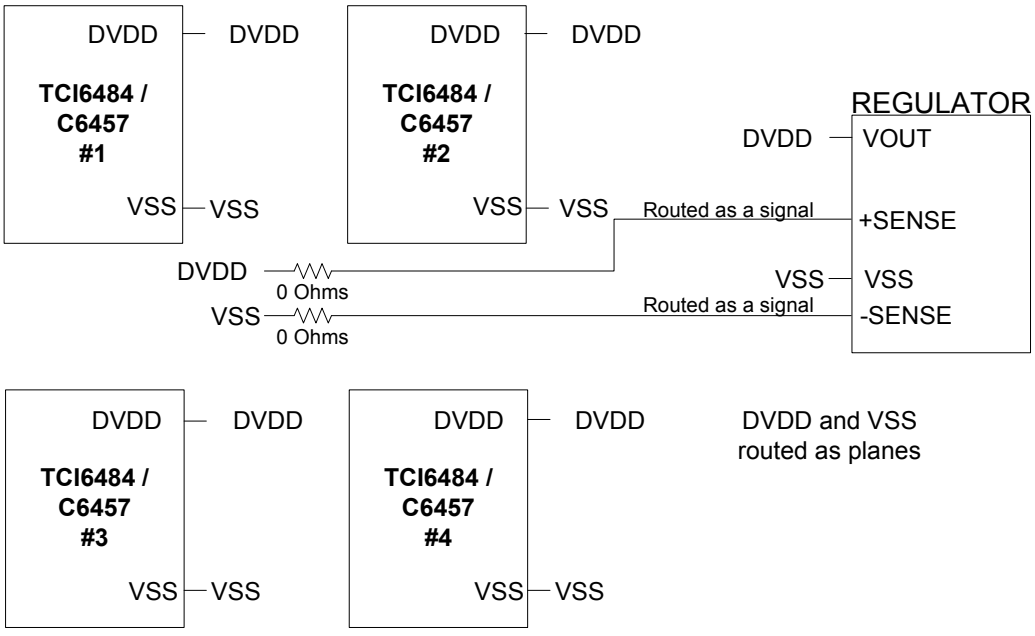
The voltage tolerances specified in the data manual include all DC tolerances and the transient response of the power supply. These specify the absolute maximum and minimum levels that must be maintained at the pins of the DSP device under all conditions. Special attention to the power supply solution is needed to achieve this level of performance, especially the 3% tolerance on the core power plane (CV_{DD}).

To maintain the 3% tolerance at the pins, the tolerance must be a combination of the power supply DC output accuracy and the effect of transients. A reasonable goal for the DC power supply output accuracy is 1.5%, leaving 1.5% for the transients. At a nominal 1.1-V CVDD, 3% tolerance is +/-33 mV. This allows 16.5 mV of DC accuracy from the output of the power supply and another 16.5 mV due to transients.

5.5.1 Using Remote Sense Power Supplies

Use of a power supply that supports the remote sense capability allows the power supply to control the voltage at the load. Special layout care must be used to keep this sense trace from being lost during PCB layout. One solution is placement of a small resistor at the load and connecting the sense trace to the voltage plane through it. If a power plane is shared by a group of DSP devices, the sense resistor should be placed at the center of this group. If a negative sense pin is supported by the voltage regulator, it should be handled in a similar way. An example of this type of implementation is shown in Figure 15.

Figure 15 Multiple DSP Remote Sense Connections



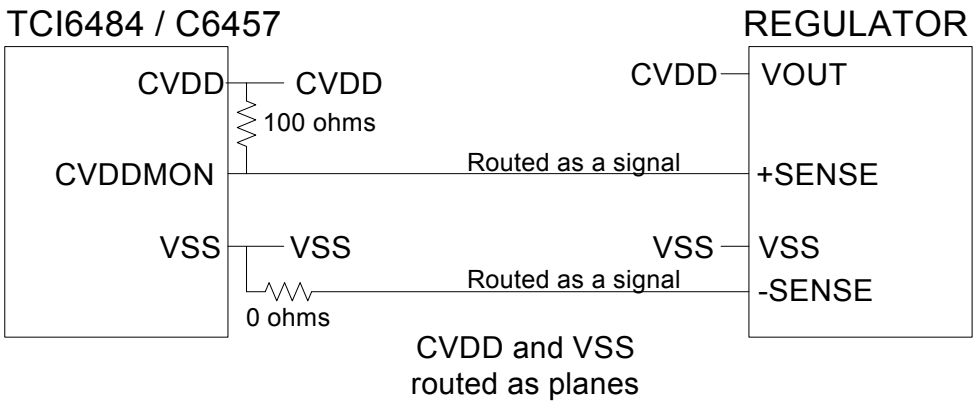
If the connection is between one DSP device and one voltage regulator, there are voltage monitor pins that can be used for this case (CVDDMON, DVDD18MON, and DVDD33MON). The monitor pins indicate the voltage on the die and therefore provide the best remote sense voltage. These monitor pins should be connected directly to the positive side sense pin of the voltage regulator.

Note—If the monitor pins are not used to monitor the voltage, they should be connected to their respective power planes (i.e. CVDDMON connects to CVDD, DVDD18MON connects to DVDD18, and DVDD33MON connects to DVDD33).

The voltage regulator output could become unstable and drive to a high voltage if the positive sense line does not receive the correct voltage. Some voltage regulators (i.e. the TI PTH08T240F) include a low impedance path between the VOUT and +SENSE so that this would result only in a small drop in performance. If this feature is not present in the voltage regulator, it is recommended to place a 100-Ω resistor near the DSP between the voltage plane and the monitor pin.

If the VDD monitor connection to the DSP (i.e. CVDDMON) is not present for some reason, the positive sense will still regulate to the proper voltage. If a negative sense pin is provided by the regulator this should be connected to the GND plane near the DSP using a 0-Ω resistor. The single DSP remote sense connections are shown in Figure 16 for the CVDD plane. The same solution could be used for all/any planes.

Figure 16 Single DSP Remote Sense Connections



5.5.2 Voltage Plane IR Drop

The voltage gradient (IR drop) needs to be considered whether or not a supply with the remote sense capability is used. The DSPs closer to the supply will have a slightly higher voltage and the DSPs farther from the supply will have a slightly lower voltage. This voltage differential can be minimized by making the copper planes thicker or by spacing the DSPs across a wider area of the plane. Be sure to consider both the core power plane(s) and the ground plane(s). The resistance of the plane can be determined by the following formula:

$$R = \text{rho} \times \text{length} \div (\text{width} \times \text{thickness})$$

where rho is the resistivity of copper equal to 1.72^{-8} Ω-meters. PCB layer thickness is normally stated in *ounces*. One ounce of copper is about 0.012 inches or 30.5^{-6} meters thick. The width must be derated to account for vias and other obstructions. A 50-mm wide strip of 1-oz copper plane derated 50% for vias will have a resistance of 0.57 mΩ per inch.

5.6 Power-Supply Decoupling and Bulk Capacitors

In order to properly decouple the supply planes from system noise, decoupling and bulk capacitors are required.

Considering current technology, 0402-sized capacitors should be used for standard decouplers where possible. Proper board design and layout should allow for correct placement of all capacitors (see Table 5 for capacitor recommendations and values).

Generically speaking, bulk capacitors are used to minimize the effects of low frequency current transients (see Section 5.6.1) and decoupling or bypass capacitors are used to minimize higher frequency noise (see Section 5.6.2). Proper printed circuit board design is required to ensure functionality and performance.

One key element to consider during the circuit board (target) design is added lead inductance or the pad-to-plane length. Attachment for decoupler and bypass capacitors to the respective power planes should be made (where possible) using multiple vias in each pad that connects the pad to the respective plane. The inductance of the via connect can reduce or eliminate the effectiveness of the capacitor so proper via connections are important. Trace length from the pad to the via should be no more than 10 mils (0.01 inch) and the width of the trace should be the same width as the pad.

As with selection of any component, verification of capacitor availability over the product's production lifetime should be considered. In addition, the effects of the intended operating environment (temperature, humidity) should also be considered when selecting the appropriate decoupling and bulk capacitors.

Note—All values and recommendations are based on a single TMS320TCI6484 or TMS320C6457 DSP device and the use of recommended on board power supply modules, alternate power supplies and decoupling/bulk capacitor values will require additional evaluation.

A capacitor selection spreadsheet and user application note (TBD) is available to assist in determining the minimal amount of bulk and decoupling capacitance required (for use with the PTH08T240Fxx module only)

5.6.1 Selecting Bulk Capacitance

There are two factors that need to be considered when selecting the bulk capacitance:

- Effective impedance for the power plane to stay within the voltage tolerance
- Amount of capacitance needed to provide power during the entire period when the voltage regulator cannot respond (sometimes referred to as the transient period)

The effective impedance of the core power plane is determined by:

(Allowable Voltage Deviation due to Current Transients) ÷ (Max Current)

In "Voltage Tolerances, Noise, and Transients" on page 1-18, it was suggested that the allowable voltage deviation due to transient response is 16.5 mV (based on 1.5% of a CVDD set to 1.1 V). Using this 16.5 mV value and a maximum current of 3 amps, the maximum allowable impedance can be calculated: 16.5 mV ÷ 3 Amps = 5 mΩ

The effective ESR of the bulk capacitors should not exceed this impedance value. Multiple bulk capacitors in parallel will help achieve this overall ESR. Therefore, to achieve a maximum transient voltage peak deviation of 16.5 mV, the power supply output impedance, which is a function of the power supply bandwidth and the low impedance output capacitance, should not exceed 5 mΩ.

The expected maximum current change for the DSP device CVDD power net is on the order of 5-10 A/s. This current value assumes a transient from a device operating with a minimal activity and no peripheral usage to a worst case power condition. It does not include current transients that occur during power-on. Care should be taken during power-on that the device does not transition from the OFF state to a max power state faster than 100 ms. TI has tested the PTH08T240F power module (which has been optimized for the TMS320TCI6484 and TMS320C6457 DSP devices) and currently recommends the use of approximately 3000 µF of low-ESR capacitance (see Section 5.6.3).

Capacitance values shall not be less then those specified in Section 5.6.3. Final capacitor selection shall be determined using the capacitor selection tool (TBD).

This covers both the output capacitance requirements of the module and the bulk capacitance needs for the DSP device. TI has also tested an optimized SWIFT TPS54010-based solution that requires a similar amount of capacitance. Other regulator solutions should be analyzed, and, if possible, tested in a lab environment to determine the optimal output capacitance.

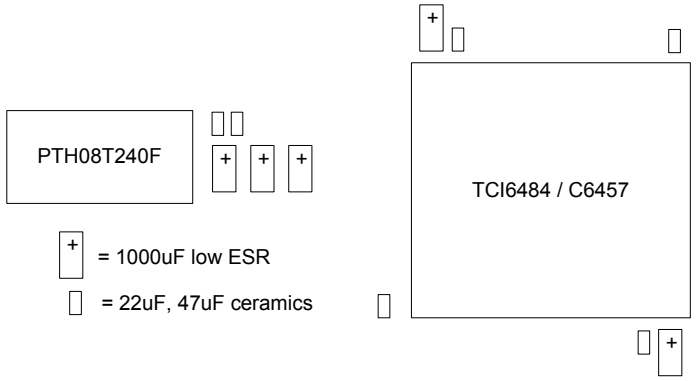
Some intermediate-size ceramic bulk capacitors (i.e. 22 µF and 47 µF) as listed in Section 5.6.3 are recommended to cover the response time between the bypass capacitors and the larger bulk capacitors.

5.6.1.1 Bulk Capacitor Details and Placement

Bulk capacitors should be placed in close proximity to the power supply module. For the purpose of this document and related devices, a bulk capacitor should be defined as any capacitor ≥ 22 µF, unless otherwise noted.

Figure 17 shows an example of the bulk capacitor placement assuming the use of the recommended PTH08T240F module and the capacitance recommendations from Table 5.

Figure 17 Bulk Capacitor Placement



Each bulk capacitor should have reduced trace lengths less than 10 mils and contain multiple vias to tie the pad to the respective power plane. It is recommended that all bulk capacitors be low-ESR types. The acceptability of each output capacitor should be based on the following criteria:

$$1000 < \text{capacitance} \times \text{ESR} \leq 5000$$

5.6.2 Selecting Decoupling Capacitors

All decoupling or bypass capacitors need to be close to the DSP device. In practice, they should be within 1.25 cm maximum distance to be effective. Ideally, these capacitors should be connected directly to the via attached to the BGA power pin. The parasitic inductance of a capacitor's package limits the effectiveness of the decoupling capacitor; therefore the physically smaller 0402 capacitors are recommended to reduce parasitic inductances introduced by larger package sizes.

Proper capacitance values are also important. Small bypass capacitors (approximately 560 pF) should be placed *closest* to the power pins on the target DSP device. Medium bypass capacitors (100 nF or as large as can be obtained in a small package such as an 0402) should be the next closest. TI recommends placing decoupling capacitors immediately next to the BGA vias, using the *interior* BGA space and at least the corners of the exterior.

The inductance of the via connect can reduce or eliminate the effectiveness of the capacitor so proper via connections are important. Trace length from the pad to the via should be no more than 10 mils and the width of the trace should be the same width as the pad. If necessary, placing decoupler capacitors on the back side of the board is acceptable provided the placement and attachment is designed correctly.

5.6.2.1 Decoupling Capacitor Details and Placement

All decoupling capacitors should be placed in close proximity to the DSP device. For the purpose of this document and related devices, a decoupler or bypass capacitor shall be defined as any capacitor < 22 µF unless otherwise noted.

See Table 5 for recommended decoupler capacitor values. Each decoupler or bypass capacitor should be directly coupled to the DSP via. Where direct coupling is impractical, use of a 10-mil (0.010-inch / 0.254-mm) or shorter trace, and having the same width as the capacitor pad is strongly recommended.

5.6.3 Example Capacitance

An example of an adequate capacitor selection is shown in Table 5. This is the capacitance that should be dedicated to the DSP device and does not cover the decoupling needed for any other components or for the filters outlined in Section 5.1 on page 15. The bulk capacitance recommendation assumes the use of the PTH08T240F power module. Power modules that do not support a Turbo-Trans type of feature may require additional output capacitance as their effective bandwidth may be more limited.

Table 5 Bulk and Bypass Capacitor Recommendations

Voltage Supply	Capacitors	Total Capacitance	Description
CV_{DD}	• 10 × 560 pF • 20 × 100 nF • 3 × 22 µF (ceramic) • 3 × 47 µF (ceramic) • 2 × 1000 µF (low ESR)	2209 µF	Scalable Core
V_{DDD11}	• 4 × 560 pF • 6 × 100 nF • 2 × 10 µF (ceramic)	20 µF	Fixed 1.1 V
DV_{DD18}	• 10 × 560 pF • 20 × 100 nF • 1 × 22 µF (ceramic) • 1 × 330 µF	352 µF	1.8-V I/O
DV_{DD33}	• 10 × 560 pF • 20 × 100 nF • 1 × 22 µF (ceramic) • 1 × 330 µF	352 µF	3.3-V I/O
End of Table 5			

Final CV_{DD} capacitor value shall not be less then the value specified in Table 5, Final selection shall be determined using the capacitor selection tool, (TBD), which takes into account the board impedance, variation in the CV_{DD} supply voltage and the ESR of the bulk and decoupling capacitors selected.

5.7 Power Saving Options

5.7.1 Clock Gating Unused Peripherals

The TMS320TCI6484 and TMS320C6457 DSPs can place inactive/unused peripherals into a low-power state. This capability is discussed in the device data manual. After power-up, only those peripherals that are needed should be left enabled.

5.7.2 General Power Saving Techniques

The following are some additional methods for reducing power:

- Lower frequency operation means lower power. The core and peripherals should be operated at the lowest frequency that meets the user requirements and the device requirements.
- SERDES link power does not scale linearly with data rate. SRIO and EMAC ports with higher link rates have a higher bandwidth/watt than slower links. Generally, running fewer high speed links is more power efficient than multiple slower links.

6 I/O Buffers

6.1 PTV Compensated Buffers

The impedance of I/O buffers is affected by process, temperature, and voltage. For the DDR interface, these impedance changes can make it difficult to meet specifications across the full range of these parameters. For that reason, the TMS320TCI6484 and TMS320C6457 DSPs use PTV-(process, temperature, voltage) compensated I/O buffers for the DDR interface. The PTV compensation works by adjusting internal impedances to nominal values based on an external reference resistance. This is implemented by connecting a resistor between the PTV18 pin and VSS. See the *DDR2 Implementation Guidelines* application report for details.

6.2 I/O Timings

The I/O timings in the TMS320TCI6484 and TMS320C6457 DSP data manuals are given for the tester test load. These timings need to be adjusted based on the actual board topology. It is highly recommended that timing for all high speed interfaces (with the exception of DDR-based and SERDES-based interfaces) on a TMS320TCI6484 or TMS320C6457 design be checked using IBIS simulations. For more details on performing IBIS simulations, see TI application report SPRA839, *Using IBIS Modes for Timing Analysis*.

6.3 External Terminators

Series impedance is not always needed but is recommended for some interfaces to avoid over-shoot/under-shoot problems. Check the recommendations in the Peripherals chapters and/or perform IBIS simulations on the interface.

6.4 Signaling Standards

6.4.1 1.8-V LVCMOS

All LVCMOS I/O buffers are JEDECcompliant 1.8-V LVMOS I/Os as defined in JEDEC standard JESD8-5A-01, *2.5 V ± 0.2 V (Normal Range) and 1.8 V – 2.7 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits*.

There are several different LVCMOS buffers used in the DSP device. The differences are mainly whether an internal pull-up or internal pull-down is implemented. There are also some differences in the drive strength for some I/Os. See the device data manual for details on different LVCMOS buffer types.

Some LVCMOS I/Os include internal pullups or pulldowns. These internal pullups and pulldowns can be considered a 100-µA current source (with a range of 45 µA to 170 µA). This equates to a nominal pullup/pulldown resistor of 18 kΩ (with a possible range of 10 kΩ to 42 kΩ)

The 1.8-V LVCMOS interfaces are not 2.5-V or 3.3-V tolerant so connections to 2.5-V or 3.3-V CMOS logic require voltage translation. For input buffers at moderate frequencies, the TI LVC logic family can be operated at 1.8 V and is 3.3-V tolerant. For faster signaling, the TI AUC family is optimized to operate at 1.8 V and is also 3.3-V tolerant. Good options for voltage translation for 1.8-V outputs that need to drive 2.5 V or higher inputs would be the CBTLV family (for a non-buffered solution) or the AVC family (for a buffered solution).

Some useful TI application notes on voltage translation options can be found in:

- TI application report SCEA030, *Voltage Translation Between 3.3-V, 2.5-V, 1.8-V, and 1.5-V Logic Standards With the TI AVCA164245 and AVCB164245 Dual-Supply Bus-Translating Transceivers*
- TI application report SCEA035, *Selecting the Right Level-Translation Solution*.

6.4.2 3.3V LVCMOS

All LVCMOS I/O buffers are JEDEC-compliant 3.3-V LVMOS I/Os as defined in JEDEC standard JESD8-5A-01, *2.5 V ± 0.2 V (Normal Range) and 1.8 V – 2.7 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits*.

There are several different LVCMOS buffers used in the DSP device. The differences are mainly whether an internal pullup or internal pulldown is implemented. There are also some differences in the drive strength for some I/Os. See the device data manual for details on different LVCMOS buffer types.

If ***NO*** 3.3-V LVCMOS IOs (peripherals) are used, the 3.3-V power supply can be omitted if the 3.3-V IOs are pulled up to the DVDD 1.8-V power rail. Please note that pulling these IOs to 1.8 V can create a worst-case leakage of 100 µA per pin for each of the 3.3-V IO pins that are pulled up to 1.8 V. This should be taken into consideration when calculating power requirements for the DVDD 1.8-V power rail.

6.4.3 SSTL

The DDR2 interface is compatible with JEDEC standard JESD8-15A, *Stub Series Terminated Logic for 1.8 V (SSTL_18)*. The I/O buffers are optimized for use with direct connections to up to two DDR2 SDRAMs and are not intended to drive DDR2 DIMM modules. It is not intended that external parallel terminations be used with the DDR2 I/Os, but both series resistors and/or ODT (on-die-terminations) are supported. See the *DDR2 Implementation Guidelines* application report for more details.

6.4.4 SERDES Interfaces

There are two peripherals on the DSP device that use high-speed serial interfaces: SGMII (EMAC) and Serial RapidIO (SRIO). These serial interfaces all use 8b/10b encoded links and SERDES (serializer/deserializer) macros. These interfaces use a clock recovery mechanism so that a separate clock is not needed. Each link is a serial stream with an embedded clock so there are no AC timings or drive strengths like those found in the LVCMOS or SSTL interfaces. There are several programmable settings for each SERDES interface that affect the electrical signaling. The most important of these are:

- Transmitter output amplitude
- Transmitter de-emphasis
- Receiver adaptive equalization

Recommendations for these settings for particular board topologies appear in the *SERDES Implementation Guidelines* application report.

The SERDES interfaces use CML logic. Compatibility to LVDS signals may be possible and is described in Section 7.12.

7 Peripherals

This section covers each of the TMS320TCI6484 and TMS320C6457 DSP peripherals/modules. This section is intended to be used in addition to the information provided in the device data manual, the peripheral specific user's guides provided for each of the peripherals, and relevant application reports. The four types of documents should be used as follows:

- *Data manual:* AC timings, register offsets
- *User Guide:* functional description, programming guide
- *Application reports:* system-level issues
- *This chapter:* configuration, system-level issues not covered in a separate application report

Each peripheral section includes recommendations on how to handle pins on interfaces that are disabled or for unused pins on interfaces that are enabled. Generally, if internal pullups or pulldowns are included, the pins can be left floating. Any pin that is output-only can always be floating. If internal pullups and pulldowns are not included, normally pins can still be floating with no functional issues for the device.

However, this normally does cause additional leakage currents that can be eliminated if external pullups or pulldowns are used. Inputs that are not floating have a leakage current of approximately 100 μA per pin. Leakage current is the same for a high or low input (either pullups or pulldowns can be used). When the pins are floating, the leakage can be several mA per pin. Connections directly to power or ground can be used only if the pins can be guaranteed to never be configured as outputs and boundary scan is not run on those pins.

7.1 Multichannel Buffered Serial Port (McBSP0 and McBSP1)

Relevant documentation for McBSP can be found in the product folder.

- *DSP Multichannel Buffered Serial Port (McBSP)* reference guide

Note—Will require some changes for device-specific differences

- IBIS model file
- TI application report SPRA839, *Using IBIS Modes for Timing Analysis*

7.1.1 Configuration of McBSP

McBSP0 and McBSP1 are not multiplexed with any other peripherals and are enabled after power up.

Each McBSP port can be driven by either an external clock (CLKS), by an internal CLKS, or by the internal sample rate generator in the McBSP. The internal CLKS clock rate is core clock ÷ X, where X is programmable from 6 to 32. Default is X = 10. CLKS (either sourced internally or externally) cannot exceed 104.448 MHz. The sample rate generator clock rate is core clock ÷ 6 and can be further divided down inside the McBSP module. Please note that if this clock is used, it must be divided down at least by 2.

If a McBSP port is not used or some of the signals are not used, the pins can be left unconnected because internal pullups/downs are included. The CLKS also has an internal pulldown so that it may be left unconnected if not used.

All standard McBSP modes are supported including the SPI mode.

7.1.2 System Implementation of McBSP

The maximum McBSP performance is achievable only when using source synchronous modes and point-to-point connections. In this case, series resistance should be used to reduce over/under-shoot. Generally acceptable values are 10 Ω, 22 Ω, or 33 Ω. To determine the optimum value, simulations using the IBIS models should be performed to check signal integrity and AC timings.

Multiple DSPs can be connected to a common McBSP bus using TDM mode. The additional loads will require a reduction in the operating frequency. Also, the specific routing topology becomes much more significant as additional DSPs are included. The way to determine the best topology and maximum operating frequency are by performing IBIS simulations.

7.2 GPIO/Device Interrupts

Documentation for GPIO/Interrupts can be found in the product folder.

- *DSP General-Purpose Input/Output (GPIO)* user's guide

Note—May require some changes for device-specific differences

- IBIS model file
- TI application report SPRA839, *Using IBIS Modes for Timing Analysis*

7.2.1 Configuration of GPIO/Interrupts

All of the GPIOs are used for device configuration strapping options. The strapping options are latched by $\overline{\text{POR}}$ going high. After $\overline{\text{POR}}$ is high, the pins are available as GPIO pins.

GPIOs are enabled at power-up and default to inputs.

All GPIOs can be used as interrupts and/or EDMA events to any of the cores.

All GPIOs have internal pulldowns except GPIO4, which has an internal pullup. Because the internal pullups and pulldowns are present, the pins can be no-connects if not used. If the opposite configuration setting is desired, an external 1-kΩ resistor should be used to overcome the internal pullup/down.

7.2.2 System Implementation of GPIO/Interrupts

It is recommended that GPIOs used as outputs have a series resistance (22 Ω or 33 Ω being typical values). The value (or need) for the series resistor can be determined by simulating with the IBIS models.

If it is desired to have a GPIO input default to a particular state (low or high), an external resistor should be used. A pullup value of 1 kΩ is recommended to make sure that it overrides the internal pulldown present on some GPIO pins. If this GPIO is also used as a strapping option, the default state needs to also be the desired boot strapping option. The $\overline{\text{RESETSTAT}}$ signal can be used to place the logic that drives a GPIO boot strapping state during the $\overline{\text{POR}}$ transition into a Hi-Z state.

7.3 Timers (Timer0 and Timer1)

Documentation for timers can be found in the product folder.

- *DSP 64-Bit Timer* user's guide

Note—May require some changes for device-specific differences

- *DSP CPU and Instruction Set* reference guide
- IBIS model file
- TI application report SPRA839, *Using IBIS Modes for Timing Analysis*

7.3.1 Configuration of Timers

There are six timer peripherals, and these are enabled at power-up.

Each timer can be configured as a single 64-bit timer or as two 32-bit timers or as a watch-dog timer. There are two external timer input signals and two external timer output signals. Each of the six timers can select either of the two timer input pins as a source, between two internal sources from the Frame Sync Module, or an internal clock, which is core clock ÷ 6. Each of the two timer output pins can be driven by any of the six timers.

When a timer is used as two 32-bit timers, the timer input and output can be used only with the lower 32-bit timer. When used as a watchdog timer, Timers 3, 4, and 5 correspond to CPU cores 0, 1, and 2, respectively. A watchdog timeout on any of these timers, when in watchdog mode, can optionally reset that particular CPU automatically.

The timer module is clocked from CPU core clock frequency ÷ 6.

If the external timer input signals are not used, the pins can be left unconnected and the internal pulldowns will bring the input to a low state.

In addition to the timer peripherals, each CPU core has a 64-bit free-running counter that advances each CPU clock after counting is enabled. The counter is accessed using two 32-bit read-only control registers in the CPU. For more details on this timer, see the Time Stamp Counter Registers described in the TI reference guide SPRU732, *TMS320C64x/C64x+ DSP CPU and Instruction Set*.

Timer inputs can optionally be used as general purpose inputs.

Timer outputs can optionally be used as general purpose outputs.

7.3.2 System Implementation of Timers

It is recommended that external timer signals use series resistance (22 Ω or 33 Ω being typical values). The value (or need) for the series resistor can be determined by simulating with the IBIS models.

External timer input signals are synchronized to the internal timer clock. Because the timer operates at CPU core ÷ 6, the timer input can be delayed from the timer input as much as one CPU core clock period × 6 (seconds).

7.4 Inter-Integrated Circuit (I^2C)

Documentation for I^2C can be found in the product folder.

- *Inter-Integrated Circuit (I^2C) Module User's Guide* user's guide
- IBIS model file
- TI application report SPRA839, *Using IBIS Modes for Timing Analysis*
- Philips Semiconductor document 39340011, *I^2C Bus Specification Version 2.1, January, 2000*

7.4.1 Configuration of I^2C

The I^2C peripheral powers up enabled. The input clock for the I^2C module is core clock ÷ 6. There is a prescaler in the I^2C module that needs to be set up to reduce this frequency to an internal module clock of 7 MHz to 12 MHz.

If the I^2C signals are not used, the SDA and SCL pins can be left floating. This does cause a slight increase in power due to leakage, which can be avoided by having pullup resistors.

7.4.2 System Implementation of I^2C

External pullup resistors to 1.8 V are needed on the I^2C signals (SCL, SDA). The recommended pullup value is 4.7 kΩ.

Multiple I^2C devices can be connected to the interface, but the speed may need to be reduced (400 kHz is the maximum) if many devices are connected.

The I^2C pins are not 2.5-V or 3.3-V tolerant. For connection to 2.5 V or 3.3 V I^2C peripherals, the PCA9306 can be used. See TI data sheet SCPS113, *PCA9306 Dual Bidirectional I^2C Bus And SMBus Voltage-level Translator.*

7.5 Ethernet (EMAC, SGMII, and MDIO)

Documentation for EMAC can be found in the product folder.

- *Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO)* user's guide

Note—Will require some changes for device-specific differences

- SGMII Specification (ENG-46158) Version 1.8, dated April 27, 2005
- *SERDES Hardware Design Guidelines* application report

7.5.1 Configuration of EMAC, SGMII, and MDIO

The EMAC interface is compliant with the SGMII v1.8 specification, which specifies LVDS signals. Only the data channels are implemented so the connected device must support clock recovery and not require a separate clock signal. When the EMAC is enabled the MDIO interface is enabled. The MDIO interface (MDCLK, MDIO) uses 1.8-V LVCMOS buffers.

The EMAC must be enabled via software before it can be accessed unless the Boot over Ethernet bootmode is selected.

If the EMAC is used, a RIOSGMIICLKP/N clock must be provided and the SERDES must be set up to generate a 1.25-Gbps link. The PLL multiplier settings for the three recommended RIOSGMIICLKP/N clock frequencies are shown in Table 6. Although the SGMII SERDES share a reference clock with the SRIO SERDES they have separate PLLs that can be set up with different multipliers.

Table 6 SGMII PLL Multiplier Settings

Reference Clock	PLL Multiplier	Full Rate	Half Rate	Quarter Rate
125 MHz	10	not used	1.25 Gbps	not used
156.25 MHz	8	not used	1.25 Gbps	not used
312.5 MHz	4	not used	1.25 Gbps	not used
End of Table 6				

If the EMAC is not used, the SERDES signals can be left unconnected. MDIO may be left unconnected but will result in an increase in leakage current. This can be avoided by adding an external pullup. If both EMAC and SRIO are not used, the RIOSGMIICLKP/N pins should be connected as shown in Figure 3 on page 1-8.

7.5.2 System Implementation of SGMII

SGMII specifies LVDS signaling as defined in IEEE Standard 1596.3-1996, *Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)*. The TCI6484 and C6457 uses a CML-based SERDES interface that requires AC-coupling to interface to LVDS levels. AC coupling capacitors (0.1 µF) are recommended for this purpose. The SERDES receiver includes an internal 100-Ω termination so an external 100-Ω termination is not needed. Examples of SERDES to LVDS connections are shown in Section 7.12.

If the connected SGMII device does not provide common-mode biasing, external components must be added to bias the LVDS-side of the AC-coupling capacitors to the nominal LVDS offset voltage (normally 1.2 V).

See the *SERDES Hardware Design Guidelines* application report for information regarding supported topologies and layout guidelines.

The SGMII interface supports hot-swap, where the AC-coupled inputs of the device may be driven without a supply voltage applied.

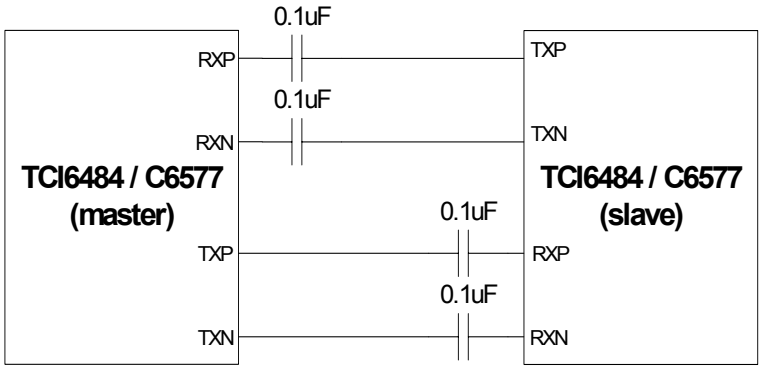
Suggestions on SGMII reference clocking solutions can be found in Section 4.1.

SRIO/SGMII SERDES power planes and power filtering requirements are covered in "5 Power Supplies" on page 1-15.

7.5.3 SGMII MAC to MAC connection

The SGMII interface can be connected from the DSP device to PHY or from the DSP device to MAC, including DSP device-to-DSP device direct connects. An example of the hardware connections is shown in Figure 18. For auto-negotiation purposes, the device can be configured as a master or a slave, or it can be set up for fixed configuration. If the device is connected to another MAC, the electrical compatibility must be evaluated to determine if additional terminations are needed.

Figure 18 SGMII MAC to MAC Connection



7.6 Serial Rapid I/O (SRIO)

Relevant documentation for SRIO can be found in the product folder.

- *Serial RapidIO (SRIO)* user's guide

Note—May require some changes for device-specific differences

- RapidIO Interconnect Specification Part VI
- *SERDES Hardware Design Guidelines* application report

7.6.1 Configuration of SRIO

SRIO defaults to disabled and with internal memories for the module in a sleep state. The memories, followed by the module, must be enabled by software before use (unless Boot over SRIO is selected).

There are four SRIO lanes. A simple form of SRIO forwarding is supported to allow a daisy-chain implementation.

The SRIO requires a differential reference clock: RIOSGMIICLKP/N. Supported frequencies for this clock are 125 MHz, 156.25 MHz, and 312.5 MHz. The SERDES (serializer/deserializer) used in the SRIO solution has a PLL that needs to be configured based on this reference clock and the desired link rate. Link rates can be full-, half-, or quarter-rate relative to the PLL frequency. See Table 7 for PLL multiplier settings relative to link rate.

Table 7 SRIO PLL Multiplier Settings

Reference Clock	PLL Multiplier	Full Rate	Half Rate	Quarter Rate
125 MHz	12.5	3.125 Gbps	not used	not used
156.25 MHz	10	3.125 Gbps	not used	not used
125 MHz	10	2.5 Gbps	1.25 Gbps	not used
156.25 MHz	8	2.5 Gbps	1.25 Gbps	not used
312.5 MHz	5	3.125 Gbps	not used	not used
312.5 MHz	4	2.5 Gbps	1.25 Gbps	not used
End of Table 7				

It is possible to configure the device to boot-load application code over the SRIO interface. Boot over SRIO is a feature that is selected using boot strapping options. For details on boot strapping options, see the device data manual.

If the SRIO peripheral is not used, the SRIO link pins can be left floating and the SERDES links should be left in the disabled state. If the SRIO and SGMII peripherals are both unused, the RIOSGMIICLKP/N can be left as a no-connect.

The SRIO SERDES ports supports hot-swap, where the AC-coupled inputs of the device may be driven without a supply voltage applied.

If the SRIO peripheral is enabled but only one link is used, the pins of the unused link can be left floating.

7.6.2 System Implementation of SRIO

The Serial RapidIO implementation is compliant to RapidIO Interconnect Specification Part VI.

See the *SERDES Hardware Design Guidelines* application report for information regarding supported topologies and layout guidelines

Suggestions on SRIO reference clocking solutions can be found in Section 4.1.

SRIO/SGMII SERDES power planes and power filtering requirements are covered in Section 5.

7.7 DDR2

Relevant documentation for DDR2 can be found in the product folder.

- *DSP DDR2 Memory Controller* user's guide

Note—May require some changes for device-specific differences

- *DDR2 Implementation Guidelines* application report
- JEDEC standard JESD79-2B, *DDR2 SDRAM Specification*

7.7.1 Configuration of DDR2

The DDR2 peripheral is enabled at power-up.

The DDR2 output clock is derived from the DDR PLL, which uses DDRREFCLKP/N as a reference clock. The DDR PLL outputs 10× the DDRREFCLKP/N frequency and the DDR output clock is ½ of the PLL output clock. For example, a 66.6 MHz reference clock results in a 667 MHz PLL output and a DDR output clock of 333 MHz for DDR2-667 support.

If the DDR2 peripheral is disabled, all interface signals (including reference clocks) can be left floating and the input buffers will be powered down.

If the DDR2 is operated in 16-bit mode, the upper DDR2 bi-directional pins should be pulled to valid states through 1-kΩ resistors. DDRDQS2, DDRDQS3, and DDRD[31:16] should have 1-kΩ pullup resistors to DVDD_18. $\overline{\text{DDRDQS2}}$ and $\overline{\text{DDRDQS3}}$ should have 1-kΩ pulldowns to GND. DDRDQM2, DDRDQM3, and DDRCLKOUT1P/N can be left unconnected.

7.7.2 System Implementation of DDR2

See *DDR2 Implementation Guidelines* application report for information regarding supported topologies and layout guidelines.

Suggestions on DDR reference clocking solutions can be found in Section 4.1.

7.8 JTAG / Emulation

Relevant documentation for JTAG/Emulation can be found in the product folder.

- TI user guide SPRU655, *60-pin Emulation Header*

Note—Differences are defined in Section 7.8.2

- IEEE standard 1149.1, *Test Access Port and Boundary-Scan Architecture*
- *AC Coupled Net Test Specification* (IEEE1149.6)

7.8.1 Configuration of JTAG/Emulation

The JTAG interface can be used for boundary scan and emulation. The boundary scan implementation is compliant to both IEEE 1149.1 and IEEE 1149.6 (for SERDES ports). Boundary scan can be used regardless of the device configuration.

As an emulation interface, the JTAG port can be used in various modes:

- *Standard emulation:* requires only five standard JTAG signals
- *HS-RTDX emulation:* requires five standard JTAG signals plus EMU0 and/or EMU1. EMU0 and/or EMU1 are bidirectional in this mode.
- *Trace port:* the trace port allows real-time dumping of certain internal data. The trace port uses the EMU18:0 pins to output the trace data, however, the number of pins used is configurable.

Emulation can be used regardless of the device configuration.

For supported JTAG clocking rates (TCLK), see the data manual. The EMU18:0 signals can operate up to 166 Mbps, depending on the quality of the board-level implementation.

Any unused emulation port signals can be left floating.

7.8.2 System Implementation of JTAG / Emulation

For most system-level implementation details, see the TI user guide SPRU655, *60-pin Emulation Header*. However, there are a few differences for the TCI6484 and C6457 implementation compared with the user guide document:

- Instead of the 100-kΩ resistor between the TVD pin and the devices JTAG I/O voltage, a 100-Ω resistor should be used.
- Although the user guide document implies 3.3-V signaling, 1.8-V signaling is required for the TCI6484 and C6457. In addition, the TVD source should be connected to 1.8 V.

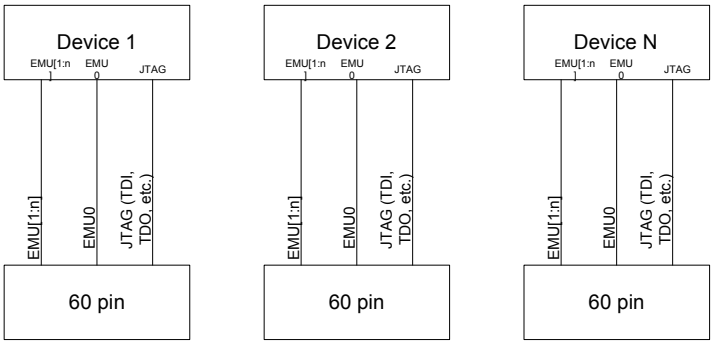
For a single DSP connection where the trace feature will not be used, the standard non-buffered connections can be used along with the standard 14-pin connector. If the trace feature will be used (which requires the 60-pin emulator connector), the five standard JTAG signals should be buffered and TCLK and RTCLK should be buffered separately. It is recommended to have the option for an AC parallel termination on TCLK because it is critical that the TCLK have a clean transition. EMU0 and EMU1 should not be buffered because these are used as bidirectional signals when used for HS-RTDX.

For a system with multiple DSPs that does not use the trace analysis features, the JTAG signals should be buffered as described above but the standard 14-pin connector can be used.

If trace analysis is desired in a system with multiple DSPs, there are two recommended solutions.

1. Emulator with Trace, Solution #1: Trace Header for Each DSP (Figure 19)

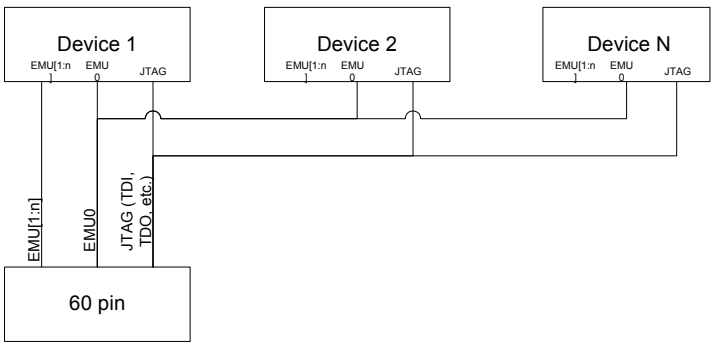
Figure 19 Emulator With Trace, Solution #1



- Pros
  - Most simple
  - Most *clean* solution, electrically
- Cons
  - Expensive (multiple headers)
  - Takes up board real estate
  - No global breakpoints, synchronous run/halt

2. Emulator with Trace, Solution #2: Single Trace Header (Figure 20)

Figure 20 Emulation With Trace, Solution #2



- Pros
  - Fairly *clean* solution, electrically
  - Supports global breakpoints, synchronous run/halt

- Cons
  - Supports trace on only one device
  - Less bandwidth for trace (EMU0 used for global breakpoints)
  - Loss of AET Actionpoints on EMU1 (only significant if EMU1 has been used as a trigger input/output between devices. EMU0 can be used instead if needed).

No external pullups/downs are needed because there are internal pullups/downs on all emulation signals.

Although no buffer is shown, for multiple-DSP connection, it is recommended to buffer the five standard JTAG signals.

If trace will be used, it is not recommended to add both a 60-pin header and a 14-pin header due to signal integrity concerns. Adapters (60-pin to 14-pin) are available to allow connection to emulators that support only the 14-pin connector.

Some emulators may not support 1.8-V I/O levels. Emulators intended to operate with the TMS320TCI6484 and TMS320C6457 DSPs should be checked for supported I/O levels. If 1.8 V is not supported, a voltage translator circuit is needed or a voltage converter board may be available. If the TCI6484 and C6457 will be in a JTAG chain with devices that have a different voltage level than 1.8 V (i.e. 3.3 V), voltage translation would be needed.

Figure 21 shows a dual-voltage JTAG solution using buffers to perform the voltage translation. The ALVC family for 3.3 V and AUC family for 1.8 V are both used because they have similar propagation delays and high drive outputs.

Figure 21 Emulator Voltage Translation With Buffers

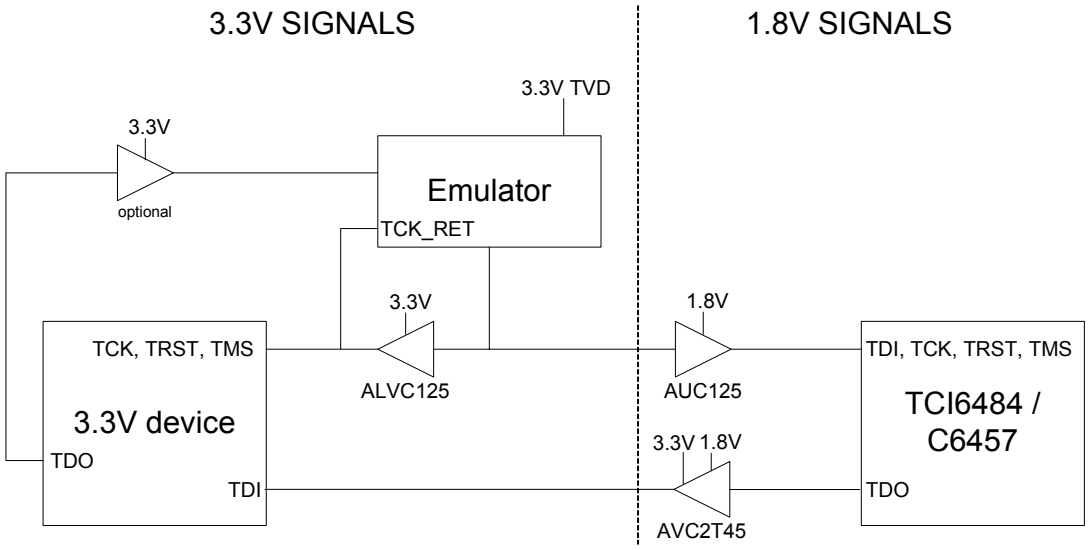
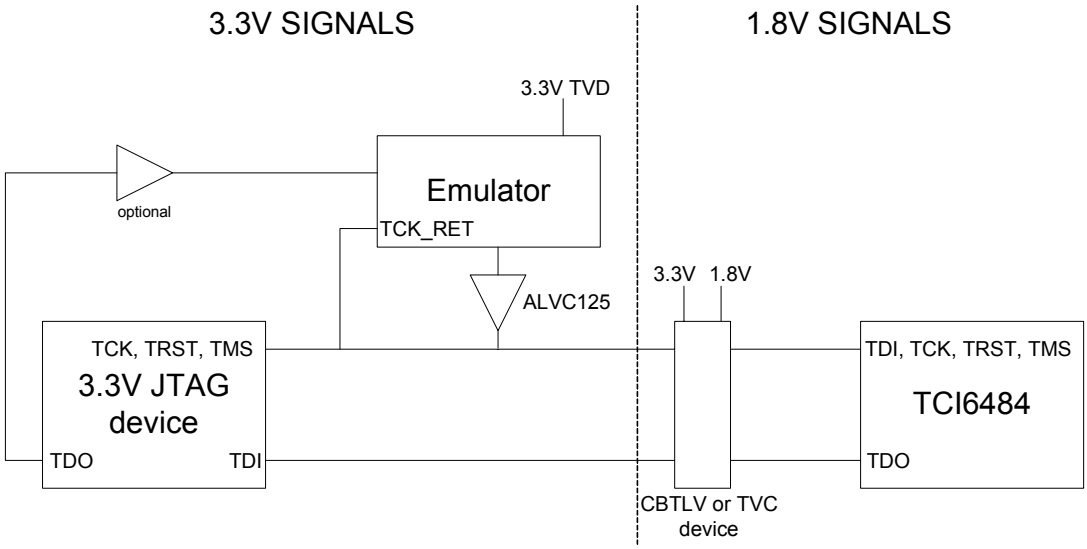


Figure 22 shows an example of using FET switch devices for voltage translation. If EMU0 and EMU1 are connected, this approach should be used because these are bidirectional signals.

Figure 22 Emulator Voltage Translation With Switches



If the trace signals are supported, they may need to have voltage translation as well. Due to the speed of that interface, it is recommended that these signals be connected directly to the emulation header.

7.9 64-Bit External Memory Interface (EMIF64)

Documentation for EMIF64 can be found in the product folder.

- *DSP External Memory Interface (EMIF)* user's guide
- IBIS model file
- TI application report SPRA839, *Using IBIS Modes for Timing Analysis*

7.9.1 Configuration of the EMIF64

The EMIF64 module must be enabled via software after reset before it can be used.

The EMIF64 input clock (AECLKIN or SYSCLK7 clock) is selected at reset via the pullup/pulldown resistor on the GPIO[15] pin. AECLKIN is the default input clock for the EMIF64 input clock. The internally-generated clock is referred to as SYSCLK7. After a reset, SYSCLK7 is CPU core clock ÷ 10. The SYSCLK7 divider can be changed via software.

If the EMIF64 peripheral is not used, most EMIF64 inputs can be left unconnected. The internal pullup and pulldown resistors on this interface should help minimize leakage.

Device boot over EMIF is available and selectable via the bootmode configuration registers. In this mode, after reset, the DSP immediately begins executing from the base address of CE3 in 8-bit asynchronous mode.

7.9.2 System Implementation of EMIF64

If only a portion of the peripheral is used, control pins that are not used should be pulled to a valid state and data pins that are not used can be left floating.

Series resistors MUST be used on the EMIF64 interface to reduce overshoot and undershoot. Recommended values include 10 Ω, 22 Ω, or 33 Ω. Simulations with IBIS models are recommended to determine optimal termination resistor values, verify signal integrity, and verify AC timings requirements have been met.

Significant signal degradation can occur when multiple devices are connected to the EMIF64. Simulations are the best way of determining the optimal physical topologies.

All synchronous memories connected to the EMIF should have clock enable low during device power ramp and reset. This is necessary to avoid inadvertent clocking of memories during power ramp and reset low. This can be implemented with a weak pulldown resistor (i.e. 10 kΩ) on the CKE signals.

7.10 Host Port Interface (HPI)

Documentation for HPI can be found in the product folder.

- *DSP Host Port Interface (HPI)* user's guide
- IBIS model file
- TI application report SPRA839, *Using IBIS Modes for Timing Analysis*

7.10.1 Configuration of HPI

The HPI module must be enabled via software after reset before it can be used.

The HPI width selection (16-bit or 32-bit) is selected at reset via the pullup/pulldown resistor on the GPIO[14] pin.

Internally, the HPI module is clocked by SYSCLK5, which is CPU core clock ÷ 6. Therefore, the maximum HPI timing is dependent on the CPU core clock frequency.

If HPI is not used, the pins may be left floating as long as the peripheral is not enabled via software; however, we recommend external pullups on unused data signals for power consumption savings.

Boot over HPI is available and selectable via the bootmode configuration registers.

7.10.2 System Implementation of HPI

Series resistors MUST be used on the HPI signals to reduce overshoot, undershoot, and EMI. Generally, acceptable values are 10 Ω, 22 Ω, or 33 Ω.

Simulations with IBIS models are recommended to determine optimal termination resistor values, verify signal integrity, and verify AC timings requirements have been met.

If only a portion of the interface is used (i.e. HPI16 mode), floating control signals should be pulled to an appropriate state and unused data signals can be left floating. However, it is recommended that external pullups be used on unused data signals power consumption savings.

7.11 Universal Test and Operations PHY (UTOPIA)

Documentation for UTOPIA can be found in the product folder.

- DSP Universal Test and Operations PHY Interface for ATM 2 (UTOPIA2) user's guide
- IBIS Model File
- *Using IBIS Modes for Timing Analysis* application report

7.11.1 Configuration of UTOPIA

The UTOPIA module must be enabled via software after reset before it can be used.

The Utopia RX and TX clocks are supplied externally. Clock rates up to 50 MHz are supported.

If the Utopia interface is not enabled, the input pins can be unconnected (floating), but this will result in some additional power consumption due to leakage. This power consumption can be minimized by adding external pullups.

7.11.2 System Implementation of UTOPIA

Series resistors MUST be used on the HPI signals to reduce overshoot, undershoot, and EMI.

The 50 MHz operation is the maximum point-to-point operational throughput. The addition of multiple devices can affect performance and 50 MHz may not be attainable. It is recommended to run IBIS simulations to check the signal integrity and maximum operating frequency for a particular board topology.

The Utopia interface can support multiple devices on the same bus using multi-PHY mode.

If only a portion of the Utopia interface is used, unused inputs should use external pullups or pulldowns to place inputs into valid states.

7.12 SERDES-LVDS Termination Options

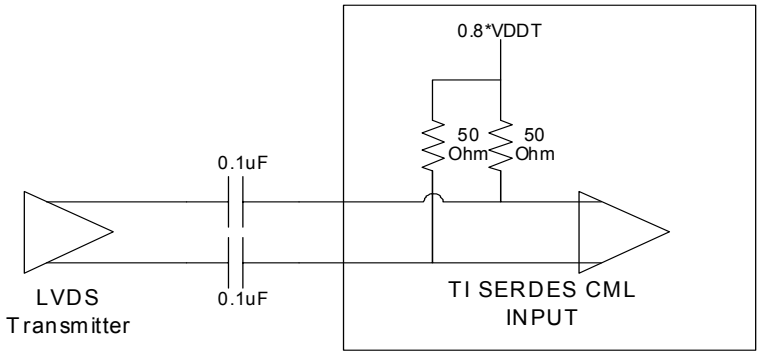
TI SERDES are CML implementations and do not directly support LVDS levels. Compatibility with standard LVDS signals is achievable with proper terminations as described in this section.

7.12.1 LVDS to CML Example

The following is an example of an LVDS to CML connection.

- Requires AC termination because the LVDS common mode voltage is too high for the TCI6484 and C6457 SERDES receivers
- CML receivers include 100-Ω termination needed by LVDS and include internal biasing (no external biasing needed)
- See Figure 23

Figure 23 LVDS to CML Connection

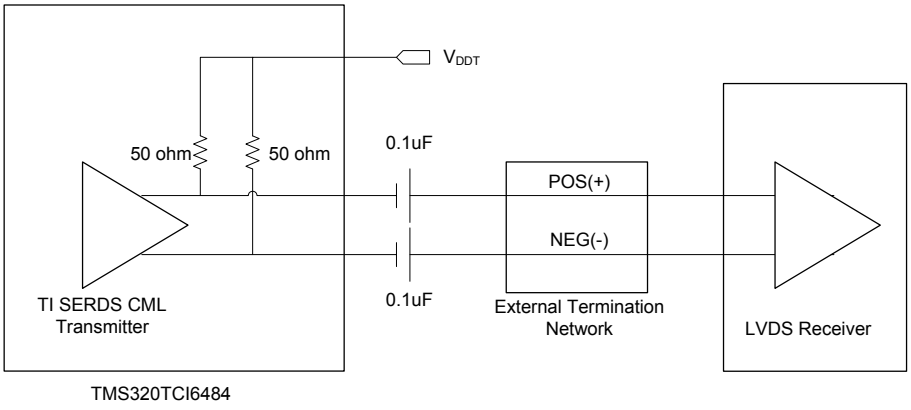


7.12.2 CML to LVDS Example

The following is an example of a CML to LVDS connection.

- Requires AC termination because the TCI6484 and C6457 CML output voltage is too low for a LVDS receiver and the common mode voltages are incompatible
- LVDS receivers require 100-Ω terminations and proper biasing
- Some LVDS receivers include 100-Ω termination and some do not
- Some LVDS receivers include internal biasing and some do not
- The basic connection diagram is shown in Figure 24

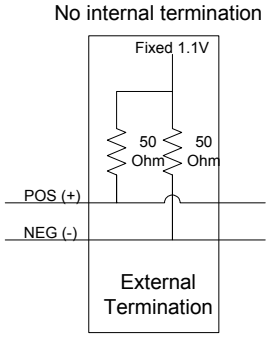
Figure 24 CML-to-LVDS Connection Basic Diagram



- If the LVDS receiver includes the 100-Ω termination and internal biasing, there is no need for external terminations

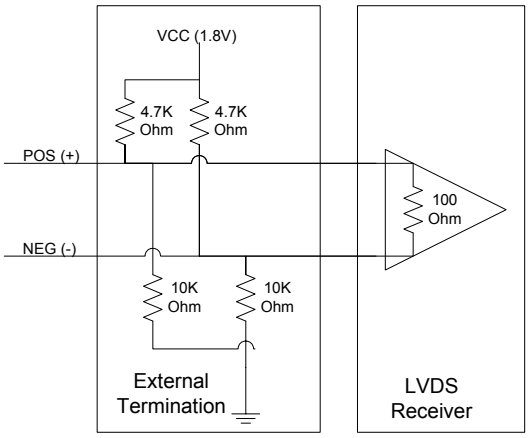
- If the LVDS receiver includes neither the 100-Ω termination or biasing, use the external terminations shown in Figure 25

Figure 25 External Terminations: Receiver Has No Internal Terminations



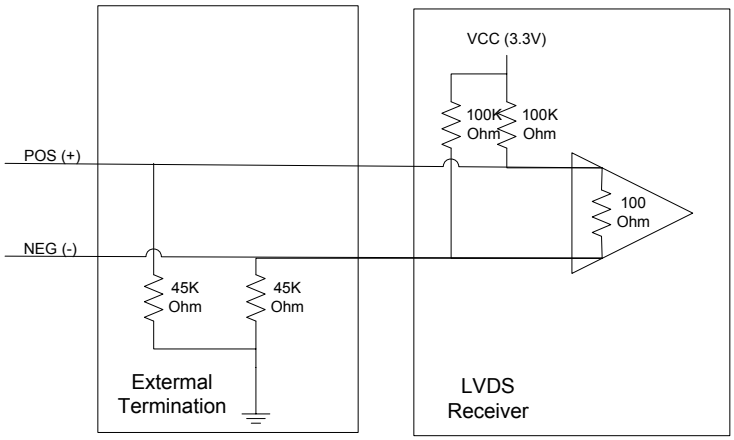
- If the LVDS receive includes the 100-Ω termination but no biasing, use the external terminations shown in Figure 26

Figure 26 External Terminations: Receiver With 100 Ω



- If the LVDS receiver includes 100-Ω terminations and internal pullups (sometimes used for fail-safe), use the type of termination shown in Figure 27. Adjust the external resistor values based on the VCC and internal resistors in order to generate a bias voltage of 1.0 V to 1.2 V.

Figure 27 External Terminations: Receiver With 100 Ω and Pullups



- There are other combinations that may be needed for other types of input buffers. The important factors are to make sure there is a 100-Ω impedance and a bias voltage set around 1.2 V.

8 References

8.1 TMS320TCI6484

The current documentation that describes the TMS320TCI6484, related peripherals, and other technical collateral, is available in the TMS320TCI6484 DSP product folder: http://focus.ti.com/docs/prod/folders/print/tms320tci6484.html.

1. TI data manual, SPRS438, *TMS320TCI6484 Communications Infrastructure Digital Signal Processor* http://www.ti.com/lit/pdf/sprs438
2. TI reference guide SPRU811, *Flip Chip Ball Grid Array Package* http://www.ti.com/lit/pdf/spru811
3. TI user guide SPRU894, *TMS320TCI648x DSP DDR2 Memory Controller* http://www.ti.com/lit/pdf/spru894
4. TI user guide SPRU806, TMS320TCI648x DSP Software-Programmable Phase-Locked Loop (PLL) Controller http://www.ti.com/lit/pdf/spru806
5. TI user guide SPRUEA7A, *TMS320TCI648x Bootloader User's Guide* http://www.ti.com/lit/pdf/spruea7
6. TI application report SCAA059, *AC-Coupling Between Differential LVPECL, LVDS, HSTL, and CML* http://www.ti.com/lit/pdf/scaa059
7. TI data sheet SLLS399, *SN65LVDS108 8-Port LVDS Repeater* http://www.ti.com/lit/pdf/slls399
8. TI data sheet SCAS683, *CDCLVP110 Low-voltage 1:10 LVPECL/HSTL With Selectable Input Clock Driver* http://www.ti.com/lit/pdf/scas683
9. TI data sheet SLLS781, *CDCL1810 1.8V, 10 Output, High-Performance Clock Distributor* http://focus.ti.com/lit/ds/slls781a/slls781a.pdf
10. TI application report SCAA068, *Advantage of Using TI's Lowest Jitter Differential Clock Buffer* http://www.ti.com/lit/pdf/scaa068
11. TI application report SCAA080, *CDCx706/x906 Termination and Signal Integrity Guidelines* http://www.ti.com/lit/pdf/scaa080
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13. TI application report SPRAAG6A, *TMS320TCI6484/6487/6488 DDR2 Implementation Guidelines* http://www.ti.com/lit/pdf/spraag6
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16. TI application report SCEA030, *Voltage Translation Between 3.3-V, 2.5-V, 1.8-V, and 1.5-V Logic Standards With the TI AVCA164245 and AVCB164245 Dual-Supply Bus-Translating Transceivers* http://www.ti.com/lit/pdf/scea030
17. TI application report SCEA035, *Selecting the Right Level-Translation Solution* http://www.ti.com/lit/pdf/scea035
18. JEDEC standard JESD8-15A, *Stub Series Terminated Logic for 1.8 V (SSTL_18)* http://www.jedec.org/download/search/JESD8-15a.pdf
19. TI application report SPRAAY1, *TMS320TCI6484 and TMS320C6457 SERDES Hardware Design Guidelines* http://www.ti.com/lit/pdf/spraay1
20. TI reference guide SPRU803, *TMS320TCI648x DSP Multichannel Buffered Serial Port (McBSP)* http://www.ti.com/lit/pdf/spru803
    NOTE: Will require some changes for device-specific differences
21. TI user guide SPRU725, *TMS320TCI648x DSP General-Purpose Input/Output (GPIO)* http://www.ti.com/lit/pdf/spru725
    NOTE: May require some changes for device-specific differences

22 TI user guide SPRU818, *TMS320TCI648x DSP 64-Bit Timer*
http://www.ti.com/lit/pdf/spru818
NOTE: May require some changes for device-specific differences

23 TI reference guide SPRU732, *TMS320C64x/C64x+ DSP CPU and Instruction Set*
http://www.ti.com/lit/pdf/spru732

24 TI user guide SPRUE11, *TMS320TCI648x DSP Inter-Integrated Circuit (I^2C) Module User's Guide*
http://www.ti.com/lit/pdf/sprue11

25 Philips Semiconductor document 39340011, *I^2C Bus Specification Version 2.1, January, 2000*
http://www.semiconductors.philips.com/acrobat_download/literature/9398/39340011.pdf

26 TI data sheet SCPS113, *PCA9306 Dual Bidirectional I^2C Bus and SMBus Voltage-level Translator*
http://www.ti.com/lit/pdf/scps113

27 TI user guide SPRUE12, *TMS320TCI648x DSP Ethernet Media Access Controller (EMAC)/Management Data Input/Output (MDIO)*
http://www.ti.com/lit/pdf/sprue12
NOTE: Will require some changes for device-specific differences

28 TI specification, SGMII Specification (ENG-46158) Version 1.8, dated April 27, 2005

29 IEEE standard 1596.3-1996, *Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)*
http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=503756&isnumber=11142

30 TI user guide SPRUE13, *TMS320TCI648x Serial RapidIO (SRIO)*
http://www.ti.com/lit/pdf/sprue13
NOTE: May require some changes for device-specific differences

31 TI specification, RapidIO Interconnect Specification Part VI: Physical Layer 1x/4x LP-Serial Specification Version 1.2, dated June 2002.

32 JEDEC standard JESD79, *DDR2 SDRAM Specification*
http://www.jedec.org/download/search/JESD79-2E.pdf

33 TI user guide SPRU655, *60-pin Emulation Header*
http://www.ti.com/lit/pdf/spru655

34 IEEE standard 1149.1, *Test Access Port and Boundary-Scan Architecture*
http://ieeexplore.ieee.org/iel5/7481/20326/00938734.pdf

35 IEEE standard 1149.6, Test Access Port and Boundary-Scan Architecture
AC Coupled Net Test Specification

36 TI user guide SPRU925, *TMS320TCI648x DSP External Memory Interface (EMIF)*
http://www.ti.com/lit/pdf/spru925

37 TI user guide SPRU874, *TMS320TCI648x DSP Host Port Interface (HPI)*
http://www.ti.com/lit/pdf/spru874

38 TI user guide SPRU726, *TMS320TCI648x DSP Universal Test and Operations PHY Interface for ATM 2 (UTOPIA2)*
http://www.ti.com/lit/pdf/spru726

39 JEDEC standard JESD8-7, *1.8 V ± 0.15 V (Normal Range) and 1.2 V - 1.95 V (Wide Range) Power Supply Voltage and Interface Standard for Nonterminated Digital Integrated Circuits*
http://www.jedec.org/download/search/JESD8-7A.pdf

40 TI application report SCAA048, *Filtering Techniques: Isolating Analog and Digital Power Supplies in TI's PLL-Based CDC Devices*
http://www.ti.com/lit/pdf/scaa048

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42 TI application report SPRAB42, *TMS320TCI6484 and TMS320C6457 Power Consumption*
http://www.ti.com/lit/pdf/sprab42
TMS320TCI6484 and TMS320C6457 Power Spreadsheet and Application Report (SPRAB42)

8.2 TMS320C6457

The current documentation that describes the TMS320C6457, related peripherals, and other technical collateral, is available in the TMS320C6457 DSP product folder: http://focus.ti.com/docs/prod/folders/print/tms320c6457.html.

1 TI data manual, SPRS582, *TMS320C6457 Fixed-Point Digital Signal Processor*
http://www.ti.com/lit/pdf/sprs582

2 TI reference guide SPRU811, *Flip Chip Ball Grid Array Package*
http://www.ti.com/lit/pdf/spru811

3 TI user's guide SPRUGK5, *TMS320C6457 DSP DDR2 Memory Controller*
http://www.ti.com/lit/pdf/sprugk5

4 TI user's guide SPRUGL3, *TMS320C6457 DSP Software-Programmable Phase-Locked Loop (PLL) Controller*
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NOTE: Will require some changes for device-specific differences

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9 Revision History

Table 8 lists the change history of this document.

Table 8 Document Revision History

Revision	Comments
SPRAAV7B	Added TMS320C6457 device.
SPRAAV7A	• Updated Table 4 with estimated power usage numbers to reflect the power characterization data presented in SPRAB43 "TMS320TCI6484 Power Spreadsheet" • Removed all references to SmartReflex as this is no longer a supported feature of the TMS320TCI6484 and TMS320C6457 DSPs. • Updated clock reference parameters • Corrected power supply ramping sequence
SPRAAV7	Initial Release
End of Table 8	

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