Application Report
SPRAB05–February 2009

PCI Express to TMS320DM646x PCI Interface Through XIO2000A Bridge

DSPS Applications

ABSTRACT

The Texas Instruments DM646x devices support interfacing to a peripheral component interconnect (PCI) bus through its PCI port. The system or the application may contain a PCI Express® interface. In order to connect the PCI Express bus to the DM646x PCI bus, an XIO2000A translation bridge is used. XIO2000A is a PCI Express to PCI/PCI-X™ bus translation bridge.

For detailed information on the XIO2000A, see the *XIO2000A/XIO2000AI PCI Express to PCI Bus Translation Bridge Data Manual* (SCPS155). This document provides board design suggestions for the various device features; however, it mainly concentrates on the XIO2000A configuration as it connects the PCI Express bus and the DM646x PCI bus.

Contents

List of Figures

List of Tables

1 Typical System Integration

Figure 1 represents a typical implementation of the interface between the PCI Express devices and the DM6467 PCI bus through the XIO2000A translational bridge. The XIO2000A device serves as a bridge between an upstream PCI Express device and downstream PCI bus devices. It has an internal arbiter to support up to six PCI devices. The XIO2000A only operates with the PCI Express interface as the primary bus and the PCI bus interface as the secondary bus.

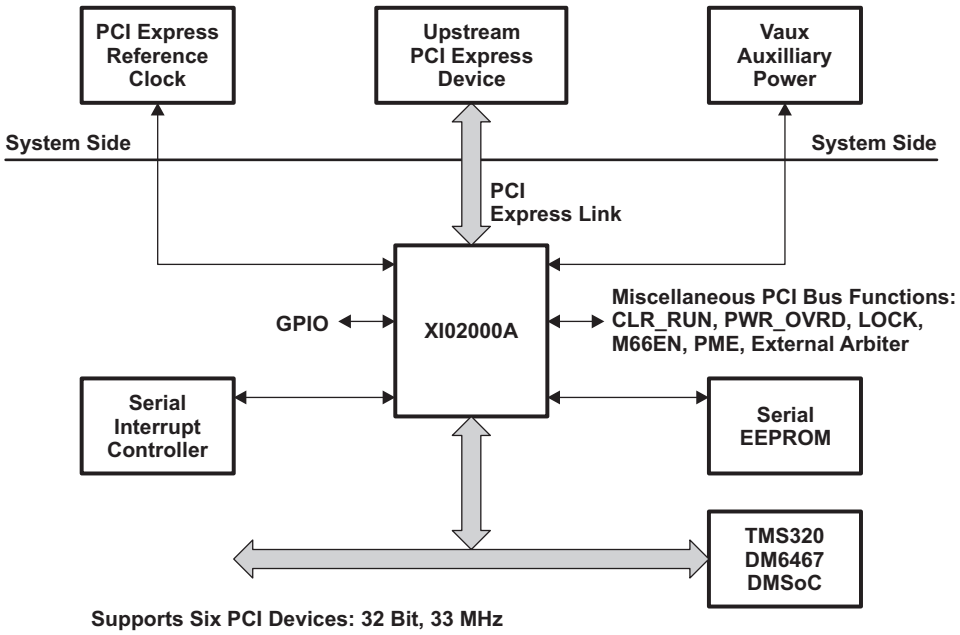
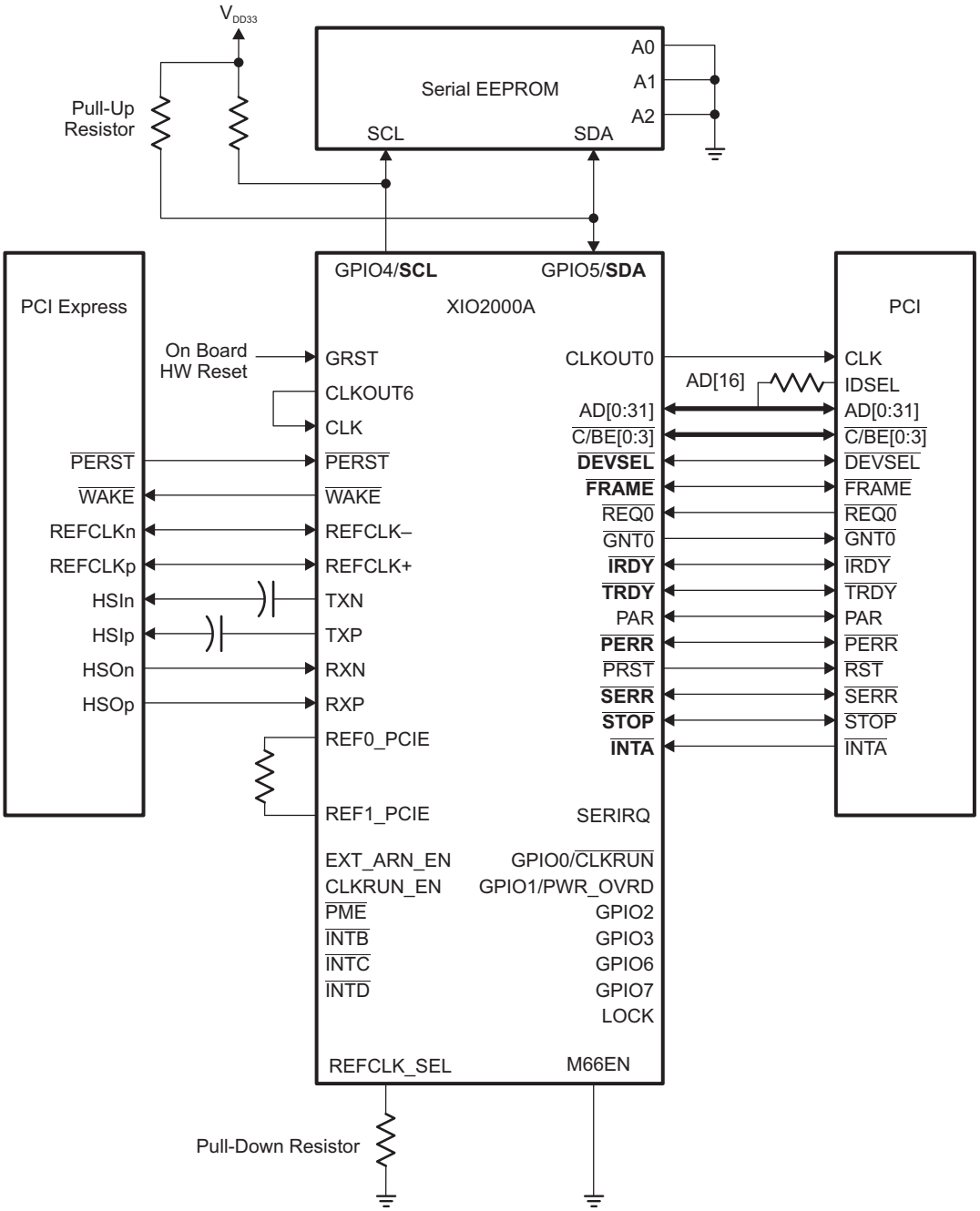


Figure 1. Typical Implementation

The interface of the DM6467 PCI bus with the PCI Express bus through the XIO2000A arbiter is shown in Figure 2.



A **The pullup resistors are connected to the terminals shown in bold.**

Figure 2. The Interface of DM6467 PCI Bus With PCI Express Bus Through XIO2000A Arbiter

Figure 3 shows the bridge adaptor card block diagram.

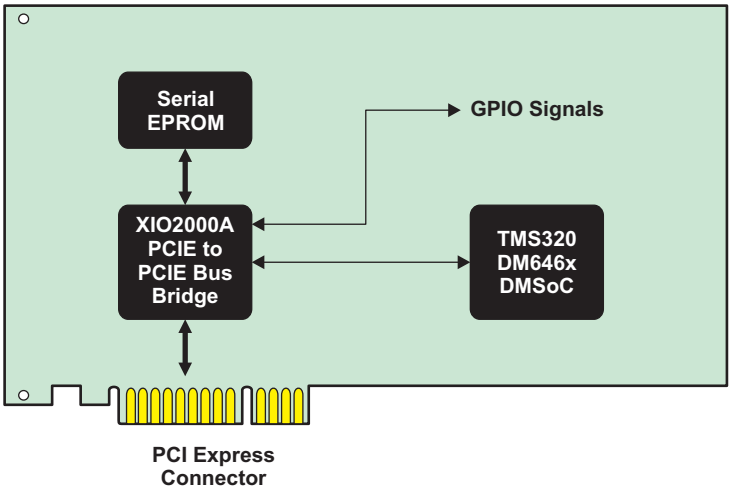


Figure 3. Bridge Adaptor Card Block Diagram

1.1 Operating Frequency

The XIO2000A translational bridge supports a 32-bit data bus and operates at either 33 MHz or 66 MHz. The bridge operating frequency depends on the DM6467 operating frequency. If the 66 MHz operating frequency is selected, then the M66EN pin is connected to V_{CCP} through the pull-up resistor; the M66EN pin is grounded for 33 MHz operating frequency. This document shows the configuration for 33 MHz operating frequency.

1.2 Reference Clock

The XI02000A requires an external reference clock either from the system or from the on-board clock. It receives the common differential clock of 100 MHz from the PCI Express pins or uses an on-board asynchronous single-ended 125-MHz reference clock. Figure 1 illustrates the common 100-MHz reference clock option. The single-ended 125-MHz reference clock is selected when the REFCLK_SEL input terminal is tied to V_{DD33}.

1.3 EEPROM Setting

The external EEPROM can be used for power-up configuration settings. The registers set by the serial EEPROM feature are located in the classic PCI configuration space. The names of these registers include the subsystem ID and subsystem vendor ID, general control, clock control and mask, arbiter control and mask, and serial IRQ control registers. The SCL and SDA pins of EEPROM are multiplexed with GPIO4 and GPIO5 pins, respectively. If the GPIO5/SDA terminal is a 1b at the de-assertion of PERST, the serial EEPROM interface is enabled. A 0b disables the serial EEPROM interface. To enable serial EEPROM external pull-up resistor is connected to V_{DD33}.

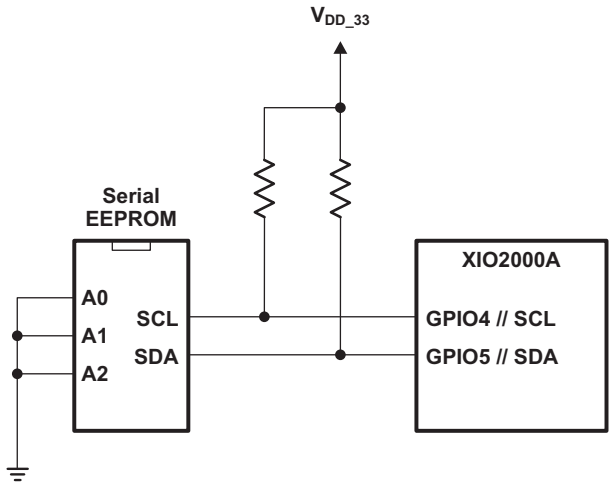


Figure 4. Serial EEPROM Application

1.4 Interrupt

The DM6467 PCI can interrupt the Host through the XIO2000A bridge on various status conditions like parity error, system error, master abort and target abort. The PCI_INTA pin of the DM6467 device is connected to the INTA pin of the XIO2000A. When the interrupt is detected from the DM6467 PCI, the XIO2000A bridge generates an MSI message and sends it to the PCI Express interface. The interrupt is generated for particular status conditions by setting appropriate bits in the PCI Host interrupt enable register. The two registers, PCI Host Interrupt Enable Set Register (PCIHINTSET) and PCI Host Interrupt Clear Register (PCIHINTCLR), are used to set and clear the interrupt, respectively. The DM6467 device can also generate an interrupt through software by setting the SOFT_INT bits.

1.5 DM6467 PCI Interface Signals

AD31:0, C/BE[3:0], PAR, DEVSEL, FRAME, REQ, GNT, PRST, INTA, STOP, TRDY, PERR, SERR, and IRDY of the DM6467 PCI are connected to respective pins of the XIO2000A as shown in Figure 2. The pullup resistors are required for terminal INTA, IRDY, TRDY, FRAME, STOP, PERR, SERR, and DEVSEL.

IDSEL for each PCI bus device must be resistively coupled (100 Ω) to one of the address lines between AD31 and AD16. For the configuration register transaction device number to the AD bit translation chart, see the *XIO2000A/XIO2000AI PCI Express to PCI Bus Translation Bridge Data Manual* (SCPS155). For the example given in this document, AD16 is connected to IDSEL of the DM6467 PCI shown in Figure 2.

Table 1 shows the connection of the DM6467 PCI signals with the XIO2000A bridge signals, column *I/O* is w.r.t. XIO2000A.

Table 1. DM6467 PCI and XIO2000A Bridge Interface Signals

DM6467 PCI Signals	XIO2000A Signals	I/O (1)	Description
PCI_AD[0:31]	AD[0:31]	I/O	PCI address data lines
PCI_C/BE[0:3]	C/BE[0:3]	I/O	PCI command byte enable
PCI_DEVSEL	DEVSEL	I/O	PCI device Select
PCI_FRAME	FRAME	I/O	PCI frame
PCI_GNT	GNT0	O	XIO2000A has six output grant signals GNT[0:5]. GNT0 is connected to the PCI_GNT signal of the DM6467.
PCI_REQ	REQ0	I	XIO2000A has six input request signals REQ[0:5]. REQ0 is connected to the PCI_REQ signal of the DM6467.
PCI_INTA	INTA	I	PCI interrupts A
PCI_IRDY	IRDY	I/O	PCI initiator ready
PCI_TRDY	TRDY	I/O	PCI target ready
PCI_PAR	PAR	I/O	PCI bus parity
PCI_PERR	PERR	I/O	PCI parity error
PCI_SERR	SERR	I/O	PCI system error
PCI_PME	PME	I	PCI power management event. This terminal may be used to detect PME events from a PCI device on the secondary bus. Note: The PME input buffer has hysteresis.
PCI_STOP	STOP	I/O	PCI stop
PCI_PRST	PRST	O	PCI reset. The bridge asserts PRST to rest devices that reside on the secondaryPCI bus.
PCI_CLK	CLKOUT0	O	XIO2000A has seven clock output signals CLKOUT[0:6]. CLKOUT0 is connected to the PCI_CLK signal of the DM6467.

(1) I = Input, O = Output, I/O = Input/Output

1.6 XIO2000A Translation Bridge

The XIO2000A supports up to six external PCI bus devices with individual CLKOUT, REQ and GNT signals. CLKOUT0, REQ0 and GNT0 of XIO2000A is connected to respective pins on the DM6467 PCI. Unused CLKOUT signals can be disabled by asserting the appropriate CLOCK_DISABLE bit in the clock control register at offset D8h. Unused REQ signals can be disabled using a weak pullup resistor to V_{CCP}. Unused GNT signals are no connects.

The DM6467 PCI doesn't support CLKRUN, LOCK, PWR_OVRD, PME and SERIRQ features, so these terminals are kept open.

The INTA pin of the XIO2000A bridge is connected to the PCI_INTA pin of the DM6467 device. The bridge pins INTB, INTC and INTD are kept open as the DM6467 PCI doesn't support these interrupt pins.

PWR_OVRD is an optional PCI bus signal that is shared with the GPIO1. The DM6467 PCI doesn't support PWR_OVRD feature, therefore, this pin is always used as GPIO1.

An external clock feedback feature is provided to de-skew the PCI bus clocks. Connecting the CLKOUT [6] terminal to the CLK terminal is required if any of the other six CLKOUT [5:0] terminals are used to clock the DM6467 PCI module. Pin CLKOUT0 of XIO2000A is connected to the PCI_CLK of the DM6467 PCI module as shown in the Figure 5.

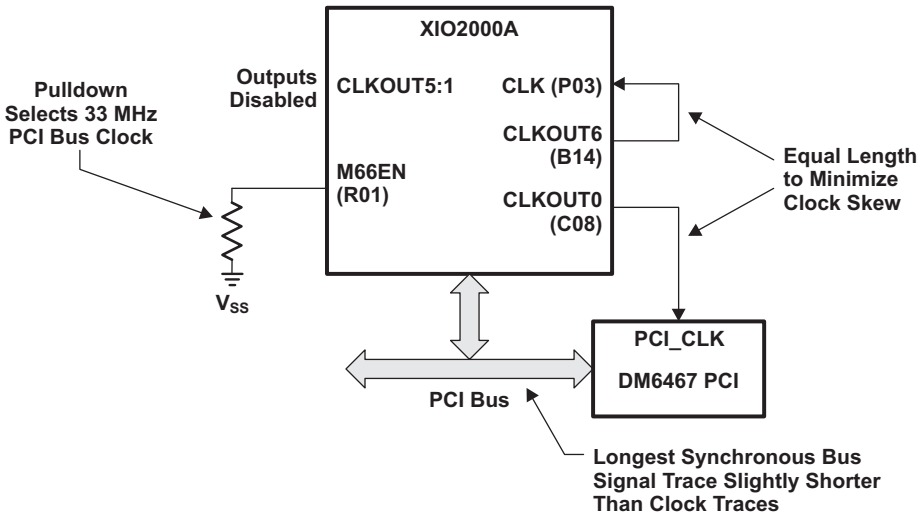


Figure 5. External PCI Bus Clock Feedback

The bridge supports external PCI bus clock sources. If an external clock is a system requirement, the external clock source is connected to the CLK terminal (P03). For external clock mode, all seven CLKOUT [6:0] terminals can be disabled using the clock control register at offset D8h

The REF0_PCIE and REF1_PCIE terminals connect to an external resistor to set the drive current for the PCI Express TX driver.

Table 2 shows the connection of PCI Express signals with XIO2000A bridge signals.

Table 2. PCI Express and XIO2000A Bridge Interface Signals

PCI Express Signals	XIO2000A Signals	I/O (1)	Description
REFCLKp	REFCLK+	I	Reference clock. REFCLK+ and REFCLK- comprise the differential input pair for the 100-MHz system reference clock
REFCLKn	REFCLK-		
HSOp	RXP	DI	Differential serial data receive signals
HSOn	RXN		
HSIp	TXP	DO	Differential serial data transmit signals
HSIn	TXN		
$\overline{\text{PERST}}$	$\overline{\text{PERST}}$	I	PCI Express reset input
$\overline{\text{WAKE}}$	$\overline{\text{WAKE}}$	O	Signal to reactivate the PCI Express link hierarchy's main power rails and reference clock. Note: Since $\overline{\text{WAKE}}$ is an open-drain output buffer, a system side pullup resistor is required.

(1) I = Input, O = Output, DI = Data In, DO = Data Out

1.7 PCI Express Interface

The XIO2000A has an x1 PCI Express interface. The XIO2000A TXP, TXN, RXP and RXN terminals are connected to the pins HSIp, HSIn, HSOp and HSOn terminals of upstream PCI Express device over a 2.5-Gb/s high-speed differential transmit and receive PCI Express x1 link. For add-in cards, the series capacitors are connected between the TXP/TXN terminals and the PCI-Express connector.

The XIO2000A PCI Express reset $\overline{\text{PERST}}$ terminal is connected to the upstream PCI Express device's $\overline{\text{PERST}}$ output.

WAKE is an open-drain output from the XIO2000A that is driven low to re-activate the PCI Express link hierarchy's main power rails and reference clocks.

1.8 Miscellaneous Terminal Consideration

Eight general-purpose input/output (GPIO) terminals are provided for system customization. The exact number of GPIO terminals varies based on implementing the clock run, power override, and serial EEPROM interface features. All eight GPIO terminals are individually configurable as either inputs or outputs by writing the corresponding bit in the GPIO control register.

Table 3 shows the details about the miscellaneous terminals.

Table 3. Miscellaneous Terminals

Signal	I/O [1]	Description
CLKRUN_EN	I	Clock run enable. Set 0 to disable and 1 to enable clock run. Note: The CLKRUN_EN input buffer has an internal active pulldown.
EXT_ARB_EN	I	External arbiter enable. Set 0 for internal arbiter and 1 for external arbiter. Note: The EXT_ARB_EN input buffer has an internal active pulldown.
GPIO0/CLKRUN	I/O	General-purpose I/O 0/clock runs. This terminalfunctions as a GPIO controlled by bit 0 (GPIO0_DIR) in the GPIO control register or the clock run terminal. This terminal is used as clock run input when the bridge is placed in clock run mode. Note: In clock run mode, an external pullup resistor is required to prevent the CLKRUN signal from floating. This terminal has an internal active pullup resistor.
GPIO1/PWR_OVRD	I/O	General-purpose I/O 1/power override. This terminal functions as a GPIO controlled by bit 1 (GPIO1_DIR) in the GPIO control register or the power override output terminal. GPIO1 becomes PWR_OVRD when bits 22:20 (OWER_OVRD) in the general control register are set to 001b or 011b. Note:This terminal has an internal active pullup resistor.
GPIO2	I/O	General-purpose I/O 2. This terminal functions as a GPIO controlled by bit 2 (GPIO2_DIR) in the GPIO control register. Note: When PERST is deasserted, this terminal must be a 1b to enable the PCI Express 1.0a compatibility mode. This terminal has an internal active pullup resistor.
GPIO3	I/O	General-purpose I/O 3. This terminal functionsas a GPIO controlled by bit 3 (GPIO3_DIR) in the GPIO control register. Note: This terminal has an internal active pullup resistor.
GPIO4/SCL	I/O	GPIO4 or serial-bus clock. This terminal functions as serial-bus clock if a pullup resistoris detected on SDA. If a pulldown resistor is detected on SDA, this terminal functions as GPIO4. Note: In serial-bus mode, an external pullup resistor is required to prevent the SCL signal from floating. This terminal has an internal active pullup resistor.
GPIO5/SDA	I/O	GPIO5 or serial-bus data. This terminal functions as serial-bus data if a pullup resistor is detected on SDA. If a pulldown resistor is detected on SDA, this terminal functions as GPIO5. Note: In serial-bus mode, an external pullup resistor is required to prevent the SDA signal from floating.
GPIO6	I/O	General-purpose I/O 6. This terminal functionsas a GPIO controlled by bit 6 (GPIO6_DIR) in the GPIO control register. Note: This terminal has an internal active pullup resistor.
GPIO7	I/O	General-purpose I/O 7. This terminal functionsas a GPIO controlled by bit 7 (GPIO7_DIR) in the GPIO control register. Note: This terminal has an internal active pullup resistor.
GRST	I	Global reset input. Asynchronously resets all logic in device, including sticky bits and power management state machines. Note:The GRST input buffer has both hysteresis and an internal active pullup. The GRST input buffer has both hysteresis and an internal active pullup. If the system designer has no need for this custom reset, the GRST terminal can simply be left floating.
LOCK_EN	I/O	This terminal functions as PCI LOCK when bit 12 (LOCK_EN) is set in the general control register. Note: In lock mode, an external pullup resistor is required to prevent the LOCK signal from floating.

(1) I = Input, O = Output

Table 3. Miscellaneous Terminals (continued)

Signal	I/O [1]	Description
M66EN	I	66-MHz mode enable 0 = Secondary PCI bus and clock outputs operate at 33 MHz 1 = Secondary PCI bus and clock outputs operate at 66 MHz. Note:If the PCI bus clock is always 33 MHz, then this terminal is connected to V_{SS}.
REFCLK_SEL	I	Reference clock select. This terminal selects thereference clock input. 0 = 100-MHz differential common reference clock used. 1 = 125-MHz single-ended, reference clock used.
SERIRQ	I/O	Serial IRQ interface. This terminal functions as a serial IRQ interface if a pullup is detected when PERST is deasserted. If a pulldown is detected, then the serial IRQ interface is disabled.
REF0_PCIE REF1_PCIE	I/O	External reference resistor connected between these two pins for setting TX driver current

2 References

- *XIO2000A/XIO2000AI PCI Express to PCI Bus Translation Bridge Data Manual* (SCPS155)
- *XIO2000A Implementation Guide* (SCPU027)
- *PCI Local Bus Specification*, Revision 2.3 available at http://www.pcisig.com/specifications/conventional/
- *PCIe Express Base Specification*, Revision 1.0a available at http://www.pcisig.com/specifications/pciexpress/base/
- *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0 available at http://www.pcisig.com/specifications/pciexpress/bridge/
- *PCI Express Card Electromechanical Specification*, Revision 1.0a available at http://www.pcisig.com/specifications/pciexpress/base/archive/
- *PCI Mobile Design Guide*, Revision 1.1 available at http://www.pcisig.com/specifications/conventional/pci_mobile_design_guide/

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265