Application Report
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Power Consumption Summary for K2E System-on-Chip (SoC) Device Family

Catalog Processors

ABSTRACT

This application report discusses estimating the power consumption of Texas Instruments' K2Ex Digital Signal Processors (DSP) using a provided device-specific power spreadsheet. It should be noted that the power model is applicable for all silicon revisions.

The power consumption of the device is highly application-dependent, therefore, the provided power spreadsheet allows a number of variables to be set according to the intended application to calculate accurate estimates of device power consumption. This spreadsheet can be used to model power consumption to assist in power supply design, thermal design, and so forth. To obtain good results from the spreadsheet, realistic usage parameters must be entered.

The data found in this document and in the accompanying spreadsheet were measured from devices at the maximum end of the power consumption range for production devices. No production devices will have average power consumption that exceeds the spreadsheet values; therefore, the spreadsheet values may be used for board thermal analysis and power supply design as a maximum long-term average.

Note that TI provides two versions of the K2E power models:

- Use 66AK2E0x for 66AK2E05 and 66AK2E02
- Use AM5K2E0x for AM5K2E04 and AM5K2E02

The 66AK2E0x power model provides all CPU and peripheral options for the super-set 66AK2E05 device. The AM5K2E0x power model provides all CPU and peripheral options for the super-set AM5K2E04. You can configure the power models for subset devices (66AK2E02 and AM5K2E02) by disabling the peripherals that are not present on those devices. For example:

- Disable A15 CorePacs 1-3 and the 10-GbE switch subsystem in the 66AK2E0x power model to get 66AK2E02.
- Disable A15 CorePacs 2-3 and the 10-GbE switch subsystem in the AM5K2E0x power model to get AM5K2E02.

In both power models, the default CPU and peripheral parameters (including %utilization) represent a typical networking application.

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1 Activity-Based Models

Power consumption for the device can vary widely depending on the use of on-chip resources. Therefore, power consumption cannot be estimated accurately without an understanding of the components of the device in use and the usage patterns for those components. By providing the usage parameters that describe what is being used on the device and how it is being used, accurate power consumption values can be obtained for power supply and thermal analysis. Expected power consumption for worse-case utilization can be determined by choosing usage parameters closest to the real-use case

The power spreadsheet divides the power consumption into two major components: baseline power and activity power.

1.1 Baseline Power

Baseline power is composed of the power consumed by the **device leakage** and the power consumed by the **baseline clock tree**. The power model defines the worst case baseline power consumed by the device under the entered operating conditions.

Device leakage power is static power, for example, it is the power that is consumed even when no part of the device is clocked. The leakage power consumption depends purely on the supply voltages (core, memory array, I/O voltages), device operating temperature (this is represented by the case temperature in the power model) and process strength. At a given voltage, leakage power increases exponentially with the case temperature. Leakage power is higher for a device that lies on the "hotter" side of the process strength and lower for a device that lies on the "colder" side of the spectrum.

Baseline clock tree power is the clocking power consumed by always-ON logic on the device, for example, the clocking power consumed when the external and on-chip oscillators are programmed to the desired frequency and all possible power and clock domains are disabled. Baseline clock tree power is purely dependent on the CPU frequency and supply voltages.

Thus, baseline power as a whole is highly dependent on voltage, temperature, CPU operating frequency and process strength.

1.2 Dynamic Power

Dynamic power is the power that is consumed by all active parts of the device:

- C66x and ARM CorePacs
- Memory subsystem
- External memory interfaces
- High speed and other peripherals

Dynamic power is composed of the module's idle clocking power and its activity power.

Idle clocking power is the power consumed when the module is enabled and configured, but is not performing any "activity", for example, 0% utilization. The idle clocking power of a module can be obtained by changing the Status to "Enabled" and entering 0 under % Utilization (this is only applicable to modules that are not Always-ON). It is independent of the operating temperature. The idle clocking power for all modules (including the ARM subsystem and the C66x CorePac) depends on the SoC frequency that also clocks the rest of the chip.

Activity power is independent of temperature, but highly dependent on the module's activity levels driven primarily by its % utilization. In the power spreadsheet, activity power is separated by the major modules/peripherals within the device. Therefore, the individual module/peripheral power consumption can be estimated independently. This helps with tailoring power consumption to specific applications.

NOTE: Module and peripheral activity power consumption includes some necessary EDMA3 and PktDMA activity used to transfer data on-chip and off-chip when required. The power contribution of these modules has been minimized to extract the power consumption solely associated with the module/peripheral under consideration.

2 Spreadsheet Parameters

The spreadsheet provides configurable parameters that allow the estimation of power consumption based on configured usage parameters. To ensure realistic results, verify that the spreadsheet is configured accurately.

The parameters are as follows:

- Frequency: Specifies the operating frequency of a module and peripheral or the frequency of the external interface to that module.
- Modes: Selects the peripheral-specific configuration mode.
- Status: Specifies whether a peripheral is Enabled and configured for use, or Disabled.
- % Utilization: Specifies the relative amount of time the module is active or in use versus off or idle.
- %Write: Specifies the relative amount of active time that the module is transmitting versus receiving. For example, if the module is idle for 60% of the time and active for 40% of the time (%utilization is 40) and is performing writes for half the active time, enter 50% under % writes. The power model will assume remaining half of the active time is used to perform reads.
- Bits: Specifies the number of data bits to be used in a selectable-width interface.
- Lane: Specifies the number of lanes used by that interface.

2.1 Power Domains Details

Power domains and associated clock domains within the device (except the Always On domain) can be disabled or enabled by software. When a power domain is disabled, the peripherals and memories in that domain are put to sleep to reduce leakage dissipation,and the peripherals are held in reset and clock-gated, reducing the baseline and activity power consumption of the device. An example is the Network Coprocessor power domain, disabling it also disables the Packet Accelerator, Security Accelerator and GbE Switch submodules that form part of the Network Coprocessor.

The spreadsheet that accompanies this application report allows you to disable or enable a power domain in the model by selecting Disabled or Enabled status for the peripheral in the drop down menu of the status column.

For more information on power domains that can be disabled and the Power Sleep Controller, see the device-specific data manual and the *KeyStone Architecture Power Sleep Controller (PSC) User's Guide* [1][1]

2.2 Device Modules/Peripherals

For information on modules and peripherals available on a device, see the device-specific data manual and relevant user guides.

3 Using the Power Estimation Spreadsheet

The use of the power estimation spreadsheet involves entering the appropriate usage parameters as input data in the spreadsheet. The following steps show the general flow:

1. Choose the appropriate speed grade: The device-specific data sheets specify two speed grades: 1250 MHz and 1400 MHz. Decode the speed grade from your part number using the "Part Number Legend" in the device-specific data sheet and select the correct option from the dropdown. It is important to select the correct speed grade because the 1.4 GHz speed grade tends to have higher leakage than 1.25 GHz in order to meet production yield. Entering SoC frequency higher than 1250 for the 1250 MHz speed grade is invalid and will black out the power results.

2. Choose the appropriate SoC operating frequency (note that the C66x CorePac, SoC and ARM subsystem are all fed by the same main PLL). For the 1250 MHz speed grade, enter between 800 Mhz to 1250 MHz, which is the standard operating range in PLL mode. While the power model allows for this, DO NOT enter a frequency greater than 1250 MHz since that is not supported for a 1250 MHz speed grade device. For the 1400 MHz speed grade, enter between 800 MHz to 1400 MHz, which is the standard operating range in PLL mode. For either speed grade, you can also go down to 50 MHz to estimate the power in bypass mode during boot.
3. Choose the case temperature for which you want to estimate power: 85°C or 100°C.
4. Enable the appropriate peripherals used for your application including the mode, frequency, and bus width for that peripheral, if applicable.
5. Enter the appropriate peripheral's or module's % utilization and % writes.

For best results, enter the information from left to right, starting at the top and moving downward. As the spreadsheet is being configured, the settings are checked for conflicts. For example, it checks to see if the specified clock frequency is within the allowed range.

The spreadsheet takes the input information and displays the details of power consumption for the chosen configuration.

3.1 Choosing Appropriate Values

Acceptable values are determined by design and the correct values to enter will be clear.

You can disable unused modules/peripherals in the spreadsheet by selecting the Disabled tab in the column labeled Status. To choose the appropriate values, you need a good understanding of the read/write balance, bit switching required estimation, and utilization of the user application.

3.1.1 % Utilization

Determining the utilization for the C66x CorePac and the Network Coprocessor (NETCP) is not as straightforward, so a brief guide is outlined here. The utilization for other modules is simply the percentage of the time the module spends doing something useful, versus being unused or idle. For these peripherals, the value is just the average over time. For example, if the DDR3 performs reads and writes one-quarter of the time and has no data to move for the other three-quarters of the time (though it continues to perform background tasks like refreshes), this would be considered 25% utilization.

- The C66x CorePac utilization is not as straightforward, because there are varying degrees of use for the DSP. The spreadsheet estimates the DSP activity with respect to three levels of execution:%Signal Processing (SP) Utilization, %Control Code (CC)Utilization, and % Idle Utilization. The user can only enter %Signal Processing Utilization and % Control Code Utilization in the power model. If the sum of %Signal Processing Utilization and % Control Code Utilization is less than 100%, then the spreadsheet assumes that the remaining percentage is Idle Utilization. **The sum of SP, CC and Idle execution levels cannot exceed 100% so you should make sure %SP + %CC is always ≤ 100.** A sum greater than 100% will result in an error pop-up. The three levels of execution are described in more detail below:
  - **Signal Processing (SP) Utilization** is used to represent scenarios with high levels of DSP activity. 100% SP activity corresponds to eight instructions fetched by the DSP and executed in parallel each DSP clock cycle, resulting in all eight functional units being active every cycle. Few DSP algorithms will achieve 100% SP utilization because this requires execution of all eight functional units every cycle with no stalls. Even intense applications do not spend all of the time executing such highly parallel code.
  - **% Control Code (CC) Utilization** is used to represent scenarios with low levels of activity. This could embody some type of task-polling loop or background task.The activity for this case represents the execution of approximately two functional units every clock cycle.
  - **% Idle Utilization** is used to represent the case in which the DSP is active, but is not doing useful work (NOP execution). This parameter cannot be explicitly entered into the spreadsheet, and is assumed to be the remaining utilization percentage when % Signal Processing Utilization and % Control Code do not sum to 100% (% Idle Utilization = 100% - % Signal Processing Utilization - % Control Code Utilization).

NOTE: It may not always be feasible to neatly separate or profile CPU code into signal processing or control code. For ease of use, it is recommended that the instructions per cycle (IPC) over all CPU code (for example, both SP and CC) be used to determine utilization and attribute all of it to signal processing. For example, an average IPC of 2.4 over the entire application code is 2.4/8 = 30% utilization (since the CPU has 8 functional units that can operate in parallel). Enter 30% for SP and leave CC at 0%

For more information about the DSP architecture, operation, or instruction set, see the *TMS320C66x DSP CPU and Instruction Set Reference Guide* [2].

- The Network Coprocessor (NETCP) on the K2E device family is a complex peripheral with significant capabilities (see the NETCP for K2E/K2L users guide for details). It also has the potential to consume considerable dynamic power if heavily utilized and thus impacts the power budget significantly. With that in mind, TI provides utilization levels for the various NETCP submodules - the Packet accelerator (PA2), Security accelerator (SA2) and the GbE Switch - for typical use cases.

Table 1. NETCP Sub-Block Utilization % for Typical Use Cases

NETCP Subblock and Use case	Packet Accelerator (PA2)	Security Accelerator (SA2)	GbE Switch
Networking	28%	7%	5%
Enterprise Gateway	7%	0%	2%

  - In the **Networking** use case, the NETCP is leveraged for inline IPSec with the Ethernet switch used for switching.
  - In the **Enterprise gateway** use case, the NETCP is used for basic classification and checksum offload with the Ethernet switch used for switching.

  It is relatively easy to calculate the utilization% for the GbE switch. The K2E device has 8 GbE ports with each capable of 1Gb/s traffic.The utilization % depends on two factors: the number of active ports and the utilization level of the active ports. For example, if 4 out of 8 ports are active with 200Mb/s traffic on each port, the GbE switch utilization % will be (4/8) * (0.2Gbps/1Gbps) = 10%.

  Note that the IO rail power represents the power consumed by the SerDes lanes on the GbE switch subsystem. It is independent of the activity level on the NETCP and is present as long as the NETCP is enabled. Disabling the NETCP assumes the SerDes lanes are also disabled and this puts the GbE switch IO rails in a very low power state.
- **General note:** System level issues may also reduce utilization. Although the spreadsheet will accept 100% utilization for all peripherals, this is not possible in reality. As memory and EDMA3 bandwidth is consumed, peripheral activity is throttled back due to these bottlenecks, and, therefore, 100% utilization is not achievable. In applications with a lot of memory and/or EDMA3 usage, individual module utilization numbers should be entered, while keeping this overall limitation in mind.

3.1.2 % Writes

Peripherals that transmit as much as they receive have 50% writes (the spreadsheet will assume the remaining 50% of the time is spent on reads). In some applications, peripherals transmit in only one direction, or have a known balance of data movement. In these cases, the % writes option is not available for configuration. For the peripherals that have the % write configuration, 50% is a typical number that should be used.

3.2 Peripheral Enabling and Disabling

As mentioned previously, the device includes the capability to disable peripherals to reduce power consumption. This can be done by configuring the Power Sleep Controller. The spreadsheet also allows you to disable peripherals controlled by the PSC to ensure the peripherals' dynamic power is not included in the power calculation if the peripheral is not being used. For more information, see the device-specific data manual and the *KeyStone Architecture Power Sleep Controller (PSC) User's Guide* [1].

A peripheral can be enabled or disabled in the spreadsheet from the column labeled Status. If a peripheral is disabled, the CVDD and I/O power for the peripheral will be 0 unless it is a SerDes peripheral in which case the I/O rails may show some leakage. If the peripheral is enabled with 0% utilization, the dynamic power in its row will represent the idle clocking power for the module. For more information see the *KeyStone Architecture Power Sleep Controller (PSC) User's Guide* [1].

4 Using the Results

The power data presented in this document and the accompanying spreadsheet were collected from devices considered to be at the maximum end of power consumption for production devices. No production units will have average power consumption that exceeds the spreadsheet values. The power consumption estimated by the spreadsheet is the maximum average power consumption. While transient currents may cause power to spike above the spreadsheet values for a small amount of time, over a long period of time, the observed average power consumption will be below the spreadsheet value. Therefore, the spreadsheet values may be used for board thermal analysis and power supply design as a maximum long-term average.

4.1 Adjusting I/O Power Results

I/O power depends on the level of peripheral activity.

4.2 Spreadsheet Layout and Details

The following sections discuss the spreadsheet layout and details.

4.2.1 Voltage Rails

The spreadsheet calculates power consumption over six voltage rails - CVDD, CVDD1, DVDD15, DVDD18, DVDD33 and VDDALV. It should be noted that "DVDD18" includes the power consumed by the DVDD18, AVDDAx and VDDAHV rails.

4.2.2 Baseline Section of Spreadsheet

As explained earlier, the baseline power portion of the results section consolidates the average power associated with leakage, always-ON clock tree and phase-locked loop (PLL) power.

4.2.3 Dynamic Section of Spreadsheet

The dynamic section contains the average power consumption associated with enabling a peripheral along with power consumed due to peripheral activity. The activity levels of a peripheral are defined by the peripheral frequency, % utilization, % writes, bus width and peripheral mode.

4.2.4 Totals Section of Spreadsheet

The totals section provides the total in each column for each power supply for Baseline plus Dynamic power. The total (mW) is equal to the total power for all voltage rails for example, total device power.

4.3 Current vs. Power Variable Option

There is an option on the spreadsheet that can be used to get the estimates across each of the power rails and the total in terms of Power (in mW) and Current (in mA).

- With the variable set to Power, it uses CVDD = SmartReflex Voltage to provide total power estimates in mW.
- With the variable set to Current, it uses CVDD = 0.85 V to provide total current estimates in mA, since that is the minimum voltage being used in production.

This is being done to provide worst case estimates that may be used for board thermal analysis and power supply design as a maximum long-term average.

4.4 Download

- http://www.ti.com/lit/zip/sprm652 for 66AK2E05 and 66AK2E02
- http://www.ti.com/lit/zip/sprm653 for AM5K2E04 and AM5K2E02

5 FAQs

Q1: What do the various ARM A15 CorePac options enable/disable/WFI represent? How is it different from enabling/disabling the ARM Subsystem?

A: Disabling an A15 CorePac will remove the leakage and dynamic power consumed by it but leaves the remaining cores and rest of the ARM subsystem active. All A15 CorePacs fall under one power/clock domain. This group of A15s and associated shared logic is called the ARM subsystem. Enabling/disabling the ARM Subsystem disables all ARM cores regardless of the status of individual A15 CorePacs.

WFI (wait for interrupt) is a feature of the ARMv7-A architecture that puts the processor in a low power state by disabling most of the clocks in the processor while keeping the processor powered up. This reduces the power drawn to the static leakage current, leaving a small clock power overhead to enable the processor to wake up from WFI mode [3].

Q2: What happens when I enable/disable other peripherals?

A: Please see the section on Power Domains Details and Peripheral Enabling and Disabling.

Q3: Why does the power spreadsheet offer only two fixed temperature options (85°C and 100°C) instead of a variable temperature range like earlier models?

A: K2E devices have a new feature called temperature compensation that adjusts the core supply voltage (CVDD) in response to changes in operating temperature. Each device is programmed with temperature thresholds that when crossed trigger a change in the supply voltage. As temperature ramps down, the supply voltage is raised every time the operating temperature crosses a programmed threshold. The temperature is sensed by the on-chip temperature sensors. The voltages are so programmed that the higher voltage after crossing a threshold essentially raises the overall power consumption of the device back to where it was at the previous threshold. For K2E devices, 85°C is the highest temp threshold. As temperature reduces below 85°C, the increase in voltage will bump up the device power back to where it was at 85°C, for example, below 85°C the worst case power consumption will be "constant". The maximum operating temperature is 100°C. Between 85°C and 100°C the leakage follows exponential behavior wrt temperature. Hence the power model gives only two options for entering the temp - 85°C and 100°C. In this way, the power model is designed to give the worst case power consumption for power supply sizing.

Q4: Why is the MSMC and Navigator utilization so low for the default use case?

A: As mentioned earlier, all %utilizations in the power model represent realistic numbers for a typical networking application. MSMC has eight memory banks that can be accessed in parallel. The transactions to MSMC generated by the active masters are expected to exercise 1 bank on average per cycle (1/8 = 13%). The NETCP is the primary user of the Navigator in this application and works in tandem with the ARM cores to generate pushes and pops for every transmit/receive packet. The rate of pushes/pops that are generated is ~5% of the Navigator's capacity.

6 References

1. *KeyStone Architecture Power Sleep Controller (PSC) User's Guide*
2. *TMS320C66x DSP CPU and Instruction Set Reference Guide*
3. Cortex-A15 MPCore Technical Reference Manual

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