TMS320DM36x DaVinci™ Digital Media Processor Video Processing Front End (VPFE)

User's Guide

Literature Number: SPRUGU5C
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About This Manual

This document describes the operation of the Video Processing Front End in the DM36x DaVinci™ Digital Media Processor.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers may be shown with the suffix h or the prefix 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties with default reset value below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure can have one of multiple meanings:
    - Not implemented on the device
    - Reserved for future device expansion
    - Reserved for TI testing
    - Reserved configurations of the device that are not supported
  - Writing non-default values to the Reserved bits could cause unexpected behavior and should be avoided.

Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

Related Documentation From Texas Instruments

For product information, visit the Texas Instruments website at http://www.ti.com.

SPRS457 — TMS320DM365 Digital Media System-on-Chip (DMSoC)

SPRS668 — TMS320DM368 Digital Media System-on-Chip (DMSoC)

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TI Embedded Processors Wiki— *Texas Instruments Embedded Processors Wiki.* Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

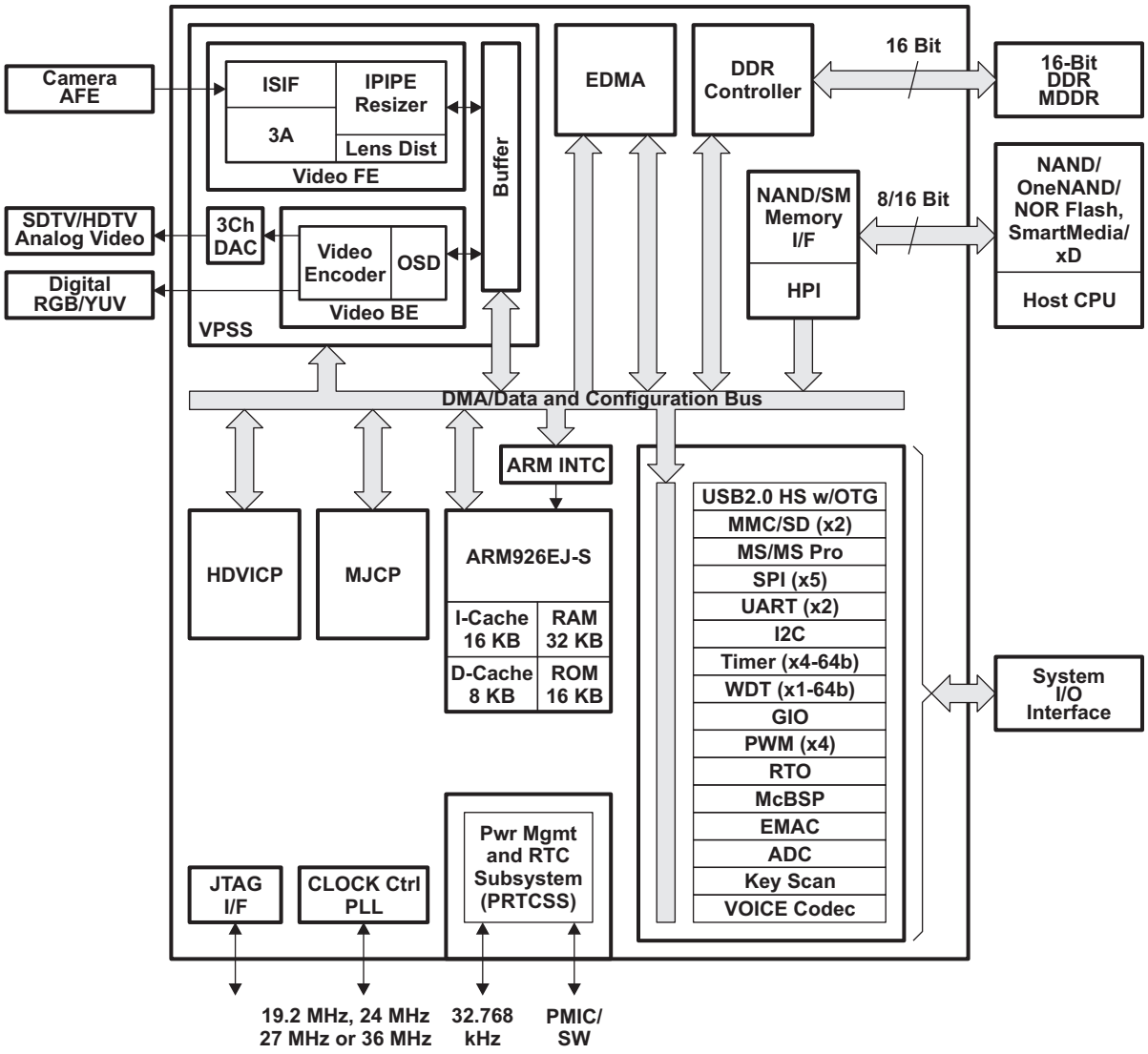
Video Processing Front End (VPFE)

1 Introduction

The TMS320DM36x Digital Media System-on-Chip (DMSoC), Figure 1, is a highly integrated, programmable platform for digital still/video cameras and other mobile imaging devices. Designed to offer camera manufacturers the ability to produce affordable DSC products with high picture quality, this device combines programmable image processing capability with a highly integrated imaging peripheral set.

The device contains an ARM9 RISC CPU and a proprietary DSP-based imaging co-processor subsystem. Together, they enable device manufacturers to implement their own proprietary image processing algorithms in software. This device also enables seamless interface to most additional external devices required for a digital camera digital sub-chip implementation via the Video Processing Front End Subsystem (VPFE). The interface is flexible enough to support various types of CCD and CMOS sensors, signal conditioning circuits, power management, SDRAM, SRAM, shutter, Iris and auto-focus motor controls. A block diagram of this device is shown in Figure 1.

Figure 1. Functional Block Diagram

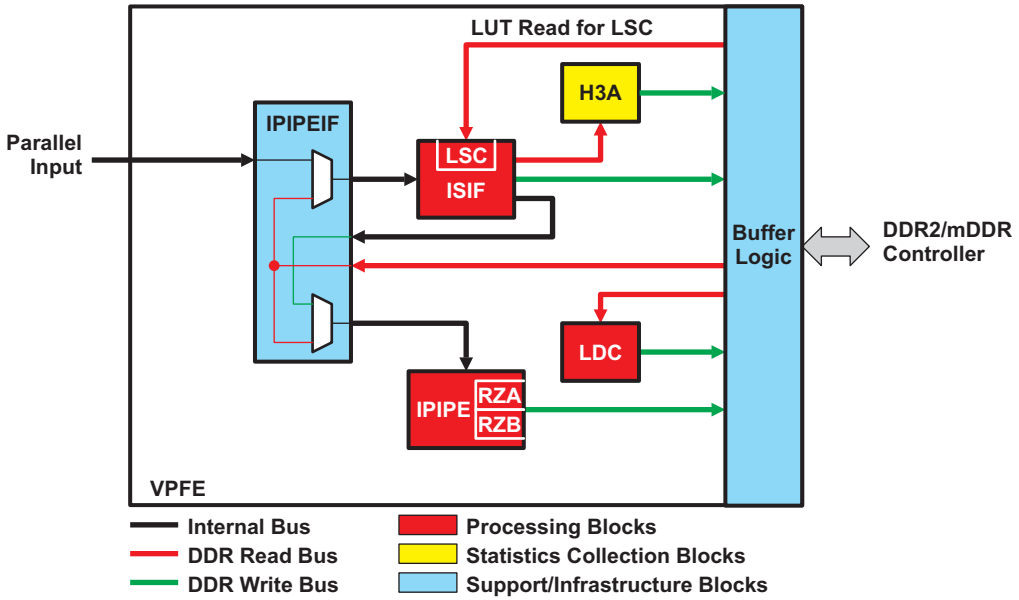


1.1 Purpose of the Video Processing Front End

The device contains a Video Processing Subsystem (VPSS), Figure 2, that provides an input interface (Video Processing Front End or VPFE) for external imaging peripherals such as image sensors, video decoders, and so on; and an output interface (Video Processing Back End or VPBE) for display devices, such as analog SDTV displays, digital LCD panels, and HDTV video encoders to name a few.

In addition to these peripherals, there is a set of common buffer memory and DMA controls to ensure efficient use of the DDR2/mDDR controller burst bandwidth. The buffer logic/memory is a unique block that is tailored for seamlessly integrating the VPSS into an image/video processing system. It acts as the primary source or sink to all the VPFE and VPBE modules that are either requesting or transferring data from/to DDR2/mDDR controller. In order to efficiently utilize the external DDR2/mDDR controller bandwidth, the buffer logic/memory interfaces with the DMA system via a high bandwidth bus (64-bit wide). The buffer logic/memory (divided into the read and write buffers and arbitration logic) is capable of performing the following functions. It is imperative that the VPSS utilize DDR2/mDDR controller bandwidth efficiently due to both its large bandwidth requirements and the real-time requirements of the VPSS modules.

Figure 2. Video Processing Subsystem (VPSS) Block Diagram



1.2 Features

The VPFE block is comprised of the Image Sensor Interface (ISIF), Image Pipe (IPIPE), Image Pipe Interface (IPIPEIF), Hardware 3A Statistic Generator (H3A), and Lens Distortion Correction (LDC) blocks. Together, these modules provide the device with a powerful and flexible front-end interface. These modules can be broken down into three distinct types. The first type consists of major processing modules that are in the direct data flow path and affect the input image data stream. These are described:

- The image sensor interface (ISIF) provides an interface to image sensors and digital video sources.
- The image pipe (IPIPE) is a parameterized hardwired image processing block whose image processing functions can be customized for each sensor type to realize good still image quality as well supporting video frame rates for digital still camera preview displays and video recording modes. An image resizer is also fully integrated within this module. Additionally, the IPIPE contains the following statistic collection functions: histogram, boxcar and the boundary signal calculator.
- The lens distortion correction (LDC) module operates on YCbCr data stored in SDRAM. LDC also performs chromatic aberration correction on RAW data.

The second group of modules are support or infrastructure modules. They are in the direct data flow path and affect the input image data, but are mainly intended to extend the functionality of the aforementioned major processing modules.

- The image IPIPE interface (IPIPEIF) module is an extension to the input interface to the ISIF and IPIPE modules. It can receive data from the sensor input, ISIF, and SDRAM. It performs some additional preprocessing operations on the data, and sends the resultant data to the ISIF and IPIPE.

In addition to the modules that directly affect input image data, there is one independent module that provides statistics on the incoming images to aid designers of camera systems.

- The hardware 3A (H3A) module is designed to support the control loops for auto focus (AF), auto white balance (AWB) and auto exposure (AE) by collecting metrics on the RAW image data from the image sensor interface (ISIF).

1.2.1 Image Sensor Interface (ISIF)

The ISIF is responsible for accepting RAW (unprocessed) image/video data from a sensor (CMOS or CCD). In addition, the ISIF can accept YCbCr video data in numerous formats, typically from so-called video decoder devices. In the case of RAW inputs, the ISIF output requires additional image processing to transform the RAW input image to the final processed image. This processing can be done in the image pipe (IPIPE) and lens distortion correction (LDC). The ISIF is programmed via control and parameter registers.

The ISIF module supports the following features:

- Conventional Bayer pattern, movie mode (for example, Panasonic/Sony), and Foveon sensor formats
- Various movie mode formats is provided via a data reformatter of ISIF, which transforms any specific sensor formats to the Bayer format. The maximum line width supported by the reformatter is 4736 pixels.
- Image processing steps applicable to Foveon sensors are limited to color-dependent gain control and black level offset control
- Progressive and interlaced sensors (hardware support for up to 2 fields and firmware support for higher number of fields, typically 3-, 4-, and 5-field sensors)
- Generates HD/VD timing signals and field ID to an external timing generator, or can synchronize to the external timing generator
- Up to 32K pixels (image size) in both the horizontal and vertical direction
- Up to 120 MHz sensor clock
- ITU-R BT.656/1120 standard format
- YCbCr 422 format, either 8- or 16-bit with discrete H and VSYNC signals
- Up to 16-bit input
- Sensor Data linearization
- Color space conversion

- Digital clamp with horizontal/vertical offset drift compensation
- Vertical Line defect correction based on a lookup table that contains defect position
- Programmable 2D-matrix Lens shading correction and offset control
- Color-dependent gain control and black level offset control
- Ability to control output to the SDRAM via an external write enable signal
- Down sampling via programmable culling patterns
- 12-bit to 8-bit DPCM compression
- 10-bit to 8-bit A-law compression
- Generating output to range 16-bits, 12-bits (12bit data pack allows for 33% saving in storage area), and 8-bits wide (8-bits wide allows for 50% saving in storage area).

1.2.2 The Image Pipe Interface (IPIPEIF)

The IPIPEIF is data and sync signals interface module for ISIF and IPIPE. Data source of this module is sensor parallel port, ISIF or SDRAM and the selected data is output to ISIF and IPIPE. This module also outputs dark frame subtraction (two-way) data which is generated by subtracting SDRAM data from sensor parallel port or ISIF data and vice versa. Depending on the functions performed, it may also readjust the HD, VD, and PCLK timing to the IPIPE and/or ISIF input.

The IPIPEIF module supports the following features:

- Up to 16-bit sensor data input
- Dark-frame subtract of raw image stored in SDRAM from image coming from sensor parallel port or ISIF
- 8-10, 8-12 DPCM decompression of 10-8, 12-8 DPCM compressed data from SDRAM
- Inverse ALAW decompression of RAW data from SDRAM
- (1,2,1) average filtering before horizontal decimation
- Horizontal decimation (downsizing) of input lines to <=2176 maximum required by the IPIPE
- Gain multiply for output data to IPIPE
- Simple defect correction to prevent a subtraction of defect pixel
- 8-bit, 12-bit unpacking of 8-bit, 12-bit packed SDRAM data

1.2.3 Image Pipe – Hardware Image Signal Processor (IPIPE)

The Image Pipe (IPIPE) is a programmable hardware image processing module that generates image data in YCbCr-4:2:2 or YCbCr-4:2:0 formats from raw CCD/CMOS data. The IPIPE can also be configured to operate in a resize-only mode, which allows YCbCr-4:2:2 or YCbCr-4:2:0 to be resized without processing every module in the IPIPE.

The following features are supported by the IPIPE:

- 12-bit RAW data image processing or 16-bit YCbCr resizing
- RGB Bayer pattern for input color filter array; does not support complementary color pattern, stripe pattern, nor Foveon sensors.
- Requires at least eight pixels for horizontal blanking and four lines for vertical blanking. In one shot mode, 16 blanking lines after processing area are required.
- Maximum horizontal and vertical offset of IPIPE processing area from synchronous signal is 65534
- Maximum input and output widths up to 2176 pixels wide (1088 for RSZ[2]).
- Raw pass-through mode for images can be wider than 2176 pixels (up to 8190 pixels)
- Automatic mirroring of pixels/lines when edge processing is performed so that the width and height is consistent throughout.
- Defect pixel correction using
  - Lookup table method that contains row and column position of the pixel to be corrected
  - On-the-fly adaptive method

- 2-D horizontal /vertical noise reduction filter
- Line crawl noise removal through green-imbalance-correction (GIC)
- Offset and gain control for white balancing at each color component (WB).
- CFA interpolation for good quality CFA interpolation with reduced false color artifacts (CFA module). CFA module also reduces aliasing caused by under sampling by Digital Anti Aliasing (DAA).
- Programmable RGB to RGB blending matrix (9 coefficients for the 3 × 3 matrix). (RGB2RGB module)
- Separate lookup tables for gamma correction on each of R, G and B components for display through piece-wise linear interpolation approach.
- Another programmable RGB to RGB blending matrix after gamma correction
- Look-up table based method to convert RGB data to RGB data using 9x9x9 table and tetrahedral interpolation.
- Programmable coefficients for RGB to YCbCr conversion
- Adjustable brightness and contrast tone through Global Brightness and Contrast Enhancement module. (GBCE module)
- 4:4:4 data to 4:2:2 data conversion by chroma low-pass filtering and down sampling to Cb and Cr. (4:4:4 to 4:2:2 module)
- Programmable look-up table for luminance edge enhancement. Adjustable brightness and contrast for Y component (Edge Enhancer module)
- Color artifacts reduction using gain control and 2D median filter (CAR module)
- Faulty color suppression filter (CGS module)
- Programmable down or up-sampling filter for both horizontal and vertical directions with range from 1/16x to 16x, in which the filter outputs two images with different magnification simultaneously (Resizer module)
- 4:2:2 to 4:2:0 conversion that can be done in the resizing block
- Different data formats [YCbCr (4:2:2 or 4:2:0), RGB (32bit/16bit), Raw data] are available while storing data in the SDRAM from IPIPE
- Flipping image horizontally and/or vertically
- Programmable histogram engine (4 windows, 256 bins)
- Boxcar calculation (1/8 or 1/16 size in each direction).
- Boundary signal calculation (row and column summations)

1.2.4 Hardware 3A (H3A)

The H3A module is designed to support the control loops for auto focus, auto white balance, and auto exposure by collecting metrics about the imaging/video data. The metrics are to adjust the various parameters for processing the imaging/video data. There are two main blocks in the H3A module:

- Auto focus engine
- Auto exposure and auto white balance engine

The AF engine extracts and filters the red, green, and blue data from the input image/video data and provides either the accumulation or peaks of the filtered output in a specified region. The specified region is a two-dimensional block of data and is referred to as a paxel when used with the auto focus engine (AF).

The AE/AWB engine accumulates the values and checks for saturated values in a sub-sampling of the video data. When used with the AE/AWB, the two-dimensional block of data is referred to as a window. Thus, other than referring them by different names, a paxel and a window are essentially the same thing. However, the number, dimensions, and starting position of the AF paxels and the AE/AWB windows are separately programmable.

1.2.4.1 Auto Focus Engine Features

The following features are supported by the AF engine:

- Peak mode in a paxel (a paxel is defined as a two dimensional block of pixels).
  - Accumulates the maximum focus value of each line in a paxel
- Accumulation/sum mode (instead of peak mode)
- Accumulates horizontal and vertical focus value in a paxel
- Focus value can be absolute value or square of the filter output
- Up to 12 paxels in the horizontal direction and up to 12 paxels in the vertical direction with vertical focus
- Up to 36 paxels in the horizontal direction and up to 128 paxels in the vertical direction with horizontal focus only
- Programmable width and height for the paxel. All paxels in the frame will be of the same size.
- Separate horizontal start for paxel and filtering
- Programmable vertical/horizontal steps within a paxel (vertical steps for vertical FV, horizontal steps for horizontal FV)
- Horizontal FV uses parallel IIR filters configured in a dual-biquad configuration with individual coefficients (2 filters with 11 coefficients each). The filters are intended to compute the sharpness/peaks in the frame to focus on.

1.2.4.2 Auto Exposure and Auto White Balance Features

The following features are supported by the AE/AWB engine:

- Accumulates clipped pixels along with all non-saturated pixels in each window per color
- Accumulates the sum of squared pixels in each window per color
- Minimum and maximum pixels values in each window per color
- Up to 36 horizontal windows with sum + {sum of squares or min+max} output.
- Up to 56 horizontal windows with sum output
- Up to 128 vertical windows
- Programmable width and height for the windows. All windows in the frame will be of same size.
- Separate vertical start coordinate and height for a black row of paxels that is different than the remaining color paxels
- Programmable horizontal sampling points in a window
- Programmable vertical sampling points in a window

1.2.5 Lens Distortion Correction (LDC)

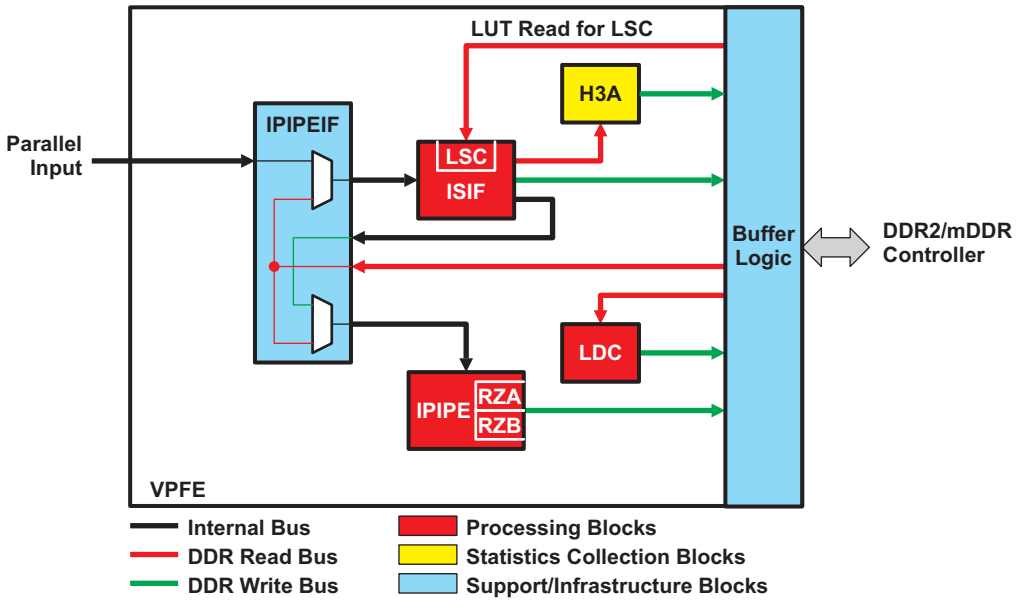
The LDC module is designed to correct barrel distortion due to the camera lens. The following features are supported by the LDC module:

- YCbCr 4:2:2/ 4:2:0 data format input/output for post-image-pipe correction
- Correct barrel distortion and pin-cushion distortion
- Radius-to-magnification-factor table to accommodate various distortion functions via programming
- Configurable center point and horizontal/vertical adjustment
- Same lookup table for Y, Cb and Cr
- 8-bit for YCbCr
- Bicubic interpolation for Y and bilinear interpolation for Cb/Cr
- Affine transformation for image warping, scaling, rotation
- Bayer-mode processing for chromatic aberration correction R and B correction only)
- Up to 16383 x 16383 image dimension

1.3 Functional Block Diagram

Figure 3 shows a high-level functional block diagram of the VPFE functional blocks, along with the different data flow paths. These data flow paths show how the various modules of the VPFE interact. The ISIF can also read the data from SDRAM via the IPIPEIF. The input to the H3A is only RAW sensor image data. The input to the IPIPE and LDC can be RAW or YCbCr video data.

Figure 3. Video Processing Front End (VPFE) Block Diagram and Data Flows



1.4 Supported Use Case Statement

The VPFE supports image data acquisition from sensor and digital video sources in various modes/formats. YCbCr sources have minimal image processing applied and can either be passed directly to external memory/SDRAM or passed through the IPIPE's resizer for scaling prior to writing to the SDRAM. RAW image data modes (non-YCbCr sources) are supported by the statistics collection modules (H3A, IPIPE's histogram, IPIPE's boundary signal calculator) as well as full image pipe processing functions, including resize.

The same processing options are supported when processing data sourced from the SDRAM. The IPIPEIF module can also perform dark frame subtraction on data from the SDRAM.

1.5 Industry Standard(s) Compliance Statement

ITU-R BT.601/656/1120

2 I/O Interfacing

2.1 Introduction

This section addresses the configuration of any external connections that the VPFE/ISP may have at the interface of the device, including I/O signals lists, I/O pin multiplexing, and protocol/data formats for typical application(s).

The VPFE signals are shown in Table 1. Note that these signals can take on different meanings depending on the specific interface chosen. All of the digital input signals below are multiplexed as GIO signals at reset (not shown in Table 1), and some are also multiplexed as SPI3 and USB signals. Pin multiplexing is controlled from the System Module level register PINMUX0 (0x01C40000). The default value of the PINMUX0 register is 0x0, which indicates that all the VPFE-related pins in the register are used for video input purpose after reset. However, it is suggested to configure the PINMUX0 register to the value 0xXXXX0000, where X is don't care, before any video capture. The following sections describe each of the input interface scenarios supported.

Table 1. Interface Signals for Video Processing Front End

Pin Name	Muxed With	I/O	Description
PCLK		Input	Pixel Clock
VD	GIO94	Bidi	V sync
HD	GIO95	Bidi	H sync
YIN7	GIO103/SPI3_SCLK	Bidi	C IN signal / C_DATA [15]
YIN6	GIO102/SPI3_SDO	Bidi	C IN signal / C_DATA [14]
YIN5	GIO101/SPI3_SDENA[0	Bidi	C IN signal / C_DATA [13]
YIN4	GIO100/SPI3_SDI3/SPI3_SDENA[1]	Bidi	C IN signal / C_DATA [12]
YIN3	GIO99	Bidi	C IN signal / C_DATA [11]
YIN2	GIO98	Bidi	C IN signal / C_DATA [10]
YIN1	GIO97	Bidi	C IN signal / C_DATA [9]
YIN0	GIO96	Bidi	C IN signal / C_DATA [8]
CIN7		Input	C IN signal / C_DATA [7]
CIN6		Input	C IN signal / C_DATA [6]
CIN5		Input	C IN signal / C_DATA [5]
CIN4		Input	C IN signal / C_DATA [4]
CIN3		Input	C IN signal / C_DATA [3]
CIN2		Input	C IN signal / C_DATA [2]
CIN1		Input	C IN signal / C_DATA [1]
CIN0		Input	C IN signal / C_DATA [0]
C_WE_FIELD	GIO93/CLKOUT0/USBDRVVBUS	Bidi	CCD Write Enable/Field ID signal

2.2 Signal Interface for Different Input Data Formats

The ISIF (VPFE interfacing module with external parallel port video input) interface signals are listed in Table 4. The interface consists of a set of signals used to transfer raw sensor data from an imager to the ISIF. Additionally, the ISIF can be configured to operate in a mode that adheres to the ITU-R BT.601/656/1120 interface specification. The ITU-R BT.601/656/1120 specification provides a standard method to transfer YCbCr-4:2:2 formatted video data. The ISIF supports 8 to 16-bit wide RAW data signals and 8/16-bit YCbCr signals as shown in Table 2.

Table 2. Data Input Formats

Port Name	Sensor (16-bit Raw)	16-bit YCbCr	8-bit YCbCr	
YIN7	C_DATA15	Y7	Y7, Cb7, Cr7	(YCSWP = 1)
YIN6	C_DATA14	Y6	Y6, Cb6, Cr6	
YIN5	C_DATA13	Y5	Y5, Cb5, Cr5	
YIN4	C_DATA12	Y4	Y4, Cb4, Cr4	
YIN3	C_DATA11	Y3	Y3, Cb3, Cr3	
YIN2	C_DATA10	Y2	Y2, Cb1, Cr,1	
YIN1	C_DATA9	Y1	Y1,Cb1, Cr1	
YIN0	C_DATA8	Y0	Y0, Cb0, Cr0	
CIN7	C_DATA7	Cb7,Cr7	Y7, Cb7, Cr7	(YCSWP = 0)
CIN6	C_DATA6	Cb6,Cr6	Y6, Cb6, Cr6	
CIN5	C_DATA5	Cb5,Cr5	Y5, Cb5, Cr5	
CIN4	C_DATA4	Cb4,Cr4	Y4, Cb4, Cr4	
CIN3	C_DATA3	Cb3,Cr3	Y3, Cb3, Cr3	
CIN2	C_DATA2	Cb2,Cr2	Y2, Cb2, Cr2	
CIN1	C_DATA1	Cb1,Cr1	Y1, Cb1, Cr1	
CIN0	C_DATA0	Cb0,Cr0	Y0, Cb0, Cr0	

When the number of RAW data line is less than 16, data can be connected to the upper or lower lines of C_DATA[15:0]. Lines not connected should be tied low. As shown in Table 3, the GWDI register should be configured properly so that the MSB of the input is connected to the MSB of the 16-bit data bus in ISIF.

Table 3. RAW Data Connection

GWDI	16-bit Data Bus in ISIF
0	C_DATA[15:0]
1	C_DATA[14:0] & 0
2	C_DATA[13:0] & 00
3	C_DATA[12:0] & 000
4	C_DATA[11:0] & 0000
5	C_DATA[10:0] & 00000
6	C_DATA[9:0] & 000000
7	C_DATA[8:0] & 0000000
8	C_DATA[7:0] & 00000000

2.3 Typical ISIF Interface

The ISIF controls timing of the interface using the HD, VD, field ID, pixel clock, and write enable signals. The ISIF can either provide HD, VD, and field ID signals to the sensor or it can use the HD, VD, and field ID signals provided by the CCD imager. The pixel clock clocks data into the ISIF at a maximum rate of 120 MHz.

When the ISIF is configured to write data to SDRAM, the write enable signal allows an external device to control which data to be written to the SDRAM. To enable the filed ID input, bit-5 of the MODESET.SWEN register should be set to interlace mode. To enable the write enable signal, bit-7 of the MODESET.CCDMD register should be set.

Note: Since the field ID and the write enable signal share the same PIN, only one of them can be connected.

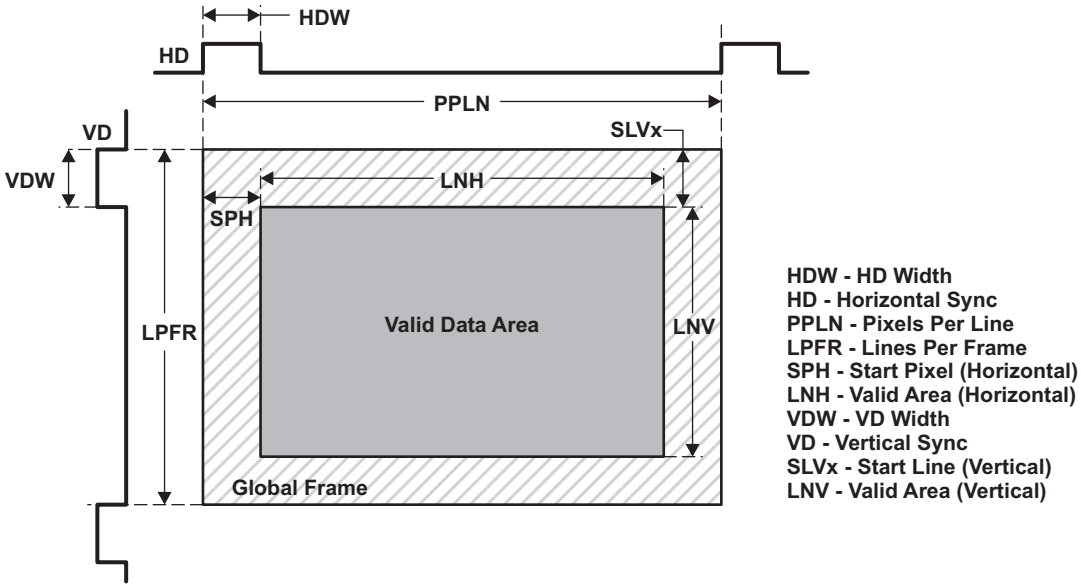
Table 4. ISIF Signal Interface

Name	I/O	Function
C_DATA[15:0]	I	Image data loaded from sensor. Bit width can be configured from 8 to 16 bits. The polarity of the input image data can be inversed by setting the MODESET.DPOL bit.
C_VSYNC (VD)	I/O	VSYNC. Vertical sync signal. This signal can be configured as an input or an output by setting MODESET.HDVDD bit. When configured as an input, the external sensor must supply the VD signal. When configured as an output the ISIF will supply the VD signal and VDW and LPFR registers must be configured. The polarity of VD can be inversed by setting the MODESET.VDPOL bit.
C_HSYNC (HD)	I/O	HSYNC. Horizontal sync signal. This signal can be configured as an input or an output by setting MODESET.HDVDD bit. When configured as an input, the external sensor must supply the HD signal. When configured as an output the ISIF will supply the HD signal and HDW and PPLN registers must be configured. The polarity of HD can be inversed by setting the MODESET.HDPOL bit.
C_FIELD	I/O	Field identification signal. This signal can be configured as an input or an output by setting MODESET.FIDD bit. When configured as an input, the external sensor must supply the field identification signal. When configured as an output, the ISIF will supply the field identification signal. When in input mode, the field ID can be configured to be latched by the VD signal. The polarity of the field ID can be inversed by setting the MODESET.FIPOL bit.
C_WEN	I	Write enable signal used to store valid frame data in SDRAM.
C_PCLK	I	Pixel clock. This signal is the pixel clock used to load image data into the ISIF. The Clock controller can configure to trigger on the rising or falling edge of the PCLK signal by setting the bit VPSS_CLK_CTRL.PCLK_INV in SYSTEM module registers. The maximum pixel clock rate is 120 MHz.

2.4 Timing Generator

The timing generator uses external sync signals (HD/VD) or provides internally generated timing signals to an imager. The CPU can control width, polarity, and position of the internally generated signals. Figure 4 shows ISIF register settings for the frame setup. The shaded area indicates the size of the physical image and the gray area indicates the valid data which can be written to the DDR/SDRAM. The vertical start position for even and odd fields can be configured separately.

Figure 4. Frame Image format



2.5 SDRAM RAW Data Storage

Data are stored to the lower bits of a 16-bit DDR/SDRAM word, or can be 8 bits or 12 bits packed. Raw data to be stored can be right-shifted according to the value set at CCDW.

Table 5 shows the format where data are stored to the lower bits of a 16-bit word and also the format that data are packed to 8 bits. The unused bits are filled with zeros.

Table 5. SDRAM RAW Data Format (1)

	CCDW	SDR Pack	Upper Word		Lower Word	
			MSB(31)	LSB(16)	MSB(15)	LSB(0)
12-bit	0	0	0	Pixel1	0	Pixel0
11-bit	1	0	0	Pixel1	0	Pixel0
10-bit	2	0	0	Pixel1	0	Pixel0
9-bit	3	0	0	Pixel1	0	Pixel0
8-bit	4	0	0	Pixel1	0	Pixel0
8-bit pack	4	2	Pixel3	Pixel2	Pixel1	Pixel0

Table 6 shows the format in which 12-bit data are packed.

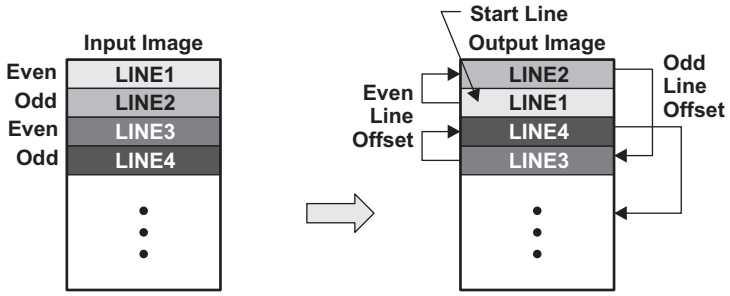
Table 6. SDRAM RAW Data Format (2)

	CCDW	SDR Pack	Upper Word				Lower Word	
			MSB(31)			LSB(16)	MSB(15)	LSB(0)
12-bit pack	0	1	Pixel2[7:0]				Pixel1	Pixel0
			Pixel5[3:0]		Pixel4		Pixel3	Pixel2[11:8]
				Pixel7			Pixel6	Pixel5[11:4]

The ISIF has an internal FIFO. The processed Data are transferred from the FIFO to the buffer logic in 32-byte burst unit. The frequency of the SDRAM clock must be equal to or higher than the pixel clock. Data are written to SDRAM only if DWEN in SYNCEN is set to “1.”

The output formatter can configure to any image format by using SDRAM line offset register, and offset control registers. Figure 5 shows how to construct a frame format in SDRAM.

Figure 5. Frame Image Format Conversion



2.6 ITU-R BT.656/ 1120 4:2:2 Parallel Interface

The ITU-R BT.656 signal interface, shown in ITU-R BT.656 (sometimes referred to as REC656), is a specification that provides a method to transfer YCbCr-4:2:2 formatted, digital video data over an 8/10-bit wide interface. Data and timing codes (data along with sync signals) are transferred over the same 8/10-bit interface.

To enable ITU-R BT.656 mode, set R656ON in REC656IF register. When in ITU-R BT.656 mode, only the data lines and clock signal are connected between the external device and the ISIF. A NTSC/PAL decoder is an example of an external device that may be connected to the ITU-R BT.656 interface.

Data lines C7-C0 are used for 8-bit YCbCr data and data lines Y1-Y0, C7-C0 are used for 10-bit YCbCr data. The video timing signals, HD, VD, and FIELD, are generated internally by the ISIF.

Since the sync information is carried along with the data lines, there are no sync signal interfaces or ISIF configuration setting to make, other than the start/end pixels and the line length and vertical frame size. The signal interface is described in Table 7.

Table 7. ITU-BT.656 Interface Signals

Name	I/O	Description
C_DATA[9:0]	I	Image Data. Mode set by REC656IF.R656ON bit. • Bit width can be configured to either 8 or 10 bits (CCDCFG.BW656) bit. • The polarity of the input image data can be reversed (MODESET.DPOL) bit
PCLK	I	Pixel clock. This signal is used to load the image data into the ISIF • • The ISIF can be configured to capture on either the rising of falling edge of the PCLK signal by setting the bit VPSS_CLK_CTRL.PCLK_INV in SYSTEM module registers

At the start and end of each video data block the device sends a unique timing reference code. The start code is called the start of active video signal (SAV), and the end code is called the end of active video signal (EAV). The SAV and EAV codes proceed and follow valid data as shown in Figure 6. HD, VD, and FIELD are generated internally by the ISIF based on the SAV and EAV codes. The delay between the end of the HD pulse and the start of valid data can be configured by setting SPH and the length of valid data can be configured by setting LNH.

Both timing reference signals, SAV and EAV, consist of a four word sequence in the following format: FF 00 00 XY, where FF 00 00 are a set preamble and the fourth word defines the field identification, the state of vertical field blanking, the state of horizontal line blanking, and error correction codes. The bit format of the fourth word is shown in Table 8 and the definitions for bits, F, V, and H, are given in Figure 6. F, V, and H are used in place of the usual horizontal sync, vertical sync, and blank timing control signals. Bits P3, P2, P1, and P0 are error correction bits for F, V, and H. The relationship between F, V, and H and the error correction bits is given in Table 10. To enable error correction, set bit ECCFVH in REC656IF. The ISIF will automatically detect and apply error correction when ECCFVH is enabled.

Figure 6. ITU-R BT.656 Signal Interface

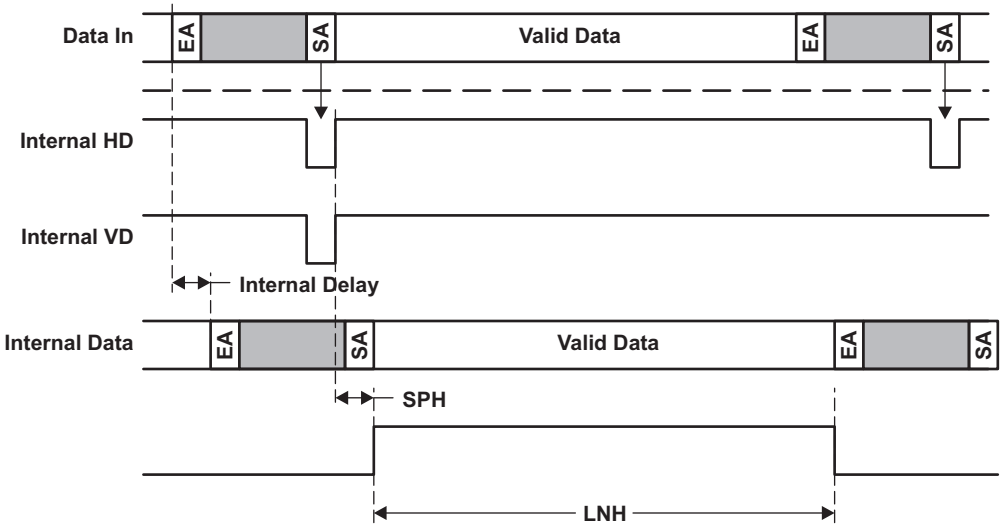


Table 8. Video Timing Reference Codes for SAV and EAV

Data Bit Number	First Word	Second Word (00)	Third Word (00)	Fourth Word (XY)
7 (MSB)	1	0	0	1
6	1	0	0	F
5	1	0	0	V
4	1	0	0	H
3	1	0	0	P3
2	1	0	0	P2
1	1	0	0	P1
0 (LSB)	1	0	0	P0

The details of F, V, and H are given in Table 9 and Table 10. P0-P3 are the protection bits.

Table 9. F, V, H Signal Descriptions

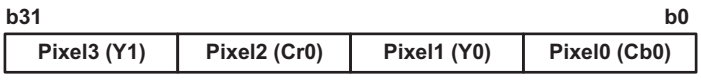
Signal	Value	Command
F	0	Field 1
	1	Field 2
V	0	0
	1	Vertical blank
H	0	SAV
	1	EAV

Table 10. F, V, H Protection Bits

F	V	H	P3	P2	P1	P0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

When operating in REC656 mode, data is stored in SDRAM according to the format shown in Figure 7.

Figure 7. BT.656 Mode Data Format in SDRAM



For BT.1120, Data width is 16 bits and the registers would be configured as:

MODESET.INPMOD = 1 .... YCbCr16bit

REC656IF.R656ON = 1 .... ITU-R BT.656 interface mode set

CCDCFG.BW656 = 0 .... SYNC detection on C7-C0

2.7 Generic YCbCr Interface Configuration

The ISIF module can accept generic YCbCr-4:2:2 formatted digital video data over an 8/16 bit wide interface. Note that the BT.656 specification is for 525-line and 625-line, digital component video signals in compliance with BT.601.

2.7.1 Generic YCbCr Configuration Signal Interface

Table 11 shows the interface connections for the generic YCbCr interface.

Unlike the BT.656 mode, discrete HD, and VD signals are required. An NTSC/PAL decoder is an example of an external device that may be connected to the YCbCr interface.

In 8-bit mode, data lines YIN[7:0] and CIN[7:0] can be used for input. When using an 8-bit interface, the CIN[7:0] inputs are typically used. However, either set of data inputs can be used or, alternately, two separate imagers can be physically connected (but only one can be active at any given time). A register setting (`CCDCFG.YCINSWP`) determines which set of 8-bit inputs are active. Note that if only the lower 8 bits are used, an additional SPI can be supported in this mode without interference.

In 16-bit mode, data lines YIN[7:0] and CIN[7:0] are used for input with the Cr/Cb data multiplexed on the CIN[7:0] signals. A register setting (`CCDCFG.YCINSWP`) can be used to swap the Y and Cr/Cb data lines.

Table 11. Interface Signals for Generic YCbCr Mode

Pin Name	I/O	Description
PCLK	Input	Pixel Clock
VD	Bidi	V sync
HD	Bidi	H sync
CIN7	Input	C IN signal
CIN6	Input	C IN signal
CIN5	Input	C IN signal
CIN4	Input	C IN signal
CIN3	Input	C IN signal
CIN2	Input	C IN signal
CIN1	Input	C IN signal
CIN0	Input	C IN signal
YIN7	Bidi	Y IN signal
YIN6	Bidi	Y IN signal
YIN5	Bidi	Y IN signal
YIN4	Bidi	Y IN signal
YIN3	Bidi	Y IN signal
YIN2	Bidi	Y IN signal
YIN1	Bidi	Y IN signal
YIN0	Bidi	Y IN signal

2.7.2 Generic YCbCr Configuration Signal Interface Description

The digital YCbCr interface supports either 8-bit or 16-bit devices. The signal interface is described in Table 12.

Table 12. YCbCr Interface Signals

Name	I/O	Description
CCD[15:0] = YI[7:0] / CI[7:0]	I	Image data. Mode set by INPMOD (not R656ON). • Bit width can be can be configured between 8 and 16 bits BW656 • The polarity of the input image data can be reversed DPOL • When 16-bit interface is used, the Y and C inputs can be swapped (YCINSWP) • When 8-bit interface is used, either half of the bus can be connected (YCINSWP) • When 8-bit interface is used, the position of the Y data can be set to either the even or odd pixel (Y8POS)
VD	I/O	VSYNC. This vertical sync signal can be configured as an input or an output HDVDD. • When configured as an input, the signal source must supply the VD signal • When configured as an output, supplies the VD signal and the Vd width and lines per frame must be configured (VDW, LPFR) • The polarity of VD can be reversed. (VDPOL)
HD	I/O	HSYNC. This horizontal sync signal can be configured as an input or an output HDVDD. • When configured as an input, the signal source must supply the HD signal • When configured as an output, supplies the HD signal and the Hd width and pixels per line must be configured (HDW, PPLN) • The polarity of HD can be reversed (HDPOL)
C_WE_FIELD	I	Field identification signal (optional – CCDMD) • Supplied by the external signal source • Can be configured to be latched by the VD signal (FIDMD) • The polarity of the field identification signal can be reversed FIPOL
PCLK	I	Pixel clock. This signal is used to load image data into the ISIF. • The ISIF can be configured to capture on either the rising or falling edge of the PCLK signal (PCLK_INV in SYSTEM module)

2.7.3 Generic YCbCr Configuration Protocol and Data Formats

In 8-bit mode, the position on the Y data in relation to Cr/Cb data can be configured by the register setting:`CCDCFG.Y8POS`.

The byte ordering of data can be swapped by the register setting: `CCDCFG.BSWD`.

Table 13. DDR2/mDDR Controller Storage Format for YCbCr Processing

	Upper Word		Lower Word	
SDRAM Address	MSB(31)	LSB(16)	MSB(15)	LSB(0)
N	Y1	Cr0	Y0	Cb0
N + 1	Y3	Cr2	Y2	Cb2
N + 2	Y5	Cr4	Y4	Cb4

2.7.4 SPI and GIO Signal Multiplexing

The SPI3 peripheral and several GIOs may be made available to the system, depending on the pin usage of the particular capture mode used by the VPFE. shows which pins are required by the VPFE for particular image capture modes and which pins can be made available for use by the SPI3 peripheral and/or extra GIOs. The PINMUX0 register shown in must be programmed according to the appropriate capture mode.

2.7.5 Y/C Data BUS Swap

There is an option to swap the upper and lower portion of the 16-bit YCbCr data bus (`ISIF.CCDCFG.YCINSWP`). This will swap the luma and chroma samples in 16-bit YCbCr mode. This will determine which half of the bus is used as the input source in 8-bit mode and can be used in 8-bit YCbCr mode to support two separate YCbCr input ports.

2.7.6 WEN/FIELD Signal Selection

Since the field ID and the write enable signal share the same pin, only one of these external signals can be connected. To enable the FIELD ID input, bit 7 of the ISIF.MODESET register should be set to INTERLACE MODE. To enable the write enable (WEN) signal, bit 5 of the ISIF.MODESET register should be set. These two bits should not be set concurrently or indeterminate results may occur.

2.7.7 Pin Mux 0 Register (PINMUX0)

The PINMUX0 register controls pin multiplexing for the VPFE pins. The pin mux 0 register (PINMUX0) is shown in and described in the *System Control Module* chapter. The address for this register is 0x01C4:0000.

3 Integration

This section describes how the VPFE/ISP subsystem is integrated into the device, including any interactions it may have with other subsystems on the device.

3.1 Clocking, Reset and Power Management Scheme

3.1.1 Clocks

There are six clock domains in the VPFE.

Table 14. Clock Domains

Name	Frequency	Description	Max Frequency
MMR	PLL0 SYSCLK4	Used for clocking the memory-mapped register (MMR) port for the control registers	121.5 MHz
DMA	PLL0 SYSCLK4	Used for clocking the DMA port for data transfers to and from the SDRAM EMIF	121.5 MHz
VPSSCLK	PLL0 SYSCLK4	Used for clocking the VPFE module internal logic. Also used to generate the IPIPEIF_PCLK	121.5 / 243 MHz
PSYNCCLK	PCLK	PCLK synchronized with the VPFE MMR clock	121.5 MHz
PCLK		The generic term PCLK in this document is an acronym for the pixel clock. There are two separate sources for the PCLKs that clock the pixels through the various VPFE modules	120 MHz
		External PCLK - if the ISIF receives data from the parallel imager input, then this is the external pixel clock (PCLK) driven by the input imager	
		IPIPEIF_PCLK - the pixel clock output of the IPIPEIF (for clocking data from SDRAM) generated from a divided down VPSSCLK according to the IPIPEIF.CLKDIV register field. Set the IPIPEIF.CFG1.CLKSEL to 1 in this case	
Crystal Clock	XTALCLK	Crystal clock	up to 48MHz

Note that there is an option to drive the VPBE module with the VPFE pixel clock (PCLK).

3.1.2 Resets

The VPFE module resets are tied to the device reset signals.

In addition, the VPSS modules can be reset by transitioning to the SyncReset state of the Power Sleep Controller (PSC). Note that the VPSS has two module domains, the VPSSmstr processing domain and the VPSSslv register interface.

3.1.3 Power Management

When powered, the VPFE modules utilize auto clock gating on a clock-by-clock basis to conserve dynamic power during periods of inactivity. When the VPSS is not required for the application, its MMR clocks (VPSSslv) and operating clocks (VPSSmstr) can be gated by the PSC to conserve dynamic power.

Additionally, when certain submodules within the VPFE are not required for the application mode, they can be disabled by software by configuring the ISP.PCCR register appropriately.

3.2 Hardware Requests

The VPSS can generate the 25 interrupts/events shown in Table 15. However, only nine of them can be sent to the ARM as interrupts and four of them can be sent to the EDMA as events. A mapping of which events are sent to the ARM and EDMA can be configured in the ISP.INTSEL[1:3] and ISP.EVTSEL registers respectively. The ISP.INTSTAT register can also be used to poll for events. More details on each module's events can be found in Table 15.

Table 15. VPSS Events

Event Number	Acronym	Module	Description
0	ISIF_INT0	ISIF	Triggered after a programmable number of input lines for each frame(VDINT0)
1	ISIF_INT1	ISIF	Triggered after a programmable number of input lines for each frame (VDINT1)
2	ISIF_INT2	ISIF	Triggered after a programmable number of input lines for each frame (VDINT2)
3	LSC_INT	ISIF	LSC interrupt muxed by 2DLSCIRQEN register
4	IPIPE_INT_REG	IPIPE	Triggered when IPIPE register update is allowed
5	IPIPE_INT_LAST_PIX	IPIPE	Triggered when the last pixel of a frame comes into IPIPE for each frame
6	Reserved		
7	IPIPE_INT_BSC	IPIPE	Triggered when boundary signal calculation is finished for each frame
8	IPIPE_INT_HST	IPIPE	Triggered when histogram processing is finished for each frame
9	IPIPEIF_INT	IPIPEIF	Triggered at the start position of VSYNC from parallel input- interface or ISIF (can be selected from IPIPEIF.CFG2.INTSRC bit)
10	AEW_INT	H3A	Triggered when auto exposure and auto white-balance processing is finished for each frame
11	AF_INT	H3A	Triggered when auto focus processing is finished for each frame
12	Reserved		
13	RSZ_INT_REG	Resizer	Triggered when the resizer register update is allowed
14	RSZ_INT_LAST_PIX	Resizer	Triggered when the last pixel of a frame comes into resizer for each frame
15	Reserved		
16	RSZ_INT_CYC_RZA	Resizer	Triggered when the number of lines programmed has been output of resizer-A for each frame
17	RSZ_INT_CYC_RZB	Resizer	Triggered when the number of lines programmed has been output of resizer-B for each frame
18	Reserved		
19	Reserved		
20	OSD_INT	OSD	Triggered at the end of each frame read from SDRAM (for VPBE)
21	VENC_INT	VENC	Triggered at the rising edge of VSYNC (for VPBE)
22	RSZ_INT_EOF0	Resizer	Triggered when writes to SDRAM(from both Resizer-A & Resizer-B) are finished for each frame. If both RSZ.RZA_420 and RSZ.RZB_420 are 2, then the interrupt is invalid.
23	RSZ_INT_EOF1	Resizer	Triggered when writes to SDRAM(from both Resizer-A & Resizer-B) are finished for each frame. If both RSZ.RZA_420 and RSZ.RZB_420 are 0 or 1, then the interrupt is invalid.
24	H3A_INT_EOF	H3A	Triggered at the same time as last process (AF or AEW) to finish for each frame (triggered when both AF and AEW processes are done)
25	IPIPE_INT_EOF	IPIPE	Triggered when boxcar's write to SDRAM transfer is finished for each frame
26	LDC_INT_EOF	LDC	Triggered when LDC processing is finished for each frame
27	IPIPE_INT_DPC_INI	IPIPE	This is a request to initialize both defect pixel table bank #0 and bank #1. Triggered when IPIPE.DPC_LUT_EN is 1 and the first valid pixel comes into IPIPE. If defect pixel tables are not ready, Firmware has to initialize them.
28	PIPE_INT_DPC_ RNEW0	IPIPE	This is a request to renewal defect pixel table bank #0. Triggered when the status of defect pixel table bank #0 changed to empty.
29	IPIPE_INT_DPC_ RNEW1	IPIPE	This is a request to renewal defect pixel table bank #1. Triggered when the status of defect pixel table bank #1 changed to empty.

3.2.1 Interrupt Requests

The nine interrupts selected in the ISP.INTSEL[1:3] registers are assigned to the ARM interrupt controller as shown in Table 16.

Table 16. ARM Interrupts - VPSS

INT Number	Acronym
0	VPSSINT0
1	VPSSINT1
2	VPSSINT2
3	VPSSINT3
4	VPSSINT4
5	VPSSINT5
6	VPSSINT6
7	VPSSINT7
8	VPSSINT8

VPSSINT0, VPSSINT7 and VPSSINT8 are multiplexed with the other module interrupts (NSFINT (noise filter) and IMXINT1 from IMCOP) in the system. The system level register, ARM_INTMUX, must be configured to select VPSSINT0, 7 and 8 interrupts for use. Corresponding bit fields in the ARM_INTMUX register are specified in Table 17.

Table 17. ARM_INTMUX Register (specified only VPSS interrupt mux)

Bits	Field Name	Description for ARM_INTMUX	Type	Reset
31	INT0	VPSS_INT0 or PBIST 0 = VPSS_INT0 1 = Reserved	R/W	0
26-15	Reserved		-	0
25	INT7	VPSS_INT7 or NSFINT 0 = VPSS_INT7 1 = NSFINT	R/W	0
24	INT8	VPSS_INT8 or IMXINT1 0 = VPSS_INT8 1 = IMXINT1	R/W	0

3.2.2 EDMA Requests

The four events selected in the ISP.EVTSEL register are assigned to the EDMA as shown in Table 18.

Table 18. EDMA Events - VPSS

Event Number	Binary	Event Name
4	0000100	VPSSEVT1
5	0000101	VPSSEVT2
6	0000110	VPSSEVT3
7	0000111	VPSSEVT4

There are two primary reasons for using an EDMA event from the VPSS. The first is to trigger an EDMA transfer of boundary signal vectors from the VPSS internal memory to external memory before they are overwritten by the next frame. The second is to allow for an update of the module registers by using the DMA scheme verses the direct CPU write. Normally, the ARM performs this function, but in some cases the ARM can be tied up with other activities and the interrupt latency is critical when dealing with the VPFE modules. Consider the following example: a still image is processed by the image pipe. Since an 8MP still image is too wide for a single pass through the image pipe, two passes are required. The image pipe registers need to be altered as soon as each pass is complete. Tying an IPIPE event to the EDMA allows instantaneous DMA of the new register settings for the subsequent passes.

3.3 VPSS Top-Level Register Mapping Summary

Table 19 provides a summary of the VPSS top-level register mapping.

Table 19. VPFE Module Register Map

VPSS Registers	Address Range		Size
ISP System Registers	0x01C70000	0x01C700FF	256B
VPSS System Registers	0x01C70200	0x01C702FF	256B
Resizer Registers	0x01C70400	0x01C77FF	1KB
IPIPE Registers	0x01C70800	0x01C70FFF	2KB
ISIF Registers	0x01C71000	0x01C711FF	512B
IPIPEIF Registers	0x01C71200	0x01C712FF	256B
H3A Registers	0x01C71400	0x01C714FF	256B
LDC Registers	0x01C71600	0x01C717FF	512B
OSD Registers	0x01C71C00	0x01C71CFF	256B
VENC Registers	0x01C71E00	0x01C71FFF	512B

3.4 VPSS Embedded Memory Mapping Summary

In the VPSS module, there are a few modules which *may* require their corresponding look-up tables (LUT) to be configured to the customer-specific values, and a few modules (histogram and BSC) output the results in the internal memory of the VPSS. The address map for those LUTs and internal memories is specified below.

Table 20. VPFE Embedded Memory Map

Embedded Memory	Module	Address Range	Size
IPIPE_HST_TB0	Histogram	0x01C72000 – 0x01C727FF	2KB
IPIPE_HST_TB1	Histogram	0x01C72800 – 0x01C72FFF	2KB
IPIPE_HST_TB2	Histogram	0x01C73000 – 0x01C737FF	2KB
IPIPE_HST_TB3	Histogram	0x01C73800 – 0x01C73FFF	2KB
IPIPE_BSC_TB0	BSC	0x01C74000 – 0x01C75FFF	8KB
IPIPE_BSC_TB1	BSC	0x01C76000 – 0x01C77FFF	8KB
IPIPE_DPC_TB0	Defect Pixel Correction	0x01C78000 – 0x01C781FF	512B
IPIPE_DPC_TB1	Defect Pixel Correction	0x01C78400 – 0x01C785FF	512B
IPIPE_YEE_TB	Edge Enhancer	0x01C78800 – 0x01C78FFF	2KB
IPIPE_GBC_TB	GBCE	0x01C79000 – 0x01C797FF	2KB
IPIPE_D3L_TB0	3D LUT	0x01C79800 – 0x01C79BFF	1KB
IPIPE_D3L_TB1	3D LUT	0x01C79C00 – 0x01C79FFF	1KB
IPIPE_D3L_TB2	3D LUT	0x01C7A000 – 0x01C7A3FF	1KB
IPIPE_D3L_TB3	3D LUT	0x01C7A400 – 0x01C7A7FF	1KB
IPIPE_GAMR_TB	Gamma Correction	0x01C7A800 – 0x01C7AFFF	2KB
IPIPE_GAMG_TB	Gamma Correction	0x01C7B000 – 0x01C7B7FF	2KB
IPIPE_GAMB_TB	Gamma Correction	0x01C7B800 – 0x01C7BFFF	2KB
ISIF_LIN_TB0	ISIF Linearization	0x01C7C000 – 0x01C7C1FF	512B
ISIF_LIN_TB1	ISIF Linearization	0x01C7C400 – 0x01C7C5FF	512B
LDC_LUT	LDC	0x01C7F000 – 0x01C7F3FF	1KB
OSD_CLUT	OSD (VPBE)	0x01C7F800 – 0x01C7FBFF	1KB

These embedded memories can be directly accessed by ARM through the configuration bus with exceptions for the LDC and OSD modules. The access path for the look-up tables for the LDC and OSD modules is controlled by the bit fields VPSS.VPBE_CLK_CTRL.LDC_CLK_SEL and VPSS.VPBE_CLK_CTRL.OSD_CLK_SEL, respectively. When these bit fields are set to 1, ARM can directly access the corresponding memories of the DC and OSD modules. Otherwise (by default), the memories can be accessed by the corresponding module configuration registers.

The LDC.LDC_LUT_ADDR, LDC.LDC_LUT_WDATA & LDC.LDC_LUT_RDATA registers are for LDC look-up table access and the OSD.CLUT_RAM_YCB & OSD.CLUT_RAM_CR registers are for OSD color look-up table access.

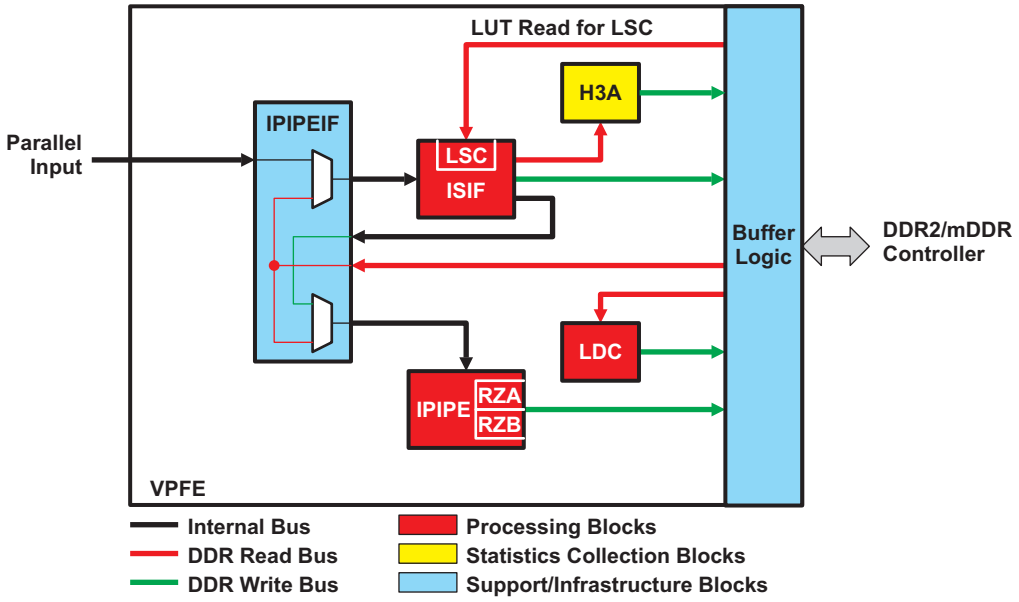
3.5 VPFE/ISP Top-Level Signal Interaction

The ISIF_VSYNC signal drives the event-trigger input signal of all four PWM modules. The PWM can configure the trigger to detect the rising or falling edge of the ISIF_VSYNC signal. This capability is provided to allow the PWM module to be used as an ISIF timer.

4 VPFE/ISP Functional Description

The VPFE block diagram is shown in Figure 8. Additional detailed block diagrams are shown in the interface and image processing subsections.

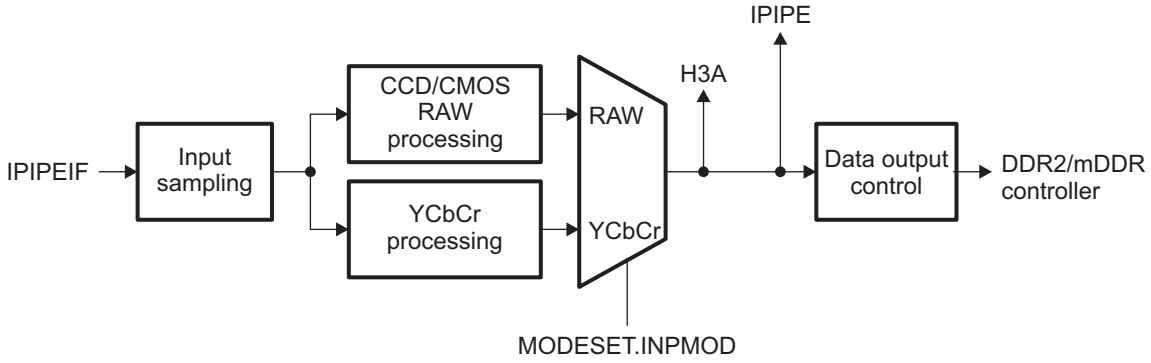
Figure 8. Video Processing Front End (VPFE) Block Diagram



4.1 Image Sensor Interface (ISIF)

The image sensor interface (ISIF) module interfaces with external image sources as well as CCD sensors. It supports both RAW Bayer data from CCD/CMOS sensors and processed YCbCr data from either a CMOS sensor with integrated image processing or a video decoder interface. A high-level block diagram of the ISIF module is shown in Figure 9.

Figure 9. Image Sensor Interface (ISIF) – Top Level Block Diagram

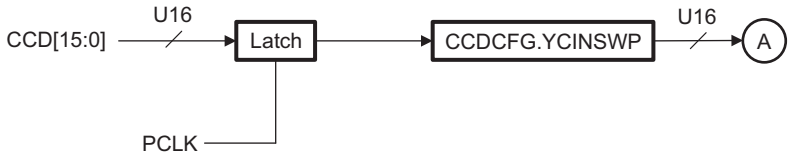


4.1.1 ISIF Input Sampling

The ISIF module input sampling and formatting are shown in Figure 10.

There is an option to swap the upper and lower portion of the 16-bit YUV data bus (CCDCFG.YCINSWP). This will swap the luma and chroma samples in 16-bit YUV mode and will determine which half of the bus is used as the input source in 8-bit mode, and which can be used in 8-bit YUV mode to support two separate YUV input ports. Since this bit affects both RAW and YUV input modes, CCDCFG.YCINSWP should always be set to '0' in RAW input mode (MODESET.INPMOD = 0).

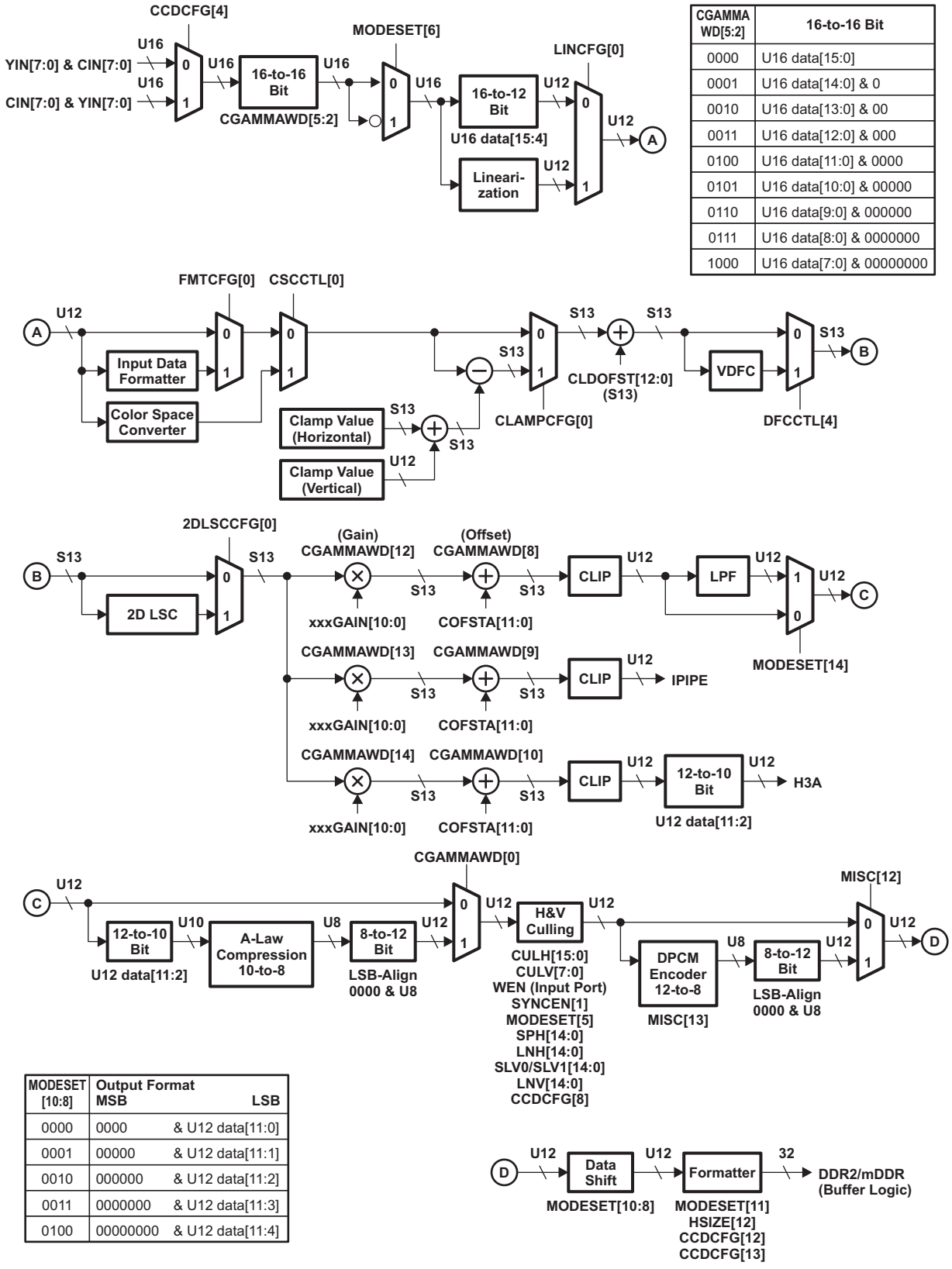
Figure 10. Image Sensor Interface - Input Formatting



4.1.2 ISIF Processing Data Flow

Figure 11 illustrates the raw data processing flow for the sensor interface.

Figure 11. Sensor Interface (ISIF) – RAW Data Processing Flow



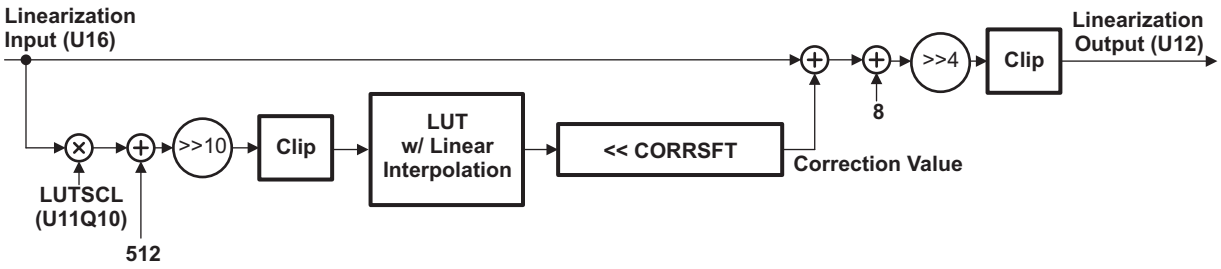
CGAMMAWD[5:2]	16-to-16 Bit
0000	U16 data[15:0]
0001	U16 data[14:0] & 0
0010	U16 data[13:0] & 00
0011	U16 data[12:0] & 000
0100	U16 data[11:0] & 0000
0101	U16 data[10:0] & 00000
0110	U16 data[9:0] & 000000
0111	U16 data[8:0] & 0000000
1000	U16 data[7:0] & 00000000

MODESET [10:8]	Output Format MSB	LSB
0000	0000	& U12 data[11:0]
0001	00000	& U12 data[11:1]
0010	000000	& U12 data[11:2]
0011	0000000	& U12 data[11:3]
0100	00000000	& U12 data[11:4]

4.1.3 Sensor Linearization

The sensor linearization module corrects the non-linear response of image sensors while capturing the image. A lookup table is programmed with an offset value to add to the original pixel value based on the original pixel value.

Figure 12. Linearization Block Diagram

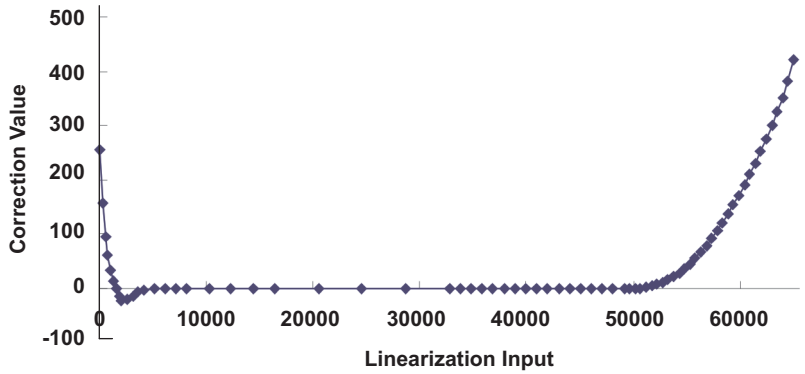


As shown in Figure 12 a scale factor is applied to the input prior to lookup.

scaled_input = (Linearization_in * LUTSCL + 512) >> 10
table_index = (scaled_input > 65535) ? 65535 : scaled_input
LUTSCL: Scale factor (U11Q10. Range: 0-1+1023/1024)

The lookup table is a sampling of the linearization correction curve based on calibration of the image sensor. Intermediate values between sampling points are computed using linear interpolation (see Figure 13).

Figure 13. Linearization Correction Curve



As shown in Table 21, the table has 192 entries, and the entire correction curve is divided into seven regions. The regions for the darkest part and the brightest part of the response curve have dense sampling.

Table 21. Linearization Lookup Table (LUT)

Region	Number of Sample Points	LUT Address
table_in[15:11] == 00000	32	table_in[10:6]
table_in[15:11] == 00001	4	table_in[10:9] + 32
table_in[15:12] == 0001	4	table_in[11:10] + 36
table_in[15:13] == 001	4	table_in[12:11] + 40
table_in[15:14] == 01	4	table_in[13:12] + 44
table_in[15:14] == 10	16	table_in[13:10] + 48
table_in[15:14] == 11	128	table_in[13:7] + 64

The LUT entries are signed 10-bit data. After linear interpolation, the correction value is left-shifted by a programmable amount (CORRSFT), and then added to the input. This is then converted to unsigned 12-bit by right-shift, followed by clipping.

```
x0 = LUT[table_index]
y0 = LUT[table_index + 1]
correction_value = ((1 – fraction) * x0 + fraction * y0) << CORRSFT
adjusted_value = (Linearization_in + correction_value + 8) >> 4
Linearization_out = (adjusted_value > 4095) ? 4095 :
                    ((adjusted_value < 0) ? 0 : adjusted_value)
CORRSFT: Shift value (U3. Range: 0-6)
```

If the linearization module is disabled, then the upper 12 bits of U16 input are sent to the next block.

4.1.3.1 Linearization LUT Memories

The LUT of 192 entries has to be filled in two memory regions in the interleaved manner as shown in Figure 14.

Figure 14. Linearization LUT memories

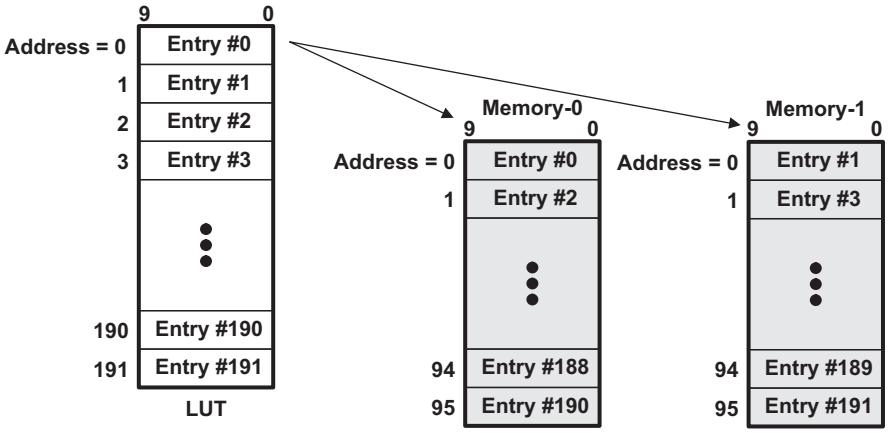


Table 22. LUT Memory Regions

Memory Region	Address Range	Description
ISIF_LIN_LUT0 (Memory-0)	0x01C7C000 – 0x01C7C1FF	ISIF Linearity Compensation LUT #0
ISIF_LIN_LUT1 (Memory-1)	0x01C7C400 – 0x01C7C5FF	ISIF Linearity Compensation LUT #1

4.1.4 Input Data Formatter

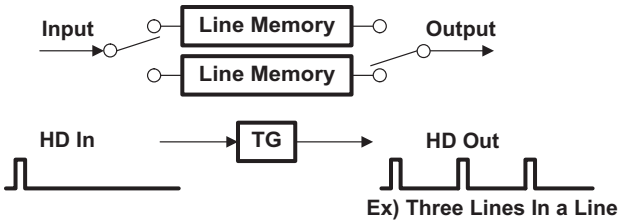
There are two functional blocks: input data formatter, and color space converter, which use two 4736 x 12 bits (corresponds to one line of maximum 4736 pixels with each pixel equal to 12 bits in size) memories. Only one of the functional blocks can be enabled in the flow at a given time as shown in Figure 12.

The data formatter block allows the ISIF to handle a wide variety of current and future readout schemes other than Bayer format. Two line memories and a programmable address generator are used to translate those patterns to that of a standard Bayer pattern (or any other pattern). This allows the back end processing (noise filters, interpolation, histogram, 3A statistics) to remain unchanged.

The data formatter block also supports “divided input lines.” If an input line is divided into multiple lines and fed to the ISIF, the formatter gathers the divided lines and organizes a single line. Up to four divided lines can be supported.

The data formatter can split an input line into 1, 2, 3, or 4 output lines, or can combine the divided 1, 2, 3, or 4 input lines into a single line. Figure 15 shows an example generating three output lines from an input line with a new, internally generated HD signal. This HD signal then gates the downstream processing rather than the original sensor HD signal. Details of how to configure the formatter are provided in the following sections.

Figure 15. Splitting an Input Line Into Three Output Lines



Since the size of the line memories is 4736 x 12 bits, the following restrictions apply for the data formatter.

Split Lines

- The maximum number of pixels that can be supported in an output line if the input line is transformed into one output line is 4736.
- The maximum number of pixels that can be supported in an output line if the input line is transformed into two output lines is 2368.
- The maximum number of pixels that can be supported in an output line if the input line is transformed into three output lines is 1578.
- The maximum number of pixels that can be supported in an output line if the input line is transformed into four output lines is 1184.

Combine Lines

- The maximum number of pixels that can be supported in an output line if one input line is transformed into an output line is 4736.
- The maximum number of pixels that can be supported in an output line if two input lines are transformed into an output line is 2368.
- The maximum number of pixels that can be supported in an output line if three input lines are transformed into an output line is 1578.
- The maximum number of pixels that can be supported in an output line if four input lines are transformed into an output line is 1184.

4.1.4.1 Formatter Area Settings

As shown in Figure 16 FMTSPH, FMTLNH, FMTSLV, and FMTLNV registers are used for the formatter area settings.

Figure 16. Data Formatter Area Settings

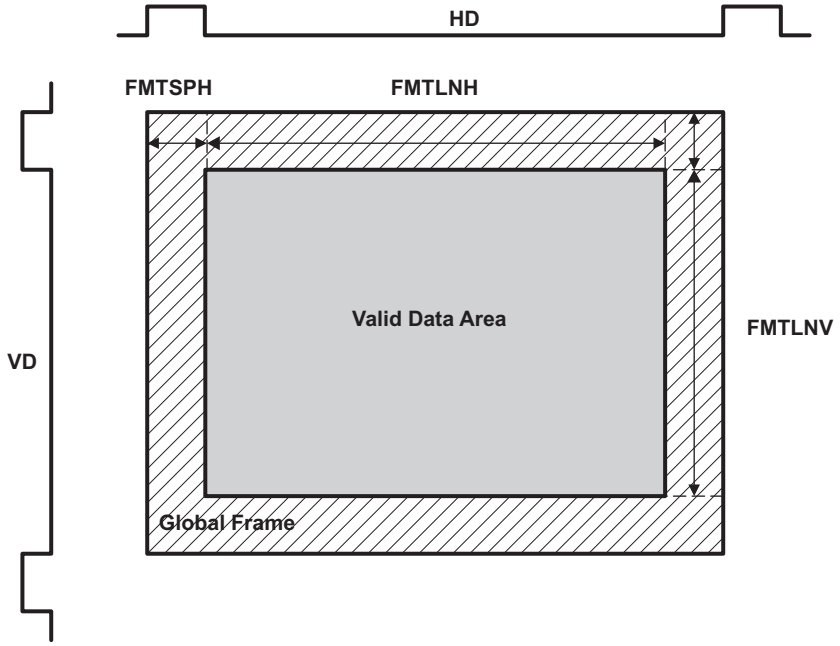


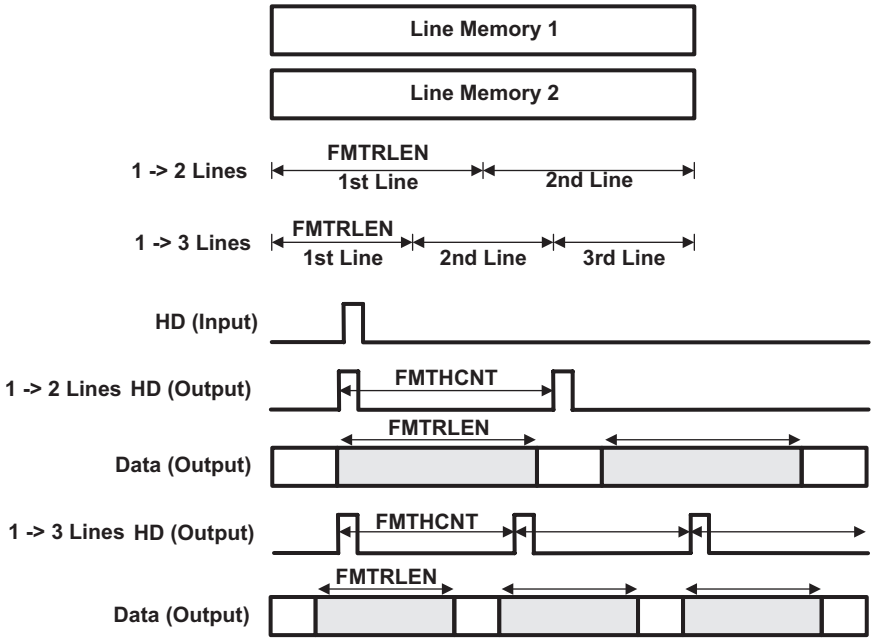
Table 23 explains some of the registers for the area settings. The input line is input to the formatter, and the output line is output from the formatter

Table 23. Formatter Area Setting Registers

Register	Description
FMTSPH	The first valid pixel of an input line
FMTLNH	Valid length of an input line = FMTLNH+1
FMTSLV	The first valid input line
FMTLNV	The number of the valid input lines = FMTLNV+1
FMTRLEN	The length of an output line
FMTHCNT	HD interval for output lines
SPH	The first pixel in an output line to be stored to SDRAM
LNH	Number of pixels in an output line to be stored to SDRAM = LNH+1
SLV	The line to start data storing to SDRAM. It is based on the input line count.
LNV	The number of the output lines to be stored to SDRAM = LNV+1

The number of pixels in an output line should be set to register FMTRLEN, and the HD output interval should be set to register FMTHCNT. There is no need to set FMTHCNT while combining the multiple input lines into a single line. Figure 17 shows the example to split an input line into two or three output lines.

Figure 17. Data Formatter Output Control



4.1.4.2 Formatter Programming

The data formatter derives its flexibility by supporting up to 16 different addresses and a program that can contain up to 32 entries.

4.1.4.2.1 Address Pointer

There are 16 address pointer registers (FMTAPTR0-15) which contain:

- LINE[1:0] : 2-bit line number to specify which output line it belongs to — 0, 1, 2, or 3. It's valid only for the line splitting.
- INIT[12:0] : 13-bit initial address

Each of the address values is either auto-incremented by programmable value (register: FMTAINC) or auto-decremented by the FMTAINC. This capability is the key for supporting a multitude of read-out patterns, including dual-tap AFE modules.

4.1.4.2.2 Program

There are 32 program entry registers which contain:

- PGMxxEN : Program entry valid flag
- PGMxxAPTR[2:0] : Specify the address pointer
- PGMxxUPDT: Address update (Increment or decrement)

Each of the program entries has a valid flag, so the formatter can also support images larger than the memory limit (length: 4480) by not choosing some of the entries. The total program memory of 32 entries is divided into either two or four SETs as shown below.

- Program memory of 16 entries each for odd and even lines – to split the line.
  - SET0 for even input line: Program entry 0-15

  - SET1 for odd input line: Program entry 16-3
- Program memory of eight entries for up to four input lines – to combine the lines
  - SET0 for 1st input line: Program entry 0-7
  - SET1 for 2nd input line: Program entry 8-15
  - SET2 for 3rd input line: Program entry 16-23
  - SET3 for 4th input line: Program entry 24-31

The number of program entries per SET must be specified by register FMTPLEN. Program entry should be set from the lower registers within a SET. For instance, start from Program entry 16 for odd input lines. The following examples show the programmability of the data formatter.

Figure 18. Conventional Read-Out Pattern

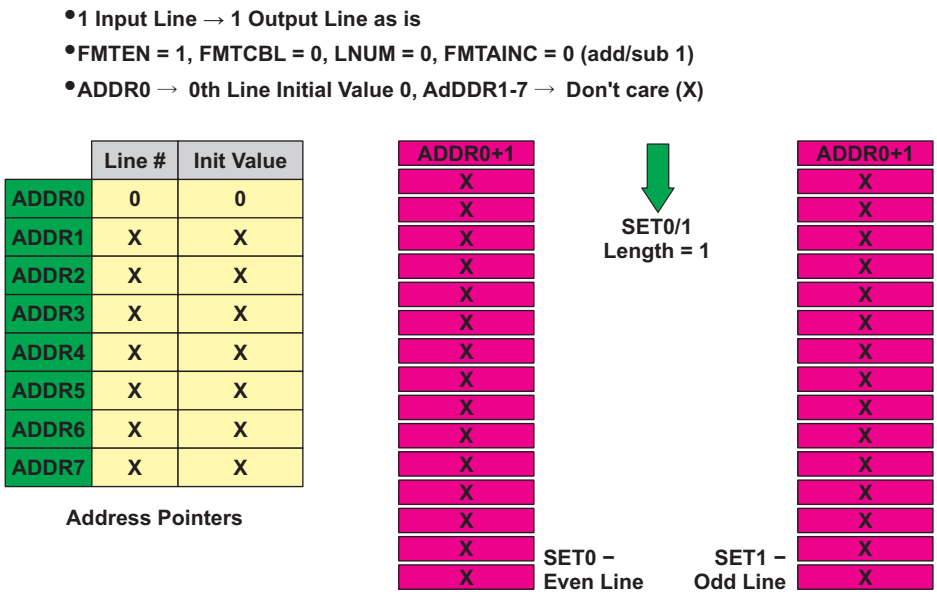


Figure 19. Conventional Read-Out Pattern with Two-tap AFE

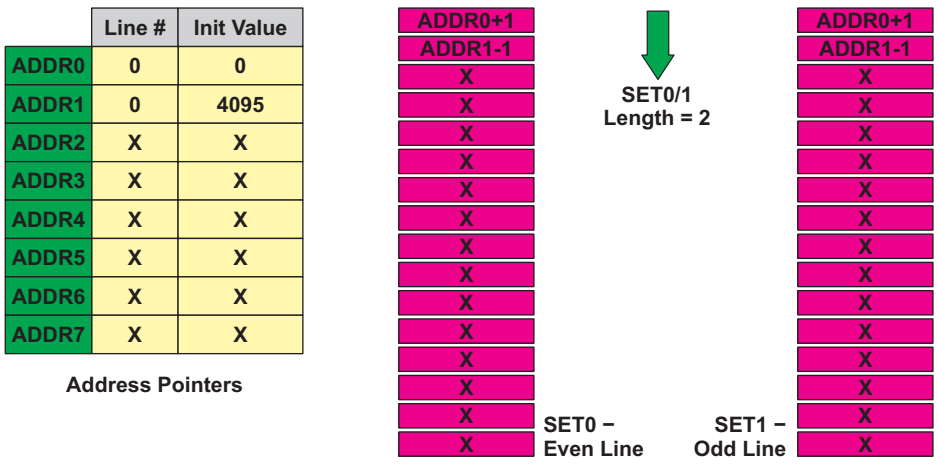
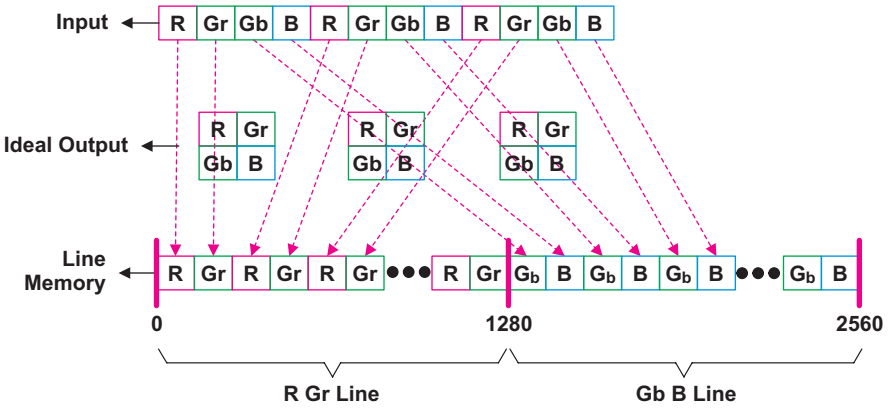


Figure 20. Example of SONY VGA CCD Configuration



- Input → 0, 1, 1280, 1281, 2, 3, 1282, 1283, ... and So On
- Output → 0, 1, 2, 3, ... and So On
- FMTEN = 1, FMTCBL = 0, LNUM = 1, FMTAINC = 0 (add/sub 1)
- Note: 1280 in Input Line is Equal to 0 in 2nd Output Line

	Line #	Init Value
ADDR0	0	0
ADDR1	1	0
ADDR2	X	X
ADDR3	X	X
ADDR4	X	X
ADDR5	X	X
ADDR6	X	X
ADDR7	X	X

Address Pointers

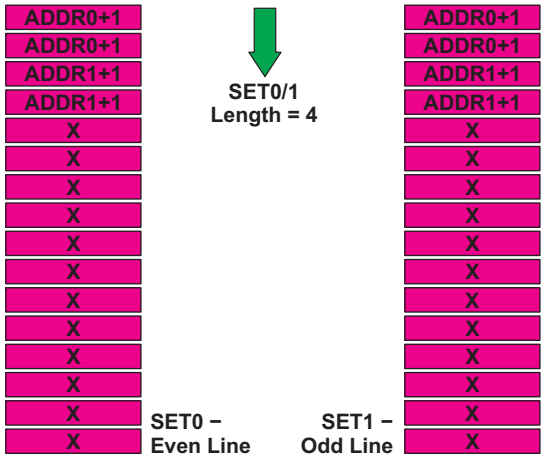


Figure 21. Example of SONY VGA CCD Configuration with Two-tap AFE

- Input → 0, 2559, 1, 2558,1280, 1279, 1281, 1278, 2, 2557, 3, 2556, ... and So On
- Output → 0, 1, 2, 3, ...and So On
- FMTEN = 1, FMTCBL = 0, LNUM = 1, FMTAINC = 0 (add/sub 1)
- NOTE: 2559 In Input Line is Equal to 1279 In 2nd Output Line.

	Line #	Init Value
ADDR0	0	0
ADDR1	1	1279
ADDR2	1	0
ADDR3	0	1279
ADDR4	X	X
ADDR5	X	X
ADDR6	X	X
ADDR7	X	X

Address Pointers

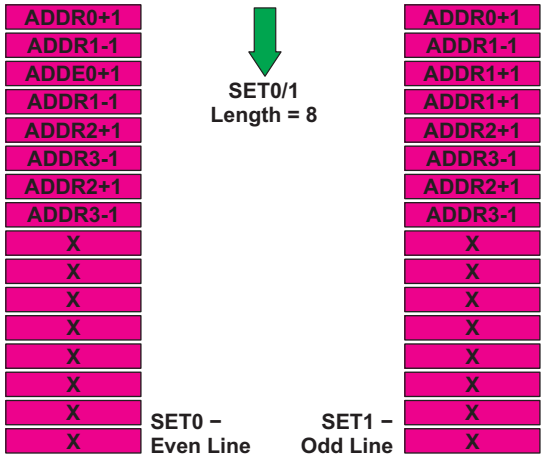
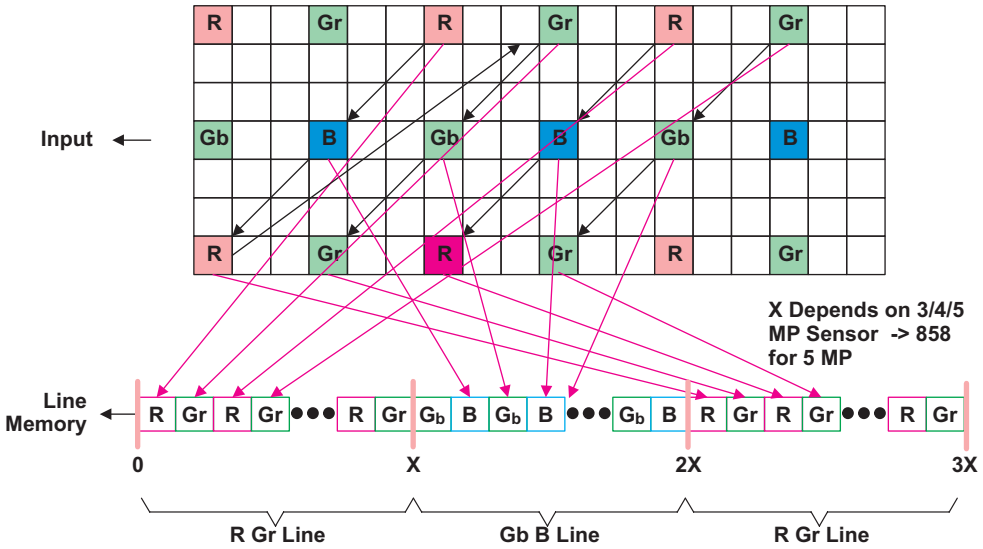


Figure 22. Example of Matsushita VGA CCD Configuration



- Input → 2, 859, 1716, 3, 860, 1717, ... and So On
- Output → 2, 3, 4, 5, ...and So On (Outputs 0, 1, 858 Are Not Read From Sensor)
- FMTEN = 1, FMTCBL = 0, LNUM = 2, FMTAINC = 0 (add/sub 1)
- NOTE: 858 In Input is Equal to 0 In 2nd Output Line and 2 X 858 In Input is 0 In 3rd Output Line

	Line #	Init Value
ADDR0	0	2
ADDR1	1	1
ADDR2	2	0
ADDR3	X	X
ADDR4	X	X
ADDR5	X	X
ADDR6	X	X
ADDR7	X	X

Address Pointers

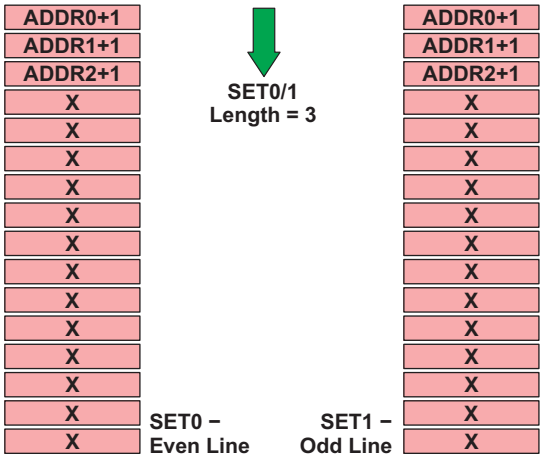
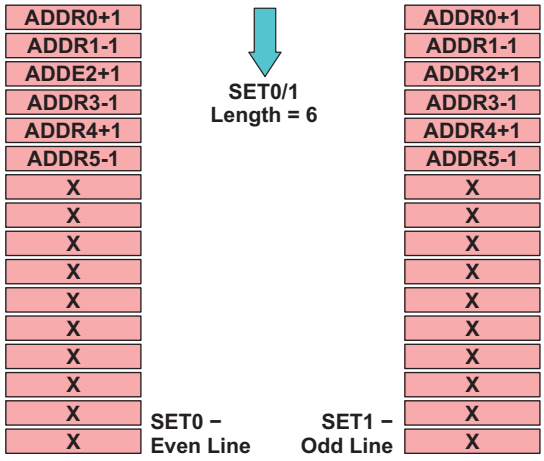


Figure 23. 12 Example of Matsushita VGA CCD Configuration with Two-tap AFE

- Input → 2, 2572, 859, 1714, 1716, 857, 3, 2571, 860, 1713, 1717, 856, ... and So On
- Output → 2, 3, 4, 5, ...and So On
- FMTEN = 1, FMTCBL = 0, LNUM = 2, FMTAINC = 0 (add/sub 1)
- NOTE: 858 In Input is Equal to 0 in 2nd Output Line and 2 x 858 in Input is 0 in 3rd Output Line.

	Line #	Init Value
ADDR0	0	2
ADDR1	2	855
ADDR2	1	1
ADDR3	1	856
ADDR4	2	0
ADDR5	0	857
ADDR6	X	X
ADDR7	X	X

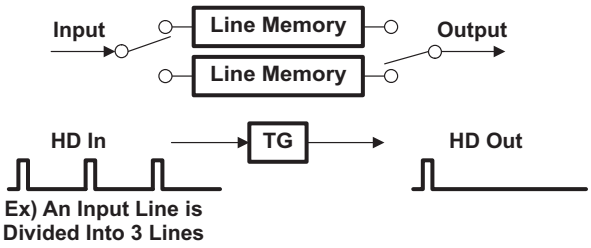
Address Pointers



4.1.4.2.3 Combine the Divided Input Lines

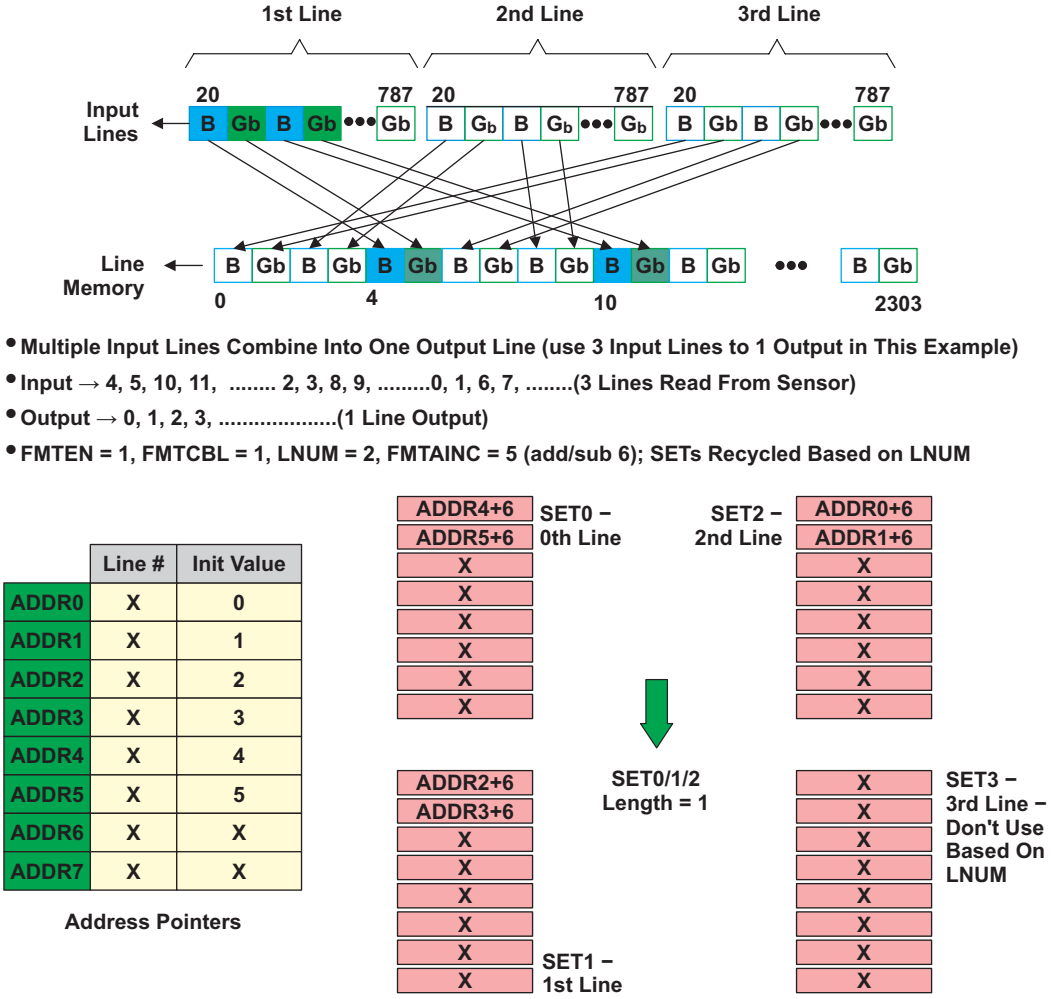
The formatter can gather the divided input lines and organize a single line. Figure 24 shows an example generating a single output line from three input lines, and masking the two out of three HD input pulses.

Figure 24. Combine Three Input Lines Into a Single Line



The following examples show the register setting.

Figure 25. Example of Combining Three Input Lines Into a Single Line



The detailed register settings for the example shown in Figure 25 and described in Table 24.

Table 24. Register Settings

Data Formatter Registers		
Name	**Value**	**Description**
FMTEN	1	Formatter enable
FMTCBL	1	Combine input lines
FMTAINC	5	Address increment = FMTAINC+1 = 6
FMTSPH	20	The first valid pixel of a divided line
FMTLNH	767	Valid length of a divided line = FMTLNH+1 = 768
FMTSLV	16	The first valid divided line
FMTLNV	4589	The number of the valid divided lines = FMTLNV+1 = 4590
FMTRLEN	2304	The length of an organized line = (FMTLNH+1) x (LNUM+1) = 2304
LNUM	2	Split/Combine line number = LNUM+1 = 3
FMTPLEN0	1	Number of PGM entries for SET0 = FMTPLEN0+1 = 2
FMTPLEN1	1	Number of PGM entries for SET1 = FMTPLEN1+1 = 2
FMTPLEN2	1	Number of PGM entries for SET2 = FMTPLEN2+1 = 2
FMTAPTR0	0	Address Pointer 0, INIT=0

Table 24. Register Settings (continued)

Data Formatter Registers		
Name	**Value**	**Description**
FMTAPTR1	1	Address Pointer 1, INIT=1
FMTAPTR2	2	Address Pointer 2, INIT=2
FMTAPTR3	3	Address Pointer 3, INIT=3
FMTAPTR4	4	Address Pointer 4, INIT=4
FMTAPTR5	5	Address Pointer 5, INIT=5
PGM0EN	1	Program 0 Valid flag
PGM1EN	1	Program 1 Valid flag
PGM8EN	1	Program 8 Valid flag
PGM9EN	1	Program 9 Valid flag
PGM16EN	1	Program 16 Valid flag
PGM17EN	1	Program 17 Valid flag
PGM0UPDT&APTR	4	Program 0 Address pointer = ADDR4+6
PGM1UPDT&APTR	5	Program 1 Address pointer = ADDR5+6
PGM8UPDT&APTR	2	Program 8 Address pointer = ADDR2+6
PGM9UPDT&APTR	3	Program 9 Address pointer = ADDR3+6
PGM16UPDT&APTR	0	Program 16 Address pointer = ADDR0+6
PGM17UPDT&APTR	1	Program 17 Address pointer = ADDR1+6
Registers Common to the ISIF		
SPH	0	The first pixel in an organized line to be stored to SDRAM
LNH	2303	Number of pixels in an organized line to be stored to SDRAM = LNH+1 = 2304 (e.g., LNH = FMTRLEN -1))
SLV	19	The line to start data storing to SDRAM. It's based on the divided line count. (e.g., SLV = FMTSLV + (LNUM+1) = 19))
LNV	1529	The number of the organized lines to be stored to SDRAM = LNV+1 = 1530 (e.g., LNV = (FMTLNV+1) + (ILC+1) -1 = 1529))

Figure 26. Example of SONY CCD Configuration

- **Multiple Input Lines Combine Into One Output Line (use 3 Input Lines to 1 Output in This Example)**
- **Input → 2, 5, 8, ... 1, 4, 7, ...0, 3, 6, ...(3 Lines Read From Sensor)**
- **Output → 0, 1, 2, 3, ...(1 Line Output)**
- **FMTEN = 1, FMTCBL = 1, LNUM = 2, FMTAINC = 2 (add/sub 3); SETs Recycled Based on LNUM**

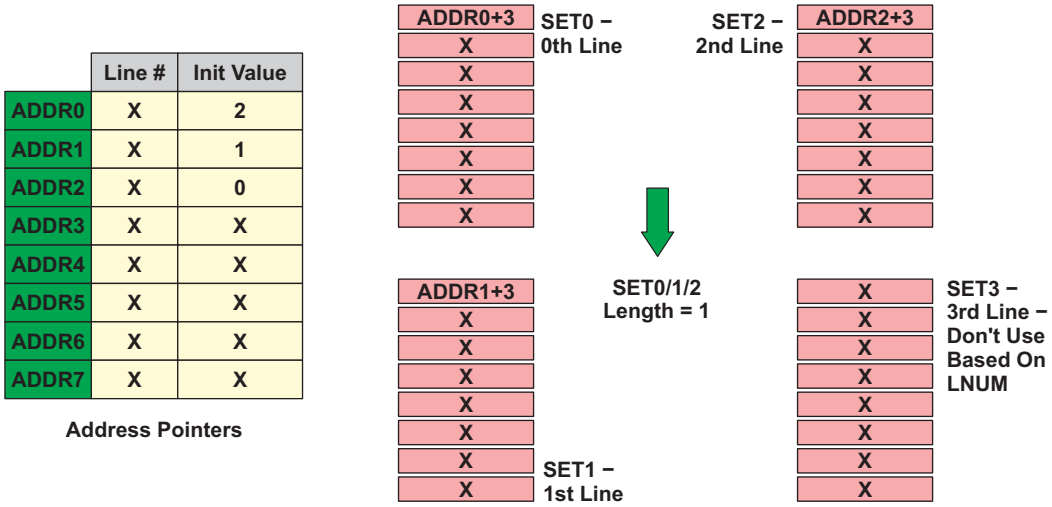
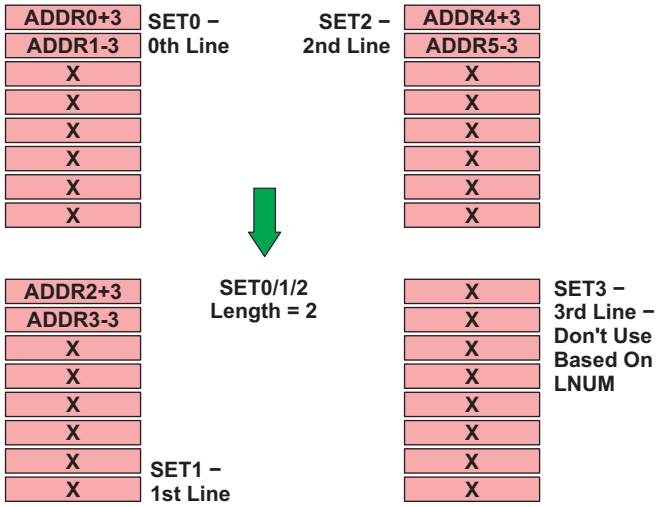


Figure 27. Example of SONY CCD Configuration with Two-tap AFE

- Multiple Input Lines Combine Into One Output Line (use 3 Input Lines to 1 Output in This Example)
- Input → 2, N, 5, N-3, ... 1, N-1, 4, N-4, ...0, N-2, 3, N-5, ...(3 Lines Read From Sensor)
- Output → 0, 1, 2, 3, ...(1 Line Output)
- FMTEN = 1, FMTCBL = 1, LNUM = 2, FMTAINC = 2 (add/sub 3); SETs Recycled Based on LNUM

	Line #	Init Value
ADDR0	X	2
ADDR1	X	N
ADDR2	X	1
ADDR3	X	N-1X
ADDR4	X	0
ADDR5	X	N-2
ADDR6	X	X
ADDR7	X	X

Address Pointers



4.1.4.3 Color Space Converter

The color space converter (CSC) includes four 8-bit x 12-bit multipliers and one adder for the color space conversion. These multiplier/adder units are used for the operation described in Figure 29. Data are taken from two input lines during the operation.

Figure 28. Color Space Converter Functional Block Diagram

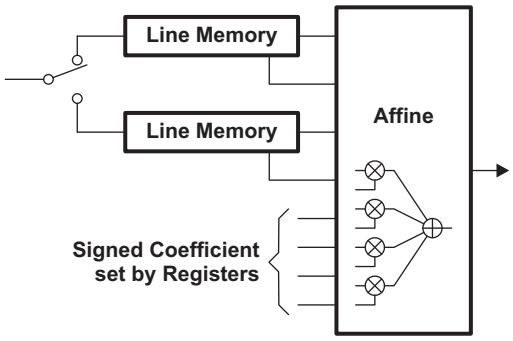
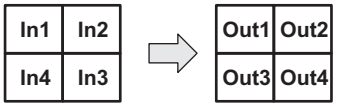


Figure 29. Color Space Converter Operation

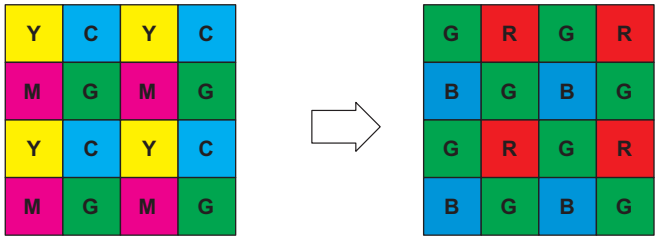


$$\begin{pmatrix} Out1 \\ Out2 \\ Out3 \\ Out4 \end{pmatrix} = \begin{pmatrix} M00 & M01 & M02 & M03 \\ M10 & M11 & M12 & M13 \\ M20 & M21 & M22 & M23 \\ M30 & M31 & M32 & M33 \end{pmatrix} \begin{pmatrix} In1 \\ In2 \\ In3 \\ In4 \end{pmatrix}$$

M00-M33 : Signed 8-Bits Data with 5-Bit Decimal
The Value Range –4 = < Mxx < 4

Coefficients are signed 8-bit (decimal is 5 bits). The CSC can convert CMYG filtered CCD data to Bayer Matrix (RGBG) data as shown in Figure 30.

Figure 30. CSC CMYG Filtered CCD Data to RGBG Data Converter Operation



$$\begin{pmatrix} G \\ R \\ B \\ G \end{pmatrix} = \begin{pmatrix} 0.5 & 0.5 & -0.5 & 0 \\ 0.5 & -0.5 & 0.5 & 0 \\ -0.5 & 0.5 & 0.5 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} Y \\ C \\ M \\ G \end{pmatrix}$$

The following figures explain which input pixels are used for the operation. There is a 1-line latency between the input and the output.

Figure 31. CSC - Input Pixels Used

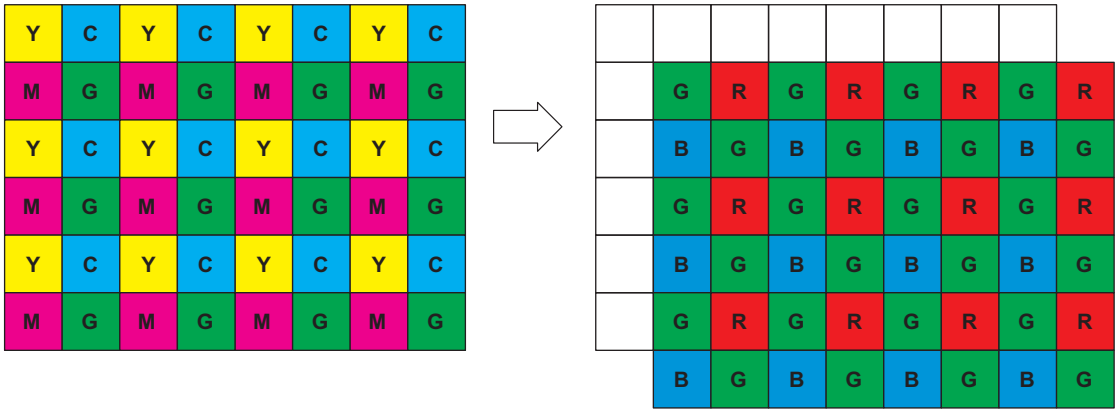


Figure 32. CSC - 1st Pixel / 1st Line Generation

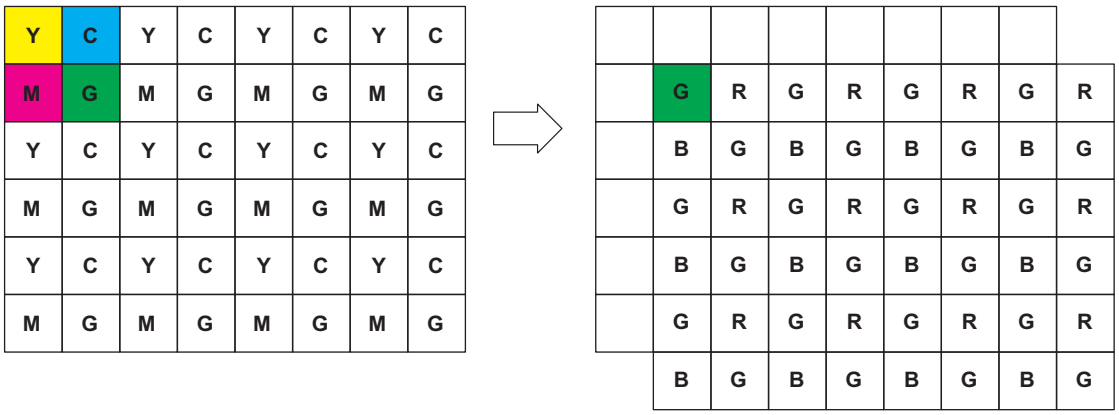


Figure 33. CSC - 2nd Pixel / 1st Line Generation

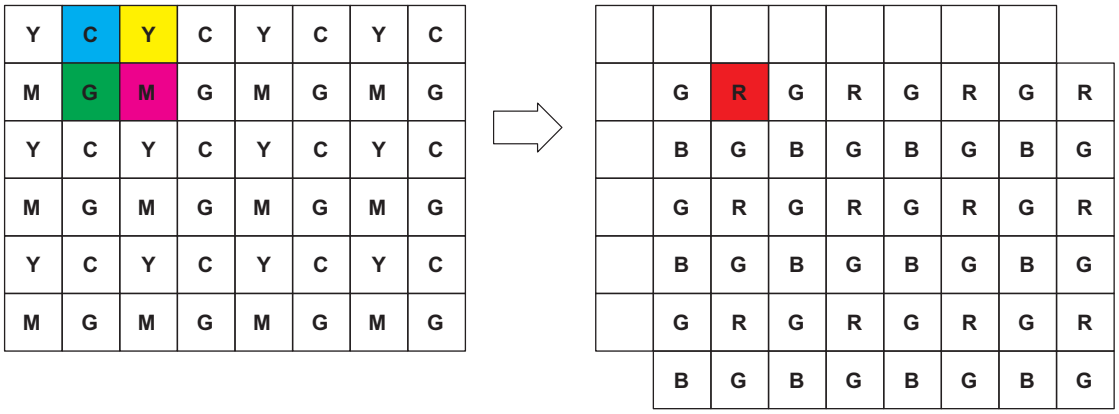


Figure 34. CSC - 2nd Last Pixel / 1st Line Generation

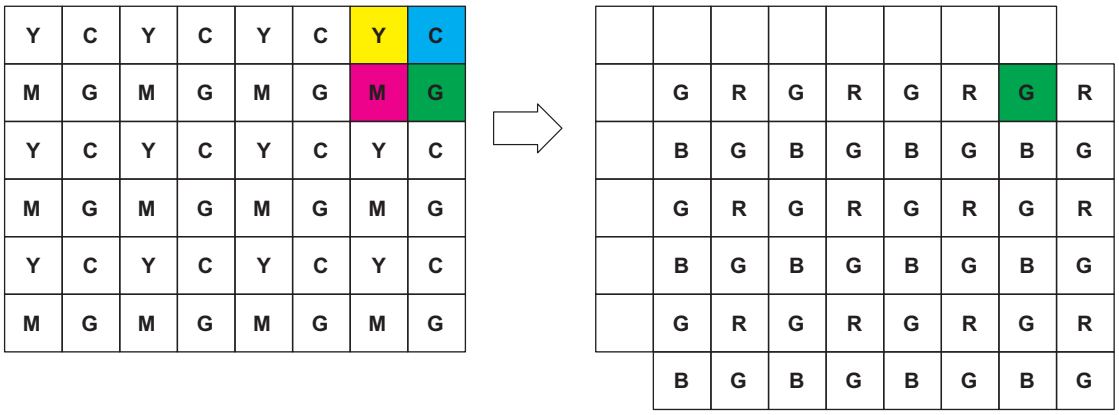
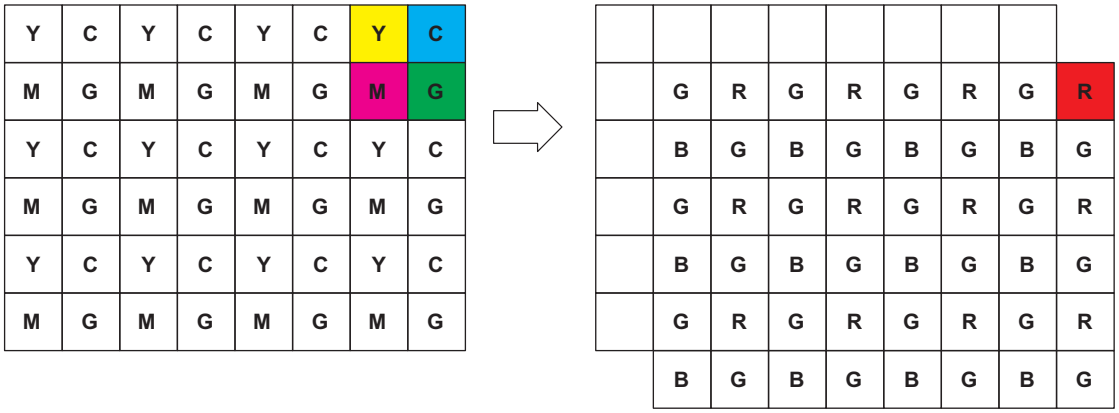


Figure 35. CSC - Last Pixel / 1st Line Generation



As shown in Figure 34 and Figure 35, the operation for the last pixel and the second last pixel uses the same input data. Also, the operation for the last line and the second last line uses the same input data.

Figure 36. CSC - 1st Pixel / Last Line Generation

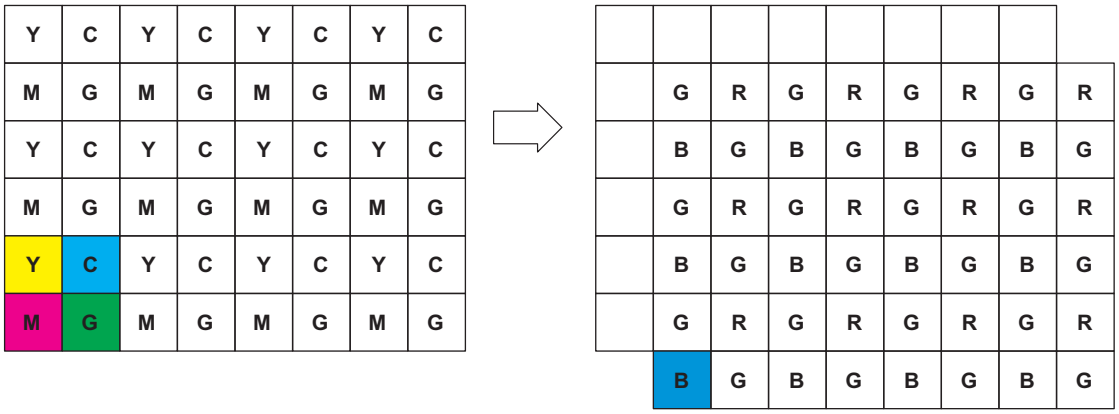


Figure 37. 2nd Pixel / Last Line Generation

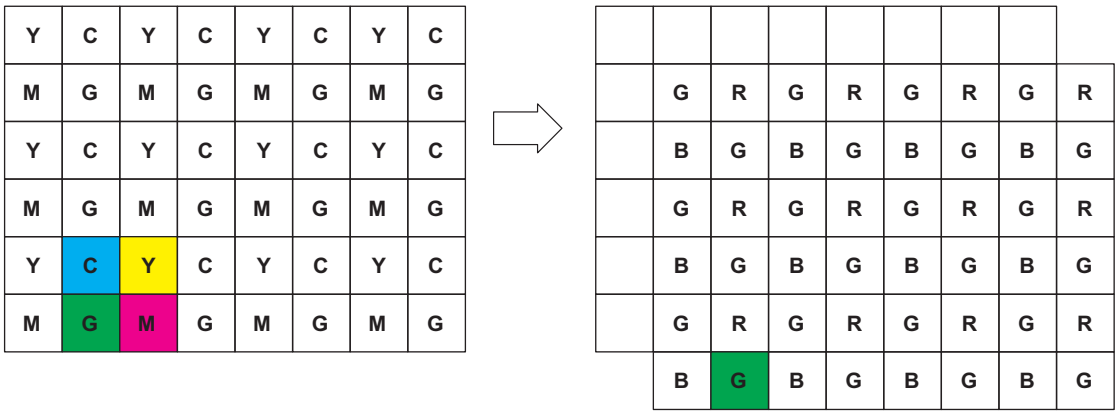


Figure 38. 2nd Last Pixel / Last Line Generation

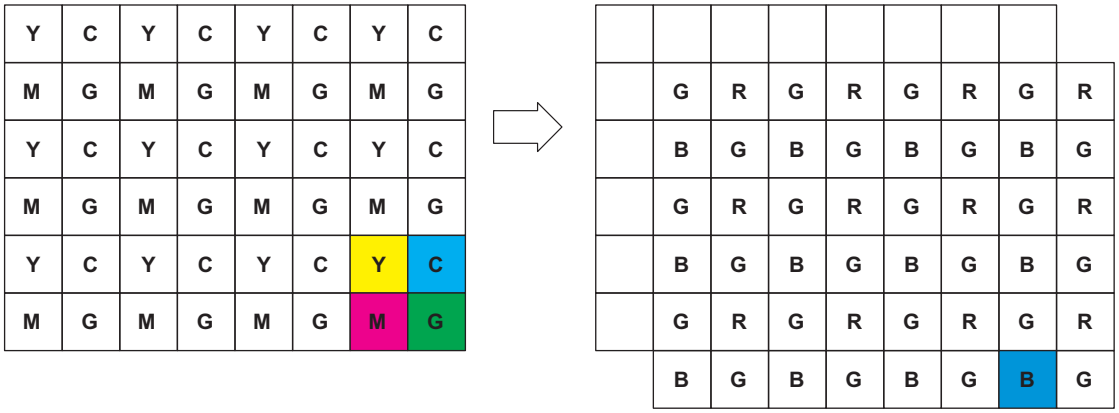
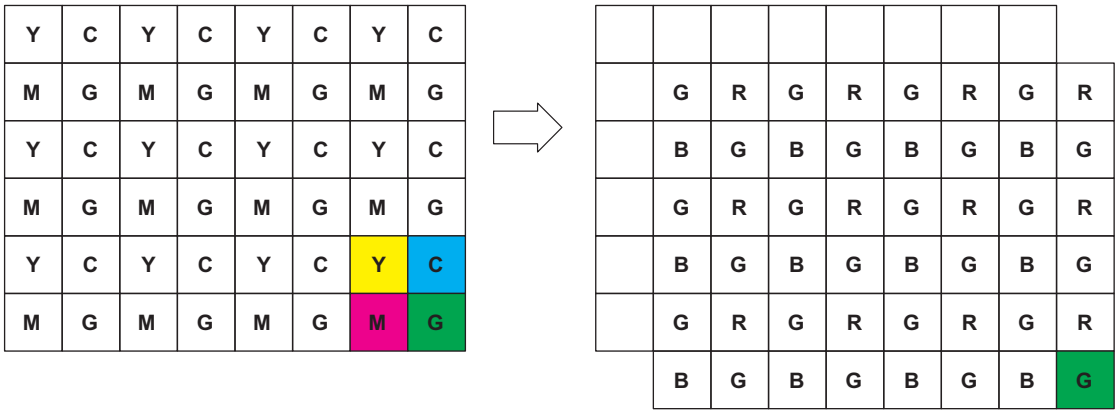


Figure 39. Last Pixel / Last Line Generation

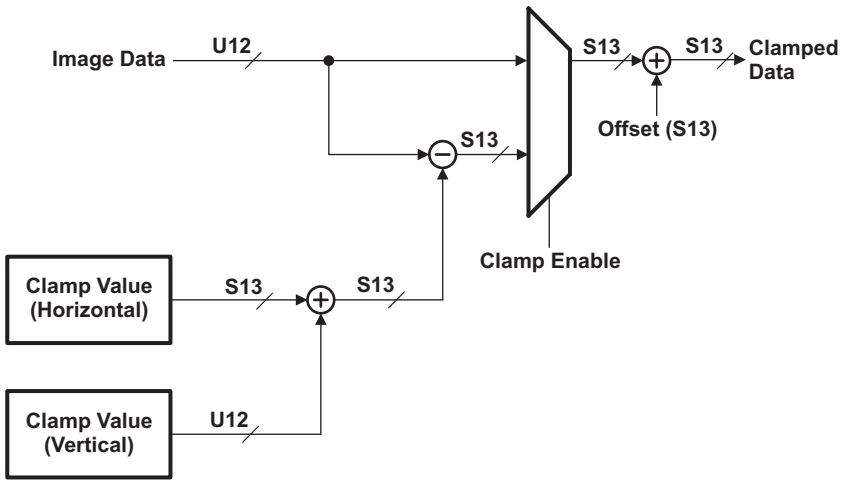


In addition to the registers specific to the color space converter, some of the registers are shared with the input data formatter to configure the valid area, which are FMTSPH, FMTLNH, FMTSLV, and FMTLNV shown in Figure 16. There should be at least one invalid pixel at the end of the line, and also one invalid line at the end of the frame.

4.1.4.4 Black Clamp

The next sub-module is the black clamp block. Clamp value is calculated based on the pixel value at the optical black (OB) region. Clamp value is calculated separately for horizontal and vertical directions to compensate for the offset drift in both horizontal and vertical directions. The sum of the horizontal and vertical clamp values is subtracted from the image data, and then the additional DC offset (S13) is added as shown in Figure 40.

Figure 40. Digital Clamp Block Diagram



Clamp value can be calculated regardless of the color (CLMD=0), or can be calculated separately for each four color (CLMD=1).

4.1.4.4.1 Value for Horizontal Direction

Clamp value for horizontal direction is calculated using the pixel values at the upper OB region. The maximum pixel value to be used for the clamp value calculation can be limited to 1023 if CLHLMT is set.

If CLHLMT = 1

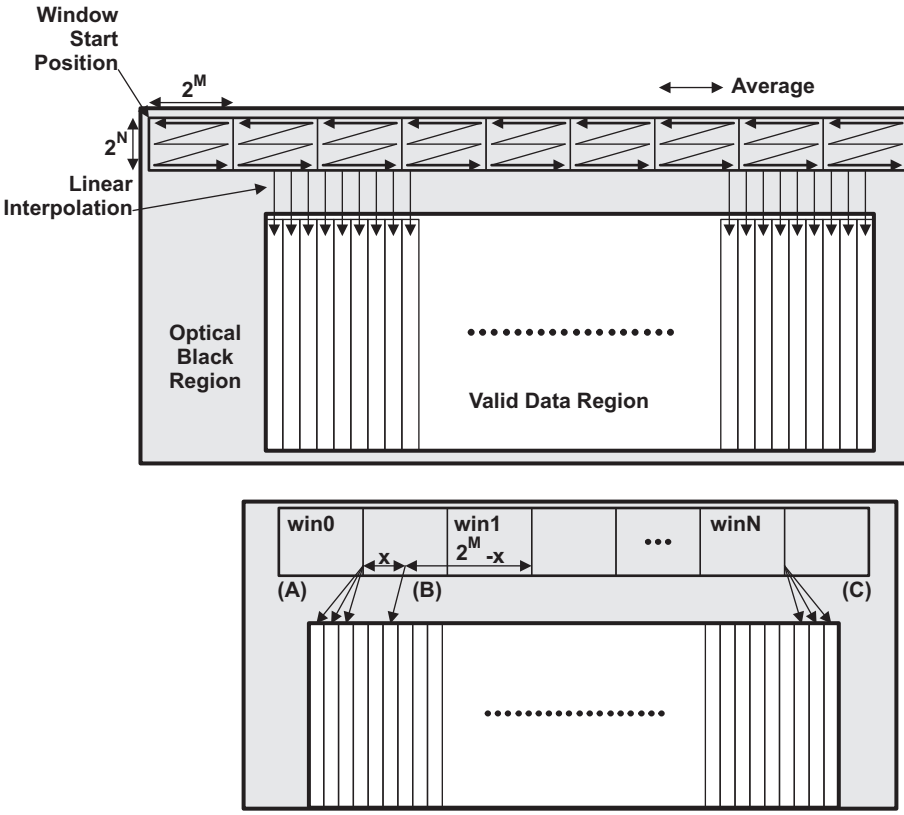
- CLMD=0: The pixel value greater than 1023 will be replaced by the last pixel value which was equal to or less than 1023
- CLMD=1: The pixel value greater than 1023 will be replaced by the last pixel value of the same color which was equal to or less than 1023

Clamp value calculation for horizontal direction could be disabled in case there is no upper OB. The operating modes are:

- Horizontal clamp value calculation is enabled. The calculated horizontal clamp value is subtracted from the Image data along with the Vertical clamp value. (CLHMD=1)
- Horizontal clamp value is not updated. The horizontal clamp value used for the previous image is subtracted from the image data along with the vertical clamp value. (CLHMD=2)
- Horizontal clamp value is not updated. Only the vertical clamp value is subtracted from the image data. (CLHMD=0)

Up to 32 windows can be set in a row for clamp value calculation. Windows are the same size in a format 2^Mx2^N (where ^ denotes an exponent).

Figure 41. Clamp Value for Horizontal Direction



The clamp value calculation involves these steps:

1. Calculate the average of the pixel value in each window.
2. Set the average of the leftmost window or the rightmost window as the base value.
3. Subtract the base value from the average of each window. Use this value as a clamp value for each window.
4. Acquire the horizontal distance from the valid pixel to be processed to the center of the closest two windows.
5. Calculate the clamp value of the valid pixel by linear interpolation, using the clamp value of the closest two windows.
6. If the valid pixel is on the left of the center of the leftmost window, the clamp value of the leftmost window is applied. If the valid pixel is on the right of the center of the rightmost window, the clamp value of the rightmost window is applied.

4.1.4.4.2 Clamp Value for Vertical Direction

Clamp value for vertical direction is calculated using the pixel values at the left or right OB region. Line average is calculated for the OB H valid (2^L) period (where ^ denotes an exponent). The averages for the previous lines are also added back so as to reduce the difference between the lines.

Figure 42. Clamp Value for Vertical Direction (1)

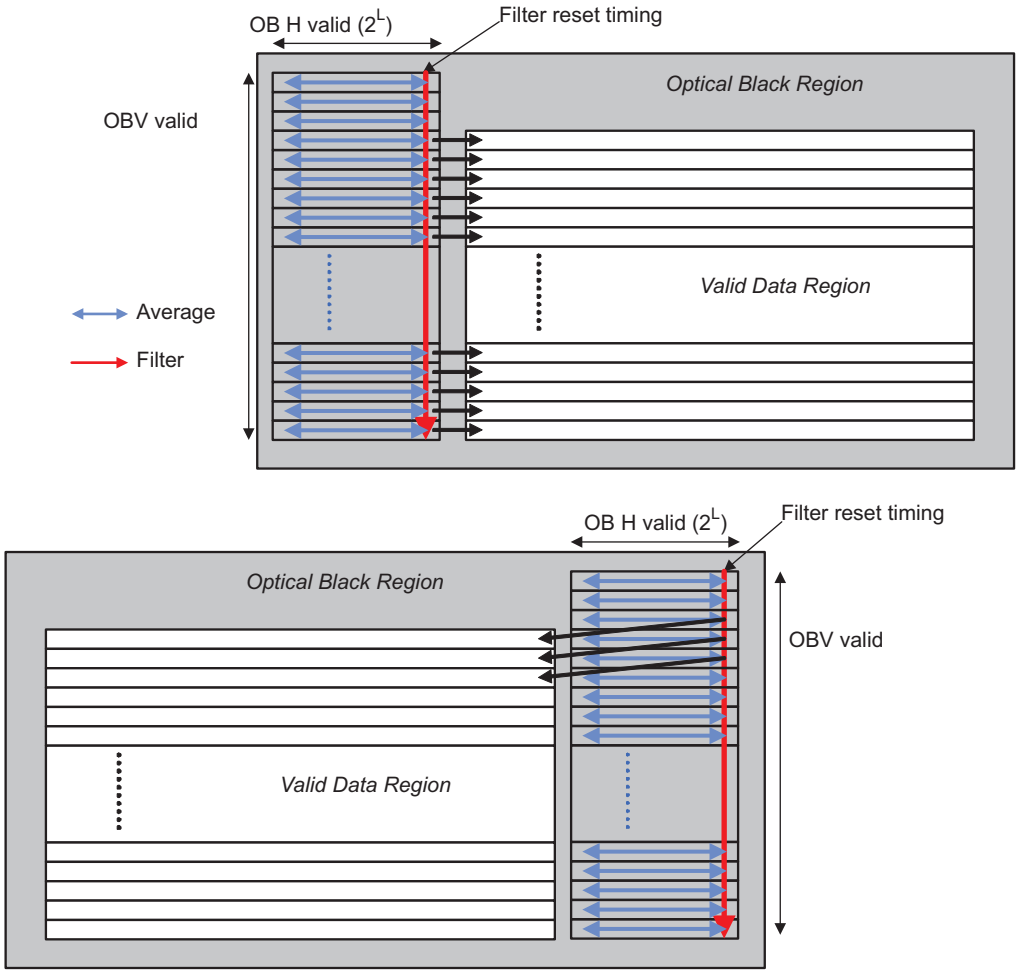
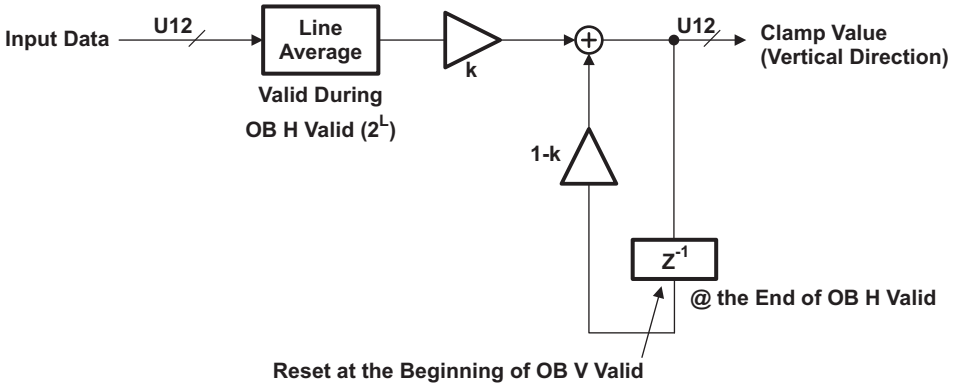


Figure 43. Clamp Value for Vertical Direction (2)



$$ClampValue(Vn) = LineAverage(Vn) \cdot k + ClamValue(Vn-1) \cdot (1-k)$$

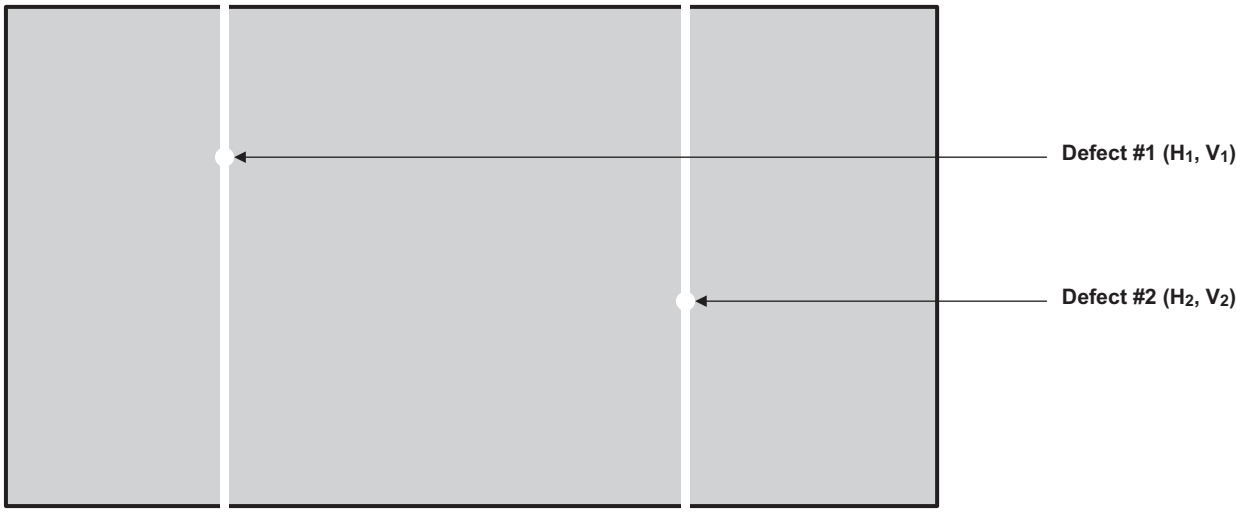
The register that holds the clamp value for the previous line is reset at the beginning of the OB V valid. The reset value can be selected from:

- Value set via the configuration register. (CLVRVSL=1)
- The base value calculated for Horizontal direction. (CLVRVSL=0)
- No update (same as the previous image). (CLVRVSL=2)

4.1.4.5 Vertical Line Defect Correction

The vertical line defect correction block can correct up to eight vertical line defects.

Figure 44. Vertical Line Defects



Vertical line defects are corrected by subtracting the defect level (method 1), or replaced by the average of pixel (i-2) and pixel (i+2) (method 2).

For method 1, the defect level is defined for the point of the defect, for the pixels upper than the defect, and for the pixels lower than the defect. If the data to be corrected are saturating, they are linear interpolated (replaced by the average of pixel (i-2) and pixel (i+2)) instead, or just fed through.
data_corrected(H1, V1) = data(H1, V1) – SUBH1V1
data_corrected(H1, V1upper) = data(H1, V1upper) – SUBH1V1upper (V1upper < V1)
data_corrected(H1, V1lower) = data(H1, V1lower) – SUBH1V1lower (V1lower > V1)

The coordinates of the defects and the defect level should be set to the table prior to the processing. Defect correction of the pixels upper than the defect can be disabled by the bit field DFCCTL.VDFCUDA. Other features include:

- Set the coordinates of the defects and the value to be subtracted from the data to the table (8x50) as shown in Table 25, prior to the processing. Up to eight defects can be set
- The coordinates are 13-bit width for horizontal and vertical direction, so image size up to 8,192 x 8,192 is supported.
- Defect level (value to be subtracted from the data) is 8-bit width, but can be up-shifted up to 4 bits by VDFLSFT.
- The defect must be set from left to right as shown in Figure 45.
- Defect correction of the pixels upper than the defect can be disabled by bye bit field DFCCTL.VDFCUDA.

Figure 45. The Order of the Vertical Line Defects

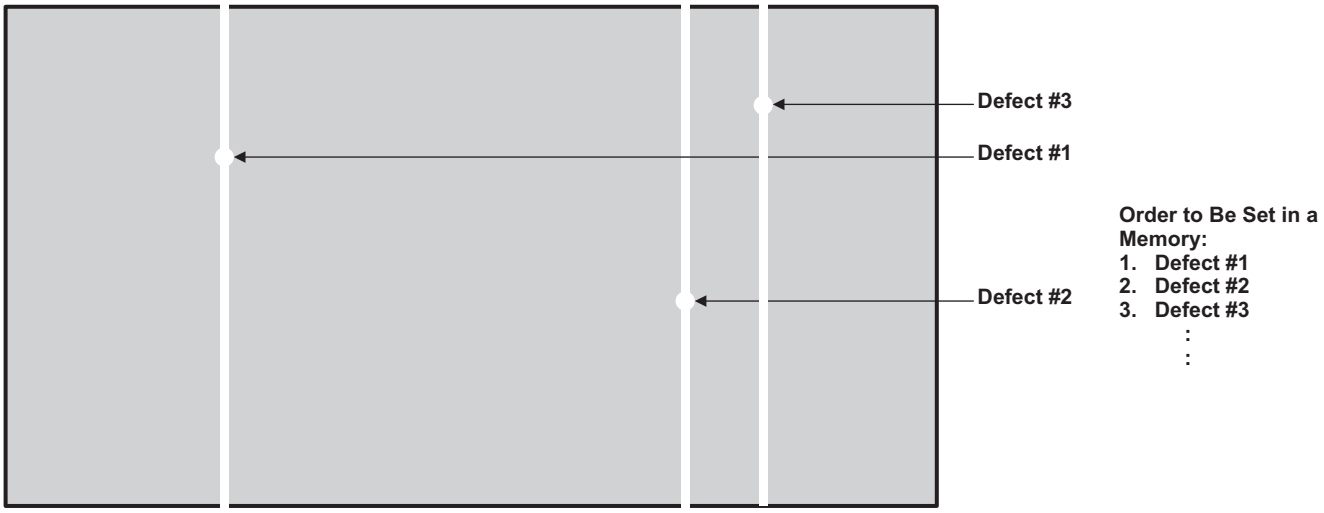


Table 25. Vertical Line Defect Information Table

Bit	Defect Information
12:0	Vertical position of the defects
25:13	Horizontal position of the defects
33:26	Defect level of the Vertical line defect position (V = Vdefect)
41:34	Defect level of the pixels upper than the Vertical line defect (V < Vdefect)
49:42	Defect level of the pixels lower than the Vertical line defect (V > Vdefect)

The correction method is common to all the defects, and can be selected from the following three by VDFCSL.

- Defect level subtraction. Just fed through if data are saturating
- Defect level subtraction. Horizontal interpolation ((i-2)+(i+2))/2 if data are saturating
- Horizontal interpolation ((i-2)+(i+2))/2

4.1.4.5.1 Vertical Line Defect Table Update Procedure

The following steps includes the update procedure for the vertical line defect table.

1. Make sure that VDFCEN is disabled
2. Write the V coordinate of the first defect to DFCMEM0, and the H coordinate to DFCMEM1. Also set the defect level to DFCMEM2 - DFCMEM4 if the correction method is 0 or 1
3. Set ‘1’ to DFCMWR with DFCMARST set
4. Wait until DFCMWR gets cleared, and write the next data to DFCMEM0 - DFCMEM4
5. Set ‘1’ to DFCMWR with DFCMARST cleared
6. Repeat 4~5 until all entries are written to the Vertical line Defect table.
7. In case the defect entry is less than 8, an extra write cycle is required to fill the next table location with a certain value. Clear DFCMEM0 to all '0', set DFCMEM1 to all '1', and set ‘1’ to DFCMWR with DFCMARST cleared
8. Enable Vertical line Defect Correction by setting VDFCEN

4.1.4.6 2D Lens Shading Correction

Some optics show significant lens shading, the phenomenon that the image is bright in the center and decreases in brightness towards the edge of the field. The 2D LSC module is used to compensate for this effect. It can be enabled by setting the 2DLSCCFG.ENABLE register bit.

The 2D LSC multiplies each pixel by a gain mask that is stored down-sampled in SDRAM memory. This gain mask can be dependent in aperture, exposure time, and other photographic settings, on lens shading characteristics to correct the dim corner effect, and can also be dependent on the image contents to implement adaptive lighting adjustment. The gain mask can be visualized as a 3-D contour map, where the magnitude of each point in the 2-D map is stored as in a 2-D array, controlling how much to scale the pixels in an image.

To minimize memory bandwidth consumption and processing time, the gain mask is stored as a down-sampled array. The gain map down-sampling factors supported are MxN, where M represents the horizontal sampling factor and N represents the vertical sampling factor. M and N can be independently chosen among the following scaling values with the requirement that N ≤ M: 8, 16, 32, 64, and 128. The gain map can be stored in the following supported formats: U8Q8, U8Q7, U8Q6, and U8Q5, with an optional base (DC offset) of 1.0 to shift the range up. The offset map is stored in S8Q0 format with optional shift up. Separate horizontal and vertical sampling factors allow the lens shading correction to work with the normal 1:1 aspect ratio image pixels, as well as “tall-and-skinny” pixels typical in CCD sensor's preview mode image data.

Due to limited local buffer memory, the maximum line width that the 2D LSC can support is limited as a function of the horizontal sampling factor (M). The table below indicates these maximum widths for each M value.

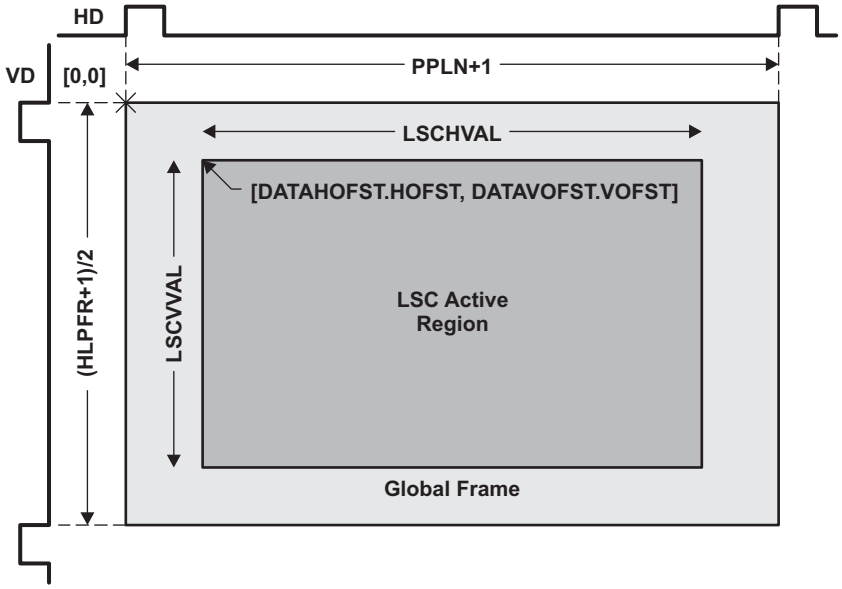
Table 26. Maximum Supported Line Widths

M	Maximum Line Width
8	1016
16	2032
32	4064
64	8128
128	16256

4.1.4.7 Image Framing with Respect to Gain Map Samples

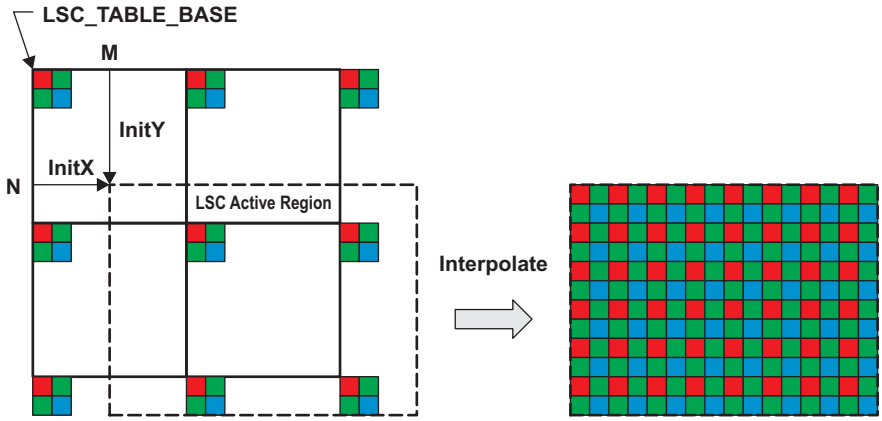
The gain map is internally up-sampled to full resolution before being applied to the image. In order to account for all the possible cropping schemes and zoom ratios, the 2D LSC can be configured such that a single gain map can be stored in memory that maps to sensor lens. The LSC active region is defined by the combination of DATAHOFST, DATAVOFST, LSCHVAL and LSCVVAL registers.

Figure 46. LSC Active Region for ISIF Input Frame



The starting point of the pre-configured lens shading map can be easily modified in software to align with the ISIF input image frame. The location of the gain mask data in memory is specified by the mask SDRAM input addresses (2DLSCGRBU, 2DLSCGRBL) and line offset (2DLSCGROF) registers. The input address must be aligned to a four byte boundary, and the line offset must be aligned on a 32-bit boundary. In the full resolution case, the address will be set to the beginning of the map. When the LSC active region is defined over a cropped region of the full image, the SDRAM input address can be set to the upper-left corner of the grid closest to the beginning of the active region, and the 2DLSCINI.INITX and 2DLSCINI.INITY registers will mark the offset into the up-sampled gain map where the active region begins. Figure 47 shows the LSC active region with respect to the gain map grid. Note that (InitX, InitY) deals with the pixel phase inside a gain map grid, so InitX and InitY must each be less than M and N respectively.

Figure 47. CFA Gain Mask Upsampling via Bilinear Interpolation



4.1.4.8 CFA Gain Mask Upsampling

Before applying the mask, the mask is internally upsampled and interpolated back to full resolution via bilinear interpolation.

Note that the CFA gain mask function is neutral to color pattern. The starting color of the gain mask should be consistent with the starting color of the image, and can be any color. In order to align starting colors, the LSC2D_INI.INITX and LSC2D_INI.INITY registers must be even. The 2D LSC engine upsamples each phase of the mask data as a separate plane and applies the upsampled mask to the image with the same color phasing. In other words, the red gains are interpolated with red gains, and applied to the red input pixels. The same is done for each of the other three colors in the color pattern. The LSC module is designed to work with Bayer CFA data, having the R/Gr/Gb/B color pattern. For the purpose of functional description, we assume Red is the starting color, but any other starting color or other 2x2 pattern can be used by placing color gains in the appropriate order.

Upsampling of the pixel-by-pixel gains is performed by locating the four same-color anchors for each destination gain value and applying bilinear interpolation.

Gain for a red pixel at destination coordinate (x, y) is computer as:

$$R(x, y) = \frac{R00 \times (M-k)(N-1) + R01 \times k \times (N-1) + R10 \times (M-k) \times 1 + R11 \times k \times I}{MN}$$

Where:

$k = (x + InitX) \bmod M$ $\quad Roo = R(i, j)$

$I = (y + InitY) \bmod N$ $\quad R01 = R(i + M, j)$

$i = floor\left(\frac{(x + InitX)}{M}\right) * M$ $\quad R10 = R(i, j + N)$

$j = floor\left(\frac{(y + InitY)}{N}\right) * N$ $\quad R11 = R(i + M, j + N)$

Similarly for the other colors we have:

$$GR(x, y) = \frac{GR00 \times (M-k)(N-1) + GR01 \times k \times (N-1) + GR10 \times (M-k) \times 1 + GR11 \times k \times I}{MN}$$

$$GB(x, y) = \frac{GB00 \times (M-k)(N-1) + GB01 \times k \times (N-1) + GB10 \times (M-k) \times 1 + GB11 \times k \times I}{MN}$$

$$B(x, y) = \frac{B00 \times (M-k)(N-1) + B01 \times k \times (N-1) + B10 \times (M-k) \times 1 + B11 \times k \times I}{MN}$$

However, the relation of (k, l) and (i, j) to(x, y) for other colors is different with the relation for red. For GR, we have (changes are bolded):

k=(x-1+InitX) mod M $\quad$ **GR**00=**GR**(i, j)

l=(y+InitY) mod N $\quad$ **GR**01=**GR**(i+M, j)

$i = floor\left(\frac{(x - 1 + InitX)}{M}\right) * M + 1$ $\quad$ **GR**10 = **GR**(i, j + N)

$j = floor\left(\frac{(y + InitY)}{N}\right) * N$ $\quad$ **GR**11 = **GR**(j + M, j + N)

For example, for M=N=8, GR(5, 2) is (4,2) from the upper-left anchor GR(1, 0), and is to be interpolated among GR(1, 0), GR(9,0), GR(1,8), GR(9,8) by

$$GR(5,2) = \frac{\begin{pmatrix} GR(1,0)*(8-4)*(8-2) \\ + GR(9,0)*4*(8-2) \\ + GR(1,8)*(8-4)*2 \\ + GR(9,8)*4*2 \end{pmatrix} + 32}{64}$$

Note: The +32 in the example above is used to force rounding while using integer math. Each of the interpolation equations above also are similarly rounded to the nearest integer, even though the +MN/2 is not explicitly included in the equation.

4.1.4.9 CFA Multiplication

The gain value interpolated for each pixel is multiplied with a corresponding input pixel. The product is rounded to the nearest integer, and then clipped or saturated to the valid range of 14 bits.

4.1.4.10 CFA Gain Mask Format

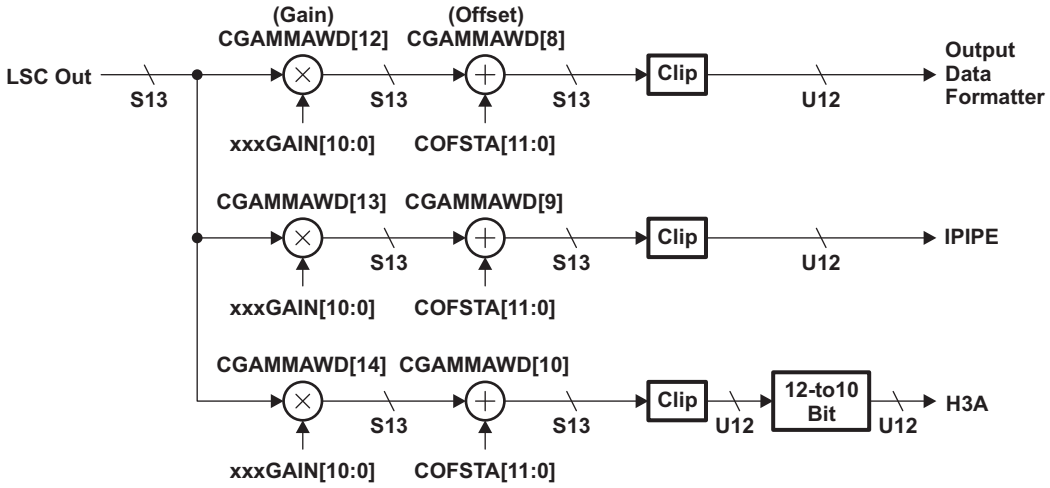
The four input down-sampled color gains for each MxN block should be packed into 32-bit words in SDRAM as indicated in Figure 48.

4.1.4.11 Gain and Offset

There are color-dependent gain controls for SDRAM, IPIPE, and H3A paths. Gain applied to each data is selected according to the pixel position and the color pattern settings (CCOLP). Gain factors are U12Q9 which ranges from 0 to 7+511/512, and common for all the paths. Gain control can be enabled or disabled individually for each path.

After the gain control, a single offset value can be added to each path individually. The offset value is U12 which ranges from 0 to 4,095. Data (S13) are then truncated to U12.

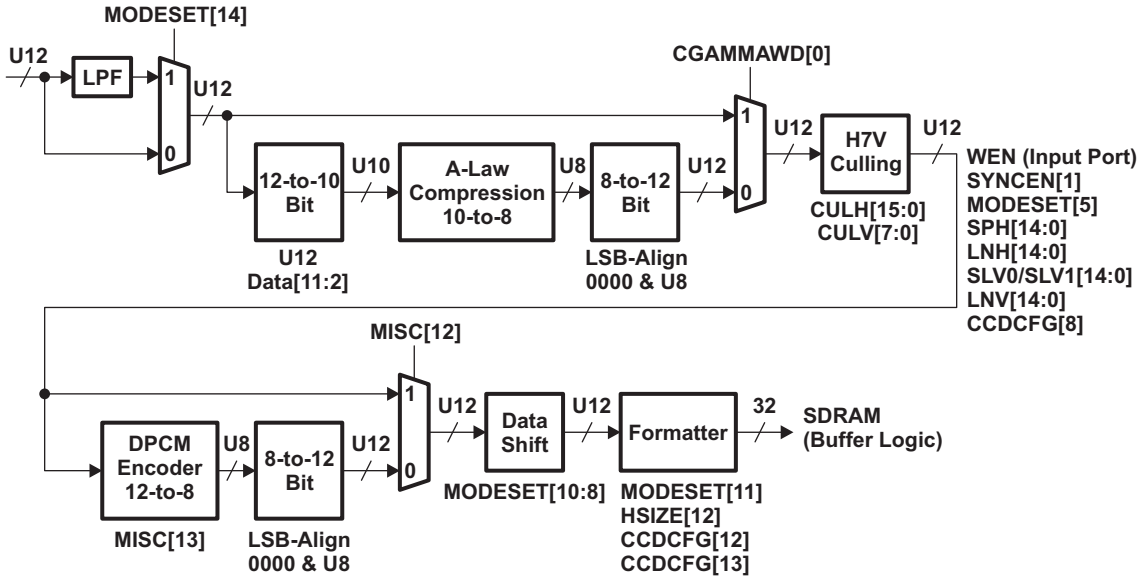
Figure 48. Gain and Offset



4.1.4.12 Output Formatter for SDRAM

The final stage of the RAW Data processing is the Output Formatter for DDR/SDRAM, which is shown in Figure 49.

Figure 49. Output Formatter Block Diagram



4.1.4.13 Low-Pass Filter

The output formatter block provides an option for applying an anti-aliasing filter for horizontal culling. The low-pass filter consists of a simple three-tap filter.

4.1.4.14 A-Law Compression

There is an optional 10-bit to 8-bit A-Law compression block, where the upper 10-bits of 12-bits data are compressed to 8 bits using a fixed A-Law table to reduce the required bandwidth in transmission between the ISIF and the SDRAM. The A-law table has a same characteristic as Voice codec, and is shown in Table 27 and Table 28.

Note that IPIPEIF has an inverse A-Law table option so it can reverse this non-linear operation if the saved data is to be read back in for further processing.

Table 27. A-Law Table (1)

Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law
0	0	64	64	128	112	192	140	256	161	320	176	384	189	448	200
1	1	65	65	129	113	193	141	257	161	321	176	385	189	449	200
2	2	66	66	130	113	194	141	258	161	322	177	386	189	450	200
3	3	67	67	131	114	195	142	259	161	323	177	387	189	4531	200
4	4	68	68	132	114	196	142	260	162	324	177	388	190	452	200
5	5	69	69	133	115	197	142	261	162	325	177	389	190	453	200
6	6	70	70	134	115	198	143	262	162	326	177	390	190	454	201
7	7	71	71	135	116	199	143	263	162	327	178	391	190	455	201
8	8	72	72	136	116	200	143	264	163	328	178	392	190	456	201
9	9	73	73	137	117	201	144	265	163	329	178	393	190	457	201
10	10	74	74	138	117	202	144	266	163	330	178	394	191	458	201
11	11	75	75	139	118	203	144	267	163	331	178	395	191	459	201
12	12	76	76	140	118	204	145	268	164	332	179	396	191	460	201
13	13	77	77	141	119	205	145	269	164	333	179	397	191	461	202
14	14	78	78	142	119	206	145	270	164	334	179	398	191	462	202
15	15	79	78	143	120	207	146	271	164	335	179	399	191	463	202
16	16	80	79	144	120	208	146	272	165	336	179	400	192	464	202
17	17	81	80	145	121	209	146	273	165	337	180	401	192	465	202
18	18	82	81	146	121	210	147	274	165	338	180	402	192	466	202
19	19	83	82	147	122	211	147	275	166	339	180	403	192	467	202
20	20	84	83	148	122	212	147	276	166	340	180	404	192	468	203
21	21	85	84	149	123	213	148	277	166	341	181	405	193	469	203
22	22	86	84	150	123	214	148	278	166	342	181	406	193	470	203
23	23	87	85	151	124	215	148	279	167	343	181	407	193	471	203
24	24	88	86	152	124	216	149	280	167	344	181	408	193	472	203
25	25	89	87	153	125	217	149	281	167	345	181	409	193	473	203
26	26	90	88	154	125	218	149	282	167	346	182	410	193	474	204
27	27	91	88	155	125	219	150	283	168	347	182	411	194	475	204
28	28	92	89	156	126	220	150	284	168	348	182	412	194	476	204
29	29	93	90	157	126	221	150	285	168	349	182	413	194	477	204
30	30	94	91	158	127	222	151	286	168	350	182	414	194	478	204
31	31	95	91	159	127	223	151	287	168	351	183	415	194	479	204
32	32	96	92	160	128	224	151	288	169	352	183	416	194	480	204
33	33	97	93	161	128	225	152	289	169	353	183	417	195	481	205
34	34	98	93	162	129	226	152	290	169	354	183	418	195	482	205
35	35	99	94	163	129	227	152	291	169	355	183	419	195	483	205
36	36	100	95	164	129	228	152	292	170	356	184	420	195	484	205
37	37	101	96	165	130	229	153	293	170	357	184	421	195	485	205
38	38	102	96	166	130	230	153	294	170	358	184	422	195	486	205

Table 27. A-Law Table (1) (continued)

Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law
39	39	103	97	167	131	231	153	295	170	359	184	423	196	487	205
40	40	104	98	168	131	232	154	296	171	360	184	424	196	488	206
41	41	105	98	169	132	233	154	297	171	361	185	425	196	489	206
42	42	106	99	170	132	234	154	298	171	362	185	426	196	490	206
43	43	107	100	171	132	235	155	299	171	363	185	427	196	491	206
44	44	108	100	172	133	236	155	300	172	364	185	428	196	492	206
45	45	109	101	173	133	237	155	301	172	365	185	429	197	493	206
46	46	110	102	174	134	238	155	302	172	366	185	430	197	494	206
47	47	111	102	175	134	239	156	303	172	367	186	431	197	495	207
48	48	112	103	176	134	240	156	304	173	368	186	432	197	496	207
49	49	113	103	177	135	241	156	305	173	369	186	433	197	497	207
50	50	114	104	178.	135	242	157	306	173	370	186	434	197	498	207
51	51	115	105	179	136	243	157	307	173	371	186	435	198	499	207
52	52	116	105	180	136	244	157	308	173	372	187	436	198	500	207
53	53	117	106	181	136	245	157	309	174	373	187	437	198	501	207
54	54	118	106	182	137	246	158	310	174	374	187	438	198	502	208
55	55	119	107	183	137	247	158	311	174	375	187	439	198	503	208
56	56	120	108	184	137	248	158	312	174	376	187	440	198	504	208
57	57	121	108	185	138	249	159	313	175	377	188	441	198	505	208
58	58	122	109	186	138	250	159	314	175	378	188	442	199	506	208
59	59	123	109	187	139	251	159	315	175	379	188	443	199	507	208
60	60	124	110	188	139	252	159	316	175	380	188	444	199	508	208
61	61	125	110	189	139	253	160	317	175	381	188	445	199	509	208
62	62	126	111	190	140	254	160	318	176	382	188	446	199	510	209
63	63	127	112	191	140	255	160	319	176	383	189	447	199	511	209

Table 28. A-Law Table (2)

Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law
512	209	576	217	640	224	704	231	768	237	832	243	896	248	960	253
513	209	577	217	641	225	705	231	769	237	833	243	897	248	961	253
514	209	578	217	642	225	706	231	770	237	834	243	898	248	962	253
515	209	579	217	643	225	707	231	771	237	835	243	899	248	963	253
516	209	580	218	644	225	708	232	772	238	836	243	900	248	964	253
517	210	581	218	645	225	709	232	773	238	837	243	901	248	965	253
518	210	582	218	646	225	710	232	774	238	838	243	902	248	966	253
519	210	583	218	647	225	711	232	775	238	839	243	903	249	967	253
520	210	584	218	648	225	712	232	776	238	840	243	904	249	968	253
521	210	585	218	649	225	713	232	777	238	841	244	905	249	969	253
522	210	586	218	650	226	714	232	778	238	842	244	906	249	970	254
523	210	587	218	651	226	715	232	779	238	843	244	907	249	971	254
524	211	588	219	652	226	716	232	780	238	844	244	908	249	972	254
525	211	589	219	653	226	717	232	781	238	845	244	909	249	973	254
526	211	590	219	654	226	718	233	782	238	846	244	910	249	974	254
527	211	591	219	655	226	719	233	783	239	847	244	911	249	975	254
528	211	592	219	656	226	720	233	784	239	848	244	912	249	976	254
529	211	593	219	657	226	721	233	785	239	849	244	913	249	977	254
530	211	594	219	658	226	722	233	786	239	850	244	914	249	97.8	254
531	211	595	219	659	227	723	233	787	239	851	244	915	249	979	254
532	212	596	220	660	227	724	233	788	239	852	244	916	250	980	254
533	212	597	220	661	227	725.	233	789	239	853	245	917	250	981	254

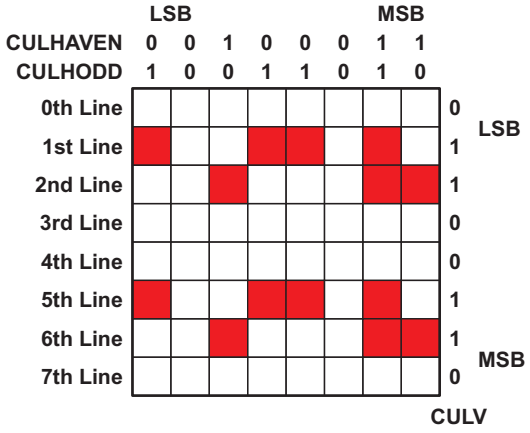
Table 28. A-Law Table (2) (continued)

Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law	Input	A-Law
534	212	598	220	662	227	726	233	790	239	854	245	918	250	982	254
535	212	599	220	663	227	727	233	791	239	855	245	919	250	983	254
536	212	600	220	664	227	728	233	792	239	856	245	920	250	984	255
537	212	601	220	665	227	729	234	793	239	857	245	921	250	985	255
538	212	602	220	666	227	730	234	794	240	858	245	922	250	986	255
539	212	603	220	667	227	731	234	795	240	859	245	923	250	987	255
540	213	604	220	668	227	732	234	796	240	860	245	924	250	988	255
541	213	605	221	669	228	733	234	797	240	861	245	925	250	989	255
542	213	606	221	670	228	734	234	798	240	862	245	926	250	990	255
543	213	607	221	671	228	735	234	799	240	863	245	927	250	991	255
544	213	608	221	672	228	736	234	800	240	864	245	928	250	992	255
545	213	609	221	673	228	737	234	801	240	865	246	929.	250	993	255
546	213	610	221	674	228	738	234	802	240	866	246	930	251	994	255
547	214	611	221	675	228	739	235	803	240	867	246	931	251	995	255
548	214	612	221	676	228	740	235	804	240	868	246	932	251	996	255
549	214	613	221	677	228	741	235	805	240	869	246	933	251	997	255
550	214	614	222	678	229	742	235	806	241	870	246	934	251	998	255
551	214	615	222	679	229	743	235	807	241	871	246	935	251	999	255
552	214	616	222	680	229	744	235	808	241	872	246	936	251	1000	255
553	214	617	222	681	229	745	235	809	241	873	246	937	251	1001	255
554	214	618	222	682	229	746	235	810	241	874	246	938	251	1002	255
555	215	619	222	683	229	747	235	811	241	875	246	939	251	1003	255
556	215	620	222	684	229	748	235	812	241	876	246	940	251	1004	255
557	215	621	222	685	229	749	235	813	241	877	246	941	251	1005	255
558	215	622	222	686	229	750	236	814	241	878	247	942	251	1006	255
559	215	623	223	687	229	751	236	815	241	879	247	943	252	1007	255
560	215	624	223	688	230	752	236	816	241	880	247	944	252	1008	255
561	215	625	223	689	230	753	236	817	242	881	247	945	252	1009	255
562	215	626	223	690	230	754	236	818	242	882	247	946	252	1010	255
563	216	627	223	691	230	755	236	819	242	883	247	947	252	1011	255
564	216	628	223	692	230	756	236	820	242	884	247	948	252	1012	255
565	216	629	223	693	230	757	236	821	242	885	247	949	252	1013	255
566	216	630	223	694	230	758	236	822	242	886	247	950	252	1014	255
567	216	631	223	695	230	759	236	823	242	887	247	951	252	1015	255
568	216	632	224	696	230	760	236	824	242	888	247	952	252	1016	255
569	216	633	224	697	230	761	237	825	242	889	247	953	252	1017	255
570	216	634	224	698	231	762	237	826	242	890	247	954	252	1018	255
571	217	635	224	699	231	763	237	827	242	891	248	955	252	1019	255
572	217	636	224	700	231	764	237	828	242	892	248	956	252	1020	255
573	217	637	224	701	231	765	237	829	243	893	248	957	253	1021	255
574	217	638	224	702	231	766	237	830	243	894	248	958	253	1022	255
575	217	639	224	703	231	767	237	831	243	895	248	959	253	1023	255

4.1.4.15 Culling

The culling block performs a programmable decimation function for both horizontal and vertical directions. The horizontal and vertical decimation of image data can be controlled by 2 registers. The 16-bit CULH register specifies the horizontal culling pattern for even and odd lines. The 8-bit CULV register specifies the pattern for the vertical direction. The LSB of CULV represent the top line of the CCD, the MSB is the 7th line. The figure below is an example showing how CULH and CULV apply a decimation pattern to the data. The pixels colored in red are transferred to DDR/SDRAM. In this case CULH = 0x59C4 and CULV = 0x0066.

Figure 50. Decimation Pattern



4.1.4.16 12 to 8-bit DPCM Compression

The DPCM compression block can compress 12-bit image data to 8-bit data for bandwidth reduction in transmission between the ISIF and the SDRAM. The IPIPE interface uses the 8-bit to 12-bit DPCM decoder so that data can be decompressed for processing.

The compression system uses two different predictors; one is simple and the other is complex. Predictor1 is very simple, so the processing power and the memory requirements are reduced with it (when the image quality is already high enough). Predictor2 gives a slightly better prediction for pixel value and the image quality can be improved with it.

4.1.4.17 SDRAM Data Storage

Data are stored to the lower bits of a 16-bit DDR/SDRAM word, or can be 8-bits or 12-bits packed. For raw data, data to be stored can be right-shifted according to the value set at CCDW.

Table 29 shows the format where data are stored to the lower bits of a 16-bit word and also the format where the data are packed to 8-bits. The unused bits are filled with zeros.

Table 29. SDRAM Data Format (1)

Bit	CCDW	SDR Pack	Upper Word		Lower Word	
			MSB(31)	LSB(16)	MSB(15)	LSB(0)
12	0	0	0	Pixel1	0	Pixel0
11	1	0	0	Pixel1	0	Pixel0
10	2	0	0	Pixel1	0	Pixel0
9	3	0	0	Pixel1	0	Pixel0
8	4	0	0	Pixel1	0	Pixel0
8-bit pack	4	2	Pixel3	Pixel2	Pixel1	Pixel0

Table 30 shows the format in which 12-bit data are packed.

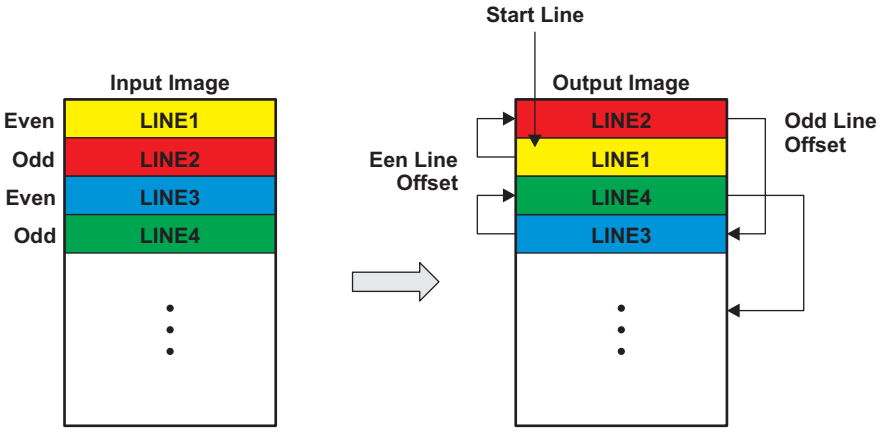
Table 30. SDRAM Data format (2)

Bit	CCDW	SDR Pack	Upper Word		Lower Word	
			MSB(31)	LSB(16)	MSB(15)	LSB(0)
12	0	1	Pixel2[7:0]		Pixel1	Pixel0
			Pixel5[3:0]	Pixel4	Pixel3	Pixel0
				Pixel7	Pixel6	Pixel5[11:4]

The ISIF has an internal, 16-bit by 16-bytes FIFO. The processed data are transferred from the FIFO to the buffer logic in 32-byte burst unit. The frequency of the SDRAM clock must be equal to or higher than the pixel clock. Data are written to SDRAM only if DWEN in SYNCEN is set to “1.”

The output formatter can configure to any image format by using SDRAM line offset register, and offset control registers. The next figure shows how to construct a frame format in SDRAM.

Figure 51. Frame Image Format Conversion

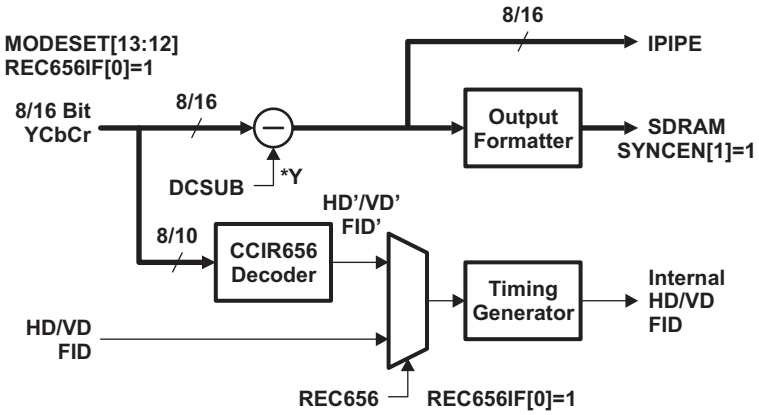


4.1.5 YCbCr Signal Processing

Figure 52 shows the YCbCr signal processing flow in the ISIF block. The ISIF accepts 4:2:2 sampled YCbCr input data. The luminance and chrominance are 8 bits each, scaled 0 to 255. The color difference signals are multiplexed into one 8-bit bus beginning with a Cb sample. The Y and CbCr busses may be input parallel (16-bit mode) or may be time-multiplexed and input as a single bus (8-bit mode). The single bus may also contain SAV and EAV video timing reference codes (ITU-R BT.656 mode). In ITU-R BT.656 mode, the ISIF is controlled by the start active video (SAV) time code in the 8-bit pixel data. All timing information is transmitted using a 4-byte synchronization pattern. A synchronization pattern is sent immediately before and after each line during active picture and retrace ISIF decodes SAV code and is synchronized at this timing.

The 16-bit or 8-bit YCbCr data are stored in SDRAM as 4:2:2 format. Table 31 shows data format in SDRAM. Y data typically has a range of 16 to 235, however, it is possible to subtract a DC value from Y signal.

Figure 52. ISIF YCbCr Data Processing Flow



4.1.5.1 DC Subtract

An offset can optionally be subtracted from the luma (Y) component of the data by programming the CLDCOFST.CLDC register field. Note that in YCbCr processing, the CLAMPCFG.CLEN field must be disabled '0' or indeterminate results may occur.

4.1.5.2 REC656 Mode

Processing of the data in REC656 mode is identical to that of the other YCbCr modes; however, there is an additional decoder block that extracts the sync information from the data signal and generates the HD/VD/Field signals for downstream processing. If data width is 10 bits, configure ISIF to YCbCr 16-bit mode (MODESET.INPMOD=1), so that 10-bit data are stored to the lower 10 bits of a 16-bit SDRAM word.

4.1.5.3 SDRAM Data Storage

In packed YCbCr 4:2.2 mode, data are stored in SDRAM with two pixels per 32 bits, shown in Table 31.

Table 31. YCbCr Mode SDRAM Output Format

SDRAM Address	Upper Word		Lower Word	
	MSB(31)	LSB(16)	MSB(15)	LSB(0)
N	Y1	Cr0	Y0	Cb0
N+1	Y3	Cr1	Y2	Cb1
N+2	Y5	Cr2	Y4	Cb2

4.1.6 Data Output Control

Data output to SDRAM is enabled via the SYNCEN.DWEN setting. The MSB of the chroma signal can also be inverted (CCDCFG.MSBINVI). The ISIF module's final stage is the line output control, which controls how the input lines are written to SDRAM. The values CADU and CADL define the starting address where the frame should be written in SDRAM. The value, HSIZE.SDOFST, defines the distance between the beginning of output lines, in bytes. Both the starting address and line offset values are programmed in 32-byte units; that is, either 16 or 32 pixels, depending on the HSIZE.PACK8 setting. the HSIZE.ADCR register bit can be set to decrement the addresses across each line to invert an image horizontally. The register SDOFST can be used to define additional offsets depending on the Field ID and even/odd line numbers. This provides a means to de-interlace an interlaced, two-field input and also to invert an input image vertically. See Figure 51 for some examples of usage.

SDOFST.FIINV — invert interpretation of the Field ID signal

SDOFST.FOFST — offset, in lines, of field = 1

SDOFST.LOFTS0 — offset, in lines, between even lines on even fields (field 0)

SDOFST.LOFTS1 — offset, in lines, between odd lines on even fields (field 0)

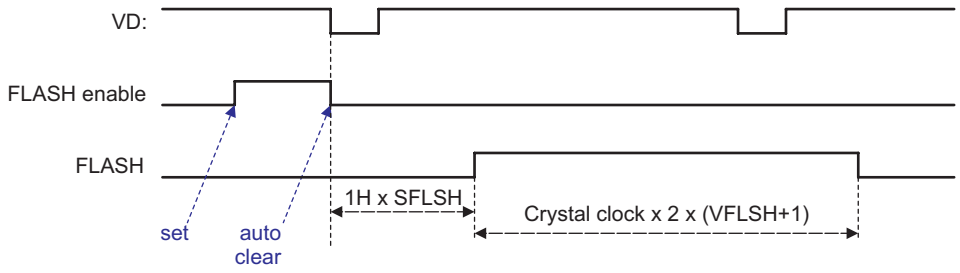
SDOFST.LOFTS2 — offset, in lines, between even lines on odd fields (field 1)

SDOFST.LOFTS3 — offset, in lines, between odd lines on odd fields (field 1)

4.1.7 Flash Timing Control

ISIF can generate a timing signal for FLASH to control the start time and the exposure period.

Figure 53. Flash Timing Signal



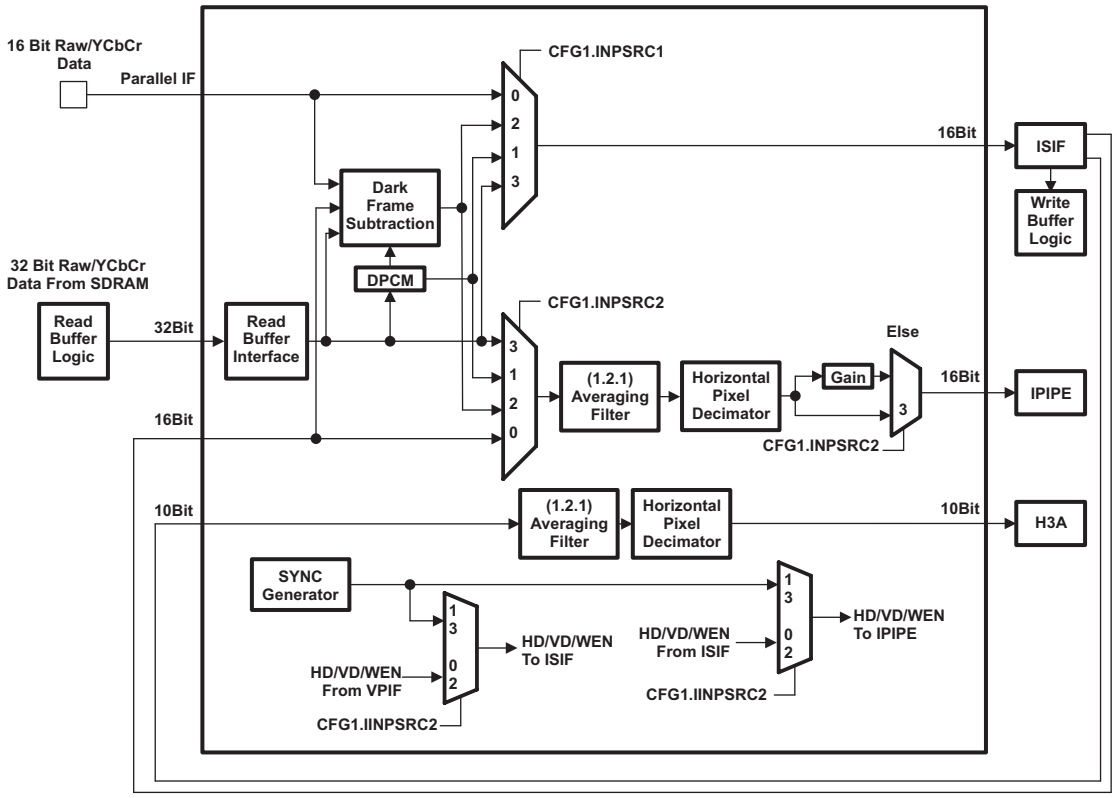
As shown in Figure 53, SFLSH is a configuration register that specifies the set timing of the FLASH signal, and VFLSH is a register that specifies the valid length of the FLASH signal. The FLASH signal is set at the beginning of the line specified by SFLSH, and remain high for Crystal clock x 2 x (VFLSH+1).

The VFLSH register is 16 bits wide, so if the Crystal clock is 48 MHz, the maximum length of the valid period will be 2.7 msec.

4.2 Image Pipe Interface (IPIPEIF)

The IPIPE Interface (IPIPEIF) is the data and sync signals input interface module for the IPIPE. The rest of this section describes the functionality of each sub-block in the IPIPEIF as shown in Figure 54.

Figure 54. Image Pipe Interface Processing Flow

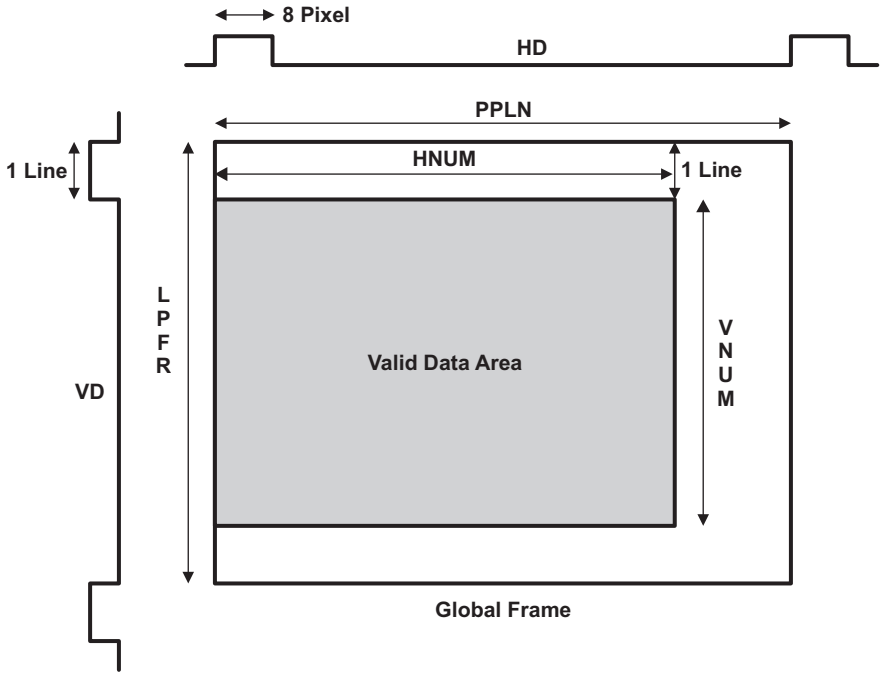


4.2.1 Input Interface and Preprocessing

The IPIPEIF consists of two major interface blocks. It can receive data from both the sensor parallel raw data via the device parallel port, and from the read buffer interface via SDRAM/DDRAM. The input sources and data type (RAW or YUV) are configured in the CFG1.INPSRC1 register field. IPIPEIF can also receive data from both the preprocessed raw data via the ISIF controller module and from the read buffer interface via SDRAM/DDRAM. The input sources and data type (RAW or YUV) are configured in the CFG1.INPSRC2 register field. The four available options for input source/type combinations and any preprocessing operations are discussed further in the following sub-sections.

When input from SDRAM/DDRAM is required, the SDRAM/DDRAM address (ADDRU, ADDRL) and line offset (ADOFS) registers must be programmed in units of 32 bytes. Additionally, the HNUM and VNUM registers define the number of pixels per line and lines per frame to read from the SDRAM as shown in Figure 55. For all SDRAM input modes except Darkfame subtract, the LPFR and PPLN registers define the interval of VD and HD, respectively.

Figure 55. Global Frame Definition in SDRAM Input Modes (except Darkframe)



4.2.2 ISIF Raw Input Mode (CFG1.INPSRC1 = CFG1.INPSRC2 = 0)

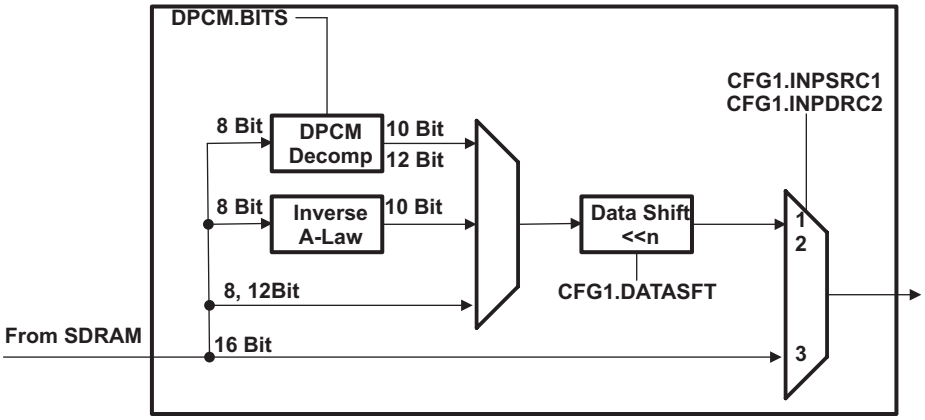
CFG1.INPSRC1
The input data is from the sensor parallel port and its data format is RAW (up to 16-bit).

CFG1.INPSRC2
The input data is from the video port interface of the ISIF and its data format is RAW (up to 12-bit)i

4.2.3 SDRAM RAW Input Mode (CFG1.INPSRC1 = CFG1.INPSRC2 = 1)

Figure 56 shows the DCPM sub-block that will be discussed in this section.

Figure 56. DPCM Sub-Block



When the input source is RAW data from the SDRAM read buffer interface, the data can either be read as 1 pixel for every 8 bits, or 16 bits in memory (CFG1.UNPACK). The 8-bit RAW data can either be linear or non-linear.

In order to save SDRAM capacity and bandwidth, the ISIF includes two options:

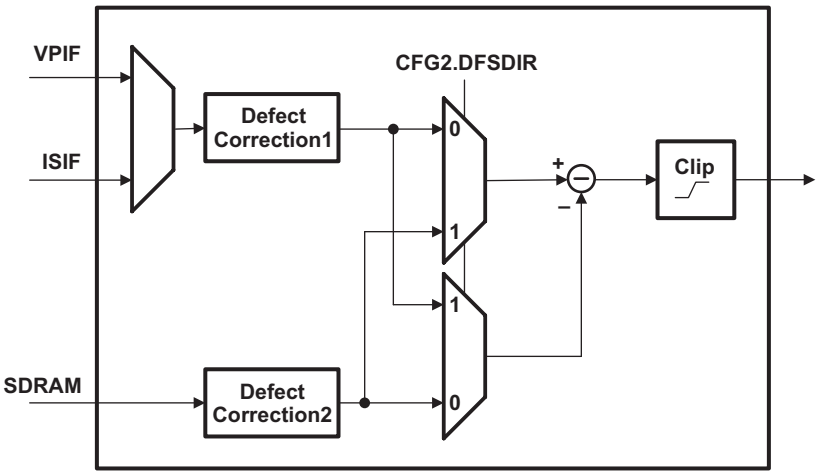
- Apply 10-bit to 8-bit A-Law compression for packing the sensor data to 1-byte per pixel. In order to process this data properly, the Inverse A-law block is provided to decompress the 8-bit non-linear data back to 10-bit linear data if enabled (CFG1.UNPACK). This 10 bit data is padded with four low zeros to form a 12-bit bus.
- Apply 12- bit to 8-bit DPCM compression for packing the sensor data to 1-byte per pixel. In order to process this data properly, the DPCM decompression block is provided to decompress the 8-bit compressed data back to 12-bit linear data if enabled (DPCM.ENA). This 12 bit data can be shifted by the CFG1.DATASFT register field to select which 12 bits to use

If the Inverse A-law and DPCM decompression are not enabled, then the data read from SDRAM can be shifted by the CFG1.DATASFT register field to select which 12 bits to use.

4.2.4 ISIF RAW Input with Dark Frame Subtract from SDRAM Mode (CFG1.INPSRC1 = CFG1.INPSRC2 = 2)

Figure 57 shows the DFS sub-block that will be discussed in this section.

Figure 57. DFS Sub-Block

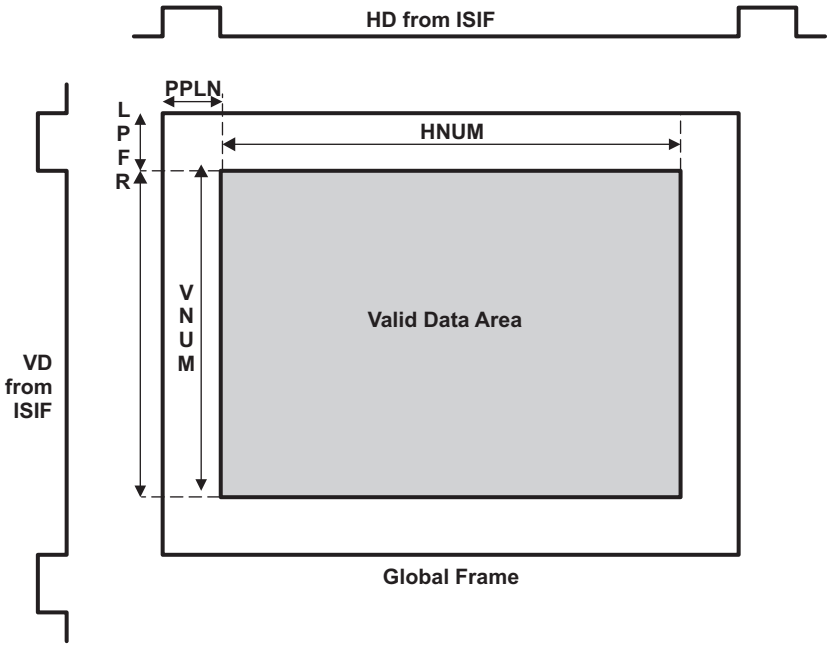


The dark frame subtract function is used to remove fixed pattern noise in the sensor. Typically, the ISIF writes a dark frame (frame captured when the shutter is closed) to SDRAM using 8 bits of linear data packed into two pixels per 16 bits. Eight bits should be enough even if the resolution of the RAW data is 12 bits, since a dark frame should not have values greater than 255 unless it is a fault pixel.

In this mode, everything from the previous two sections also applies since RAW data is used from both the ISIF and SDRAM. Data can also be read from SDRAM with CFG1.UNPACK set to '1'. Each pixel read from SDRAM will be subtracted from each pixel sent from the parallel I/F or the ISIF.

The output of the dark frame Subtract operation is 12-bits wide (U12Q0). There must be adequate SDRAM bandwidth if this feature is enabled. If the data fetched from memory arrives late, then there is no way of knowing. Also note that in dark frame subtract mode, the PPLN and LPFR registers should be used to indicate the horizontal and vertical start position of the subtraction from the ISIF data, as shown in Figure 58. The value of the LPFR must be greater than 0, since you cannot subtract the first line from the Parallel I/F or the ISIF.

Figure 58. Global Frame Definition in Darkframe Subtract Mode



4.2.5 SDRAM YCbCr 4:2:2 Input Mode

When the input source is YCbCr 4:2:2 data from the SDRAM read buffer interface, the data is expected to be stored as 16 bits in memory, so there is no shifting or other preprocessing done.

4.2.6 Timing Generation

When the input source is from the parallel port I/F (CFG1.INPSRC1 = 0 or 2), CFG1.CLKSEL should be set to '0' so that data is latched into the IPIPE using the PCLK, HD, and VD signals from the parallel port I/F.

When the input source is from the video port interface of the ISIF (CFG1.INPSRC2 = 0 or 2), CFG1.CLKSEL should be set to '0' so that data is latched into the IPIPE using the PCLK, HD, and VD signals from the ISIF.

When the input source is not from the parallel port I/F (CFG1.INPSRC1 = 1 or 3), then CFG1.CLKSEL should be set to '1' so that the IPIPEIF generates the proper timing of PCLK, HD, and VD signals to the IPIPE. The CLKDIV register is then used to select a divide ratio of the SDRAM(DMA) clock for the pixel clock frequency which is used to clock the data into the PCLK.

When the input source is not from the ISIF (CFG1.INPSRC2 = 1 or 3), then CFG1.CLKSEL should be set to '1' so that the IPIPEIF generates the proper timing of PCLK, HD, and VD signals to the IPIPE. The CLKDIV register is then used to select a divide ratio of the SDRAM(DMA) clock for the pixel clock frequency which is used to clock the data into the PCLK. The value of this register depends on the resize ratios of the IPIPE resizers and the available SDRAM system bandwidth.

When CFG1.INPSRC1 or CFG1.INPSRC2 is not set to '0', then the IPIPE I/F SDRAM data reading and timing generation can be enabled (ENABLE.ENABLE) in either one-shot mode, or continuous mode (CFG1.ONESHOT).

The SDRAM input function (1 or 3) either CFG1.INPSRC1 or CFG1.INPSRC2 can be selected. Only one can be selected at a time.

4.2.7 Averaging Filter (1,2,1)

The averaging filter can be optionally enabled by setting the CFG1.AVGFILT register bit. It acts as an anti-aliasing filter for the horizontal pixel decimator. It typically is only needed when the pixel decimator is used (CFG1.DECM = '1'). It operates on every other pixel (same color) in a RAW bayer input or every Y component in YCbCr data in the following equation: $output = (input[i-1] + 2 * input[i] + input[i+1]) >> 2$

4.2.8 Horizontal Pixel Decimator (Downsizer)

The image pipe input is limited to 2176 pixels per horizontal line due to line memory width restrictions in the various filtering blocks. In order to support sensors that output greater than 2176 pixels per line, a line width decimator can be enabled (CFG1.DECM) to downsample the input lines to a width equal to or less than the 2176 pixel maximum. The resize ratio can be configured by programming the RSZ register to be within the range from 16 to 112, to give a resampling range from 1x to 1/7x (16/RSZ).

4.2.9 RAW Data Gain

A gain factor ranging from 0.00195(1/512) to 1.99805(1023/512) is multiplied to the RAW output of the IPIPEIF. The gain constant is set in the GAIN register using U10Q9 format.

4.2.10 Defect Pixel Correction

A simple defect pixel correction can be applied to the ISIF input data path and SDRAM input data path respectively. DPC parameters provide threshold level to be replaced with neighborhood pixel or averaged pixel.

```
If (image(n) < DPC.TH) || ((image(n-2) > DPC.TH)&& (image(n+2)> DPC.TH)
                    image(n) = image(n)
Else if image(n-2) > DPC.TH
                    image(n) = image(n+2)
Else if image(n+2) > DPC.TH
                    image(n) = image(n-2)
Else
                    image(n) = (image(n-2)+ image(n+2))/2
```

4.3 Image Pipe (IPIPE)

Image Signal Processing (IPIPE) is a programmable hardware image processing module that generates image data in YCbCr-4:2:2 or YCbCr-4:2:0 format from raw CCD/CMOS data. IPIPE can also be configured to operate in a resize-only mode, which allows YCbCr-4:2:2 or YCbCr-4:2:0 to be resized without applying the processing of other modules in IPIPE. In addition, IPIPE supports output of Bayer data. The data processing paths can be configured by setting the SRC_FMT.FMT field. The output of the IPIPE is typically used for both video/image compression and display.

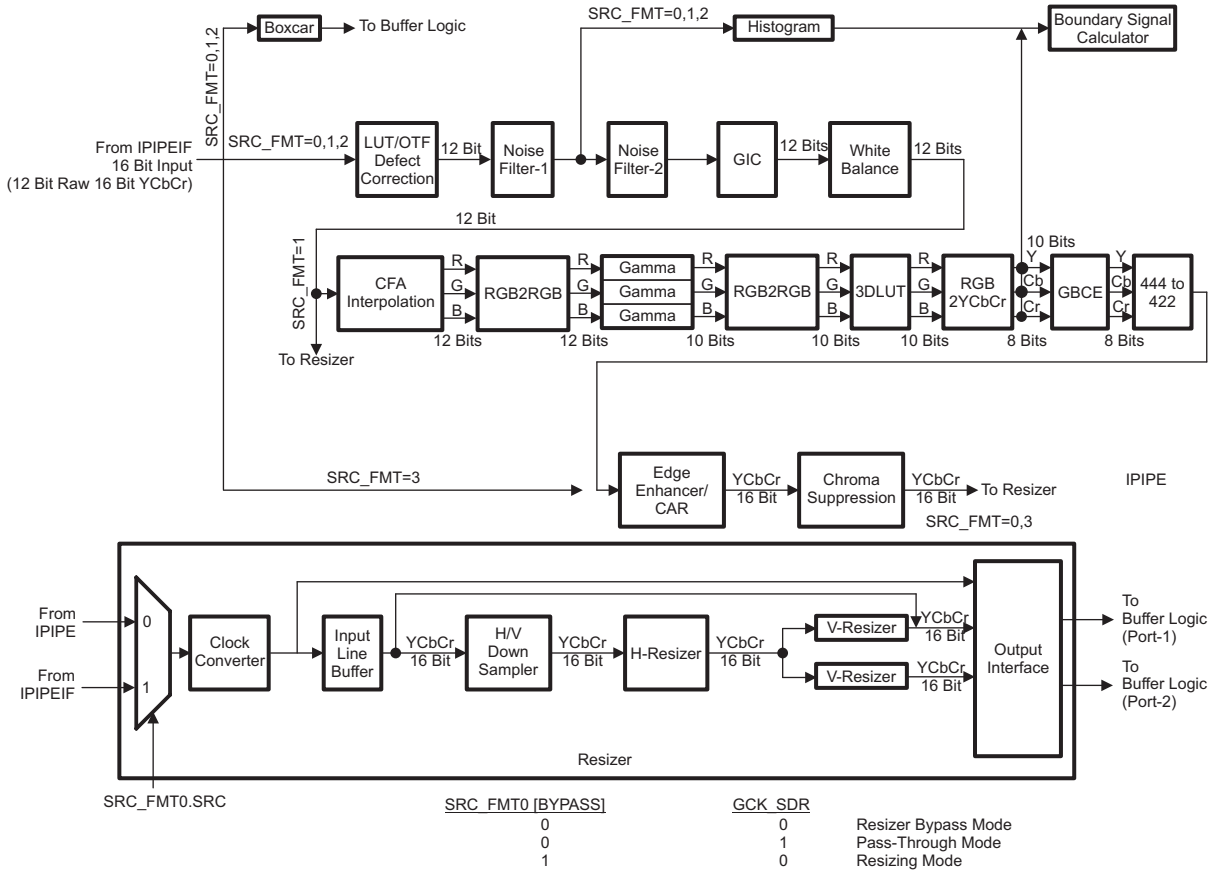
4.3.1 Data Flow in IPIPE

IPIPE has three different processing paths.

- Case 1: IPIPE reads CCD raw data and applies all IPIPE functions and stores the YCbCr (or RGB) data to SDRAM.
- Case 2: IPIPE reads CCD raw data and stores the Bayer data after white balance to SDRAM.
- Case 3: IPIPE reads YCbCr-422 data and applies edge enhancement, chroma suppression, and Resize to output YCbCr (or RG B) data to SDRAM.

IPIPE data flow is shown in Figure 59.

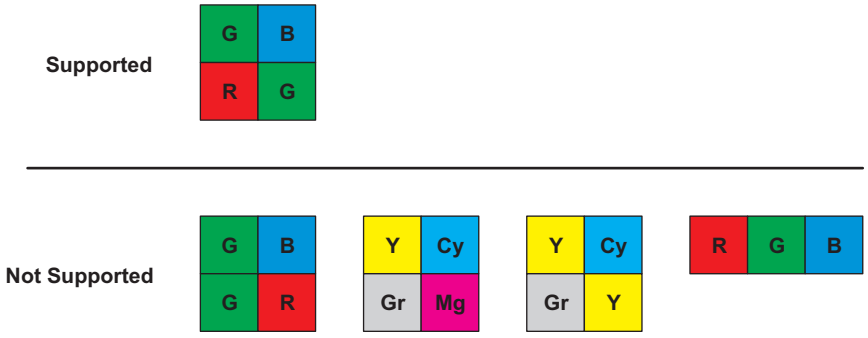
Figure 59. IPIPE Data Flow



4.3.2 CFA Arrangements

IPIPE supports raw data in Bayer formats as shown in Figure 60. Other RGB formats or complementary color formats are not supported.

Figure 60. Conventional 2x2 CFA Formats



4.3.3 Input Interface

The IPIPE engine receives 12-bit RAW image data or 16-bit YCbCr data via IPIPEIF. IPIPE can work with up to 2176 pixels in each horizontal line, except in RAW pass-through mode. If the image width is larger than 2176, it must be scaled down at IPIPEIF. Otherwise, the input image must be split into several blocks. If the input data is YCbCr, all RGB processing modules are skipped, and only edge enhancer, chroma artifact reduction (CAR), chroma suppression, and resizer are applied to the input data. If the input data is YCbCr-420, only Y or C may be processed at a time, and only the resizer process can be applied. In RAW pass-through mode, images up to 8190 pixels per line may be processed. In RAW pass-through mode, the input data is directly written out to SDRAM.

The input to IPIPE is in the following formats.

Table 32. IPIPE Input Format

IPIPE Input	RAW	LOW	LOW	LOW	LOW	RAW11	RAW10	RAW9	RAW8
	YCbCr 16 bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	Y 8 bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	CbCr 8 bit	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
IPIPE Input	RAW	RAW7	RAW6	RAW5	RAW4	RAW3	RAW2	RAW1	RAW0
	YCbCr 16 bit	Cb/Cr7	Cb/Cr6	Cb/Cr5	Cb/Cr4	Cb/Cr3	Cb/Cr2	Cb/Cr1	Cb/Cr0
	Y 8 bit	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
	CbCr 8 bit	Cb/Cr7	Cb/Cr6	Cb/Cr5	Cb/Cr4	Cb/Cr3	Cb/Cr2	Cb/Cr1	Cb/Cr0

4.3.4 LUT Defect Correction

The look-up-table (LUT) defect pixel correction is the first stage of the IPIPE image-processing pipeline. The LUT defect correction module fixes defects in input data. LUT defect correction module supports up to 256 defect point table. However, the table may be renewed as required during image processing. Therefore the maximum number of defect information is only limited by system level performance. The module uses two sets of 128x29 memories to hold defect information. The table contains the information of horizontal position (13 bits), vertical position (13 bits), and correction method (3 bits) as shown in Table 33. The information must be listed in the order of "from left to right" and "from the top to the bottom." The first position in defect information table and the number of defects which are actually used may be specified through register values. For correcting border pixels (top, bottom, left and right), data are properly mirrored.

Table 33. Defect Information Packing

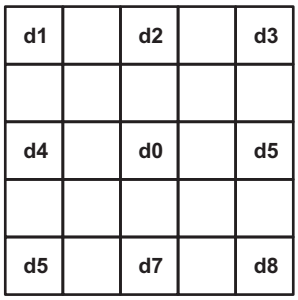
Correction Method	Vertical Position	Horizontal Position
28..26	25..13	12..0

The correction methods are described in Table 34. The pixels in defect correction methods are numbered as shown in Figure 61.

Table 34. LUT Methods

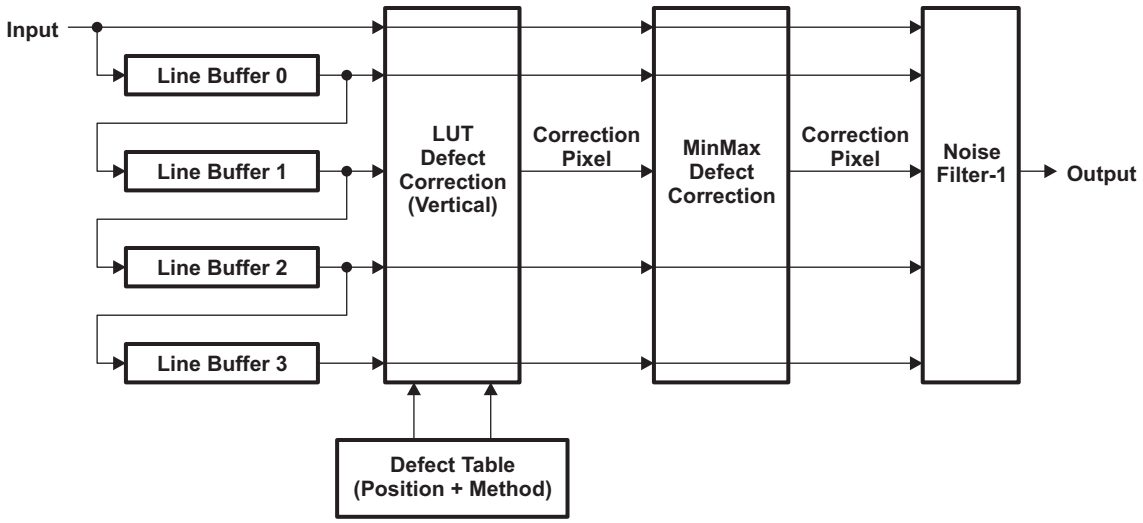
Method	Processing
0	Replace with black dot (or a white dot) to force OTF-DPC to work on the pixel
1	Copy from left (d4)
2	Copy from right (d5)
3	Horizontal interpolation (d4+d5)/2
4	Vertical interpolation (d2+d7)/2
5	Copy from top d2
6	Copy from bottom d7
7	2D interpolation (d2+d4+d5+d7)/2

Figure 61. Numbering in Defect Correction Algorithm



The defect correction process is described in Figure 62.

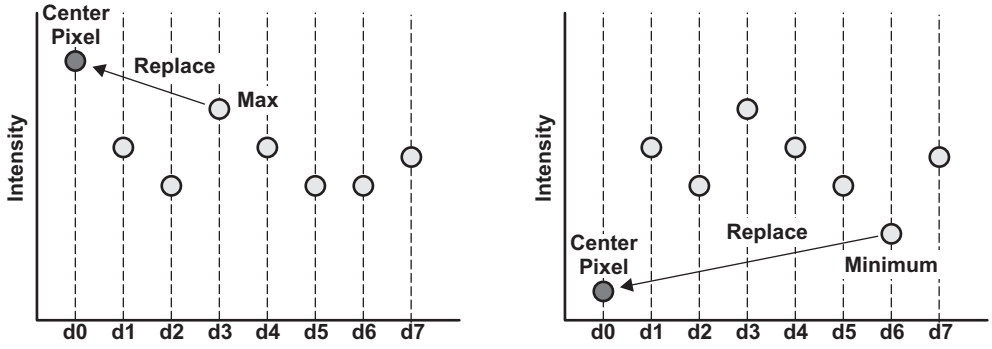
Figure 62. LUT Defect Correction Process



4.3.5 OTF Defect Pixel Correction

In the OTF defect correction module, each pixel is compared with the surrounding eight pixels in the same color plane. If the center pixel is larger than the maximum pixel among them, the output is the second largest value. If the center pixel is the minimum pixel among them, it is replaced by the second smallest value. If the center pixel is neither the maximum nor minimum, the center pixel is the output.

Figure 63. MinMax Defect Correction



The MinMax Defect Correction module also supports couplet defect correction (MinMax2 Defect Correction). In MinMax2 Defect Correction (see Figure 63), the center pixel is compared with the 2nd maximum and the second minimum pixel among the surrounding eight pixels. If the center pixel is larger than the second maximum signal by more than thrD, the center pixel is considered as a defect pixel. Then, the center pixel is replaced with the maximum value of surrounding pixels, unless the difference between the maximum pixel and the second maximum value is larger than thrC (Figure 64). In that case, the center pixel is replaced with the second maximum pixel (Figure 65).

Figure 64. MinMax Defect Pixel Correction (dmax)

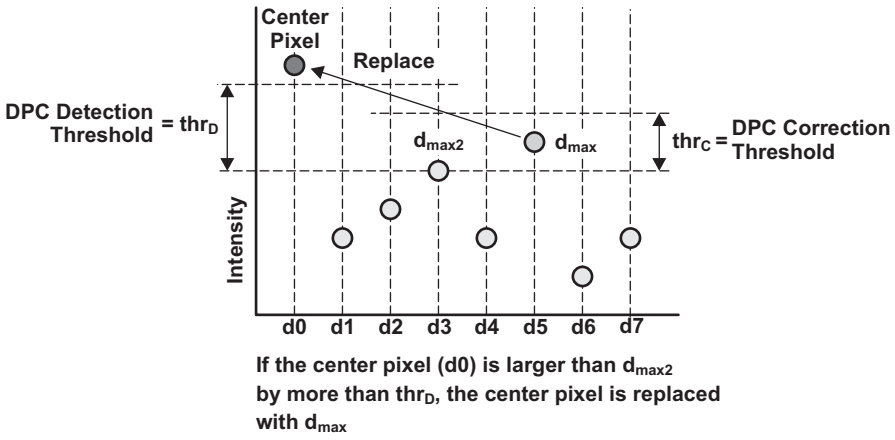
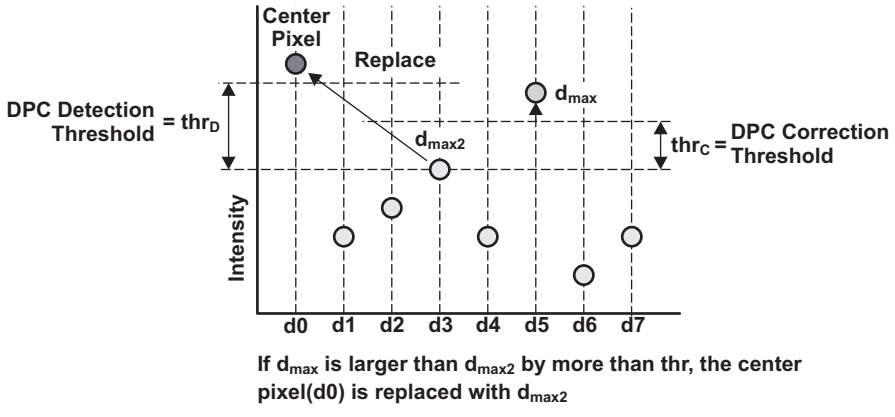


Figure 65. MinMax Defect Pixel Correction (dmax2)



The minimum side is treated in the same way with opposite signs. In summary, the center pixel is replaced in the following manner.

$$d_0' = \begin{cases} d_{max} & (d_0 > d_{max\,2} + thr_D)\,and\,(d_{max} \le d_{max\,2} + thr_C) \\ d_{max\,2} & (d_0 > d_{max\,2} + thr_D)\,and\,(d_{max} > d_{max\,2} + thr_C) \\ d_{min} & (d_0 < d_{min\,2} - thr_D)\,and\,(d_{min} \ge d_{min\,2} - thr_C), \\ d_{min\,2} & (d_0 < d_{min\,2} - thr_D)\,and\,(d_{min} < d_{min\,2} - thr_C) \\ d_0 & otherwise \end{cases}$$

Here, d_{max} and d_{max2} are the maximum and the second maximum of the surrounding pixels, and d_{min} and d_{min2} are the minimum and the second minimum, respectively. The parameters thrD and thrC may be independently set for each color component.

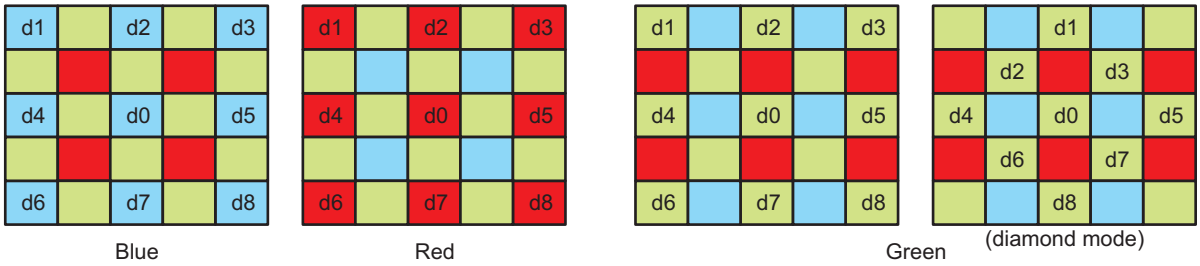
In DPC2.0 mode of MinMax2, threshold values are statically specified by register values. The thrD and thrC are independently specified for each color (R, Gr, Gb, or B) by DPC_OTF_2_D_THR_*X* and DPC_OTF_2_C_THR_*X* (*X* is one of R, GR, GR, or B).

DPC3.0 mode of the MinMax2 algorithm calculates the threshold values from the activity of the surrounding pixels.

4.3.6 Noise Filter

The two-dimensional noise filter reduces noise in raw input data. Data points used for this filtering is shown in Figure 66. The pixel being filtered is "d0". "d0" ~ "d8" are same color pixels. Two numbering methods are available for green.

Figure 66. Noise Filter Array



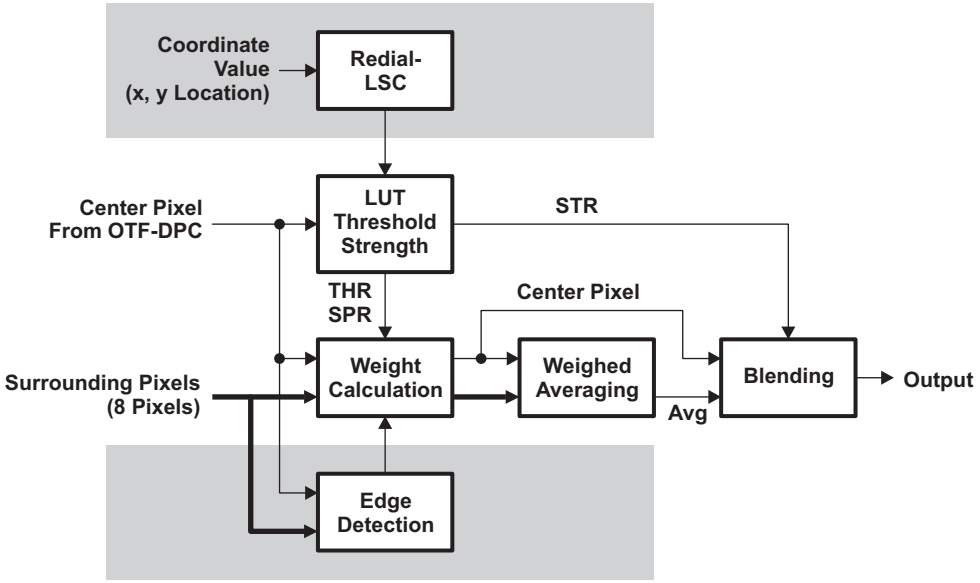
The basic concept of the 2D noise filter is area averaging by excluding far-apart-value neighbors. This algorithm uses the following two tables:

- Threshold table (10 bits, 8 entries) which is used in the filtering algorithm
- Intensity table (5 bits, 8 entries) which stores the averaging weight

THR and STR are read from the look-up table and interpolated to create the intermediate value. SPR is set through the register. The noise filter is applied according to the following equations. The block diagram of the noise filter module is shown in Figure 67.

The threshold value is multiplied by radial-LSC gain g (u4.5) to compensate the noise increase caused by lens-shading correction module in ISIF.

Figure 67. Noise Filter Module Block Diagram



The threshold and strength values are read from the LUT in the manner described in Table 35.

Table 35. Noise Filter LUT

Input>>shf	THR (u10)	STR (u5)
0-127	THR0	STR0
128-255	THR1	STR1
256-383	THR2	STR2
384-511	THR3	STR3
512-639	THR4	STR4
640-767	THR5	STR5
768-895	THR6	STR6
896-1023	THR7	STR7
Noise filter LUT. For an intermediate input value, the output values are linearly interpolated between two entries.		

THR0-7 and STR0-7 are specified by DF2_1ST_THR[0-7] and DF2_1ST_STR[0-7] in 2D-Noise Filter 1. Edge detection finds edges and controls the weight accordingly. If this function is enabled, horizontal or vertical edge is detected through the equations shown below (the numbering in these equations is always in box mode). Here, *min* and *max* are specified by D2F_1ST_EDG_MIN, and D2F_1ST_EDG_MAX in 2D-Noise Filter 1.

$$hedge = abs\left(\frac{(d_1 + 2d_2 + d_3) - (d_6 + 2d_7 + d_8)}{8}\right)$$

$$vedge = abs\left(\frac{(d_1 + 2d_4 + d_6) - (d_3 + 2d_5 + d_8)}{8}\right)$$

$$hedge > max, vedge < min \Rightarrow horizontal\ edge$$

$$hedge < min, vedge > max \Rightarrow vertical\ edge$$

The threshold value is multiplied by radial-LSC gain g (u4.5) to compensate the noise enhancement caused by the lens-shading-correction module in ISIF.

4.3.7 Green-Imbalance Correction (GIC)

Green-Imbalance-correction (GIC) is implemented to reduce the effect of line-crawling (Gb-Gr difference), and it works only on Gb and Gr. IPIPE contains two algorithms; one is a simple lowpass filtering with constant gain and the other is an adaptive gain control algorithm.

The simple averaging algorithm is applied in the following way. When the center site is green (Gb or Gr), the 2D pre-filter mixes G_0 and $Gs_2 = (G_a + G_b + G_c + G_d)/4$ with a constant gain value set by the register.

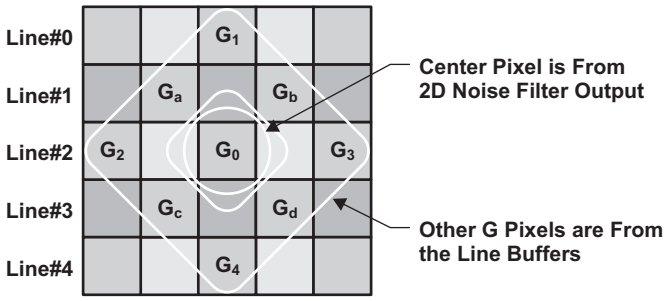
GOUT = ((256 - gain) G_0 / 128 + gain Gs_2 /128+1) /2

$Gs_2 = (G_a + G_b + G_c + G_d)/4$

0 ≤ gain ≤128

Here, G_0 is the output of the 2D noise filter, and G_a through G_d are the surrounding pixels from line buffers as shown in Figure 68.

Figure 68. GIC Pixels



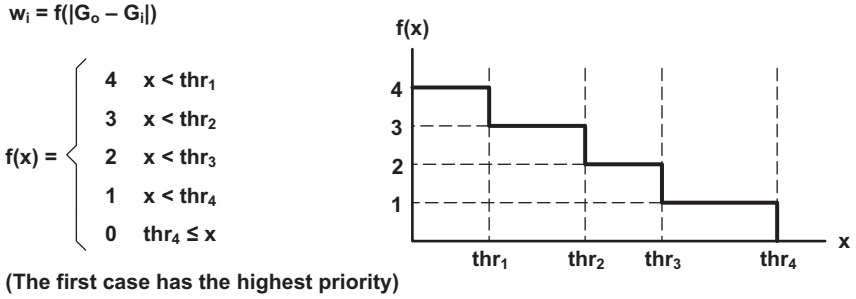
The adaptive algorithm is applied in the following way. The output data GOUT is a weighted average of the center and the surrounding four pixels.

$$G_0' = \frac{\{(32 - 2w_1 - 2w_2 - 2w_3 - 2w_4)\cdot G_0 + (w_1 + w_2)\cdot G_a + (w_1 + w_3)\cdot G_b + (w_2 + w_4)\cdot G_c + (w_3 + w_4)\cdot G_d + 16\}}{32}$$

$$G_{OUT} = ((256 - gain)\cdot G_0/128 + gain\cdot G'_0/128 + 1)/2$$

The weight coefficients (w_1, w_2, w_3, and w_4) are determined by the function shown in Figure 69. The output mixing ratio w_t is determined by the register. These parameters are defined independently for each color (R, Gr, Gb, and B).

Figure 69. Adaptive GIC Weight Function



The threshold values are calculated in the following manner. gLSC is radial-LSC gain and is explained in Section 4.3.6.

$$thr_0 = clip\left(\left(GIC\_THR \times g_{LSC}\right) >> 5\right)$$

$$thr_1 = clip\left(\left(\left(GIC\_THR + GIC\_SLP\right) \times g_{LSC}\right) >> 5\right)$$

$$thr_2 = clip\left(\left(\left(GIC\_THR + 2 \times GIC\_SLP\right) \times g_{LSC}\right) >> 5\right)$$

$$thr_3 = clip\left(\left(\left(GIC\_THR + 3 \times GIC\_SLP\right) \times g_{LSC}\right) >> 5\right)$$

The threshold values (thr1 to thr4) may be replaced with the threshold value of NF-2. The parameters *nf_thr* and *nf_dif* are identical to *thr* and *dif* in Section 4.3.6 . g_{GIC} is a U8Q5 gain specified by register value GIC_NFGAN.

$$thr_0 = clip\left(\left(nf\_thr \times g_{GIC}\right) >> 5\right)$$

$$thr_1 = clip\left(\left(\left(nf\_thr + nf\_dif\right) \times g_{GIC}\right) >> 5\right)$$

$$thr_2 = clip\left(\left(\left(nf\_thr + 2 \times nf\_dif\right) \times g_{GIC}\right) >> 5\right)$$

$$thr_3 = clip\left(\left(\left(nf\_thr + 3 \times nf\_dif\right) \times g_{GIC}\right) >> 5\right)$$

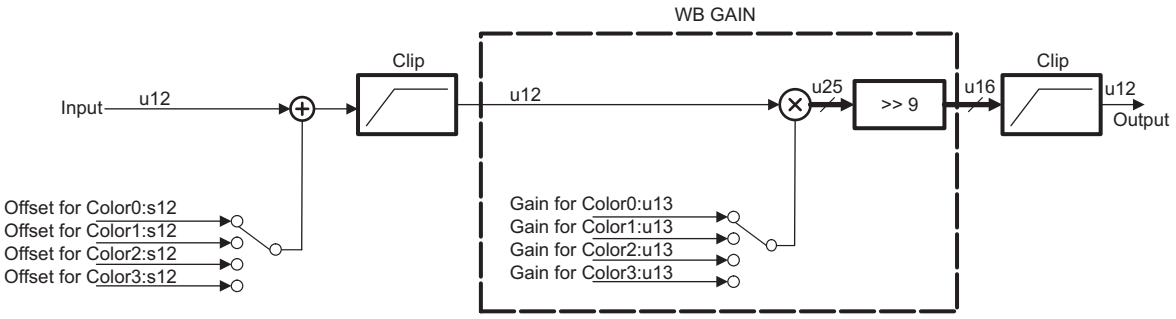
4.3.8 White Balance

The white balance module executes white balance to each color component. White balance gains adjust a ratio of each color in a CFA pattern.

Figure 70 shows a block diagram of this white balance module. In the white balance gain adjuster, the raw data is multiplied by a selected gain corresponding to the color. The white balance gain can be selected from four 13-bit values. Firmware can assign any combination of four pixels in the horizontal and vertical direction. The precision of each gain is as follows:

- OFFSET: -2048 to +2047
- WB GAIN: x 0 – x 15.998 (step = 1/512)

Figure 70. White Balancing in IPIPE

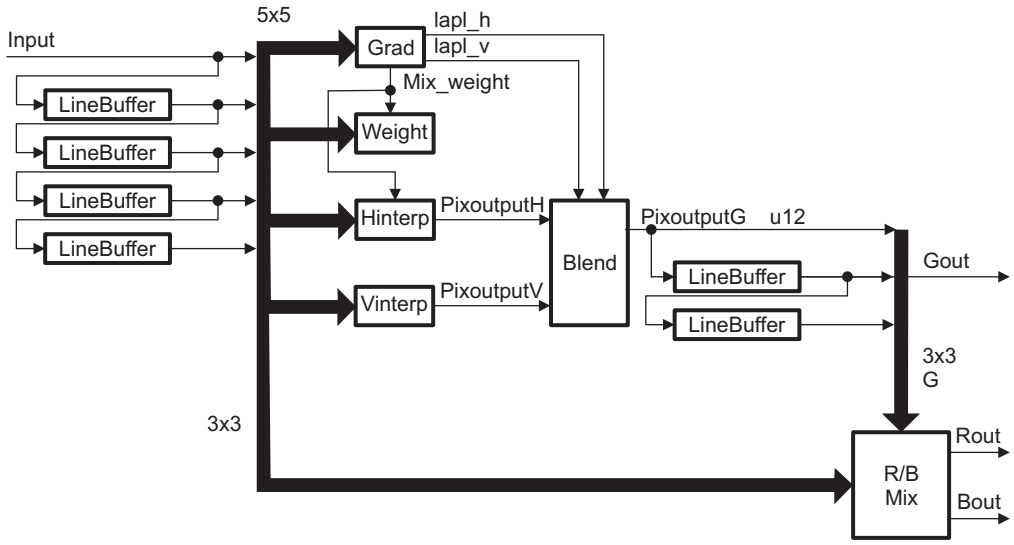


4.3.9 CFA Interpolation

The IPIPE CFA (color filter array) interpolation module generates RGB 4:4:4 data from a Bayer RGB pattern. The block diagram of the CFA (color filter array) interpolation module is shown in Figure 71. The color filter array consists of the line delay block, the edge-direction detector, and the pixel interpolator. The edge-direction detector detects most probable edge direction of an object to which the target pixel belongs, and the pixel interpolator calculates the missing color according to its edge direction within 5×5 pixel window.

The CFA interpolation module also supports digital anti-aliasing (DAA) which reduces aliasing caused by under-sampling.

Figure 71. CFA Interpolation Functional Model



4.3.10 RGB2RGB Blending Module

The RGB2RGB blending module transforms the RGB data generated by the CFA interpolation module using a 3×3 square matrix transformation in combination with an added offset. The RGB to RGB blending is calculated using the following formula. Each gain range is from -8 to +7.996 with step 1/256 = 0.004. The offset is -4096 to 4095.

$$\begin{pmatrix} R\_out \\ G\_out \\ B\_out \end{pmatrix} = \begin{pmatrix} gain\_RR & gain\_GR & gain\_BR \\ gain\_RG & gain\_GG & gain\_BG \\ gain\_RB & gain\_GB & gain\_BB \end{pmatrix} \begin{pmatrix} R\_in \\ G\_in \\ B\_in \end{pmatrix} + \begin{pmatrix} offset\_R \\ offset\_G \\ offset\_B \end{pmatrix}$$

4.3.11 Gamma Correction Module

The gamma correction module performs a gamma correction independently for each color in the RGB color space by using a piece-wise linear interpolation. The ROM table and RAM table are selectable through a register. Each RAM table has 512 entries, and each entry accommodates a 10-bit offset and 10-bit slope (see Figure 74). The range of slope value is from -512 to +511. The ROM table has 1024 entries and an output of 8-bit value. As shown in Figure 54, this module exists independently for each color so that the independent setting is possible. Figure 72 shows a block diagram of the gamma correction module. It is composed of two tables and one selector. When the BYPASS bit is asserted, the input data is divided by 16. Figure 73 shows an example of the gamma curve.

Figure 72. Gamma Correction Module Block Diagram

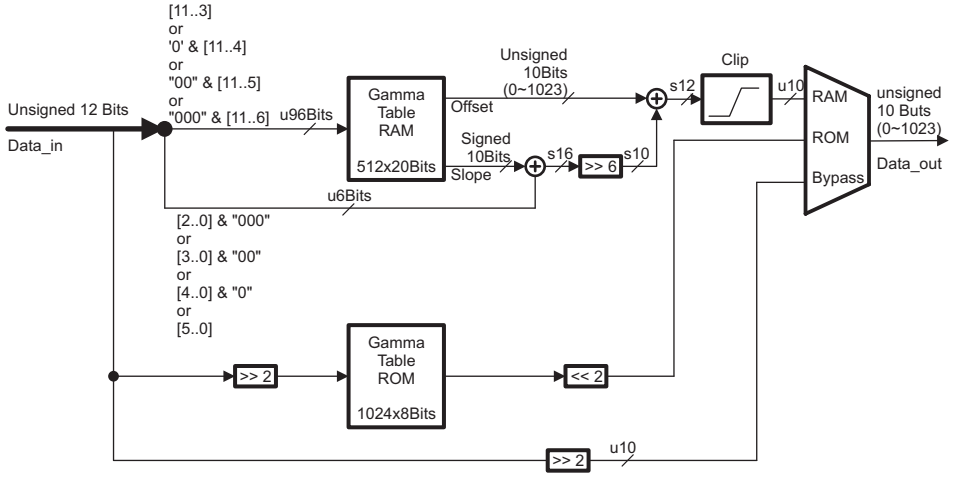


Figure 73. Example of Gamma Curve

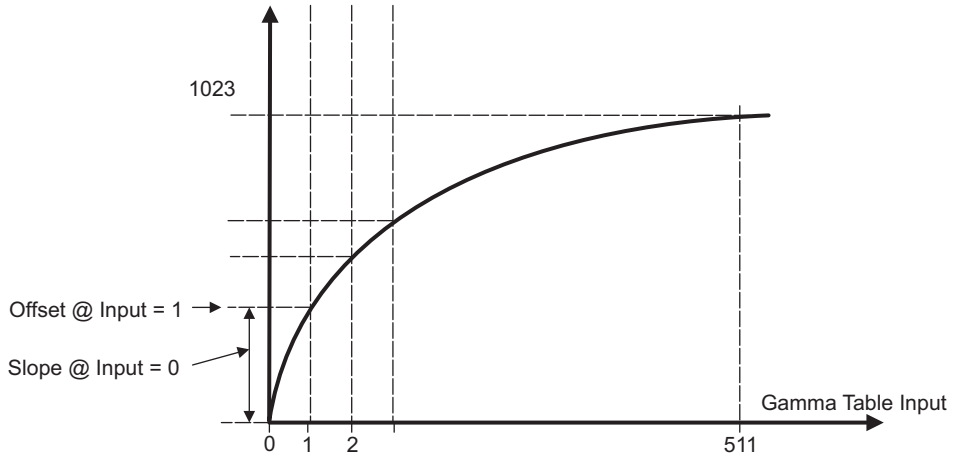


Figure 74. Gamma Table Offset/Slope Packing

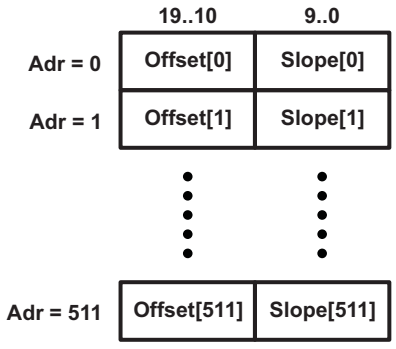


Table 36. LUT Memory Regions for Gamma Correction

Memory Region	Address Range	Description
IPIPE_GAMR_TB	0x01C7A800 – 0x01C7AFFF	IPIPE Gamma LUT for R
IPIPE_GAMG_TB	0x01C7B000 – 0x01C7B7FF	IPIPE Gamma LUT for G
IPIPE_GAMB_TB	0x01C7B800 – 0x01C7BFFF	IPIPE Gamma LUT for B

4.3.12 Second RGB2RGB Conversion Matrix

The second RGB2RGB blending module transforms the RGB data after gamma correction using a 3x3 square matrix transformation in combination with an added offset. The RGB to RGB blending is calculated using the following formula. Each gain range is from -4 to +3.996 with step 1/256 = 0.004 (s3.8). The offset is -1024 to 1023 (s11).

$$\begin{pmatrix} R\_out \\ G\_out \\ B\_out \end{pmatrix} = \begin{pmatrix} gain\_RR & gain\_GR & gain\_BR \\ gain\_RG & gain\_GG & gain\_BG \\ gain\_RB & gain\_GB & gain\_BB \end{pmatrix} \begin{pmatrix} R\_in \\ G\_in \\ B\_in \end{pmatrix} + \begin{pmatrix} offset\_R \\ offset\_G \\ offset\_B \end{pmatrix}$$

4.3.13 3D LUT Color Conversion

The 3-D LUT converts RGB pixel data into another RGB data using a 9x9x9 entry three-dimensional look-up-table. Input and output are both in 10-bit format. If the input is at the lattice point, the output is the value stored in the table.

$R_{out} = LUT_R\ [P(R_{in} \bmod 128, G_{in} \bmod 128, B_{in} \bmod 128)]$ $\quad R_{in} \bmod 128 = 0$

$G_{out} = LUT_G\ [P(R_{in} \bmod 128, G_{in} \bmod 128, B_{in} \bmod 128)]$ $\quad G_{in} \bmod 128 = 0$

$B_{out} = LUT_B\ [P(R_{in} \bmod 128, G_{in} \bmod 128, B_{in} \bmod 128)]$ $\quad B_{in} \bmod 128 = 0$

The entry number is determined by the following equation:

$$P(R, G, B) = R + 9G + 81B$$

If the input is not on the lattice point, the output is determined by the tetrahedral interpolation.

$R_i = R \bmod 128$ $\quad R_{dif} = R - 128 = R_i$

$G_i = G \bmod 128$ $\quad G_{dif} = G - 128 = G_i$

$B_i = B \bmod 128$ $\quad B_{dif} = B - 128 = B_i$

$R_0 = LUT_R[P0]$	$G_0 = LUT_G[P0]$	$B_0 = LUT_B[P0]$
$R_1 = LUT_R[P1]$	$G_1 = LUT_{G[P1]}$	$B_1 = LUT_B[P1]$
$R_2 = LUT_R[P2]$	$G_2 = LUT_G[P2]$	$B_2 = LUT_B[P2]$
$R_3 = LUT_R[P3]$	$G_3 = LUT_G[P3]$	$B_3 = LUT_B[P3]$

$R_{out} = R_0 + (R_1 - R_0)\ x + (R_2 - R_1) * y + (R_3 - R_2) * z$

$G_{out} = G_0 + (G_1 - G_0)\ x + (G_2 - G_1) * y + (G_3 - G_2) * z$

$B_{out} = B_0 + (B_1 - B_0)\ x + (B_2 - B_1) * y + (B_3 - B_2) * z$

P0-P3 and x, y, and z are determined by Table 37.

Table 37. 3D LUT Content

Input/Output Condition					
Input Condition	P0	P1	P2	P3	(X, Y, Z)
$R_{dif}=>G_{dif}=>B_{dif}$	(R_i, G_i, B_i)	(R_i+1, G_i, B_i)	$(R_i+1, G_i, +1, B_i)$	(R_i+1, G_i+1, B_i+1)	$R_{dif}=>G_{dif}=>B_{dif}$
$R_{dif}=>Bdif=>G_{dif}$	(R_i, G_i, B_i)	(R_i+1, G_i, B_i)	(R_i+1, G_i, B_i+1)	(R_i+1, G_i+1, B_i+1)	$R_{dif}=>Bdif=>G_{dif}$
$G_{dif}=>Rdif=>B_{dif}$	(R_i, G_i, B_i)	(R_i, G_i+1, B_i)	(R_i+1, G_i+1, B_i)	(R_i+1, G_i+1, B_i+1)	$G_{dif}=>Rdif=>B_{dif}$
$G_{dif}=>Bdif=>R_{dif}$	(R_i, G_i, B_i)	(R_i, G_i+1, B_i)	$(Ri, Gi+1, B_i+1)$	(R_i+1, G_i+1, B_i+1)	$G_{dif}=>Bdif=>R_{dif}$
$B_{dif}=>Rdif=>G_{dif}$	(R_i, G_i, B_i)	(R_i, G_i, B_i+1)	(R_i+1, G_i, B_i+1)	(R_i+1, G_i+1, B_i+1)	$B_{dif}=>Rdif=>G_{dif}$
$B_{dif}=>Gdif=>R_{dif}$	(R_i, G_i, B_i)	(R_i, G_i, B_i+1)	(R_i, G_i+1, B_i+1)	(R_i+1, G_i+1, B_i+1)	$B_{dif}=>Gdif=>R_{dif}$

Here, x, y, and z are: x = X/128; y = Y/128; z = Z/128

For example, if R_{dif}=>G_{dif}=>B_{dif},

$$P_0 = P(R_i, G_i, B_i) = R_i + 9G_i + 81B_i$$
$$P1 = P(R_i + 1, G_i, B_i) = (R_i + 1) + 9G_i + 81B_i = P_0 + 1$$
$$P2 = P(R_i + 1, G_i + 1, B_{i)} = (R_i + 1) + 9(G_i + 1) + 81B_i = P_0 + 10$$
$$P3 = P(R_i + 1, G_i + 1, B_i + 1) = (R_i + 1) + 9(G_i + 1) + 81(B_i + 1) = P_0 + 91$$

P0, P1, P2, and P3 are always in different banks. the data in LUT are packed in a manner described in Figure 75.

Figure 75. 3D LUT Data Packing

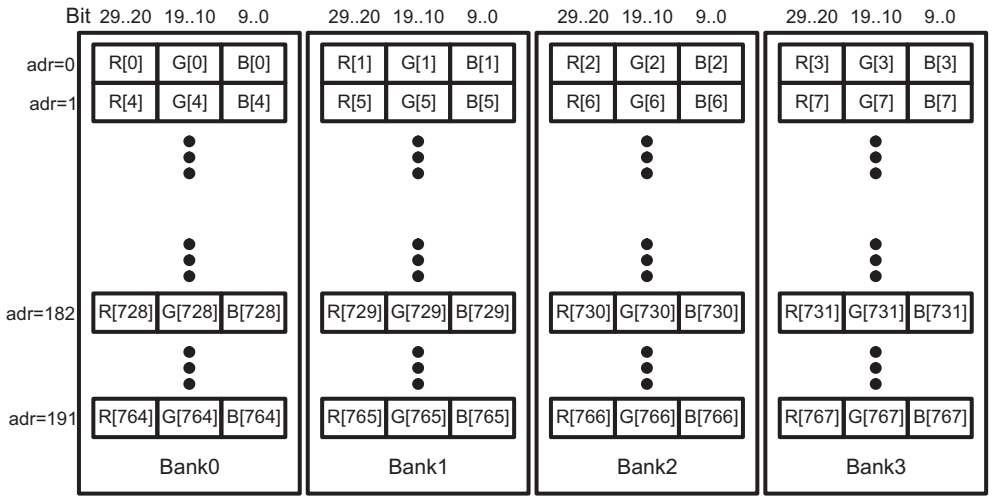


Table 38. LUT Memory Regions for 3D LUT

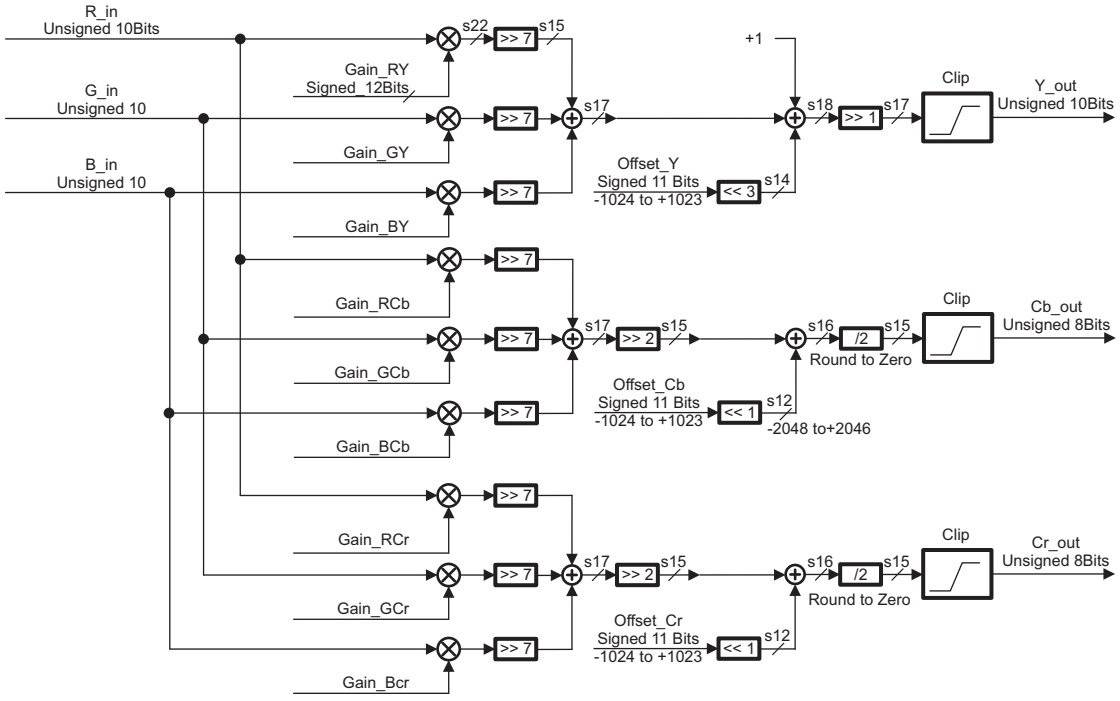
Memory Region	Address Range	Description
IPIPE_D3L_TB0	0x01C79800 – 0x01C79BFF	IPIPE_ 3D_LUT#0
IPIPE_D3L_TB1	0x01C79C00 – 0x01C79FFF	IPIPE_ 3D_LUT#1
IPIPE_D3L_TB2	0x01C7A000 – 0x01C7A3FF	IPIPE_ 3D_LUT#2
IPIPE_D3L_TB3	0x01C7A400 – 0x01C7A7FF	IPIPE_3D_LUT#3

4.3.14 RGB2YCbCr Conversion Matrix

This module transforms the RGB data to YCbCr data format using a 3x3 square matrix transformation in combination with an added offset. The transform is calculated using the following equation. Each gain range is from -8 to +7.996 with step 1/256 = 0.004. The offset is -1024 to 1023 for Y, Cb, and Cr. The block diagram of the RGB to RGB blending module is shown in the next page. The output is calculated by the following equation. The output is calculated with the following equation:

$$\begin{bmatrix} Y\_out \\ Cb\_out \\ Cr\_out \end{bmatrix} = \begin{bmatrix} gain\_RY & gain\_GY & gain\_BY \\ gain\_RCb & gain\_GCb & gain\_BCb \\ gain\_RCr & gain\_GCr & gain\_BCr \end{bmatrix} \begin{bmatrix} R\_in \\ G\_in \\ B\_in \end{bmatrix} + \begin{bmatrix} offset\_Y \\ offset\_Cb \\ offset\_Cr \end{bmatrix}$$

Figure 76. RGB2YCbCr Module Block Diagram



4.3.15 Global Brightness and Contrast Enhancement

Global brightness and contrast enhancement (GBCE) applies adaptive tone mapping on the Y channel for the best image quality. The Y channel is converted by the 1024 entry 8-bit output look-up-table. The look-up-table is calculated by software and written to IPIPE's memory table before capturing the target frame.

$$Y_{output} = LUT\left[Y_{input}\right]$$
$$Cb_{output} = Cb_{input} \quad \text{(GBCE Mode 1)}$$
$$Cr_{output} = Cr_{input}$$

The GBCE also has another (mode-2), where Y and C signals are multiplied by a gain value. The gain value is a function of Y input, and is in unsigned 10-bit format.

$$Y_{output} = clip_{U8}\left(\left(gain \times Y_{input}\right) >> 10\right)$$
$$Cb_{output} = clip_{U8}\left(\frac{\left(gain \times Cb_{input}\right)}{256}\right) \quad \text{(GBCE mode 2)}$$
$$Cr_{output} = clip_{U8}\left(\frac{\left(gain \times Cr_{input}\right)}{256}\right)$$
$$gain = LUT\left[Y_{input}\right]$$

If the GBCE is off, the Y value is converted to u8 and Cb and Cr are not changed.

$$Y_{output} = \left(Y_{input} + 2\right) >> 2$$
$$Cb_{output} = Cb_{input} \quad \text{(GBCE off)}$$
$$Cr_{output} = Cr_{input}$$

The table is packed in 20 bits in the following manner:

Table 39. GBCE LUT Packing in Mode 1

	19..18	17..10	9..8	7..0
adr = 0		LUT[1]		LUT[0]
adr = 1		LUT[3]		LUT[2]
		. .		. .
adr = 511		LUT[1023]		LUT[1022]

Table 40. GBCE LUT Packing in Mode 2

	19..10	9..0
adr = 0	LUT[1]	LUT[0]
adr = 1	LUT[3]	LUT[2]
	. .	. .
adr = 511	LUT[1023]	LUT[1022]

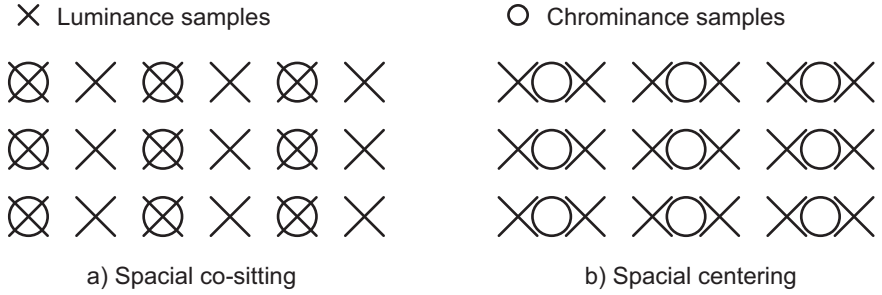
Table 41. LUT Memory Regions for GBCE

Memory Region	Address Range	Description
IPIPE_GBC_TB	0x01C79000 – 0x01C797FF	IPIPE GBCE LUT

4.3.16 4:2:2 Conversion Module

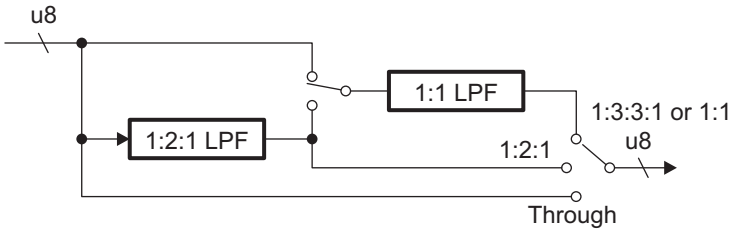
The 4:2:2 conversion module converts the image data to YCbCr-4:2:2 format by taking the average of every two Cb and Cr components. Y and Cb/Cr sampling point of either spatial co-sited or spatial centering are selectable. Horizontal 3 taps and 4 or 2 taps filters are used for spatial co-sited and spatial centering, respectively.

Figure 77. Chroma Sub-Sampling Position



A block diagram of 4:2:2 conversion module is shown in Figure 78.

Figure 78. 4:2:2 Conversion Functional Model



4.3.17 2D Edge Enhancer

The edge enhancer module operates on the luminance (Y data) component of images to improve the image quality. Edges in input images are detected by a 2D high-pass filter, and its sharpness is increased by the value from a non-linear table. A block diagram of the luminance non-linear edge enhancer is shown in Figure 79. Entry for the non-linear table is 10-bit and the output is in signed 9-bit.

In the edge enhancer, the linear filter with programmable coefficient is applied to the Y input. Here, M is 5x5 matrix with programmable coefficients.

$$HPF(h,v) = \left(\sum_{j=-2}^{2} \sum_{i=-2}^{2} M_{i,j} Y(h+i, v+j) \right) >> shf_{HPF},$$

$$M = \begin{pmatrix} M_{2,2} & M_{1,2} & M_{0,2} & M_{1,2} & M_{2,2} \\ M_{2,1} & M_{1,1} & M_{0,1} & M_{1,1} & M_{2,1} \\ M_{2,0} & M_{1,0} & M_{0,0} & M_{1,0} & M_{2.0} \\ M_{2,1} & M_{1,1} & M_{0,1} & M_{1,1} & M_{2,1} \\ M_{2,2} & M_{1,2} & M_{0,2} & M_{1,2} & M_{2,2} \end{pmatrix}$$

The HPF value is shrunk by a threshold value (u6) specified by a register, and clipped to signed 10 bits to get the index for the LUT.

$$index = clip\left(shrink\left(HPF, threshold_{HPF}\right), -512, 511\right)$$

$$shrink(x, threshold) = \begin{cases} x + threshold & x < -threshold \\ 0 & -threshold \le x \le threshold \\ x - threshold & threshold < x \end{cases}$$

$$clip(x, limit_{LOW}, limit_{HIGH}) = \begin{cases} -limit_{LOW} & x < -limit_{LOW} \\ x & -limit_{LOW} \le x \le limit_{HIGH} \\ limit_{HIGH} & limit_{HIGH} < x \end{cases}$$

The edge-enhancement intensity is looked up from the LUT.

$E_{int} = LUT[index]$

The mapping to the memory is shown in Table 42.

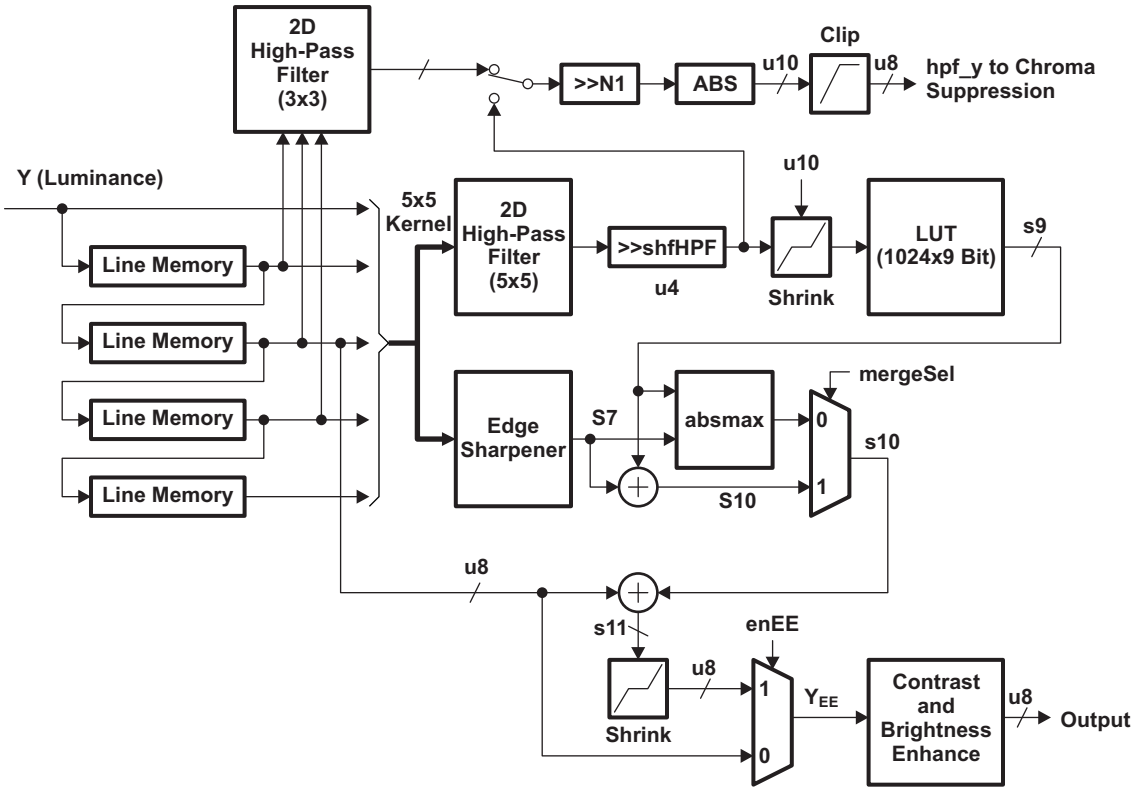
Table 42. Edge Enhancer LUT Mapping

Address (32-Bit Word Address)	Bit Position	LUT Index
0x00000h	8 .. 0	0
	17 ..9	1
0x00001h	8 .. 0	2
	17 .. 9	3
0x00002h	8 .. 0	4
	17 .. 9	5
0x00003h	8 .. 0	6
	17 .. 9	7
. . .	. . .	. . .
0x000FFh	8 .. 0	510
	17 .. 9	511
0x00100h	8 .. 0	-512
	17 .. 0	-511
0x00101h	8 .. 0	-510
	17 .. 9	-509
. . .	. . .	. . .
0x001FD	8 .. 0	-6
	17 .. 9	-5
0x001FE	8 .. 0	-4
	17 .. 9	-3
0x001FFh	8 .. 0	-2
	17 .. 9	-1

Table 43. LUT Memory Regions for Edge Enhancement Module

Memory Region	Address Range	Description
IPIPE_YEE_TB	0x01C78800 – 0x01C78FFF	IPIPE Edge Enhancement LUT

Figure 79. 2D Edge Enhancer Block Diagram



The edge sharpener module enhances edge clarity without producing Halo artifact. In this module, edge intensity is derived by the following 2D linear filter with fixed coefficients.

$$S_{i,j} = \begin{pmatrix} 0 & -1 & -2 & -1 & 0 \\ -1 & 0 & 2 & 0 & -1 \\ -2 & 2 & 8 & 2 & -2 \\ -1 & 0 & 2 & 0 & -1 \\ 0 & -1 & -2 & -1 & 0 \end{pmatrix}$$

$$sharpness(h,v) = clip\left(shrink\left(g \sum_{j=-2}^{2} \sum_{i=-2}^{2} S_{i,j} Y(h+i, v+j), -threshold_{LOW}, threshold_{LOW} \right) >> 6, threshold_{HIGH} \right)$$

The gain (g) and threshold values for the shrink/clip function (thresholdLOW, thresholdHIGH) are determined by register values. The bit width of g and $threshold_{HIGH}$ is in u6, and $threshold_{LOW}$ is in u6.6.

This edge intensity is then clipped by a threshold value.

$$S_{int} = \begin{cases} clip(sharpness, grad) & Halo\ reduction\ on \\ sharpness & Halo\ reduction\ off \end{cases}$$

The threshold value (grad) is a function of the activity around the target pixel, which is derived from gradient values.

Capping with gradient value prevents overly enhancing edges, and suppresses halo artifacts around edges. The output from EdgeEnhancer and EdgeSharpner are merged with the following function.

$$E_{merge} = \begin{cases} E_{int} + S_{int} & mergedsel = 1 \\ abs\,max\left(E_{int}, S_{int}\right) & mergedsel = 0 \end{cases}$$

$$abs\,max\left(x, y\right) = \begin{cases} x & abs\left(y\right) \le abs\left(x\right) \\ y & otherwise \end{cases}.$$

The E_{merge} value is added to the Y input value to make the final output.

For the chroma suppression, another 2D high pass filter (HPF) is implemented. One of the following four coefficient sets is selectable.

$$\begin{pmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{pmatrix}, \begin{pmatrix} 0 & 0 & 0 \\ 1 & -2 & 1 \\ 0 & 0 & 0 \end{pmatrix}, \begin{pmatrix} 0 & 1 & 0 \\ 0 & -2 & 0 \\ 0 & 1 & 0 \end{pmatrix}, or \begin{pmatrix} 0 & 1 & 0 \\ 1 & -4 & 1 \\ 0 & 1 & 0 \end{pmatrix}$$

At the end of the edge enhancer process, brightness and contrast adjust is applied to the Y signal. The process is described by the equation:

$$Y_{ctr\_brt} = clip8\left(clip8\left(\left(Y_{EE} \times CTR\right) \gg 4\right) + BRT\right)$$

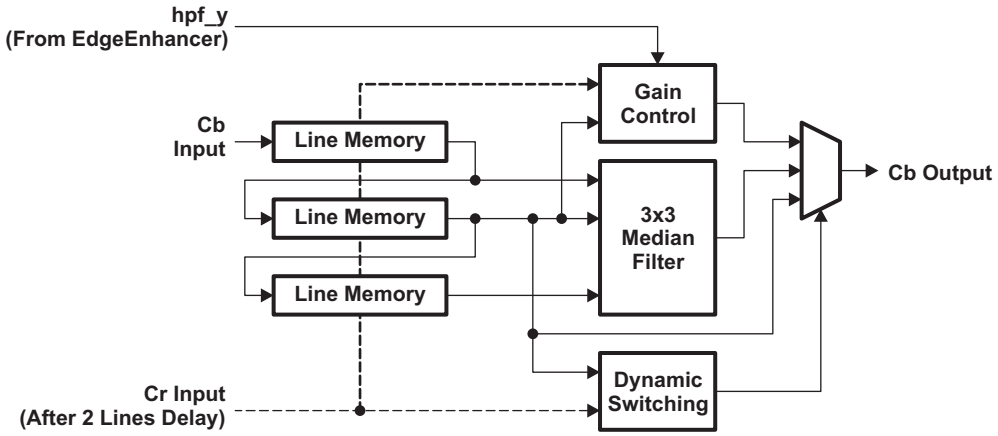
$$clip8\left(x\right) = \begin{cases} x & x \le 255 \\ 255 & 255 < x \end{cases}$$

Here, YEE is the output of the edge enhancer, CTR is a u4.4 contrast enhancement factor (YUV_ADJ[CTR]), BRT is a u8 brightness enhancement factor (YUV_ADJ[BRT]), and Y_{CTR_BRT} is the output as shown in Figure 79.

4.3.18 Chroma Artifact Reduction

Chroma artifact reduction (CAR) reduces color artifacts at the edges caused by CFAI or other filters. CAR has two methods: 3x3 median filter, and chroma gain control, for this purpose. Also, dynamic switching between these two methods is available to fully utilize the best performance of each method.

Figure 80. CAR Block Diagram (Cb)

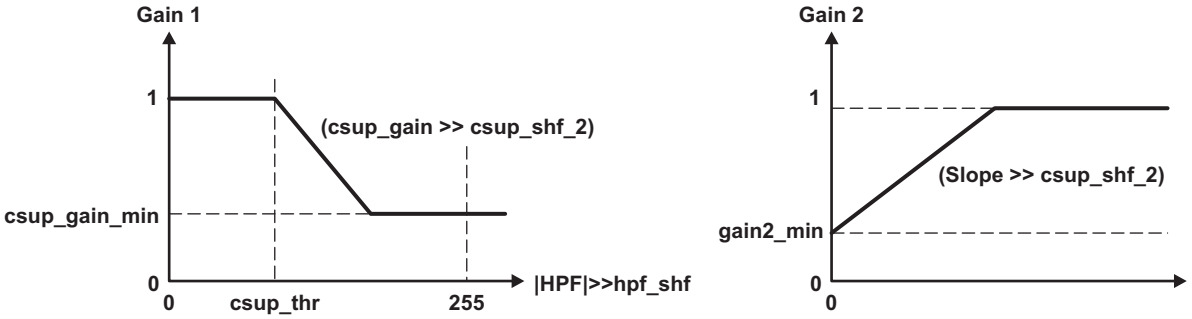


In gain control mode, the gain is calculated by the following function:

$$gain = \begin{cases} 1 & |HPF| < csup\_thr \\ gain1 \times gain2 & otherwise \end{cases}$$

The gain values (gain1 and gain2) are calculated by the function shown in Figure 81.

Figure 81. Gain1 and Gain2 in CAR



The dynamic switching between 3×3 median filter and gain control is done in the following way.

- If $cb^2 + cr^2$ < switch_limit, use median filter
- If (switch_coef)$(cb^2 + cr^2) < cb^2$, use gain control
- If both conditions are not met, do not apply any filter.

Here, switch_limit and switch_coef are determined by register values. The condition-1 limits the area where median filter is applied only on unsaturated area, in order to prevent desaturation of colors. The condition-2 limits gain control to be applied only to the area where the following condition is satisfied.

$$\left(\frac{cb}{\sqrt{cb^2 + cr^2}} \right) > \tan(\theta_{th}) \theta_{th} = \arctan\left(\sqrt{(switch\_coef)}\right)$$

With the appropriate θ_{th} value, this condition will selectively remove the purple artifact near the edges.

4.3.19 Chroma Gain Suppression

Chroma gain suppression (CGS) module controls the gain of Cb and Cr overly bright areas to reduce noises and remove color artifacts.

$$Cb_{output} = \frac{\left(total\_gain \times Cb_{input}\right)}{256}$$

$$Cr_{output} = \frac{\left(total\_gain \times Cr_{input}\right)}{256}$$

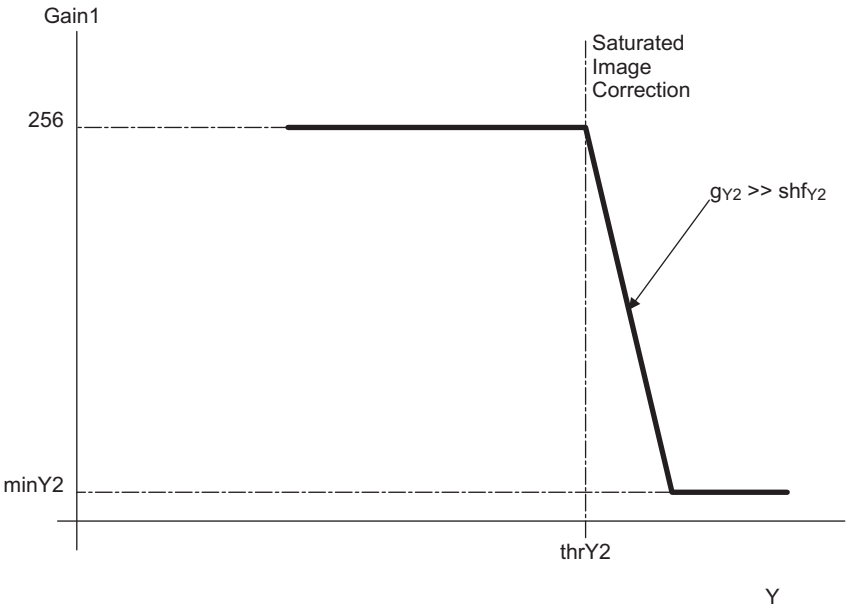
The gain value is determined by the following function:

$$gain_1 = \begin{cases} 256 & Y < thrY_2, \\ max\ (\ 256 - g_{Y2} \times (Y - thrY_2) >> shf_{Y2},\ min\ Y_2) & thrY_2 \le Y \end{cases}$$

$$total\_gain = gain_1$$

These functions are also illustrated in Figure 82.

Figure 82. Gain1 in CGS Block



4.3.20 Horizontal and Vertical Resizer Module

The resizer module is capable of re-scaling images into various sizes ranging from x1/16 scale-down to x16 scale-up. Also, resizer uses averaging method for down scaling. The data flow diagram of the Resize module is described in Figure 83. After the resizing process, the processed data are transferred to the SDRAM. Table 44 shows the format of YCbCr image data in SDRAM.

The scaling process is carried out using interpolation with 4-tap filter. The interpolation method is either 4-tap cubic convolution, or 3-tap linear filter + 2-tap linear interpolation depending on the user's choice. The range of resizing ratio is determined by two parameters HRSZ and VRSZ, which may be set independently. The resizing ratio of the output image equals to 256/ HRSZ for horizontal process and 256/VRSZ for vertical process. The upper and lower limits of HRSZ and VRSZ are 16 and 4096, which correspond to x16 scale-up and x1/16 scale-down, respectively. This module is capable of producing two output images simultaneously (resize-1 and resize-2). The sizes of output images are limited to below 2176 pixels/line for resize-1 and below 1088 for resize-2 in normal mode. In down-scale mode, the output with is limited to below 1088 pixel/line for resize-1, and below 544 pixel/line for resize-2.

The interpolation method used in resizing is either 4-tap cubic convolution or 2-tap linear interpolation for horizontal direction. Assume input signals are,

$i_0, i_1, i_2, ..., i_n, ...$

and the output signals are

$o_0, o_1, o_2, ..., o_m, ...,$

as shown in Figure 84. Then, the output pixel o_m is produced by the following equation

$$0_m = h(1+d)i_{n-1} + h(d)i_n + (d-1)i_{n-1} + h(d2)i_{n-2}$$

where

$$n = \text{floor}\left(\frac{(mN+p)}{256}\right)$$

$$d = \frac{(mN+p)}{256} - n$$

Here, h(x) is an interpolation function, floor(x) is the smallest integer which does not exceed x, and p/256 is the position (or phase) of the first output pixel. The interpolation function h(x) may be selected from cubic convolution of linear interpolation function shown in Figure 85. Both 4-tap cubic convolution and 2-tap linear interpolation can be used for vertical resizing.

Figure 83. Horizontal and Vertical Resize Module

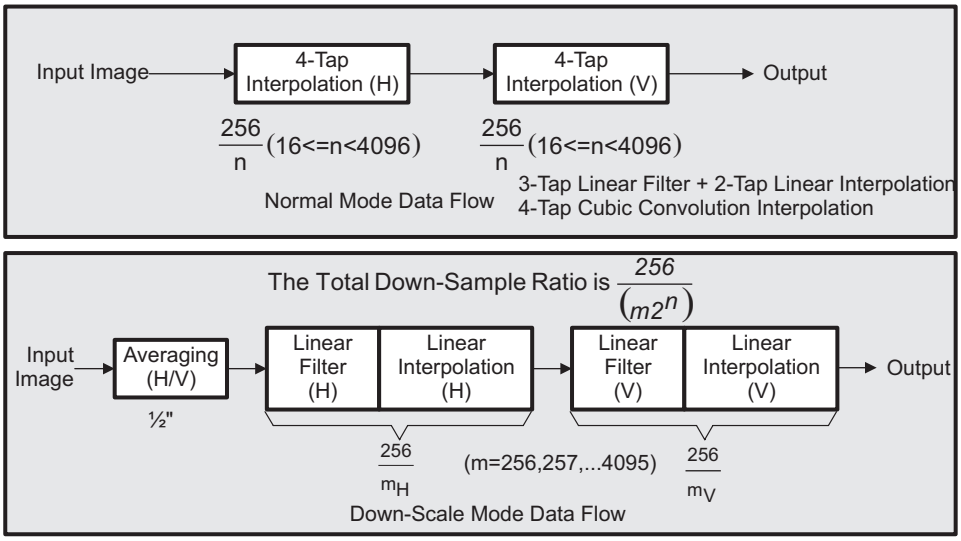
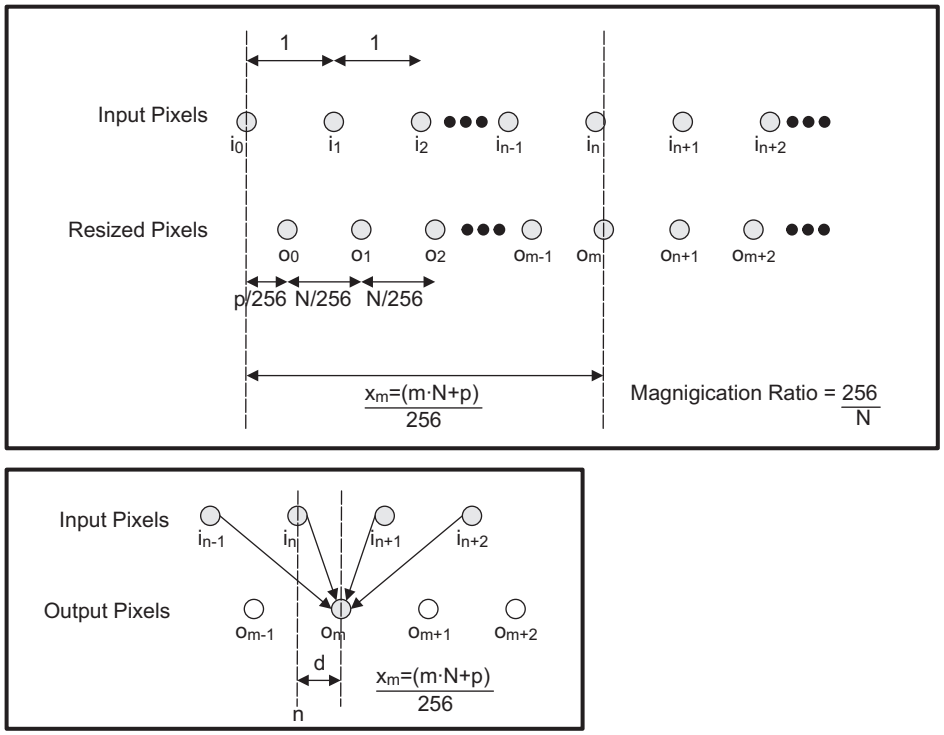


Figure 84. Interpolation Method



$$o_m = h(1+d)\cdot i_{n-1} + h(d)\cdot i_n + h(d-1)\cdot i_{n+1} + h(d-2)\cdot i_{n+2}$$

$$n = \text{floor}\left(\frac{mN+p}{256}\right) \qquad d = \frac{m\cdot N+p}{256} - n$$

Figure 85. Interpolation Function

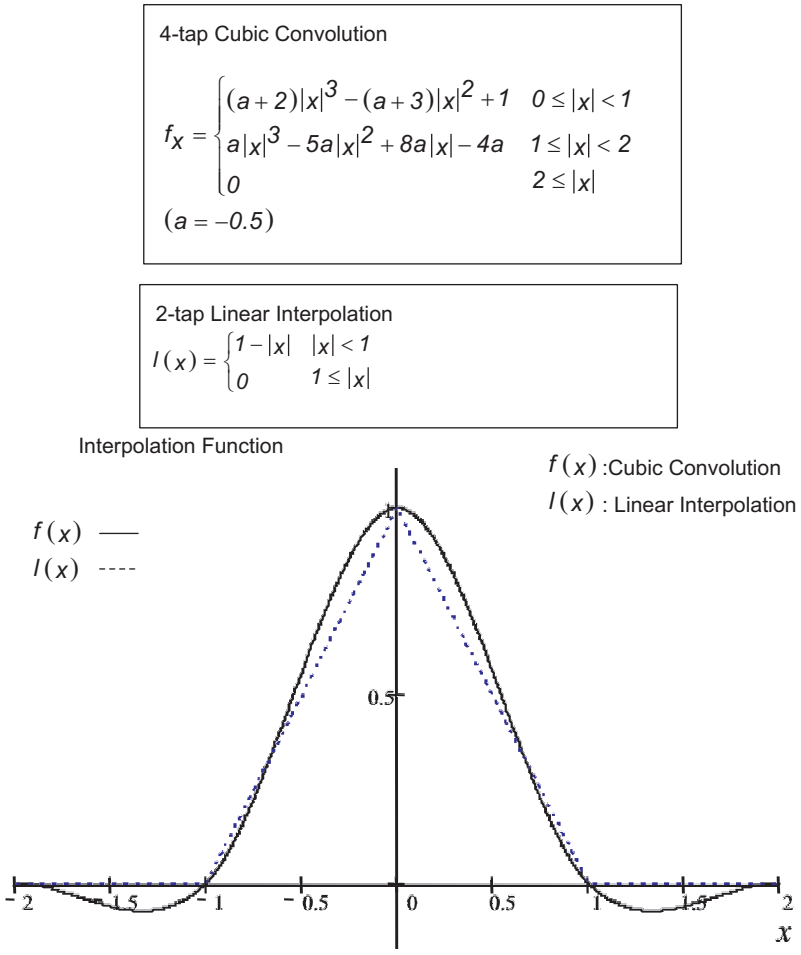


Table 44. YcbCr-422 Memory Format

Byte address	4n	4n+1	4n+2	4n+3
YCbCr data	Cb0	Y0	Cr0	Y1

4.3.20.1 Resizer Performance

Scale-up performance of the module depends on the frequency ratio between the pixel clock and SDRAM clock. When the pixel and SDRAM clock are 40MHz and 200MHz respectively, the total scale-up capability is approximately (200MHz/40MHz) x 2pallaral-output = x10-scale-up, i.e. x6-scale-up for image-a and x4-scale-up for image-b. More precise measure of the performance limit is as following. The vertical resize ratio for image-a and image-b must satisfy.

$$\text{(horizontal size of input image)} \times \left(\frac{\text{SDRAM clock speed}}{\text{pixel clock speed}} \right) > ha \times ra + hb \times rb + overhead$$

where,

$$ha = max\ (\text{width of input image} - a,\ \text{width of output image} - a)$$
$$hb = max\ (\text{width of input image} - b,\ \text{width of output image} - b)$$

$$ra = ceil \left(\frac{(\text{vertical resize ration of image} - a)}{2} \right)$$
$$rb = ceil \left(\frac{(\text{vertical resize ration of image} - b)}{2} \right)$$

$$overhead = 70 \times (ra + rb) \quad (1)$$

Here, max(a, b) is the larger of a and b, and ceil(x) is the smallest integer number that is equal to or greater than x. It is recommended that the right side value be smaller than the left side value with enough guard number.

Actual performance limit of resize output is also limited by the band-width of the attached SDRAM. Average output pixel per clock of each line must not exceed the band-width available to IPIPE module. For example, if the allowed band-width is 1 byte/clock, output pixel per clock in each line must be lower than 1 pixel per every 2 clocks with some margin for overhead. Therefore, allowed resize ratio in this case will be

image-a ratio <= x1, and image-b ratio <= x1

or

image-a ratio <= x2, and no image-b.

Bandwidth regulator (Section 4.3.20.9) must be configured to allow the required bandwidth.

4.3.20.2 Resizer Input

The resizer takes input from either IPIPE or IPIPEIF. The input is in the following formats.

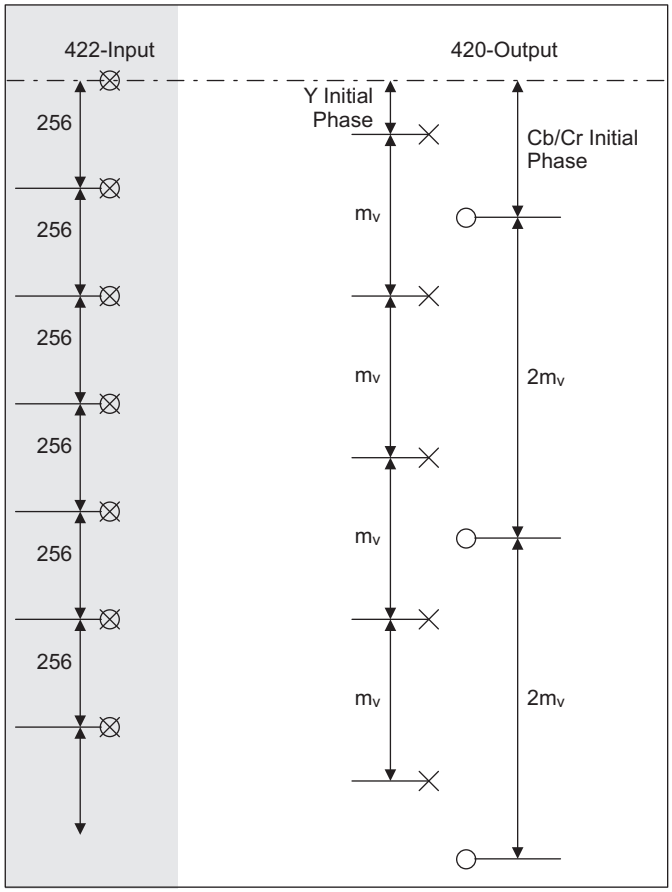
Table 45. Resizer Input Format

IPIPE Input	RAW	LOW	LOW	LOW	LOW	RAW11	RAW10	RAW9	RAW8
	YCbCr 16 bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	Y 8 bit	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
	CbCr 8 bit	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
IPIPE Input	RAW	RAW7	RAW6	RAW5	RAW4	RAW3	RAW2	RAW1	RAW0
	YCbCr 16 bit	Cb/Cr7	Cb/Cr6	Cb/Cr5	Cb/Cr4	Cb/Cr3	Cb/Cr2	Cb/Cr1	Cb/Cr0
	Y 8 bit	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
	CbCr 8 bit	Cb/Cr7	Cb/Cr6	Cb/Cr5	Cb/Cr4	Cb/Cr3	Cb/Cr2	Cb/Cr1	Cb/Cr0

4.3.20.3 4:2:2 to 4:2:0 Conversion

The resizer converts 422 format to 420. In this mode, vertical scaling ratio for Cb/Cr is doubled to halves the vertical sampling points. Y data and Cb/Cr data are written to separate memory spaces.

Figure 86. 4:2:2 to 4:2:0 Conversion



4.3.20.4 4:2:0 Input Mode

The resizer can process 420 image data. In each frame, either Y or Cb/Cr data can be processed at a time. In order to process full 420 image with Y and Cb/Cr, IPIPE needs to run twice.

Figure 87. 4:2:0 Y Processing

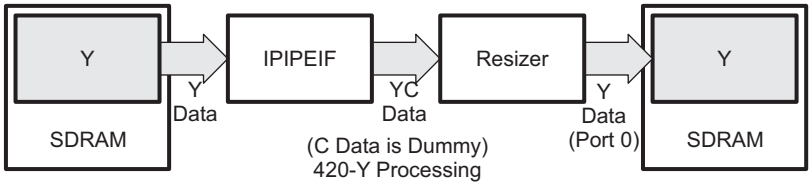
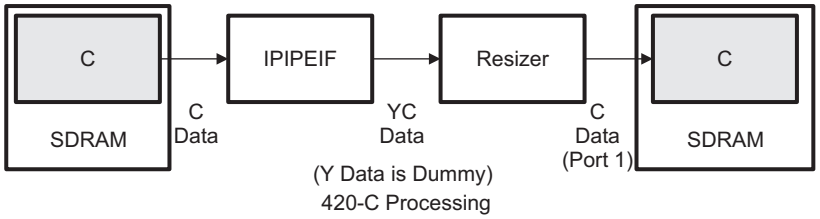


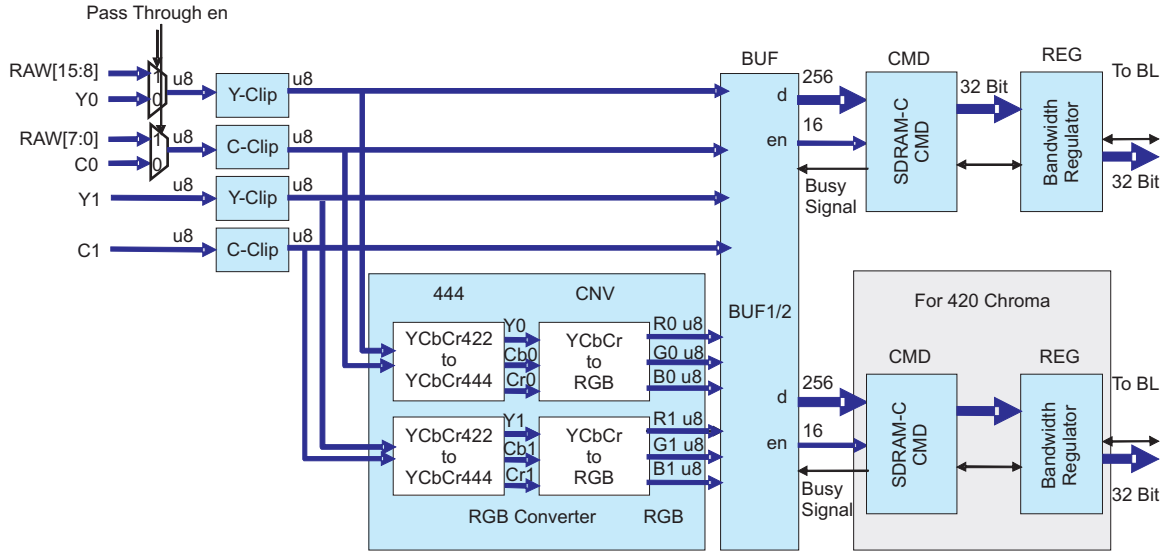
Figure 88. 4:2:0 C Processing



4.3.20.5 Output Interface

The block diagram of output interface module is shown in Figure 89. Y-Clip and C-Clip modules limit the range of image data to [ymin to ymax] or [cmin to cmax]. The values are specified in the register map. After completion the transfer of each frame, rsz_eof is sent to BufferLogic. This signal is issued at the same timing as rsz_int_dma interrupt.

Figure 89. Output Interface Block Diagram



4.3.20.6 RGB Converter

The IPIPE module supports output of RGB data to SDRAM. The YCbCr 4:2:2 data from the resizer module is first converted to YCbCr 4:4:4 data by linear interpolation. Since the pixels at the left and right edges are mirrored for the interpolation, two pixels at each edge are affected. To remove this effect, 2 pixels at each edge may be removed from the output. In this case, the horizontal size of the output image is 2 or 4 pixels smaller than specified in resizer register.

The YCbCr 4:4:4 data is converted to RGB using the following equation.

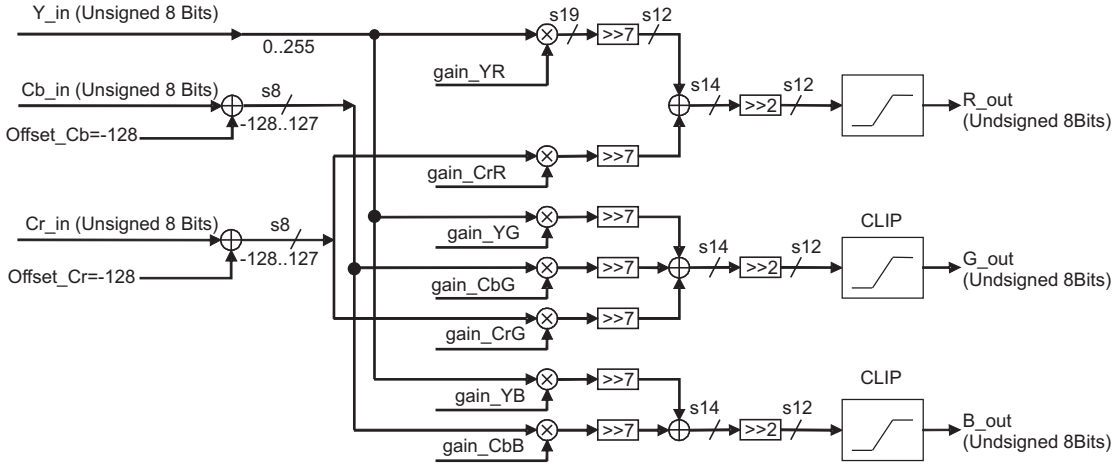
$$\begin{pmatrix} R \\ G \\ B \end{pmatrix} = \begin{pmatrix} 1 & 0 & 1.402 \\ 1 & -0.34414 & -0.71414 \\ 1 & 1.772 & 0 \end{pmatrix} \cdot \begin{pmatrix} Y \\ Cb-128 \\ Cr-128 \end{pmatrix}$$

This equation is realized in actual circuit using the following equations.

$$R = (512 \cdot Y/128 + 718 \cdot Cb'/128)/4$$
$$G = (512 \cdot Y/128 - 176 \cdot Cr'/128 - 366 \cdot Cb'/128)/4$$
$$B = (512 \cdot Y/128 + 907 \cdot Cr'/128)/4$$
$$Cb' = Cb - 128$$
$$Cr' = Cr - 128$$

The block diagram of RGB conversion is shown in Figure 90.

Figure 90. YCbCr to RGB Block Diagram



There are two RGB-output mode: 32-bit mode and 16-bit mode. In 32-bit mode, RGB data (8-bit each) and alpha (8-bit blending factor) are written to SDRAM. Alpha value is set through register. In 16-bit mode, R (5-bit), G (6-bit), and B (5-bit) are written.

Enabling of RGB conversion and 32-bit/16-bit selection may be independently specified to the Resize-A picture and Resize-B picture.

4.3.20.7 Resizer Output Data format

The data storage pattern in SDRAM for different resizer output formats is shown below.

4.3.20.7.1 422 Output Data

The 422 data from the resizer module are stored in the SDRAM in the following packing format.

Figure 91. 422 Data Packing

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Y1	Cr0	Y0	Cb0

4.3.20.7.2 420 Output Data

The 420 data from the resizer module are stored in the SDRAM in the following packing format.

Figure 92. 420-Y Data Packing

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Y3	Y2	Y1	Y0

Figure 93. 420-C Data Packing

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Cr1	Cb1	Cr0	Cb0

4.3.20.7.3 RAW Output Data

RAW data (Bayer data) are stored in the SDRAM in the following packing format.

Figure 94. RAW Data Packing

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Not used	RAW1	Not used	RAW0

4.3.20.7.4 RGB Ouput Data

RGB data are stored in the SDRAM in the following packing format.

Figure 95. RGB Data Packing (32-bit)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Alpha (blending factor)	Red	Green	Blue

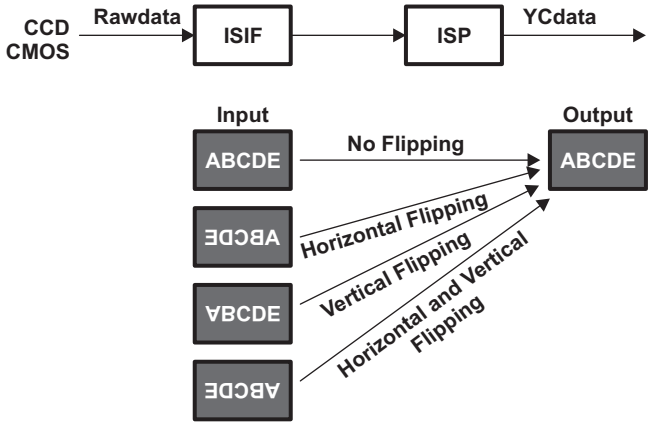
Figure 96. RGB Data Packing (16-bit)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Red-1	Green-1	Blue-1	Red-0	Green-0	Blue-0

4.3.20.8 Output Image Flipping

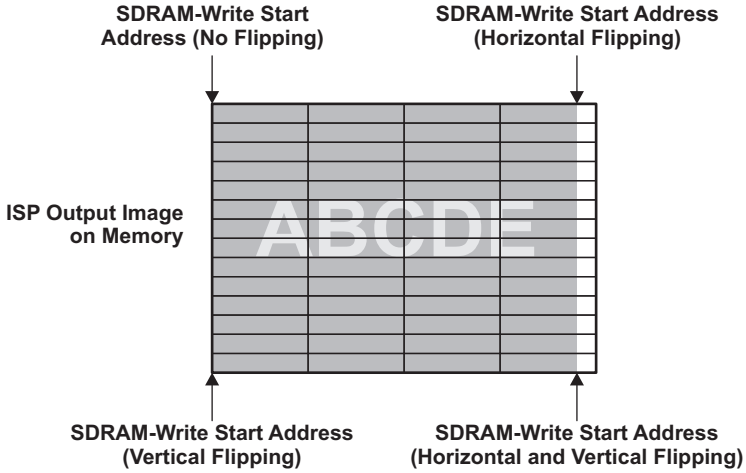
The flipping image function is implemented to support flipped raw data input. Horizontal, vertical and horizontal/vertical flipping modes are implemented as shown in Figure 97.

Figure 97. Data Flipping Mode



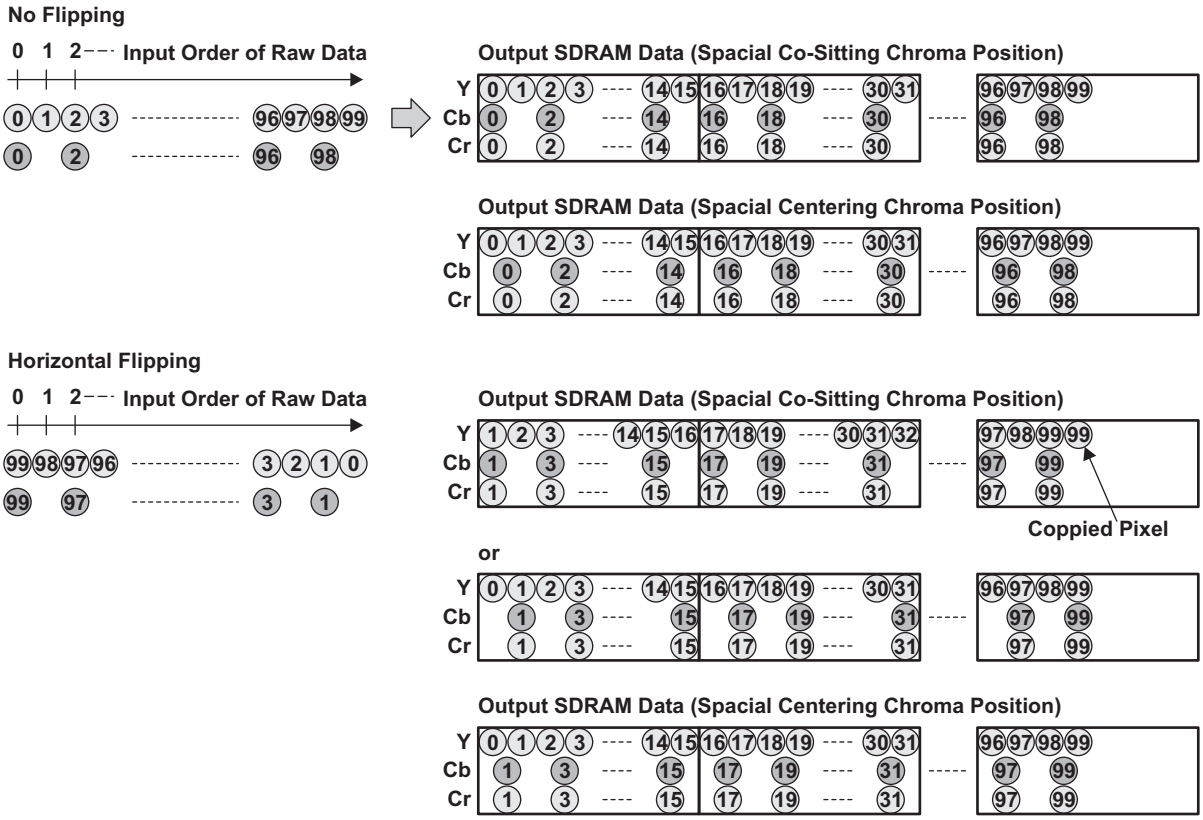
The SDRAM write-start-address is needed to be set at the register by ARM. The address at each flipping mode is illustrated in Figure 98.

Figure 98. Write Start Address at Each Flipping Mode



In the non on-the-fly operation mode, ISIF flips the data and write raw data in the SDRAM. IPIPE does not flip data in the mode. Therefore horizontal flipping mode does not support the frame division operation. Figure 99 illustrates output data format to SDRAM at no flipping and horizontal flipping modes.

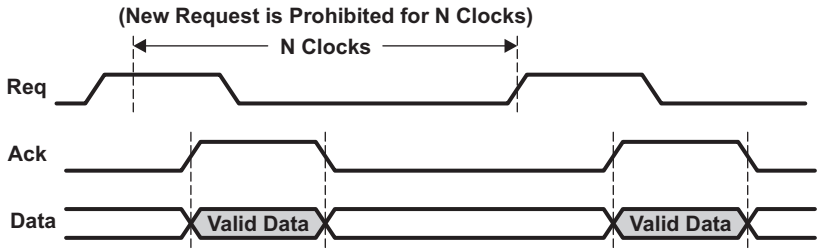
Figure 99. Output Data Format to SDRAM



4.3.20.9 Output Bandwidth Regulator

The bandwidth regulator module limits the maximum bandwidth used by IPIPE output. This module suppresses issuing of a new request for the desired period of time (N clocks) after each request. The period is specified by clock cycles through register values. N is between 0 and 255, and can be set independently for resize-A and resize-B. With a given N value, the maximum bandwidth used by IPIPE is 256/(N+1) bit/cycle.

Figure 100. SDRAM Access Request Prohibited Period



4.3.21 Histogram

Histogram and boxcar may not work at the same time, since the modules share one set of memories. The histogram module counts the number of pixels having a value in a region. Features of the histogram function are as follows:

- The data to be summed will be taken either from NF memory or from RGB2YCbCr module.
- When data are collected from NF memory, the sampled colors are R/G/B/Y. Y is derived in the following method. (HST_MUL_R, HST_MUL_GR, HST_MUL_GB, HST_MUL_B are in S4.4 format)
  Y=(HST_MUL_R*R+HST_MUL_GR*Gr+HST_MUL_GB*Gb+HST_MUL_B*B).
  For G histogram, either Gb, Gr, or (Gb+Gr)/2 is used
- When data are collected from RGB2YCbCr module, Cb is collected from (even, even) positions, Y from (odd, even) and (even, odd) positions and Cr from (odd, odd) positions.
- There are two banks of memory, and two sets of 512 x 20-bit memory are used for each bank.
- Two banks of memory sets are available. Tables are selected by HST_TBL.
- "The number of regions" x "the number of bins" <= 256
- The number of regions (areas) : 1, 2, 3, or 4
- The position and size of each region is specified by HST_n_HPS, HST_n_VPS, HST_n_VSZ, HST_n_HSZ (n = 0, 1, 2 or 3).
- Each region can be turned on/off counting.
- The regions have priority orders.
- Each region has its own start coordinate X/Y (12-bit) and horizontal/vertical sizes (12-bit)
- When regions are overlapped, value in the overlapped region is only accumulated in the region with the highest priority.
- The number of colors to be counted: 1, 2, 3, or 4
- Each color in all regions can be turned off counting.
- The value of each pixel is down-shifted before counting.
- The down-shift bit number: 0 ~ 11 bits
- When the value of a bin reaches to (2^{20} - 1), the value is saturated until the memory is cleared.
- The number of bins: 32, 64, 128, or 256

The histogram memory can be cleared at the VD signal. When memory is cleared, the first line of each frame can not be sampled by histogram if the width of the frame is larger than 512. If the width of the frame is smaller than 512, the first cell (512/width) lines can not be collected, where cell(x) is the smallest integer value above x. If the clearing function is not enabled, the histogram bins are accumulated over the previous values.

The histogram has two banks of memories, and they can be switched alternatively. The mapping of histogram memory is shown in Table 46.

Table 46. Histogram Memory Mapping

Memory #	**Address**	**Histogram table**	**Table Address**
	(32 bit word)		
Histogram memory #0	0x0000h	Histogram 0 (Bank 0)	Table address = 0x0000h
Histogram memory #0	0x0001h	Histogram 0 (Bank 0)	Table address = 0x0001h
Histogram memory #0	0x0002h	Histogram 0 (Bank 0)	Table address = 0x0002h
.	.	.	.
.	.	.	.
.	.	.	.
Histogram memory #0	0x01FEh	Histogram 0 (Bank 0)	Table address = 0x01FEh
Histogram memory #0	0x01FFh	Histogram 0 (Bank 0)	Table address = 0x01FFh
Memory #	**Address (byte)**	**Histogram table**	**Table Address**
Histogram memory #1	0x0000h	Histogram 1 (Bank 0)	Table address = 0x0000h
Histogram memory #1	0x0001h	Histogram 1 (Bank 0)	Table address = 0x0001h
Histogram memory #1	0x0002h	Histogram 1 (Bank 0)	Table address = 0x0002h
.	.	.	.
.	.	.	.
.	.	.	.
Histogram memory #1	0x01FEh	Histogram 1 (Bank 0)	Table address = 0x01FEh
Histogram memory #1	0x01FFh	Histogram 1 (Bank 0)	Table address = 0x01FFh
Memory #	**Address (byte)**	**Histogram table**	**Table Address**
Histogram memory #2	0x0000h	Histogram 0 (Bank 1)	Table address = 0x0000h
Histogram memory #2	0x0001h	Histogram 0 (Bank 1)	Table address = 0x0001h
Histogram memory #2	0x0002h	Histogram 0 (Bank 1)	Table address = 0x0002h
.	.	.	.
.	.	.	.
.	.	.	.
Histogram memory #2	0x01FEh	Histogram 0 (Bank 1)	Table address = 0x01FEh
Histogram memory #2	0x01FFh	Histogram 0 (Bank 1)	Table address = 0x01FFh
Memory #	Address (byte)	Histogram table	Table Address
Histogram memory #3	0x0000h	Histogram 1 (Bank 1)	Table address = 0x0000h
Histogram memory #3	0x0001h	Histogram 1 (Bank 1)	Table address = 0x0001h
Histogram memory #3	0x0002h	Histogram 1 (Bank 1)	Table address = 0x0002h
.	.	.	.
.	.	.	.
.	.	.	.
Histogram memory #3	0x01FEh	Histogram 1 (Bank 1)	Table address = 0x01FEh
Histogram memory #3	0x01FFh	Histogram 1 (Bank 1)	Table address = 0x01FFh

The memory map for histogram changes according to HST_PARA[BIN], (see Figure 101).

Figure 101. Histogram Memory Map Changes

(1) HST_PARA[BIN] = 0 (The Number of Bins is 32)

Histogram 0 Table Address Format									
Bit	8	7	6	5	4	3	2	1	0
Description	0	Region (0,1,2,3)		Color 0:R, 1:B	BIN Number (0-31)				

Histogram 1 Table Address Format									
Bit	8	7	6	5	4	3	2	1	0
Description	0	Region (0,1,2,3)		Color 0:G, 1:Y	BIN Number (0-31)				

(2) HST_PARA[BIN] = 1 (The Number of Bins is 64)

Histogram 0 Table Address Format									
Bit	8	7	6	5	4	3	2	1	0
Description	Region (0,1,2,3)		Color 0:R, 1:B	BIN Number (0-63)					

Histogram 1 Table Address Format									
Bit	8	7	6	5	4	3	2	1	0
Description	Region (0,1,2,3)		Color 0:G, 1:Y	BIN Number (0-63)					

(3) HST_PARA[BIN] = 2 (The Number of Bins is 128)

Histogram 0 Table Address Format									
Bit	8	7	6	5	4	3	2	1	0
Description	Region (0,1)	Color 0:R, 1:B	BIN Number (0-127)						

Histogram 1 Table Address Format									
Bit	8	7	6	5	4	3	2	1	0
Description	Region (0,1)	Color 0:G, 1:Y	BIN Number (0-127)						

(4) HST_PARA[BIN] = 3 (The Number of Bins is 255)

Histogram 0 Table Address Format									
Bit	8	7	6	5	4	3	2	1	0
Description	Color 0:R, 1:B	BIN Number (0-255)							

Histogram 1 Table Address Format									
Bit	8	7	6	5	4	3	2	1	0
Description	Color 0:G, 1:Y	BIN Number (0-255)							

Table 47. Histogram Memory Regions (Bins)

Memory Region	Address Range	Description
IPIPE_HST_TB0	0x01C72000 – 0x01C727FF	IPIPE Histogram Memory #0
IPIPE_HST_TB1	0x01C72800 – 0x01C72FFF	IPIPE Histogram Memory #1
IPIPE_HST_TB2	0x01C73000 – 0x01C737FF	IPIPE Histogram Memory #2
IPIPE_HST_TB3	0x01C73800 – 0x01C73FFF	IPIPE Histogram Memory #3

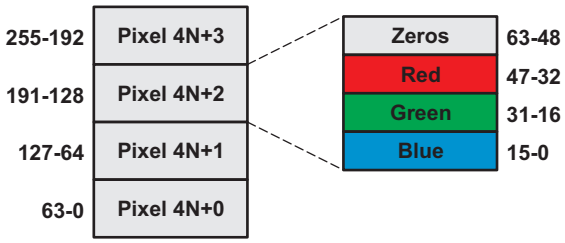
4.3.22 Boxcar

The histogram and boxcar modules may not work at the same time, since they share one set of memories.

The boxcar module generates a boxcar by taking mosaic image data and averaging the red, green, and blue pixels in an 8×8 or 16×16×16 block to produce one red, green, and blue output as shown in Figure 103 and in Figure 104.

The result from this operation is a full color image with (1/64) or (1/256) area of the original image. The maximum input horizontal width is 8190 pixels wide when 16x16 block is used. If 8×8 block is used, it is 4096 bits. Also, the image size (width and height) must be a multiple of 16 for 16×16 block, and a multiple of 8 for 8×8 block. The boxcar operation works on up to 12-bit Bayer data and output 16-bit data. The output data are 48-bit RGB data for each 8×8 or 16×16 block. The 48-bit data is aligned in 64-bit format in SDRAM as shown in Figure 102.

Figure 102. Boxcar Data Packing in SDRAM



The first address of SDRAM access is specified by IPIPE_BOX_SDR_SAD_H and IPIPE_BOX_SDR_SAD_L. The output data are written to SDRAM continuously line by line; there are no address offsets between lines. After completion of image transfer of each frame, ipipe_eof signal is sent to BufferLogic. This signal is issued at the same timing as ipipe_int_dma.

$$R_{output_{i,j}} = \left(\sum_{y=8i}^{8i+7} \sum_{x=8j}^{8j+7} R_{y,x} \right) \gg shf$$

$$B_{output_{i,j}} = \left(\sum_{y=8i}^{8i+7} \sum_{x=8j}^{8j+7} B_{y,x} \right) \gg shf$$

$$G_{output_{i,j}} = \left(\frac{\left(\sum_{y=8i}^{8i+7} \sum_{x=8j}^{8j+7} Gb_{y,x} \right)}{2} + \frac{\left(\sum_{y=8i}^{8i+7} \sum_{x=8j}^{8j+7} Gr_{y,x} \right)}{2} \right) \gg shf$$

The right-shift value is specified by a register IPIPE_BOX_SHF, which has the range of 0 to 4. (The shift down is to fit 20-bit accumulated value into 16-bit output.) For green signal processing, divide-by-two operation rounds off the LSB.

The boxcar module shares memories with histogram module; therefore they can not run simultaneously. The boxcar can run in parallel with other parts of IPIPE other than the histogram.

Figure 103. Boxcar Operation (8 × 8 block)

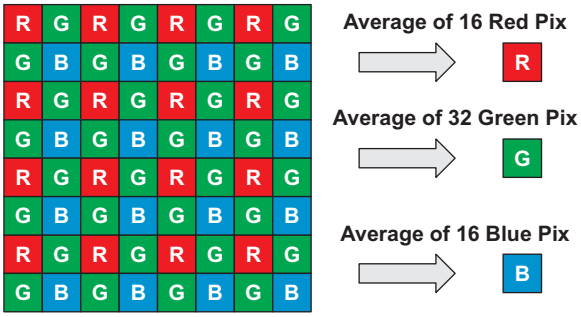
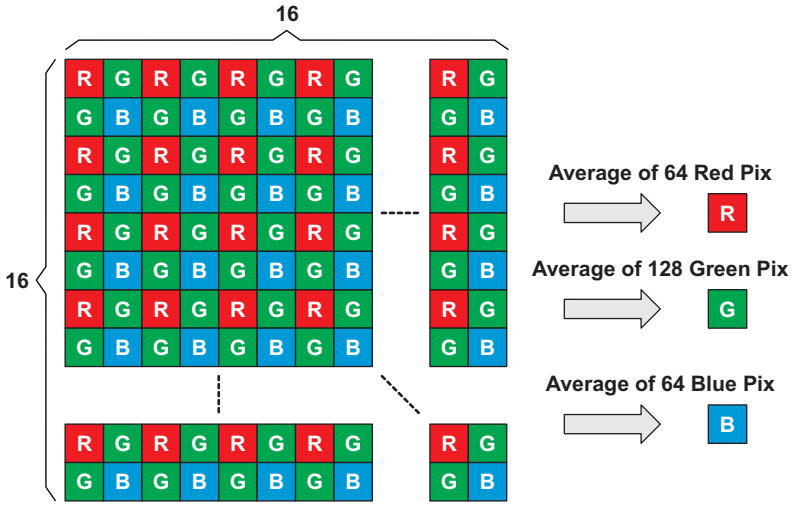


Figure 104. Boxcar Operation Figure (16 × 16 block)



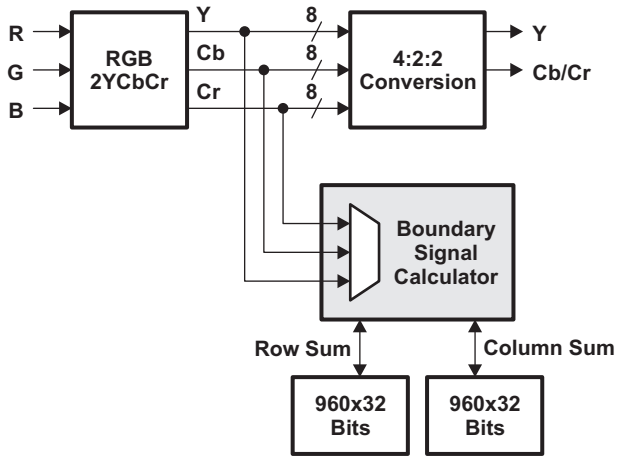
4.3.23 Boundary Signal Calculator

The boundary signal calculator generates the row summations and column summations from YCbCr 4:4:4 data. Figure 105 shows the block diagram of boundary signal calculator.

Two kinds of vectors are generated: the vector of sums of row pixels and the vector of sums of column pixels. Both vectors are from one of Y, Cb or Cr data.

For both row and column sums, up to four vectors can be generated. Both row and column sums are 16-bit values which are stored to 960x32-bit memories, respectively. The maximum number of sums is 1920 for both row and column. If successive frames are to be processed, more than 16 lines between the frames cannot be used for calculation.

Figure 105. Boundary Signal Calculator Block Diagram



The following parameters are required for row sum vectors:

- The position of the first pixel to be summed (ROW_HPOS, ROW_VPOS)
- The spacing between adjacent sampling pixels (ROW_HSKIP, ROW_VSKIP)
- The number of sampled pixels (ROW_HNUM, ROW_VNUM)
- The number of row sum vectors (ROW_VCT). The down shift value of input data (ROW_SHF)
- These parameters are described in Figure 106. With these parameters, each vector is calculated in the following way.

$$d'_{h,v} = d_{h,v} >> ROW\_SHF$$

$$rowsum'_{n,v} = \sum_{i=0}^{i<ROW\_HNUM+1} d'_{ROW\_HPOS+n\cdot(ROWLH+1)+i\cdot(ROW\_HSKIP+1),\,ROW\_VPOS+v\cdot(ROW\_VSKIP+1)}$$

$$ROWLV+1 = (ROW\_VSKIP+1)\cdot(ROW\_VNUM+1)$$

$$ROWLH+1 = (ROW\_HSKIP+1)\cdot(ROW\_HNUM+1)$$

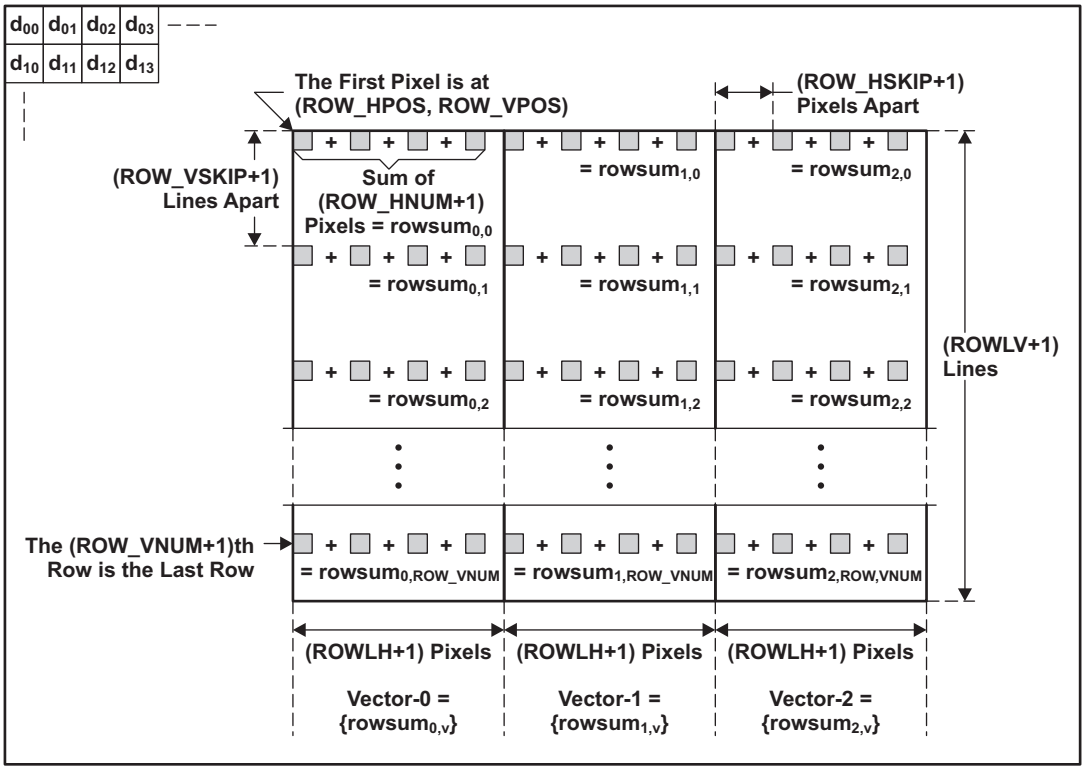
$$rowsum_{n,v} = \begin{cases} rowsum'_{n,v} & rowsum'_{n,v} < 2^{16} \\ 2^{16}-1 & \text{otherwise} \end{cases}$$

$$(0 \le n < ROW\_VCT, 0 \le v < ROW\_VNUM)$$

The number of row sums cannot exceed 1920. ROW_VCT and ROW_VNUM should be set accordingly.

$$(ROW\_VCT+1)\times(ROW\_VNUM+1) \le 1920$$

Figure 106. Row Sum Vector Calculation



The following parameters are required for column sum vectors:

- The position of the first pixel to be summed (COL_HPOS, COL_VPOS)
- The spacing between adjacent sampling pixels (COL_HSKIP, COL_VSKIP)
- The number of sampled pixels (COL_HNUM, COL_VNUM)
- The number of column sum vectors (COL_VCT)
- The down shift value of input data (COL_SHF)

These parameters are described in Figure 107. Each vector is calculated in the following way.

$$d''_{h,V} = d_{h,V} >> COL\_SHF$$

$$colsum'_{n,h} = \sum_{i=0}^{i<COL\_VNUM} d''_{COL\_HPOS+h\cdot(COL\_HSKIP+1),COL\_VPOS+n\cdot(COLLV+1)+i\cdot(COL\_VSKIP+1)}$$

$$COLLV+1 = (COL\_VSKIP+1)\cdot(COL\_VNUM+1)$$

$$COLLH+1 = (COL\_HSKIP+1)\cdot(COL\_HNUM+1)$$

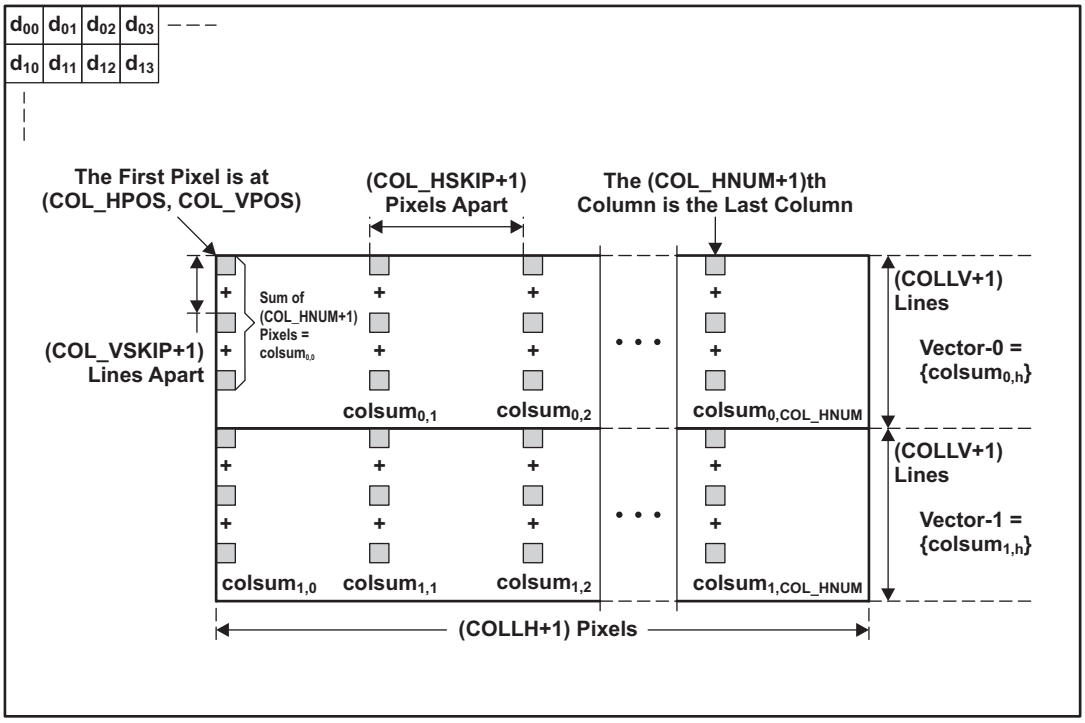
$$colsum_{n,h} = \begin{cases} colsum_{n,h}' & colsum_{n,h}' < 2^{16} \\ 2^{16}-1 & \text{otherwise} \end{cases}$$

$$(0 \le n < COL\_CVT, 0 \le h < COL\_HNUM)$$

The number of column sums cannot exceed 1920. COL_VCT and COL_HNUM should be set accordingly.

$$(COL\_VCT+1)\times(COL\_HNUM+1) \le 1920$$

Figure 107. Column Sum Vector Calculation



The mapping of the BSC memory is shown in Table 48 and Table 49.

Table 48. Mapping of ROWSUM Vector to BSC Memory

Address	Bit position	Vector number	Vector Element
(32 bit word address)			
0x00000h	15..0	0	ROWSUM0
	31..16	0	ROWSUM1
0x00001h	15..0	0	ROWSUM2
	31..16	0	ROWSUM3
0x00002h	15..0	0	ROWSUM4
	31..16	0	ROWSUM5
.	.	.	.
.	.	.	.
ROW_VNUM/2	15..0	1	ROWSUM0
	31..16	1	ROWSUM1
ROW_VNUM/2+1	15..0	1	ROWSUM2
	31..16	1	ROWSUM3
.	.	.	.
.	.	.	.
2 x ROW_VNUM/2	15..0	2	ROWSUM0
	31..16	2	ROWSUM1
2 x ROW_VNUM/2+1	15..0	2	ROWSUM2
	31..16	2	ROWSUM3
.	.	.	.
.	.	.	.

Table 49. Mapping of COLMSUM Vector to BSC Memory

Address	Bit position	Vector number	Vector Element
(32 bit word address)			
0x00000h	15..0	0	COLSUM0
	31..16	0	COLSUM1
0x00001h	15..0	0	COLSUM2
	31..16	0	COLSUM3
0x00002h	15..0	0	COLSUM4
	31..16	0	COLSUM5
.	.	.	.
.	.	.	.
COL_HNUM/2	15..0	1	COLSUM0
	31..16	1	COLSUM1
COL_HNUM /2+1	15..0	1	COLSUM2
	31..16	1	COLSUM3
.	.	.	.
.	.	.	.
2 x COL_HNUM /2	15..0	2	COLSUM0
	31..16	2	COLSUM1
2 x COL_HNUM /2+1	15..0	2	COLSUM2
	31..16	2	COLSUM3
.	.	.	.
.	.	.	.

Table 50. BSC Output of Memory Regions

Memory Region	Address Range	Description
IPIPE_BSC_TB0	0x01C74000 – 0x01C75FFF	IPIPE BSC Accumulation Memory #0
IPIPE_BSC_TB1	0x01C76000 – 0x01C7FFFF	IPIPE BSC Accumulation Memory #1

4.4 Statistics Collection - Hardware 3A (H3A)

The H3A module is designed to support the control loops for auto focus, auto white balance, and auto exposure by collecting metrics about the imaging/video data. The metrics are to adjust the various parameters for processing the imaging/video data. There are two main blocks in the H3A module:

- Auto focus engine (AF)
- Auto exposure and auto white balance engine (AE/AWB)

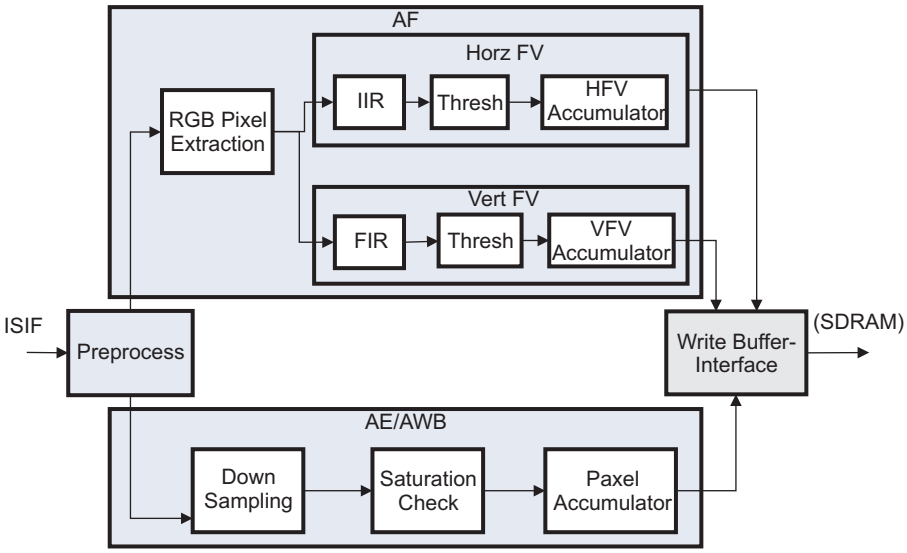
The AF engine extracts and filters the red, green, and blue data from the input image/video data and provides either the accumulation or peaks of the data in a specified region. The specified region is a two-dimensional block of data and is referred to as a paxel for the case of AF.

The AE/AWB engine accumulates the values and checks for saturated values in a sub-sampling of the video data. In the case of the AE/AWB, the two-dimensional block of data is referred to as a window. Thus, other than referring to them by different names, a paxel and a window are essentially the same thing. However the number, dimensions, and starting position of the AF paxels and the AE/AWB windows are separately programmable.

4.4.1 H3A Functional Description

As shown in Figure 108 the H3A module has two data paths through the design and a single data interface out of the module. After the preprocessing step, the data passes through two separate engines: one for auto focus and one for auto exposure and auto white balance. Note that the AF paxel and AE/AWB window number, dimensions, and starting coordinates are independent. Intermediate results of the AF and AE/AWB computation are stored in the shared memory accumulator control block. The final results are written out (as per section 2.2.4) to either internal buffer memory or external SDRAM through buffer logic and system SCR.

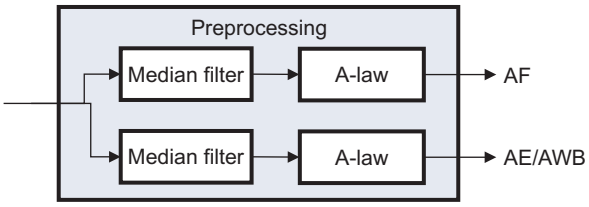
Figure 108. H3A High-Level Block Diagram



4.4.2 H3A Preprocessing

Prior to directing the image/video data to the AF and AE/AWB data paths, the H3A module has the task of preprocessing the input data. The necessary preprocessing steps include a horizontal median filtering step and a 10-bit to 8-bit A-law compression step. Figure 109 shows the preprocessing done for the AF and AE/AWB blocks. The median filter and the A-law can each be enabled/disabled via register settings.

Figure 109. Preprocessing Stage Prior to the AF and AE/AWB



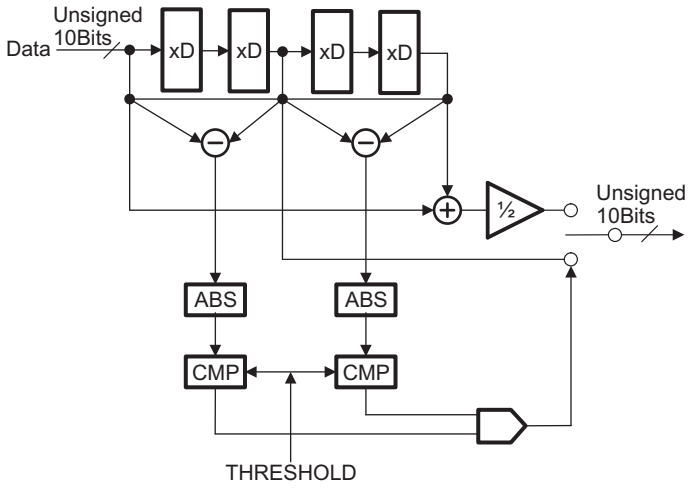
The horizontal median filter, shown in Figure 110, calculates the absolute difference between the current pixel (i) and pixel (i-2) and between the current pixel (i) and pixel (i+2). If the absolute difference exceeds a threshold, and the sign of the differences is the same, then the average of pixel (i-2) and pixel (i+2) replaces pixel (i). The horizontal median filter's threshold is configurable and the horizontal median filter can either be enabled or disabled.

The A-law conversion routine compresses the 10-bit value to an 8-bit value. In the case of the A-law table being enabled, the output is still 10-bits with the upper two bits filled with a 0.

Figure 110. Horizontal Median Filter Implementation

Function Model:

```
for (i=0, i< length_pixel, i++){
        sub1 = input_data(i) - input_data(i-2);
        sub2 = input_data(i) - input_data(i+2);
if ((abs(sub1) > THRESHOLD && abs(sub2) > THRESHOLD) &&
((sub1<0 && sub2<0) || (sub1>0 && sub2>0)))
        output_data(i) = (input_data(i-2) + input_data(i+2))/2;
else
        output_data(i) = input_data(i);
}
```



4.4.3 Auto Focus Engine

The auto focus engine works by extracting each green (Gr or Gb) pixel from the video stream and subtracts a fixed offset of 128 or 512 (depending of whether the A-law is enabled or disabled) from the pixel value. The offset value is then passed through an IIR filter and the absolute value of the filter output is the focus value or FV. Both FV and FV^2 are produced. The FV and FV^2 values can either be accumulated or the maximum for each line/column can be accumulated. The maximum FV or FV^2 of each line in a Paxel is acquired if FV mode is set to peak mode.

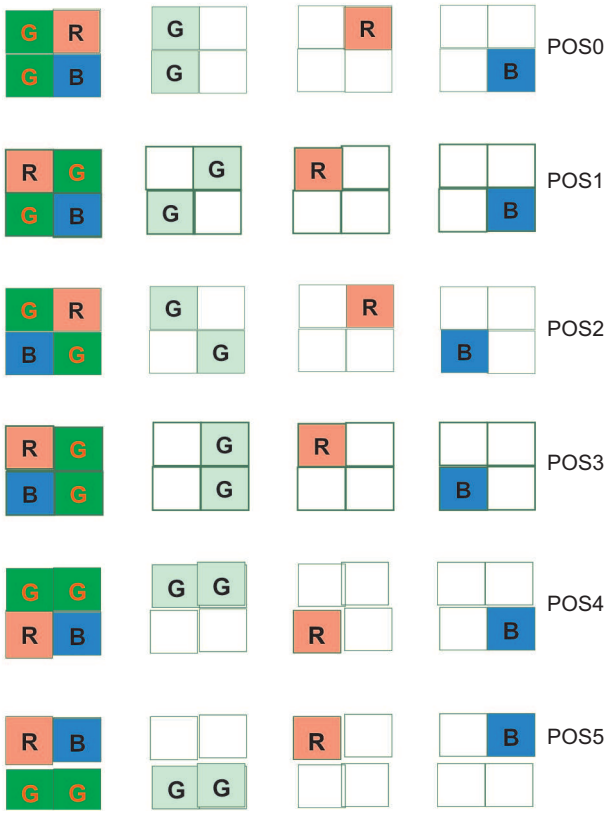
4.4.3.1 Paxel Extraction

The paxel starting coordinate (PAXSH, PAXSV) specifies the starting point of paxel grid, with respect to first pixel of input image frame.

The paxel starting coordinate also indicates which color pixels are extracted if the Vertical Focus is enabled. Normally either Gr or Gb are used for AF, but hardware does not really care if it's red, green, or blue. If vertical focus is not enabled, then the red, green, and blue pixel extraction is controlled by a register setting that specifies which of the four possible modes is to be used, as shown in Figure 111. The red and blue pixel positions are interchangeable.

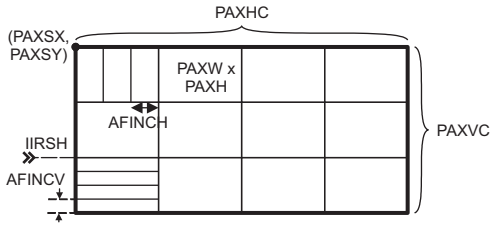
As pertains to the green pixels, since there are two pixels in the 2x2 grid, the outputs of the FV accumulators are summed together to create a single value for each paxel. Firmware must note this since the amplitude of the green output will be containing two pixels while the red and blue output is only one pixel.

Figure 111. Red, Green, and Blue Pixel Extraction Examples



Each paxel is PAXW x PAXH (width x height) pixels. Inside each paxel, horizontal FV can skip lines, operating on one every AFINCV lines. Vertical FV can skip columns, operating on one every AFINCH columns. Up to 32 columns are supported for each paxel. If floor (PAXW/AFINCH) >= 32, only the first 32 designated columns are operated on. PAXW, PAXH, AFINCV and AFINCH are all even numbers, so AF always operates on the same green color, Gr or Gb. IIR filters for the horizontal FVs start operation at column IIRSH.

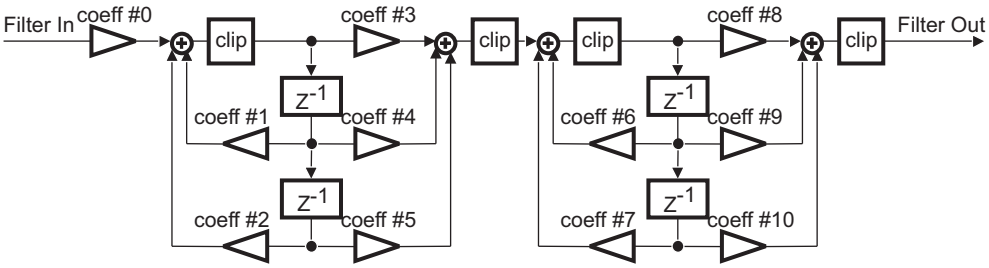
Figure 112. Horizontal/vertical FV Paxel Configuration



4.4.3.2 Horizontal Focus Value Calculator

The focus value calculator takes the unsigned extracted data and subtracts 128 or 512 (depending on whether the A-law is enabled or disabled) to place the data in the range -128 or -512 to 127 or 511. After removing the offset, the data is sent through two IIR filters each with a set of 11 coefficients. Each coefficient is 12-bits wide with 6 bits of decimal (S12Q6). The filter shift registers are cleared on each horizontal line at the position set by the IIR horizontal start register. The absolute value of the output (16-bits wide with 4 bits of decimal, U16Q4) is then sent to the accumulator module. Signed clipping is performed during the focus value calculation. If the input value is m-bits (signed) and the required output value is n-bits, then clipping essentially transforms the input to be between -2^{n-1} and 2^{n-1}. Values lower than -2^{n-1} set to -2^{n-1} and values higher than 2^{n-1} are set to 2^{n-1}. Figure 113 represents this process.

Figure 113. IIR Filter



4.4.3.3 HFV Accumulator

The HFV Accumulator takes the FV values from the horizontal IIR filter and accumulates the FV and FV^2 values for each Paxel. The size and number of Paxels is configurable by registers. In the Peak Mode, maximum value is accumulated. In the Sum mode, all FV are accumulated in a Paxel. There's a threshold register HFV_THR to which the FV and FV^2 are compared. When FV and FV^2 exceed the threshold, it is accumulated and a counter incremented.

aIIRout = abs(IIRout);

HFV = (aIIRout >= threshold) ? aIIRout - threshold : 0;

if (aIIRout>= threshold) HFVcount++;

HFVsq = (HFV * HFV + RNDADD) >> RNDSHIFT ;

RNDADD and RNDSHIFT depend on whether pixels are 8-bit or 10-bit, and achieves rounding down by 8 or 10 bits.

4.4.3.4 Vertical Focus Value Calculator

The focus value calculator takes the unsigned extracted data through two FIR filters each with a set of five coefficients. Each coefficient is 8-bits wide with 4 bits of decimal (S8Q4). Filter outcome is downshifted by 4 bits and taken absolute value to produce a 16-bit unsigned value. This is then sent to threshold and square logic to produce FV and FV-sq.

If vertical focus is disabled, HFVcount and HFVsq are not sent through the DMA interface. If vertical focus is enabled, only the green color channel values are sent through the DMA interface.

4.4.3.5 VFV Accumulator

The VFV Accumulator takes the VFV and VFVsq values from the vertical FIR filters and accumulates them, horizontally and vertically within each paxel. The FVcount is also maintained for each paxel.

FIR_coef = [coef_0, coef_1, coef_2, coef_3, coef_4]; /* coefficient values in S8.4 format */ aFIRout = abs(FIR_out);

FIR_out = (inner_product(extracted_G, FIR_coef) + 8) >> 4;

VFV = (aFIRout >= threshold) ? aFIRout - threshold : 0;

if (aFIRout >= threshold) FVcount++;

VFVsq = (VFV * VFV + RNDADD) >> RNDSHIFT ;

RNDADD and RNDSHIFT depend on whether pixels are 8-bit or 10-bit, and achieves rounding down by 8 or 10 bits.

4.4.4 AE/AWB Engine

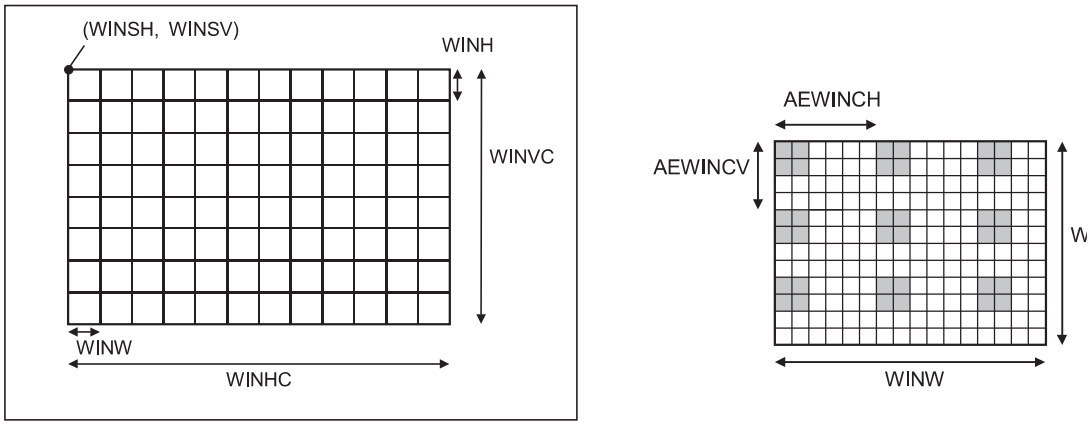
The AE/AWB Engine starts by sub-sampling the frames into windows and further sub-sampling each window into 2x2 blocks. Then for each of the sub-sampled 2x2 blocks each pixel is accumulated. Also, each pixel is compared to a limit set in a register. If any of the pixels in the 2x2 block are greater than or equal to the limit then the block is not counted in the unsaturated block counter. All pixels greater than the limit are replaced by the limit and the value of the pixel is accumulated

4.4.4.1 Sub-Sampler

The Sub-Sampler module takes setting from the register for the starting position of the windows is set by WINSH for the horizontal start and WINSV for the vertical start. The width of the window is set by WINW and the height by WINH. The number of windows in a horizontal direction is set by WINHC while WINVC set the number of windows in the vertical dimension.

Each window is further sampled down to a set of 2x2 blocks. The horizontal distance between the start of blocks is set by AEWINCH. The vertical distance between the start of blocks is set by AEWINCV.

Figure 114. AE/AWB Window Configuration



4.4.4.2 Saturation Check

The saturation check module takes the data from the sub-sampler and compares it to the value in the limit register. It replaces the value of a pixel that is greater than the value in the limit register. If all four pixels in the 2 x 2 block are below the limit, then the value of the unsaturated block counter is incremented. There is one unsaturated block counter per window..

4.4.4.3 AE/AWB Accumulators

The data output from the saturation check module and the sub-sampler module are each accumulated for each pixel. Therefore, the result of this accumulation (per window) is the sum total of red, green1, green2, and blue pixels. There are two sets, one for saturation check and one without. The accumulated results will be written out in U16 format. The precision of the accumulator is 26 bits to support window size of 512x512 (256x256 for each color) without any clipping. The accumulated results can be right shifted up to 15 bits to avoid overflow when built into a packet. The shift value is configured by the SUMSHFT field in the AEWCFG register. In addition to the sum and unsaturated sum in each window, the AE/AWB engine also computes the sum of squared pixels or the minimum pixel value, and the maximum value per window per color, it is also possible to send just accumulator values and increase the maximum number of horizontal windows to 56.

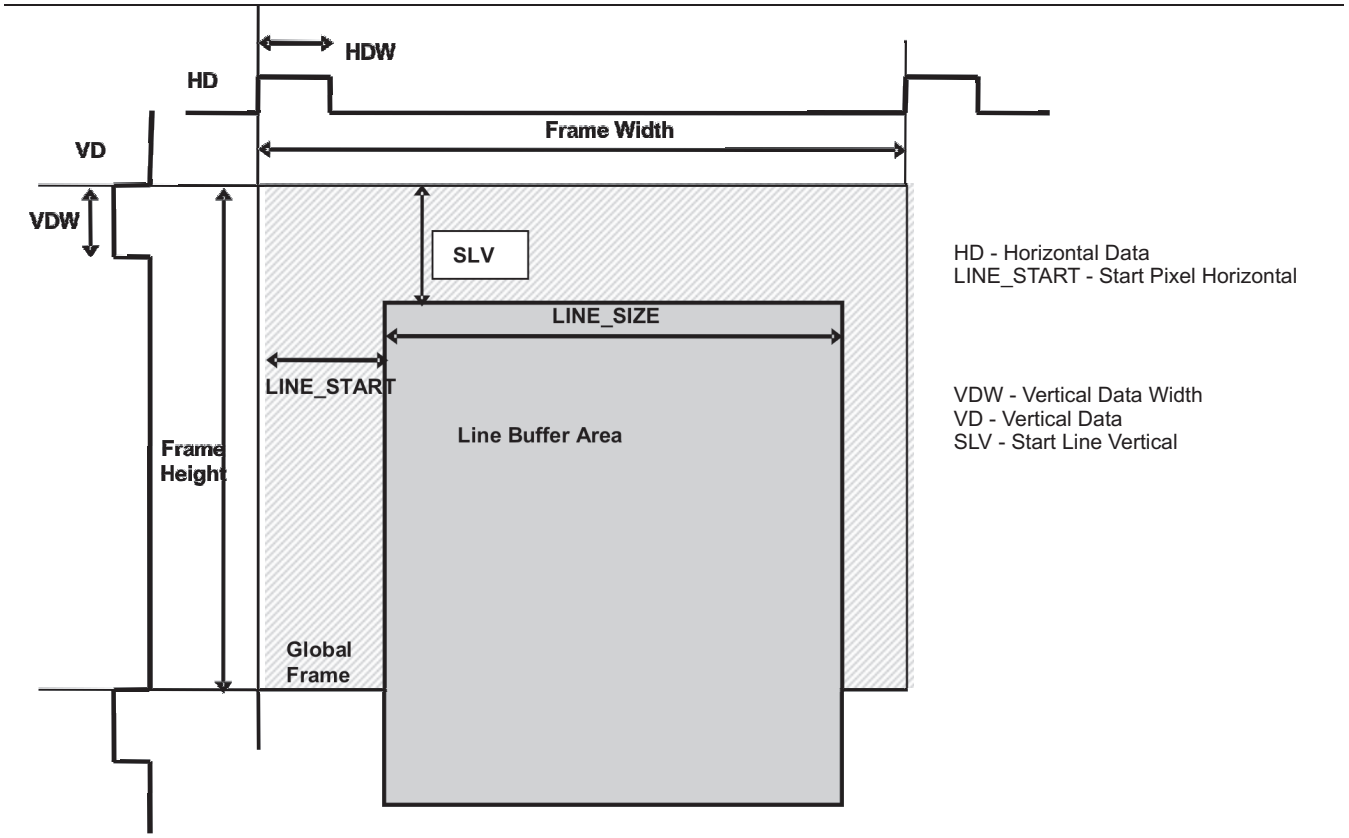
4.4.4.4 Support for a Single Black Row of Paxels/Windows

In addition to the 128 vertical paxels/windows, the AE/AWB module provides support for an additional vertical row of paxels/windows for black data. The black row of paxels/windows can either be before or after the 128 regular vertical paxels/windows. The vertical start setting for the black row of paxels is specified by a separate register setting. Furthermore, the height of the black row of paxels is specified separately from the regular vertical rows of paxels/windows.

4.4.5 Line Framing Logic

In certain cases the number of clock cycles between HD pulses will be greater than the line buffer included in the H3A. In order to solve this problem, a framing module was added prior to the line buffer. The framing module uses the LINE_START register to find the position of the first pixel to place into the line buffer. All other registers will reference this point as the 0 pixel for their start positions. The maximum line size is 4096. After LINE_SIZE clock cycles, the framing logic will disable the line buffer and wait until the next HD. If the next HD comes prior to LINE_SIZE clock cycles, then the active region will end immediately and the counter will wait for the LINE_START count to be reached again. For the vertical position, the SLV filed in the LINE_START register can be used to determine where the start point of the frame is, relative to the rising edge of VD. This logic allows for an active frame to cross VD boundaries and remain in the same frame. Figure 115 shows an example of the frame settings and format module.

Figure 115. Frame Settings/Format



4.4.6 DMA Interface

The DMA Interface module is responsible for taking the data from the AF engine and the AE/AWB engine and building packets to be sent out to the SDRAM/DDRAM. The data interface has separate start and end pointers for the both the AF and AE/AWB engine. It will continuously loop through this data as it builds the packets. In order to optimize the transfer sizes, the DMA interface sends out an AF or AE transfer for each row of paxels or windows.

NOTE: This requires that each horizontal row of paxels or windows will start and end on a 32-byte boundary. If a horizontal row of paxels or windows ends on a non-32 byte boundary, the hardware will pack zeroes. The counts for the AEW that occur every eight windows will be sent in the row with the 8th consecutive window.

The packet formats can be seen in the following tables.

Table 51. AF Packet Format with Vertical AF Disabled

Buffer start address (byte address)	31	16	15	0
AFBUFST	Sum of pixel values used in HFV			(Paxel 0: G)
	HFV_1 (peak or sum)			(Paxel 0: G)
	HFV_2 (peak or sum)			(Paxel 0: G)
	ZEROES			(Paxel 0: G)
	Sum of pixel values used in HFV			(Paxel 0: R)
	HFV_1 (peak or sum)			(Paxel 0: R)
	HFV_2 (peak or sum)			(Paxel 0: R)
	ZEROES			(Paxel 0: R)
	Sum of pixel values used in HFV			(Paxel 0: B)
	HFV_1 (peak or sum)			(Paxel 0: B)
	HFV_2 (peak or sum)			(Paxel 0: B)
	ZEROES			(Paxel 0: B)
	Sum of pixel values used in HFV			(Paxel 1)
	HFV_1 (peak or sum)			(Paxel 1)
	HFV_2 (peak or sum)			(Paxel 1)
				(Paxel 1)
	...			

Table 52. AF Packet Format with Vertical AF Enabled

Buffer start address (byte address)	31	16	15	0
AFBUFST	Sum of pixel values used in HFV			(Paxel 0)
	HFV_1 (peak or sum)			(Paxel 0)
	HFV_sq_1 (peak-sq or sum-sq)			(Paxel 0)
	HFV_count_1			(Paxel 0)
	HFV_2 (peak or sum)			(Paxel 0)
	HFV_sq_2 (peak-sq or sum-sq)			(Paxel 0)
	HFV_count_2			(Paxel 0)
	ZEROES			(Paxel 0)
	VFV_1			(Paxel 0)
	VFV_sq_1			(Paxel 0)
	VFV_count_1			(Paxel 0)

Table 52. AF Packet Format with Vertical AF Enabled (continued)

Buffer start address (byte address)	31	16	15	0
	ZEROES			(Paxel 0)
	VFV_2			(Paxel 0)
	VFV_sq_2			(Paxel 0)
	VFV_count_2			(Paxel 0)
	ZEROES			(Paxel 0)
	Sum of pixel values used in HFV			(Paxel 1)
	HFV_1 (peak or sum)			(Paxel 1)
	HFV_sq_1 (peak-sq or sum-sq)			(Paxel 1)
	HFV_count_1			(Paxel 1)
	...			

Table 53. AE/AWB Packet Format for Sum of Square Mode

Buffer address (byte address)	31 16	15 0	
AEWBUFST	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 0 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
AEWBUFST + 32 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 1 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
AEWBUFST + 64 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 2 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
AEWBUFST + 96 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 3 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
AEWBUFST + 128 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 4 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
AEWBUFST + 160 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 5 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	

Table 53. AE/AWB Packet Format for Sum of Square Mode (continued)

Buffer address (byte address)	31 16	15 0	
	Saturator Accum [3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
AEWBUFST + 192 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 6 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
AEWBUFST + 224 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 7 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Sum of squares[0]		
	Sum of squares[1]		
	Sum of squares[2]		
	Sum of squares[3]		
AEWBUFST + 256 bytes	Unsat count, win 1	Unsat count, win 0	Unsaturated block count For the above 8 windows
	Unsat count, win 3	Unsat count, win 2	
	Unsat count, win 5	Unsat count, win 4	
	Unsat count, win 7	Unsat count, win 6	
	Data for next 8 windows and so on. If the total number of windows is not a multiple of 8, then the unsaturated counters are written immediately following the last window data. For example, if the total number of windows (including black row) are 43, then the first 40 windows are written out as per the 272-byte boundary above. Then the remaining 3 windows are written at +0, +32, and +64 bytes. The counts are written out at +96 instead of +256-byte boundary.		

Table 54. AE/AWB Packet Format for Min-Max Mode

Buffer address (byte address)	31 16	15 0	
AEWBUFST	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 0 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
AEWBUFST + 32 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 1 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
AEWBUFST + 64 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 2 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
AEWBUFST + 96 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 3 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
AEWBUFST + 128 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 4 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
	Minimum[1]	Minimum[0]	
	Minimum[3]	Minimum[2]	
	Maximum[1]	Maximum[0]	
	Maximum[3]	Maximum[2]	
AEWBUFST + 160 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 5 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	

Table 54. AE/AWB Packet Format for Min-Max Mode (continued)

Buffer address (byte address)	31	16	15	0	
	Saturator Accum [3]		Saturator Accum[2]		
	Minimum[1]		Minimum[0]		
	Minimum[3]		Minimum[2]		
	Maximum[1]		Maximum[0]		
	Maximum[3]		Maximum[2]		
AEWBUFST + 192 bytes	Sub Sample Accum[1]		Sub Sample Accum[0]		Window 6 Data
	Sub Sample Accum[3]		Sub Sample Accum[2]		
	Saturator Accum[1]		Saturator Accum[0]		
	Saturator Accum [3]		Saturator Accum[2]		
	Minimum[1]		Minimum[0]		
	Minimum[3]		Minimum[2]		
	Maximum[1]		Maximum[0]		
	Maximum[3]		Maximum[2]		
AEWBUFST + 224 bytes	Sub Sample Accum[1]		Sub Sample Accum[0]		Window 7 Data
	Sub Sample Accum[3]		Sub Sample Accum[2]		
	Saturator Accum[1]		Saturator Accum[0]		
	Saturator Accum [3]		Saturator Accum[2]		
	Minimum[1]		Minimum[0]		
	Minimum[3]		Minimum[2]		
	Maximum[1]		Maximum[0]		
	Maximum[3]		Maximum[2]		
AEWBUFST + 256 bytes	Unsat count, win 1		Unsat count, win 0		Unsaturated block count For the above 8 windows
	Unsat count, win 3		Unsat count, win 2		
	Unsat count, win 5		Unsat count, win 4		
	Unsat count, win 7		Unsat count, win 6		
	Data for next 8 windows and so on. If the total number of windows is not a multiple of 8, then the unsaturated counters are written immediately following the last window data. For example, if the total number of windows (including black row) are 43, then the first 40 windows are written out as per the 272-byte boundary above. Then the remaining 3 windows are written at +0, +32, and +64 bytes. The counts are written out at +96 instead of +256-byte boundary.				

Table 55. AE/AWB Packet Format for Sum-Only Mode

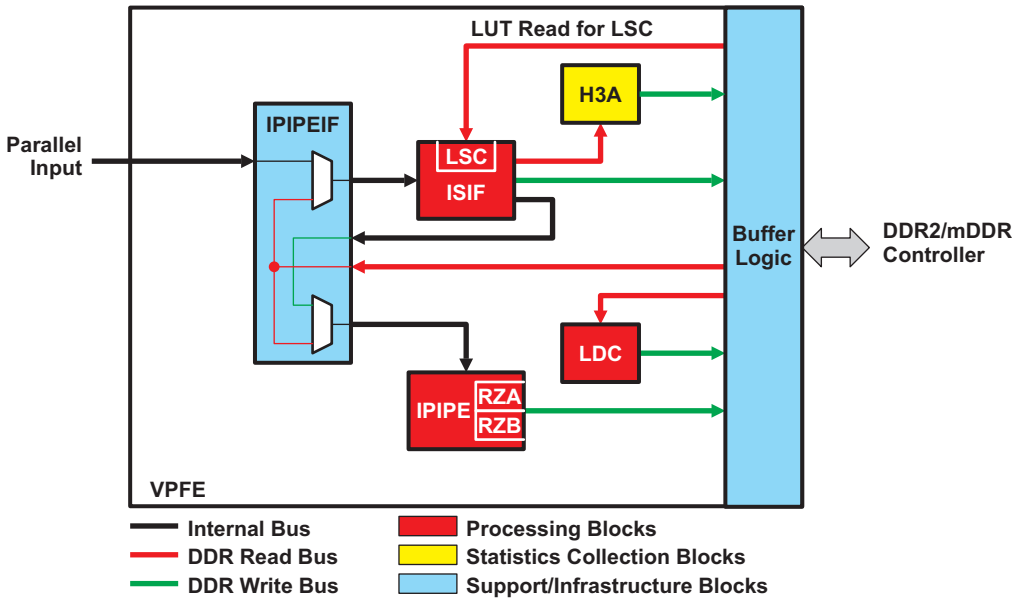
Buffer address (byte address)	31 16	15 0	
AEWBUFST	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 0 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
AEWBUFST + 16 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 1 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
AEWBUFST + 32 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 2 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
AEWBUFST + 48 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 3 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
AEWBUFST + 64 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 4 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
AEWBUFST + 80 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 5 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
AEWBUFST + 96 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 6 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
AEWBUFST + 112 bytes	Sub Sample Accum[1]	Sub Sample Accum[0]	Window 7 Data
	Sub Sample Accum[3]	Sub Sample Accum[2]	
	Saturator Accum[1]	Saturator Accum[0]	
	Saturator Accum [3]	Saturator Accum[2]	
AEWBUFST + 128 bytes	Unsat count, win 1	Unsat count, win 0	Unsaturated block count
	Unsat count, win 3	Unsat count, win 2	For the above 8 windows
	Unsat count, win 5	Unsat count, win 4	
	Unsat count, win 7	Unsat count, win 6	
	Data for next 8 windows and so on. If the total number of windows is not a multiple of 8, then the unsaturated counters are written immediately following the last window data. For example, if the total number of windows (including black row) are 43, then the first 40 windows are written out as per the 144-byte boundary above. Then the remaining 3 windows are written at +0, +16, and +32 bytes. The counts are written out at +48 instead of +128-byte boundary.		

5 Programming Model

5.1 Setup for Typical Configuration

A typical configuration of the VPFE for a digital camera application includes interfacing to a CCD/CMOS sensor. In addition to programming these external devices, the VPFE is programmed in Preview mode to capture data at a 30-Hz frame rate (draft mode). The VPFE sub-module is configured to capture/read this data and format for display via the Image Pipe. Simultaneously, the H3A collects data to be used by user-defined 3A algorithms, and so on. Figure 116 shows the VPFE data flow diagram. The input to the Image Sensor Interface (ISIF) and IPIPE is either raw image data or YCC data. The input to the H3A is only raw image data.

Figure 116. DM36x Video Processing Front End Block Diagram



5.2 Resetting the Camera Subsystem

The entire VPSS subsystem (VPFE and VPBE) can be reset via the Power/Sleep Controller.

5.3 Configuring the Clocks and the Control Signals

The input pixel data clock must be provided by the external imager device. The VPFE syncs to the externally provided signals.

5.4 Programming the Image Sensor Interface (ISIF)

This section discusses the issues related to the image sensor interface software control. It lists which registers are required to be programmed in different modes, how to enable and disable the different blocks in the ISIF, and how to check the status of the ISIF. It also discusses the different register access types and provides a list of programming constraints.

5.4.1 Hardware Setup/Initialization

5.4.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the ISIF are reset to their reset values.

5.4.1.2 Register Setup

Prior to enabling the ISIF, the hardware must be properly configured via register writes. Table 56 identifies the register parameters that must be programmed before enabling the ISIF. Since many of these registers are latched into the hardware by the PCLK, it should be actively clocking during register configuration.

Table 56. ISIF Required Configuration Parameters

Function	Configuration Required
External Pin Signal Configuration	MODESET.HDVDD MODESET.FIDD MODESET.VDPOL MODESET.HDPOL MODESET.FIPOL MODESET.SWEN MODESET.CCDMD CCDCFG.VDLC CCDCFG.EXTRG
Input Mode	MODESET.INPMOD REC656IF.R656ON
YC Input Swap	CCDCFG.YCINSWP
SDRAM Output Enable	SYNCEN.DWEN
Output port MUX enable	ISP.BCR.SRC_SEL_ISIF_IPIPE

Table 57 identifies additional configuration requirements depending on whether the corresponding condition is met. The table can be read as:

if(**Condition** is TRUE), then **Configuration Required** parameters must be programmed.

Table 57. ISIF Conditional Configuration Parameters

Function	Condition	Configuration Required
VSYNC/HSYNC set as outputs	MODESET.HDVDD	HDW VDW PPLN LPFR
Interlaced Fields	MODESET.CCDMD	CCDCFG.FIDMD
External WEN	MODESET.SWEN	CCDCFG.WENLOG
External Trigger	CCDCFG.EXTRG	CCDCFG.TRGSEL
REC656 Input	REC656IF.R656ON	REC656IF.ECCFVH CCDCFG.BW656
YCC Input	MODESET.INPMOD != 0	CLDOFST.CLDC
8 bit YCC Input	MODESET.INPMOD == 2	CCDCFG.Y8POS

Table 57. ISIF Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required
Raw Input	MODESET.INPMOD == 0 && !REC656IF.R656ON	MODESET.DPOL CGAMMAWD.GWDI LINCFG0.LINEN DFCCTL.VDFCEN CLAMPCFG.CLEN 2DLSCCFG.ENABLE FMTCFG.FMTEN CSCCTL.CSCEN CGAMMAWD.WBEN[2:0] CGAMMAWD.OFSTEN[2:0] CGAMMAWD.CFAP CCOLP CRGAIN CGRGAIN CGBGAIN CBGAIN COFSTA CLDCOFST
Linearization Enabled	LINCFG0.LINEN	LINCFG0.CORRSFT LINCFG1.LUTSCL Setup linearization look-up table
Vertical Line Defect Correction	DFCCTL.VDFCEN	DFCCTL.VDFCSL DFCCTL.VDFCUDA DFCCTL.VDFCSFT VDFSATLV.VDFSLV DFCMEMCTL DFCMEM[4:0] DATAHOFST DATAVOFST
2D Lens Shading Correction		LSCHVAL LSCVVAL 2DLSCCFG 2DLSCOFST 2DLSCINI 2DLSCGRBU 2DLSCGRBL 2DLSCGROF 2DLSCORBU 2DLSCORBL 2DLSCOROF 2DLSCIRQEN DATAHOFST DATAVOFST Setup LSC gain and offset look-up tables in SDRAM

Table 57. ISIF Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required
		NOTE: These registers must be set before setting 2DLSCCFG.ENABLE = 1. Additionally, PCLK should be toggling at least 7 times between setting these registers and the 2DLSCCFG.ENABLE bit.
Input Data Formatter	FMTCFG.FMTEN	FMTCFG FMTPLEN FMTSPH FMTLNH FMTSLV FMTLNV FMTRLEN FMTHCNT FMTAPTR[15:0] FMTPGMVF[1:0] FMTPGMAPU[1:0] FMTPGMAPS[7:0]
Color Space Converter	CSCCTL.CSCEN	CSCM[7:0]
DPCM Enabled	MISC.DPCMEN	MISC.DPCMPRE
Black Clamp	CLAMPCFG.CLEN	CLAMPCFG CLDCOFST CLSV CLHWIN[2:0] CLVRV CLVWIN[3:0]
Flash Signal Control	FLSHCFG0.FLSHEN	FLSHCFG1 FLSHCFG2
Write to SDRAM	SYNCEN.DWEN(Common configuration required for raw and YCC modes)	CCDCFG.SDRPACK CCDCFG.BSWD CCDCFG.MSBINVI SPH LNH SLV0 SLV1 LNV CADU CADL CULH CULV HSIZE SDOFST
Write to SDRAM in Raw Mode	MODESET.SWEN && MODESET.INPMOD == 0	MODESET.HLPF MODESET.CCDW COFSTA CGAMMAWD.CCDTBL CGAMMAWD.WBEN0 CGAMMAWD.OFSTEN0

Table 57. ISIF Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required
		MISC.DPCMEN
IPIPE Input	MODESET.INPMOD == 0 && IPIPE is receiving data from ISIF	CGAMMAWD.WBEN1 CGAMMAWD.OFSTEN1
H3A Input	MODESET.INPMOD == 0 && H3A is receiving data from ISIF	CGAMMAWD.WBEN2 CGAMMAWD.OFSTEN2
White Balance (Color) Gains	CGAMMAWD.WBEN0 || CGAMMAWD.WBEN1 || CGAMMAWD.WBEN2	CRGAIN CGRGAIN CGBGAIN
White Balance offset	CGAMMAWD.OFSTEN0 || CGAMMAWD.OFSTEN1 || CGAMMAWD.OFSTEN2	CBGAIN COFSTA CBGAIN
Interrupt Usage	VDINT[2:0] are enabled	VDINT0 VDINT1 VDINT2
2D LSC interrupt is enabled		2DLSCIRQEN

5.4.2 Enable/Disable Hardware

Setting the SYNCEN.SYEN bit enables the Image Sensor Interface. This should be done after all of the required registers mentioned in the previous section are programmed.

The ISIF always operates in continuous mode. In other words, after enabling the ISIF, it continues to process sequential frames until the SYNCEN.SYEN bit is cleared by software. When this happens, the frame being processed is disabled immediately, and does not continue to process the current frame.

When the ISIF is in master mode (HSYNC/VSYNC signals set to outputs), fetching and processing of the frame begins immediately upon setting the SYNCEN.SYEN bit.

When the ISIF is in slave mode (HSYNC/VSYNC signals set to inputs), processing of the frame is dependent upon the input timing of the external sensor/decoder. In order to guarantee that data from the external device is not missed, the ISIF should be enabled prior to data transmission from the external device. In this way, the ISIF waits for the data from the external device.

5.4.2.1 Enabling/Disabling the 2D LSC

When enabling or disabling the 2D LSC, caution must be taken on the timing of register modifications. In order to avoid causing a pre-fetch error or other unexpected behavior, the following safeguards should be implemented:

1. While configuring the 2DLSC registers, the PCLK input into the ISIF must be toggling.
2. All of the 2DLSC registers should be configured appropriately BEFORE enabling the 2DLSCCFG.ENABLE register bit.
3. After enabling the 2DLSCCFG.ENABLE register bit, the hardware immediately begins fetching the first two rows of gain data. When this is complete, the PREFETCH-COMPLETED status flag is set. If the 2DLSCCFG.ENABLE register bit is disabled before SOF status flag is set, then the PREFETCH-ERROR flag is set and the state of the 2DLSC may lead to unexpected errors. Therefore, the 2DLSCCFG.ENABLE register bit should not be disabled until after the SOF status flag is set.
4. When the 2D LSC operation on the active region is completed, the DONE status flag is set. At this point, if the 2DLSCCFG.ENABLE register bit is still set to 1, then the hardware immediately begins to pre-fetch the gain values for the next frame. As mentioned before, if the 2DLSCCFG.ENABLE register bit is disabled after the DONE flag is set, but before the SOF flag for the next frame is set, then the PREFETCH-ERROR flag is set and the state of the 2D LSC may lead to unexpected errors.
5. Therefore, due to the constraints set in Steps 3 and 4 above, the 2DLSCCFG.ENABLE register bit should only be disabled after the SOF status flag is set and before the DONE status flag is set for that

same frame. When the 2DLSC or the whole ISIF needs to be disabled for switching modes, the SOF interrupt should be enabled so that software knows when it is safe to disable the 2D LSC. Then the ISIF can be disabled after the DONE status signal is set for that frame.

5.4.3 Events and Status Checking

The ISIF module can generate four different interrupts: VDINT0, VDINT1, VDINT2, and 2DLSCINT. Note that the SYNCEN.SYEN bit should be enabled to receive any of the ISIF interrupts.

5.4.3.1 VDINT0, VDINT1 and VDINT2 Interrupts

As shown in Figure 117 and Figure 118, VDINT0, VDINT1, and VDINT2 interrupts occur relative to the VSYNC pulse. The trigger timing is selected by using the MODESET.VDPOL setting. VDINT0, VDINT1, and VDINT2 occur after receiving the number of horizontal lines (HSYNC pulse signals) set in the VDINT0, VDINT1, and VDINT2 registers, respectively.

NOTE: In the case of BT.656 input mode, there is a VSYNC at the beginning of each field. Therefore, there are two interrupts for each frame (i.e., one for each field).

If MODESET.VDPOL equals 0, the VDINT0, VDINT1, and VDINT2 HSYNC counters begin counting HSYNC pulses from the rising edge of the external VSYNC.

Figure 117. VDINT0/1/2 Interrupt Behavior when VDPOL=0

If MODESET.VDPOL equals one, the VDINT0, VDINT1, and VDINT2 HSYNC counters begin counting HSYNC pulsed from the rising edge of the external VD.

Figure 118. VDINT0/1/2 Interrupt Behavior when VDPOL=1

5.4.3.2 2D LSC Interrupt

The 2D LSC can be configured to generate a single LSC interrupt based on the events outlined in Table 58.

Table 58. 2D LSC Event Flags

DONE	Set when the internal state of the LSC moves from BUSY to IDLE.
PRE-FETCH ERROR	Set when the gain table is read too slowly from SDRAM.
PRE-FETCH COMPLETE	Set when the pre-fetch buffer contains three full pixel rows. The LSC hardware is ready to begin processing pixels, when this occurs. Software can use this interrupt to reduce the potential for a PREFETCH_ERROR.
SOF	Set when the LSC valid region begins. Registers can be modified for the next frame after this event has occurred.

The 2DLSCIRQEN register can be configured to select which events are masked and which are propagated to the LSC interrupt signal. The 2DLSCIRQST register can be read and cleared to identify which events have occurred.

5.4.3.3 Status Checking

The MODESET.MDFS bit is set when the field status is on an even field and it is cleared when the field status is on an odd field.

The 2DLSC has a register that monitors the status of the LSC (see Section 5.4.3.2).

5.4.4 Register Accessibility During Frame Processing

There are two types of register access in the ISIF module.

- **Shadow registers** (event-latched registers) - These registers can be read and written at any time, but the written values only take effect (become latched) at certain times based on some event. Note that reads still return the most recent write even though the setting are not used until the specific event occurs.
- **Busy-writeable registers** - These registers/fields can be read or written even if the module is busy. Changes to the underlying setting take place instantaneously.

The registers/fields listed below are busy-writeable, all the others are shadowed. Shadowed registers can be optionally set as busy-writeable registers by setting CCDCFG.VDLC to 1.

SYNCEN.SYEN	MODESET.FIPOL	VDINT0	DFCMEMCTL
MODESET.INPMOD	MODESET.HDPOL	VDINT1	DFCMEM0
MODESET.CCDW	MODESET.VDPOL	VDINT2	DFCMEM1
MODESET.CCDMD	MODESET.FIDD	CGAMMAWD.GWDI	DFCMEM2
MODESET.DPOL	MODESET.HDVDD	REC656IF	DFCMEM3
MODESET.SWEN	CCOLP	CCDCFG	DFCMEM4

Most of the 2D LSC configuration registers are latched at LSC SOF. It is recommended to update the 2D LSC registers (to change the LSC configuration for the next frame) after the LSC SOF event and before it starts to pre-fetch the gain values for the next frame (end of LSC active region is reached). The LSC SOF is mapped into the LSC interrupt or can be monitored through the 2DLSCIRQST register.

5.4.5 Inter-Frame Operations

Between frames, it may be necessary to enable/disable functions or modify the memory pointers. Since the SYNCEN.DWEN register and memory pointer registers are shadowed, these modifications can take place any time before the end of the frame and the data gets latched in for the next frame. Likewise, the 2D LSC registers can be changed after receiving the LSC SOF interrupt but before it starts to pre-fetch the gain values for the next frame (end of LSC active region is reached). The host controller performs these changes upon receiving an interrupt.

5.4.6 Summary of Constraints

The following is a list of register configuration constraints to adhere to when programming the ISIF module. It can be used as a quick checklist. More detailed register setting constraints can be found in the individual register descriptions.

- PCLK cannot be higher than 120 MHz.
- If the SDRAM output port is enabled:
  - The memory output line offset and address should be on 32-byte boundaries.
  - (LNH-1) must be a multiple of 32 bytes.
- External WEN cannot be used at the same time as external FID.

- For 2D LSC:
  - N≤M (where M is the horizontal down-sampling factor and N is the vertical down-sampling factor).
  - 2DLSCINI values must be even numbers.
  - Maximum widths with respect to selected M value are:

M	Maximum Line Width
8	1016
16	2032
32	4064
64	8128
128	16256

5.5 Programming the Image Pipe Interface (IPIPEIF)

This section discusses issues related to the software control of the IPIPE interface. It lists which registers are required to be programmed in different modes, how to enable and disable the IPIPE interface, how to check the status the IPIPE interface, discusses the different register access types, and enumerates several programming constraints.

5.5.1 Hardware Setup/Initialization

This section discusses the configuration of the IPIPE interface required before image processing can begin.

5.5.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the IPIPE interface are reset to their reset values.

5.5.1.2 Register Setup

Prior to enabling the IPIPE interface, the hardware must be properly configured via the register writes. Table 59 and Table 60 identify the register parameters that must be programmed before enabling the IPIPE interface.

Table 59. IPIPE Interface Required Configuration Parameters (ISIF Enabled)

Function	Configuration Required
Input Source	CFG1.INPSRC1
Input Clock	CFG1.CLKSEL CLKDIV
DPCM Decoding	DPCM

Table 60. IPIPE Interface Required Configuration Parameters (IPIPE Enabled)

Function	Configuration Required
Input Source	CFG1.INPSRC2
Input Clock	CFG1.CLKSEL CLKDIV
Decimation and Anti-Aliasing Filter	CFG1.DECIM CFG1.AVGFILT

Table 61 identifies additional configuration requirements depending on whether the corresponding condition is met. The table can be read as:

if(**Condition** is TRUE), then **Configuration Required** parameters must be programmed.

Table 61. IPIPE Interface Conditional Configuration Parameters (IPIPE Enabled)

Function	Condition	Configuration Required
Decimation Value	CFG1.DECM	RSZ INIRSZ
Clock Divider	CFG1.CLKSEL	CLKDIV
ISIF input, Parallel I/F source	CFG1.INPSRC1 = 0,2	CFG2.HDPOL CFG2.VDPOL
IPIPE input, ISIF source	CFG1.INPSRC2 = 0	CFG2.YUV16
IPIPE input, raw input	(CFG1.INPSRC2 = 0 && CFG2.YUV16 = 0) || CFG1.INPSRC2 = 1, 2	GAIN OCLIP DPC1
Input from SDRAM	CFG1.INPSRC1 != 0 || CFG1.INPSRC2 != 0	PPLN LPFR HNUM VNUM ADDRU ADDRL ADOFS DPC2
Raw input from SDRAM	CFG1.INPSRC1 = 1,2 || CFG1.INPSRC2 = 1.2	CFG1.UNPACK DPCM
Raw input from SDRAM	(CFG1.INPSRC1 = 1,2 || CFG1.INPSRC2 = 1.2)	CFG1.DATASFT
Input from SDRAM	CFG1.INPSRC1 = 1,2,3 || CFG1.INPSRC2 = 1.2,3	CFG1.ONESHOT
Dark frame subtract	CFG1.INPSRC1 = 2 || CFG1.INPSRC2 = 2	CFG2.DFSDIR
IPIPEIF Interrupt	Interrupt is used	CFG2.INTSRC

5.5.2 Enable/Disable Hardware

When CFG1.INPSRCx = 0, the IPIPEIF does not need to be enabled. It processes whatever the ISIF sends. If CFG1.INPSRDx ≠ 0, then the IPIPEIF begins to fetch data from SDRAM by setting the ENABLE.ENABLE bit. This should be done after all of the required registers in the IPIPE and IPIPEIF are programmed.

When the input source is the SDRAM, the IPIPEIF can, optionally, operate in one-slot mode or continuous mode by setting the CFG1.ONESHOT parameter. If one-shot mode is enabled, then after enabling the IPIPEIF, the ENABLE.ENABLE bit is automatically turned off (set to 0) and only a single frame is processed from memory. In this mode, fetching and processing of the frame begins immediately upon setting the ENABLE.ENABLE bit.

When the input source is the Image Sensor Interface, processing of the frame is dependent upon the timing of the ISIF. In order to guarantee that data from the ISIF is not missed, the IPIPEIF should be enabled prior to the ISIF. In this way, the IPIPEIF waits for data from the ISIF.

When the IPIPEIF is in continuous mode, it can be disabled by clearing the ENABLE.ENABLE bit after processing of the last frame. The disable takes place immediately since it is a busy-write register.

5.5.3 Events and Status Checking

The IPIPEIF generates an IPIPEIF event based on the CFG2.INTSRC bit-field setting.

5.5.4 Register Accessibility During Frame Processing

There are two types of register access in the IPIPEIF module.

- **Shadow registers** - These registers can be read and written (if the field is writeable) at any time. However, the written values take effect at the start of frame (VSYNC active edge). Note that reads still return the most recent write even though settings are not used until the next start of frame. The following are the shadow registers in the IPIPE interface:

ENABLE.SYNCOFF	HNUM	RSZ
CFG1. DECIM	VNUM	GAIN
CFG1.AVGFILT	ADDRU	RSZ3A. DECM
PPLN	ADDRL	RSZ3A.AVGFILT
LPFR	ADOFS	RSZ3A.RSZ

- **Busy-writeable registers** - These registers/fields can be read or written even if the module is busy. Changes to the underlying setting take place instantaneously. The following registers are busy-writeable:

ENABLE.ENABLE	CFG1.UNPACK	CFG2
CFG1.INPSRC1	CFG1.INPSRC2	INIRSZ
CFG1.DATASFT	CFG1.ONESHOT	OCLIP
CFG1.CLKSEL	DPCM	DPC1
		DPC2
		INIRSZ3A

5.5.5 Inter-Frame Operations

Between frames, it may be necessary to enable/disable functions or modify the memory pointers. Since several of the registers are shadowed, these modifications can take place any time before the end of the frame and the data gets latched in for the next frame. The host controller can perform these changes upon receiving an interrupt or and EDMA transfer can be programmed to make these changes upon receiving an event.

5.5.6 Summary of Constraints

The following is a list of register configuration constraints to adhere to when programming the IPIPEIF. It can be used as a quick checklist. More detailed register setting constraints can be found in the individual register descriptions.

- If the SDRAM output port is enabled:
  - The memory output line offset and address should be on 32-byte boundaries.
  - Data is fetched starting on the second VSYNC.
- In dark-frame subtract, LPFR must be > 0, since the first line cannot be fetched.

5.6 Programming the Image Pipe (IPIPE)

This section discusses the issues related to the IPIPE software control. It lists which registers are required to be programmed in different modes, how to enable and disable the IPIPE, discusses the different register access types, and enumerates several programming constraints.

5.6.1 Hardware Setup/Initialization

This section describes the IPIPE configuration required before image processing can begin in IPIPE module.

5.6.1.1 Reset Behavior

Upon VPSS hardware reset, all of the registers in the IPIPE are reset to their reset values. However, since the IPIPE programmable look-up tables (LUT DPC, Gamma Correction, Edge Enhancer, 3DLUT, and histogram work memory) are stored in internal RAM, their contents do not have reset values. If the reset is a chip-level power-on-reset (reset after power is applied), then the contents of these tables are unknown. If the reset is a VPSS module reset (when power remains active), then the contents of these tables remains the same as before the reset.

5.6.1.2 Register Setup

Prior to enabling the IPIPE, the hardware must be properly configured via register writes. In order to write to the IPIPE registers, the IPIPE.GCK_MMR register must first be set to 1. In order to write to the Resizer registers, the RSZ.GCK_MMR register must first be set to 1.Table 62 identifies the register parameters that must be programmed before enabling the IPIPE.

Table 62. IPIPE Required Configuration Parameters

Function	Configuration Required (IPIPE Registers)	Configuration Required (Resizer Registers)
Function Enable/Disable	SRC_MODE SRC_FMT	SRC_MODE SRC_FMT0
Input Size	SRC_VPS SRC_VSZ SRC_HPS SRC_HSZ	SRC_VPS SRC_VSZ SRC_HPS SRC_HSZ
Clocks	GCK_PIX	GCK_SDR
BOXCAR Output	BOX_SDR_SAD_H BOX_SDR_SAD_L	
SDRAM Output		RZX_SDR_Y_SAD_H RZX_SDR_Y_SAD_L
SDRAM Output for 4:2:0 mode		RZX_SDR_Y_SAD_H RZX_SDR_Y_SAD_L RZX_SDR_C_SAD_H RZX_SDR_C_SAD_L
DMA Regulator		DMA_RZX DMA_RZB
ISP configuration (output port MUX)	ISP.BCR.SRC_SEL_ISIF_IPIPE ISP.BCR.SRC_SEL_IPIPE_LDC	

Table 63 identifies additional configuration requirements depending on whether the corresponding condition is met.

The table can be read as: if(**Condition** is TRUE), then **Configuration Required** parameters must be programmed.

Table 63. Conditional Configuration Parameters

Function	Condition	Configuration Required	
		IPIPE	Resizer
IPIPE Raw Processing Path Functions	SRC_FMT = 0, 1	SRC_COL DPC_LUT_EN DPC_OTF_EN D2F_1ST_EN D2F_2ND_EN	

Table 63. Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required	
		IPIPE	**Resizer**
		GIC_EN BOX_EN HST_EN WB2_OFT_R WB2_OFT_GR WB2_OFT_GB WB2_OFT_B WB2_WGN_R WB2_WGN_GR WB2_WGN_GB WB2_WGN_B LSC_VOFT LSC_VA2 LSC_VA1 LSC_VS LSC_HOFT LSC_HA2 LSC_HA1 LSC_HS LSC_GAN_R LSC_GAN_GR LSC_GAN_GB LSC_GAN_B LSC_OFT_R LSC_OFT_GR LSC_OFT_GB LSC_OFT_B LSC_SHF LSC_MAX	
IPIPE Raw-to-YCbCr Processing Path Functions	SRC_FMT = 0	CFA_MODE RGB1_MUL_RR RGB1_MUL_GR RGB1_MUL_BR RGB1_MUL_RG RGB1_MUL_GG RGB1_MUL_BG RGB1_MUL_RB RGB1_MUL_GB RGB1_MUL_BB RGB1_OFT_OR RGB1_OFT_OG RGB1_OFT_OB GMM_CFG RGB2_MUL_RR RGB2_MUL_GR RGB2_MUL_BR	

Table 63. Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required	
		IPIPE	Resizer
		RGB2_MUL_RG RGB2_MUL_GG RGB2_MUL_BG RGB2_MUL_RB RGB2_MUL_GB RGB2_MUL_BB RGB2_OFT_OR RGB2_OFT_OG RGB2_OFT_OB D3LUT_EN YUV_ADJ YUV_MUL_RY YUV_MUL_GY YUV_MUL_BY YUV_MUL_RCB YUV_MUL_GCB YUV_MUL_BCB YUV_MUL_RCR YUV_MUL_GCR YUV_MUL_BCR YUV_OFT_Y YUV_OFT_CB YUV_OFT_CR YUV_PHS GBCE_EN	
YCbCr Processing Path Functions	SRC_FMT = 0,3	YEE_EN CAR_EN CGS_EN	SRC_EN SRC_MODE SRC_FMT0 SRC_FMT1 SRC_VPS SRC_VSZ SRC_HPS SRC_HSZ YUV_Y_MIN YUV_Y_MAX YUV_C_MIN YUV_C_MAX YUV_PHS SEQ RZA_EN RZB_EN
Boxcar	SRC_FMT = 0,1,2 && BOX_EN	BOX_MODE BOX_TYP BOX_SHF BOX_SDR_SAD_H	

Table 63. Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required	
		IPIPE	Resizer
		BOX_SDR_SAD_L	
LUT Defect Correction	DPC_LUT_EN	DPC_LUT_SEL DPC_LUT_ADR DPC_LUT_SIZ Setup defect look-up table	
On-The-Fly Defect Correction	DPC_OTF_EN	DPC_OTF_TYP DPC_OTF_2_D_THR_R DPC_OTF_2_D_THR_GR DPC_OTF_2_D_THR_GB DPC_OTF_2_D_THR_B DPC_OTF_2_C_THR_R DPC_OTF_2_C_THR_GR DPC_OTF_2_C_THR_GB DPC_OTF_2_C_THR_B DPC_OTF_3_SHF DPC_OTF_3_D_THR DPC_OTF_3_D_SLP DPC_OTF_3_D_MIN DPC_OTF_3_D_MAX DPC_OTF_3_C_THR DPC_OTF_3_C_SLP DPC_OTF_3_C_MIN DPC_OTF_3_C_MAX	
Noise Filter-1	D2F_1ST_EN	D2F_1ST_TYP D2F_1ST_THR[8] D2F_1ST_STR[8] D2F_1ST_SPR[8] D2F_1ST_EDG_MIN D2F_1ST_EDG_MAX	
Noise Filter-2	D2F_2ND_EN	D2F_2ND_TYP D2F_2ND_THR[8] D2F_2ND_STR[8] D2F_2ND_SPR[8] D2F_2ND_EDG_MIN D2F_2ND_EDG_MAX	
Green Imbalance Correction	GIC_EN	GIC_TYP GIC_GAN GIC_NFGAN GIC_THR GIC_SLP	
Histogram	HST_EN	HST_MODE HST_SEL HST_PARA HST_0_VPS HST_0_VSZ HST_0_HPS	

Table 63. Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required	
		IPIPE	Resizer
		HST_0_HSZ HST_1_VPS HST_1_VSZ HST_1_HPS HST_1_HSZ HST_2_VPS HST_2_VSZ HST_2_HPS HST_2_HSZ HST_3_VPS HST_3_VSZ HST_3_HPS HST_3_HSZ HST_TBL HST_MUL_R HST_MUL_GR HST_MUL_GB HST_MUL_B	
Boundary Signal Calculator	BSC_EN	BSC_MODE BSC_TYP	
BSC Row Sums	BSC_TYP.REN	BSC_ROW_VCT BSC_ROW_SHF BSC_ROW_VPOS BSC_ROW_VNUM BSC_ROW_VSKIP BSC_ROW_HPOS BSC_ROW_HNUM BSC_ROW_HSKIP	
BSC Column Sums	BSC_TYP.CEN	BSC_COL_VCT BSC_ COL _SHF BSC_ COL _VPOS BSC_ COL _VNUM BSC_ COL _VSKIP BSC_ COL _HPOS BSC_ COL _HNUM BSC_ COL _HSKIP	
Gamma Correction	GMM_CFG.BYPR=0 || GMM_CFG.BYPG=0 || GMM_CFG.BYPB=0	GMM_CFG.TBL GMM_CFG.SIZ Setup gamma table(s) if in RAM	
3D LUT	D3LUT_EN	Setup look-up tables for the three colors RGB	
Global Brightness and Contrast Enhancement	GBCE_EN	GBCE_TYP Setup look-up table for GBCE	
Edge Enhancement	YEE_EN	YEE_TYP YEE_SHF	

Table 63. Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required	
		IPIPE	Resizer
		YEE_MUL_00 YEE_MUL_01 YEE_MUL_02 YEE_MUL_10 YEE_MUL_11 YEE_MUL_12 YEE_MUL_20 YEE_MUL_21 YEE_MUL_22 YEE_THR YEE_E_GAN YEE_E_THR_1 YEE_E_THR_2 YEE_G_GAN YEE_G_OFT Setup Edge Enhancement LUT	
Chroma Artifact Reduction	CAR_EN	CAR_TYP CAR_SW CAR_HPF_TYP CAR_HPF_SHF CAR_HPF_THR CAR_GN1_GAN CAR_GN1_SHF CAR_GN1_MIN CAR_GN2_GAN CAR_GN2_SHF CAR_GN2_MIN	
Chroma Gain Suppression	CGS_EN	CGS_GN1_L_THR CGS_GN1_L_GAN CGS_GN1_L_SHF CGS_GN1_L_MIN CGS_GN1_H_THR CGS_GN1_H_GAN CGS_GN1_H_SHF CGS_GN1_H_MIN CGS_GN2_L_THR CGS_GN2_L_GAN CGS_GN2_L_SHF CGS_GN2_L_MIN	
Resizer Enabled[(1)]	RZx_EN		RZx_MODE RZx_420 RZx_I_VPS RZx_I_HPS RZx_O_VSZ RZx_O_HSZ

(1) RZx refers to either RZA (for resizer-A) or RZB (for resizer-B), depending on which resizer is being configured.

Table 63. Conditional Configuration Parameters (continued)

Function	Condition	Configuration Required	
		IPIPE	Resizer
			RZx_V_PHS_Y RZx_V_PHS_C RZx_V_DIF RZx_V_TYP RZx_V_LPF RZx_H_PHS RZx_H_PHS_ADJ RZx_H_DIF RZx_H_TYP RZx_H_LPF RZx_DWN_EN RZx_DWN_AV RZx_RGB_EN RZx_RGB_TYP RZx_RGB_BLD RZx_SDR_Y_BAD_H RZx_SDR_Y_BAD_L RZx_SDR_Y_SAD_H RZx_SDR_Y_SAD_L RZx_SDR_Y_OFT RZx_SDR_Y_PTR_S RZx_SDR_Y_PTR_E RZx_SDR_C_BAD_H RZx_SDR_C_BAD_L RZx_SDR_C_SAD_H RZx_SDR_C_SAD_L RZx_SDR_C_OFT RZx_SDR_C_PTR_S RZx_SDR_C_PTR_E
Resizer RGB Output Configuration	RZx_RGB_EN		RZx_RGB_TYP
Resizer RGB Alpha value in 32 bit out mode	RZx_RGB_TYP.TYP = 0		RZx_RGB_BLD
Interrupt Usage	If Resizer interrupts are required (RSZ_INT_CYC_RZx)		IRQ_RZx

In certain bypass modes, the data still passes through modules that need to be reset to their default values so that the data being passed through is not modified. The following sections identify which registers need to be set to which values in the various bypass modes.

5.6.1.2.1 Resizer Bypass Mode

Since the YCbCr data still passes through the RZA block in resizer bypass mode, the following Resizer registers must be set accordingly:

SRC_FMT1[420] = 422
RZA_EN = ENABLE
RZA_420[Y[= DISABLE
RZA_420[C] = DISABLE
RZA_I_VPS = 0
RZA_I_HPS = 0
RZA_V_PHS_Y = 0
RZA_V_PHS_C = 0
RZA_V_DIF = 256
RZA_V_LPF[Y] = 0
RZA_V_LPF[C] = 0
RZA_H_PHS = 0
RZA_H_PHS_ADJ = 0
RZA_H_DIF = 256
RZA_H_LPF[Y] = 0
RZA_H_LPF[C] = 0
RZA_DWN_EN = DISABLE
RZA_RGB_EN = DISABLE
RZB_EN = DISABLE

5.6.1.2.2 Raw Input, Raw Output Mode (IPIPE.SRC_FMT = 1)

In this mode, the raw data bypassed the raw-to-YCbCr processes, but since it still passes through the RZA processing blocks, the following registers must be set accordingly:

IPIPE.SRC_FMT = 1
SRC_FMT1[RAW] = 1
RZA_EN = ENABLE
RZA_420[Y[= DISABLE
RZA_420[C] = DISABLE
RZA_I_VPS = 0
RZA_I_HPS = 0
RZA_V_PHS_Y = 0
RZA_V_PHS_C = 0
RZA_V_DIF = 256
RZA_V_LPF[Y] = 0
RZA_V_LPF[C] = 0
RZA_H_PHS = 0
RZA_H_PHS_ADJ = 0
RZA_H_DIF = 256
RZA_H_LPF[Y] = 0
RZA_H_LPF[C] = 0
RZA_DWN_EN = DISABLE
RZA_RGB_EN = DISABLE
RZB_EN = DISABLE

5.6.1.3 Internal (Embedded) Memory Access

Internal memories (look-up tables, output storage memories for histogram, and BSC) that are embedded in the VPSS memories (see Section 3.4) are accessed by ARM through the configuration bus. Note that the histogram memory can be made self-cleaning by setting the register field HST_TBL.CLR to 1.

NOTE: In order to access these memories, the IPIPE.GCK_MMR register must be first set to 1 and the PCLK input to IPIPE must be enabled. If PCLK is not being driven by an external imager at the time these registers need to be accessed, the IPIPEIF can be configured to drive the PCLK input to IPIPE by setting the IPIPEIF.CFG.CLKSEL register bit to 1.

5.6.2 Enable/Disable Hardware

Setting the IPIPE.SRC_EN.EN bit enables the IPIPE. This should be done after all of the required registers and tables mentioned in the previous section are programmed.

When the IPIPE is set to one-shot mode, only a single frame is processed. When the IPIPE is in continuous mode, it can be disabled by clearing the IPIPE.SRC_EN.EN bit during the processing of the last frame. The disable is latched in at the end of the frame it was written in.

5.6.3 Events and Status Checking

IPIPE has five interrupt signals, and the Resizer also has five interrupt signals. Enabling of the interrupt signals is controlled by the interrupt controller. The same interrupt events can be used to trigger the EDMA events that are controlled by the event controller.

5.6.3.1 IPIPE Interrupt Signals

IRQ0 (IPIPE_INT_REG) is issued when the IPIPE register update is allowed.

IRQ1 (IPIPE_INT_LAST_PIX) is issued when the last pixel of a frame comes into IPIPE.

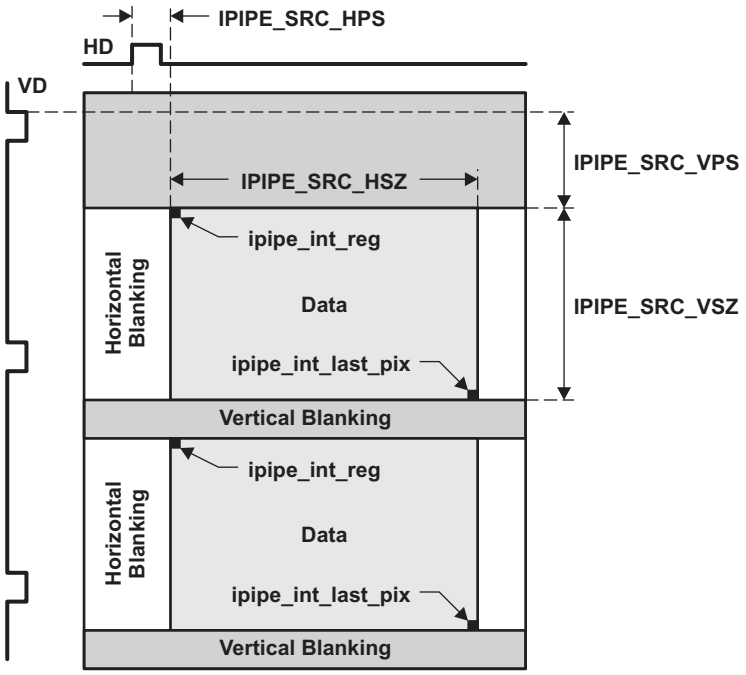
IRQ2 (IPIPE_INT_DMA) is issued when the boxcar SDRAM transfer is done. On this timing, IPIPE_EOF is sent to BL.

IRQ3 (IPIPE_INT_BSC) is issued when the boundary signal calculation is done.

IRQ4 (IPIPE_INT_HST) is issued when the histogram is done.

The interrupts IPIPE_INT_REG and IPIPE_INT_LAST_PIX are issued at the beginning and the end of the valid data area.

Figure 119. IPIPE_INT_REG and IPIPE_INT_LAST_PIX are Issued



5.6.3.2 Resizer Interrupt Signals

RSZ_INT_REG is issued when the RSZ register update is allowed.

RSZ_INT_LAST_PIX is issued when the last pixel of a frame comes into RSZ

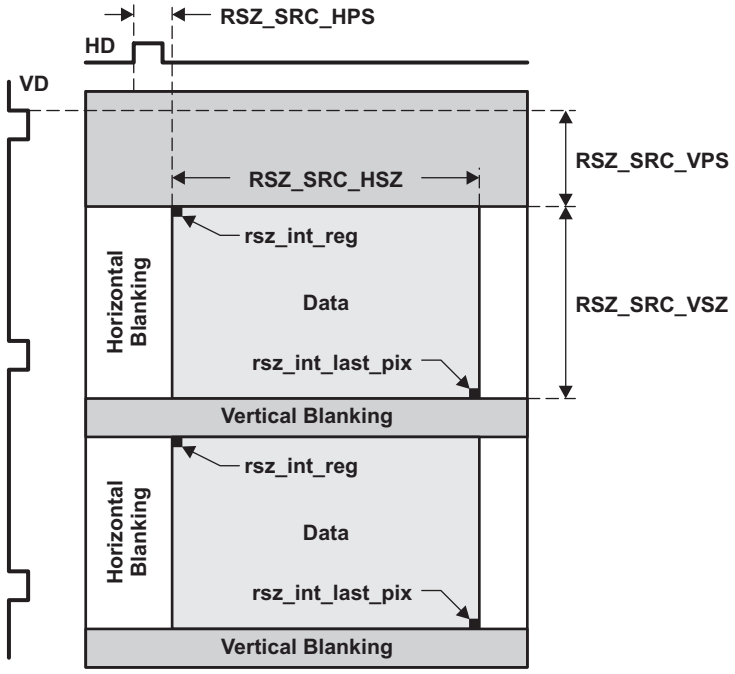
RSZ_INT_DMA is issued when the RSZ SDRAM (both resize-A and resize-B) transfer is done. On this timing, RSZ_EOF is sent to BL.

RSZ_INT_CYC_RZA is issued after every Na lines of image-a of the RSZ are written to SDRAM. (Na is specified by the register IRQ_RZA).

RSZ_INT_CYC_RZB is issued after every Na lines of image-b of the RSZ are written to SDRAM. (Na is specified by the register IRQ_RZB).

The interrupts RSZ_INT_REG and RSZ_INT_LAST_PIX are issued at the beginning and the end of the valid data area.

Figure 120. RSZ_INT_REG and RSZ_INT_LAST_PIX are Issued



5.6.4 Register Accessibility During Frame Processing

There are two types of register access in the IPIPE.

- **Shadow registers** - These registers can be read and written (if the field is writeable) at any time after receiving the IRQ0 event. However, the written values take effect at the start of next frame. Note that reads still return the most recent write even though settings are not used until the next start of frame. If these registers are written before receiving the IRQ0 event, the written values may apply to the current frame or the next frame. All the IPIPE registers not listed as busy-writeable registers below are included as shadow registers.
- **Busy-writeable registers** - These registers/fields can be read or written even if the module is busy. Changes to the underlying setting take place instantaneously. Therefore, to avoid unintended behavior, it is recommended that these registers only be written when the module is not busy. The following registers are busy-writeable:

IPIPE_GCK_PIX
IPIPE_GCK_SDR
IPIPE_HST_SEL
IPIPE_SRC_VPS
IPIPE_SRC_HPS
IPIPE_SRC_EN

RSZ_GCK_PIX
RSZ_GCK_SDR
RSZ_SRC_MODE
RSZ_SRC_FMT0
RSZ_SRC_VPS
RSZ_SRC_HPS
RSZ_SRC_EN

5.6.5 Inter-Frame Operations

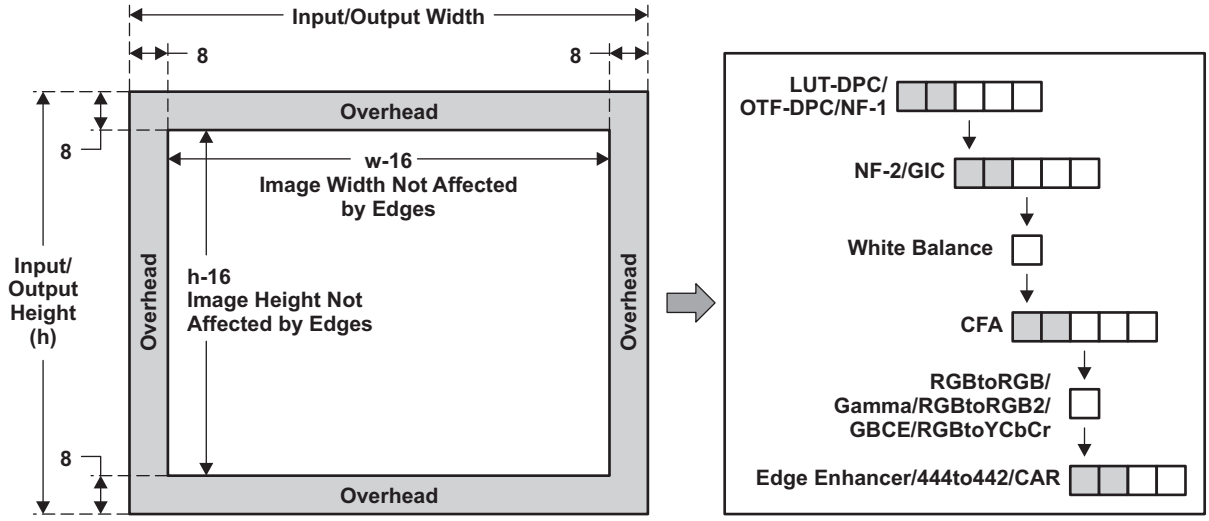
Between frames, it may be necessary to enable/disable functions or modify the memory pointers. Since several of the registers are shadowed, these modifications can take place any time after the IRQ0 (update register) interrupt and before the end of the frame and the data gets latched in for the next frame. The host controller can perform these changes upon receiving an interrupt or and EDMA transfer can be programmed to make these changes upon receiving an event.

Also, due to the input/output maximum width constraint of 2176 pixels (RZA), it may be necessary to process the image in vertical slices. The vertical slices processed by the IPIPE are required to overlap, due to the mirroring of image data at the edges, by internal filtering processes. The amount of overlap is determined by which filtering functions are enabled during processing. The next section indicates how many edge pixels/lines are needed for edge overhead by enabling certain functions within the IPIPE.

5.6.6 Overhead Lines and Pixels

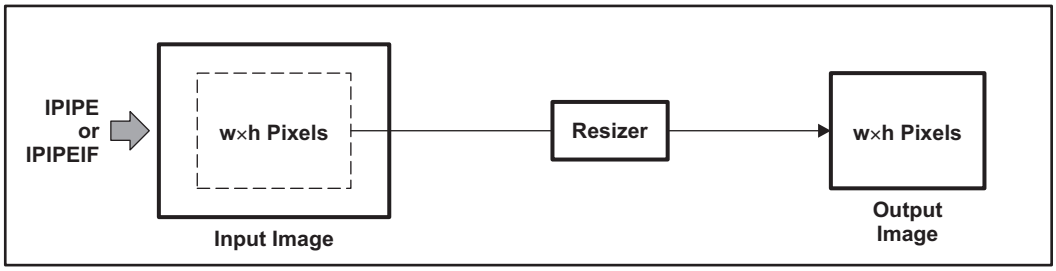
Filtering processes in IPIPE create overhead pixels at the lateral side (left/right). Figure 121 shows the lateral overhead of each process. LUT DPC, OTF-DPC, and Noise filter-1 together give an overhead of two pixels at the edges. Noise filter-2 and GIC together give an overhead of two pixels and the white balance module, RGB2RGB, Gamma, RGB2RGB2, GBCE, and YCbCr, require any overhead on horizontal sides. EE, 444to422, and CAR together give an overhead of two pixels. All the sub-blocks together give a total overhead of eight pixels of each side, horizontally.

Figure 121. 8 Pixels on Each Side are Affected by Boundary Conditions

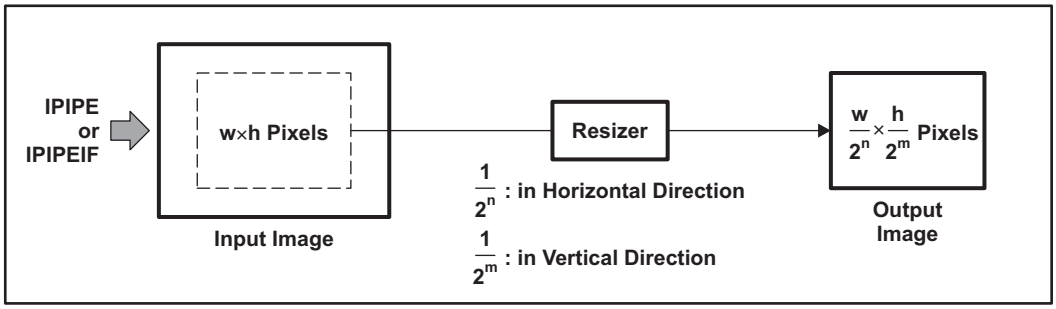


The number of overhead pixels at edges from the Resizer module depends on the Resizer's parameters.

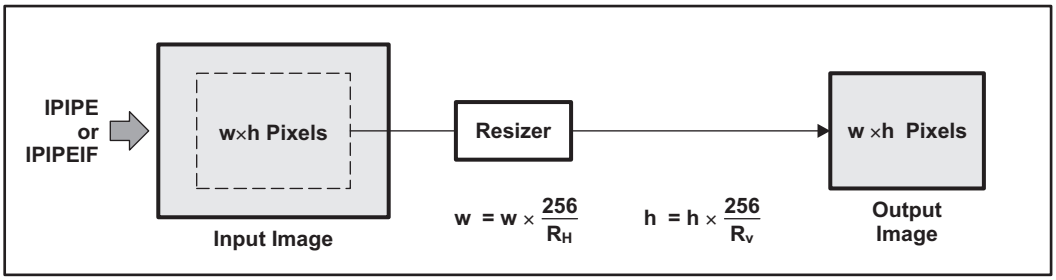
- Cropping only (no scale up or down or no sub-pixel shift) - Zero-pixel overhead at the edges.



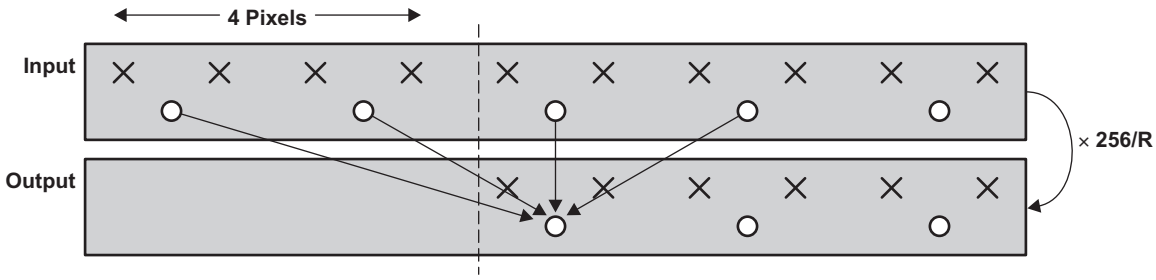
- Downscale to 1/2n size (no interpolation or no sub-pixel shift) - Zero-pixel overhead at edges.



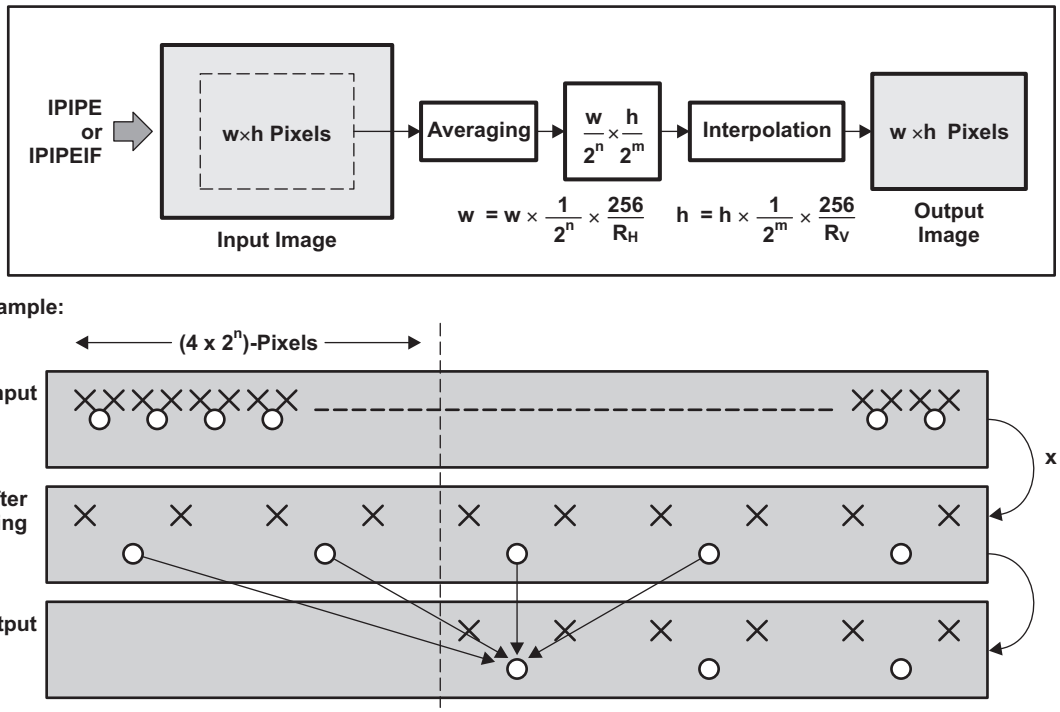
- Normal mode (x 256/Rh and x 256/Rv) - 4-pixel overhead at the edges.



Example:

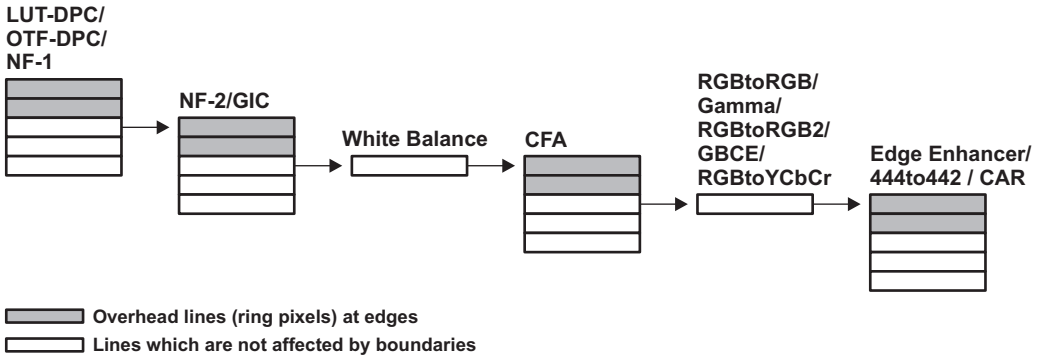


- Down-scale mode (x 1/2n x 256/Rh, and x 1/2m x 256/Rv with 256 < RH, RV) - (4 x 2n)-pixel overhead at the edges.



On the vertical side, a total of eight lines of overhead are required per side (top and bottom) with same distribution of overhead on the horizontal side. For more information on block level, see Figure 122.

Figure 122. 8 Lines at Each Side are Affected by the Boundary Conditions



NOTE: CFA has one more line delay to match the internal timing, in addition to the two explained above. Therefore, the total vertical latency of IPIPE is 9 lines.

5.6.6.1 Frame Division Mode

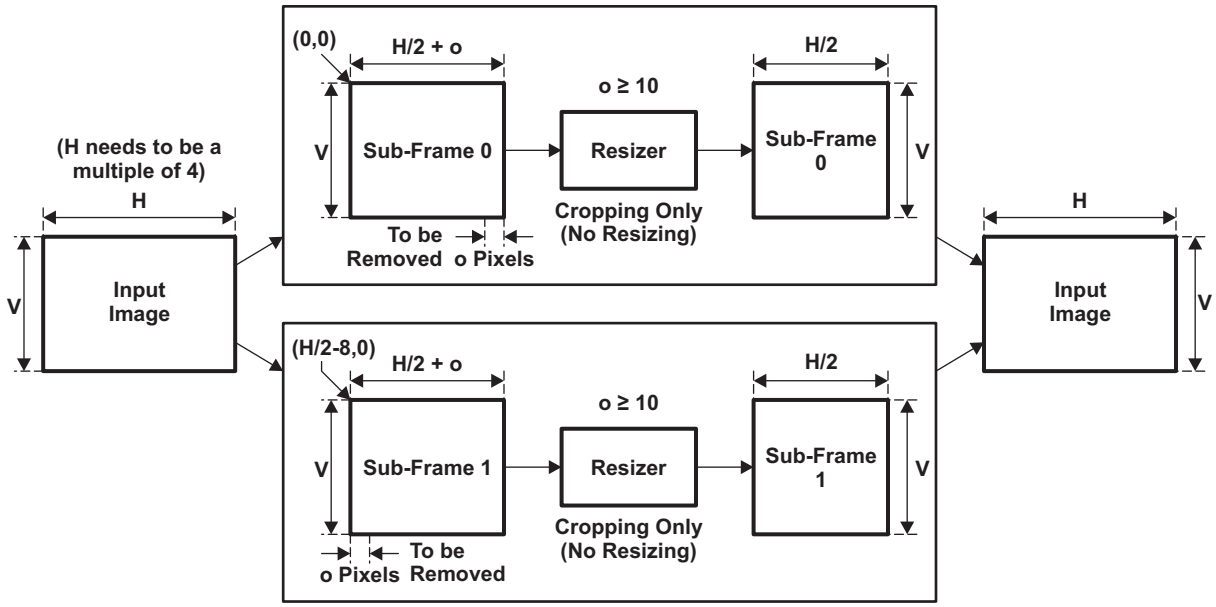
IPIPE supports input images split into sub-blocks (frame-division-mode). The overheads at the boundaries of each block are masked by the Resizer module. In the following section, examples of these operations are described.

5.6.6.1.1 Frame Division Mode – No Resizing

If only IPIPE is applied to the image and rescaling operation is not applied (only cropping is applied), 10 pixels (horizontal) or 8 pixels (vertical) between two frames are consumed as border pixels (ring pixels).

In the following example, both the left side frame (frame-0) and the right side frame (frame-1) need to have more than 10 pixels of border pixels, which are removed by cropping (see Figure 123).

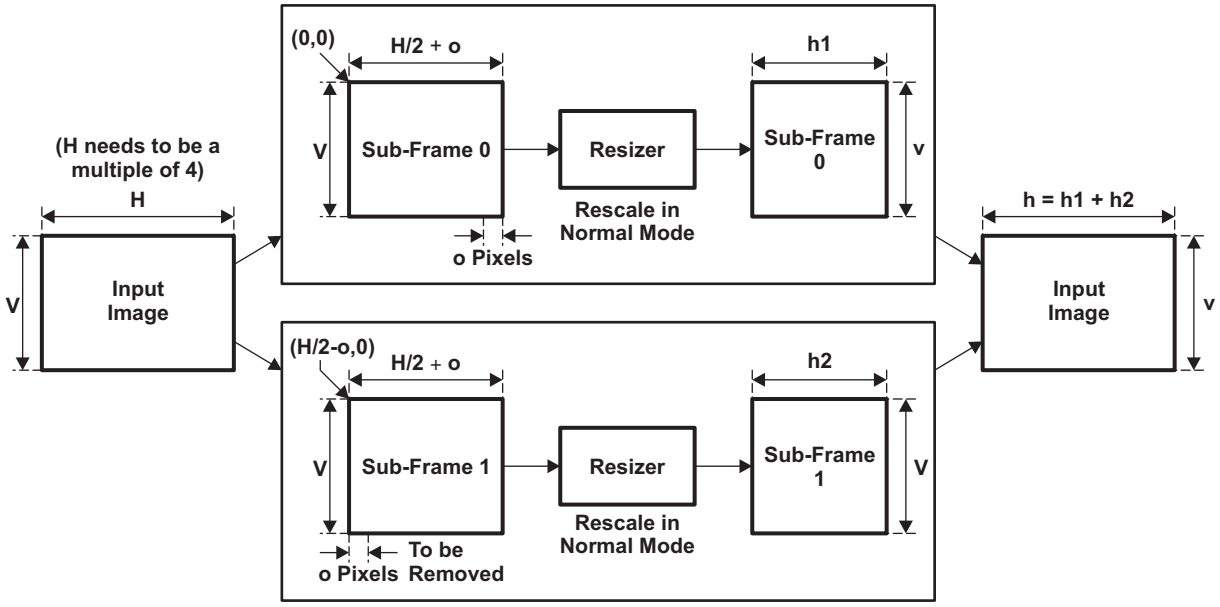
Figure 123. Frame Division Operation Example (No Rescaling)



5.6.6.1.2 Frame Division Mode – Resizing With Normal Mode

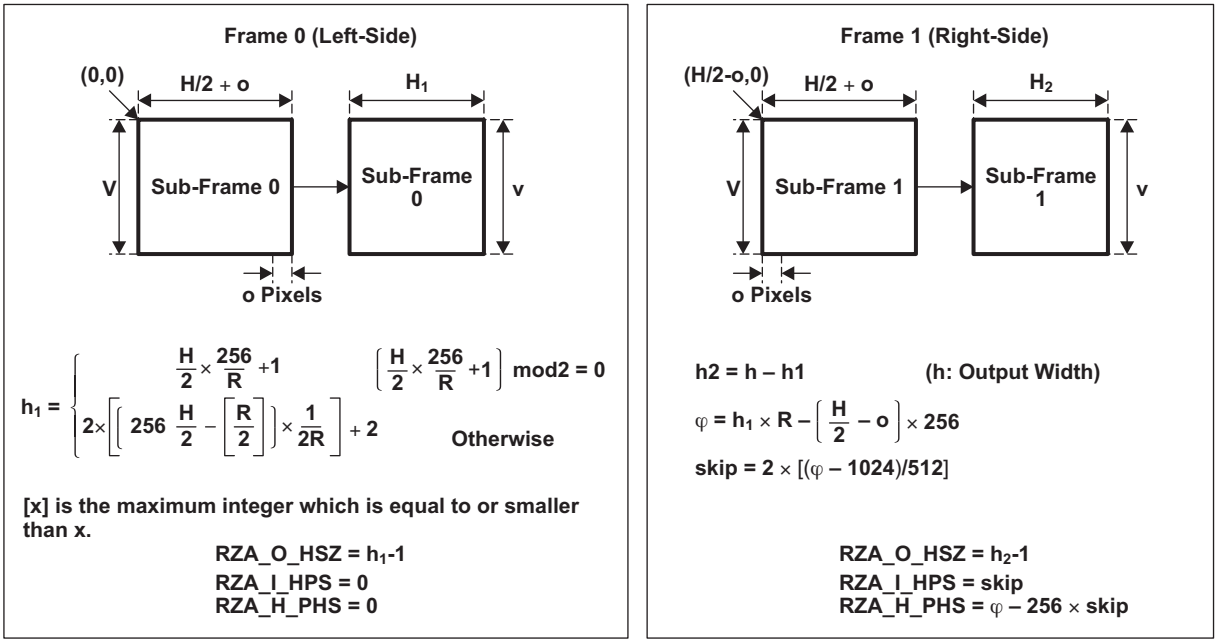
If both IPIPE and Resizer in normal mode are applied, images are rescaled in the following way. Here, the scaling ratio is *R*; the Resizer scales the image to x256/*R* size. The input width, *H*, needs to be a multiple of 4.

Figure 124. Frame Division Operation Example (Normal Mode)



The parameters used in the resizing process are described in Figure 125. For resize-B operation, RZA is replaced with RZB.

Figure 125. Resizer Parameters for Frame-0 (Left) and Frame-1 (Right) in Normal Mode



In this case, some pixels are used to match the two frames in addition to the 10 border pixels caused by IPIPE operation. With the Resizer working in normal mode, the following numbers of pixels are required.

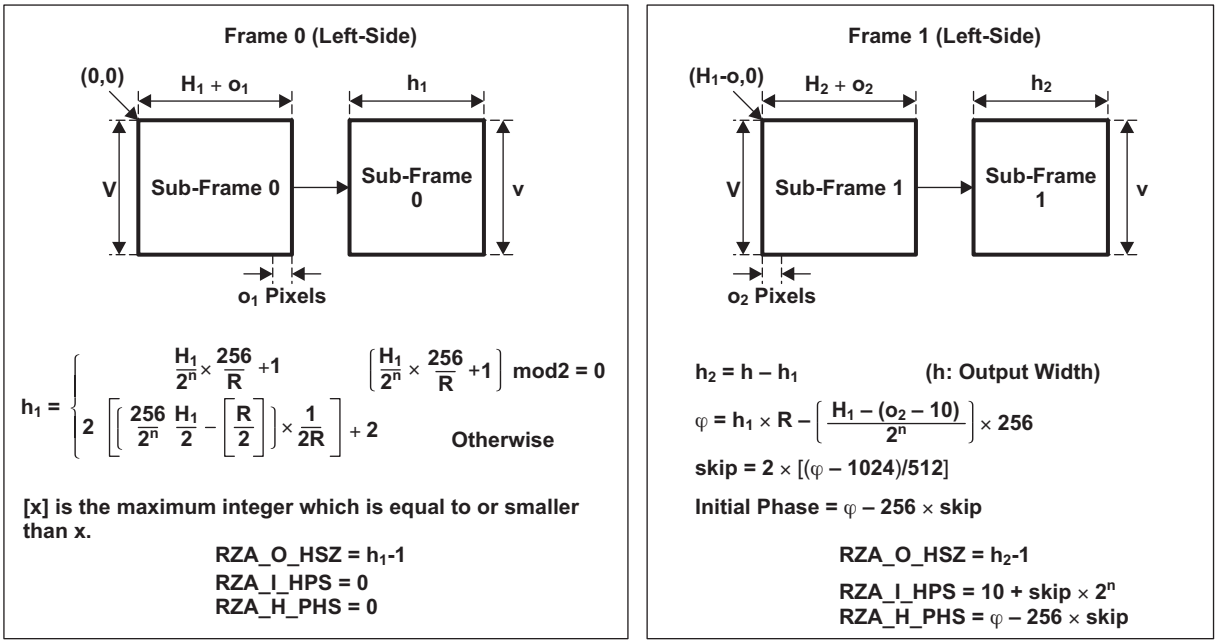
$$o \geq \begin{cases} 10+4 & if\left(\frac{H}{2}\frac{256}{R}+1\right) mod\ 2 = 0 \\ 10+4+2\ ceil\ (R/1024) & if\left(\frac{H}{2}\frac{256}{R}+1\right) mod\ 2 = 1 \end{cases}$$

The upper case, (10 + 4), is for the condition in which the resized image from frame-0 has an even numbered width. The lower case is for the condition in which the output has an odd numbered width. In this case, the Resizer needs to add an extra number of pixels to make the output width an even number.

5.6.6.1.3 Frame Division Mode – Resizing With Down-Scale Mode

If both IPIPE and Resizer in down-scale mode are applied, images are rescaled in the following way. Here, the scaling ratio is $\blacksquare^{n}$ 256/*R*, where *n* is the down-scale mode parameter. The image, as shown in Figure 126, is split into two frames with widths of H_1 and H_2, which need to be multiples of 2^{n+1}. For resize-B operation, RZA is replaced with RZB.

Figure 126. Resizer Parameters for Frame-0 (Left) and Frame-1 (Right) in Down-Scale Mode



The following numbers of pixels are consumed as border pixels. The input frames need to have extra pixels with these sizes.

$$o_1, o_2 \geq \begin{cases} 10 + 4 \times 2^n & if \left(\frac{H}{2} \frac{256}{R} \right) mod\ 2 = 0 \\ 10 + 4 \times 2^n + 2\ ceil\ (R/1024) \times 2^n & if \left(\frac{H}{2} \frac{256}{R} \right) mod\ 2 = 1 \end{cases}$$

5.6.7 Summary of Constraints

The following is a list of register configuration constraints to adhere to when programming the IPIPE. It can be used as a quick checklist. More detailed register setting constraints can be found in the individual register descriptions.

- The first input pixel should be the RED pixel in order for the register names to be aligned with the appropriate colors.
- Both the input and output widths should be ≤ 2176 pixels.
- RZB output width should be ≤ 1088 pixels.
- Input height and width should be ≤ ISIF module output height and width.
- Output width should be even.
- Each input line should have at least IPIPE_HSZ + 1 + 8 PCLK cycles.
- Each input frame should have at least IPIPE_VSZ + 1 + 10 HD pulses (+4 in continuous mode).
- Resize ratios are limited to the range from 1/16x scale down to 16x scale up.

5.7 Programming the LDC

This section discusses issues related to the software control of the LDC module. It lists which registers are required to be programmed in different modes, how to enable and disable the LDC, how to check the status of the LDC, discusses the different register access types, and enumerates several programming constraints.

5.7.1 Hardware Setup/Initialization

This section discusses the LDC configuration required before image processing can begin.

5.7.1.1 Reset Behavior

Upon VPSS hardware reset, all of the registers in the LDC are reset to their reset values. However, since the LDC programmable look-up table is stored in internal RAM, its contents do not have reset values. If the reset is a chip-level, power-on reset (reset applied after power is applied), then the contents of the table are unknown. If the reset is a VPSS module reset (when power remains active), then the contents of the table remain the same as before the reset.

5.7.1.2 Register Setup

Prior to enabling the LDC, the hardware must be properly configured via register writes. Table 64 identifies the register parameters that must be programmed before enabling the LDC.

Table 64. LDC Required Configuration Parameters

Function	Configuration Required
LDC Clock Enable	VPSS.VPBE_CLK_CTRL.LDC_CLK_ENABLE
Functional Mode	PCR.MODE
Frame Size	FRAME_SIZE
Source Information	RD_BASE RD_OFST
Source Information in 4:2:0 mode	420C_RD_BASE
Destination Information	WR_BASE WR_OFST
Destination Information in 4:2:0 mode	420C_WR_BASE
LDC LUT Memory access	VPSS.VPBE_CLK_CTRL.LDC_CLK_SEL
LDC Output to SDRAM	ISP.BCR.SRC_SEL_IPIPE_LDC

Table 65 identifies additional configuration requirements depending on whether the corresponding condition is met. The table can be read as:

if(**Condition** is TRUE), then **Configuration Required** parameters must be programmed

Table 65. LDC Conditional Configuration Parameters

Function	Condition	Configuration Required
LDC Parameters	PCR.MODE = 0,1,2	INITXY CONFIG CENTER KHV BLOCK LUT_ADDR LUT_WDATA LUT_RDATA AFFINE_AB AFFINE_CD AFFINE_EF Setup LDC Look-Up Table

5.7.1.3 Internal Memory Access

The LDC look-up table (stored in VPSS internal memory) can be accessed by either the ARM or LDC module configuration registers, depending on the VPSS.VPBE_CLK_CTRL.LDC_CLK_SEL register bit field. If the LDC module is configured to access the LDC LUT memory, then the memory can be accessed by the LUT_ADDR, LUT_WDATA, and LUT_RDATA registers. The LUT_ADDR register is used to set the LUT address pointer to which the access is needed.

5.7.1.3.1 Read/Write Procedures

When the LDC module has access to the LUT, the LDC internal memory values can be both written and read. There are three registers that allow for the memory contents to be read and written. The address register (LUT_ADDR) is used to select the specific table entry. The write data register (LUT_WDATA) can be used to write to the specified location. The read data register (LUT_RDATA) can be used to read from the specified location. The LDC supports linear increments on reads and writes automatically. The following example shows how the programmer can read/write the memory. If data is read/written, the address pointer is automatically incremented. For random/contiguous reads/writes, the LUT_ADDR register needs to be modified.

Example: Write all the entries of the table (using linear increment):

```
WRITE (LUT_ADDR, 0); for(I=0; i<768;i++) WRITE (LUT_WDATA, LUT[i]);
```

When ARM has access to the LUT, software has to take care of increment/decrement operations while accessing the LUT memory.

NOTE: Proper care has to be taken in setting the VPSS.VPBE_CLK_CTRL.LDC_CLK_SEL register bit field.

5.7.2 Enable/Disable Hardware

Setting the PCR.EN bit enables the LDC module. This should be done after all of the required registers mentioned in the previous section are programmed.

The LDC always operates in one-shot mode. The module cannot be disabled, but disables itself when processing of the current frame ends.

5.7.3 Events and Status Checking

The LDC generates the LDC event to the VPSS at the end of each frame. It is configured active.

5.7.4 Register Accessibility During Frame Processing

There is only one type of register access in the LDC module.

- **Busy-lock registers**:
  - Busy-lock registers cannot be written when the module is busy. Writes are allowed to occur, but no change occurs in the registers (blocked writes from hardware perspective, but allowed writes from software perspective). Once the busy bit in the PCR register is reset to 0, the busy-lock registers can be written.
  - All LDC registers belong to this category.

The ideal procedure for changing the LDC registers is:

```
IF (busy==0)OR IF (EOF interrupt occurs) CHANGE REGISTERS ENABLE LDC
```

5.7.5 Inter-Frame Operations

Since the LDC operates in one-shot mode only and the registers all have busy-lock access, there can be no modifications to the registers during frame processing. Software must wait until the completion of an LDC process before changing the registers to begin processing another frame.

5.7.5.1 Partial Frame Correction

The hardware can be utilized to process a portion of the image, rather than the whole image. This allows an image to process through multiple firmware/hardware interactions to correct only a portion of the image to save time.

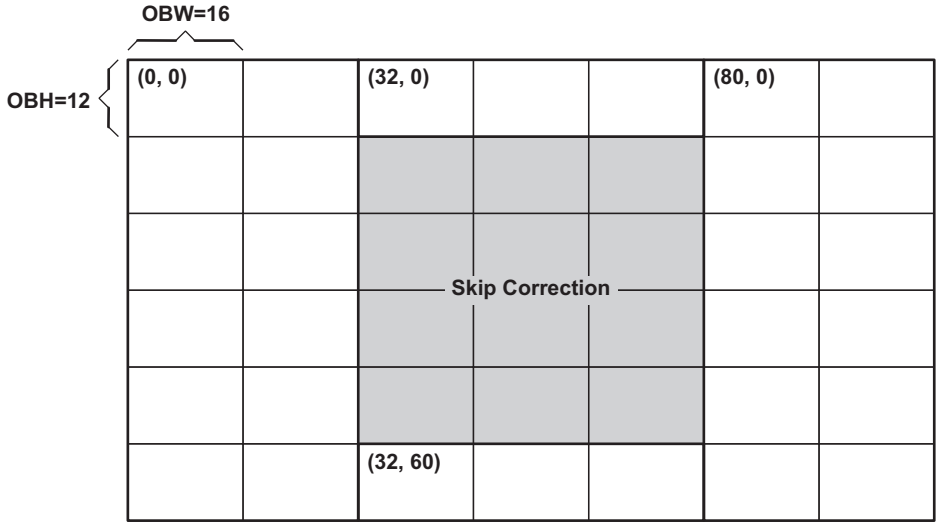
The following parameters are needed:

- InitX - X coordinate of upper-left corner of output frame
- InitY - Y coordinate of upper-left corner of output frame
- FrameW - Width of output frame

- FrameH - Height of output frame
- FrameBase - SDRAM address of upper-left corner of output frame
- FrameW should be a multiple of OBW (which is a multiple of 16), FrameH should be a multiple of OBH (which is even), and FrameBase should be a multiple of 32 (byte address)

Figure 127 shows an example of multiple-pass processing with the middle of the image being skipped.

Figure 127. Multiple-Pass Correction Example



InitX	InitY	FrameW	FrameH	WrFrameBase
0	0	32	72	0x10000
32	0	48	12	0x10040
80	0	32	72	0x100A0
32	60	48	12	0x134C0

The hardware does not copy skipped blocks from the input frame to the output frame (necessary task, unless output frame = input frame). It is the firmware's responsibility to set up and initiate this memory copy.

5.7.6 Summary of Constraints

The following is a list of register configuration constraints to adhere to when programming the LDC. It can be used as a quick checklist. More detailed register settings can be found in the individual register descriptions.

- All SDRAM addresses and offsets must be 32-byte aligned.
- OBH must be an even number.
- OBW must be a multiple of 16 pixels.
- The frame width and height must be multiples of OBW and OBH, respectively.
- The maximum frame width and height for a single pass is 4096 pixels.

5.8 Programming the H3A

This section discusses issues related to the software control of the H3A module. It lists which registers are required to be programmed in different modes, how to enable and disable the H3A, how to check the status of the H3A, discusses the different register access types, and enumerates several programming constraints.

5.8.1 Hardware Setup/Initialization

This section discusses the H3A configuration required before image processing can begin.

5.8.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the H3A are reset to their reset values.

5.8.1.2 Register Setup

For register configuration purposes, the H3A AF Engine and AEW Engine can be independently configured. There are separate enable bits for each engine, so this section is divided into the AF Engine and the AEW Engine.

5.8.1.2.1 AF Engine

Prior to enabling the AF Engine, the hardware must be properly configured via register writes. Table 66 identifies the register parameters that must be programmed before enabling the H3A AF Engine.

Table 66. AF Engine Required Configuration Parameters

Function	Configuration Required
AF Optional Preprocessing	PCR.AF_ALAW_EN PCR.AF_MED_EN
AF Mode Configuration	PCR.RGBPOS PCR.FVMODE
Paxel Start and Size Information	AFPAX1 AFPAX2 AFPAXSTART AFIIRSH
Memory Address	AFBUFST
Filter Coefficients	AFCOEF0[10:0] AFCOEF1[10:0]
Input Frame	LINE_START

Table 67 identifies additional configuration requirements depending on whether the corresponding condition is met. The table can be read as:

if(**Condition** is TRUE), then **Configuration Required** parameters must be programmed.

Table 67. AF Engine Conditional Configuration Parameters

Function	Condition	Configuration Required
Horizontal Median Filter	PCR.AF_MED_EN	PCR.MED_TH
Horizontal Focus Enable	PCR.AF_VF_EN = 0	HFV_THR
Both Horizontal and Vertical Focus Enable	PCR.AF_VF_EN = 1	VFV_CFG1 VFV_CFG2 VFV_CFG3 VFV_CFG4 HFV_THR

The following references offer guidelines on how to program the filter coefficients and make use of the H3A output:

- M. Gamadia, V. Peddigari, N. Kehtarnavaz, S-Y. Lee, G. Cook, *Real-time Implementation of Auto Focus on the TI DSC Processor*, Proceedings of SPIE Real-Time Imaging Conference, Jan 2004
- N. Kehtarnavaz, H-J. Oh, *Development and real-time implementation of a rule-based auto-focus algorithm*, Journal of Real-Time Imaging, 9, 197-203, 2003

5.8.1.2.2 AEW Engine

Prior to enabling the AEW Engine, the hardware must be properly configured via register writes. Table 45 identifies the register parameters that must be programmed before enabling the H3A AEW Engine.

Table 68. AEW Engine Required Configuration Parameters

Function	Configuration Required
AEW Optional Preprocessing	PCR.AEW_ALAW_EN
Saturation Limit	PCR.AVE2LMT
Window Start and Size Information	AEWIN1 AEWINSTART AEWINBLK AEWSUBWIN
Memory Address	AEWBUFST
Input Frame	LINE_START

5.8.2 Enable/Disable Hardware

Setting the PCR.AF_EN bit enables the AF Engine, and the PCR.AEW_EN bit enables the AEW Engine. This should be done after all of the required registers in the previous section are programmed.

The H3A input source is the Image Sensor Interface (ISIF) and processing of the frame is dependent upon the timing of the ISIF. In order to guarantee that data from the ISIF is not missed, the H3A should be enabled prior to the ISIF. In this way, the H3A waits for the data from the ISIF. The AF Engine or AEW Engine can be disabled by clearing the PCR.AF_EN or PCR.AEW_EN bit, respectively, during the processing of the last frame. The disable is latched in at the end of the frame it was written in.

5.8.3 Events and Status Checking

The H3A module generates three interrupts (or three events to the EDMA) to the interrupt controller. They are described as follows:

1. AF_INT - This interrupt is generated after the completion of auto-focus processing per frame.
2. AEW_INT - This interrupt is generated after the completion of auto-exposure/auto-white balance processing per frame.
3. H3A_INT - This interrupt is generated at the same time as the last process to finish for each frame. This means that the interrupt comes when both the AF and AEW processes are finished.

The PCR.BUSYAF and/or PCR.BUSYAEAWB status bits are set when the start of frame occurs (if the PCR.AF_EN and/or PCR.AEW_EN bits are 1 at that time). They are automatically reset to 0 at the end of processing a frame. The PCR.BUSYAF and/or PCR.BUSYAEAWB status bits may be polled to determine the end-of-frame status.

5.8.4 Register Accessibility During Frame Processing

There are two types of register access in the H3A module.

- **Shadow registers**:
  - These registers/fields can be read and written (if the field is writeable) at any time. However, the written values take effect only at the start of a frame. Note that reads still return the most recent write even though the settings are not used until the next start of frame.
  - The following registers are shadow registers in the H3A module:

AFPAX1
AFPAX2
AFPAXSTART
AFIIRSH
AEWIN10
AEWINSTART
AEWINBLK
AEWSUBWIN

AEWCFG

- **Busy-lock registers**:
  - Busy-lock registers cannot be written when the module is busy. Writes are allowed to occur, but no change occurs in the registers (blocked writes from the hardware perspective, but allowed writes from the software perspective). Once the busy bit in the PCR register is reset to 0, the busy-lock registers can be written.
  - All the registers EXCEPT the registers mentioned above as shadow registers, are busy-lock registers.

The ideal procedure for changing the H3A registers is:

```
IF (busy == 0) OR IF (EOF interrupt occurs) DISABLE AF or AE/AWB CHANGE REGISTERS ENABLE AF or
AE/AWB
```

5.8.5 Inter-Frame Operations

Between frames, it may be necessary to modify the memory pointers before processing the next frame. Since the PCR and memory pointer registers are shadowed, these modifications can take place any time before the end of the frame and the data gets latched in for the next frame. The host controller can perform these changes upon receiving an interrupt or an EDMA transfer can be programmed to make these changes upon receiving an event.

5.8.6 Summary of Constraints

The following is a list of register configuration constraints to adhere to when programming the H3A. It can be used as a quick checklist. More detailed register setting constraints can be found in the individual register descriptions.

- The H3A should not be enabled for Foveon formatted input.
- The output addresses must be on 64-byte boundaries.
- The maximum width is 4096 pixels per line.

AF Engine:

- The paxel horizontal start value must be greater than or equal to the IIR horizontal start position.
- The width and height of the paxels must be an even number.
- The minimum width of the auto focus paxel must be 8 pixels.
- Paxels cannot overlap the last pixel in a line.
- Paxels must be adjacent to one another.

AEW Engine:

- The width and height of the windows must be an even number.
- Sub-sampling windows can only start on even numbers.
- The minimum width of the AE/AWB windows must be 8 pixels.

5.9 Programming ISP/VPSS Subsystem Level Registers

This section discusses issues related to the ISP/VPSS software control subsystem level. The ISP/VPSS subsystem comprises the infrastructure data path switches, interrupt control muxing, and clock gating control within the VPSS. This section briefly lists which registers are required to be programmed in different configurations of the VPSS.

5.9.1 Hardware Setup/Initialization

This section discusses the configuration of the ISP and VPSS subsystems before image processing can begin.

5.9.1.1 Reset Behavior

Upon hardware reset of the VPSS, all of the registers in the ISP and VPSS register modules are reset to their reset values.

5.9.1.2 Register Setup

Prior to enabling the modules within the VPSS, the buffer logic hardware must be properly configured via register writes. Table 69 identifies the register parameters that must be programmed properly before enabling various modules. The items not bolded are optional, depending on whether the operational mode of the module requires the setting or not.

Table 69. ISP and VPSS Subsystem Required Configuration Parameters

Module	Configuration Required
ISIF	**ISP.PCCR.ISIF_CLK_ENABLE** ISP.BCR.SRC_SEL_ISIF_IPIPE
IPIPEIF	**ISP.PCCR.IPIPEIF_CLK_ENABLE**
IPIPE	**ISP.PCCR.IPIPE_CLK_ENABLE** ISP.BCR.SRC_SEL_ISIF_IPIPE (boxcar/ISIF) ISP.BCR.SRC_SEL_IPIPE_LDC (boxcar/LDC) **ISP.PCCR.RSZ_CLK_ENABLE**
LDC	**VPSS.VPBE_CLK_CTRL.LDC_CLK_ENABLE** **VPSS.VPBE_CLK_CTRL.LDC_CLK_SEL** ISP.BCR.SRC_SEL_IPIPE_LDC (boxcar/LDC)
H3A	**ISP.PCCR.H3A_CLK_ENABLE**

5.9.2 Event and Status Checking

The ISP/VPSS subsystem controls the selection of which module interrupts are routed to the ARM interrupt controller and EDMA event controllers using the ISP.INTSEL[3:1] and ISP.EVTSEL registers. The ISP.INTSTAT register can also be used to poll for events. For more details, see Section 3.2.

5.9.3 Inter-Frame Operations

Since the ISP and VPSS subsystem registers are busy-writeable, care must be taken when modifying any of these registers. It is recommended that affected modules be disabled while switching modes and modifying any of these registers.

5.9.4 Summary of Constraints

None noted.

5.10 Error Identification

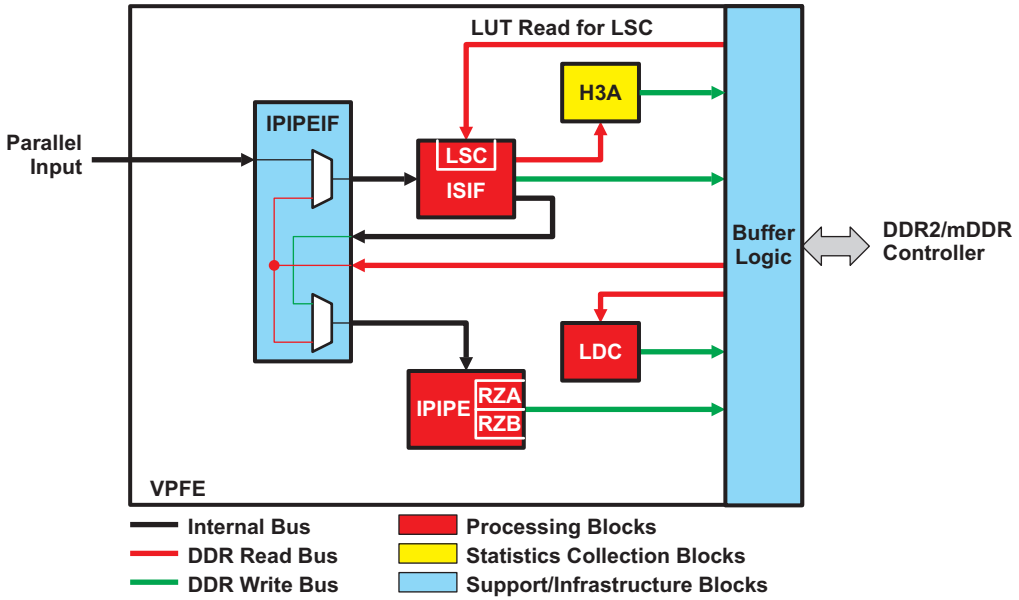
The modules that make use of hardware error identification and reporting are the ISIF (LSC) and IPIPEIF. To find more information about the error reporting registers and interrupts of these modules, see Section 5.4 and Section 5.5.

5.11 Supported Use Cases

The VPFE is designed to support a variety of video and imaging applications. For the purposes of describing the VPFE configuration for typical use cases, the application space can be divided into the following two input types: CCD/CMOS sensor data and YUV video data. This section discusses typical VPFE configurations for both of these input types separately and then discusses how both applications use the IPIPE Resizers to resize or change the aspect ration of processed video or image data.

Figure 128 shows all the possible data paths through the VPFE. Each mode described in this section has a unique data path through the various modules.

Figure 128. Data Paths Through the VPFE



5.11.1 CCD/CMOS Sensor Input Specific Applications

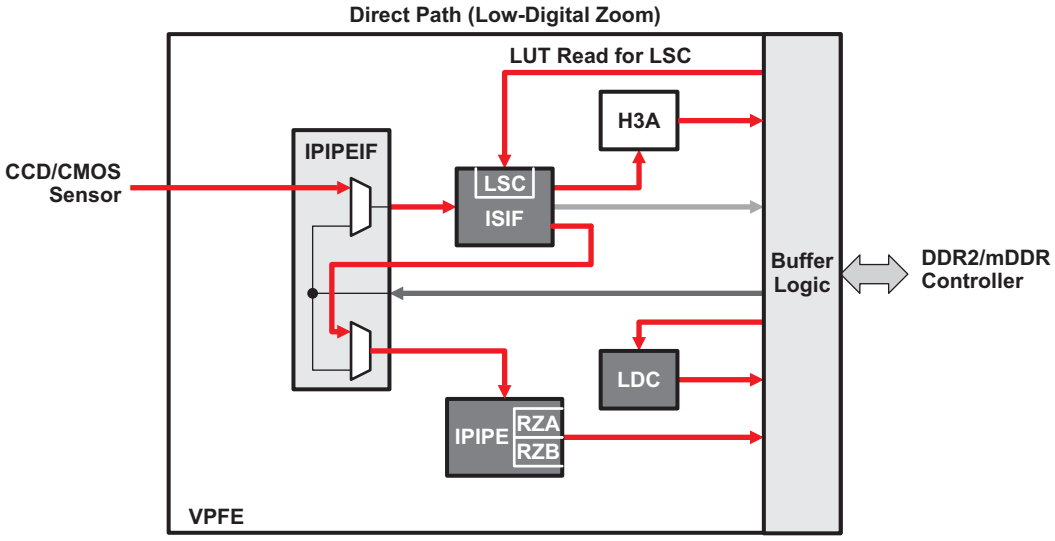
Digital still cameras and digital video cameras are the primary applications that use CCD or CMOS sensor input sources. CCD or CMOS sensors output analog data at a rate determined by a timing generator (TG). The analog front end (AFE) converts this data to a digital signal and transmits this digital raw sensor data to the input interface of the CCD controller. Depending on the sensor, this data is typically in a Bayer pattern where every pixel represents only one of the three primary colors (RGB) or their complementary colors (CYGM). The VPFE contains programmable functions that capture and digitally process this raw data into YUV-formatted video or image data that can be compressed or displayed directly on an external display.

In this application, there are three basic modes of operation that require different VPFE data paths and configurations: preview/movie capture mode, still image capture mode, and still image processing mode.

5.11.1.1 Preview/Movie Capture Mode

In a digital still camera or video camera, preview and movie capture modes are where the VPFE receives raw video data from the sensor, converts it to YUV format, and displays it on the display in real-time. There is only one distinguishing detail between preview mode and movie capture mode. In preview mode, the video data is only temporarily stored in a circular buffer in the SDRAM memory until it can be displayed and/or transmitted; in movie capture mode, the video data is additionally compressed and stored in non-volatile memory (for example, Flash, digital video tape, DVD, hard disk, and so on). Both modes have the same data path through the VPFE, as shown in Figure 129, except for one potential exception: for preview mode, only one resizer output of the IPIPE is required to resize the image display size; however, in movie capture mode, if the display size is different than the encoded movie size, then both resizers can be used to output these two sizes of the video (for example, display is VGA and MPEG encode is D1).

Figure 129. Preview/Movie Capture Data Paths



Register Field	Value
ISP.PCCR.ISIF_CLK_ENABLE	1
ISP.PCCR.IPIPEIF_CLK_ENABLE	1
ISP.PCCR.IPIPE_CLK_ENABLE	1
ISP.PCCR.RSZ_CLK_ENABLE	1
VPSS.VPBE_CLK_CTRL.LDC_CLK_ENABLE	1
ISP.PCCR.H3A_CLK_ENABLE	1
ISP.PCCR.BL_CLK_ENABLE	1
ISP.BCR.SRC_SEL_ISIF_IPIPE (ISIF/boxcar)	0
ISP.BCR.SRC_SEL_IPIPE_LDC (boxcar/LDC)	0

All of the modules may be enabled for this mode. The camera application spends the majority of its time in this mode, so the SDRAM bandwidth consumption is minimized by having a single image data path to memory (in addition to the H3A statistic data path) which is resized to the correct display size. The ARM can read the histogram information from the IPIPE memory-mapped registers after a frame has completed. Additionally, the ARM or an EDMA transfer can read the BSC vectors used for video stabilization from the IPIPE memory-mapped registers for each frame. LDC can be enabled for correction on each frame.

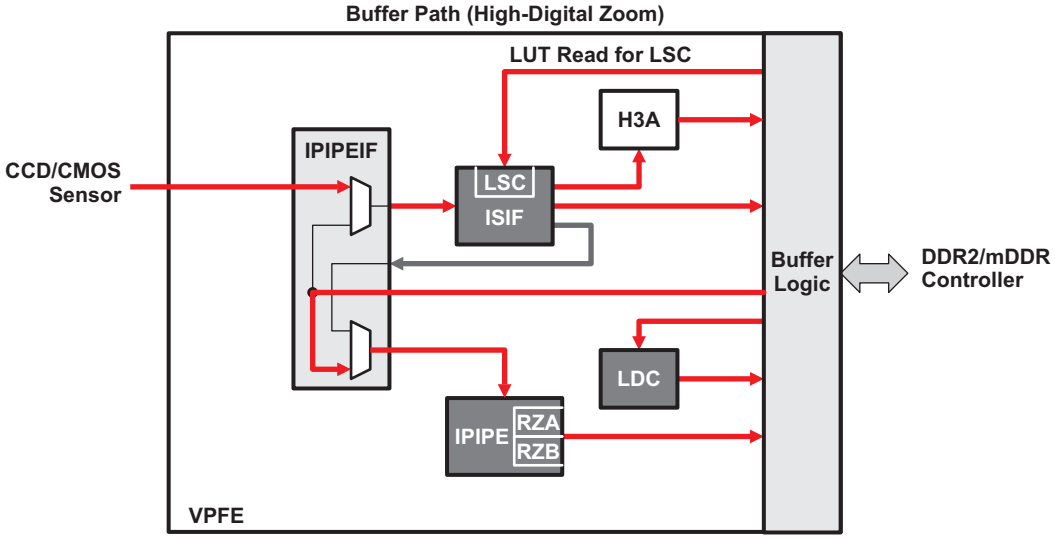
Note: For BOXCAR, LDC, and ISIF write ports, only two of them can be active at any time (see the ISP.BCR.SCR_SEL_ISIF_IPIPE and ISP.BCR.SRC_SEL_IPIPE_LDC registers).

Typically in this mode, the ISIF receives the digital raw data from the sensor/AFE in a down-sampled resolution format. Different sensors may have different readout patterns in this mode (e.g., draft mode, movie mode, VGA mode, etc.). The full 16-bit raw data is output to the IPIPEIF and the upper 10-bit raw data is output to the H3A module. The IPIPE performs most of the image signal processing (e.g., CFA interpolation, white balance, noise filtering, etc.) and converts the raw data to YUV 4:2:2/4:2:0 video format. If the input is not the correct size or aspect ration for display or storage and/or if digital zoom is required, then the IPIPE can output two separately resized outputs of the image concurrently. The image(s) output from the IPIPE sent to SDRAM in a circular buffer where they are consumed for display and/or compression. End-of-frame interrupts from the IPIPE and/or other VPFE modules can trigger ARM interrupt service routines to change the address of the write buffer in the IPIPE module for each frame. The image statistics from the H3A and IPIPE-embedded histogram can be used by the ARM for implementing algorithms to modify the image processing parameters of the IPIPE and/or focus lens of the imager for subsequent frames.

5.11.1.1.1 Digital Zoom Case

As the digital zoom factors increase, there may be a threshold where the IPIPE cannot process the data fast enough as per its requirement found in Section 4.3.20. At this point, the ISIF should send the cropped output to SDRAM instead of the IPIPE. Then, the IPIPE can read this data at a slower pixel clock defined by the IPIPEIF-divided clock and PPLN value. This rate can be made as slow as possible while still meeting the required frame rate so as to keep the instantaneous SDRAM bandwidth to a minimum. Additionally, DPCM compression can be utilized on the SDRAM path so that this bandwidth is reduced even further. This buffer path is shown in Figure 130.

Figure 130. Preview/Movie Capture Data Paths (Buffer Path)

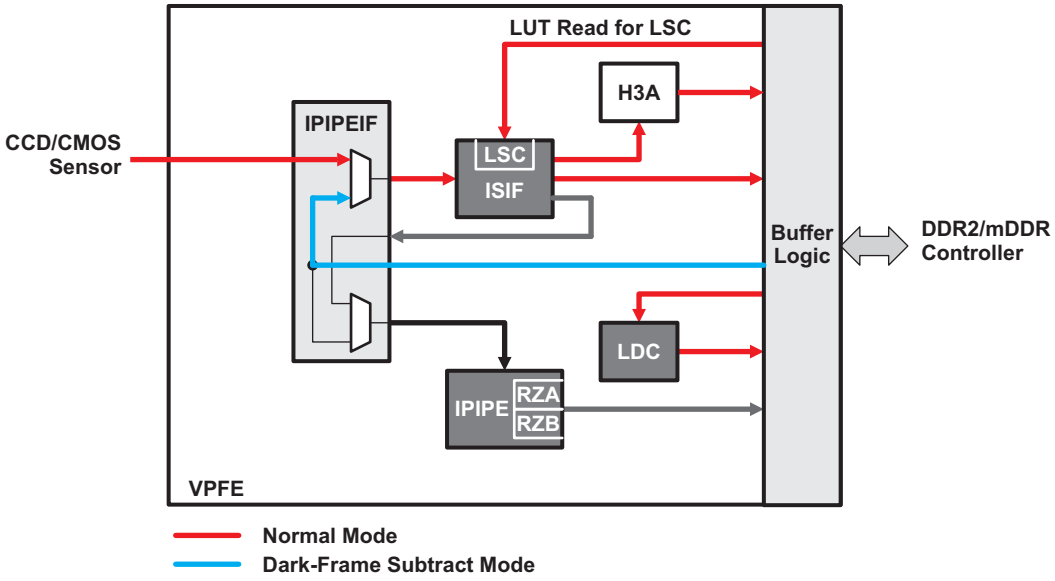


Register Field	Value
ISP.PCCR.ISIF_CLK_ENABLE	1
ISP.PCCR.IPIPEIF_CLK_ENABLE	1
ISP.PCCR.IPIPE_CLK_ENABLE	X
ISP.PCCR.RSZ_CLK_ENABLE	X
VPSS.VPBE_CLK_CTRL.LDC_CLK_ENABLE	1
ISP.PCCR.H3A_CLK_ENABLE	1
ISP.PCCR.BL_CLK_ENABLE	1
ISP.BCR.SRC_SEL_ISIF_IPIPE (ISIF/boxcar)	1 (ISIF o/p)
ISP.BCR.SRC_SEL_IPIPE_LDC (boxcar/LDC)	0 (LDC o/p)

5.11.1.1.2 Still Image Capture

In a digital still camera or video camera, still image capture is where the VPFE is receiving full resolution raw image data from the sensor and storing it to SDRAM to be analyzed, processed and/or later stored to non-volatile memory (e.g., flash, digital video tape, DVD, hard disk, and so on). The data path through the VPFE for still image capture is shown in Figure 131.

Figure 131. Raw Image Capture Data Path



Register Field	Value
ISP.PCCR.ISIF_CLK_ENABLE	1
ISP.PCCR.IPIPEIF_CLK_ENABLE	1
ISP.PCCR.IPIPE_CLK_ENABLE	X
ISP.PCCR.RSZ_CLK_ENABLE	X
VPSS.VPBE_CLK_CTRL.LDC_CLK_ENABLE	1
ISP.PCCR.H3A_CLK_ENABLE	1
ISP.PCCR.BL_CLK_ENABLE	1
ISP.BCR.SRC_SEL_ISIF_IPIPE (ISIF/boxcar)	1 (ISIF o/p)
ISP.BCR.SRC_SEL_IPIPE_LDC (boxcar/LDC)	0 (LDC o/p)

As shown in Figure 131, dark-frame subtract can be optionally enabled, depending on SDRAM bandwidth usage and sensor quality. Typically, in still capture mode, the ISIF receives the full resolution of the digital raw data from the sensor/AFE. Some sensors (typically CMOS) read the data out in progressive format, whereas other (typically CCD) read the data in multiple fields.

If the format is progressive, the ISIF can perform lens shading correction on the incoming image and the H3A can extract AEW parameters.

If the input format is field based, then software should set the line offset and starting address of the ISIF outputs accordingly so that the frame is de-interleaved as it is stored into SDRAM memory. Then, the LSC and/or AEW parameter extraction can later be done on the data from SDRAM.

If the image is 2176 pixels wide or less, it is possible for the output of the ISIF to go directly into the IPIPE instead of SDRAM. However, the data path shown in Figure 131 would be used most of the time for still image capture. This is because additional processing on the raw data may be required to improve the quality of the image, such as noise filtering and/or lens distortion correction (covered in the next section). Also, if the image width is greater than 2176 pixels, then this path is required so that the IPIPE can process the image in slices from SDRAM.

Lens distortion correction processing can be applied to the captured image in SDRAM in multiple turns or a single turn depending upon the captured image size.

5.11.1.1.3 Still Image Processing

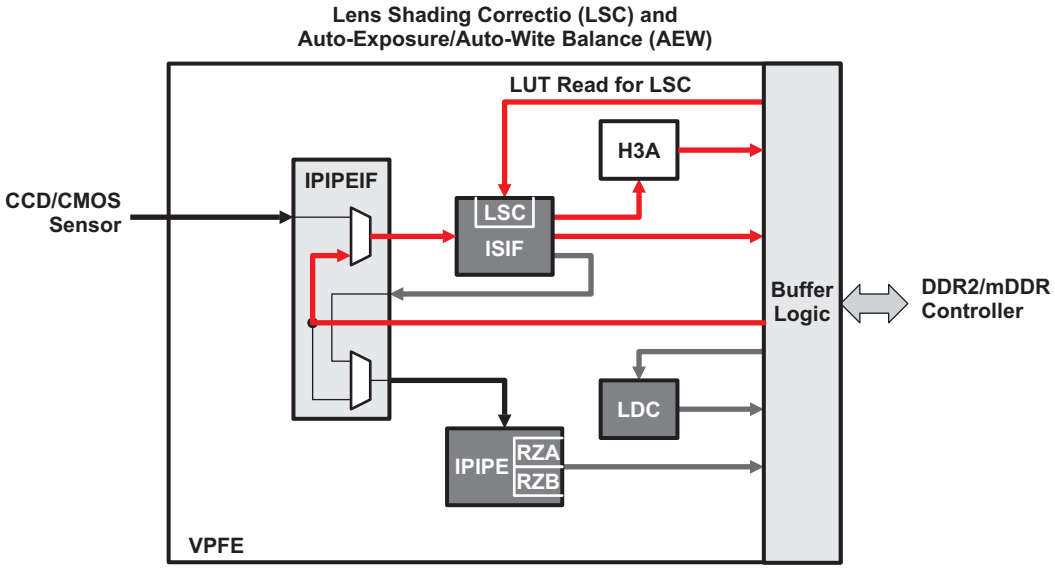
In a digital still camera or video camera, still image processing mode is when the raw image data that was captured to SDRAM during still capture mode is processed into YUV image data which can be later compressed and stored in non-volatile memory. The IPIPE performs most of the image processing steps required, including the raw-to-YUV processing, however, the VPFE in the DM36x is designed with additional raw image processing operations to further improve the quality of the final image. The next three sections describe optional steps and paths through the VPFE that can be taken to improve image quality; the fourth section describes the required final path of processing through the IPIPE.

NOTE: If the input format is progressive, then the step shown in the next section can be skipped since it should have already been done during image capture.

5.11.1.1.3.1 Lens Shading Correction (LSC) and Auto-Exposure/Auto-White (AEW) Balance Statistic Extraction

If the input was originally read out in fields and de-interleaved in SDRAM, the now-progressive raw data can pass from SDRAM through the ISIF with the LSC function enabled to perform a lens shading correction function on the image. Additionally, the output of the ISIF can pass through the H3A and AEW function to extract 2A information from the still image. The data path for this process step is shown in Figure 132.

Figure 132. Lens Shading Correction Data Path

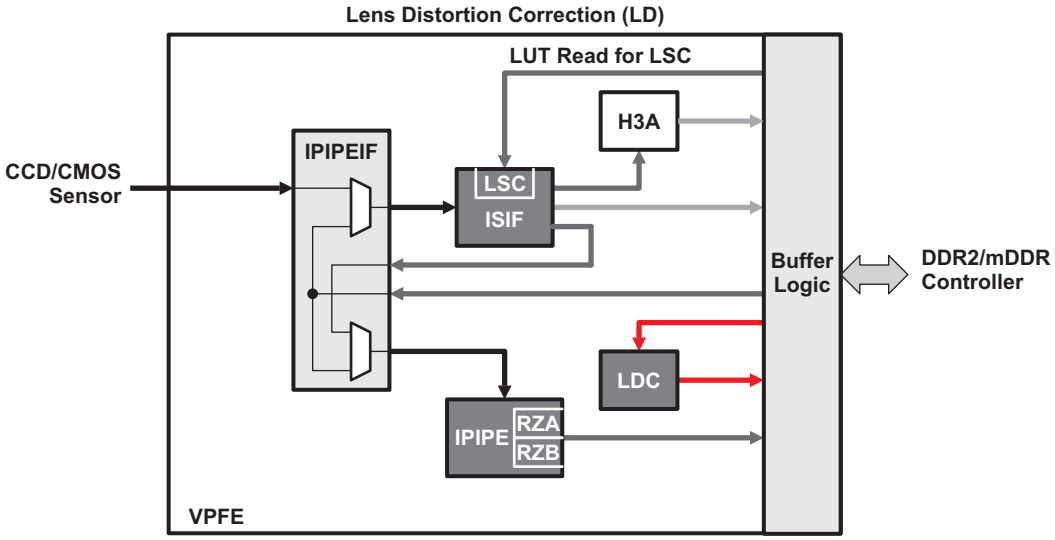


Register Field	Value
ISP.PCCR.ISIF_CLK_ENABLE	1
ISP.PCCR.IPIPEIF_CLK_ENABLE	1
ISP.PCCR.IPIPE_CLK_ENABLE	0
ISP.PCCR.RSZ_CLK_ENABLE	0
VPSS.VPBE_CLK_CTRL.LDC_CLK_ENABLE	0
ISP.PCCR.H3A_CLK_ENABLE	1
ISP.PCCR.BL_CLK_ENABLE	1
ISP.BCR.SRC_SEL_ISIF_IPIPE (ISIF/boxcar)	1 (ISIF o/p)
ISP.BCR.SRC_SEL_IPIPE_LDC (boxcar/LDC)	0 (LDC o/p)

5.11.1.1.3.2 Lens Distortion Correction (LDC)

Raw data captured in SDRAM can pass through the LDC with the LD function enabled to perform a lens distortion correction function on the image. The data path for this process step is shown in Figure 133.

Figure 133. Lens Distortion Correction Data Path

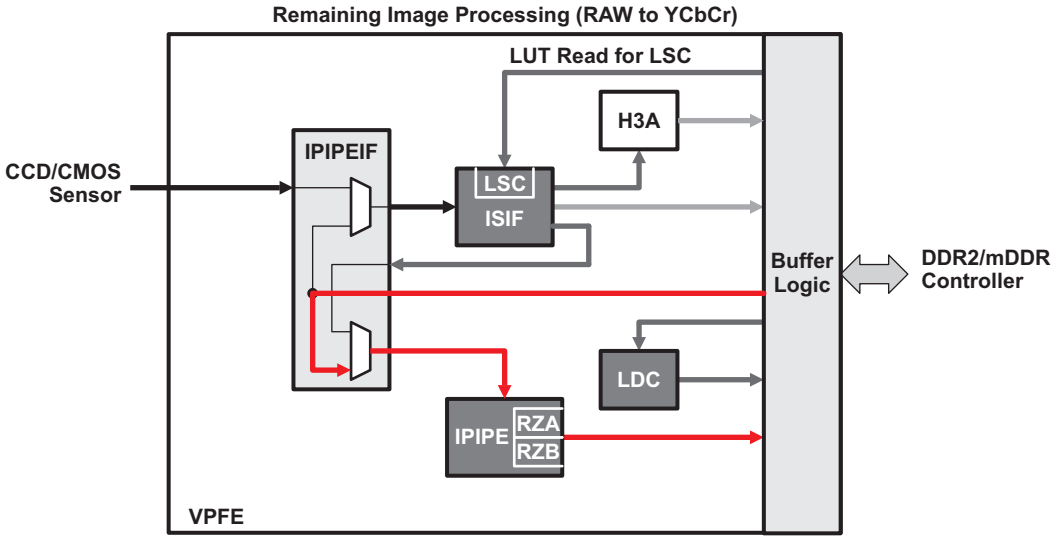


Register Field	Value
ISP.PCCR.ISIF_CLK_ENABLE	1
ISP.PCCR.IPIPEIF_CLK_ENABLE	1
ISP.PCCR.IPIPE_CLK_ENABLE	0
ISP.PCCR.RSZ_CLK_ENABLE	0
VPSS.VPBE_CLK_CTRL.LDC_CLK_ENABLE	0
ISP.PCCR.H3A_CLK_ENABLE	1
ISP.PCCR.BL_CLK_ENABLE	1
ISP.BCR.SRC_SEL_ISIF_IPIPE (ISIF/boxcar)	X
ISP.BCR.SRC_SEL_IPIPE_LDC (boxcar/LDC)	0 (LDC o/p)

5.11.1.1.3.3 Remaining Image Processing (Raw to YCbCr)

Raw data captured in SDRAM can pass through the IPIPE with the raw-to-YCbCr data path enabled to perform the remaining image processing functions on the image. The data path for this step is shown in Figure 134 . As the figures shows, both resizer outputs are enabled. Typically, one resizer would output the full resolution still image and the other resizer may output a *thumb-nail* or *screen-nail* image to be encoded for quick display during image playback.

Figure 134. Remaining Image Processing Data Path



Register Field	Value
ISP.PCCR.ISIF_CLK_ENABLE	0
ISP.PCCR.IPIPEIF_CLK_ENABLE	1
ISP.PCCR.IPIPE_CLK_ENABLE	1
ISP.PCCR.RSZ_CLK_ENABLE	1
VPSS.VPBE_CLK_CTRL.LDC_CLK_ENABLE	0
ISP.PCCR.H3A_CLK_ENABLE	0
ISP.PCCR.BL_CLK_ENABLE	1
ISP.BCR.SRC_SEL_ISIF_IPIPE (ISIF/boxcar)	X
ISP.BCR.SRC_SEL_IPIPE_LDC (boxcar/LDC)	1 (boxcar o/p)

Since the internal line memory is optimized for image resolutions of 5MP, the IPIPE can process a maximum output and input width of 2600 pixels in a single pass. Therefore, for images larger than 5MP, it required multiple passes through the IPIPE to process a full-resolution, still-captured image. This is done by partitioning the input image into multiple overlapping vertical slices and aligning the output in such a way that the processed image is seamlessly stitched together. We refer to this mode of the IPIPE as frame division mode - V.

In addition to vertical slicing, it may be required to perform horizontal slicing of the processing so that compression of the output image can be pipelined in parallel. This concept can be implemented in much the same way as the vertical slicing. We refer to this mode of the IPIPE as frame division mode - H. Frame division mode is explained in greater detail in Section 5.6.6.1.

5.11.2 YUV Video Input-Specific Applications

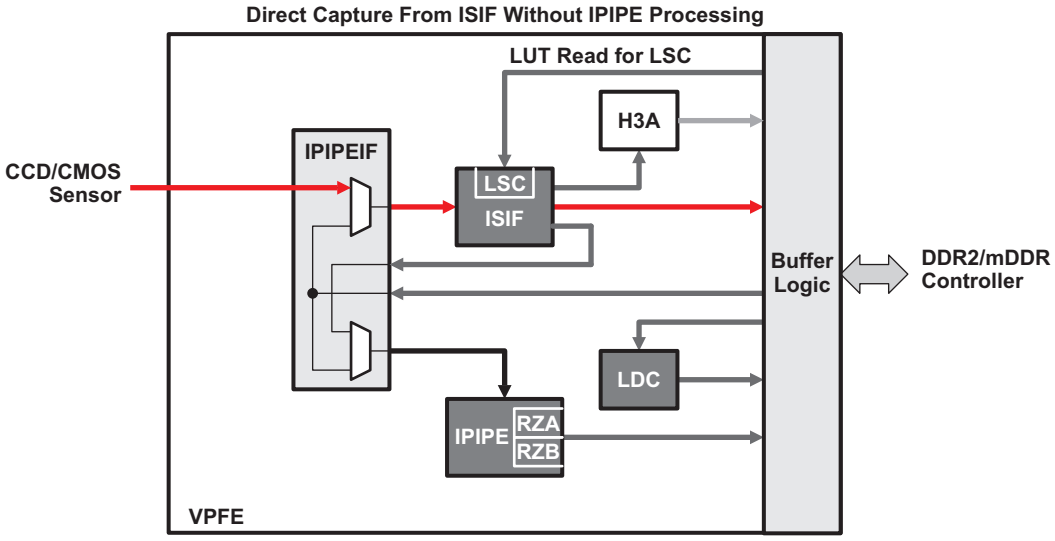
There are a variety of applications that use YUV video input sources: IP phones, video surveillance systems, and digital video recorders to name a few. Most any application that needs to capture YUV video, compress it, and transmit or store it can be included in this application category.

5.11.2.1 Video Capture Mode

Video capture mode is where the VPFE is receiving YUV video data from a digital video source and storing it to SDRAM for further processing and/or compression. On its input interface, the ISIF of the VPFE can capture BT.656-formatted video or generic 8- or 16-bit YUV digital video data from a digital video source such as an NTSC/PAL video decoder.

The possible data paths through the VPFE for video capture are shown in Figure 135.

Figure 135. Video Capture Data Path

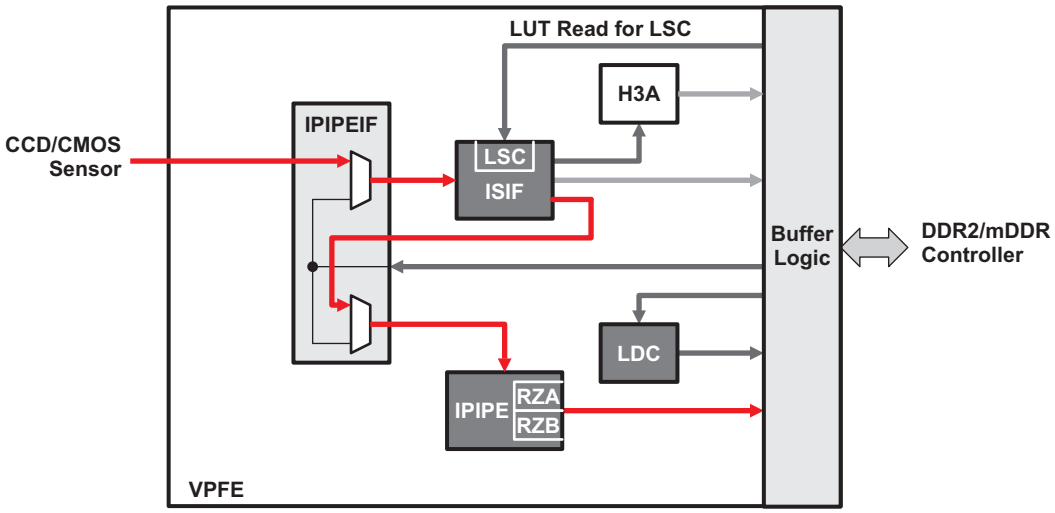


Register Field	Value
ISP.PCCR.ISIF_CLK_ENABLE	1
ISP.PCCR.IPIPEIF_CLK_ENABLE	1
ISP.PCCR.IPIPE_CLK_ENABLE	0
ISP.PCCR.RSZ_CLK_ENABLE	0
VPSS.VPBE_CLK_CTRL.LDC_CLK_ENABLE	0
ISP.PCCR.H3A_CLK_ENABLE	0
ISP.PCCR.BL_CLK_ENABLE	1
ISP.BCR.SRC_SEL_ISIF_IPIPE (ISIF/boxcar)	1 (ISIF o/p)
ISP.BCR.SRC_SEL_IPIPE_LDC (boxcar/LDC)	X

As Figure 136 shows, the ISIF module is the only module enabled for this mode.

The YUV data captured through ISIF can be passed to IPIPE for further processing or resizing and then stored into SDRAM as shown in Figure 136.

Figure 136. YUV Video Capture Data Path



Register Field	Value
ISP.PCCR.ISIF_CLK_ENABLE	1
ISP.PCCR.IPIPEIF_CLK_ENABLE	1
ISP.PCCR.IPIPE_CLK_ENABLE	1
ISP.PCCR.RSZ_CLK_ENABLE	1
VPSS.VPBE_CLK_CTRL.LDC_CLK_ENABLE	0
ISP.PCCR.H3A_CLK_ENABLE	0
ISP.PCCR.BL_CLK_ENABLE	1
ISP.BCR.SRC_SEL_ISIF_IPIPE (ISIF/boxcar)	X
ISP.BCR.SRC_SEL_IPIPE_LDC (boxcar/LDC)	1 (boxcar o/p)

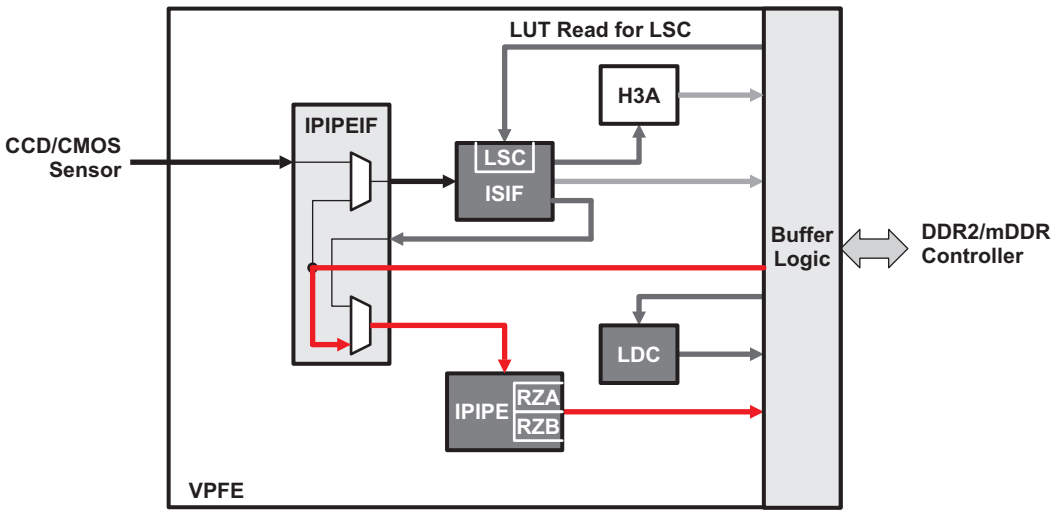
5.11.3 Video/Image Resize Applications

Application from both CCD/CMOS sensor data and YUV video data input categories use the resizers in the IPIPE to resize YUV 4:2:2-formatted video images from SDRAM.

5.11.3.1 Processed Image Resize

Processed image resize is where the resizers in the IPIPE take YUV-formatted image/video data from SDRAM and resize it back to SDRAM. Typically, the image coprocessors uncompress image or video data first and, then have the IPIPE resize the image to be displayed on a display device or recompressed again. Normally, only one resizer is required, but both can be used. The data path through the VPFE for video/image resize is shown in Figure 137.

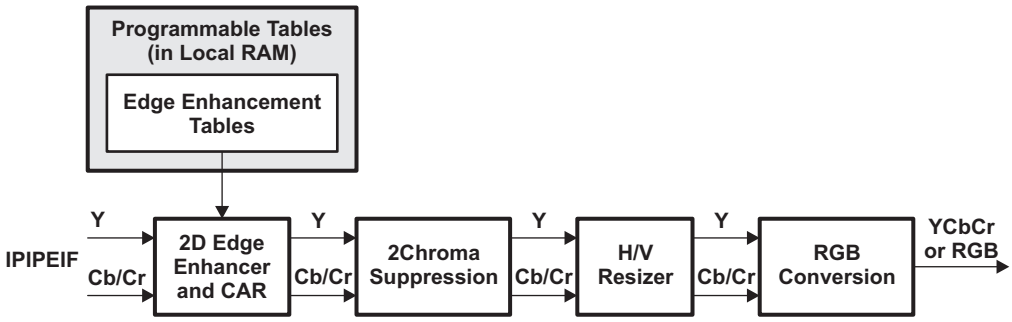
Figure 137. Processed Image Resize Data Path



Register Field	Value
ISP.PCCR.ISIF_CLK_ENABLE	0
ISP.PCCR.IPIPEIF_CLK_ENABLE	1
ISP.PCCR.IPIPE_CLK_ENABLE	1
ISP.PCCR.RSZ_CLK_ENABLE	1
VPSS.VPBE_CLK_CTRL.LDC_CLK_ENABLE	0
ISP.PCCR.H3A_CLK_ENABLE	0
ISP.PCCR.BL_CLK_ENABLE	1
ISP.BCR.SRC_SEL_ISIF_IPIPE (ISIF/boxcar)	X
ISP.BCR.SRC_SEL_IPIPE_LDC (boxcar/LDC)	1 (boxcar o/p)

Within the IPIPE, the YCbCr input skips the raw data processing and enters the final stages of the IPIPE, as shown in Figure 138.

Figure 138. YCbCr Input Resize Data Path in IPIPE



5.11.3.1.1 Multi-Pass Resize

There are two constraints in the IPIPE resizers that may require multiple passes in order to achieve a desired size:

1. Resize ratio range is limited to between 1/16x and 16x resize.
2. Maximum input/output width is 2176 pixels.

Resize ratio range: a single pass through the IPIPE can resize an image down to 1/16 or up to 16 times the input width and/or height. In order to achieve resize operations beyond this range, multiple passes through the IPIPE are required until the final sizing is achieved. For example, if a 1/20x resize is required, then a 1/10x resize and a 1/2x resize can be applied, in two passes.

Maximum output width: Since the internal line memory is optimized for video resolutions and still images up to 5MP, the IPIPE can operate on a maximum output/input width of 2176 pixels in a single pass. Therefore, it requires multiple passes through the IPIPE to resize to larger images that exceed this horizontal width requirement. This is done by partitioning the input image into multiple vertical slices and aligning the output is such a way that the processed image is seamlessly stitched together.

The basic idea is to begin subsequent slices at exactly where previous images left off. The starting phase and pixel registers can be programmed to this exact location. This location can be calculated using the algorithm details and examples in Section 5.6.6.1.

6 VPFE Registers

Table 70 lists the sub-modules associated with the VPFE subsystem.

Table 70. Video Processing Front End Sub-Module Register Map

Address: Offset	Acronym	Register Description	Section
0x01C7:1000	ISIF	Image Sensor Interface	Section 6.1
0x01C7:1200	IPIPEIF	Image Pipe Interface	Section 6.2
0x01C7:0800	IPIPE	Image Pipe	Section 6.3
0x01C7:0400	RSZ	Resizer	Section 6.4
0x01C7:1400	H3A	Hardware 3A	Section 6.5
0x01C7:1600	LDC	Lens Distortion Correction	Section 6.6
0x01C7:0000	ISP	ISP System Configuration	Section 6.7
0x01C7:0200	VPSS	VPSS System Configuration	Section 6.8

6.1 Image Sensor Interface (ISIF) Registers

Table 71 lists the memory-mapped registers for the Image Sensor Interface (ISIF). See the device-specific data manual for the memory address of these registers.

Table 71. Image Sensor Interface (ISIF) Registers

Offset	Acronym	Register Description	Section
0h	SYNCEN	Synchronization Enable	Section 6.1.1
004h	MODESET	Mode Setup	Section 6.1.2
008h	HDW	HD pulse width	Section 6.1.3
00Ch	VDW	VD pulse width	Section 6.1.4
010h	PPLN	Pixels per line	Section 6.1.5
014h	LPFR	Lines per frame	Section 6.1.6
018h	SPH	Start pixel horizontal	Section 6.1.7
01Ch	LNH	Number of pixels in line	Section 6.1.8
020h	SLV0	Start line vertical - field 0	Section 6.1.9
024h	SLV1	Start line vertical - field 1	Section 6.1.10
028h	LNV	Number of lines vertical	Section 6.1.11
02Ch	CULH	Culling - horizontal	Section 6.1.12
030h	CULV	Culling - vertical	Section 6.1.13
034h	HSIZE	Horizontal size	Section 6.1.14
038h	SDOFST	SDRAM Line Offset	Section 6.1.15
03Ch	CADU	SDRAM Address - high	Section 6.1.16
040h	CADL	SDRAM Address - low	Section 6.1.17
044h	LINCFG0	LINCFG0 - Linearization Mode Configuration	Section 6.1.18
048h	LINCFG1	LINCFG1 - Linearization Mode Configuration	Section 6.1.19
04Ch	CCOLP	CCD Color Pattern	Section 6.1.20
050h	CRGAIN	CCD Gain Adjustment - R/Ye	Section 6.1.21
054h	CGRGAIN	CCD Gain Adjustment - Gr/Cy	Section 6.1.22
058h	CGBGAIN	CCD Gain Adjustment - Gb/G	Section 6.1.23
05Ch	CBGAIN	CCD Gain Adjustment - B/Mg	Section 6.1.24
060h	COFSTA	CCD Offset Adjustment	Section 6.1.25
064h	FLSHCFG0	FLSHCFG0	Section 6.1.26
068h	FLSHCFG1	FLSHCFG1	Section 6.1.27

Table 71. Image Sensor Interface (ISIF) Registers (continued)

Offset	Acronym	Register Description	Section
06Ch	FLSHCFG2	FLSHCFG2	Section 6.1.28
070h	VDINT0	VD Interrupt #0	Section 6.1.29
074h	VDINT1	VD Interrupt #1	Section 6.1.30
078h	VDINT2	VD Interrupt #2	Section 6.1.31
080h	CGAMMAWD	Gamma Correction settings	Section 6.1.32
084h	REC656IF	CCIR 656 Control	Section 6.1.33
088h	CCDCFG	CCD Configuration	Section 6.1.34
08Ch	DFCCTL	Defect Correction - Control	Section 6.1.35
090h	VDFSATLV	Defect Correction - Vertical Saturation Level	Section 6.1.36
094h	DFCMEMCTL	Defect Correction - Memory Control	Section 6.1.37
098h	DFCMEM0	Defect Correction - Set V Position	Section 6.1.38
09Ch	DFCMEM1	Defect Correction - Set H Position	Section 6.1.39
0A0h	DFCMEM2	Defect Correction - Set SUB1	Section 6.1.40
0A4h	DFCMEM3	Defect Correction - Set SUB2	Section 6.1.41
0A8h	DFCMEM4	Defect Correction - Set SUB3	Section 6.1.42
0ACh	CLAMPCFG	Black Clamp configuration	Section 6.1.43
0B0h	CLDCOFST	DC offset for Black Clamp	Section 6.1.44
0B4h	CLSV	Black Clamp Start position	Section 6.1.45
0B8h	CLHWIN0	Horizontal Black Clamp configuration	Section 6.1.46
0BCh	CLHWIN1	Horizontal Black Clamp configuration	Section 6.1.47
0C0h	CLHWIN2	Horizontal Black Clamp configuration	Section 6.1.48
0C4h	CLVRV	Vertical Black Clamp configuration	Section 6.1.49
0C8h	CLVWIN0	Vertical Black Clamp configuration	Section 6.1.50
0CCh	CLVWIN1	Vertical Black Clamp configuration	Section 6.1.51
0D0h	CLVWIN2	Vertical Black Clamp configuration	Section 6.1.52
0D4h	CLVWIN3	Vertical Black Clamp configuration	Section 6.1.53
0D8h	DATAHOFST	H direction Data Offset	Section 6.1.54
0DCh	DATAVOFST	V direction Data Offset	Section 6.1.55
0E0h	LSCHVAL	HVAL for LSC	Section 6.1.56
0E4h	LSCVVAL	VVAL for LSC	Section 6.1.57
0E8h	2DLSCCFG	2D Lens Shading Correction Configuration	Section 6.1.58
0ECh	DDLSCOFST	2D LSC Gain Table Offset	Section 6.1.59
0F0h	DDLSCINI	2D LSC Initial Position	Section 6.1.60
2F4h	DDLSCGRBU	2D LSC Gain Table A2Dress base (Upper)	Section 6.1.61
0F8h	DDLSCGRBL	2D LSC Gain Table A2Dress base (Lower)	Section 6.1.62
0FCh	DDLSCGROF	2D LSC Gain Table offset	Section 6.1.63
100h	DDLSCORBU	2D LSC Offset Table A2Dress base (Upper)	Section 6.1.64
104h	DDLSCORBL	2D LSC Offset Table A2Dress base (Lower)	Section 6.1.65
108h	DDLSCOROF	2D LSC Offset Table offset	Section 6.1.66
10Ch	DDLSCIRQEN	2D LSC Interrupt Request Enable	Section 6.1.67
110h	DDLSCIRQST	2D LSC Interrupt Request Status	Section 6.1.68
114h	FMTCFG	CCD Formatter configuration	Section 6.1.69
118h	FMTPLEN	CCD Formatter - Program Entries	Section 6.1.70
11Ch	FMTSPH	CCD Formatter - Start pixel horizontal	Section 6.1.71
120h	FMTLNH	CCD Formatter - number of pixels	Section 6.1.72
124h	FMTSLV	CCD Formatter - start line vertical	Section 6.1.73
128h	FMTLNV	CCD Formatter - number of lines	Section 6.1.74

Table 71. Image Sensor Interface (ISIF) Registers (continued)

Offset	Acronym	Register Description	Section
12Ch	FMTRLEN	CCD Formatter - Read out line length	Section 6.1.75
130h	FMTHCNT	CCD Formatter - HD cycles	Section 6.1.76
134h	FMTAPTR0	CCD Formatter - Address pointer	Section 6.1.77
138h	FMTAPTR1	CCD Formatter - Address pointer	Section 6.1.78
13Ch	FMTAPTR2	CCD Formatter - Address pointer	Section 6.1.79
140h	FMTAPTR3	CCD Formatter - Address pointer	Section 6.1.80
144h	FMTAPTR4	CCD Formatter - Address pointer	Section 6.1.81
148h	FMTAPTR5	CCD Formatter - Address pointer	Section 6.1.82
14Ch	FMTAPTR6	CCD Formatter - Address pointer	Section 6.1.83
150h	FMTAPTR7	CCD Formatter - Address pointer	Section 6.1.84
154h	FMTAPTR8	CCD Formatter - Address pointer	Section 6.1.85
158h	FMTAPTR9	CCD Formatter - Address pointer	Section 6.1.86
15Ch	FMTAPTR10	CCD Formatter - Address pointer	Section 6.1.87
160h	FMTAPTR11	CCD Formatter - Address pointer	Section 6.1.88
164h	FMTAPTR12	CCD Formatter - Address pointer	Section 6.1.89
168h	FMTAPTR13	CCD Formatter - Address pointer	Section 6.1.90
16Ch	FMTAPTR14	CCD Formatter - Address pointer	Section 6.1.91
170h	FMTAPTR15	CCD Formatter - Address pointer	Section 6.1.92
174h	FMTPGMVF0	CCD Formatter - Program Valid Flags #0	Section 6.1.93
178h	FMTPGMVF1	CCD Formatter - Program Valid Flags #1	Section 6.1.94
17Ch	FMTPGMAPU0	CCD Formatter - Program Address Pointer #0	Section 6.1.95
180h	FMTPGMAPU1	CCD Formatter - Program Address Pointer #0	Section 6.1.96
184h	FMTPGMAPS0	CCD Formatter - Program Address Pointer select	Section 6.1.97
188h	FMTPGMAPS1	CCD Formatter - Program Address Pointer select	Section 6.1.98
18Ch	FMTPGMAPS2	CCD Formatter - Program Address Pointer select	Section 6.1.99
190h	FMTPGMAPS3	CCD Formatter - Program Address Pointer select	Section 6.1.100
194h	FMTPGMAPS4	CCD Formatter - Program Address Pointer select	Section 6.1.101
198h	FMTPGMAPS5	CCD Formatter - Program Address Pointer select	Section 6.1.102
19Ch	FMTPGMAPS6	CCD Formatter - Program Address Pointer select	Section 6.1.103
1A0h	FMTPGMAPS7	CCD Formatter - Program Address Pointer select	Section 6.1.104
1A4h	CSCCTL	Color Space Converter Enable	Section 6.1.105
1A8h	CSCM0	Color Space Converter - Coefficients #0	Section 6.1.106
1ACh	CSCM1	Color Space Converter - Coefficients #1	Section 6.1.107
1B0h	CSCM2	Color Space Converter - Coefficients #2	Section 6.1.108
1B4h	CSCM3	Color Space Converter - Coefficients #3	Section 6.1.109
1B8h	CSCM4	Color Space Converter - Coefficients #4	Section 6.1.110
1BCh	CSCM5	Color Space Converter - Coefficients #5	Section 6.1.111
1C0h	CSCM6	Color Space Converter - Coefficients #6	Section 6.1.112
1C4h	CSCM7	Color Space Converter - Coefficients #7	Section 6.1.113

6.1.1 Synchronization Enable (SYNCEN)

The synchronization enable (SYNCEN) register is shown in Figure 139 and described in Table 72.

Figure 139. Synchronization Enable (SYNCEN) Register

31-16		
Reserved		
R-0		
15-2	**1**	**0**
Reserved	DWEN	SYEN
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 72. Synchronization Enable (SYNCEN) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	DWEN		Data Write Enable Controls whether or not CCD raw data is written to SDRAM. This bit is latched by VD.
		0	Disable
		1	Enable
0	SYEN		VD/HD Enable If VD/HD are defined as output, activates internal timing generator. If VD/HD are defined as inputs, activates internal timing generator to synchronize with VD/HD.
		0	Disable
		1	Enable

6.1.2 Mode Setup (MODESET)

The mode setup (MODESET) register is shown in Figure 140 and described in Table 73.

Figure 140. Mode Setup (MODESET) Register

31-16							
Reserved							
R-0							
15	14	13-12		11	10-8		
MDFS	HLPF	INPMOD		Reserved	CCDW		
R-0	R/W-0	R/W-2h		R-0	R/W-0		
7	6	5	4	3	2	1	0
CCMD	DPOL	SWEN	FIPOL	HDPOL	VDPOL	FIDD	HDVDD
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 73. Mode Setup (MODESET) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15	MDFS		Field Status
		0	Odd field
		1	Even field
14	HLPF		3_tap Low_Pass (anti_aliasing) Filter 1/4, 1/2, 1/4 filtering applied to CCD data. This bit is latched by VD
		0	Off
		1	On
13-12	INPMOD		Data input mode
		0	CCD RAW data
		1h	YCbCr 16-bit
		2h	YCbCr 8-bit
		3h	Reserved
11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-8	CCDW		CCD RAW Data Right Shift for Data Written to SDRAM valid only when INPMOD is set to '0'
		0	No shift
		1h	1-bits
		2h	2-bits
		3h	3-bits
		4h	4-bits
		5h-7h	Reserved
7	CCDMD		Sensor Field Mode. This bit should not be set if the External Write Enable bit is set.
		0	NoR-0interlaced (progressive)
		1	Interlaced
6	DPOL		CCD input Data Polarity
		0	Normal (no change)
		1	1's complement
5	SWEN		External WEN Selection When set to 1 and when ENABLE is set to 1, the external WEN signal is used as the external memory write enable (to SDRAM/DDRAM). The data is stored to memory only when the external sync (HD and VD) signals are active. This bit should not be set if the C_WE_Field bit is set.
		0	Do not use external WEN (Write Enable)
		1	Use external WEN (Write Enable)

Table 73. Mode Setup (MODESET) Field Descriptions (continued)

Bit	Field	Value	Description
4	FIPOL		Field Indicator Polarity
		0	Positive
		1	Negative
3	HDPOL		HD Sync Polarity
		0	Positive
		1	Negative
2	VDPOL		VD Sync Polarity
		0	Positive
		1	Negative
1	FIDD		Field ID Signal Direction
		0	Input
		1	Output
0	HDVDD		VD/HD Sync Direction
		0	Input
		1	Output

6.1.3 HD Pulse Width (HDW)

The HD pulse width (HDW) register is shown in Figure 141 and described in Table 74.

Figure 141. HD Pulse Width (HDW) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	HDW
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 74. HD Pulse Width (HDW) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	HDW	0-FFFh	Width of HD sync pulse if output: HDW+1 pixel clocks HDWIDTH is not used when HD is input, i.e., when VDHDOUT in MODESET is cleared to '0'. This bit field is latched by VD.

6.1.4 VD Pulse Width (VDW)

The VD pulse width (VDW) register is shown in Figure 142 and described in Table 75.

Figure 142. VD Pulse Width (VDW) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VDW
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 75. VD Pulse Width (VDW) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VDW	0-FFFh	Width of VD sync pulse if output: VDW+1 lines VDWIDTH is not used when VD is input (i.e. when VDHDOUT in MODESET is cleared to 0). This bit field is latched by VD.

6.1.5 Pixels Per Line (PPLN)

The pixels per line(PPLN) register is shown in Figure 143and described in Table 76.

Figure 143. Pixels Per Line (PPLN) Register

31-16
Reserved
R-0
15-0
PPLN
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 76. Pixels Per Line (PPLN) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	PPLN	0-FFFFh	Pixels per line Number of pixel clock periods in one line HD period = PPLN+1 pixel clocks PPLN is not used when HD and VD are inputs(i.e., when VDHDOUT in MODESET is cleared to '0). This bit field is latched by VD.

6.1.6 Lines Per Frame (LPFR)

The lines per frame register (LPFR) is shown in Figure 144 and described in Table 77.

Figure 144. Lines Per Frame (LPFR) Register

31-16
Reserved
R-0
15-0
LPFR
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 77. Lines Per Frame (LPFR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	LPFR	0-FFFFh	Half lines per filed or frame Sets number of half lines per frame or field. VD period = (LPFR+1)/2 lines. LPFR is not used when HD and are inputs, i.e., when VDHDOUT in MODESET is cleared to 0. This bit field is latched by VD.

6.1.7 Start Pixel Horizontal (SPH)

The start pixel horizontal (SPH) register is shown in Figure 145and described in Table 78.

Figure 145. Start Pixel Horizontal (SPH) Register

31-16
Reserved
R-0

15	14-0
Rsvd	SPH
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 78. Start Pixel Horizontal (SPH) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	SPH	0-7FFFh	Start pixel, horizontal. Sets pixel clock position at which data output to SDRAM begins, measured from the start of HD. This bit field is latched by VD.

6.1.8 Number of Pixels in Line (LNH)

The number of pixels in line (LNH) register is shown in Figure 146 and described in Table 79.

Figure 146. Number of Pixels in Line (LNH) Register

31-16
Reserved
R-0

15	14-0
Rsvd	LNH
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 79. Number of Pixels in Line (LNH) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	LNH	0-7FFFh	Number of pixels in line Sets number of horizontal pixels that will be output to SDRAM = (LNH + 1) '&' 0xFFF0, i.e. the number of horizontal output pixels is truncated to multiples of 16. This bit field is latched by VD.

6.1.9 Start Line Vertical - Field 0 (SLV0)

The start line vertical - field 0 (SLV0) register is shown in Figure 147and described in Table 80.

Figure 147. Start Line Vertical - Field 0 (SLV0) Register

31-16
Reserved
R-0

15	14-0
Rsvd	SLV0
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 80. Start Line Vertical - Field 0 (SLV0) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	SLV0	0-7FFFh	Start Line, Vertical (Field 0) Sets line at which data output to SDRAM will begin, measured from the start of VD. This bit field is latched by VD.

6.1.10 Start Line Vertical - Field 1(SLV1)

The start line vertical - field 1 (SLV1) register is shown in Figure 148 and described in Table 81.

Figure 148. Start Line Vertical - Field 1 (SLV1) Register

31-16
Reserved
R-0

15	14-0
Rsvd	SLV1
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 81. Start Line Vertical - Field 1 (SLV1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	SLV1	0-7FFFh	Start Line, Vertical (Field 1) Sets line at which data output to SDRAM will begin, measured from the start of VD. This bit field is latched by VD.

6.1.11 Number of Lines Vertical (LNV)

The number of lines vertical (LNV) register is shown in Figure 149 and described in Table 82.

Figure 149. Number of Lines Vertical (LNV) Register

31-16
Reserved
R-0

15	14-0
Rsvd	LNV
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 82. Number of Lines Vertical (LNV) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	LNV	0-7FFFh	Number of vertical lines. Sets number of vertical lines that will be output to SDRAM. The number of lines output to SDRAM = (LNV + 1). This bit field is latched by VD.

6.1.12 Culling Horizontal (CULH)

The culling horizontal (CULH) register is shown in Figure 150 and described in Table 83.

Figure 150. Culling Horizontal (CULH) Register

31-16
Reserved
R-0

15-8	7-0
CLHE	CLHO
R/W-255	R/W-255

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 83. Culling Horizontal (CULH) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CLHE	0-FFh	Horizontal Culling Pattern for Even Line when writing to SDRAM, 8-bit mask: 0: cull, 1:retain LSB is first pixel, MSB is 8th pixel, then pattern repeats. This bit field is latched by VD
7-0	CLHO	0-FFh	Horizontal Culling Pattern for Odd Line when writing to SDRAM, 8-bit mask: 0: cull, 1:retain LSB is first pixel, MSB is 8th pixel, then pattern repeats. This bit field is latched by VD

6.1.13 Culling Vertical (CULV)

The culling vertical (CULV) register is shown in Figure 151 and described in Table 84.

Figure 151. Culling Vertical (CULV) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	CULV
R-0	R/W-255

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 84. Culling Vertical (CULV) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	CULV	0-FFh	Vertical Culling Pattern, 8-bit mask: 0: cull, 1:retain LSB is first line, MSB is 8th line, then pattern repeats. This bit field is latched by VD

6.1.14 Horizontal Size (HSIZE)

The horizontal size (HSIZE) register is shown in Figure 152 and described in Table 85 .

Figure 152. Horizontal Size (HSIZE) Register

31-16
Reserved
R-0

15-13	12	11-0
Reserved	ADCR	HSIZE
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 85. Horizontal Size (HSIZE) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12	ADCR		SDRAM address update. By setting this bit, SDRAM address in a line is automatically decreased so that a line can be Horizontally flipped in the SDRAM.
		0	Address increment
		1	Address decrement
11-0	HSIZE	0-FFFh	Address offset for each line. Sets size of line in SDRAM, units: 32 bytes Either 16 or 32 pixels depending on setting of PACK8. This bit field is latched by VD.

6.1.15 SDRAM Line Offset (SDOFST)

The SDRAM line offset (SDOFST) register is shown in Figure 153 and described in Table 86.

Figure 153. SDRAM Line Offset (SDOFST) Register

31-16						
Reserved						
R-0						
15	14	13-12	11-9	8-6	5-3	2-0
Rsvd	FIINV	FOFST	LOFTS0	LOFTS1	LOFTS2	LOFTS3
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 86. SDRAM Line Offset (SDOFST) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14	FIINV		Field identification signal inverse. This field is latched by VD
		0	Non inverse
		1	Inverse
13-12	FOFST		Field line offset value of odd field (FID = 1). This field is latched by VD
		0	+1 line
		1h	+2 line
		2h	+3 line
		3h	+4 line
11-9	LOFTS0		Line offset values of even line and even field (FID = 0). This field is latched by VD
		0	+1 line
		1h	+2 lines
		2h	+3 lines
		3h	+4 lines
		4h	-1 line
		5h	-2 lines
		6h	-3 lines
		7h	-4 lines
8-6	LOFTS1		Line offset values of odd line and even field (FID = 0). This bit is latched by VD.
		0	+1 line
		1h	+2 lines
		2h	+3 lines
		3h	+4 lines
		4h	-1 line
		5h	-2 lines
		6h	-3 lines
		7h	-4 lines
5-3	LOFTS2		Line offset values of even line and odd field (FID = 1). This bit is latched by VD.
		0h	+1 line
		1h	+2 lines
		2h	+3 lines
		3h	+4 lines
		4h	-1 line
		5h	-2 lines
		6h	-3 lines
		7h	-4 lines

Table 86. SDRAM Line Offset (SDOFST) Field Descriptions (continued)

Bit	Field	Value	Description
2-0	LOFTS3		Line offset values of odd line and odd field (FID = 1). This bit is latched by VD.
		0	+1 line
		1h	+2 lines
		2h	+3 lines
		3h	+4 lines
		4h	-1 line
		5h	-2 lines
		6h	-3 lines
		7h	-4 lines

6.1.16 SDRAM Address - High (CADU)

The SDRAM address-high (CADU-S) register is shown in Figure 154and described in Table 87.

Figure 154. SDRAM Address-High (CADU) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	CADU
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 87. SDRAM Address-High (CADU) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	CADU	0-7FFh	Upper 11 bits of the SDRAM starting address for ISIF output The address is specified offset from the SDRAM base address in units of 32 bytes. This bit field is latched by VD.

6.1.17 SDRAM Address - Low (CADL)

The SDRAM address-low (CADL) register is shown in Figure 155 and described in Table 88.

Figure 155. SDRAM Address-Low (CADL) Register

31-16
Reserved
R-0

15-0
CADL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 88. SDRAM Address-Low (CADL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	CADL	0-FFFFh	Lower 16 bits of the SDRAM starting address for ISIF output The address is specified offset from the SDRAM base address in units of 32 bytes. This bit field is latched by VD.

6.1.18 Linearization Mode Config (LINCFG0) Register

The linearization mode config (LINCFG0) register is shown in Figure 156 and described in Table 89.

Figure 156. Linearization Mode Config (LINCFG0) Register

31-16
Reserved
R-0

15-7	6-4	3-1	0
Reserved	CORRSFT	Reserved	LINEN
R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 89. Linearization Mode Config (LINCFG0) Field Descriptions

Bit	Field	Value	Description
31-7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6-4	CORRSFT		Shift up value for the correction value (S10)
		0	no shift
		1h	1bit left shift
		2h	2bit left shift
		3h	3bit left shift
		4h	4bit left shift
		5h	5bit left shift
		6h	6bit left shift
		7h	Reserved
3-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	LINEN		Linearization Enable
		0	Disable
		1	Enable

6.1.19 Linearization Mode Config (LINCFG1)

The linearization mode config (LINCFG1) register is shown in Figure 157 and described in Table 90.

Figure 157. Linearization Mode Config (LINCFG1) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	LUTSCL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 90. Linearization Mode Config (LINCFG1) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	LUTSCL	0-7FFh	Scale factor (U11Q10) for LUT input. Range: 0 - 1+1023/1024

6.1.20 CCD Color Pattern (CCOLP)

The CCD color pattern (CCOLP) register is shown in Figure 158 and described in Table 91.

Figure 158. CCD Color Pattern (CCOLP) Register

31-16							
Reserved							
R-0							
15-14	13-12	11-10	9-8	7-6	5-4	3-2	1-0
CP17_6	CP15_4	CP13_2	CP11_0	CP07_6	CP05_4	CP03_2	CP01_0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 91. CCD Color Pattern (CCOLP) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-14	CP17_6		Color pattern for pixel position 0 (Field 1) Mosaic: Pixel count=0 at EVEN line Stripe: Pixel count=0.
		0	R/Ye
		1h	Gr/Cy
		2h	Gb/G
		3h	B/Mg
13-12	CP15_4		Color pattern for pixel position 1 (Field 1) Mosaic: Pixel count=1 at EVEN line Stripe: Pixel count=1.
		0	R/Ye
		1h	Gr/Cy
		2h	Gb/G
		3h	B/Mg
11-10	CP13_2		Color pattern for pixel position 2 (Field 1) Mosaic: Pixel count=0 at ODD line Stripe: Pixel count=2.
		0	R/Ye
		1h	Gr/Cy
		2h	Gb/G
		3h	B/Mg
9-8	CP11_0		Color pattern for pixel position 3 (Field 1) Mosaic: Pixel count=1 at ODD line Stripe: Not applicable.
		0	R/Ye
		1h	Gr/Cy
		2h	Gb/G
		3h	B/Mg
7-6	CP07_6		Color pattern for pixel position 0 (Field 0) Mosaic: Pixel count=0 at EVEN line Stripe: Pixel count=0.
		0	R/Ye
		1h	Gr/Cy
		2h	Gb/G
		3h	B/Mg
5-4	CP05_4		Color pattern for pixel position 1 (Field 0) Mosaic: Pixel count=1 at EVEN line Stripe: Pixel count=1.
		0	R/Ye
		1h	Gr/Cy
		2h	Gb/G
		3h	B/Mg
3-2	CP03_2		Color pattern for pixel position 2 (Field 0) Mosaic: Pixel count=0 at ODD line Stripe: Pixel count=2.
		0	R/Ye
		1h	Gr/Cy
		2h	Gb/G
		3h	B/Mg

Table 91. CCD Color Pattern (CCOLP) Field Descriptions (continued)

Bit	Field	Value	Description
1-0	CP01_0		Color pattern for pixel position 3 (Field 0) Mosaic: Pixel count=1 at ODD line Stripe: Not applicable.
		0	R/Ye
		1h	Gr/Cy
		2h	Gb/G
		3h	B/Mg

6.1.21 CCD Gain Adjustment - R/Ye (CRGAIN)

The CCD gain adjustment - R/Ye (CRGAIN) register is shown in Figure 159 and described in Table 92.

Figure 159. CCD Gain Adjustment - R/Ye (CRGAIN) Register

31-16	
Reserved	
R-0	
15-12	11-0
Reserved	CGR
R-0	R/W-512

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 92. CCD Gain Adjustment - R/Ye (CRGAIN) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	CGR	0-FFFh	R/Ye gain : Gain adjustment factor for CCD data Value is U12Q9, Range: 0 - 7+511/512. This bit is latched by VD.

6.1.22 CCD Gain Adjustment - Gr/Cy (CGRGAIN)

The CCD gain adjustment - Gr/Cy (CGRGAIN) register is shown in Figure 160 and described in Table 93.

Figure 160. CCD Gain Adjustment - Gr/Cy (CGRGAIN) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	CGGR
R-0	R/W-512

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 93. CCD Gain Adjustment - Gr/Cy (CGRGAIN) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	CGGR	0-FFFh	Gr/Cy gain :Gain adjustment factor for CCD data Value is U12Q9, Range: 0 - 7+511/512. This bit is latched by VD.

6.1.23 CCD Gain Adjustment - Gb/G (CGBGAIN)

The CCD gain adjustment - Gb/G (CGBGAIN) register is shown in Figure 161 and described in Table 94.

Figure 161. CCD Gain Adjustment - Gb/G (CGBGAIN) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	CGGB
R-0	R/W-512

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 94. CCD Gain Adjustment - Gb/G (CGBGAIN) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	CGGB	0-FFFh	Gb/G gain :Gain adjustment factor for CCD data Value is U12Q9, Range: 0 - 7+511/512. This bit is latched by VD.

6.1.24 CCD Gain Adjustment - B/Mg (CBGAIN)

The CCD gain adjustment - B/Mg (CBGAIN) register is shown in Figure 162 and described in Table 95.

Figure 162. CCD Gain Adjustment - B/Mg (CBGAIN) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	CGB
R-0	R/W-512

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 95. CCD Gain Adjustment - B/Mg (CBGAIN) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	CGB	0-FFFh	B/Mg gain :Gain adjustment factor for CCD data Value is U12Q9, Range: 0 - 7+511/512. This bit is latched by VD.

6.1.25 CCD Offset Adjustment (COFSTA)

The CCD offset adjustment (COFSTA) register is shown in Figure 163 and described in Table 96.

Figure 163. CCD Offset Adjustment (COFSTA) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	COFT
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 96. CCD Offset Adjustment (COFSTA) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	COFT	0-FFFh	Offset adjustment after gain adjustment Value is added to data after gain (0-4,095). This bit is latched by VD.

6.1.26 FlashCFG0 (FLSHCFG0)

The FlashCFG0 (FLSHCFG0) register is shown in Figure 164 and described in Table 97.

Figure 164. FlashCFG0 (FLSHCFG0) Register

31-16
Reserved
R-0

15-1	0
Reserved	FLSHEN
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 97. FlashCFG0 (FLSHCFG0) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	FLSHEN		Flash timing signal enable
		0	Disable
		1	Enable

6.1.27 FlashCFG1 (FLSHCFG1)

The FlashCFG1 (FLSHCFG1) register is shown in Figure 165 and described in Table 98.

Figure 165. FlashCFG1 (FLSHCFG1) Register

31-16
Reserved
R-0

15	14-0
Rsvd	SFLSH
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 98. FlashCFG1 (FLSHCFG1) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	SFLSH	0-7FFFh	Start line to set the FLASH timing signal.

6.1.28 FlashCFG2 (FLSHCFG2)

The FlashCFG2 (FLSHCFG2) register is shown in Figure 166 and described in Table 99.

Figure 166. FlashCFG2 (FLSHCFG2) Register

31-16
Reserved
R-0

15-0
VFLSH
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 99. FlashCFG2 (FLSHCFG2) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VFLSH	0-FFFFh	Valid width of the FLASH timing signal.

6.1.29 VD Interrupt #0 (VDINT0)

The VD Interrupt #0 (VDINT0) register is shown in Figure 167 and described in Table 100.

Figure 167. VD Interrupt #0 (VDINT0) Register

31-16
Reserved
R-0

15	14-0
Rsvd	CVD0
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 100. VD Interrupt #0 (VDINT0) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	CVD0	0-7FFFh	VD0 Interrupt Timing in a field (line number)

6.1.30 VD Interrupt #1 (VDINT1)

The VD Interrupt #1 (VDINT1) register is shown in Figure 168 and described in Table 101.

Figure 168. VD Interrupt #1 (VDINT1) Register

31-16
Reserved
R-0

15	14-0
Rsvd	CVD1
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 101. VD Interrupt #1 (VDINT1) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	CVD1	0-7FFFh	VD1 Interrupt Timing in a field (line number)

6.1.31 VD Interrupt #2 (VDINT2)

The VD Interrupt #2 (VDINT2) register is shown in Figure 169 and described in Table 102.

Figure 169. VD Interrupt #2 (VDINT2) Register

31-16
Reserved
R-0

15	14-0
Rsvd	CVD2
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 102. VD Interrupt #2 (VDINT2) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	CVD2	0-7FFFh	VD2 Interrupt Timing in a field (line number)

6.1.32 Gamma Correction Settings (CGAMMAWD)

The gamma correction settings (CGAMMAWD) register is shown in Figure 170 and described in Table 103.

Figure 170. Gamma Correction Settings (CGAMMAWD) Register

31-16							
Reserved							
R-0							
15	14	13	12	11	10	9	8
Reserved	WBEN2	WBEN1	WBEN0	Reserved	OFSTEN2	OFSTEN1	OFSTEN0
R-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0
7-6		5	4-1				0
Reserved		CFAP	GWDI				CCDTBL
R-0		R/W-0	R/W-0				R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 103. Gamma Correction Settings (CGAMMAWD) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14	WBEN2		White Balance Enable for H3A Input. This bit is latched by VD.
		0	Disable
		1	Enable
13	WBEN1		White Balance Enable for IPIPE Input. This bit is latched by VD.
		0	Disable
		1	Enable
12	WBEN0		White Balance Enable for SDRAM Capture. This bit is latched by VD.
		0	Disable
		1	Enable
11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10	OFSTEN2		Offset control Enable for H3A. This bit is latched by VD.
		0	Disable
		1	Enable
9	OFSTEN1		Offset control Enable for IPIPE. This bit is latched by VD.
		0	Disable
		1	Enable
8	OFSTEN0		Offset control Enable for SDRAM capture. This bit is latched by VD.
		0	Disable
		1	Enable
7-6	Reserved	0	Any writes to these bit(s) must always have a value of 0.
5	CFAP		CFA Pattern. This bit is latched by VD.
		0	Mosaic
		1	Stripe

Table 103. Gamma Correction Settings (CGAMMAWD) Field Descriptions (continued)

Bit	Field	Value	Description
4-1	GWDI		Select MSB of RAW input data 9-15: Reserved. This bit is latched by VD.
		0	bit 15
		1h	bit 14
		2h	bit 13
		3h	bit 12
		4h	bit 11
		5h	bit 10
		6h	bit 9
		7h	bit 8
		8h	bit 7
		9h-Fh	Reserved
0	CCDTBL		On/Off control of Gamma (A-LAW) table to ISIF data saved to SDRAM. This bit is latched by VD.
		0	off
		1	on

6.1.33 CCIR 656 Control (REC656IF)

The CCIR 656 control (REC656IF) register is shown in Figure 171 and described in Table 104.

Figure 171. CCIR 656 Control (REC656IF) Register

31	2	1	0
Reserved		ECCFVH	R656ON
R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 104. CCIR 656 Control (REC656IF) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	ECCFVH		FVH Error Correction Enable
		0	Off
		1	On
0	R656ON		REC656 Interface Enable
		0	Off
		1	On

6.1.34 CCD Configuration (CCDCFG)

The CCD configuration (CCDCFG) register is shown in Figure 172 and described in Table 105.

Figure 172. CCD Configuration(CCDCFG) Register

31-16							
Reserved							
R-0							
15	14	13	12	11	10	9	8
VDLC	Reserved	MSBINVI	BSWD	Y8POS	EXTRG	TRGSEL	WENLOG
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7-6		5	4	3-2		1-0	
FIDMD		BW656	YCINSWP	Reserved		SDRPACK	
R/W-0		R/W-0	R/W-0	R/W-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 105. CCD Configuration (CCDCFG) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15	VDLC		Enable synchronizing function registers on VSYNC
		0	Latched on VSYNC
		1	Not latched on VSYNC
14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13	MSBINVI		MSB of Chroma input signal stored to SDRAM inverted
		0	normal
		1	MSB inverted
12	BSWD		Byte Swap Data stored to SDRAM
		0	normal
		1	Swap Bytes
11	Y8POS		Location of Y signal when YCbCr 8bit data is input
		0	even pixel
		1	odd pixel
10	EXTRG		External Trigger
		0	Disable
		1	Enable
9	TRGSEL		Signal that initializes SDRAM address when EXTRG = 1
		0	WEN bit (SYNCEN register)
		1	FID input port
8	WENLOG		Specifies CCD valid area
		0	Internal valid and WEN signals are ANDed logically
		1	Internal valid and WEN signals are ORed logically
7-6	FIDMD		Setting of FID detection function
		0	FID signal is latched at the VSYNC timing
		1	FID signal is not latched
5	BW656		The data width in CCIR656 input mode
		0	8-bits
		1	10-bits
4	YCINSWP		Y input (YIN[7:0]) and C input (CIN[7:0]) are swapped
		0	YIN[7:0] = Y signal / CIN[7:0] = C signal
		1	YIN[7:0] = C signal / CIN[7:0] = Y signal

Table 105. CCD Configuration (CCDCFG) Field Descriptions (continued)

Bit	Field	Value	Description
3-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1-0	SDRPACK		SDRAM pack
		0	16bits/pixel
		1h	12bits/pixel
		2h	8bits/pixel
		3h	Reserved

6.1.35 Defect Correction Control (DFCCTL)

The defect correction control (DFCCTL) register is shown in Figure 173 and described in Table 106.

Figure 173. Defect Correction Control (DFCCTL) Register

31-16			
Reserved			
R-0			
15-11			10-8
Reserved			VDFLSFT
R-0			R/W-0
7	6-5	4	3-0
VDFCUDA	VDFCSL	VDFCEN	Reserved
R/W-0	R/W-0	R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 106. Defect Correction Control (DFCCTL) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-8	VDFLSFT	0-7h	Vertical line Defect level shift value Defect Level (value to be subtracted from the data) is 8bit width, but can be up-shifted up to 4bits by VDFLSFT. Left shift value = VDFLSFT (Range: 0-4) Setting the value greater than 4 to VDFLSFT is not allowed.
7	VDFCUDA		Vertical line Defect Correction upper pixels disable
		0	The whole line is corrected
		1	Pixels upper than the defect are not corrected
6-5	VDFCSL		Vertical line Defect Correction mode select
		0	Defect level subtraction. Just fed through if data are saturating.
		1h	Defect level subtraction. Horizontal interpolation ((i-2)+(i+2))/2 if data are saturating.
		2h	Horizontal interpolation ((i-2)+(i+2))/2.
		3h	Reserved
4	VDFCEN		Vertical line Defect Correction enable. This bit field is latched by VD.
		0	Off
		1	On
3-0	Reserved	0	Any writes to these bit(s) must always have a value of 0.

6.1.36 Defect Correction Vertical Saturation Level (VDFSATLV)

The defect correction - vertical saturation level (VDFSATLV) register is shown in Figure 174 and described in Table 107.

Figure 174. Defect Correction Vertical Saturation Level (VDFSATLV) Register

31-16	
Reserved	
R-0	
15-12	11-0
Reserved	VDFSLV
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 107. Defect Correction Vertical Saturation Level (VDFSATLV) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VDFSLV	0-FFFh	Vertical line Defect Correction saturation level. VDFSLV is U12 (Range: 0 - 4,095).

6.1.37 Defect Correction Memory Control (DFCMEMCTL)

The defect correction - memory control (DFCMEMCTL) register is shown in Figure 175 and described in Table 108.

Figure 175. Defect Correction Memory Control (DFCMEMCTL) Register

31-8					
Reserved					
R-0					
7-5	4	3	2	1	0
Reserved	DFCMCLR	Reserved	DFCMARST	DFCMRD	DFCMWR
R-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 108. Defect Correction Memory Control (DFCMEMCTL) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4	DFCMCLR		Memory clear Writing '1' to this bit clears the memory contents to all zero. It will be automatically cleared to '0' when the memory clear is completed.
		0	Memory clear complete
		1	Clear memory
3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2	DFCMARST		Memory Address Reset Setting DFCMWR or DFCMRD with LSCMARST set starts memory access to address offset 0. DFCMARST is automatically cleared if data transfer completes. Setting DFCMWR or DFCMRD with LSCMARST cleared starts memory access to the next address.
		0	Increment the memory address
		1	Clear the memory address to offset 0
1	DFCMRD		Memory Read (for debug) Writing '1' to this bit starts reading from the memory. It will be automatically cleared when the data transfer is completed, and the data can be read from DFCMEM4-0.
		0	Memory read complete
		1	Memory read
0	DFCMWR		Memory write Writing '1' to this bit starts writing to the memory. It will be automatically cleared when the data transfer is completed. DFCMEM4-0 should be set prior to the memory access.
		0	Memory write complete
		1	Memory write

6.1.38 Defect Correction Set V Position (DFCMEM0)

The defect correction - set V position 0 (DFCMEM0) register is shown in Figure 176 and described in Table 109.

Figure 176. Defect Correction Set V Position 0 (DFCMEM0) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	DFCMEM0
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 109. Defect Correction Set V Position 0 (DFCMEM0) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	DFCMEM0	0-1FFFh	Memory 0 Set V position of the defects.

6.1.39 Defect Correction Set H Position 1 (DFCMEM1)

The defect correction - set H position (DFCMEM1) register is shown in Figure 177 and described in Table 110 .

Figure 177. Defect Correction Set H Position 1 (DFCMEM1) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	DFCMEM1
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 110. Defect Correction Set H Position 1 (DFCMEM1) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	DFCMEM1	0-1FFFh	Memory 1 Set H position of the defects.

6.1.40 Defect Correction Set SUB1 (DFCMEM2)

The defect correction - set SUB1 (DFCMEM2) register is shown in Figure 178 and described in Table 111.

Figure 178. Defect Correction Set SUB1 (DFCMEM2) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	DFCMEM2
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 111. Defect Correction Set SUB1 (DFCMEM2) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	DFCMEM2	0-FFh	Memory 2 Set SUB1: Defect level of the Vertical line defect position (V = Vdefect). DFCMEM2 can be up shifted according to VDFLSFT, and subtracted from the data for Vertical line defect correction.

6.1.41 Defect Correction Set SUB2 (DFCMEM3)

The defect correction - set SUB2 (DFCMEM3) register is shown in Figure 179 and described in Table 112.

Figure 179. Defect Correction Set SUB2 (DFCMEM3) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	DFCMEM3
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 112. Defect Correction Set SUB2 (DFCMEM3) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	DFCMEM3	0-FFh	Memory 3 Set SUB2: Defect level of the pixels upper than the Vertical line defect (V > Vdefect). DFCMEM3 can be up shifted according to VDFLSFT, and subtracted from the data for Vertical line defect correction.

6.1.42 Defect Correction Set SUB3 (DFCMEM4)

The defect correction - set SUB3 (DFCMEM4) register is shown in Figure 180 and described in Table 113.

Figure 180. Defect Correction Set SUB3 (DFCMEM4) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	DFCMEM4
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 113. Defect Correction Set SUB3 (DFCMEM4) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	DFCMEM4	0-FFh	Memory 4 Set SUB3: Defect level of the pixels lower than the Vertical line defect (V > Vdefect). DFCMEM4 can be up shifted according to VDFLSFT, and subtracted from the data for Vertical line defect correction.

6.1.43 Black Clamp Configuration (CLAMPCFG)

The black clamp configuration (CLAMPCFG) register is shown in Figure 181 and described in Table 114.

Figure 181. Black Clamp Configuration (CLAMPCFG) Register

31-16
Reserved
R-0

15-5	4	3	2-1	0
Reserved	CLMD	Rsvd	CLHMD	CLEN
R-0	R/W-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 114. Black Clamp Configuration (CLAMPCFG) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4	CLMD		Black Clamp Mode
		0	Clamp value calculated regardless of the color
		1	Clamp value calculated separately for each 4 color
3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2-1	CLHMD	0-3h	Horizontal Clamp Mode
0	CLEN		Black Clamp Enable
		0	Disbale
		1	Enable

6.1.44 DC Offset for Black Clamp (CLDCOFST)

The DC offset for black clamp (CLDCOFST) register is shown in Figure 182 and described in Table 115.

Figure 182. DC Offset for Black Clamp (CLDCOFST) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	CLDC
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 115. DC Offset for Black Clamp (CLDCOFST) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	CLDC	0-1FFFh	DC offset for Black Clamp (S13)

6.1.45 Black Clamp Start Position (CLSV)

The black clamp start position (CLSV) register is shown in Figure 183 and described in Table 116.

Figure 183. Black Clamp Start Position (CLSV) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	CLSV
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 116. Black Clamp Start Position (CLSV) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	CLSV	0-1FFFh	Black Clamp Start position (V)

6.1.46 Horizontal Black Clamp Configuration (CLHWIN0)

The horizontal black clamp configuration 0 (CLHWIN0) register is shown in Figure 184 and described in Table 117.

Figure 184. Horizontal Black Clamp Configuration 0 (CLHWIN0) Register

31-16
Reserved
R-0

15-14	13-12	11-10	9-8
Reserved	CLHWN	Reserved	CLHWM
R-0	R/W-0	R-0	R/W-0

7	6	5	4-0
Reserved	CLHLMT	CLHWBS	CLHWC
R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 117. Horizontal Black Clamp Configuration 0 (CLHWIN0) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-12	CLHWN	0-3h	Vertical dimension of a window (2^N)
11-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-8	CLHWM	0-3h	Horizontal dimension of a window (2^M)
7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6	CLHLMT	0-1	Horizontal Black clamp
5	CLHWBS	0-1	Base Window select
4-0	CLHWC	0-1Fh	Window count per color

6.1.47 Horizontal Black Clamp Configuration 1 (CLHWIN1)

The horizontal black clamp configuration 1 (CLHWIN1) register is shown in Figure 185 and described in Table 118.

Figure 185. Horizontal Black Clamp Configuration 1 (CLHWIN1) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	CLHSH
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 118. Horizontal Black Clamp Configuration 1 (CLHWIN1) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	CLHSH	0-1FFFh	Window Start position (H)

6.1.48 Horizontal Black Clamp Configuration 2 (CLHWIN2)

The horizontal black clamp configuration 2 (CLHWIN2) register is shown in Figure 186 and described in Table 119.

Figure 186. Horizontal Black Clamp Configuration 2 (CLHWIN2) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	CLHSV
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 119. Horizontal Black Clamp Configuration 2 (CLHWIN2) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	CLHSV	0-1FFFh	Window Start position (V)

6.1.49 Vertical Black Clamp Configuration (CLVRV)

The vertical black clamp configuration (CLVRV) register is shown in Figure 187 and described in Table 120.

Figure 187. Vertical Black Clamp Configuration (CLVRV) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	CLVRV
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 120. Vertical Black Clamp Configuration (CLVRV) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	CLVRV	0-FFFh	Reset value (U12) for the Clamp Value register

6.1.50 Vertical Black Clamp Configuration 0 (CLVWIN0)

The vertical black clamp configuration 0 (CLVWIN0) register is shown in Figure 188and described in Table 121.

Figure 188. Vertical Black Clamp Configuration 0 (CLVWIN0) Register

31-16
Reserved
R-0

15-8	7-6	5-4	3	2-0
CLVCOEF	Reserved	CLVRVSL	Rsvd	CLVOBH
R/W-0	R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 121. Vertical Black Clamp Configuration 0 (CLVWIN0) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CLVCOEF	0-FFh	Line average coefficient (k)
7-6	Reserved	0	Any writes to these bit(s) must always have a value of 0.
5-4	CLVRVSL		Reset value for the Clamp value of previous line.
		0	Base value calculated for Horizontal direction
		1h	Value set via the configuration register
		2h	No update (same as previous image)
		3h	Reserved
3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2-0	CLVOBH	0-7h	Optical Black H valid (2^L)

6.1.51 Vertical Black Clamp Configuration 1 (CLVWIN1)

The vertical black clamp configuration 1 (CLVWIN1) register is shown in Figure 189 and described in Table 122 .

Figure 189. Vertical Black Clamp Configuration 1 (CLVWIN1) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	CLVSH
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 122. Vertical Black Clamp Configuration 1 (CLVWIN1) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	CLVSH	0-1FFFh	Optical Black Start position (H).

6.1.52 Vertical Black Clamp Configuration 2 (CLVWIN2)

The vertical black clamp configuration 2 (CLVWIN2) register is shown in Figure 190 and described in Table 123.

Figure 190. Vertical Black Clamp Configuration 2 (CLVWIN2) Register

31-16
Reserved
R-0

L

15-13	12-0
Reserved	CLVSV
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 123. Vertical Black Clamp Configuration 2 (CLVWIN2) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	CLVSV	0-1FFFh	Optical Black Start position (V).

6.1.53 Vertical Black Clamp Configuration 3 (CLVWIN3)

The vertical black clamp configuration 3 (CLVWIN3) register is shown in Figure 191 and described in Table 124.

Figure 191. Vertical Black Clamp Configuration 3 (CLVWIN3) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	CLVOBV
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 124. Vertical Black Clamp Configuration 3 (CLVWIN3) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	CLVOBV	0-1FFFh	Optical Black V valid.

6.1.54 H Direction Data Offset (DATAHOFST)

The H direction data offset (DATAHOFST) register is shown in Figure 192 and described in Table 125.

Figure 192. H Direction Data Offset (DATAHOFST) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	HOFST
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 125. H Direction Data Offset (DATAHOFST) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	HOFST	0-3FFFh	H direction Data offset for Defect Correction and Lens Shading Correction Range: 0-16,383 It is valid whether the Formatter is enabled or not. In case the Formatter is enabled and HOFST=0, the first valid pixel for the DFC/LSC is the first pixel in a formatted line.

6.1.55 V Direction Data Offset (DATAVOFST)

The V direction data offset (DATAVOFST) register is shown in Figure 193 and described in Table 126.

Figure 193. V Direction Data Offset (DATAVOFST) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VOFST
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 126. V Direction Data Offset (DATAVOFST) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VOFST	0-3FFFh	V direction Data offset for Defect Correction and Lens Shading Correction Range: 0-16,383 It is valid whether the Formatter is enabled or not. In case the Formatter is enabled and VOFST=0, the first valid pixel for the DFC/LSC is the first pixel in a formatted line.

6.1.56 HVAL for LSC (LSCHVAL)

The HVAL for LSC (LSCHVAL) register is shown in Figure 194 and described in Table 127.

Figure 194. HVAL for LSC (LSCHVAL) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	HVAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 127. HVAL for LSC (LSCHVAL) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	HVAL	0-3FFFh	Number of valid pixels in H direction HVAL is for LSC. Number of valid pixels = HVAL + 1

6.1.57 VVAL for LSC (LSCVVAL)

The VVAL for LSC (LSCVVAL) register is shown in Figure 195 and described in Table 128.

Figure 195. VVAL for LSC (LSCVVAL) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VVAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 128. VVAL for LSC (LSCVVAL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VVAL	0-3FFFh	Number of valid pixels in V direction VVAL is for LSC. Number of valid pixels = VVAL + 1

6.1.58 2D Lens Shading Correction Configuration (2DLSCCFG)

The 2D lens shading correction configuration (2DLSCCFG) register is shown in Figure 196 and described in Table 129.

Figure 196. 2D Lens Shading Correction Configuration (2DLSCCFG) Register

31-16
Reserved
R-0

15	14-12	11	10-8	7	6-4	3-1	0
Reserved	GAIN_MODE_M	Reserved	GAIN_MODE_N	BUSY	Reserved	GAIN_FORMAT	ENABLE
R-0	R/W-6	R-0	R/W-6	R-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 129. 2D Lens Shading Correction Configuration (2DLSCCFG) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-12	GAIN_MODE_M		Horizontal dimension of a paxel
		0	Reserved
		3	Paxel is 8 pixels wide
		4	Paxel is 16 pixels wide
		5	Paxel is 32 pixels wide
		6	Paxel is 64 pixels wide
		7	Paxel is 128 pixels wide
11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-8	GAIN_MODE_N		Vertical dimension of a paxel
		0	Reserved
		3	Paxel is 8 pixels tall
		4	Paxel is 16 pixels tall
		5	Paxel is 32 pixels tall
		6	Paxel is 64 pixels tall
		7	Paxel is 128 pixels tall
7	BUSY		Busy Status
		0	Idle
		1	Busy
6-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.
3-1	GAIN_FORMAT		Gain table format
		0	Coded as 8-bit fraction (range 0 : 255/256)
		1	Coded as 8-bit fraction + 1 (range 1 : 1+255/256)
		2	Coded as 1-bit integer, 7bit fraction (range 0 : 1+127/128)
		3	Coded as 1-bit integer, 7bit fraction +1 (range 1 : 2+127/128)
		4	Coded as 2-bit integer, 6bit fraction (range 0 : 3+63/64)
		5	Coded as 2-bit integer, 6bit fraction +1 (range 1 : 4+63/64)
		6	Coded as 3-bit integer, 5bit fraction (range 0 : 7+31/32)
		7	Coded as 3-bit integer, 5bit fraction +1 (range 1 : 8+31/32)
0	ENABLE		2D Lens shading correction enable Writing a 0 will disable LSC at the end of the current frame. Writing a 1 will start fetching the gain table immediately but processing will not begin until start of next frame. Therefore, all other 2D LSC registers must be set before this bit is set to 1.
		0	Disable
		1	Enable

6.1.59 2D LSC Gain Table Offset (DDLSCOFST)

The 2D LSC gain table offset (DDLSCOFST) register is shown in Figure 197 and described in Table 130.

Figure 197. 2D LSC Gain Table Offset (DDLSCOFST) Register

31-16				
Reserved				
R-0				
15-8	7	6-4	3-1	0
OFSTSF	Reserved	OFSTSFT	Reserved	OFSTEN
R/W-1	R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 130. 2D LSC Gain Table Offset (DDLSCOFST) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	OFSTSF	0-FFh	Scaling factor for Offsets (U8Q7) Setting a value more than 1 is not allowed.
7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6-4	OFSTSFT		Shift up value for Offsets (S8Q0)
		0	
		1	
		2	
		3	
		4	
		5	
		6-7	
3-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	OFSTEN	0	Disable
		1	Enable

6.1.60 2D LSC Initial Position (DDLSCINI)

The 2D LSC initial position (DDLSCINI) register is shown in Figure 198 and described in Table 131.

Figure 198. 2D LSC Initial Position (DDLSCINI) Register

31-16
Reserved
R-0

15	14-8	7	6-0
Reserved	Y	Reserved	X
R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 131. 2D LSC Initial Position (DDLSCINI) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-8	Y	0-7Fh	Initial Y position, in pixels, of the first active pixel in reference to the first active paxel. Must be an even number.
7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6-0	X	0-7Fh	Initial X position, in pixels, of the first active pixel in reference to the first active paxel. Must be an even number.

6.1.61 2D LSC Gain Table Address Base (Upper) (DDLSCGRBU)

The 2D LSC gain table address base (Upper) (DDLSCGRBU) register is shown in Figure 199 and described in Table 132.

Figure 199. 2D LSC Gain Table Address Base (Upper) (DDLSCGRBU) Register

31-16
Reserved
R-0
15-0
BASE31_16
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 132. 2D LSC Gain Table Address base (Upper) (DDLSCGRBU) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	BASE31_16	0-FFFFh	Gain Table address base (Upper 16-bits) Table address in bytes. This bit field sets the address of the gain table in memory.

6.1.62 2D LSC Gain Table Address Base (Lower) (DDLSCGRBL)

The 2D LSC gain table address base (Lower) (DDLSCGRBL) register is shown in Figure 200 and described in Table 133.

Figure 200. 2D LSC Gain Table Address Base (Lower) (DDLSCGRBL) Register

31-16
Reserved
R-0
15-0
BASE15_0
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 133. 2D LSC Gain Table Address Base (Lower) (DDLSCGRBL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	BASE15_0	0-FFFFh	Gain Table address base (Lower 16-bits) Table address in bytes. Table is 32-bit aligned so this register must be a multiple of 4. This bit field sets the address of the gain table in memory.

6.1.63 2D LSC Gain Table Offset (DDLSCGROF)

The 2D LSC gain table offset (DDLSCGROF) register is shown in Figure 201 and described in Table 134.

Figure 201. 2D LSC Gain Table Offset (DDLSCGROF) Register

31-16
Reserved
R-0
15-0
OFFSET
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 134. 2D LSC Gain Table Offset (DDLSCGROF) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	OFFSET	0-FFFFh	Gain Table offset Defines the length, in bytes, of one row of the table. Table is 32-bit aligned, so this register must be a multiple of 4. Note that the row in memory could be longer than what LSC uses.

6.1.64 2D LSC Offset Table Address Base (Upper) (DDLSCORBU)

The 2D LSC offset table address base (Upper) (DDLSCORBU) is shown in Figure 202 and described in Table 135.

Figure 202. 2D LSC Offset Table Address Base (Upper) (DDLSCORBU) Register

31-16
Reserved
R-0
15-0
BASE31_16
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 135. 2D LSC Offset Table Address Base (Upper) (DDLSCORBU) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	BASE31_16	0-FFFFh	Offset Table address base (Upper 16-bits) Table address in bytes. This bit field sets the address of the gain table in memory.

6.1.65 2D LSC Offset Table Address Base (Lower) (DDLSCORBL)

The 2D LSC offset table address base (Lower) (DDLSCORBL) is shown in Figure 203 and described in Table 136.

Figure 203. 2D LSC Offset Table Address Base (Lower) (DDLSCORBL) Register

31-16
Reserved
R-0
15-0
BASE15_0
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 136. 2D LSC Offset Table Address Base (Lower) (DDLSCORBL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	BASE15_0	0-FFFFh	Offset Table address base (Lower 16-bits) Table address in bytes. Table is 32-bit aligned so this register must be a multiple of 4. This bit field sets the address of the gain table in memory.

6.1.66 2D LSC Offset Table Offset (DDLSCOROF)

The 2D LSC offset table offset (DDLSCOROF) register is shown in Figure 204 and described in Table 137.

Figure 204. 2D LSC Offset Table Offset (DDLSCOROF) Register

31-16
Reserved
R-0

15-0
OFFSET
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 137. 2D LSC Offset Table Offset (DDLSCOROF) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	OFFSET	0-FFFFh	Offset table offset defines the length, in bytes, of one row of the table. Table is 32-bit aligned, so this register must be a multiple of 4. Note that the row in memory could be longer than what LSC uses.

6.1.67 2D LSC Interrupt Request Enable (DDLSCIRQEN)

The 2D LSC interrupt request enable (DDLSCIRQEN) register is shown in Figure 205 and described in Table 138 .

Figure 205. 2D LSC Interrupt Request Enable (DDLSCIRQEN) Register

31-16				
Reserved				
R-0				
15-4	3	2	1	0
Reserved	SOF	PREFETCH_COM PLETED	PREFETCH_ERROR	DONE
R-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 138. 2D LSC Interrupt Request Enable (DDLSCIRQEN) Field Descriptions

Bit	Field	Value	Description
31-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.
3	SOF		Interrupt enable for LSC SOF Indicates the start of the LSC valid region. LSC configuration registers can be updated after LSC SOF for the next frame.
		0	Interrupt masked
		1	Interrupt enabled
2	PREFETCH_COMPLETED		Interrupt enable for Prefetch Complete Indicates current state of the prefetch buffer. Could be used to start sending the data once the buffer is full to minimize the risk of an underflow. This event is triggered when the buffer contains 3 full paxel rows. It could be used to minimize buffer underflow risks.
		0	Interrupt masked
		1	Interrupt enabled
1	PREFETCH_ERROR		Interrupt enable for Prefetch Error The prefetch error indicates when the gain table was read to slowly from SDRAM. When this event is pending the module goes into transparent mode (output=input). Normal operation can be resumed at the start of the next frame after 1) clearing this event 2) disabling the LSC module 3) enabling it
		0	Interrupt masked
		1	Interrupt enabled
0	DONE		Interrupt enable for LSC Done The event is triggered when the internal state of LSC toggles from BUSY to IDLE.
		0	Interrupt masked
		1	Interrupt enabled

6.1.68 2D LSC Interrupt Request Status (DDLSCIRQST)

The 2D LSC interrupt request status (DDLSCIRQST) register is shown in Figure 206 and described in Table 139.

Figure 206. 2D LSC Interrupt Request Status (DDLSCIRQST) Register

31-16				
Reserved				
R-0				
15-4	**3**	**2**	**1**	**0**
Reserved	SOF	PREFETCH_COM PLETED	PREFETCH_ERROR	DONE
R-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 139. DD LSC Interrupt Request Status (2DLSCIRQST) Field Descriptions

Bit	Field	Value	Description
31-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.
3	SOF		Interrupt Status for LSC SOF Set at start of the LSC valid region, clear by writing 1. LSC configuration registers can be updated after LSC SOF for the next frame.
		1	clear bit
2	PREFETCH_COMPLETED		Interrupt Status for Prefetch Complete Set when the prefetch buffer contains 3 full paxel rows, clear by writing 1. It could be used to minimize buffer underflow risks.
		1	clear bit
1	PREFETCH_ERROR		Interrupt Status for Prefetch Error Set when the gain table was read to slowly from SDRAM, clear by writing 1. When this event is set the module goes into transparent mode (output=input). Normal operation can be resumed at the start of the next frame after 1) clearing this event 2) disabling the LSC module 3) enabling it
		1	clear bit
0	DONE		Interrupt Status for LSC Done Set when the internal state of LSC toggles from BUSY to IDLE, cleared by writing 1.
		1	clear bit

6.1.69 CCD Formatter configuration (FMTCFG)

The CCD formatter configuration (FMTCFG) register is shown in Figure 207 and described in Table 140 .

Figure 207. CCD Formatter Configuration (FMTCFG) Register

31-16							
Reserved							
R-0							
15-12	11-8	7-6	5-4	3	2	1	0
Reserved	FMTAINC	Reserved	LNUM	Reserved	LNALT	FMTCBL	FMTEN
R-0	R/W-0	R-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 140. CCD Formatter Configuration (FMTCFG) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-8	FMTAINC	0-Fh	Address increment Address increment = (FMTAINC + 1) Range (1-16). This bit is latched by VD.
7-6	Reserved	0	Any writes to these bit(s) must always have a value of 0.
5-4	LNUM		Split/Combine number of lines. This bit is latched by VD.
		0	1 output line
		1	1 input line -> 2 output lines (FMTCBL=0)
		2	1 input line -> 3 output lines (FMTCBL=0)
		3	1 input line -> 4 output lines (FMTCBL=0)
3	Reserved	0	Reserved. Any writes to these bit(s) must always have a value of 0.
2	LNALT		Line alternating. This bit is latched by VD.
		0	Normal mode
		1	Line alternative mode
1	FMTCBL		Combine Input lines. This bit is latched by VD.
		0	Split 1 input line into multiple output lines
		1	Combine multiple input lines into 1 output line
0	FMTEN		CCD Formatter enable. This bit is latched by VD.
		0	Disable
		1	Enable

6.1.70 CCD Formatter Program Entries (FMTPLEN)

The CCD formatter - program entries (FMTPLEN) register is shown in Figure 208 and described in Table 141.

Figure 208. CCD Formatter Program Entries (FMTPLEN) Register

31-16
Reserved
R-0

15	14-12	11	10-8	7-4	3-0
Reserved	FMTPLEN3	Reserved	FMTPLEN2	FMTPLEN1	FMTPLEN0
R-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 141. CCD Formatter Program Entries (FMTPLEN) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-12	FMTPLEN3	0-7h	Number of program entries for SET3 Number of entries = (FMTPLEN3 + 1) Range: 1-8 Valid only if FMTCBL is set. This bit is latched by VD.
11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-8	FMTPLEN2	0-7h	Number of program entries for SET2 Number of entries = (FMTPLEN2 + 1) Range: 1-8 Valid only if FMTCBL is set. This bit is latched by VD.
7-4	FMTPLEN1	0-Fh	Number of program entries for SET1 Number of entries = (FMTPLEN1 + 1) Range: 1-16 (FMTCBL = 0) 1-8 (FMTCBL = 1) Setting a value greater than 7 to FMTPLEN1 is not allowed if FMTCBL is set. This bit is latched by VD.
3-0	FMTPLEN0	0-Fh	Number of program entries for SET0 Number of entries = (PLEN0 + 1) Range: 1-16 (FMTCBL = 0) 1-8 (FMTCBL = 1) Setting a value greater than 7 to FMTPLEN1 is not allowed if FMTCBL is set. This bit is latched by VD.

6.1.71 CCD Formatter Start Pixel Horiz (FMTSPH)

The CCD formatter - start pixel horiz (FMTSPH) register is shown in Figure 209 and described in Table 142.

Figure 209. CCD Formatter Start Pixel Horiz (FMTSPH) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	FMTSPH
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 142. CCD Formatter Start Pixel Horiz (FMTSPH) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	FMTSPH	0-1FFFh	The first pixel in a line fed into the formatter

6.1.72 CCD Formatter Number of Pixels (FMTLNH)

The CCD formatter - number of pixels (FMTLNH) register is shown in Figure 210 and described in Table 143.

Figure 210. CCD Formatter Number of Pixels (FMTLNH) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	FMTLNH
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 143. CCD Formatter Number of Pixels (FMTLNH) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	FMTLNH	0-1FFFh	Number of pixels in a line fed to the formatter. Number of pixels = FMTLNH + 1

6.1.73 CCD Formatter Start Line Vertical (FMTSLV)

The CCD formatter - start line vertical (FMTSLV) register is shown in Figure 211and described in Table 144.

Figure 211. CCD Formatter Start Line Vertical (FMTSLV) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	FMTSLV
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 144. CCD Formatter Start Line Vertical (FMTSLV) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	FMTSLV	0-1FFFh	Start line vertical

6.1.74 CCD Formatter Number of Lines (FMTLNV)

The CCD formatter - number of lines (FMTLNV) register is shown in Figure 212 and described in Table 145.

Figure 212. CCD Formatter Number of Lines (FMTLNV) Register

31-16
Reserved
R-0

15	14-0
Rsvd	FMTLNV
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 145. CCD Formatter Number of Lines (FMTLNV) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-0	FMTLNV	0-7FFFh	Number of lines in vertical Number of lines = FMTLNV + 1

6.1.75 CCD Formatter Read Out Line Length (FMTRLEN)

The CCD formatter - read out line length (FMTRLEN) register is shown in Figure 213 and described in Table 146.

Figure 213. CCD Formatter Read Out Line Length (FMTRLEN) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	FMTRLEN
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 146. CCD Formatter Read Out Line Length (FMTRLEN) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	FMTRLEN	0-1FFFh	Number of pixels in an output line Maximum value = 4480

6.1.76 CCD Formatter HD Cycles (FMTHCNT)

The CCD formatter - HD cycles (FMTHCNT) register is shown in Figure 214 and descried in Table 147.

Figure 214. CCD Formatter HD Cycles (FMTHCNT) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	FMTHCNT
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 147. CCD Formatter HD Cycles (FMTHCNT) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	FMTHCNT	0-1FFFh	HD interval for output lines Set all '0' to this register if combining multiple lines into a single line.

6.1.77 CCD Formatter Address Pointer (FMTAPTR0)

The CCD formatter address pointer 0 (FMTAPTR0) register is shown in Figure 215 and described in Table 148.

Figure 215. CCD Formatter Address Pointer 0 (FMTAPTR0) Register

31-16
Reserved
R-0

15	14-13	12-0
Reserved	LINE	INIT
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 148. CCD Formatter Address Pointer 0 (FMTAPTR0) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-13	LINE		The output line the address belongs to Valid only if FMTCBL is cleared
		0	1st line
		1	2nd line
		2	3rd line
		3	4th line
12-0	INIT	0-1FFFh	Initial address value for address pointer 0. This address can not exceed FMTRLEN - 1

6.1.78 CCD Formatter Address Pointer (FMTAPTR1)

The CCD formatter address pointer 1 (FMTAPTR1) register is shown in Figure 216 and described in Table 149.

Figure 216. CCD Formatter Address Pointer 1 (FMTAPTR1) Register

31-16
Reserved
R-0

15	14-13	12-0
Reserved	LINE	INIT
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 149. CCD Formatter Address Pointer 1 (FMTAPTR1) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-13	LINE		The output line the address belongs to Valid only if FMTCBL is cleared
		0	1st line
		1	2nd line
		2	3rd line
		3	4th line
12-0	INIT	0-1FFFh	Initial address value for address pointer 1. This address can not exceed FMTRLEN - 1

6.1.79 CCD Formatter Address Pointer 2 (FMTAPTR2) Register

The CCD formatter address pointer 2 (FMTAPTR2) register is shown in Figure 217 and described in Table 150 .

Figure 217. CCD Formatter Address Pointer 2 (FMTAPTR2) Register

31-16
Reserved
R-0

15	14-13	12-0
Reserved	LINE	INIT
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 150. FCCD Formatter Address Pointer 2 (FMTAPTR2) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-13	LINE		The output line the address belongs to Valid only if FMTCBL is cleared
		0	1st line
		1	2nd line
		2	3rd line
		3	4th line
12-0	INIT	0-1FFFh	Initial address value for address pointer 2. This address can not exceed FMTRLEN - 1

6.1.80 CCD Formatter Address Pointer 3 (FMTAPTR3)

The CCD formatter address pointer 3 (FMTAPTR3) register is shown in Figure 218 and described in Table 151.

Figure 218. CCD Formatter Address Pointer 3 (FMTAPTR3) Register

31-16
Reserved
R-0

15	14-13	12-0
Reserved	LINE	INIT
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 151. CCD Formatter Address Pointer 3 (FMTAPTR3) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-13	LINE		The output line the address belongs to Valid only if FMTCBL is cleared
		0	1st line
		1	2nd line
		2	3rd line
		3	4th line
12-0	INIT	0-1FFFh	Initial address value for address pointer 3. This address can not exceed FMTRLEN - 1

6.1.81 CCD Formatter Address Pointer 4 (FMTAPTR4)

The CCD formatter address pointer 4 (FMTAPTR4) register is shown in Figure 219 and described in Table 152.

Figure 219. CCD Formatter Address Pointer 4 (FMTAPTR4) Register

31-16
Reserved
R-0

15	14-13	12-0
Reserved	LINE	INIT
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 152. CCD Formatter Address Pointer 4 (FMTAPTR4) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-13	LINE		The output line the address belongs to Valid only if FMTCBL is cleared
		0	1st line
		1	2nd line
		2	3rd line
		3	4th line
12-0	INIT	0-1FFFh	Initial address value for address pointer 4. This address can not exceed FMTRLEN - 1

6.1.82 CCD Formatter Address Pointer 5 (FMTAPTR5)

The CCD formatter address pointer 5 (FMTAPTR5) register is shown in Figure 220 and described in Table 153 .

Figure 220. CCD Formatter Address Pointer 5 (FMTAPTR5) Register

31-16
Reserved
R-0

15	14-13	12-0
Reserved	LINE	INIT
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 153. CCD Formatter Address Pointer 5 (FMTAPTR5) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-13	LINE		The output line the address belongs to Valid only if FMTCBL is cleared
		0	1st line
		1	2nd line
		2	3rd line
		3	4th line
12-0	INIT	0-1FFFh	Initial address value for address pointer 5. This address can not exceed FMTRLEN - 1

6.1.83 CCD Formatter Address Pointer (FMTAPTR6)

The CCD formatter address pointer 6 (FMTAPTR6) register is shown in Figure 221 and described in Table 154.

Figure 221. CCD Formatter Address Pointer 6 (FMTAPTR6) Register

31-16
Reserved
R-0

15	14-13	12-0
Reserved	LINE	INIT
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 154. CCD Formatter Address Pointer 6 (FMTAPTR6) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0
14-13	LINE		The output line the address belongs to Valid only if FMTCBL is cleared
		0	1st line
		1	2nd line
		2	3rd line
		3	4th line
12-0	INIT	0-1FFFh	Initial address value for address pointer 6. This address can not exceed FMTRLEN - 1

6.1.84 CCD Formatter Address Pointer (FMTAPTR7)

The CCD formatter address pointer 7 (FMTAPTR7) register is shown in Figure 222 and described in Table 155.

Figure 222. CCD Formatter Address Pointer (FMTAPTR7) Register

31-16
Reserved
R-0

15	14-13	12-0
Reserved	LINE	INIT
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 155. CCD Formatter Address Pointer 7 (FMTAPTR7) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-13	LINE		The output line the address belongs to Valid only if FMTCBL is cleared
		0	1st line
		1	2nd line
		2	3rd line
		3	4th line
12-0	INIT	0-1FFFh	Initial address value for address pointer 7. This address can not exceed FMTRLEN - 1.

6.1.85 CCD Formatter Address Pointer 8 (FMTAPTR8)

The CCD formatter address pointer 8 (FMTAPTR8) register is shown in Figure 223 and described in Table 156.

Figure 223. CCD Formatter Address Pointer (FMTAPTR8) Register

31-16
Reserved
R-0

15	14-13	12-0
Reserved	LINE	INIT
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 156. CCD Formatter Address Pointer (FMTAPTR8) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-13	LINE		The output line the address belongs to Valid only if FMTCBL is cleared
		0	1st line
		1	2nd line
		2	3rd line
		3	4th line
12-0	INIT	0-1FFFh	Initial address value for address pointer 8. This address can not exceed FMTRLEN - 1

6.1.86 CCD Formatter Address Pointer 9 (FMTAPTR9)

The CCD formatter address pointer 9 (FMTAPTR9) register is shown in Figure 224 and described in Table 157.

Figure 224. CCD Formatter Address Pointer (FMTAPTR9) Register

31-16
Reserved
R-0

15	14-13	12-0
Reserved	LINE	INIT
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 157. CCD Formatter Address Pointer 9 (FMTAPTR9) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-13	LINE		The output line the address belongs to Valid only if FMTCBL is cleared
		0	1st line
		1	2nd line
		2	3rd line
		3	4th line
12-0	INIT	0-1FFFh	Initial address value for address pointer 9. This address can not exceed FMTRLEN - 1.

6.1.87 CCD Formatter Address Pointer 10 (FMTAPTR10)

The CCD formatter - Address pointer 10 (FMTAPTR10) register is shown in Figure 225 and described in Table 158.

Figure 225. CCD Formatter Address Pointer 10 (FMTAPTR10) Register

31-16
Reserved
R-0

15	14-13	12-0
Reserved	LINE	INIT
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 158. CCD Formatter Address Pointer 10 (FMTAPTR10) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-13	LINE		The output line the address belongs to Valid only if FMTCBL is cleared
		0	1st line
		1	2nd line
		2	3rd line
		3	4th line
12-0	INIT	0-1FFFh	Initial address value for address pointer 10 This address can not exceed FMTRLEN - 1

6.1.88 CCD Formatter Address Pointer 11 (FMTAPTR11)

The CCD formatter - address pointer 11 (FMTAPTR11) register is shown in Figure 226 and described in Table 159.

Figure 226. CCD Formatter Address Pointer 11 (FMTAPTR11) Register

31-16
Reserved
R-0

15	14-13	12-0
Reserved	LINE	INIT
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 159. CCD Formatter Address Pointer 11 (FMTAPTR11) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-13	LINE		The output line the address belongs to Valid only if FMTCBL is cleared
		0	1st line
		1	2nd line
		2	3rd line
		3	4th line
12-0	INIT	0-1FFFh	Initial address value for address pointer 11. This address can not exceed FMTRLEN - 1.

6.1.89 CCD Formatter Address Pointer 12 (FMTAPTR12)

The CCD formatter - address pointer 12 (FMTAPTR12) register is shown in Figure 227 and described in Table 160.

Figure 227. CCD Formatter Address Pointer 12 (FMTAPTR12) Register

31-16
Reserved
R-0

15	14-13	12-0
Reserved	LINE	INIT
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 160. CCD Formatter Address Pointer (FMTAPTR12) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-13	LINE		The output line the address belongs to Valid only if FMTCBL is cleared
		0	1st line
		1	2nd line
		2	3rd line
		3	4th line
12-0	INIT	0-1FFFh	Initial address value for address pointer 12. This address can not exceed FMTRLEN - 1.

6.1.90 CCD Formatter Address pointer 13 (FMTAPTR13)

The CCD formatter - address pointer 13 (FMTAPTR13) register is shown in Figure 228 and described in Figure 228.

Figure 228. CCD Formatter Address Pointer 13 (FMTAPTR13) Register

31-16
Reserved
R-0

15	14-13	12-0
Reserved	LINE	INIT
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 161. CCD Formatter Address Pointer 13 (FMTAPTR13) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-13	LINE		The output line the address belongs to Valid only if FMTCBL is cleared
		0	1st line
		1	2nd line
		2	3rd line
		3	4th line
12-0	INIT	0-1FFFh	Initial address value for address pointer 13. This address can not exceed FMTRLEN - 1.

6.1.91 CCD Formatter Address Pointer (FMTAPTR14)

The CCD formatter - address pointer 14 (FMTAPTR14) register is shown in Figure 229 and described in Table 162.

Figure 229. CCD Formatter Address Pointer (FMTAPTR14) Register

31-16
Reserved
R-0

15	14-13	12-0
Reserved	LINE	INIT
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 162. CCD Formatter Address pointer (FMTAPTR14) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-13	LINE		The output line the address belongs to Valid only if FMTCBL is cleared
		0	1st line
		1	2nd line
		2	3rd line
		3	4th line
12-0	INIT	0-1FFFh	Initial address value for address pointer 14. This address can not exceed FMTRLEN - 1.

6.1.92 CCD Formatter Address Pointer (FMTAPTR15)

The CCD formatter - address pointer 15 (FMTAPTR15) register is shown in Figure 230 and described in Table 163 .

Figure 230. CCD Formatter Address Pointer (FMTAPTR15) Register

31-16
Reserved
R-0

15	14-13	12-0
Reserved	LINE	INIT
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 163. CCD Formatter Address pointer (FMTAPTR15) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	0	Any writes to these bit(s) must always have a value of 0.
14-13	LINE		The output line the address belongs to Valid only if FMTCBL is cleared
		0	1st line
		1	2nd line
		2	3rd line
		3	4th line
12-0	INIT	0-1FFFh	Initial address value for address pointer 15 This address can not exceed FMTRLEN - 1

6.1.93 CCD Formatter Program Valid Flags #0 (FMTPGMVF0) Register

The CCD formatter - program valid flags #0 (FMTPGMVF0) register is shown in Figure 231 and described in Table 164.

Figure 231. CCD Formatter Program Valid Flags #0 (FMTPGMVF0) Register

31-16
Reserved
R-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PGM15EN	PGM14EN	PGM13EN	PGM12EN	PGM11EN	PGM10EN	PGM09EN	PGM08EN	PGM07EN	PGM06EN	PGM05EN	PGM04EN	PGM03EN	PGM02EN	PGM01EN	PGM00EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 164. CCD Formatter Program Valid Flags #0 (FMTPGMVF0) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15	PGM15EN		Program 15 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
14	PGM14EN		Program 14 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
13	PGM13EN		Program 13 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
12	PGM12EN		Program 12 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
11	PGM11EN		Program 11 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
10	PGM10EN		Program 10 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
9	PGM09EN		Program 9 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
8	PGM08EN		Program 8 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
7	PGM07EN		Program 7 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
6	PGM06EN		Program 6 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
5	PGM05EN		Program 5 Valid Flag
		0	Skip this pixel
		1	This pixel is valid

Table 164. CCD Formatter Program Valid Flags #0 (FMTPGMVF0) Field Descriptions (continued)

Bit	Field	Value	Description
4	PGM04EN		Program 4 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
3	PGM03EN		Program 3 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
2	PGM02EN		Program 2 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
1	PGM01EN		Program 1 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
0	PGM00EN		Program 0 Valid Flag
		0	Skip this pixel
		1	This pixel is valid

6.1.94 CCD Formatter Program Valid Flags #1 (FMTPGMVF1) Register

The CCD formatter - program valid flags #1 (FMTPGMVF1) register is shown in Figure 232 and described in Table 165.

Figure 232. CCD Formatter Program Valid Flags #1 (FMTPGMVF1) Register

31-16
Reserved
R-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PGM31EN	PGM30EN	PGM29EN	PGM28EN	PGM27EN	PGM26EN	PGM25EN	PGM24EN	PGM23EN	PGM22EN	PGM21EN	PGM20EN	PGM19EN	PGM18EN	PGM17EN	PGM16EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 165. CCD Formatter Program Valid Flags #1 (FMTPGMVF1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15	PGM31EN		Program 31 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
14	PGM30EN		Program 30 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
13	PGM29EN		Program 29 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
12	PGM28EN		Program 28 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
11	PGM27EN		Program 27 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
10	PGM26EN		Program 26 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
9	PGM25EN		Program 25 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
8	PGM24EN		Program 24 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
7	PGM23EN		Program 23 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
6	PGM22EN		Program 22 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
5	PGM21EN		Program 21 Valid Flag
		0	Skip this pixel
		1	This pixel is valid

Table 165. CCD Formatter Program Valid Flags #1 (FMTPGMVF1) Field Descriptions (continued)

Bit	Field	Value	Description
4	PGM20EN		Program 20 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
3	PGM19EN		Program 19 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
2	PGM18EN		Program 18 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
1	PGM17EN		Program 17 Valid Flag
		0	Skip this pixel
		1	This pixel is valid
0	PGM16EN		Program 16 Valid Flag
		0	Skip this pixel
		1	This pixel is valid

6.1.95 CCD Formatter Program Address Pointer #0 (FMTPGMAPU0)

The CCD formatter - program address pointer #0 (FMTPGMAPU0) register is shown in Figure 233 and described in Table 166.

Figure 233. CCD Formatter Program Address Pointer #0 (FMTPGMAPU0) Register

31-16
Reserved
R-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PGM15UPDT	PGM14UPDT	PGM13UPDT	PGM12UPDT	PGM11UPDT	PGM10UPDT	PGM9UPDT	PGM8UPDT	PGM7UPDT	PGM6UPDT	PGM5UPDT	PGM4UPDT	PGM3UPDT	PGM2UPDT	PGM1UPDT	PGM0UPDT
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 166. CCD Formatter Program Address Pointer #0 (FMTPGMAPU0) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15	PGM15UPDT		Program 15 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
14	PGM14UPDT		Program 14 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
13	PGM13UPDT		Program 13 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
12	PGM12UPDT		Program 12 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
11	PGM11UPDT		Program 11 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
10	PGM10UPDT		Program 10 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
9	PGM9UPDT		Program 9 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
8	PGM8UPDT		Program 8 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
7	PGM7UPDT		Program 7 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
6	PGM6UPDT		Program 6 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)

Table 166. CCD Formatter Program Address Pointer #0 (FMTPGMAPU0) Field Descriptions (continued)

Bit	Field	Value	Description
5	PGM5UPDT		Program 5 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
4	PGM4UPDT		Program 4 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
3	PGM3UPDT		Program 3 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
2	PGM2UPDT		Program 2 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
1	PGM1UPDT		Program 1 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
0	PGM0UPDT		Program 0 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)

6.1.96 CCD Formatter Program Address Pointer #1 (FMTPGMAPU1)

The CCD formatter - program address pointer #1 (FMTPGMAPU1) register is shown in Figure 234 and described in Table 167.

Figure 234. CCD Formatter Program Address Pointer #1 (FMTPGMAPU1)

31-16
Reserved
R-0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PGM31UPDT	PGM30UPDT	PGM29UPDT	PGM28UPDT	PGM27UPDT	PGM26UPDT	PGM25UPDT	PGM24UPDT	PGM23UPDT	PGM22UPDT	PGM21UPDT	PGM20UPDT	PGM19UPDT	PGM18UPDT	PGM17UPDT	PGM16UPDT
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 167. CCD Formatter Program Address Pointer #1 (FMTPGMAPU1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15	PGM31UPDT		Program 31 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
14	PGM30UPDT		Program 30 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
13	PGM29UPDT		Program 29 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
12	PGM28UPDT		Program 28 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
11	PGM27UPDT		Program 27 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
10	PGM26UPDT		Program 26 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
9	PGM25UPDT		Program 25 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
8	PGM24UPDT		Program 24 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
7	PGM23UPDT		Program 23 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
6	PGM22UPDT		Program 22 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)

Table 167. CCD Formatter Program Address Pointer #1 (FMTPGMAPU1) Field Descriptions (continued)

Bit	Field	Value	Description
5	PGM21UPDT		Program 21 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
4	PGM20UPDT		Program 20 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
3	PGM19UPDT		Program 19 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
2	PGM18UPDT		Program 18 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
1	PGM17UPDT		Program 17 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)
0	PGM16UPDT		Program 16 Address Pointer Update
		0	APTR* + N (Auto increment)
		1	APTR* - N (Auto decrement)

6.1.97 CCD Formatter Program Address Pointer Select (FMTPGMAPS0)

The CCD formatter - program address pointer select 0 (FMTPGMAPS0) register is shown in Figure 235 and described in Table 168.

Figure 235. CCD Formatter Program Address Pointer Select 0 (FMTPGMAPS0) Register

31-16			
Reserved			
R-0			
15-12	11-8	7-4	3-0
PGM3APTR	PGM2APTR	PGM1APTR	PGM0APTR
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 168. CCD Formatter Program Address Pointer Select 0 (FMTPGMAPS0) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-12	PGM3APTR	0-Fh	Program 3 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
11-8	PGM2APTR	0-Fh	Program 2 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
7-4	PGM1APTR	0-Fh	Program 1 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
3-0	PGM0APTR	0-Fh	Program 0 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)

6.1.98 CCD Formatter Program Address Pointer Select 1 (FMTPGMAPS1)

The CCD formatter - program address pointer select 1(FMTPGMAPS1) register is shown in Figure 236 and described in Table 169.

Figure 236. CCD Formatter Program Address Pointer Select 1 (FMTPGMAPS1) Register

31-16
Reserved
R-0

15-12	11-8	7-4	3-0
PGM7APTR	PGM6APTR	PGM5APTR	PGM4APTR
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 169. CCD Formatter Program Address Pointer Select 1 (FMTPGMAPS1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-12	PGM7APTR	0-Fh	Program 7 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
11-8	PGM6APTR	0-Fh	Program 6 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
7-4	PGM5APTR	0-Fh	Program 5 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
3-0	PGM4APTR	0-Fh	Program 4 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)

6.1.99 CCD Formatter Program Address Pointer Select 2 (FMTPGMAPS2)

The CCD formatter - program address pointer select 2 (FMTPGMAPS2) register is shown in Figure 237and described in Table 170.

Figure 237. CCD Formatter Program Address Pointer Select 2 (FMTPGMAPS2) Register

31-16
Reserved
R-0

15-12	11-8	7-4	3-0
PGM11APTR	PGM10APTR	PGM9APTR	PGM8APTR
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 170. CCD Formatter Program Address Pointer Select 2 (FMTPGMAPS2) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-12	PGM11APTR	0-Fh	Program 11 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
11-8	PGM10APTR	0-Fh	Program 10 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
7-4	PGM9APTR	0-Fh	Program 9 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
3-0	PGM8APTR	0-Fh	Program 8 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)

6.1.100 CCD Formatter Program Address Pointer Select 3 (FMTPGMAPS3)

The CCD formatter - program address pointer select 3 (FMTPGMAPS3) register is shown in Figure 238and described in Table 171.

Figure 238. CCD Formatter Program Address Pointer Select 3 (FMTPGMAPS3)

31-16
Reserved
R-0

15-12	11-8	7-4	3-0
PGM15APTR	PGM14APTR	PGM13APTR	PGM12APTR
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 171. CCD Formatter Program Address Pointer Select 3 (FMTPGMAPS3) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-12	PGM15APTR	0-Fh	Program 15 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
11-8	PGM14APTR	0-Fh	Program 14 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
7-4	PGM13APTR	0-Fh	Program 13 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
3-0	PGM12APTR	0-Fh	Program 12 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)

6.1.101 CCD Formatter Program Address Pointer Select 4 (FMTPGMAPS4)

The CCD formatter - program address pointer select 4 (FMTPGMAPS4) register is shown in Figure 239 and described in Table 172.

Figure 239. CCD Formatter Program Address Pointer Select 4 (FMTPGMAPS4)

31-16			
Reserved			
R-0			
15-12	11-8	7-4	3-0
PGM19APTR	PGM18APTR	PGM17APTR	PGM16APTR
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 172. FCCD Formatter Program Address Pointer Select 4 (FMTPGMAPS4) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-12	PGM19APTR	Fh	Program 19 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
11-8	PGM18APTR	0-Fh	Program 18 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
7-4	PGM17APTR	0-Fh	Program 17 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
3-0	PGM16APTR	0-Fh	Program 16 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)

6.1.102 CCD Formatter Program Address Pointer Select 5 (FMTPGMAPS5)

The CCD formatter - program address pointer select 5 (FMTPGMAPS5) register is shown in Figure 240 and described in Table 173.

Figure 240. CCD Formatter Program Address Pointer Select 5 (FMTPGMAPS5) Register

31-16			
Reserved			
R-0			
15-12	11-8	7-4	3-0
PGM23APTR	PGM22APTR	PGM21APTR	PGM20APTR
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 173. CCD Formatter Program Address Pointer Select 5 (FMTPGMAPS5) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-12	PGM23APTR	0-Fh	Program 23 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
11-8	PGM22APTR	0-Fh	Program 22 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
7-4	PGM21APTR	0-Fh	Program 21 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
3-0	PGM20APTR	0-Fh	Program 20 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)

6.1.103 CCD Formatter Program Address Pointer Select 6 (FMTPGMAPS6)

The CCD formatter - program address pointer select 6 (FMTPGMAPS6) register is shown in Figure 241 and described in Table 174.

Figure 241. CCD Formatter Program Address Pointer Select 6 (FMTPGMAPS6) Register

31-16
Reserved
R-0

15-12	11-8	7-4	3-0
PGM27APTR	PGM26APTR	PGM25APTR	PGM24APTR
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 174. CCD Formatter Program Address Pointer Select 6 (FMTPGMAPS6) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-12	PGM27APTR	0-Fh	Program 27 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
11-8	PGM26APTR	0-Fh	Program 26 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
7-4	PGM25APTR	0-Fh	Program 25 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
3-0	PGM24APTR	0-Fh	Program 24 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)

6.1.104 CCD Formatter Program Address Pointer Select 7 (FMTPGMAPS7)

The CCD formatter - program address pointer select 7 (FMTPGMAPS7) register is shown in Figure 242 and described in Table 175 .

Figure 242. CCD Formatter Program Address Pointer Select 7 (FMTPGMAPS7) Register

31-16			
Reserved			
R-0			
15-12	11-8	7-4	3-0
PGM31APTR	PGM30APTR	PGM29APTR	PGM28APTR
R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 175. CCD Formatter Program Address Pointer Select 7 (FMTPGMAPS7) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-12	PGM31APTR	0-Fh	Program 31 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
11-8	PGM30APTR	0-Fh	Program 30 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
7-4	PGM29APTR	0-Fh	Program 29 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)
3-0	PGM28APTR	0-Fh	Program 28 Address Pointer Select n: APTRn n:0-15 (APTR0 - APR15)

6.1.105 Color Space Converter Enable (CSCCTL)

The color space converter enable (CSCCTL) register is shown in Figure 243and described in Table 176.

Figure 243. Color Space Converter Enable (CSCCTL) Register

31-16
Reserved
R-0

15-1	0
Reserved	CSCEN
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 176. Color Space Converter Enable (CSCCTL) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	CSCEN		Controls ON/OFF of Color Space Converter
		0	Disable
		1	Enable

6.1.106 Color Space Converter Coefficients #0 (CSCM0)

The color space converter - coefficients #0 (CSCM0) register is shown in Figure 244 and described in Table 177.

Figure 244. Color Space Converter Coefficients #0 (CSCM0) Register

31-16	
Reserved	
R-0	
15-8	7-0
CSCM01	CSCM00
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 177. Color Space Converter Coefficients #0 (CSCM0) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CSCM01	0-FFh	Color space conversion coefficient value M01 This value is S8Q5
7-0	CSCM00	0-FFh	Color space conversion coefficient value M00 This value is S8Q5

6.1.107 Color Space Converter Coefficients #1 (CSCM1)

The color space converter - coefficients #1 (CSCM1) register is shown in Figure 245 and described in Table 178.

Figure 245. Color Space Converter Coefficients #1 (CSCM1) Register

31-16	
Reserved	
R-0	
15-8	7-0
CSCM03	CSCM02
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 178. Color Space Converter Coefficients #1 (CSCM1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CSCM03	0-FFh	Color space conversion coefficient value M03 This value is S8Q5
7-0	CSCM02	0-FFh	Color space conversion coefficient value M02 This value is S8Q5

6.1.108 Color Space Converter Coefficients #2 (CSCM2)

The color space converter - coefficients #2 (CSCM2) register is shown in Figure 246 and described in Figure 246.

Figure 246. Color Space Converter Coefficients #2 (CSCM2) Register

31-16
Reserved
R-0

15-8	7-0
CSCM11	CSCM10
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 179. Color Space Converter Coefficients #2 (CSCM2) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CSCM11	0-FFh	Color space conversion coefficient value M11 This value is S8Q5
7-0	CSCM10	0-FFh	Color space conversion coefficient value M10 This value is S8Q5

6.1.109 Color Space Converter Coefficients #3 (CSCM3)

The color space converter - coefficients #3 (CSCM3) register is shown in Figure 247 and described in Table 180.

Figure 247. Color Space Converter Coefficients #3 (CSCM3) Register

31-16
Reserved
R-0

15-8	7-0
CSCM13	CSCM12
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 180. Color Space Converter Coefficients #3 (CSCM3) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CSCM13	0-FFh	Color space conversion coefficient value M13 This value is S8Q5
7-0	CSCM12	0-FFh	Color space conversion coefficient value M12 This value is S8Q5

6.1.110 Color Space Converter Coefficients #4 (CSCM4)

The color space converter - coefficients #4 (CSCM4) register is shown in Figure 248 and described in Table 181.

Figure 248. Color Space Converter Coefficients #4 (CSCM4) Register

31-16
Reserved
R-0

15-8	7-0
CSCM21	CSCM20
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 181. Color Space Converter Coefficients #4 (CSCM4) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CSCM21	0-FFh	Color space conversion coefficient value M21 This value is S8Q5
7-0	CSCM20	0-FFh	Color space conversion coefficient value M20 This value is S8Q5

6.1.111 Color Space Converter Coefficients #5 (CSCM5)

The color space converter - coefficients #5 (CSCM5) register is shown in Figure 249 and described in Table 182.

Figure 249. Color Space Converter Coefficients #5 (CSCM5) Register

31-16
Reserved
R-0

15-8	7-0
CSCM23	CSCM22
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 182. Color Space Converter Coefficients #5 (CSCM5) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CSCM23	0-FFh	Color space conversion coefficient value M23 This value is S8Q5
7-0	CSCM22	0-FFh	Color space conversion coefficient value M22 This value is S8Q5

6.1.112 Color Space Converter Coefficients #6 (CSCM6)

The color space converter - coefficients #6 register (CSCM6)is shown in Figure 250 and described in Table 183.

Figure 250. Color Space Converter Coefficients #6 (CSCM6) Register

31-16	
Reserved	
R-0	
15-8	7-0
CSCM31	CSCM30
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 183. Color Space Converter Coefficients #6 (CSCM6) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CSCM31	0-FFh	Color space conversion coefficient value M31 This value is S8Q5
7-0	CSCM30	0-FFh	Color space conversion coefficient value M30 This value is S8Q5

6.1.113 Color Space Converter Coefficients #7 (CSCM7)

The color space converter - coefficients #7 (CSCM7) register is shown in Figure 251 and described in Table 184.

Figure 251. Color Space Converter Coefficients #7 (CSCM7) Register

31-16	
Reserved	
R-0	
15-8	7-0
CSCM33	CSCM32
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 184. Color Space Converter Coefficients #7 (CSCM7) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	CSCM33	0-FFh	Color space conversion coefficient value M33 This value is S8Q5
7-0	CSCM32	0-FFh	Color space conversion coefficient value M32 This value is S8Q5

6.2 Image Pipe Input Interface Registers (IPIPEIF) Registers

The Image Pipe Input Interface registers are shown in Table 185.

Table 185. Image Pipe Input Interface Register Map (IPIPEIF)

Offset	Acronym	Register Description	Section
0h	ENABLE	IPIPE I/F Enable	Section 6.2.1
04h	CFG1	IPIPE I/F Configuration 1	Section 6.2.2
08h	PPLN	IPIPE I/F Interval of HD / Start pixel in HD	Section 6.2.3
0Ch	LPFR	IPIPE I/F Interval of VD / Start line in VD	Section 6.2.4
10h	HNUM	IPIPE I/F Number of valid pixels per line	Section 6.2.5
14h	VNUM	IPIPE I/F Number of valid lines per frame	Section 6.2.6
18h	ADDRU	IPIPE I/F Memory address (upper)	Section 6.2.7
1Ch	ADDRL	IPIPE I/F Memory address (lower)	Section 6.2.8
20h	ADOFS	IPIPE I/F Address offset of each line	Section 6.2.9
24h	RSZ	IPIPE I/F Horizontal resizing parameter	Section 6.2.10
28h	GAIN	IPIPE I/F Gain parameter	Section 6.2.11
2Ch	DPCM	IPIPE I/F DPCM configuration	Section 6.2.12
30h	CFG2	IPIPE I/F Configuration 2	Section 6.2.13
34h	INIRSZ	IPIPE I/F Initial position of resize	Section 6.2.14
38h	OCLIP	IPIPE I/F Output clipping value	Section 6.2.15
3Ch	DTUDF	IPIPE I/F Data underflow error status	Section 6.2.16
40h	CLKDIV	IPIPE I/F Clock rate configuration	Section 6.2.17
44h	DPC1	IPIPE I/F Defect pixel correction	Section 6.2.18
48h	DPC2	IPIPE I/F Defect pixel correction	Section 6.2.19
54h	RSZ3A	IPIPE I/F Horizontal resizing parameter for H3A	Section 6.2.20
58h	INIRSZ3A	IPIPE I/F Initial position of resize for H3A	Section 6.2.21

6.2.1 IPIPE I/F Enable (ENABLE)

The IPIPE I/F Enable (ENABLE) register is shown in Figure 252 and described in Table 186.

Figure 252. IPIPE I/F Enable (ENABLE) Register

31-16		
Reserved		
R-0		
15-2	**1**	**0**
Reserved	SYNCOFF	ENABLE
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 186. IPIPE I/F Enable (ENABLE) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	SYNCOFF		SYNC out mask This register masks the VSUNC output to other module.
		0	VSYNC output enable
		1	VSYNC output disable
0	ENABLE		IPIPE I/F Enable This register is used to start the operation of SDRAM buffer memory read and generates SYNC signals. This register is available when INPSRC (CFG[3:2]) = 1, 2, or 3.
		0	Disable
		1	Enable

6.2.2 IPIPE I/F Configuration 1 (CFG1)

The IPIPE I/F Configuration 1 (CFG1) register is shown in Figure 253 and described in Table 187.

Figure 253. IPIPE I/F Configuration 1 (CFG1) Register

31-16				
Reserved				
R-0				
15-14	**13-11**	**10**	**9-8**	
INPSRC1	DATASFT	CLKSEL	UNPACK	
R/W-0	R/W-0	R/W-0	R/W-0	
7	**6-4**	**3-2**	**1**	**0**
AVGFILT	Reserved	INPSRC2	DECM	ONESHOT
R/W-0	R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 187. IPIPE I/F Configuration 1 (CFG1) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-14	INPSRC1		Parallel Port/YCbCr Data Port Selection
		0	from Parallel Port/
		1h	from SDRAM (raw data)
		2h	from Parallel Port & SDRAM (Darkframe)
		3h	from SDRAM (YUV data)
13-11	DATASFT		SDRAM Read Data Shift (0-7) This register is available when INPSRCx = 1 or 2.
		0	Output data (13:0) = read data(13:0)
		1h	Output data (13:0) = read data(12:0) & "0"
		2h	Output data (13:0) = read data(11:0) & "00"
		3h	Output data (13:0) = read data(10:0) & "000"
		4h	Output data (13:0) = read data(9:0) & "0000"
		5h	Output data (13:0) = read data(8:0) & "00000"
		6h	Output data (13:0) = read data(7:0) & "000000"
		7h	Output data (13:0) = read data(15:2)
10	CLKSEL		IPIPEIF & IPIPE Clock Select This register is available when INPSRCx = 1 or 3. Should code "0" when INPSRCx = 0 or 2.
		0	pixel clock (PCLK)
		1	divided SDRAM clock as per CLKDIV
9-8	UNPACK		8/12-Bit Packed Mode When CCD raw data is stored in 8-bit packed mode or 12-bit packed mode, this register should code "1" or "3". This register is effective when INPSRCx = 1 or 2.
		0	16 bits / pixel
		1h	8 bits / pixel
		2h	8 bits / pixel+inverse Alaw(8-10)
		3h	12 bits / pixel
7	AVGFILT		Averaging Filter It applies (1,2,1) filter for the RGB/YCbCr data.
		0	off
		1	on
6-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.

Table 187. IPIPE I/F Configuration 1 (CFG1) Field Descriptions (continued)

Bit	Field	Value	Description
3-2	INPSRC2		ISIF/YCbCr Data Port Selection
		0	from ISIF
		1h	from SDRAM (raw data)
		2h	from ISIF & SDRAM (Darkframe)
		3h	from SDRAM (YUV data)
1	DECIM		Pixel Decimation rate defined by RSZ register
		0	no decimation
		1	decimate
0	ONESHOT		One Shot Mode This register is available when INPSRCx = 1 or 3.
		0	continuous mode
		1	one shot mode

6.2.3 IPIPE I/F Interval of HD / Start Pixel in HD (PPLN)

The IPIPE I/F Interval of HD / Start pixel in HD register is shown in Figure 254 and described in Table 188.

Figure 254. IPIPE I/F Interval of HD / Start pixel in HD (PPLN)

31-16
Reserved
R-0

15-13	12-0
Reserved	PPLN
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 188. IPIPE I/F Interval of HD / Start pixel in HD (PPLN) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	PPLN	0-1FFFh	Case-1: Interval of Horizontal Sync (HD) Specifies the interval of horizontal sync. This register is available when INPSRCx = 1 or 3. Case-2: Start Pixel in Horizontal Sync (HD) Specifies the start pixel in horizontal sync. This register is available when INPSRCx = 2

6.2.4 IPIPE I/F Interval of VD / Start Line in VD (LPFR)

The IPIPE I/F Interval of VD / Start line in VD register is shown in Figure 255 and described in Table 189.

Figure 255. IPIPE I/F Interval of VD / Start line in VD (LPFR) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	LPFR
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 189. IPIPE I/F Interval of VD / Start line in VD (LPFR) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	LPFR	0-1FFFh	Case-1: Interval of Vertical Sync (VD) Specifies the interval of vertical sync. This register is available when INPSRCx = 1 or 3. Case-2: Start Pixel in Vertical Sync (VD) Specifies the start line in vertical sync. This register is available when INPSRCx = 2

6.2.5 IPIPE I/F Number of Valid Pixels per Line (HNUM)

The IPIPE I/F (HNUM) register is shown in Figure 256 and described in Table 190.

Figure 256. IPIPE I/F Number of Valid Pixels per Line (HNUM) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	HNUM
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 190. IPIPE I/F Number of Valid Pixels per Line (HNUM) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	HNUM	0-1FFFh	The Number of Valid Pixel in a Line Specifies the number of valid pixel in a horizontal line. This register is available when INPSRCx = 1, 2 or 3

6.2.6 IPIPE I/F Number of Valid Lines per Frame (VNUM)

The IPIPE I/F (VNUM) register is shown in Figure 257 and described in Table 191.

Figure 257. IPIPE I/F Number of valid Lines per Frame (VNUM) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VNUM
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 191. IPIPE I/F Number of Valid Lines per Frame (VNUM) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VNUM	0-1FFFh	The Number of Valid Line in a Vertical Specifies the number of valid line in a vertical. This register is available when INPSRCx = 1, 2 or 3

6.2.7 IPIPE I/F Memory Address (Upper) (ADDRU)

The PIPE I/F memory address (Upper)(ADDRU) register is shown in Figure 258 and described in Table 192.

Figure 258. IPIPE I/F Memory Address (Upper)(ADDRU) Register

31-16
Reserved
R-0

15-11	10	9	8-0
Reserved	ADDRMSB	ADOFS9	ADDRMSB
R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 192. IPIPE I/F Memory Address (Upper)(ADDRU) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10	ADDRMSB	0-1	Memory Address – MSB. This register is available when INPSRCx = 1, 2 or 3.
9	ADOFS9	0-1	The Address Offset of each line - MSB bit. This register is available when INPSRCx = 1, 2 or 3.
8-0	ADDRMSB	0-1FFh	Memory Address – Upper This register is available when INPSRCx = 1, 2 or 3.

6.2.8 IPIPE I/F Memory Address (Lower) (ADDRL)

The IPIPE I/F memory address (Lower)(ADDRL) register is shown in Figure 259 and described in Table 193.

Figure 259. IPIPE I/F Memory Address (Lower)(ADDRL) Register

31-16
Reserved
R-0

15-0
ADDRL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 193. IPIPE I/F Memory Address (Lower)(ADDRL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	ADDRL	0-FFFFh	Memory Address – Lower Memory address lower 16-bits are specified in units of 32-bytes. This register is available when INPSRCx = 1, 2 or 3.

6.2.9 IPIPE I/F Address Offset of Each Line (ADOFS)

The IPIPE I/F address offset of each line (ADOFS) register is shown in Figure 260 and described in Table 194.

Figure 260. IPIPE I/F Address Offset of Each Line (ADOFS) Register

31-16
Reserved
R-0

15-9	8-0
Reserved	ADOFS
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 194. IPIPE I/F Address offset of Each Line (ADOFS) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Any writes to these bit(s) must always have a value of 0.
8-0	ADOFS	0-1FFh	The Address Offset of each line Specifies the offset address each start line is specified in units of 32-bytes. This register is available when INPSRCx = 1, 2 or 3.

6.2.10 IPIPE I/F Horizontal Resizing Parameter (RSZ)

The IPIPE I/F horizontal resizing parameter (RSZ) register is shown in Figure 261 and described in Table 195.

Figure 261. IPIPE I/F Horizontal Resizing Parameter (RSZ) Register

31-16
Reserved
R-0

15-7	6-0
Reserved	RSZ
R-0	R/W-16

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 195. IPIPE I/F Horizontal Resizing Parameter (RSZ) Field Descriptions

Bit	Field	Value	Description
31-7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6-0	RSZ	0-7Fh	The Horizontal Resizing Parameter. Specifies the horizontal resizing parameter. The RSZ register can be configured within 16 to 112 range. This resizing ratio is determined by 16/RSZ (= 1/1 to 1/7)

6.2.11 IPIPE I/F Gain Parameter (GAIN)

The IPIPE I/F gain parameter (GAIN) register is shown in Figure 262 and described in Table 196.

Figure 262. IPIPE I/F Gain Parameter (GAIN) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	GAIN
R-0	R/W-512

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 196. IPIPE I/F Gain Parameter (GAIN) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	GAIN	0-3FFh	Gain Parameter. Specifies the gain parameter for IPIPE output data. The GAIN register can be configured within 0.00195(1/512) to 1.99805(1023/512) range. This gain default value is x1 gain. These bits don't influence Data of YCC.

6.2.12 IPIPE I/F DPCM Configuration (DPCM)

The IPIPE I/F DPCM configuration (DPCM) register is shown in Figure 263and described in Table 197.

Figure 263. IPIPE I/F DPCM Configuration (DPCM) Register

31-16
Reserved
R-0

15-3	2	1	0
Reserved	BITS	PRED	ENA
R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 197. IPIPE I/F DPCM Configuration (DPCM) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2	BITS		DPCM Decompression Mode
		0	8bit to 10bit DPCM
		1	8bit to 12bit DPCM
1	PRED		DPCM Prediction Mode
		0	Simple Predictor
		1	Advanced Predictor
0	ENA		DPCM Decompression enable
		0	DPCM off (no decompress)
		1	DPCM on

6.2.13 IPIPE I/F Configuration 2 (CFG2)

The IPIPE I/F configuration 2 (CFG2) register is shown in Figure 264 and described in Table 198.

Figure 264. IPIPE I/F Configuration 2 (CFG2) Register

31-8							
Reserved							
R-0							
7	6	5	4	3	2	1	0
YUV8P	YUV8	DFSDIR	WENE	YUV16	VDPOL	HDPOL	INTSRC
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 198. IPIPE I/F Configuration 2 (CFG2) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7	YUV8P	0-1	Y/C phase When YUV8 is selected, YUV8P specifies the Chroma phase (odd or even pixel).
6	YUV8		YUV 8bit mode When INPTYP is 1YUV16bit mode and YUV8 is 1, it converts 8bit data to 16bit data and drives to IPIPE.
		0	YUV 16bit mode
		1	YUV 8bit mode
5	DFSDIR		DFS direction of subtraction
		0	
		1	
4	WENE		External WEN Selection When set to 1 and when ENABLE is set to 1, the external WEN signal is used to recognize the valid pixel for resize filter calculation.
		0	do not use external WEN (Write Enable)
		1	use external WEN (Write Enable)
3	YUV16		Input Type This register is available when CFG1.INPSRC2 = 0. Should code "0" otherwise.
		0	RAW sensor data
		1	YUV 16-bit data
2	VDPOL		VD Sync Polarity When input VD is active low SYNC pulse, should set to '1'
		0	positive
		1	negative
1	HDPOL		HD Sync Polarity When input HD is active low SYNC pulse, should set to '1'
		0	positive
		1	negative
0	INTSRC		IPIPE I/F Interrupt Source Select
		0	start position of VD from parallel port
		1	start position of VD from ISIF

6.2.14 IPIPE I/F Initial Position of Resize (INIRSZ)

The IPIPE I/F initial position of resize (INIRSZ) register is shown in Figure 265 and described in Table 199.

Figure 265. IPIPE I/F Initial Position of Resize (INIRSZ) Register

31-16
Reserved
R-0

15-14	13	12-0
Reserved	ALNSYNC	INIRSZ
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 199. IPIPE I/F Initial Position of Resize (INIRSZ) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13	ALNSYNC	0-1	Force the HD and VD align with start position. writing 1 align the HD/VD position to initial data position which is specified by INIRSZ
12-0	INIRSZ	0-1FFFh	Initial Position of Resizer Specifies the initial position from HD for resize

6.2.15 IPIPE I/F Output Clipping Value (OCLIP)

The IPIPE I/F output clipping value (OCLIP) register is shown in Figure 266 and described in Table 200 .

Figure 266. IPIPE I/F Output Clipping Value (OCLIP) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	OCLIP
R-0	R/W-4095

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 200. IPIPE I/F Output Clipping Value (OCLIP) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	OCLIP	0-FFFh	Output Clipping Value after gain Control

6.2.16 IPIPE I/F Data Underflow Error Status (DTUDF)

The IPIPE I/F data underflow error status (DTUDF) register is shown in Figure 267 and described in Table 201.

Figure 267. IPIPE I/F Data Underflow Error Status (DTUDF) Register

31-16
Reserved
R-0

15-1	0
Reserved	DTUDF
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 201. IPIPE I/F Data Underflow Error Status (DTUDF) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	DTUDF	0-1	Data Underflow Error Status. Reading '1' shows there is data under flow and at least one data is corrupted while reading from SDRAM. Writing '1' to this register clears (=0) the error (=1) status. Programmers need to configure proper read clock frequency or SDRAM priority to avoid the data underflow.

6.2.17 IPIPE I/F Clock Rate Configuration (CLKDIV)

The IPIPE I/F clock rate configuration (CLKDIV) register is shown in Figure 268 and described in Table 202.

Figure 268. IPIPE I/F Clock Rate Configuration (CLKDIV) Register

31-16
Reserved
R-0

15-0
CLKDIV
R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 202. IPIPE I/F Clock Rate Configuration(CLKDIV) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	CLKDIV	0-FFFFh	Clock rate configuration clock rate = M/N x VPSS clock rate M=CLKDIV[15:8]+1,N=CLKDIV[7:0]+1 M/N should not be greater than 1/2. This configuration is effective only when CONFIG1.CLKSEL=1

6.2.18 IPIPE I/F Defect Pixel Correction (DPC1)

The IPIPE I/F defect pixel correction (DPC1) register is shown in Figure 269 and described in Table 203.

Figure 269. IPIPE I/F Defect Pixel Correction (DPC1) Register

31-16
Reserved
R-0

15-13	12	11-0
Reserved	ENA	TH
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 203. IPIPE I/F Defect Pixel Correction (DPC1) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12	ENA		DPC enable applies DPC for VPIF,ISIF input path
		0	off
		1	on
11-0	TH	0-FFFh	DPC threshold value

6.2.19 PIPE I/F Defect Pixel Correction (DPC2)

The IPIPE I/F defect pixel correction (DPC2) register is shown inFigure 270 and described in Table 204.

Figure 270. IPIPE I/F Defect Pixel Correction (DPC2) Register

31-16
Reserved
R-0

15-13	12	11-0
Reserved	ENA	TH
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

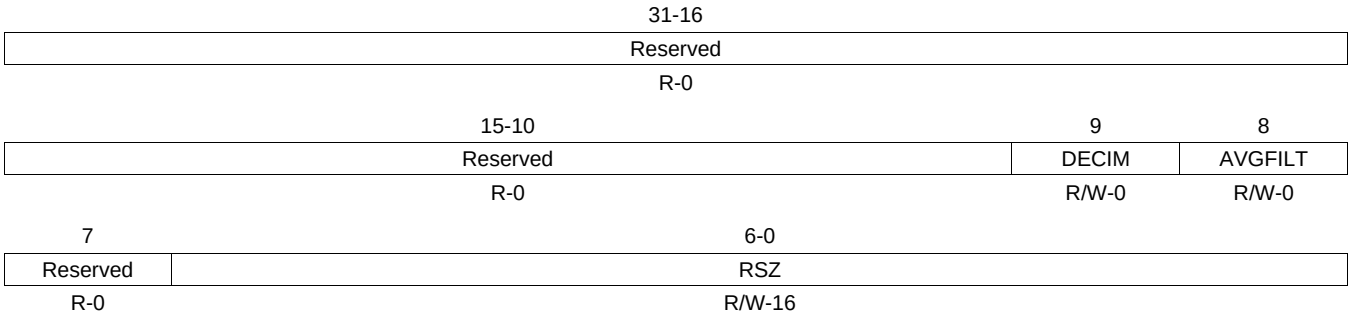
Table 204. IPIPE I/F Defect Pixel Correction (DPC2) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12	ENA		DPC enable applies DPC for SDRAM input path.
		0	off
		1	on
11-0	TH	0-FFFh	DPC threshold value

6.2.20 IPIPE I/F Horizontal Resizing Parameter for H3A (RSZ3A)

The IPIPE I/F horizontal resizing parameter for H3A (RSZ3A) register is shown in Figure 271 and described in Table 205.

Figure 271. IPIPE I/F Horizontal Resizing Parameter for H3A (RSZ3A) Register



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

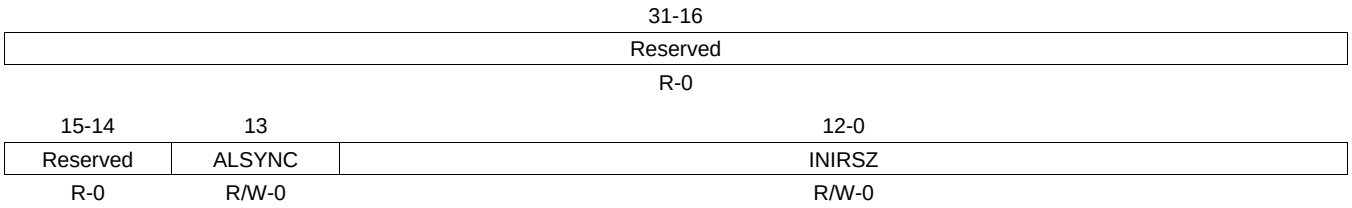
Table 205. IPIPE I/F Horizontal Resizing Parameter for H3A (RSZ3A) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9	DECIM		Pixel Decimation rate defined by RSZ register.
		0	no decimation
		1	decimate
8	AVGFILT		Averaging Filter It applies (1,2,1) filter for the RGB/YCbCr data.
		0	off
		1	on
7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6-0	RSZ	0-7Fh	The Horizontal Resizing Parameter Specifies the horizontal resizing parameter. The RSZ register can be configured within 16 to 112 range. This resizing ratio is determined by 16/RSZ (= 1/1 to 1/7)

6.2.21 PIPE I/F Initial Position of Resize for H3A (INIRSZ3A)

The IPIPE I/F initial position of resize for H3A (INIRSZ3A) register is shown in Figure 272 and described in Table 206.

Figure 272. IPIPE I/F Initial Position of Resize for H3A (INIRSZ3A) Register



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 206. IPIPE I/F Initial Position of Resize for H3A (INIRSZ3A) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13	ALSYNC	0-1	Force the HD and VD align with start position. writing 1 align the HD/VD position to initial data position which is specified by INIRSZ3A
12-0	INIRSZ	0-1FFFh	Initial Position of Resizer Specifies the initial position from HD for resize

6.3 Image Pipe (IPIPE) Registers

Table 207 lists the memory-mapped registers for the image pipe (IPIPE). See the device-specific data manual for the memory addresses of these registers.

Table 207. IPIPE Registers

Offset	Acronym	Register Description	Section
0h	SRC_EN	IPIPE Enable	Section 6.3.1
004h	SRC_MODE	One Shot Mode	Section 6.3.2
008h	SRC_FMT	Input/Output Data Paths	Section 6.3.3
00Ch	SRC_COL	Color Pattern	Section 6.3.4
010h	SRC_VPS	Vertical Start Position	Section 6.3.5
014h	SRC_VSZ	Vertical Processing Size	Section 6.3.6
018h	SRC_HPS	Horizontal Start Position	Section 6.3.7
01Ch	SRC_HSZ	Horizontal Processing Size	Section 6.3.8
024h	DMA_STA	Status Flags (Reserved)	Section 6.3.9
028h	GCK_MMR	MMR Gated Clock Control	Section 6.3.10
02Ch	GCK_PIX	PCLK Gated Clock Control	Section 6.3.11
030h	Reserved	Reserved	
034h	DPC_LUT_EN	LUTDPC: Enable	Section 6.3.12
038h	DPC_LUT_SEL	LUTDPC: Processing Mode Selection	Section 6.3.13
03Ch	DPC_LUT_ADR	LUTDPC: Start Address in LUT	Section 6.3.14
040h	DPC_LUT_SIZ	LUTDPC: Number of available entries in LUT	Section 6.3.15
044h	DPC_OTF_EN	OTFDPC (=On The Fly Defect Pixel Correction): Enable	Section 6.3.16
048h	DPC_OTF_TYP	OTFDPC: Algorithm Selection	Section 6.3.17
04Ch	DPC_OTF_2_D_THR_R	OTFDPC: DPC2.0 Defect Detection Threshold	Section 6.3.18
050h	DPC_OTF_2_D_THR_GR	OTFDPC: DPC2.0 Defect Detection Threshold	Section 6.3.19
054h	DPC_OTF_2_D_THR_GB	OTFDPC: DPC2.0 Defect Detection Threshold	Section 6.3.20
058h	DPC_OTF_2_D_THR_B	OTFDPC: DPC2.0 Defect Detection Threshold	Section 6.3.21
05Ch	DPC_OTF_2_C_THR_R	OTFDPC: DPC2.0 Defect Correction Threshold	Section 6.3.22
060h	DPC_OTF_2_C_THR_GR	OTFDPC: DPC2.0 Defect Correction Threshold	Section 6.3.23
064h	DPC_OTF_2_C_THR_Gb	OTFDPC: DPC2.0 Defect Correction Threshold	Section 6.3.24
068h	DPC_OTF_2_C_THR_B	OTFDPC: DPC2.0 Defect Correction Threshold	Section 6.3.25
06Ch-08Ch	Reserved	Reserved	
090h	LSC_VOFT	LSC (=Lens Shading Correction): Vertical Offset	Section 6.3.26
094h	LSC_VA2	LSC: Vertical Quadratic Coefficient	Section 6.3.27
098h	LSC_VA1	LSC: Vertical Linear Coefficient	Section 6.3.28
009Ch	LSC_VS	LSC: Vertical Quadratic/Linear Shift Length	Section 6.3.29
0A0h	LSC_HOFT	LSC: Horizontal Offset	Section 6.3.30
0A4h	LSC_HA2	LSC: Horizontal Quadratic Coefficient	Section 6.3.31
0A8h	LSC_HA1	LSC: Horizontal Linear Coefficient	Section 6.3.32
0ACh	LSC_HS	LSC: Horizontal Quadratic/Linear Shift Length	Section 6.3.33
0B0h	LSC_GAN_R	LSC: Total Gain	Section 6.3.34
0B4h	LSC_GAN_GR	LSC: Total Gain	Section 6.3.35
0B8h	LSC_GAN_GB	LSC: Total Gain	Section 6.3.36
0BCh	LSC_GAN_B	LSC: Total Gain	Section 6.3.37
0C0h	LSC_OFT_R	LSC: Total Offset	Section 6.3.38
0C4h	LSC_OFT_GR	LSC: Total Offset	Section 6.3.39
0C8h	LSC_OFT_GB	LSC: Total Offset	Section 6.3.40
0CCh	LSC_OFT_B	LSC: Total Offset	Section 6.3.41

Table 207. IPIPE Registers (continued)

Offset	Acronym	Register Description	Section
0D0h	LSC_SHF	LSC Gain Shift Length	Section 6.3.42
0D4h	LSC_MAX	LSC Gain Maximum Value	Section 6.3.43
0D8h	D2F_1ST_EN	NF1 (=1st 2D Noise Filter): Enable	Section 6.3.44
0DCh	D2F_1ST_TYP	NF1: Configuration	Section 6.3.45
0E0h	D2F_1ST_THR[8]	NF1: LUT Values (Threshold)	Section 6.3.46
100h	D2F_1ST_STR[8]	NF1: LUT Values (Intensity)	Section 6.3.47
140h	D2F_1ST_EDG_MIN	NF1: Edge Detection Minimum Threshold	Section 6.3.48
144h	D2F_1ST_EDG_MAX	NF1: Edge Detection Maximum Threshold	Section 6.3.49
148h	D2F_2ND_EN	NF2 (=2nd 2D Noise Filter): Enable	Section 6.3.50
14Ch	D2F_2ND_TYP	NF2: Configuration	Section 6.3.51
150h	D2F_2ND_THR[8]	NF2: LUT Values (Threshold)	Section 6.3.52
170h	D2F_2ND_STR[8]	NF2: LUT Values (Intensity)	Section 6.3.53
1B0h	D2F_2ND_EDG_MIN	NF2: Edge Detection Minimum Threshold	Section 6.3.54
1B4h	D2F_2ND_EDG_MAX	NF2: Edge Detection Maximum Threshold	Section 6.3.55
1B8h	GIC_EN	GIC (=Green Imbalance Correction): Enable	Section 6.3.56
1BCh	GIC_TYP	GIC: Configuration	Section 6.3.57
1C0h	GIC_GAN	GIC: Weight	Section 6.3.58
1C4h	GIC_NFGAN	GIC: NF2 Threshold Gain	Section 6.3.59
1C8h	GIC_THR	GIC: Threshold1	Section 6.3.60
1CCh	GIC_SLP	GIC: Slope (Threshold2 - Threshold1)	Section 6.3.61
1D0h	WB2_OFT_R	WB2: Offset	Section 6.3.62
1D4h	WB2_OFT_GR	WB2: Offset	Section 6.3.63
1D8h	WB2_OFT_GB	WB2: Offset	Section 6.3.64
1DCh	WB2_OFT_B	WB2: Offset	Section 6.3.65
1E0h	WB2_WGN_R	WB2: Gain	Section 6.3.66
1E4h	WB2_WGN_GR	WB2: Gain	Section 6.3.67
1E8h	WB2_WGN_GB	WB2: Gain	Section 6.3.68
1ECh	WB2_WGN_B	WB2: Gain	Section 6.3.69
1F0h-228h	Reserved	Reserved	
22Ch	RGB1_MUL_RR	RGB1 (=1st RGB2RGB conv): Matrix Coefficient	Section 6.3.70
230h	RGB1_MUL_GR	RGB1: Matrix Coefficient	Section 6.3.71
234h	RGB1_MUL_BR	RGB1: Matrix Coefficient	Section 6.3.72
238h	RGB1_MUL_RG	RGB1: Matrix Coefficient	Section 6.3.73
23Ch	RGB1_MUL_GG	RGB1: Matrix Coefficient	Section 6.3.74
240h	RGB1_MUL_BG	RGB1: Matrix Coefficient	Section 6.3.75
244h	RGB1_MUL_RB	RGB1: Matrix Coefficient	Section 6.3.76
248h	RGB1_MUL_GB	RGB1: Matrix Coefficient	Section 6.3.77
24Ch	RGB1_MUL_BB	RGB1: Matrix Coefficient	Section 6.3.78
250h	RGB1_OFT_OR	RGB1: Offset	Section 6.3.79
254h	RGB1_OFT_OG	RGB1: Offset	Section 6.3.80
258h	RGB1_OFT_OB	RGB1: Offset	Section 6.3.81
25Ch	GMM_CFG	Gamma Correction Configuration	Section 6.3.82
260h	RGB2_MUL_RR	RGB2 (=2nd RGB2RGB conv): Matrix Coefficient	Section 6.3.83
264h	RGB2_MUL_GR	RGB2: Matrix Coefficient	Section 6.3.84
268h	RGB2_MUL_BR	RGB2: Matrix Coefficient	Section 6.3.85
26Ch	RGB2_MUL_RG	RGB2: Matrix Coefficient	Section 6.3.86
270h	RGB2_MUL_GG	RGB2: Matrix Coefficient	Section 6.3.87

Table 207. IPIPE Registers (continued)

Offset	Acronym	Register Description	Section
274h	RGB2_MUL_BG	RGB2: Matrix Coefficient	Section 6.3.88
278h	RGB2_MUL_RB	RGB2: Matrix Coefficient	Section 6.3.89
27Ch	RGB2_MUL_GB	RGB2: Matrix Coefficient	Section 6.3.90
280h	RGB2_MUL_BB	RGB2: Matrix Coefficient	Section 6.3.91
284h	RGB2_OFT_OR	RGB2: Offset	Section 6.3.92
288h	RGB2_OFT_OG	RGB2: Offset	Section 6.3.93
28Ch	RGB2_OFT_OB	RGB2: Offset	Section 6.3.94
290h	D3LUT_EN	D3LUT (=3D LUT): 3D LUT Enable	Section 6.3.95
294h	YUV_ADJ	YUV (RGB2YCbCr conv): Luminance Adjustment (Contrast and Brightness)	Section 6.3.96
298h	YUV_MUL_RY	YUV: Matrix Coefficient	Section 6.3.97
29Ch	YUV_MUL_GY	YUV: Matrix Coefficient	Section 6.3.98
2A0h	YUV_MUL_BY	YUV: Matrix Coefficient	Section 6.3.99
2A4h	YUV_MUL_RCB	YUV: Matrix Coefficient	Section 6.3.100
2A8h	YUV_MUL_GCB	YUV: Matrix Coefficient	Section 6.3.101
2ACh	YUV_MUL_BCB	YUV: Matrix Coefficient	Section 6.3.102
2B0h	YUV_MUL_RCR	YUV: Matrix Coefficient	Section 6.3.103
2B4h	YUV_MUL_GCR	YUV: Matrix Coefficient	Section 6.3.104
2B8h	YUV_MUL_BCR	YUV: Matrix Coefficient	Section 6.3.105
2BCh	YUV_OFT_Y	YUV: Offset	Section 6.3.106
2C0h	YUV_OFT_CB	YUV: Offset	Section 6.3.107
2C4h	YUV_OFT_CR	YUV: Offset	Section 6.3.108
2C8h	YUV_PHS	Chrominance Position (for 422 Down Sampler)	Section 6.3.109
2CCh	GBCE_EN	GBCE (=Global Brightness and Contrast Enhancement): Enable	Section 6.3.110
2D0h	GBCE_TYP	GBCE: Method Selection	Section 6.3.111
2D4h	YEE_EN	YEE: Enable	Section 6.3.112
2D8h	YEE_TYP	YEE: Method Selection	Section 6.3.113
2DCh	YEE_SHF	YEE: HPF Shift Length	Section 6.3.114
2E0h	YEE_MUL_00	YEE: HPF Coefficient	Section 6.3.115
2E4h	YEE_MUL_01	YEE: HPF Coefficient	Section 6.3.116
2E8h	YEE_MUL_02	YEE: HPF Coefficient	Section 6.3.117
2ECh	YEE_MUL_10	YEE: HPF Coefficient	Section 6.3.118
2F0h	YEE_MUL_11	YEE: HPF Coefficient	Section 6.3.119
2F4h	YEE_MUL_12	YEE: HPF Coefficient	Section 6.3.120
2F8h	YEE_MUL_20	YEE: HPF Coefficient	Section 6.3.121
2FCh	YEE_MUL_21	YEE: HPF Coefficient	Section 6.3.122
300h	YEE_MUL_22	YEE: HPF Coefficient	Section 6.3.123
304h	YEE_THR	YEE: Lower Threshold before Referring to LUT	Section 6.3.124
308h	YEE_E_GAN	YEE: Edge Sharpener Gain	Section 6.3.125
30Ch	YEE_E_THR_1	YEE: Edge Sharpener HP Value Lower Threshold	Section 6.3.126
310h	YEE_E_THR_2	YEE: Edge Sharpener HP Value Upper Limit	Section 6.3.127
314h	YEE_G_GAN	YEE: Edge Sharpener Gain on Gradient	Section 6.3.128
318h	YEE_G_OFT	YEE: Edge Sharpener Offset on Gradient	Section 6.3.129
31Ch	CAR_EN	CAR (=Chroma Artifact Reduction): Enable	Section 6.3.130
320h	CAR_TYP	CAR: Method Selection	Section 6.3.131
324h	CAR_SW	CAR: Method Selection	Section 6.3.132
328h	CAR_HPF_TYP	CAR: Method Selection	Section 6.3.133
32Ch	CAR_HPF_SHF	CAR: Down Shift Size (HPF)	Section 6.3.134

Table 207. IPIPE Registers (continued)

Offset	Acronym	Register Description	Section
330h	CAR_HPF_THR	CAR: HPF Value Threshold	Section 6.3.135
334h	CAR_GN1_GAN	CAR: Gain1 Intensity	Section 6.3.136
338h	CAR_GN1_SHF	CAR: Gain1 Down Shift Size	Section 6.3.137
33Ch	CAR_GN1_MIN	CAR: Gain1 Minimum	Section 6.3.138
340h	CAR_GN2_GAN	CAR: Gain2 Intensity	Section 6.3.139
344h	CAR_GN2_SHF	CAR: Gain2 Down Shift Size	Section 6.3.140
348h	CAR_GN2_MIN	CAR: Gain2 Minimum	Section 6.3.141
34Ch	CGS_EN	CGS (=Chroma Gain Suppression): Enable	Section 6.3.142
350h	Reserved	Reserved	
354h	Reserved	Reserved	
358h	Reserved	Reserved	
35Ch	Reserved	Reserved	
360h	CGS_GN1_H_THR	CGS: Gain1-H Threshold	Section 6.3.143
364h	CGS_GN1_H_GAN	CGS: Gain1-H Slope	Section 6.3.144
368h	CGS_GN1_H_SHF	CGS: Gain1-H Down Shift Size	Section 6.3.145
36Ch	CGS_GN1_H_MIN	CGS: Gain1-H Minimum	Section 6.3.146
370h	Reserved	Reserved	
374h	Reserved	Reserved	
378h	Reserved	Reserved	
37Ch	Reserved	Reserved	
380h	BOX_EN	BOX: Enable	Section 6.3.147
384h	BOX_MODE	BOX: One Shot Mode	Section 6.3.148
388h	BOX_TYP	BOX: Block Size (16x16 or 8x8)	Section 6.3.149
38Ch	BOX_SHF	BOX: Down Shift Value of Input	Section 6.3.150
390h	BOX_SDR_SAD_H	BOX: SDRAM Address MSB	Section 6.3.151
394h	BOX_SDR_SAD_L	BOX: SDRAM Address LSB	Section 6.3.152
398h	Reserved	Reserved	
39Ch	HST_EN	HST: Enable	Section 6.3.153
3A0h	HST_MODE	HST: One Shot Mode	Section 6.3.154
3A4h	HST_SEL	HST: Source Select	Section 6.3.155
3A8h	HST_PARA	HST: Parameters Select	Section 6.3.156
3ACh	HST_0_VPS	HST: Vertical Start Position	Section 6.3.157
3B0h	HST_0_VSZ	HST: Vertical Size	Section 6.3.158
3B4h	HST_0_HPS	HST: Horizontal Start Position	Section 6.3.159
3B8h	HST_0_HSZ	HST: Horizontal Size	Section 6.3.160
3BCh	HST_1_VPS	HST: Vertical Start Position	Section 6.3.161
3C0h	HST_1_VSZ	HST: Vertical Size	Section 6.3.162
3C4h	HST_1_HPS	HST: Horizontal Start Position	Section 6.3.163
3C8h	HST_1_HSZ	HST: Horizontal Size	Section 6.3.164
3CCh	HST_2_VPS	HST: Vertical Start Position	Section 6.3.165
3D0h	HST_2_VSZ	HST: Vertical Size	Section 6.3.166
3D4h	HST_2_HPS	HST: Horizontal Start Position	Section 6.3.167
3D8h	HST_2_HSZ	HST: Horizontal Size	Section 6.3.168
3DCh	HST_3_VPS	HST: Vertical Start Position	Section 6.3.169
3E0h	HST_3_VSZ	HST: Vertical Size	Section 6.3.170
3E4h	HST_3_HPS	HST: Horizontal Start Position	Section 6.3.171
3E8h	HST_3_HSZ	HST: Horizontal Size	Section 6.3.172

Table 207. IPIPE Registers (continued)

Offset	Acronym	Register Description	Section
3ECh	HST_TBL	HST: Table Select	Section 6.3.173
3F0h	HST_MUL_R	HST: Matrix Coefficient	Section 6.3.174
3F4h	HST_MUL_GR	HST: Matrix Coefficient	Section 6.3.175
3F8h	HST_MUL_GB	HST: Matrix Coefficient	Section 6.3.176
3FCh	HST_MUL_B	HST: Matrix Coefficient	Section 6.3.177
400h	BSC_EN	BSC (=Boundary Signal Calculator): Enable	Section 6.3.178
404h	BSC_MODE	BSC: One Shot Mode	Section 6.3.179
408h	BSC_TYP	BSC: Y/Cb/Cr Select	Section 6.3.180
40Ch	BSC_ROW_VCT	BSC: Number of Row Vectors	Section 6.3.181
410h	BSC_ROW_SHF	BSC: Down Shift Value of Input for Row Sum	Section 6.3.182
414h	BSC_ROW_VPOS	BSC: Vertical Starting Position of Row Sum	Section 6.3.183
418h	BSC_ROW_VNUM	BSC: Vertical Number of Sampled Lines for Row Sum	Section 6.3.184
41Ch	BSC_ROW_VSKIP	BSC: Vertical Spacing between Adjacent Sampled Lines for Row Sum	Section 6.3.185
420h	BSC_ROW_HPOS	BSC: Horizontal Starting Position of Row Sum	Section 6.3.186
424h	BSC_ROW_HNUM	BSC: Horizontal Number of Sampled Lines for Row Sum	Section 6.3.187
428h	BSC_ROW_HSKIP	BSC: Horizontal Spacing between Adjacent Sampled Lines for Row Sum	Section 6.3.188
42Ch	BSC_COL_VCT	BSC: Number of Column Vectors	Section 6.3.189
430h	BSC_COL_SHF	BSC: Down Shift Value of Input for Column Sum	Section 6.3.190
434h	BSC_COL_VPOS	BSC: Vertical Starting Position of Column Sum	Section 6.3.191
438h	BSC_COL_VNUM	BSC: Vertical Number of Sampled Lines for Column Sum	Section 6.3.192
43Ch	BSC_COL_VSKIP	BSC: Vertical Spacing between Adjacent Sampled Lines for Column Sum	Section 6.3.193
440h	BSC_COL_HPOS	BSC: Horizontal Starting Position of Column Sum	Section 6.3.194
444h	BSC_COL_HNUM	BSC: Horizontal Number of Sampled Lines for Column Sum	Section 6.3.195
448h	BSC_COL_HSKIP	BSC: Horizontal Spacing between Adjacent Sampled Lines for Column Sum	Section 6.3.196

6.3.1 IPIPE Enable (SRC_EN)

The IPIPE Enable (SRC_EN) register is shown in Figure 273 and described in Table 208.

Figure 273. IPIPE Enable (SRC_EN) Register

31-16	
Reserved	
R-0	
15-1	**0**
Reserved	EN
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 208. IPIPE Enable (SRC_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		IPIPE Enable The start flag of the IPIPE module. When EN is 1, the IPIPE module starts a processing from the next rising edge of the VD. If the processing mode of the IPIPE module is "one shot", the EN is cleared to 0 after the end of the processing area.
		0	Disable
		1	Enable

6.3.2 One Shot Mode (SRC_MODE)

The One Shot Mode (SRC_MODE) register is shown in Figure 274 and described in Table 209.

Figure 274. One Shot Mode (SRC_MODE) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	WRT	OST
R-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 209. One Shot Mode (SRC_MODE) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	WRT		C_WE Mode Selection. The mode selection of the ipipeif_wrt which is an input port of the IPIPE module. If WRT is 0, the IPIPE module doesn't use the ipipeif_wrt. Else the IPIPE module uses it.
		0	Disable
		1	Enable
0	OST		One Shot Mode. The processing mode selection of the IPIPE module. Value 0 indicates the mode of "free run", value 1 indicates the mode of "one shot," which clears SRC_EN[EN] after each frame.
		0	Disable
		1	Enable

6.3.3 Input/Output Data Paths (SRC_FMT)

The Input/Output Data Paths (SRC_FMT) register is shown in Figure 275and described in Table 210.

Figure 275. Input/Output Data Paths (SRC_FMT) Register

31-16
Reserved
R-0

15-2	1-0
Reserved	FMT
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 210. Input/Output Data Paths (SRC_FMT) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1-0	FMT		Data path selection.
		0	Bayer input, YCbCr (or RGB) output
		1h	Bayer input, Bayer output (Bayer output is from white balance output)
		2h	Bayer input, Output disable (For histogram or Boxcar only mode)
		3h	YCbCr (16bit) input, YCbCr (or RGB) output

6.3.4 Color Pattern (SRC_COL)

The Color Pattern (SRC_COL) register is shown in Figure 276 and described in Table 211.

Figure 276. Color Pattern (SRC_COL) Register

31-16				
Reserved				
R-0				
15-8	7-6	5-4	3-2	1-0
Reserved	OO	OE	EO	EE
R-0	R/W-3h	R/W-2h	R/W-1h	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 211. Color Pattern (SRC_COL) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-6	OO		Color of the odd line and odd pixel This parameter is valid when SRC_FMT[FMT] is 0, 1 ,or 2.
		0	Red
		1h	Green (red line)
		2h	Green (blue line)
		3h	Blue
5-4	OE		Color of the odd line and even pixel This parameter is valid when SRC_FMT[FMT] is 0, 1, or 2.
		0	Red
		1h	Green (red line)
		2h	Green (blue line)
		3h	Blue
3-2	EO		Color of the even line and odd pixel This parameter is valid when SRC_FMT[FMT] is 0, 1, or 2.
		0	Red
		1h	Green (red line)
		2h	Green (blue line)
		3h	Blue
1-0	EE		Color of the even line and even pixel This parameter is valid when SRC_FMT[FMT] is 0, 1, or 2.
		0	Red
		1h	Green (red line)
		2h	Green (blue line)
		3h	Blue

6.3.5 Vertical Start Position (SRC_VPS)

The Vertical Start Position (SRC_VPS) register is shown in Figure 277 and described in Table 212.

Figure 277. Vertical Start Position (SRC_VPS) Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 212. Vertical Start Position (SRC_VPS) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	Vertical Start Position (0 - 65534) The vertical position of the global frame from the rising edge of the VD. The IPIPE module will start an image processing from VAL'th line.

6.3.6 Vertical Processing Size (SRC_VSZ)

The Vertical Processing Size (SRC_VSZ) register is shown in Figure 278 and described in Table 213.

Figure 278. Vertical Processing Size (SRC_VSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 213. Vertical Processing Size (SRC_VSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical Processing Size (0-8190) The vertical size of the processing area. The IPIPE module will process (VAL+1) lines.

6.3.7 Horizontal Start Position (SRC_HPS)

The Horizontal Start Position (SRC_HPS) register is shown in Figure 279 and described in Table 214.

Figure 279. Horizontal Start Position (SRC_HPS) Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 214. Horizontal Start Position (SRC_HPS) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	Horizontal Start Position (0-65534) The horizontal position of the global frame from the rising edge of the HD. The IPIPE module will start an image processing from VAL'th pixel.

6.3.8 Horizontal Processing Size (SRC_HSZ)

The Horizontal Processing Size (SRC_HSZ) register is shown in Figure 280 and described in Table 215.

Figure 280. Horizontal Processing Size (SRC_HSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 215. Horizontal Processing Size (SRC_HSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal Processing Size (0-8189) The horizontal size of the processing area. VAL[0] can not be written. The IPIPE module will process (VAL+1) pixels.

6.3.9 Status Flags (Reserved) (DMA_STA)

The Status Flags (Reserved) (DMA_STA) register is shown in Figure 281 and described in Table 216 .

Figure 281. Status Flags (Reserved) (DMA_STA) Register

31-8
Reserved
R-0

7-5	4	3	2	1	0
Reserved	HP_STATUS	HB_STATUS	BSC_STATUS	BP_STATUS	BE_STATUS
R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R = Read only; -*n* = value after reset

Table 216. Status Flags (Reserved) (DMA_STA) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4	HP_STATUS	0-1	Histogram Process Status When this bit is high, histogram module is busy
3	HB_STATUS	0-1	Histogram Bank Status This bit shows the memory bank which histogram is currently accessing
2	BSC_STATUS	0-1	Boundary Signal Calculator Process Status When this bit is high, BSC module is busy
1	BP_STATUS	0-1	Boxcar Process Status When this bit is high, Boxcar module is busy
0	BE_STATUS	0-1	Boxcar Error Status This bit shows the error status of Boxcar output

6.3.10 MMR Gated Clock Control (GCK_MMR)

The MMR Gated Clock Control (GCK_MMR) register is shown in Figure 282 and described in Table 217.

Figure 282. MMR Gated Clock Control (GCK_MMR) Register

31-16
Reserved
R-0

15-1	0
Reserved	REG
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 217. MMR Gated Clock Control (GCK_MMR) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	REG		IPIPE MMR Clock Enable The on/off selection of the MMR interface clock (clk_mmr_g0) which is used for MMR register accesses. When this bit is off, the registers except the following may not be written. Read access to all registers is allowed. SRC_EN GCK_MMR GCK_PIX BOX_EN HST_EN BSC_EN
		0	off
		1	on

6.3.11 PCLK Gated Clock Control (GCK_PIX)

The PCLK Gated Clock Control (GCK_PIX) register is shown in Figure 283 and described in Table 218.

Figure 283. PCLK Gated Clock Control (GCK_PIX) Register

31-16				
Reserved				
R-0				
15-4	**3**	**2**	**1**	**0**
Reserved	G3	G2	G1	G0
R-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 218. PCLK Gated Clock Control (GCK_PIX) Field Descriptions

Bit	Field	Value	Description
31-4	Reserved		Any writes to these bit(s) must always have a value of 0.
3	G3	0	IPIPE G3 Clock Enable The on/off selection of clk_pix_g3 which is used for the IPIPE processing of "Edge enhancer" and "Chroma artifact reduction". Data path need to be configured accordingly using SRC_FMT.
		0	off
		1	on
2	G2		IPIPE G2 Clock Enable The on/off selection of clk_pix_g2 which is used for the IPIPE processing of "CFA" to "422 conv", "Histogram (YCbCr input)", and "Boundary Signal Calculator". Data path need to be configured accordingly using SRC_FMT.
		0	off
		1	on
1	G1		IPIPE G1 Clock Enable The on/off selection of clk_pix_g1 which is used for the IPIPE processing of "Defect Pixel Correction" to "White Balance", and "Histogram (RAW input)". Data path need to be configured accordingly using SRC_FMT.
		0	off
		1	on
0	G0		IPIPE G0 Clock Enable The on/off selection of clk_pix_g0 which is used for the IPIPE processing of "Boxcar". Data path need to be configured accordingly using SRC_FMT.
		0	off
		1	on

6.3.12 LUTDPC Enable (DPC_LUT_EN)

The LUT Defect Pixel Correction Enable (DPC_LUT_EN) register is shown in Figure 284 and described in Table 219 .

Figure 284. LUTDPC Enable (DPC_LUT_EN) Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 219. LUTDPC Enable (DPC_LUT_EN) Field Descriptions

Bit	Field	Value0	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		LUT Defect Pixel Correction Enable
		0	disable
		1	enable

6.3.13 LUTDPC: Processing Mode Selection (DPC_LUT_SEL)

The LUT Defect Pixel Correction Processing Mode Selection (DPC_LUT_SEL) register is shown in Figure 285 and described in Table 220.

Figure 285. LUTDPC Processing Mode Selection (DPC_LUT_SEL) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	TBL	SEL
R-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 220. LUTDPC Processing Mode Selection (DPC_LUT_SEL) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	TBL		LUT type selection
		0	up to 1024 entries
		1	infinite number of entries
0	SEL		Replace dot selection on option #0 This bit indicates the correction method for option #0 in LUT entries
		0	replace with black dot
		1	replace with white dot

6.3.14 LUTDPC: Start Address in LUT (DPC_LUT_ADR)

The LUT Defect Pixel Correction Start Address in LUT (DPC_LUT_ADR) register is shown in Figure 286 and described in Table 221.

Figure 286. LUTDPC Start Address in LUT (DPC_LUT_ADR) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	ADR
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 221. LUTDPC Start Address in LUT (DPC_LUT_ADR) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	ADR	0-3FFh	Start Address in LUT

6.3.15 LUTDPC: Number of Available Entries in LUT (DPC_LUT_ADR)

The LUT Defect Pixel Correction Number of Available Entries in LUT (DPC_LUT_ADR) register is shown in Figure 287 and described in Table 222.

Figure 287. LUTDPC Number of Available Entries in LUT (DPC_LUT_ADR) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	SIZ
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 222. LUTDPC Number of Available Entries in LUT (DPC_LUT_ADR) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	SIZ	0-3FFh	Number of valid data in LUT (SIZ+1) of valid data in LUT. If DPC_LUT_SEL[TBL] is 1, the number is ignored.

6.3.16 OTFDPC (=On The Fly Defect Pixel Correction): Enable (DPC_OTF_EN)

The OTFDPC (=On The Fly Defect Pixel Correction): Enable (DPC_OTF_EN) register is shown in Section 6.3.16 and described in Table 223 .

Figure 288. OTFDPC (=On The Fly Defect Pixel Correction): Enable (DPC_OTF_EN) Register

31-16	
Reserved	
R-0	
15-1	**0**
Reserved	EN
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 223. OTFDPC (=On The Fly Defect Pixel Correction): Enable (DPC_OTF_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		OTF Defect Pixel Correction Enable
		0	disable
		1	enable

6.3.17 OTFDPC: Algorithm Selection (DPC_OTF_TYP)

The Algorithm Selection (DPC_OTF_TYP) register is shown in Figure 289 and described in Table 224.

Figure 289. Algorithm Selection (DPC_OTF_TYP)

31-16
Reserved
R-0

15-2	1	0
Reserved	TYP	ALG
R-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 224. Algorithm Selection (DPC_OTF_TYP) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	TYP		Defect Detection Method
		0	with Max1/Min1
		1	with Max2/Min2
0	ALG		Algorithm Selection. **Note:** To select MinMax Algorithm following values are set. ALG : 0 TYP : 0 DPC_OTF_2_D_THR_[x] : 0 DPC_OTF_2_C_THR_[x] : maximum value
		0	DPC2.0 algorithm
		1	DPC3.0 algorithm

6.3.18 OTFDPC: DPC2.0 Defect Detection Threshold (DPC_OTF_2_D_THR_R)

The DPC2.0 Defect Detection Threshold (DPC_OTF_2_D_THR_R) register is shown in Figure 290 and described in Table 225.

Figure 290. DPC2.0 Defect Detection Threshold (DPC_OTF_2_D_THR_R) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 225. DPC2.0 Defect Detection Threshold (DPC_OTF_2_D_THR_R) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	DPC2.0 Defect Detection Threshold for R

6.3.19 OTFDPC: DPC2.0 Defect Detection Threshold (DPC_OTF_2_D_THR_GR)

The DPC2.0 Defect Detection Threshold (DPC_OTF_2_D_THR_GR) register is shown in Figure 291 and described in Table 226.

Figure 291. DPC2.0 Defect Detection Threshold (DPC_OTF_2_D_THR_GR)

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 226. DPC2.0 Defect Detection Threshold (DPC_OTF_2_D_THR_GR) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	DPC2.0 Defect Detection Threshold for Gr

6.3.20 OTFDPC: DPC2.0 Defect Detection Threshold (DPC_OTF_2_D_THR_GB)

The DPC2.0 Defect Detection Threshold (DPC_OTF_2_D_THR_GB) register is shown in Figure 292 and described in Table 227.

Figure 292. DPC2.0 Defect Detection Threshold (DPC_OTF_2_D_THR_GB) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 227. DPC2.0 Defect Detection Threshold (DPC_OTF_2_D_THR_GB) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	DPC2.0 Defect Detection Threshold for Gb

6.3.21 OTFDPC: DPC2.0 Defect Detection Threshold (DPC_OTF_2_D_THR_B)

The DPC2.0 Defect Detection Threshold (DPC_OTF_2_D_THR_B) register is shown in Figure 293 and described in Table 228.

Figure 293. DPC2.0 Defect Detection Threshold (DPC_OTF_2_D_THR_B) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 228. DPC2.0 Defect Detection Threshold (DPC_OTF_2_D_THR_B) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	DPC2.0 Defect Detection Threshold for B

6.3.22 OTFDPC: DPC2.0 Defect Correction Threshold (DPC_OTF_2_C_THR_R)

The DPC2.0 Defect Correction Threshold (DPC_OTF_2_C_THR_R) register is shown in Figure 294 and described in Table 229.

Figure 294. DPC2.0 Defect Correction Threshold (DPC_OTF_2_C_THR_R) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 229. DPC2.0 Defect Correction Threshold (DPC_OTF_2_C_THR_R) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	DPC2.0 Defect Correction Threshold for R

6.3.23 OTFDPC: DPC2.0 Defect Correction Threshold (DPC_OTF_2_C_THR_GR)

The DPC2.0 Defect Correction Threshold (DPC_OTF_2_C_THR_GR) register is shown in Figure 295 and described in Table 230.

Figure 295. DPC2.0 Defect Correction Threshold (DPC_OTF_2_C_THR_GR) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 230. DPC2.0 Defect Correction Threshold (DPC_OTF_2_C_THR_GR) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	DPC2.0 Defect Correction Threshold for Gr

6.3.24 OTFDPC: DPC2.0 Defect Correction Threshold (DPC_OTF_2_C_THR_Gb)

The DPC2.0 Defect Correction Threshold (DPC_OTF_2_C_THR_Gb) register is shown in Figure 296 and described in Table 231.

Figure 296. DPC2.0 Defect Correction Threshold (DPC_OTF_2_C_THR_Gb) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 231. DPC2.0 Defect Correction Threshold (DPC_OTF_2_C_THR_Gb) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	DPC2.0 Defect Correction Threshold for Gb

6.3.25 OTFDPC: DPC2.0 Defect Correction Threshold (DPC_OTF_2_C_THR_B)

The DPC2.0 Defect Correction Threshold (DPC_OTF_2_C_THR_B) register is shown in Figure 297 and described in Table 232.

Figure 297. DPC2.0 Defect Correction Threshold (DPC_OTF_2_C_THR_B) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 232. DPC2.0 Defect Correction Threshold (DPC_OTF_2_C_THR_B) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	DPC2.0 Defect Correction Threshold for B

6.3.26 LSC (=Lens Shading Correction): Vertical Offset (LSC_VOFT)

The LSC (=Lens Shading Correction): Vertical Offset (LSC_VOFT) register is shown in Figure 298 and described in Table 233.

Figure 298. LSC (=Lens Shading Correction): Vertical Offset (LSC_VOFT) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 233. LSC (=Lens Shading Correction): Vertical Offset (LSC_VOFT) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	LSC_VOFT Vertical Offset

6.3.27 LSC: Vertical Quadratic Coefficient (LSC_VA2)

The Vertical Quadratic Coefficient (LSC_VA2) register is shown in Figure 299 and described in Table 234.

Figure 299. Vertical Quadratic Coefficient (LSC_VA2) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 234. Vertical Quadratic Coefficient (LSC_VA2) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	LSC_VA2 Vertical Quadratic Coefficient

6.3.28 LSC: Vertical Linear Coefficient (LSC_VA1)

The Vertical Linear Coefficient (LSC_VA1) register is shown in Figure 300 and described in Table 235.

Figure 300. Vertical Linear Coefficient (LSC_VA1) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 235. Vertical Linear Coefficient (LSC_VA1) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	LSC_VA1 Vertical Linear Coefficient

6.3.29 LSC: Vertical Quadratic/Linear Shift Length (LSC_VS)

The Vertical Quadratic/Linear Shift Length (LSC_VS) register is shown in Figure 301 and described in Table 236.

Figure 301. Vertical Quadratic/Linear Shift Length (LSC_VS) Register

31-16
Reserved
R-0

15-8	7-4	3-0
Reserved	VS2	VS1
R-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 236. Vertical Quadratic/Linear Shift Length (LSC_VS) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-4	VS2	0-Fh	LSC_VS2 Vertical Quadratic Shift Length
3-0	VS1	0-Fh	LSC_VS1 Vertical Linear Shift Length

6.3.30 LSC: Horizontal Offset (LSC_HOFT)

The Horizontal Offset (LSC_HOFT) register is shown in Figure 302 and described in Table 237.

Figure 302. Horizontal Offset (LSC_HOFT) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 237. Horizontal Offset (LSC_HOFT) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	LSC_HOFT Horizontal Offset

6.3.31 LSC: Horizontal Quadratic Coefficient (LSC_HA2)

The Horizontal Quadratic Coefficient (LSC_HA2) register is shown in Figure 303 and described in Table 238.

Figure 303. Horizontal Quadratic Coefficient (LSC_HA2) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 238. Horizontal Quadratic Coefficient (LSC_HA2) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	LSC_HA2 Horizontal Quadratic Coefficient

6.3.32 LSC: Horizontal Linear Coefficient (LSC_HA1)

The Horizontal Linear Coefficient (LSC_HA1) register is shown in Figure 304 and described in Table 239.

Figure 304. Horizontal Linear Coefficient (LSC_HA1) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 239. Horizontal Linear Coefficient (LSC_HA1) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	LSC_HA1 Horizontal Linear Coefficient

6.3.33 LSC: Horizontal Quadratic/Linear Shift Length (LSC_HS)

The Horizontal Quadratic/Linear Shift Length (LSC_HS) register is shown in Figure 305 and described in Table 240.

Figure 305. Horizontal Quadratic/Linear Shift Length (LSC_HS) Register

31-16
Reserved
R-0

15-8	7-4	3-0
Reserved	HS2	HS1
R-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 240. Horizontal Quadratic/Linear Shift Length (LSC_HS) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-4	HS2\	0-Fh	LSC_HS2 Horizontal Quadratic Shift Length
3-0	HS1	0-Fh	LSC_HS1 Horizontal Linear Shift Length

6.3.34 LSC: Total Gain (LSC_GAN_R)

The Total Gain (LSC_GAN_R) register is shown in Figure 306 and described in Table 241.

Figure 306. Total Gain (LSC_GAN_R) Register

31-16	
Reserved	
R-0	
15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 241. Total Gain (LSC_GAN_R) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	LSC_GAN_R Total Gain for R

6.3.35 LSC: Total Gain (LSC_GAN_GR)

The Total Gain (LSC_GAN_GR) register is shown in Figure 307 and described in Table 242.

Figure 307. Total Gain (LSC_GAN_GR) Register

31-16	
Reserved	
R-0	
15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 242. Total Gain (LSC_GAN_GR) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	LSC_GAN_Gr Total Gain for Gr

6.3.36 LSC: Total Gain (LSC_GAN_GB)

The Total Gain (LSC_GAN_GB) register is shown in Figure 308 and described in Table 243.

Figure 308. Total Gain (LSC_GAN_GB) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 243. Total Gain (LSC_GAN_GB) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	LSC_GAN_Gb Total Gain for Gb

6.3.37 LSC: Total Gain (LSC_GAN_B)

The Total Gain (LSC_GAN_B) register is shown in Figure 309 and described in Table 244.

Figure 309. Total Gain (LSC_GAN_B) Register

31-16	
Reserved	
R-0	
15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 244. Total Gain (LSC_GAN_B) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	LSC_GAN_B Total Gain for B

6.3.38 LSC: Total Offset (LSC_OFT_R)

The Total Offset (LSC_OFT_R) register is shown in Figure 310 and described in Table 245.

Figure 310. Total Offset (LSC_OFT_R) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 245. Total Offset (LSC_OFT_R) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	LSC_OFT_R Total Offset for R

6.3.39 LSC: Total Offset (LSC_OFT_GR)

The Total Offset (LSC_OFT_GR) register is shown in Figure 311 and described in Table 246.

Figure 311. Total Offset (LSC_OFT_GR) Register

31-16	
Reserved	
R-0	
15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 246. Total Offset (LSC_OFT_GR) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	LSC_OFT_Gr Total Offset for Gr

6.3.40 LSC: Total Offset (LSC_OFT_GB)

The Total Offset (LSC_OFT_GB) register is shown in Figure 312 and described in Table 247.

Figure 312. Total Offset (LSC_OFT_GB) Register

31-16	
Reserved	
R-0	
L	
15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 247. Total Offset (LSC_OFT_GB) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	LSC_OFT_Gb Total Offset for Gb

6.3.41 LSC: Total Offset (LSC_OFT_B)

The Total Offset (LSC_OFT_B) register is shown in Figure 313 and described in Table 248.

Figure 313. Total Offset (LSC_OFT_B) Register

31-16	
Reserved	
R-0	
15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 248. Total Offset (LSC_OFT_B) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	LSC_OFT_B Total Offset for B

6.3.42 LSC: Gain Shift Length (LSC_SHF)

The Gain Shift Length (LSC_SHF) register is shown in Figure 314 and described in Table 249.

Figure 314. Gain Shift Length (LSC_SHF) Register

31-16
Reserved
R-0

15-4	3-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 249. Gain Shift Length (LSC_SHF) Field Descriptions

Bit	Field	Value	Description
31-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.
3-0	VAL	0-Fh	LSC_SHF Gain Shift Length

6.3.43 LSC: Gain Maximum Value (LSC_MAX)

The Gain Maximum Value (LSC_MAX) register is shown in Figure 315 and described in Table 250.

Figure 315. Gain Maximum Value (LSC_MAX) Register

31-16
Reserved
R-0

15-9	8-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 250. Gain Maximum Value (LSC_MAX) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Any writes to these bit(s) must always have a value of 0.
8-0	VAL	0-1FFh	LSC_MAX Gain Maximum Value

6.3.44 NF1 (=1st 2D Noise Filter): Enable (D2F_1ST_EN)

The NF1 (=1st 2D Noise Filter): Enable (D2F_1ST_EN) register is shown in Figure 316 and described in Table 251.

Figure 316. NF1 (=1st 2D Noise Filter): Enable (D2F_1ST_EN) Register

31-16	
Reserved	
R-0	
15-1	**0**
Reserved	EN
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 251. NF1 (=1st 2D Noise Filter): Enable (D2F_1ST_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		1st Noise Filter Enable
		0	disable
		1	enable

6.3.45 NF1: Configuration (D2F_1ST_TYP)

The Configuration (D2F_1ST_TYP) register is shown in Figure 317 and described in Table 252.

Figure 317. Configuration (D2F_1ST_TYP) Register

31-16				
Reserved				
R-0				
15-9	8	7	6-5	4-0
Reserved	LSC	TYP	SHF	SPR
R-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 252. Configuration (D2F_1ST_TYP) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Any writes to these bit(s) must always have a value of 0.
8	LSC		Applies LSC Gain to Threshold Value
		0	disable
		1	enable
7	TYP		Sampling Method of Green Pixels
		0	Box (same as R or B)
		1	Diamond
6-5	SHF	0-3h	Down Shift Value in LUT Reference Address
4-0	SPR	0-1Fh	Spread Value

6.3.46 NF1: LUT Values (Threshold) (D2F_1ST_THR[8])

The LUT Values (Threshold) (D2F_1ST_THR[8]) register is shown in Figure 318 and described in Table 253.

Figure 318. LUT Values (Threshold) (D2F_1ST_THR[8]) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 253. LUT Values (Threshold) (D2F_1ST_THR[8]) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	LUT Values (threshold) Threshold values in noise filter - 1 algorithm

6.3.47 NF1: LUT Values (Intensity) (D2F_1ST_STR[8])

The LUT Values (Intensity) (D2F_1ST_STR[8]) register is shown in Figure 319 and described in Table 254.

Figure 319. LUT Values (Intensity) (D2F_1ST_STR[8]) Register

31-16
Reserved
R-0

15-5	4-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 254. LUT Values (Intensity) (D2F_1ST_STR[8]) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4-0	VAL	0-1Fh	LUT Values (intensity) Intensity values in noise filter - 1algorithm

6.3.48 NF1: Edge Detection Minimum Threshold (D2F_1ST_EDG_MIN)

The Edge Detection Minimum Threshold (D2F_1ST_EDG_MIN) register is shown in Figure 320 and described in Table 255.

Figure 320. Edge Detection Minimum Threshold (D2F_1ST_EDG_MIN) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 255. Edge Detection Minimum Threshold (D2F_1ST_EDG_MIN) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Edge Detection Minimum Threshold for NF-1

6.3.49 NF1: Edge Detection Maximum Threshold (D2F_1ST_EDG_MAX)

The Edge Detection Maximum Threshold (D2F_1ST_EDG_MAX) register is shown in Figure 321 and described in Table 256

Figure 321. Edge Detection Maximum Threshold (D2F_1ST_EDG_MAX) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 256. Edge Detection Maximum Threshold (D2F_1ST_EDG_MAX) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Edge Detection Maximum Threshold for NF-1

6.3.50 NF2: NF2 (=2nd 2D Noise Filter): Enable (D2F_2ND_EN)

The NF2 (=2nd 2D Noise Filter): Enable (D2F_2ND_EN) register is shown in Figure 322 and described in Table 257.

Figure 322. NF2 (=2nd 2D Noise Filter): Enable (D2F_2ND_EN) Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 257. NF2 (=2nd 2D Noise Filter): Enable (D2F_2ND_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		2nd Noise Filter Enable
		0	disable
		1	enable

6.3.51 NF2: Configuration (D2F_2ND_TYP)

The Configuration (D2F_2ND_TYP) register is shown in Figure 323 and described in Table 258.

Figure 323. Configuration (D2F_2ND_TYP) Register

31-16				
Reserved				
R-0				
15-9	8	7	6-5	4-0
Reserved SEL	LSC	TYP	SHF	SPR
R-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 258. Configuration (D2F_2ND_TYP) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Any writes to these bit(s) must always have a value of 0.
8	LSC		Applies LSC Gain to Threshold Value
		0	disable
		1	enable
7	TYP		Sampling Method of Green Pixels
		0	Box (same as R or B)
		1	Diamond
6-5	SHF	0-3h	Down Shift Value in LUT Reference Address
4-0	SPR	0-1Fh	Spread Value

6.3.52 NF2: LUT Values (Threshold) (D2F_2ND_THR[8])

The LUT Values (Threshold) (D2F_2ND_THR[8]) register is shown in Figure 324 and described in Table 259.

Figure 324. LUT Values (Threshold) (D2F_2ND_THR[8]) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 259. LUT Values (Threshold) (D2F_2ND_THR[8]) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	LUT Values (threshold) Threshold values in noise filter - 2 algorithm

6.3.53 NF2: LUT Values (Intensity) (D2F_2ND_STR[8])

The LUT Values (Intensity) (D2F_2ND_STR[8]) register is shown in Figure 325 and described in Table 260.

Figure 325. LUT Values (Intensity) (D2F_2ND_STR[8]) Register

31-16
Reserved
R-0

15-5	4-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after rese

Table 260. LUT Values (Intensity) (D2F_2ND_STR[8]) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4-0	VAL	0-1Fh	LUT Values (intensity) Intensity values in noise filter - 2 algorithm

6.3.54 NF2: Edge Detection Minimum Threshold (D2F_2ND_EDG_MIN)

The Edge Detection Minimum Threshold (D2F_2ND_EDG_MIN) register is shown in Figure 326 and described in Table 261.

Figure 326. Edge Detection Minimum Threshold (D2F_2ND_EDG_MIN) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 261. Edge Detection Minimum Threshold (D2F_2ND_EDG_MIN) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Edge Detection Minimum Threshold for NF-2

6.3.55 NF2: Edge Detection Maximum Threshold (D2F_2ND_EDG_MAX)

The Edge Detection Maximum Threshold (D2F_2ND_EDG_MAX) register is shown in Figure 327 and described in Table 262.

Figure 327. Edge Detection Maximum Threshold (D2F_2ND_EDG_MAX) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 262. Edge Detection Maximum Threshold (D2F_2ND_EDG_MAX) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Edge Detection Maximum Threshold for NF-2

6.3.56 GIC (=Green Imbalance Correction): Enable (GIC_EN)

The GIC (=Green Imbalance Correction): Enable (GIC_EN) register is shown in Figure 328 and described in Table 263.

Figure 328. GIC (=Green Imbalance Correction): Enable (GIC_EN) Register

31-16	
Reserved	
R-0	
15-1	**0**
Reserved	EN
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 263. GIC (=Green Imbalance Correction): Enable (GIC_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		Green Imbalance Correction Enable
		0	disable
		1	enable

6.3.57 GIC: Configuration (GIC_TYP)

The Configuration (GIC_TYP) register is shown in Figure 329 and described in Figure 329.

Figure 329. Configuration (GIC_TYP) Register

31-16
Reserved
R-0

15-3	2	1	0
Reserved	LSC	SEL	TYP
R-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 264. Configuration (GIC_TYP) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2	LSC		Applies LSC Gain to Threshold Value
		0	disable
		1	enable
1	SEL		Threshold Selection This bit selects the threshold either from the register value (GIC_THR) or threshold table of NF-2
		0	use GIC register value
		1	use NF2 threshold
0	TYP		Algorithm Selection
		0	use difference as index
		1	use 1D high pass value as index

6.3.58 GIC: Weight (GIC_GAN)

The Weight (GIC_GAN) register is shown in Figure 330 and described in Table 265.

Figure 330. Weight (GIC_GAN) Register

31-16	
Reserved	
R-0	
15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 265. Weight (GIC_GAN) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	GAIN or weight value for mixing of GICed data and the original data

6.3.59 GIC: NF2 Threshold Gain (GIC_NFGAN)

The NF2 Threshold Gain (GIC_NFGAN) register is shown in Figure 331 and described in Table 266.

Figure 331. NF2 Threshold Gain (GIC_NFGAN) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 266. NF2 Threshold Gain (GIC_NFGAN) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	NF2 Threshold Gain When NF-2 threshold values are used, this gain value is multiplied to those values. The gains are in U3.5 format.

6.3.60 GIC: Threshold1 (GIC_THR)

The Threshold1 (GIC_THR) register is shown in Figure 332 and described in Table 267.

Figure 332. Threshold1 (GIC_THR) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 267. Threshold1 (GIC_THR) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Threshold1. This value is used as the first threshold when GIC_TYP[SEL]=0. When using simple averaging algorithm (constant gain mode), set this value to maximum.

6.3.61 GIC: Slope (Threshold2 - Threshold1) (GIC_SLP)

The Slope (Threshold2 - Threshold1) (GIC_SLP) register is shown in Figure 333 and described in Table 268.

Figure 333. Slope (Threshold2 - Threshold1) (GIC_SLP) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 268. Slope (Threshold2 - Threshold1) (GIC_SLP) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Slope This value is used to determine Threshold2, Threshold3, and Threshold4 when GIC_TYP[SEL]=0 This value equals to (Threshold2 - Threshold1), (Threshold3 - Threshold2), (Threshold4 - Threshold3)

6.3.62 WB2: Offset (WB2_OFT_R)

The White Balance: Offset (WB2_OFT_R) register is shown in Figure 334 and described in Table 269.

Figure 334. WB2: Offset (WB2_OFT_R) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 269. WB2: Offset (WB2_OFT_R) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	White balance Offset for R (S12)

6.3.63 WB2: Offset (WB2_OFT_GR)

The White Balance: Offset (WB2_OFT_GR) register is shown in Figure 335 and described in Table 270.

Figure 335. WB2: Offset (WB2_OFT_GR) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 270. WB2: Offset (WB2_OFT_GR) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	White balance Offset for Gr (S12)

6.3.64 WB2: Offset (WB2_OFT_GB)

The White Balance: Offset (WB2_OFT_GB) register is shown in Figure 336 and described in Table 271.

Figure 336. WB2: Offset (WB2_OFT_GB) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 271. WB2: Offset (WB2_OFT_GB) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	White balance Offset for Gb (S12).

6.3.65 WB2: Offset (WB2_OFT_B)

The White Balance: Offset (WB2_OFT_B) register is shown in Figure 337 and described in Table 272 .

Figure 337. WB2: Offset (WB2_OFT_B) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 272. WB2: Offset (WB2_OFT_B) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	White balance Offset for B (S12).

6.3.66 WB2: Gain (WB2_WGN_R)

The White Balance: Gain (WB2_WGN_R) register is shown in Figure 338 and described in Table 273.

Figure 338. WB2: Gain (WB2_WGN_R) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-512

LEGEND: R = Read only; -*n* = value after reset

Table 273. WB2: Gain (WB2_WGN_R) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	White balance Gain for R (U4.9 = 0 - 15.998).

6.3.67 WB2: Gain (WB2_WGN_GR)

The White Balance: Gain (WB2_WGN_GR) register is shown in Figure 339 and described in Table 274.

Figure 339. WB2: Gain (WB2_WGN_GR) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-512

LEGEND: R = Read only; -*n* = value after reset

Table 274. WB2: Gain (WB2_WGN_GR) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	White balance Gain for Gr (U4.9 = 0 - 15.998).

6.3.68 WB2: Gain (WB2_WGN_GB)

The White Balance: Gain (WB2_WGN_GB) register is shown in Section 6.3.68 and described in Table 275.

Figure 340. WB2: Gain (WB2_WGN_GB) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-512

LEGEND: R = Read only; -*n* = value after reset

Table 275. WB2: Gain (WB2_WGN_GB) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	White balance Gain for Gb (U4.9 = 0 - 15.998).

6.3.69 WB2: Gain (WB2_WGN_B)

The White Balance: Gain (WB2_WGN_B) register is shown in Figure 341 and described in Table 276.

Figure 341. WB2: Gain (WB2_WGN_B) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-512

LEGEND: R = Read only; -*n* = value after reset

Table 276. WB2: Gain (WB2_WGN_B) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	White balance Gain for B (U4.9 = 0 - 15.998).

6.3.70 RGB1: Matrix Coefficient (RGB1_MUL_RR)

The RGB1 (=1st RGB2RGB conv): Matrix Coefficient (RGB1_MUL_RR) register is shown in Figure 342 and described in Table 277.

Figure 342. RGB1: Matrix Coefficient (RGB1_MUL_RR) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-256

LEGEND: R = Read only; -*n* = value after reset

Table 277. RGB1: Matrix Coefficient (RGB1_MUL_RR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for RR (S4.8 = -8 - +7.996)

6.3.71 RGB1: Matrix Coefficient (RGB1_MUL_GR)

The RGB1: Matrix Coefficient (RGB1_MUL_GR) register is shown in Figure 343 and described in Table 278.

Figure 343. RGB1: Matrix Coefficient (RGB1_MUL_GR) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 278. RGB1: Matrix Coefficient (RGB1_MUL_GR) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for GR (S4.8 = -8 - +7.996)

6.3.72 RGB1: Matrix Coefficient (RGB1_MUL_BR)

The RGB1: Matrix Coefficient (RGB1_MUL_BR) register is shown in Figure 344 and described in Table 279.

Figure 344. RGB1: Matrix Coefficient (RGB1_MUL_BR) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 279. RGB1: Matrix Coefficient (RGB1_MUL_BR) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for BR (S4.8 = -8 - +7.996)

6.3.73 RGB1: Matrix Coefficient (RGB1_MUL_RG)

The RGB1: Matrix Coefficient (RGB1_MUL_RG) register is shown in Figure 345 and described in Table 280.

Figure 345. RGB1: Matrix Coefficient (RGB1_MUL_RG) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 280. RGB1: Matrix Coefficient (RGB1_MUL_RG) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for RG (S4.8 = -8 - +7.996)

6.3.74 RGB1: Matrix Coefficient (RGB1_MUL_GG)

The RGB1: Matrix Coefficient (RGB1_MUL_GG) register is shown in Figure 346 and described in Table 281.

Figure 346. RGB1: Matrix Coefficient (RGB1_MUL_GG) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-256

LEGEND: R = Read only; -*n* = value after reset

Table 281. RGB1: Matrix Coefficient (RGB1_MUL_GG) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for GG (S4.8 = -8 - +7.996).

6.3.75 RGB1: Matrix Coefficient (RGB1_MUL_BG)

The RGB1: Matrix Coefficient (RGB1_MUL_BG) register is shown in Figure 347 and described in Table 282.

Figure 347. RGB1: Matrix Coefficient (RGB1_MUL_BG) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 282. RGB1: Matrix Coefficient (RGB1_MUL_BG) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for BG (S4.8 = -8 - +7.996)

6.3.76 RGB1: Matrix Coefficient (RGB1_MUL_RB)

The RGB1: Matrix Coefficient (RGB1_MUL_RB) register is shown in Figure 348 and described in Table 283.

Figure 348. RGB1: Matrix Coefficient (RGB1_MUL_RB) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 283. RGB1: Matrix Coefficient (RGB1_MUL_RB) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for RB (S4.8 = -8 - +7.996)

6.3.77 RGB1: Matrix Coefficient (RGB1_MUL_GB)

The RGB1: Matrix Coefficient (RGB1_MUL_GB) register is shown in Figure 349 and described in Table 284.

Figure 349. RGB1: Matrix Coefficient (RGB1_MUL_GB) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 284. RGB1: Matrix Coefficient (RGB1_MUL_GB) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for GB (S4.8 = -8 - +7.996)

6.3.78 RGB1: Matrix Coefficient (RGB1_MUL_BB)

The RGB1: Matrix Coefficient (RGB1_MUL_BB) register is shown in Figure 350 and described in Table 285.

Figure 350. RGB1: Matrix Coefficient (RGB1_MUL_BB) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-256

LEGEND: R = Read only; -*n* = value after reset

Table 285. RGB1: Matrix Coefficient (RGB1_MUL_BB) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for BB (S4.8 = -8 - +7.996)

6.3.79 RGB1: Offset (RGB1_OFT_OR)

The RGB1: Offset (RGB1_OFT_OR) register is shown in Figure 351 and described in Table 286.

Figure 351. RGB1: Offset (RGB1_OFT_OR) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 286. RGB1: Offset (RGB1_OFT_OR) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Offset for R (S13)

6.3.80 RGB1: Offset (RGB1_OFT_OG)

The RGB1: Offset (RGB1_OFT_OG) register is shown in Figure 352 and described in Table 287.

Figure 352. RGB1: Offset (RGB1_OFT_OG) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 287. RGB1: Offset (RGB1_OFT_OG) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Offset for G (S13)

6.3.81 RGB1: Offset (RGB1_OFT_OB)

The RGB1: Offset (RGB1_OFT_OB) register is shown in Figure 353 and described in Table 288.

Figure 353. RGB1: Offset (RGB1_OFT_OB) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 288. RGB1: Offset (RGB1_OFT_OB) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Offset for B (S13)

6.3.82 Gamma Correction Configuration (GMM_CFG)

The gamma correction configuration (GMM_CFG) register is shown in Figure 354 and described in Table 289.

Figure 354. Gamma Correction Configuration (GMM_CFG) Register

31-16
Reserved
R-0

15-7	6-5	4	3	2	1	0
Reserved	SIZ	TBL	Rsvd	BYPB	BYPG	BYPR
R-0	R/W-3h	R/W-0	R-0	R/W-1	R/W-1	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 289. Gamma Correction Configuration (GMM_CFG) Field Descriptions

Bit	Field	Value	Description
31-7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6-5	SIZ		Size of Gamma Table
		0	64 words
		1h	128 words
		2h	256 words
		3h	512 words
4	TBL		Selection of Gamma Table .
		0	RAM
		1	ROM
3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2	BYPB		Gamma Correction Mode for B
		0	No bypass
		1	Bypass
1	BYPG		Gamma Correction Mode for G
		0	No bypass
		1	Bypass
0	BYPR		Gamma Correction Mode for R
		0	No bypass
		1	Bypass

6.3.83 RGB2 (=2nd RGB2RGB conv): Matrix Coefficient (RGB2_MUL_RR)

The RGB2 (=2nd RGB2RGB conv): Matrix Coefficient (RGB2_MUL_RR) register is shown in Figure 355 and described in Table 290.

Figure 355. RGB2 (=2nd RGB2RGB conv): Matrix Coefficient (RGB2_MUL_RR) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-256

LEGEND: R = Read only; -*n* = value after reset

Table 290. RGB2 (=2nd RGB2RGB conv): Matrix Coefficient (RGB2_MUL_RR) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Matrix Coefficient for RR (S3.8 = -4 - +3.996)

6.3.84 RGB2: Matrix Coefficient (RGB2_MUL_GR)

The Matrix Coefficient (RGB2_MUL_GR) register is shown in Figure 356 and described in Table 291.

Figure 356. Matrix Coefficient (RGB2_MUL_GR) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 291. Matrix Coefficient (RGB2_MUL_GR) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Matrix Coefficient for GR (S3.8 = -4 - +3.996)

6.3.85 RGB2: Matrix Coefficient (RGB2_MUL_BR)

The Matrix Coefficient (RGB2_MUL_BR) register is shown in Figure 357 and described in Table 292.

Figure 357. Matrix Coefficient (RGB2_MUL_BR) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 292. Matrix Coefficient (RGB2_MUL_BR) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Matrix Coefficient for BR (S3.8 = -4 - +3.996)

6.3.86 RGB2: Matrix Coefficient (RGB2_MUL_RG)

The Matrix Coefficient (RGB2_MUL_RG) register is shown in Figure 358 and described in Table 293.

Figure 358. Matrix Coefficient (RGB2_MUL_RG) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 293. Matrix Coefficient (RGB2_MUL_RG) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Matrix Coefficient for RG (S3.8 = -4 - +3.996)

6.3.87 RGB2: Matrix Coefficient (RGB2_MUL_GG)

The Matrix Coefficient (RGB2_MUL_GG) register is shown in Figure 359 and described in Table 294.

Figure 359. Matrix Coefficient (RGB2_MUL_GG) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-256

LEGEND: R = Read only; -*n* = value after reset

Table 294. Matrix Coefficient (RGB2_MUL_GG) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Matrix Coefficient for GG (S3.8 = -4 - +3.996)

6.3.88 RGB2: Matrix Coefficient (RGB2_MUL_BG)

The Matrix Coefficient (RGB2_MUL_BG) register is shown in Figure 360 and described in Table 295.

Figure 360. Matrix Coefficient (RGB2_MUL_BG) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 295. Matrix Coefficient (RGB2_MUL_BG) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Matrix Coefficient for BG (S3.8 = -4 - +3.996)

6.3.89 RGB2: Matrix Coefficient (RGB2_MUL_RB)

The Matrix Coefficient (RGB2_MUL_RB) register is shown in Figure 361 and described in Table 296.

Figure 361. Matrix Coefficient (RGB2_MUL_RB) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 296. Matrix Coefficient (RGB2_MUL_RB) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Matrix Coefficient for RB (S3.8 = -4 - +3.996)

6.3.90 RGB2: Matrix Coefficient (RGB2_MUL_GB)

The Matrix Coefficient (RGB2_MUL_GB) register is shown in Figure 362 and described in Table 297.

Figure 362. Matrix Coefficient (RGB2_MUL_GB) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 297. Matrix Coefficient (RGB2_MUL_GB) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Matrix Coefficient for GB (S3.8 = -4 - +3.996)

6.3.91 RGB2: Matrix Coefficient (RGB2_MUL_BB)

The Matrix Coefficient (RGB2_MUL_BB) register is shown in Figure 363 and described in Table 298.

Figure 363. Matrix Coefficient (RGB2_MUL_BB) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-256

LEGEND: R = Read only; -*n* = value after reset

Table 298. Matrix Coefficient (RGB2_MUL_BB) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Matrix Coefficient for BB (S3.8 = -4 - +3.996)

6.3.92 RGB2: Offset (RGB2_OFT_OR)

The Offset (RGB2_OFT_OR) register is shown in Figure 364 and described in Table 299.

Figure 364. Offset (RGB2_OFT_OR) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 299. Offset (RGB2_OFT_OR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Offset for R (S11)

6.3.93 RGB2: Offset (RGB2_OFT_OG)

The Offset (RGB2_OFT_OG) register is shown in Figure 365 and described in Table 300.

Figure 365. Offset (RGB2_OFT_OG) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 300. Offset (RGB2_OFT_OG) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Offset for G (S11)

6.3.94 RGB2: Offset (RGB2_OFT_OB)

The Offset (RGB2_OFT_OB) register is shown in Figure 366 and described in Table 301.

Figure 366. Offset (RGB2_OFT_OB) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 301. Offset (RGB2_OFT_OB) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Offset for B (S11)

6.3.95 D3LUT (=3D LUT): 3D LUT Enable (D3LUT_EN)

The D3LUT (=3D LUT): 3D LUT Enable (D3LUT_EN) register is shown in Figure 367 and described in Table 302.

Figure 367. D3LUT (=3D LUT): 3D LUT Enable (D3LUT_EN) Register

31-16	
Reserved	
R-0	
15-1	**0**
Reserved	EN
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 302. D3LUT (=3D LUT): 3D LUT Enable (D3LUT_EN) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		3D LUT Enable
		0	disable
		1	enable

6.3.96 YUV: Luminance Adjustment (Contrast and Brightness) (YUV_ADJ)

The YUV (RGB2YCbCr conv): Luminance Adjustment (Contrast and Brightness) (YUV_ADJ) register is shown in Figure 368 and described in Table 303.

Figure 368. YUV: Luminance Adjustment (Contrast and Brightness) (YUV_ADJ) Register

31-16
Reserved
R-0

15-8	7-0
BRT	CTR
R/W-0	R/W-16

LEGEND: R = Read only; -*n* = value after reset

Table 303. YUV (RGB2YCbCr conv): Luminance Adjustment (Contrast and Brightness) (YUV_ADJ) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	BRT	0-FFh	Brightness Offset value for brightness control.
7-0	CTR	0-FFh	Contrast Multiplier coefficient for contrast control (U4.4 = 0 - +15.94)

6.3.97 YUV: Matrix Coefficient (YUV_MUL_RY)

The YUV: Matrix Coefficient (YUV_MUL_RY) register is shown in Figure 369 and described in Table 304.

Figure 369. YUV: Matrix Coefficient (YUV_MUL_RY) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-77

LEGEND: R = Read only; -*n* = value after reset

Table 304. YUV: Matrix Coefficient (YUV_MUL_RY) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for RY (S4.8 = -8 - +7.996)

6.3.98 YUV: Matrix Coefficient (YUV_MUL_GY)

The YUV: Matrix Coefficient (YUV_MUL_GY) register is shown in Figure 370 and described in Table 305.

Figure 370. YUV: Matrix Coefficient (YUV_MUL_GY) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-150

LEGEND: R = Read only; -*n* = value after reset

Table 305. YUV: Matrix Coefficient (YUV_MUL_GY) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for GY (S4.8 = -8 - +7.996)

6.3.99 YUV: Matrix Coefficient (YUV_MUL_BY)

The YUV: Matrix Coefficient (YUV_MUL_BY) register is shown in Figure 371 and described in Table 306.

Figure 371. YUV: Matrix Coefficient (YUV_MUL_BY) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-29

LEGEND: R = Read only; -*n* = value after reset

Table 306. YUV: Matrix Coefficient (YUV_MUL_BY) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for BY (S4.8 = -8 - +7.996)

6.3.100 YUV: Matrix Coefficient (YUV_MUL_RCB)

The YUV: Matrix Coefficient (YUV_MUL_RCB) register is shown in Figure 372 and described in Table 307.

Figure 372. YUV: Matrix Coefficient (YUV_MUL_RCB) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W--43

LEGEND: R = Read only; -*n* = value after reset

Table 307. YUV: Matrix Coefficient (YUV_MUL_RCB) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for RCb (S4.8 = -8 - +7.996)

6.3.101 YUV: Matrix Coefficient (YUV_MUL_GCB)

The YUV: Matrix Coefficient (YUV_MUL_GCB) register is shown in Figure 373 and described in Table 308.

Figure 373. YUV: Matrix Coefficient (YUV_MUL_GCB) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W--85

LEGEND: R = Read only; -*n* = value after reset

Table 308. YUV: Matrix Coefficient (YUV_MUL_GCB) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for GCb (S4.8 = -8 - +7.996)

6.3.102 YUV: Matrix Coefficient (YUV_MUL_BCB)

The YUV: Matrix Coefficient (YUV_MUL_BCB) register is shown in Figure 374 and described in Table 309.

Figure 374. YUV: Matrix Coefficient (YUV_MUL_BCB) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-128

LEGEND: R = Read only; -*n* = value after reset

Table 309. YUV: Matrix Coefficient (YUV_MUL_BCB) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for BCb (S4.8 = -8 - +7.996)

6.3.103 YUV: Matrix Coefficient (YUV_MUL_RCR)

The YUV: Matrix Coefficient (YUV_MUL_RCR) register is shown in Figure 375 and described in Table 310 .

Figure 375. YUV: Matrix Coefficient (YUV_MUL_RCR) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-128

LEGEND: R = Read only; -*n* = value after reset

Table 310. YUV: Matrix Coefficient (YUV_MUL_RCR) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for RCr (S4.8 = -8 - +7.996)

6.3.104 YUV: Matrix Coefficient (YUV_MUL_GCR)

The YUV: Matrix Coefficient (YUV_MUL_GCR) register is shown in Figure 376 and described in Table 311.

Figure 376. YUV: Matrix Coefficient (YUV_MUL_GCR) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W--107

LEGEND: R = Read only; -*n* = value after reset

Table 311. YUV: Matrix Coefficient (YUV_MUL_GCR) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for GCr (S4.8 = -8 - +7.996)

6.3.105 YUV: Matrix Coefficient (YUV_MUL_BCR)

The YUV: Matrix Coefficient (YUV_MUL_BCR) register is shown in Figure 377 and described in Table 312.

Figure 377. YUV: Matrix Coefficient (YUV_MUL_BCR) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W--21

LEGEND: R = Read only; -*n* = value after reset

Table 312. YUV: Matrix Coefficient (YUV_MUL_BCR) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	Matrix Coefficient for BCr (S4.8 = -8 - +7.996)

6.3.106 YUV: Offset (YUV_OFT_Y)

The YUV: Offset (YUV_OFT_Y) register is shown in Figure 378 and described in Table 313.

Figure 378. YUV: Offset (YUV_OFT_Y) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 313. YUV: Offset (YUV_OFT_Y) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Y Output Offset (S11)

6.3.107 YUV: Offset (YUV_OFT_CB)

The YUV: Offset (YUV_OFT_CB) register is shown in Figure 379 and described in Table 314.

Figure 379. YUV: Offset (YUV_OFT_CB) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-128

LEGEND: R = Read only; -*n* = value after reset

Table 314. YUV: Offset (YUV_OFT_CB) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Cb Output Offset (S11)

6.3.108 YUV: Offset (YUV_OFT_CR)

The YUV: Offset (YUV_OFT_CR) register is shown in Figure 380and described in Table 315.

Figure 380. YUV: Offset (YUV_OFT_CR) Register

31-16
Reserved
R-0

15-11	10-0
Reserved	VAL
R-0	R/W-128

LEGEND: R = Read only; -*n* = value after reset

Table 315. YUV: Offset (YUV_OFT_CR) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Any writes to these bit(s) must always have a value of 0.
10-0	VAL	0-7FFh	Cr Output Offset (S11)

6.3.109 Chrominance Position (for 422 Down Sampler) (YUV_PHS)

The Chrominance Position (for 422 Down Sampler) (YUV_PHS) register is shown in Figure 381 and described in Table 316.

Figure 381. Chrominance Position (for 422 Down Sampler) (YUV_PHS) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	LPF	POS
R-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 316. Chrominance Position (for 422 Down Sampler) (YUV_PHS) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	LPF		121-LPF Enable for Chrominance
		0	off
		1	on
0	POS		Phase position of the output of the Chrominance If SRC_FMT = 3 (YCbCr input), then the phase position of the INPUT of the Chrominance is selected by this register.
		0	same position with Luminance
		1	the middle of the Luminance

6.3.110 Global Brightness and Contrast Enhancement (GBCE_EN)

The GBCE (Global Brightness and Contrast Enhancement): Enable (GBCE_EN) register is shown in Figure 382 and described in Table 317 .

Figure 382. GBCE (Global Brightness and Contrast Enhancement): Enable (GBCE_EN) Register

31-16	
Reserved	
R-0	
15-1	**0**
Reserved	EN
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 317. GBCE (Global Brightness and Contrast Enhancement): Enable (GBCE_EN) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		Global Brightness and Contrast Enhancement Enable
		0	disable
		1	enable

6.3.111 Method Selection (GBCE_TYP)

The Method Selection (GBCE_TYP) register is shown in Figure 383 and described in Table 318.

Figure 383. Method Selection (GBCE_TYP) Register

31-16	
Reserved	
R-0	
15-1	**0**
Reserved	TYP
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 318. Method Selection (GBCE_TYP) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	TYP		Method Selection Y: Y is read from LUT. Cb and Cr are unchanged. GAIN: Y, Cb, and Cr are multiplied by the value in LUT. Entry for LUT is Y input value.
		0	Y value table
		1	Gain table

6.3.112 YEE: Enable (YEE_EN)

The YEE (=Edge Enhancer): Enable (YEE_EN) register is shown in Figure 384 and described in Table 319.

Figure 384. YEE: Enable (YEE_EN) Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 319. YEE: Enable (YEE_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		Edge Enhancer Enable
		0	disable
		1	enable

6.3.113 YEE: Method Selection (YEE_TYP)

The YEE: Method Selection (YEE_TYP) register is shown in Figure 385 and described in Table 320.

Figure 385. YEE: Method Selection (YEE_TYP) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	HAL	SEL
R-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 320. YEE: Method Selection (YEE_TYP) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	HAL		Halo Reduction (in Edge Sharpener) Enable
		0	disable
		1	enable
0	SEL		Merging Method between Edge Enhancer and Edge Sharpener ABSMAX(x, y) = (|x|>|y|) ? x : y
		0	absmax(EE, ES)
		1	EE + ES

6.3.114 YEE: HPF Shift Length (YEE_SHF)

The YEE: HPF Shift Length (YEE_SHF) register is shown in Figure 386 and described in Table 321.

Figure 386. YEE: HPF Shift Length (YEE_SHF) Register

31-16
Reserved
R-0

15-4	3-0
Reserved	SHF
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 321. YEE: HPF Shift Length (YEE_SHF) Field Descriptions

Bit	Field	Value	Description
31-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.
3-0	SHF	0-Fh	YEE_SHF Down shift length of high pass filter (HPF) in edge enhancer

6.3.115 YEE: HPF Coefficient (YEE_MUL_00)

The YEE: HPF Coefficient (YEE_MUL_00) register is shown in Figure 387 and described in Table 322.

Figure 387. YEE: HPF Coefficient (YEE_MUL_00) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 322. YEE: HPF Coefficient (YEE_MUL_00) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 00 (S10)

6.3.116 YEE: HPF Coefficient (YEE_MUL_01)

The YEE: HPF Coefficient (YEE_MUL_01) register is shown in Figure 388 and described in Table 323.

Figure 388. YEE: HPF Coefficient (YEE_MUL_01) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 323. YEE: HPF Coefficient (YEE_MUL_01) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 01 (S10)

6.3.117 YEE: HPF Coefficient (YEE_MUL_02)

The YEE: HPF Coefficient (YEE_MUL_02) register is shown in Figure 389 and described in Table 324.

Figure 389. YEE: HPF Coefficient (YEE_MUL_02) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 324. YEE: HPF Coefficient (YEE_MUL_02) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 02 (S10)

6.3.118 YEE: HPF Coefficient (YEE_MUL_10)

The YEE: HPF Coefficient (YEE_MUL_10) register is shown in Figure 390 and described in Table 325.

Figure 390. YEE: HPF Coefficient (YEE_MUL_10) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 325. YEE: HPF Coefficient (YEE_MUL_10) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 10 (S10)

6.3.119 YEE: HPF Coefficient (YEE_MUL_11)

The YEE: HPF Coefficient (YEE_MUL_11) register is shown in Figure 391 and described in Table 326.

Figure 391. YEE: HPF Coefficient (YEE_MUL_11) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 326. YEE: HPF Coefficient (YEE_MUL_11) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 11 (S10)

6.3.120 YEE: HPF Coefficient (YEE_MUL_12)

The YEE: HPF Coefficient (YEE_MUL_12) register is shown in Figure 392 and described in Table 327.

Figure 392. YEE: HPF Coefficient (YEE_MUL_12) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 327. YEE: HPF Coefficient (YEE_MUL_12) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 12 (S10)

6.3.121 YEE: HPF Coefficient (YEE_MUL_20)

The YEE: HPF Coefficient (YEE_MUL_20) register is shown in Figure 393 and described in Table 328 .

Figure 393. YEE: HPF Coefficient (YEE_MUL_20) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 328. YEE: HPF Coefficient (YEE_MUL_20) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 20 (S10)

6.3.122 YEE: HPF Coefficient (YEE_MUL_21)

The YEE: HPF Coefficient (YEE_MUL_21) register is shown in Figure 394 and described in Table 329.

Figure 394. YEE: HPF Coefficient (YEE_MUL_21) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 329. YEE: HPF Coefficient (YEE_MUL_21) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 21 (S10)

6.3.123 YEE: HPF Coefficient (YEE_MUL_22)

The YEE: HPF Coefficient (YEE_MUL_22) register is shown in Figure 395 and described in Table 330.

Figure 395. YEE: HPF Coefficient (YEE_MUL_22) Register

31-16
Reserved
R-0

15-10	9-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 330. YEE: HPF Coefficient (YEE_MUL_22) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	VAL	0-3FFh	YEE_HPF Coefficient 22 (S10)

6.3.124 YEE: Lower Threshold before Referring to LUT (YEE_THR)

The YEE: Lower Threshold before Referring to LUT (YEE_THR) register is shown in Figure 396 and described in Table 331.

Figure 396. YEE: Lower Threshold before Referring to LUT (YEE_THR) Register

31-16
Reserved
R-0

15-6	5-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 331. YEE: Lower Threshold before Referring to LUT (YEE_THR) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved	0	Any writes to these bit(s) must always have a value of 0.
5-0	VAL	0-3Fh	YEE_THR Lower Threshold before referring to LUT if (HPF ≤ VAL), then output = HPF+VAL. if (HPF > VAL), then output = HPF-VAL. Otherwise, output = 0.

6.3.125 YEE: Edge Sharpener Gain (YEE_E_GAN)

The YEE: Edge Sharpener Gain (YEE_E_GAN) register is shown in Figure 397 and described in Table 332.

Figure 397. YEE: Edge Sharpener Gain (YEE_E_GAN) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 332. YEE: Edge Sharpener Gain (YEE_E_GAN) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	YEE_E_GAN Edge Sharpener Gain

6.3.126 YEE: Edge Sharpener HP Value Lower Threshold (YEE_E_THR_1)

The YEE: Edge Sharpener HP Value Lower Threshold (YEE_E_THR_1) register is shown in Figure 398 and described in Table 333.

Figure 398. YEE: Edge Sharpener HP Value Lower Threshold (YEE_E_THR_1) Register

31-16
Reserved
R-0

15-12	11-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 333. YEE: Edge Sharpener HP Value Lower Threshold (YEE_E_THR_1) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	VAL	0-FFFh	YEE_E_THR_1 Edge Sharpener Lower Threshold if (HPF ≤ VAL), then output = (HPF+VAL) >> 6. if (HPF > VAL), then output = (HPF-VAL) >> 6. Otherwise, output = 0.

6.3.127 YEE: Edge Sharpener HP Value Upper Limit (YEE_E_THR_2)

The YEE: Edge Sharpener HP Value Upper Limit (YEE_E_THR_2) register is shown in Figure 399 and described in Table 334.

Figure 399. YEE: Edge Sharpener HP Value Upper Limit (YEE_E_THR_2) Register

31-16
Reserved
R-0

15-6	5-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 334. YEE: Edge Sharpener HP Value Upper Limit (YEE_E_THR_2) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved	0	Any writes to these bit(s) must always have a value of 0.
5-0	VAL	0-3Fh	YEE_E_THR_2 Edge Sharpener HP Value Upper Limit.

6.3.128 YEE: Edge Sharpener Gain on Gradient (YEE_G_GAN)

The YEE: Edge Sharpener Gain on Gradient (YEE_G_GAN) register is shown in Figure 400 and described in Table 335.

Figure 400. YEE: Edge Sharpener Gain on Gradient (YEE_G_GAN) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 335. YEE: Edge Sharpener Gain on Gradient (YEE_G_GAN) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	YEE_E_G_GAN Edge Sharpener Gain on Gradient

6.3.129 YEE: Edge Sharpener Offset on Gradient (YEE_G_OFT)

The YEE: Edge Sharpener Offset on Gradient (YEE_G_OFT) register is shown in Figure 401 and described in Table 336.

Figure 401. YEE: Edge Sharpener Offset on Gradient (YEE_G_OFT) Register

31-16
Reserved
R-0

15-6	5-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 336. YEE: Edge Sharpener Offset on Gradient (YEE_G_OFT) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved	0	Any writes to these bit(s) must always have a value of 0.
5-0	VAL	0-3Fh	YEE_G_OFT Edge Sharpener Offset on Gradient

6.3.130 CAR (=Chroma Artifact Reduction): Enable (CAR_EN)

The CAR (=Chroma Artifact Reduction): Enable (CAR_EN) register is shown in Figure 402 and described in Table 337.

Figure 402. CAR (=Chroma Artifact Reduction): Enable (CAR_EN) Register

31-16	
Reserved	
R-0	
15-1	**0**
Reserved	EN
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 337. CAR (=Chroma Artifact Reduction): Enable (CAR_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		Chroma Artifact Reduction Enable
		0	disable
		1	enable

6.3.131 CAR: Method Selection (CAR_TYP)

The Method Selection (CAR_TYP) register is shown in Figure 403 and described in Table 338 .

Figure 403. Method Selection (CAR_TYP) Register

31-16
Reserved
R-0

15-1	0
Reserved	TYP
R-0	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 338. Method Selection (CAR_TYP) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	TYP		Method Selection of Chroma Artifact Reduction. **Note:** To select Median Filter following values are set. TYP : 1 CAR_SW[SW0] : maximum value
		0	Gain control
		1	Dynamic switching

6.3.132 CAR: Method Selection (CAR_SW)

The Method Selection (CAR_SW) register is shown in Figure 404 and described in Table 339.

Figure 404. Method Selection (CAR_SW) Register

31-16	
Reserved	
R-0	
L	
15-8	7-0
SW1	SW0
R/W-0	R/W-255

LEGEND: R = Read only; -*n* = value after reset

Table 339. Method Selection (CAR_SW) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-8	SW1	0-FFh	SW1 CAR Gain Control Threshold
7-0	SW0	0-FFh	SW0 CAR Median Filter Threshold

6.3.133 CAR: Method Selection (CAR_HPF_TYP)

The Method Selection (CAR_HPF_TYP) register is shown in Figure 405 and described in Table 340.

Figure 405. Method Selection (CAR_HPF_TYP) Register

31-16
Reserved
R-0

15-3	2-0
Reserved	TYP
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 340. Method Selection (CAR_HPF_TYP) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2-0	TYP		CAR Type of HPF
		0	Y
		1	horizontal HPF
		2	vertical HPF
		3	2D HPF
		4	2D HPF from edge enhancement

6.3.134 CAR: Down Shift Size (HPF) (CAR_HPF_SHF)

The Down Shift Size (HPF) (CAR_HPF_SHF) register is shown in Figure 406 and described in Table 341.

Figure 406. Down Shift Size (HPF) (CAR_HPF_SHF) Register

31-16
Reserved
R-0

15-2	1-0
Reserved	SHF
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 341. Down Shift Size (HPF) (CAR_HPF_SHF) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1-0	SHF	0-3h	HPF_SHF CAR Down shift value for HPF

6.3.135 CAR: HPF Value Threshold (CAR_HPF_THR)

The HPF Value Threshold (CAR_HPF_THR) register is shown in Figure 407 and described in Table 342.

Figure 407. HPF Value Threshold (CAR_HPF_THR) Register

31-16	
Reserved	
R-0	
15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 342. HPF Value Threshold (CAR_HPF_THR) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	HPF_THR CAR HPF Value Threshold

6.3.136 CAR: Gain1 Intensity (CAR_GN1_GAN)

The Gain1 Intensity (CAR_GN1_GAN) register is shown in Figure 408 and described in Table 343.

Figure 408. Gain1 Intensity (CAR_GN1_GAN) Register

31-16	
Reserved	
R-0	
15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 343. Gain1 Intensity (CAR_GN1_GAN) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	GN1_GAN CAR Gain1 Intensity.

6.3.137 CAR: Gain1 Down Shift Size (CAR_GN1_SHF)

The Gain1 Down Shift Size (CAR_GN1_SHF) register is shown in Figure 409 and described in Table 344.

Figure 409. Gain1 Down Shift Size (CAR_GN1_SHF) Register

31-16
Reserved
R-0

15-3	2-0
Reserved	SHF
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 344. Gain1 Down Shift Size (CAR_GN1_SHF) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2-0	SHF	0-7h	GN1_SHF CAR Gain1 Down shift size.

6.3.138 CAR: Gain1 Minimum (CAR_GN1_MIN)

The Gain1 Minimum (CAR_GN1_MIN) register is shown in Figure 410 and described in Table 345.

Figure 410. Gain1 Minimum (CAR_GN1_MIN) Register

31-16	
Reserved	
R-0	
15-9	8-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 345. Gain1 Minimum (CAR_GN1_MIN) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Any writes to these bit(s) must always have a value of 0.
8-0	VAL	0-1FFh	GN1_MIN (0-256) CAR Gain1 Minimum.

6.3.139 CAR: Gain2 Intensity (CAR_GN2_GAN)

The Gain2 Intensity (CAR_GN2_GAN) register is shown in Figure 411 and described in Table 346.

Figure 411. Gain2 Intensity (CAR_GN2_GAN) Register

31-16	
Reserved	
R-0	
15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 346. Gain2 Intensity (CAR_GN2_GAN) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	GN2_GAN CAR Gain2 Intensity.

6.3.140 CAR: Gain2 Down Shift Size (CAR_GN2_SHF)

The Gain2 Down Shift Size (CAR_GN2_SHF) register is shown in Figure 412 and described in Table 347.

Figure 412. Gain2 Down Shift Size (CAR_GN2_SHF) Register

31-16
Reserved
R-0

15-4	3-0
Reserved	SHF
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 347. Gain2 Down Shift Size (CAR_GN2_SHF) Field Descriptions

Bit	Field	Value	Description
31-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.
3-0	SHF	0-Fh	GN2_SHF CAR Gain2 Down shift size.

6.3.141 CAR: Gain2 Minimum (CAR_GN2_MIN)

The Gain2 Minimum (CAR_GN2_MIN) register is shown in Figure 413 and described in Table 348.

Figure 413. Gain2 Minimum (CAR_GN2_MIN) Register

31-16
Reserved
R-0

15-9	8-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 348. Gain2 Minimum (CAR_GN2_MIN) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Any writes to these bit(s) must always have a value of 0.
8-0	VAL	0-1FFh	GN2_MIN (0-256) CAR Gain2 Minimum.

6.3.142 Chroma Gain Suppression Enable (CGS_EN)

The chroma gain suppression: enable (CGS_EN) register is shown in Figure 414 and described in Table 349.

Figure 414. Chroma Gain Suppression Enable (CGS_EN) Register

31	31-1	0
Reserved		EN
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 349. Chroma Gain Suppression Enable (CGS_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		Chroma Gain Suppression Enable
		0	disable
		1	enable

6.3.143 CGS: Gain1-H Threshold (CGS_GN1_H_THR)

The CGS Gain1-H Threshold register is shown in Figure 415and described in Table 350.

Figure 415. Gain1-H Threshold (CGS_GN1_H_THR) Register

31-16	
Reserved	
R-0	
15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 350. Gain1-H Threshold (CGS_GN1_H_THR) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	CGS Gain1-H Threshold Y bright side threshold.

6.3.144 CGS: Gain1-H Slope (CGS_GN1_H_GAN)

The CGS Gain1-H Slope register is shown in Figure 416 and described in Table 351.

Figure 416. Gain1-H Slope (CGS_GN1_H_GAN) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 351. Gain1-H Slope (CGS_GN1_H_GAN) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	CGS Gain1-H Slope Y bright side slope

6.3.145 CGS: Gain1-H Down Shift Size (CGS_GN1_H_SHF)

The CGS Gain1-H Down shift size register is shown in Figure 417 and described in Table 352.

Figure 417. Gain1-H Down Shift Size (CGS_GN1_H_SHF) Register

31-16
Reserved
R-0

15-3	2-0
Reserved	SHF
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 352. Gain1-H Down Shift Size (CGS_GN1_H_SHF) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2-0	SHF	0-7h	CGS Gain1-H Down shift size Y bright side down R-0 shift value

6.3.146 CGS: Gain1-H Minimum (CGS_GN1_H_MIN)

The CGS Gain1-H Minimum register is shown in Figure 418 and described in Table 353.

Figure 418. Gain1-H Minimum (CGS_GN1_H_MIN) Register

31-16	
Reserved	
R-0	
15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 353. Gain1-H Minimum (CGS_GN1_H_MIN) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	CGS Gain1-H Minimum Y bright side minimum

6.3.147 BOX: Enable (BOX_EN)

The boxcar (BOX) enable (BOX_EN) register is shown in Figure 419and described in Table 354.

Figure 419. BOX: Enable (BOX_EN) Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 354. BOX: Enable (BOX_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		Boxcar Enable
		0	disable
		1	enable

6.3.148 BOX: One Shot Mode (BOX_MODE)

The BOX: One Shot Mode register is shown in Figure 420 and described in Table 355.

Figure 420. BOX: One Shot Mode (BOX_MODE) Register

31-16
Reserved
R-0

15-1	0
Reserved	OST
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 355. BOX: One Shot Mode (BOX_MODE) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	OST		Boxcar One Shot Mode Enable
		0	continuous mode
		1	one shot mode

6.3.149 BOX: Block Size (16x16 or 8x8) (BOX_TYP)

The BOX: Block Size (16x16 or 8x8) (BOX_TYP) register is shown in Figure 421 and described in Table 356.

Figure 421. BOX: Block Size (16x16 or 8x8) (BOX_TYP) Register

31-16
Reserved
R-0

15-1	0
Reserved	SEL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 356. BOX: Block Size (16x16 or 8x8) (BOX_TYP) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	SEL		Block Size in Boxcar Sampling
		0	8 × 8
		1	16 × 16

6.3.150 BOX: Down Shift Value of Input (BOX_SHF)

The BOX: Down shift value of input (BOX_SHF) register is shown in Figure 422 and described in Table 357.

Figure 422. BOX: Down Shift Value of Input (BOX_SHF) Register

31-16
Reserved
R-0

15-3	2-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 357. BOX: Down Shift Value of Input (BOX_SHF) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2-0	VAL	0-7h	Down shift value of output data of Boxcar (0-4)

6.3.151 BOX: SDRAM Address MSB (BOX_SDR_SAD_H)

The BOX: SDRAM Address MSB (BOX_SDR_SAD_H) register is shown in Figure 423 and described in Table 358.

Figure 423. BOX: SDRAM Address MSB (BOX_SDR_SAD_H) Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 358. BOX: SDRAM Address MSB (BOX_SDR_SAD_H) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	Boxcar SDRAM Address (H) The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.3.152 BOX: SDRAM Address LSB (BOX_SDR_SAD_L)

The BOX: SDRAM Address LSB (BOX_SDR_SAD_L) register is shown in Figure 424 and described in Table 359.

Figure 424. BOX: SDRAM Address LSB (BOX_SDR_SAD_L) Register

31-16
Reserved
R-0

15-5	4-0
VAL	Reserved
R/W-0	R-0

LEGEND: R = Read only; -*n* = value after reset

Table 359. BOX: SDRAM Address LSB (BOX_SDR_SAD_L) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-5	VAL	0-7FFh	Boxcar SDRAM Address (L) The lower 16 bits of the first address in the allowed memory space in SDRAM.
4-0	Reserved	0	Reserved

6.3.153 HST: Enable (HST_EN)

The histogram enable (HST_EN) register is shown in Figure 425 and described in Table 360.

Figure 425. HST: Enable (HST_EN) Register

31-16	
Reserved	
R-0	
15-1	**0**
Reserved	EN
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 360. HST: Enable (HST_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		Histogram Enable
		0	disable
		1	enable

6.3.154 HST: One Shot Mode (HST_MODE)

The HST: One Shot Mode (HST_MODE) register is shown in Figure 426 and described in Table 361.

Figure 426. HST: One Shot Mode (HST_MODE) Register

31-16	
Reserved	
R-0	
15-1	**0**
Reserved	OST
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 361. HST: One Shot Mode (HST_MODE) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	OST		Histogram One Shot Mode Enable
		0	continuous mode
		1	one shot mode

6.3.155 HST: Source Select (HST_SEL)

The HST: Source Select (HST_SEL) register is shown in Figure 427 and described in Table 362.

Figure 427. HST: Source Select (HST_SEL) Register

31-16			
Reserved			
R-0			
15-3		2	1-0
Reserved		SEL	TYP
R-0		R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 362. HST: Source Select (HST_SEL) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2	SEL		Histogram Input Selection
		0	from 1st Noise Filter (Bayer format)
		1	from RGB2YUV (YCbCr-444 format)
1-0	TYP		Histogram Green Sampling method Selection Only valid when SEL is 0.
		0	Gr is collected
		1h	Gb is collected
		2h	Gavg is collected
		3h	Reserved

6.3.156 HST: Parameters Select (HST_PARA)

The HST: Parameters Select (HST_PARA) register is shown in Figure 428 and described in Table 363.

Figure 428. HST: Parameters Select (HST_PARA) Register

31-16
Reserved
R-0

15-14	13-12	11-8	7	6	5	4	3	2	1	0
Reserved	BIN	SHF	COL3	COL2	COL1	COL0	RGN3	RGN2	RGN1	RGN0
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 363. HST: Parameters Select (HST_PARA) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-12	BIN		Number of bins
		0	32 bins
		1h	64 bins
		2h	128 bins
		3h	256 bins
11-8	SHF	0-Fh	Shift Length of input data
7	COL3		Color 3 Enable Y : HST_SEL[SEL]=0 Y2: HST_SEL[SEL]=1
		0	disable
		1	enable
6	COL2		Color 2 Enable B : HST_SEL[SEL]=0 Cb: HST_SEL[SEL]=1
		0	disable
		1	enable
5	COL1		Color 1 Enable G : HST_SEL[SEL]=0 Y1: HST_SEL[SEL]=1
		0	disable
		1	enable
4	COL0		Color 0 Enable R : HST_SEL[SEL]=0 Cr: HST_SEL[SEL]=1
		0	disable
		1	enable
3	RGN3		Region 3 Enable
		0	disable
		1	enable
2	RGN2		Region 2 Enable
		0	disable
		1	enable
1	RGN1		Region 1 Enable
		0	disable
		1	enable
0	RGN0		Region 0 Enable
		0	disable
		1	enable

6.3.157 HST: Vertical Start Position (HST_0_VPS)

The HST: Vertical Start Position (HST_0_VPS) register is shown in Figure 429 and described in Table 364.

Figure 429. HST: Vertical Start Position (HST_0_VPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 364. HST: Vertical Start Position (HST_0_VPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical start position of the region0 from the SRC_VPS The region will start the "Histogram" processing from VAL'th line. VAL[0] can not be written.

6.3.158 HST: Vertical Size (HST_0_VSZ)

The HST: Vertical Size (HST_0_VSZ) register is shown in Figure 430 and described in Table 365.

Figure 430. HST: Vertical Size (HST_0_VSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 365. HST: Vertical Size (HST_0_VSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical size of the region0. The "Histogram" processing of the region will process (VAL+1) lines. VAL[0] can not be written.

6.3.159 HST: Horizontal Start Position (HST_0_HPS)

The HST: Horizontal Start Position (HST_0_HPS) register is shown in Figure 431 and described in Table 366.

Figure 431. HST: Horizontal Start Position (HST_0_HPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 366. HST: Horizontal Start Position (HST_0_HPS) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal start position of the region0 from the SRC_VPS. The region will start the "Histogram" processing from VAL'th pixel. VAL[0] can not be written.

6.3.160 HST: Horizontal Size (HST_0_HSZ)

The HST: Horizontal Size (HST_0_HSZ) register is shown in Figure 432 and described in Table 367.

Figure 432. HST: Horizontal Size (HST_0_HSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 367. HST: Horizontal Size (HST_0_HSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal size of the region0. The "Histogram" processing of the region will process (VAL+1) pixels. VAL[0] can not be written.

6.3.161 HST: Vertical Start Position (HST_1_VPS)

The HST: Vertical Start Position (HST_1_VPS) register is shown in Figure 433 and described in Table 368.

Figure 433. HST: Vertical Start Position (HST_1_VPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 368. HST: Vertical Start Position (HST_1_VPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical start position of the region1 from the SRC_VPS The region will start the "Histogram" processing from VAL'th line. VAL[0] can not be written.

6.3.162 HST: Vertical Size (HST_1_VSZ)

The HST: Vertical Size (HST_1_VSZ) register is shown in Figure 434 and described in Table 369.

Figure 434. HST: Vertical Size (HST_1_VSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 369. HST: Vertical Size (HST_1_VSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical size of the region1. The "Histogram" processing of the region will process (VAL+1) lines. VAL[0] can not be written.

6.3.163 HST: Horizontal Start Position (HST_1_HPS)

The HST: Horizontal Start Position (HST_1_HPS) register is shown in Figure 435 and described in Table 370.

Figure 435. HST: Horizontal Start Position (HST_1_HPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 370. HST: Horizontal Start Position (HST_1_HPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal start position of the region1 from the SRC_VPS. The region will start the "Histogram" processing from VAL'th pixel. VAL[0] can not be written.

6.3.164 HST: Horizontal Size (HST_1_HSZ)

The HST: Horizontal Size (HST_1_HSZ) register is shown in Figure 436 and described in Table 371.

Figure 436. HST: Horizontal Size (HST_1_HSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 371. HST: Horizontal Size (HST_1_HSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal size of the region1. The "Histogram" processing of the region will process (VAL+1) pixels. VAL[0] can not be written.

6.3.165 HST: Vertical Start Position (HST_2_VPS)

The HST: Vertical Start Position 2 (HST_2_VPS) register is shown in Figure 437 and described in Table 372.

Figure 437. HST: Vertical Start Position (HST_2_VPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 372. HST: Vertical Start Position (HST_2_VPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical start position of the region2 from the SRC_VPS. The region will start the "Histogram" processing from VAL'th line. VAL[0] can not be written.

6.3.166 HST: Vertical Size (HST_2_VSZ)

The HST: Vertical Size 2 (HST_2_VSZ) register is shown in Figure 438 and described in Table 373.

Figure 438. HST: Vertical Size (HST_2_VSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 373. HST: Vertical Size (HST_2_VSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical size of the region2 The "Histogram" processing of the region will process (VAL+1) lines. VAL[0] can not be written.

6.3.167 HST: Horizontal Start Position (HST_2_HPS)

The HST: horizontal start position 2 (HST_2_HPS) register is shown in Figure 439 and described in Table 374.

Figure 439. HST: Horizontal Start Position (HST_2_HPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 374. HST: Horizontal Start Position (HST_2_HPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Reserved.
12-0	VAL	0-1FFFh	Horizontal start position of the region2 from the SRC_VPS. The region will start the "Histogram" processing from VAL'th pixel. VAL[0] can not be written.

6.3.168 HST: Horizontal Size (HST_2_HSZ)

The HST: horizontal size 2 (HST_2_HSZ) register is shown in Figure 440 and described in Table 375.

Figure 440. HST: Horizontal Size (HST_2_HSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 375. HST: Horizontal Size (HST_2_HSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal size of the region2. The "Histogram" processing of the region will process (VAL+1) pixels. VAL[0] can not be written.

6.3.169 HST: Vertical Start Position (HST_3_VPS)

The HST: vertical start position 3 (HST_3_VPS) register is shown in Figure 441 and described in Table 376.

Figure 441. HST: Vertical Start Position (HST_3_VPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 376. HST: Vertical Start Position (HST_3_VPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical start position of the region3 from the SRC_VPS. The region will start the "Histogram" processing from VAL'th line. VAL[0] can not be written.

6.3.170 HST: Vertical Size (HST_3_VSZ)

The HST: vertical size 3 (HST_3_VSZ) register is shown in Figure 442 and described in Table 377.

Figure 442. HST: Vertical Size (HST_3_VSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 377. HST: Vertical Size (HST_3_VSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical size of the region3. The "Histogram" processing of the region will process (VAL+1) lines. VAL[0] can not be written.

6.3.171 HST: Horizontal Start Position (HST_3_HPS)

The HST: horizontal start position 3 (HST_3_HPS) register is shown in Figure 443 and described in Table 378.

Figure 443. HST: Horizontal Start Position (HST_3_HPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 378. HST: Horizontal Start Position (HST_3_HPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal start position of the region3 from the SRC_VPS. The region will start the "Histogram" processing from VAL'th pixel. VAL[0] can not be written.

6.3.172 HST: Horizontal Size (HST_3_HSZ)

The HST: horizontal size 3 (HST_3_HSZ) register is shown in Figure 444 and described in Figure 444.

Figure 444. HST: Horizontal Size (HST_3_HSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 379. HST: Horizontal Size (HST_3_HSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal size of the region3. The "Histogram" processing of the region will process (VAL+1) pixels. VAL[0] can not be written.

6.3.173 HST: Table Select (HST_TBL)

The HST: Table Select (HST_TBL) register is shown in Figure 445 and described in Table 380.

Figure 445. HST: Table Select (HST_TBL) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	CLR	SEL
R-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 380. HST: Table Select (HST_TBL) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	CLR		Table Initialization When this bit is high, the table memory is cleared at VD. When high, the first line of each frame can not be sampled.
		0	disable
		1	enable
0	SEL		Output Table Select
		0	use Table 0 and 1
		1	use Table 2 and 3

6.3.174 HST: Matrix Coefficient (HST_MUL_R)

The HST: Matrix Coefficient (HST_MUL_R) register is shown in Figure 446 and described in Table 381.

Figure 446. HST: Matrix Coefficient (HST_MUL_R) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 381. HST: Matrix Coefficient (HST_MUL_R) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Matrix Coefficient for R used for the calculation of Y sampling value (S4.4) Y=MUL_R*R+MUL_GR*Gb+MUL_GB*Gr+MUL_B*B

6.3.175 HST: Matrix Coefficient (HST_MUL_GR)

The HST: Matrix Coefficient (HST_MUL_GR) register is shown in Figure 447 and described in Table 382.

Figure 447. HST: Matrix Coefficient (HST_MUL_GR) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 382. HST: Matrix Coefficient (HST_MUL_GR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Matrix Coefficient for Gr used for the calculation of Y sampling value (S4.4) Y=MUL_R*R+MUL_GR*Gb+MUL_GB*Gr+MUL_B*B

6.3.176 HST: Matrix Coefficient (HST_MUL_GB)

The HST: Matrix Coefficient (HST_MUL_GB) register is shown in Figure 448 and described in Table 383.

Figure 448. HST: Matrix Coefficient (HST_MUL_GB) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 383. HST: Matrix Coefficient (HST_MUL_GB) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Matrix Coefficient for Gb used for the calculation of Y sampling value (S4.4) Y=MUL_R*R+MUL_GR*Gb+MUL_GB*Gr+MUL_B*B

6.3.177 HST: Matrix Coefficient (HST_MUL_B)

The HST: Matrix Coefficient (HST_MUL_B) register is shown in Figure 449 and described in Table 384.

Figure 449. HST: Matrix Coefficient (HST_MUL_B) Register

31-16	
Reserved	
R-0	
15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 384. HST: Matrix Coefficient (HST_MUL_B) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Matrix Coefficient for B used for the calculation of Y sampling value (S4.4) Y=MUL_R*R+MUL_GR*Gb+MUL_GB*Gr+MUL_B*B

6.3.178 BSC (=Boundary Signal Calculator): Enable (BSC_EN)

The BSC (=Boundary Signal Calculator): Enable (BSC_EN) register is shown in Figure 450 and described in Table 385.

Figure 450. BSC (=Boundary Signal Calculator): Enable (BSC_EN) Register

31-16	
Reserved	
R-0	
15-1	**0**
Reserved	EN
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 385. BSC (=Boundary Signal Calculator): Enable (BSC_EN) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		Boundary Signal Calculator Enable
		0	disable
		1	enable

6.3.179 BSC: One Shot Mode (BSC_MODE)

The One Shot Mode (BSC_MODE) is shown in Figure 451 and described in Table 386.

Figure 451. One Shot Mode (BSC_MODE) Register

31-16
Reserved
R-0

15-1	0
Reserved	OST
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 386. One Shot Mode (BSC_MODE) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	OST		BSC One Shot Mode Enable
		0	continuous mode
		1	one shot mode

6.3.180 BSC: Y/Cb/Cr Select (BSC_TYP)

The Y/Cb/Cr Select (BSC_TYP) register is shown in Figure 452 and described in Table 387.

Figure 452. Y/Cb/Cr Select (BSC_TYP) Register

31-16
Reserved
R-0

15-4	3	2	1-0
Reserved	CEN	REN	COL
R-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 387. Y/Cb/Cr Select (BSC_TYP) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
3	CEN		BSC Enable of column sampling
		0	disable
		1	enable
2	REN		BSC Enable of row sampling
		0	disable
		1	enable
1-0	COL		Selects the element to be summed. (Y, Cb or Cr) in BSC
		0	Y
		1	Cb
		2	Cr

6.3.181 BSC: Number of Row Vectors (BSC_ROW_VCT)

The Number of Row Vectors (BSC_ROW_VCT) register is shown in Figure 453 and described in Table 388.

Figure 453. Number of Row Vectors (BSC_ROW_VCT) Register

31-16
Reserved
R-0

15-2	1-0
Reserved	ROWNUM
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 388. Number of Row Vectors (BSC_ROW_VCT) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1-0	ROWNUM	0-3h	BSC: Number of row sum vectors number = ROWNUM + 1.

6.3.182 BSC: Down Shift Value of Input for Row Sum (BSC_ROW_SHF)

The Down Shift Value of Input for Row Sum (BSC_ROW_SHF) register is shown in Figure 454 and described in Table 389.

Figure 454. Down Shift Value of Input for Row Sum (BSC_ROW_SHF) Register

31-16
Reserved
R-0

15-3	2-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 389. Down Shift Value of Input for Row Sum (BSC_ROW_SHF) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2-0	VAL	0-7h	BSC: Down shift value for row sum vectors.

6.3.183 BSC: Vertical Starting Position of Row Sum (BSC_ROW_VPOS)

The Vertical Starting Position of Row Sum (BSC_ROW_VPOS) register is shown in Figure 455 and described in Table 390.

Figure 455. Vertical Starting Position of Row Sum (BSC_ROW_VPOS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 390. Vertical Starting Position of Row Sum (BSC_ROW_VPOS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	BSC: Vertical position of the first sampling pixel The first row to be summed.

6.3.184 BSC: Vertical Number of Sampled Lines for Row Sum (BSC_ROW_VNUM)

The Vertical Number of Sampled Lines for Row Sum (BSC_ROW_VNUM) register is shown in Figure 456 and described in Table 391.

Figure 456. Vertical Number of Sampled Lines for Row Sum (BSC_ROW_VNUM) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 391. Vertical Number of Sampled Lines for Row Sum (BSC_ROW_VNUM) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	BSC: The height of the area covered by a row sum vector Height of the region = (ROW_VNUM + 1)*(ROW_VSKIP+1). This value must be odd.

6.3.185 BSC: Vertical Spacing between Adjacent Sampled Lines for Row Sum (BSC_ROW_VSKIP)

The Vertical Spacing between Adjacent Sampled Lines for Row Sum (BSC_ROW_VSKIP) register is shown in Figure 457 and described in Table 392.

Figure 457. Vertical Spacing between Adjacent Sampled Lines for Row Sum (BSC_ROW_VSKIP) Register

31-16
Reserved
R-0

15-5	4-0
Reserved	ROWSKIPV
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 392. Vertical Spacing between Adjacent Sampled Lines for Row Sum (BSC_ROW_VSKIP) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4-0	ROWSKIPV	0-1Fh	BSC: Interval of the rows Interval = ROWSKIPV + 1.

6.3.186 BSC: Horizontal Starting Position of Row Sum (BSC_ROW_HPOS)

The Horizontal Starting Position of Row Sum (BSC_ROW_HPOS) register is shown in Figure 458 and described in Table 393.

Figure 458. Horizontal Starting Position of Row Sum (BSC_ROW_HPOS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 393. Horizontal Starting Position of Row Sum (BSC_ROW_HPOS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	BSC: Horizontal position of the first sampling pixel The first pixel in a row to be summed.

6.3.187 BSC: Horizontal Number of Sampled Lines for Row Sum (BSC_ROW_HNUM)

The Horizontal Number of Sampled Lines for Row Sum (BSC_ROW_HNUM) register is shown in Figure 459 and described in Table 394.

Figure 459. Horizontal Number of Sampled Lines for Row Sum (BSC_ROW_HNUM) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 394. Horizontal Number of Sampled Lines for Row Sum (BSC_ROW_HNUM) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	BSC: The horizontal number of samples in the area covered by a row sum vector Width of the region = (ROW_HNUM + 1)*(ROW_HSKIP+1)

6.3.188 BSC: Horizontal Spacing between Adjacent Sampled Lines for Row Sum (BSC_ROW_HSKIP)

The Horizontal Spacing between Adjacent Sampled Lines for Row Sum (BSC_ROW_HSKIP) register is shown in Figure 460 and described in Table 395.

Figure 460. Horizontal Spacing between Adjacent Sampled Lines for Row Sum (BSC_ROW_HSKIP) Register

31-16
Reserved
R-0

15-5	4-0
Reserved	ROWSKIPH
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 395. Horizontal Spacing between Adjacent Sampled Lines for Row Sum (BSC_ROW_HSKIP) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4-0	ROWSKIPH	0-1Fh	BSC: Interval of the pixels in a row to be summed Interval = ROWSKIPH + 1

6.3.189 BSC: Number of Column Vectors (BSC_COL_VCT)

The Number of Column Vectors (BSC_COL_VCT) register is shown in Figure 461 and described in Table 396.

Figure 461. Number of Column Vectors (BSC_COL_VCT) Register

31-16
Reserved
R-0

15-2	1-0
Reserved	COLNUM
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 396. Number of Column Vectors (BSC_COL_VCT) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1-0	COLNUM	0-3h	BSC: Number of column sum vectors number = COLNUM + 1.

6.3.190 BSC: Down Shift Value of Input for Column Sum (BSC_COL_SHF)

The Down Shift Value of Input for Column Sum (BSC_COL_SHF) register is shown in Figure 462 and described in Table 397.

Figure 462. Down Shift Value of Input for Column Sum (BSC_COL_SHF) Register

31-16
Reserved
R-0

15-3	2-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 397. Down Shift Value of Input for Column Sum (BSC_COL_SHF) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2-0	VAL	0-7h	BSC: Down shift value for column sum vectors.

6.3.191 BSC: Vertical Starting Position of Column Sum (BSC_COL_VPOS)

The Vertical Starting Position of Column Sum (BSC_COL_VPOS) register is shown in Figure 463 and described in Table 398.

Figure 463. Vertical Starting Position of Column Sum (BSC_COL_VPOS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 398. Vertical Starting Position of Column Sum (BSC_COL_VPOS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	BSC: Vertical position of the first sampling pixel The first column to be summed.

6.3.192 BSC: Vertical Number of Sampled Lines for Column Sum (BSC_COL_VNUM)

The Vertical Number of Sampled Lines for Column Sum (BSC_COL_VNUM) register is shown in Figure 464 and described in Table 399.

Figure 464. Vertical Number of Sampled Lines for Column Sum (BSC_COL_VNUM) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 399. Vertical Number of Sampled Lines for Column Sum (BSC_COL_VNUM) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	BSC: Vertical number of samples in the area covered by a column sum vector Height of the region = (COL_VNUM + 1)*(COL_VSKIP+1).

6.3.193 BSC: Vertical Spacing between Adjacent Sampled Lines for Column Sum (BSC_COL_VSKIP)

The Vertical Spacing between Adjacent Sampled Lines for Column Sum (BSC_COL_VSKIP) register is shown in Figure 465 and described in Table 400.

Figure 465. Vertical Spacing between Adjacent Sampled Lines for Column Sum (BSC_COL_VSKIP) Register

31-16
Reserved
R-0

15-5	4-0
Reserved	COLSKIPV
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 400. Vertical Spacing between Adjacent Sampled Lines for Column Sum (BSC_COL_VSKIP) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4-0	COLSKIPV	0-1Fh	BSC: Interval of the pixels in a column to be summed Interval = COLSKIPV + 1.

6.3.194 BSC: Horizontal Starting Position of Column Sum (BSC_COL_HPOS)

The Horizontal Starting Position of Column Sum (BSC_COL_HPOS) register is shown in Figure 466 and described in Table 401.

Figure 466. Horizontal Starting Position of Column Sum (BSC_COL_HPOS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 401. Horizontal Starting Position of Column Sum (BSC_COL_HPOS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	BSC: Horizontal position of the first sampling pixel The first column to be summed.

6.3.195 BSC: Horizontal Number of Sampled Lines for Column Sum (BSC_COL_HNUM)

The Horizontal Number of Sampled Lines for Column Sum (BSC_COL_HNUM) register is shown in Figure 467 and described in Table 402.

Figure 467. Horizontal Number of Sampled Lines for Column Sum (BSC_COL_HNUM) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-1

LEGEND: R = Read only; -*n* = value after reset

Table 402. Horizontal Number of Sampled Lines for Column Sum (BSC_COL_HNUM) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	BSC: Width of the area covered by a column sum vector Width of the region = (COL_HNUM + 1)*(COL_HSKIP+1). This value must be odd.

6.3.196 BSC: Horizontal Spacing between Adjacent Sampled Lines for Column Sum (BSC_COL_HSKIP)

The Horizontal Spacing between Adjacent Sampled Lines for Column Sum (BSC_COL_HSKIP) register is shown in Figure 468 and described in Table 403.

Figure 468. Horizontal Spacing between Adjacent Sampled Lines for Column Sum (BSC_COL_HSKIP) Register

31-16
Reserved
R-0

15-5	4-0
Reserved	COLSKIPH
R-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 403. Horizontal Spacing between Adjacent Sampled Lines for Column Sum (BSC_COL_HSKIP) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4-0	COLSKIPH	0-1Fh	BSC: Interval of the columns Interval = COLSKIPH + 1.

6.4 Resizer (RSZ) Registers

Table 404 lists the memory-mapped registers for the resizer (RSZ) registers. See the device-specific data manual for the memory addresses of these registers.

Table 404. Resizer (RSZ) Registers

Offset	Acronym	Register Description	Section
0h	SRC_EN	Source Enable	Section 6.4.1
04h	SRC_MODE	One Shot Mode	Section 6.4.2
08h	SRC_FMT0	Input Data Paths	Section 6.4.3
0Ch	SRC_FMT1	Source Image Format	Section 6.4.4
010h	SRC_VPS	Vertical Start Position	Section 6.4.5
014h	SRC_VSZ	Vertical Processing Size	Section 6.4.6
018h	SRC_HPS	Horizontal Start Position	Section 6.4.7
01Ch	SRC_HSZ	Horizontal Processing Size	Section 6.4.8
020h	DMA_RZA	SDRAM Request Minimum Interval for RZA	Section 6.4.9
024h	DMA_RZB	SDRAM Request Minimum Interval for RZB	Section 6.4.10
028h	DMA_STA	Status of Resizer (Reserved)	Section 6.4.11
02Ch	GCK_MMR	MMR Gated Clock Control	Section 6.4.12
030h	Reserved	Reserved	
034h	GCK_SDR	SDR Gated Clock Control	Section 6.4.13
038h	IRQ_RZA	Interval of RZA Circular IRQ	Section 6.4.14
03Ch	IRQ_RZB	Interval of RZB Circular IRQ	Section 6.4.15
040h	YUV_Y_MIN	Saturation (Luminance Minimum)	Section 6.4.16
044h	YUV_Y_MAX	Saturation (Luminance Maximum)	Section 6.4.17
048h	YUV_C_MIN	Saturation (Chrominance Minimum)	Section 6.4.18
04Ch	YUV_C_MAX	Saturation (Chrominance Maximum)	Section 6.4.19
050h	YUV_PHS	Chrominance Position	Section 6.4.20
054h	SEQ	Processing Mode	Section 6.4.21
058h	RZA_EN	RZA: Enable	Section 6.4.22
05Ch	RZA_MODE	RZA: One Shot Mode	Section 6.4.23
060h	RZA_420	RZA: 420 Output Format	Section 6.4.24
064h	RZA_I_VPS	RZA: Vertical Start Position of the Input	Section 6.4.25
068h	RZA_I_HPS	RZA: Horizontal Start Position of the Input	Section 6.4.26
06Ch	RZA_O_VSZ	RZA: Vertical Size of the Output	Section 6.4.27
070h	RZA_O_HSZ	RZA: Horizontal Size of the Output	Section 6.4.27
074h	RZA_V_PHS_Y	RZA: Initial Phase of Vertical Resizing Process for Luminance	Section 6.4.29
078h	RZA_V_PHS_C	RZA: Initial Phase of Vertical Resizing Process for Chrominance	Section 6.4.30
07Ch	RZA_V_DIF	RZA: Vertical Resize Parameter	Section 6.4.31
080h	RZA_V_TYP	RZA: Interpolation Method for Vertical Rescaling	Section 6.4.32
084h	RZA_V_LPF	RZA: Vertical LPF Intensity	Section 6.4.33
088h	RZA_H_PHS	RZA: Initial Phase of Horizontal Resizing Process	Section 6.4.34
08Ch	RZA_H_PHS_ADJ	RZA: Additional Initial Phase of Vertical Resizing Process for Luminance	Section 6.4.35
090h	RZA_H_DIF	RZA: Horizontal Resize Parameter	Section 6.4.36
094h	RZA_H_TYP	RZA: Interpolation Method for Horizontal Rescaling	Section 6.4.37
098h	RZA_H_LPF	RZA: Horizontal LPF Intensity	Section 6.4.38
09Ch	RZA_DWN_EN	RZA: Down Scale Mode Enable	Section 6.4.39
0A0h	RZA_DWN_AV	RZA: Down Scale Mode Averaging Size	Section 6.4.40
0A4h	RZA_RGB_EN	RZA: RGB Output Enable	Section 6.4.41
0A8h	RZA_RGB_TYP	RZA: RGB Output Bit Mode	Section 6.4.42

Table 404. Resizer (RSZ) Registers (continued)

Offset	Acronym	Register Description	Section
0ACh	RZA_RGB_BLD	RZA: YC422 to YC444 Conversion Method	Section 6.4.43
0B0h	RZA_SDR_Y_BAD_H	RZA: SDRAM Base Address MSB	Section 6.4.44
0B4h	RZA_SDR_Y_BAD_L	RZA: SDRAM Base Address LSB	Section 6.4.45
0B8h	RZA_SDR_Y_SAD_H	RZA: SDRAM Start Address MSB	Section 6.4.46
0BCh	RZA_SDR_Y_SAD_L	RZA: SDRAM Start Address LSB	Section 6.4.47
0C0h	RZA_SDR_Y_OFT	RZA: SDRAM Line Offset	Section 6.4.48
0C4h	RZA_SDR_Y_PTR_S	RZA: Start Line of SDRAM Pointer	Section 6.4.49
0C8h	RZA_SDR_Y_PTR_E	RZA: End Line of SDRAM Pointer	Section 6.4.50
0CCh	RZA_SDR_C_BAD_H	RZA: SDRAM Base Address MSB (for 420 Chroma)	Section 6.4.51
0D0h	RZA_SDR_C_BAD_L	RZA: SDRAM Base Address LSB (for 420 Chroma)	Section 6.4.52
0D4h	RZA_SDR_C_SAD_H	RZA: SDRAM Start Address MSB (for 420 Chroma)	Section 6.4.53
0D8h	RZA_SDR_C_SAD_L	RZA: SDRAM Start Address LSB (for 420 Chroma)	Section 6.4.54
0DCh	RZA_SDR_C_OFT	RZA: SDRAM Line Offset (for 420 Chroma)	Section 6.4.55
0E0h	RZA_SDR_C_PTR_S	RZA: Start Line of SDRAM Pointer (for 420 Chroma)	Section 6.4.56
0E4h	RZA_SDR_C_PTR_E	RZA: End Line of SDRAM Pointer (for 420 Chroma)	Section 6.4.57
0E8h	RZB_EN	RZB: Enable	Section 6.4.58
0ECh	RZB_MODE	RZB: One Shot Mode	Section 6.4.59
0F0h	RZB_420	RZB: 420 Output Format	Section 6.4.60
0F4h	RZB_I_VPS	RZB: Vertical Start Position of the Input	Section 6.4.61
0F8h	RZB_I_HPS	RZB: Horizontal Start Position of the Input	Section 6.4.62
0FCh	RZB_O_VSZ	RZB: Vertical Size of the Output	Section 6.4.63
100h	RZB_O_HSZ	RZB: Horizontal Size of the Output	Section 6.4.64
104h	RZB_V_PHS_Y	RZB: Initial Phase of Vertical Resizing Process for Luminance	Section 6.4.65
108h	RZB_V_PHS_C	RZB: Initial Phase of Vertical Resizing Process for Chrominance	Section 6.4.66
10Ch	RZB_V_DIF	RZB: Vertical Resize Parameter	Section 6.4.67
110h	RZB_V_TYP	RZB: Interpolation Method for Vertical Rescaling	Section 6.4.68
114h	RZB_V_LPF	RZB: Vertical LPF Intensity	Section 6.4.69
118h	RZB_H_PHS	RZB: Initial Phase of Horizontal Resizing Process	Section 6.4.70
11Ch	RZB_H_PHS_ADJ	RZB: Additional Initial Phase of Horizontal Resizing Process for Luminance	Section 6.4.71
120h	RZB_H_DIF	RZB: Horizontal Resize Parameter	Section 6.4.72
124h	RZB_H_TYP	RZB: Interpolation Method for Horizontal Rescaling	Section 6.4.73
128h	RZB_H_LPF	RZB: Horizontal LPF Intensity	Section 6.4.74
12Ch	RZB_DWN_EN	RZB: Down Scale Mode Enable	Section 6.4.75
130h	RZB_DWN_AV	RZB: Down Scale Mode Averaging Size	Section 6.4.76
134h	RZB_RGB_EN	RZB: RGB Output Enable	Section 6.4.77
138h	RZB_RGB_TYP	RZB: RGB Output Bit Mode	Section 6.4.78
13Ch	RZB_RGB_BLD	RZB: YC422 to YC444 Conversion Method	Section 6.4.79
140h	RZB_SDR_Y_BAD_H	RZB: SDRAM Base Address MSB	Section 6.4.80
144h	RZB_SDR_Y_BAD_L	RZB: SDRAM Base Address LSB	Section 6.4.81
148h	RZB_SDR_Y_SAD_H	RZB: SDRAM Start Address MSB	Section 6.4.82
14Ch	RZB_SDR_Y_SAD_L	RZB: SDRAM Start Address LSB	Section 6.4.83
150h	RZB_SDR_Y_OFT	RZB: SDRAM Line Offset	Section 6.4.84
154h	RZB_SDR_Y_PTR_S	RZB: Start Line of SDRAM Pointer	Section 6.4.85
158h	RZB_SDR_Y_PTR_E	RZB: End Line of SDRAM Pointer	Section 6.4.86
15Ch	RZB_SDR_C_BAD_H	RZB: SDRAM Base Address MSB (for 420 Chroma)	Section 6.4.87
160h	RZB_SDR_C_BAD_L	RZB: SDRAM Base Address LSB (for 420 Chroma)	Section 6.4.88
164h	RZB_SDR_C_SAD_H	RZB: SDRAM Start Address MSB (for 420 Chroma)	Section 6.4.89

Table 404. Resizer (RSZ) Registers (continued)

Offset	Acronym	Register Description	Section
168h	RZB_SDR_C_SAD_L	RZB: SDRAM Start Address LSB (for 420 Chroma)	Section 6.4.90
16Ch	RZB_SDR_C_OFT	RZB: SDRAM Line Offset (for 420 Chroma)	Section 6.4.91
170h	RZB_SDR_C_PTR_S	RZB: Start Line of SDRAM Pointer (for 420 Chroma)	Section 6.4.91
174h	RZB_SDR_C_PTR_E	RZB: End Line of SDRAM Pointer (for 420 Chroma)	Section 6.4.93

6.4.1 Source Enable (SRC_EN)

The Source Enable (SRC_EN) register is shown in Figure 469 and described in Table 405.

Figure 469. Source Enable (SRC_EN) Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 405. Source Enable (SRC_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		RSZ Enable The start flag of the RSZ module. When EN is 1, the RSZ module starts a processing from the next rising edge of the VD. If the processing mode of the RSZ module is "one shot", the EN is cleared to 0 after the end of the processing area.
		0	disable
		1	enable

6.4.2 One Shot Mode (SRC_MODE)

The One Shot Mode (SRC_MODE) register is shown in Figure 470 and described in Table 406.

Figure 470. One Shot Mode (SRC_MODE) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	WRT	OST
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 406. One Shot Mode (SRC_MODE) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	WRT		C_WE Mode Selection The mode selection of the ipipeif_wrt which is an input port of the IPIPE module. If WRT is 0, the IPIPE module does not use the ipipeif_wrt. Else, the IPIPE module uses it.
		0	disable
		1	enable
0	OST		One Shot Mode The processing mode selection of the IPIPE module. Value 0 indicates the mode of "free run", value 1 indicates the mode of "one shot".
		0	disable
		1	enable

6.4.3 Input Data Paths (SRC_FMT0)

The Input Data Paths (SRC_FMT0) register is shown in Figure 471 and described in Table 407.

Figure 471. Input Data Paths (SRC_FMT0) Register

31-16		
Reserved		
R-0		
15-2	1	0
Reserved	BYPASS	SRC
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 407. Input Data Paths (SRC_FMT0) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	BYPASS		Enable Pass-through mode, where large raw image up to 8190 pixels per line may be processed. When enabled, all image processing is skipped. To select BYPASS mode, following values are set. SRC_FMT1[420] = 422; RZA_EN = ENABLE; RZA_420[Y] = DISABLE; RZA_420[C] = DISABLE; RZA_I_VPS = 0; RZA_I_HPS = 0; RZA_V_PHS_Y = 0; RZA_V_PHS_C = 0; RZA_V_DIF = 256; RZA_V_LPF[Y] = 0; RZA_V_LPF[C] = 0; RZA_H_PHS = 0; RZA_H_PHS_ADJ = 0; RZA_H_DIF = 256; RZA_H_LPF[Y] = 0; RZA_H_LPF[C] = 0; RZA_DWN_EN = DISABLE; RZA_RGB_EN = DISABLE; RZB_EN = DISABLE
		0	Passthrough mode off
		1	Passthrough mode on
0	SRC		Data Path through RSZ
		0	from IPIPE
		1	from IPIPEIF

6.4.4 Source Image Format (SRC_FMT1)

The Source Image Format (SRC_FMT1) register is shown in Figure 472 and described in Table 408.

Figure 472. Source Image Format (SRC_FMT1) Register

31-16
Reserved
R-0

15-3	2	1	0
Reserved	COL	420	RAW
R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 408. Source Image Format (SRC_FMT1) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2	COL		Y/C Selection This bit is valid in 420 input mode (SRC_FMT1[420]=1)
		0	Y
		1	C
1	420		Chroma Format Selection
		0	422 image
		1	420 image
0	RAW		Pass-through mode input data format selection This bit affects the horizontal reversal (flipping) process.
		0	Flipping preserves YcbCr format
		1	Flipping preserves Raw format

6.4.5 Vertical Start Position (SRC_VPS)

The Vertical Start Position (SRC_VPS) register is shown in Figure 473 and described in Table 409.

Figure 473. Vertical Start Position (SRC_VPS) Register

31-16
Reserved
R-0
15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 409. Vertical Start Position (SRC_VPS) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	Vertical Start Position (0-65534) The vertical position of the global frame from the rising edge of the VD. The RSZ module will start an image processing from VAL'th line.

6.4.6 Vertical Processing Size (SRC_VSZ)

The Vertical Processing Size (SRC_VSZ) register is shown in Figure 474 and described in Table 410.

Figure 474. Vertical Processing Size (SRC_VSZ) Register

31-16		
Reserved		
R-0		
15-13		12-0
Reserved		VAL
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 410. Vertical Processing Size (SRC_VSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical Processing Size (0-8190) The vertical size of the processing area. The RSZ module will process (VAL+1) lines.

6.4.7 Horizontal Start Position (SRC_HPS)

The Horizontal Start Position (SRC_HPS) register is shown in Figure 475 and described in Table 411.

Figure 475. Horizontal Start Position (SRC_HPS) Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 411. Horizontal Start Position (SRC_HPS) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	Horizontal Start Position (0-65534). The horizontal position of the global frame from the rising edge of the HD. The RSZ module will start an image processing from VAL pixel.

6.4.8 Horizontal Processing Size (SRC_HSZ)

The Horizontal Processing Size (SRC_HSZ) register is shown in Figure 476 and described in Table 412.

Figure 476. Horizontal Processing Size (SRC_HSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 412. Horizontal Processing Size (SRC_HSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal Processing Size (0-8189) The horizontal size of the processing area. VAL[0] can not be written. The RSZ module will process (VAL+1) pixels.

6.4.9 SDRAM Request Minimum Interval for RZA (DMA_RZA)

The SDRAM Request Minimum Interval for RZA (DMA_RZA) register is shown in Figure 477 and described in Table 413.

Figure 477. SDRAM Request Minimum Interval for RZA (DMA_RZA) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 413. SDRAM Request Minimum Interval for RZA (DMA_RZA) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Minimum interval between two consecutive SDRAM requests for resize-A Specified in number of VPSS clock cycles

6.4.10 SDRAM Request Minimum Interval for RZB (DMA_RZB)

The SDRAM Request Minimum Interval for RZB (DMA_RZB) register is shown in Figure 478 and described in Table 414.

Figure 478. SDRAM Request Minimum Interval for RZB (DMA_RZB) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 414. SDRAM Request Minimum Interval for RZB (DMA_RZB) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Minimum interval between two consecutive SDRAM requests for resize-B Specified in number of VPSS clock cycles.

6.4.11 Status of Resizer (DMA_STA)

The Status of Resizer (DMA_STA) register is shown in Figure 479 and described in Table 415.

Figure 479. Status of Resizer (DMA_STA) Register

31-16
Reserved
R-0

15-1	0
Reserved	STATUS
R-0	R-0

LEGEND: R = Read only; -*n* = value after reset

Table 415. Status of Resizer (DMA_STA) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	STATUS	0-1	Resize Process Status

6.4.12 MMR Gated Clock Control (GCK_MMR)

The MMR Gated Clock Control (GCK_MMR) register is shown in Figure 480 and described in Table 416.

Figure 480. MMR Gated Clock Control (GCK_MMR) Register

31-16
Reserved
R-0

15-1	0
Reserved	REG
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 416. MMR Gated Clock Control (GCK_MMR) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	REG		RSZ MMR Clock Enable The on/off selection of the MMR interface clock (clk_mmr_g0) which is used for MMR register accesses. When this bit is off, the registers except the following may not be written. Read access is allowed. SRC_EN GCK_MMR GCK_SDR RZA_EN RZB_EN
		0	off
		1	on

6.4.13 SDR Gated Clock Control (GCK_SDR)

The SDR Gated Clock Control (GCK_SDR) register is shown in Figure 481 and described in Table 417.

Figure 481. SDR Gated Clock Control (GCK_SDR) Register

31-16
Reserved
R-0

15-1	0
Reserved	CORE
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 417. SDR Gated Clock Control (GCK_SDR) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	CORE		RSZ Core Clock Enable The on/off selection of clk_vpss_g0 which is used for "Resizer Core". When this bit is off, Resizer core (interpolator) is automatically bypassed (resizer-bypass mode of pass-through mode depending on SRC_FMT0 value). In resizer-bypass mode or pass-through mode, no up-scaling or down scaling process is operated. Rescaling : GCK_SDR=1, SRC_FMT0[BYPASSS]=0 Resizer bypass : GCK_SDR=0, SRC_FMT0[BYPASSS]=0 Pass-through : GCK_SDR=0, SRC_FMT0[BYPASSS]=1
		0	off
		1	on

6.4.14 Interval of RZA Circular IRQ (IRQ_RZA)

The Interval of RZA Circular IRQ (IRQ_RZA) register is shown in Figure 482 and described in Table 418.

Figure 482. Interval of RZA Circular IRQ (IRQ_RZA) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-8191

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 418. Interval of RZA Circular IRQ (IRQ_RZA) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Interval of RZA circular IRQ Interrupt signal at every (VAL+1) lines of Resize and RGB output

6.4.15 Interval of RZB Circular IRQ (IRQ_RZB)

The Interval of RZB Circular IRQ (IRQ_RZB) register is shown in Figure 483 and described in Table 419.

Figure 483. Interval of RZB Circular IRQ (IRQ_RZB) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-8191

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 419. Interval of RZB Circular IRQ (IRQ_RZB) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Interval of RZB circular IRQ Interrupt signal at every (VAL+1) lines of Resize and RGB output

6.4.16 Saturation (Luminance Minimum) (YUV_Y_MIN)

The Saturation (Luminance Minimum) (YUV_Y_MIN) register is shown in Figure 484 and described in Table 420.

Figure 484. Saturation (Luminance Minimum) (YUV_Y_MIN) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 420. Saturation (Luminance Minimum) (YUV_Y_MIN) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Minimum Luminance Value In RAW data processing, this value should be 0

6.4.17 Saturation (Luminance Maximum) (YUV_Y_MAX)

The Saturation (Luminance Maximum) (YUV_Y_MAX) register is shown in Figure 485 and described in Table 421.

Figure 485. Saturation (Luminance Maximum) (YUV_Y_MAX) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-0	R/W-255

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 421. Saturation (Luminance Maximum) (YUV_Y_MAX) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Maximum Luminance Value In RAW data processing, this value should be 255

6.4.18 Saturation (Chrominance Minimum) (YUV_C_MIN)

The Saturation (Chrominance Minimum) (YUV_C_MIN) register is shown in Figure 486 and described in Table 422.

Figure 486. Saturation (Chrominance Minimum) (YUV_C_MIN) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 422. Saturation (Chrominance Minimum) (YUV_C_MIN) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Minimum Chrominance Value In RAW data processing, this value should be 0

6.4.19 Saturation (Chrominance Maximum) (YUV_C_MAX)

The Saturation (Chrominance Maximum) (YUV_C_MAX) register is shown in Figure 487 and described in Table 423.

Figure 487. Saturation (Chrominance Maximum) (YUV_C_MAX) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-0	R/W-255

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 423. Saturation (Chrominance Maximum) (YUV_C_MAX) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	Maximum Chrominance Value In RAW data processing, this value should be 255

6.4.20 Chrominance Position (YUV_PHS)

The Chrominance Position (YUV_PHS) register is shown in Figure 488 and described in Table 424.

Figure 488. Chrominance Position (YUV_PHS) Register

31-16
Reserved
R-0

15-1	0
Reserved	POS
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 424. Chrominance Position (YUV_PHS) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	POS		Phase position of the output of the Chrominance
		0	same position with Luminance
		1	the middle of the Luminance

6.4.21 Processing Mode (SEQ)

The Processing Mode (SEQ) register is shown in Figure 489 and described in Table 425.

Figure 489. Processing Mode (SEQ) Register

31-16					
Reserved					
R-0					
15-5	4	3	2	1	0
Reserved	CRV	VRVB	HRVB	VRVA	HRVA
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 425. Processing Mode (SEQ) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4	CRV		Chroma sampling point change If CRV is 1, chroma sampling point is changed from odd-numbered pixels to even R-0 number pixels. The pixel the left end is removed and the pixel at the right end is duplicated. If CRV is 0, chroma sampling point is not changed.
		0	Flipping disable
		1	Flipping enable
3	VRVB		Vertical reversal of output image for RZB If VRVB is 1, the order of output data from RZB is flipped top to bottom. If VRVB is 0, processed pixels of RZB are output in the order of input (normal operation) in vertical direction.
		0	Flipping disable
		1	Flipping enable
2	HRVB		Horizontal reversal of output image for RZB If HRVB is 1, the order of output data from RZB is flipped left to right. If HRVB is 0, processed pixels of RZB are output in the order of input (normal operation) in horizontal direction.
		0	Flipping disable
		1	Flipping enable
1	VRVA		Vertical reversal of output image for RZA If VRVA is 1, the order of output data from RZA is flipped top to bottom. If VRVA is 0, processed pixels of RZA are output in the order of input (normal operation) in vertical direction.
		0	Flipping disable
		1	Flipping enable
0	HRVA		Horizontal reversal of output image for RZA If HRVA is 1, the order of output data from RZA is flipped left to right. If HRVA is 0, processed pixels of RZA are output in the order of input (normal operation) in horizontal direction.
		0	Flipping disable
		1	Flipping enable

6.4.22 RZA: Enable (RZA_EN)

The Resizer Channel A (RZA): Enable (RZA_EN) register is shown in Figure 490 and described in Table 426.

Figure 490. RZA: Enable (RZA_EN) Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 426. RZA: Enable (RZA_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		Resizer Enable In one-shot mode, this bit is negated on VD. In pass-through mode, RZA_EN enables the output
		0	disable
		1	enable

6.4.23 RZA: One Shot Mode (RZA_MODE)

The RZA: One Shot Mode (RZA_MODE) register is shown in Figure 491 and described in Table 427.

Figure 491. RZA: One Shot Mode (RZA_MODE) Register

31-16
Reserved
R-0

15-1	0
Reserved	OST
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 427. RZA: One Shot Mode (RZA_MODE) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	OST		One Shot Mode Enable
		0	continuous mode
		1	one shot mode

6.4.24 RZA: 420 Output Format (RZA_420)

The RZA: 420 Output Format (RZA_420) register is shown in Figure 492 and described in Table 428.

Figure 492. RZA: 420 Output Format (RZA_420) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	CEN	YEN
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 428. RZA: 420 Output Format (RZA_420) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	CEN		Output Enable for Chrominance This bit is valid in 422 input mode. When CEN=0 and YEN=0, output is 422
		0	C output disable
		1	C output enable and 422to420 conversion enabled
0	YEN		Output Enable for Luminance This bit is valid in 422 input mode. When CEN=0 and YEN=0, output is 422
		0	Y output disable
		1	Y output enable and 422to420 conversion enabled

6.4.25 RZA: Vertical Start Position of the Input (RZA_I_VPS)

The RZA: Vertical Start Position of the Input (RZA_I_VPS) register is shown in Figure 493 and described in Table 429.

Figure 493. RZA: Vertical Start Position of the Input (RZA_I_VPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 429. RZA: Vertical Start Position of the Input (RZA_I_VPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical start position of image processing After SRC_VPS, the VAL'th line is processed as the first line in each image.

6.4.26 RZA: Horizontal Start Position of the Input (RZA_I_HPS)

The RZA: Horizontal Start Position of the Input (RZA_I_HPS) register is shown in Figure 494 and described in Table 430.

Figure 494. RZA: Horizontal Start Position of the Input (RZA_I_HPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 430. RZA: Horizontal Start Position of the Input (RZA_I_HPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0
12-0	VAL	0-1FFFh	Horizontal start position of image processing After SRC_HPS, the VAL'th pixel is processed as the first pixel. VAL[0] can not be written.

6.4.27 RZA: Vertical Size of the Output (RZA_O_VSZ)

The RZA: Vertical Size of the Output (RZA_O_VSZ) register is shown in Figure 495 and described in Table 431.

Figure 495. RZA: Vertical Size of the Output (RZA_O_VSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 431. RZA: Vertical Size of the Output (RZA_O_VSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical size of the output image The number of output lines is (VAL+1).

6.4.28 RZA: Horizontal Size of the Output (RZA_O_HSZ)

The RZA: Horizontal Size of the Output (RZA_O_HSZ) register is shown in Figure 496 and described in Table 432.

Figure 496. RZA: Horizontal Size of the Output (RZA_O_HSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 432. RZA: Horizontal Size of the Output (RZA_O_HSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal size of output image The number of pixel in each line is (VAL+1). VAL[0] can not be written. RZA_O_HSZ ≤ 2176 in normal mode, RZA_O_HSZ ≤ 1088 in down scale mode

6.4.29 RZA: Initial Phase of Vertical Resizing Process for Luminance (RZA_V_PHS_Y)

The RZA: Initial Phase of Vertical Resizing Process for Luminance (RZA_V_PHS_Y) register is shown in Figure 497and described in Table 433.

Figure 497. RZA: Initial Phase of Vertical Resizing Process for Luminance (RZA_V_PHS_Y) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 433. RZA: Initial Phase of Vertical Resizing Process for Luminance (RZA_V_PHS_Y) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Initial value for the phase value in vertical resizing process for Luminance (0-10000) Usually this values is zero except in Frame Division Operation - V.

6.4.30 RZA: Initial Phase of Vertical Resizing Process for Chrominance (RZA_V_PHS_C)

The RZA: Initial Phase of Vertical Resizing Process for Chrominance (RZA_V_PHS_C) register is shown in Figure 498 and described in Table 434.

Figure 498. RZA: Initial Phase of Vertical Resizing Process for Chrominance (RZA_V_PHS_C) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 434. RZA: Initial Phase of Vertical Resizing Process for Chrominance (RZA_V_PHS_C) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Initial value for the phase value in vertical resizing process for Chrominance (0-10000) Usually this values is zero except in Frame Division Operation - V.

6.4.31 RZA: Vertical Resize Parameter (RZA_V_DIF)

The RZA: Vertical Resize Parameter (RZA_V_DIF) register is shown in Figure 499 and described in Table 435.

Figure 499. RZA: Vertical Resize Parameter (RZA_V_DIF) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-0	R/W-256

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 435. RZA: Vertical Resize Parameter (RZA_V_DIF) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Vertical Resize Parameter The actual resizing ratio is 256/VAL. ***note*** 16 ≤ VAL ≤ 4096 : Normal Mode, 256 ≤ VAL ≤ 4096 : Down Scale Mode

6.4.32 RZA: Interpolation Method for Vertical Rescaling (RZA_V_TYP)

The RZA: Interpolation Method for Vertical Rescaling (RZA_V_TYP) register is shown in Figure 500 and described in Table 436.

Figure 500. RZA: Interpolation Method for Vertical Rescaling (RZA_V_TYP) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	C	Y
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 436. RZA: Interpolation Method for Vertical Rescaling (RZA_V_TYP) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	C		Selection of resizing method for Chrominance in vertical direction
		0	4-tap cubic convolution
		1	2-tap linear interpolation
0	Y		Selection of resizing method for Luminance in vertical direction
		0	4-tap cubic convolution
		1	2-tap linear interpolation

6.4.33 RZA: Vertical LPF Intensity (RZA_V_LPF)

The RZA: Vertical LPF Intensity (RZA_V_LPF) register is shown in Figure 501and described in Table 437.

Figure 501. RZA: Vertical LPF Intensity (RZA_V_LPF) Register

31-16
Reserved
R-0

15-12	11-6	5-0
Reserved	C	Y
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 437. RZA: Vertical LPF Intensity (RZA_V_LPF) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-6	C	0-3Fh	Vertical LPF Intensity for Chrominance (0-32)
5-0	Y	0-3Fh	Vertical LPF Intensity for Luminance (0-32)

6.4.34 RZA: Initial Phase of Horizontal Resizing Process (RZA_H_PHS)

The RZA: Initial Phase of Horizontal Resizing Process (RZA_H_PHS) register is shown in Figure 502 and described in Table 438.

Figure 502. RZA: Initial Phase of Horizontal Resizing Process (RZA_H_PHS) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 438. RZA: Initial Phase of Horizontal Resizing Process (RZA_H_PHS) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Initial value for the phase value in horizontal resizing process (0-8704) Should be set to zero except in Frame Division Mode-H.

6.4.35 RZA: Additional Initial Phase of Vertical Resizing Process for Luminance (RZA_H_PHS_ADJ)

The RZA: Additional Initial Phase of Vertical Resizing Process for Luminance (RZA_H_PHS_ADJ) register is shown in Figure 503 and described in Table 439.

Figure 503. RZA: Additional Initial Phase of Vertical Resizing Process for Luminance (RZA_H_PHS_ADJ) Register

31-16
Reserved
R-0

15-9	8-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 439. RZA: Additional Initial Phase of Vertical Resizing Process for Luminance (RZA_H_PHS_ADJ) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Any writes to these bit(s) must always have a value of 0.
8-0	VAL	0-1FFh	Additional Initial Phase of Horizontal Resizing Process for Luminance This value is added to Horizontal Y phase

6.4.36 RZA: Horizontal Resize Parameter (RZA_H_DIF)

The RZA: Horizontal Resize Parameter (RZA_H_DIF) register is shown in Figure 504 and described in Table 440.

Figure 504. RZA: Horizontal Resize Parameter (RZA_H_DIF) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-0	R/W-256

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 440. RZA: Horizontal Resize Parameter (RZA_H_DIF) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Horizontal Resize Parameter The actual resizing ratio is 256/VAL. 16 ≤ VAL ≤ 4096 : Normal Mode; 256 ≤ VAL ≤ 4096 : Down Scale Mode

6.4.37 RZA: Interpolation Method for Horizontal Rescaling (RZA_H_TYP)

The RZA: Interpolation Method for Horizontal Rescaling (RZA_H_TYP) register is shown in Figure 505 and described in Table 441.

Figure 505. RZA: Interpolation Method for Horizontal Rescaling (RZA_H_TYP) Register

31-16
Reserved

15-2	1	0
Reserved	C	Y
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 441. RZA: Interpolation Method for Horizontal Rescaling (RZA_H_TYP) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	C		Selection of resizing method for Chrominance in horizontal direction
		0	4-tap cubic convolution
		1	2-tap linear interpolation
0	Y		Selection of resizing method for Luminance in horizontal direction
		0	4-tap cubic convolution
		1	2-tap linear interpolation

6.4.38 RZA: Horizontal LPF Intensity (RZA_H_LPF)

The RZA: Horizontal LPF Intensity (RZA_H_LPF) register is shown in Figure 506 and described in Table 442.

Figure 506. RZA: Horizontal LPF Intensity (RZA_H_LPF) Register

31-16
Reserved
R-0

15-12	11-6	5-0
Reserved	C	Y
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 442. RZA: Horizontal LPF Intensity (RZA_H_LPF) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-6	C	0-3Fh	Horizontal LPF Intensity for Chrominance (0-32)
5-0	Y	0-3Fh	Horizontal LPF Intensity for Luminance (0-32)

6.4.39 RZA: Down Scale Mode Enable (RZA_DWN_EN)

The RZA: Down Scale Mode Enable (RZA_DWN_EN) register is shown in Figure 507 and described in Table 443.

Figure 507. RZA: Down Scale Mode Enable (RZA_DWN_EN) Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 443. RZA: Down Scale Mode Enable (RZA_DWN_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		Down Scale Mode Enable
		0	down scale mode off
		1	down scale mode on

6.4.40 RZA: Down Scale Mode Averaging Size (RZA_DWN_AV)

The RZA: Down Scale Mode Averaging Size (RZA_DWN_AV) register is shown in Figure 508 and described in Table 444.

Figure 508. RZA: Down Scale Mode Averaging Size (RZA_DWN_AV) Register

31-16
Reserved
R-0

15-6	5-3	2-0
Reserved	V	H
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 444. RZA: Down Scale Mode Averaging Size (RZA_DWN_AV) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved	0	Any writes to these bit(s) must always have a value of 0.
5-3	V		Down Scale Mode Averaging Size in vertical direction
		0	1/2 down scale
		1h	1/4 down scale
		2h	1/8 down scale
		3h	1/16 down scale
		4h	1/32 down scale
		5h	1/64 down scale
		6h	1/128 down scale
		7h	1/256 down scale
2-0	H		Down Scale Mode Averaging Size in horizontal direction
		0	1/2 down scale
		1h	1/4 down scale
		2h	1/8 down scale
		3h	1/16 down scale
		4h	1/32 down scale
		5h	1/64 down scale
		6h	1/128 down scale
		7h	1/256 down scale

6.4.41 RZA: RGB Output Enable (RZA_RGB_EN)

The RZA: RGB Output Enable (RZA_RGB_EN) register is shown in Figure 509 and described in Table 445.

Figure 509. RZA: RGB Output Enable (RZA_RGB_EN)Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 445. RZA: RGB Output Enable (RZA_RGB_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		RGB Output Enable
		0	YCbCr output
		1	RGB output

6.4.42 RZA: RGB Output Bit Mode (RZA_RGB_TYP)

The RZA: RGB Output Bit Mode (RZA_RGB_TYP) register is shown in Figure 510 and described in Table 446.

Figure 510. RZA: RGB Output Bit Mode (RZA_RGB_TYP) Register

31-16
Reserved
R-0

15-3	2	1	0
Reserved	MSK1	MSK0	TYP
R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 446. RZA: RGB Output Bit Mode (RZA_RGB_TYP) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2	MSK1		Enable masking of the last 2 pixels. This bit is used to mask the 2 pixels at the boundary that are affected by 422 to 444 conversion.
		0	output the last 2 pixels
		1	mask the last 2 pixels (do not output)
1	MSK0		Enable masking of the first 2 pixels. This bit is used to mask the 2 pixels at the boundary that are affected by 422 to 444 conversion.
		0	output the first 2 pixels
		1	mask the first 2 pixels (do not output)
0	TYP		16bit/32bit output selection
		0	32 bit output; alpha + R + G + B (8 bit each)
		1	16 bit output; R (5bit) + G (6bit) + B (5bit)

6.4.43 RZA: YC422 to YC444 Conversion Method (RZA_RGB_BLD)

The RZA: YC422 to YC444 Conversion Method (RZA_RGB_BLD) register is shown in Figure 511 and described in Table 447.

Figure 511. RZA: YC422 to YC444 Conversion Method (RZA_RGB_BLD) Register

31-16	
Reserved	
R-0	
15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 447. RZA: YC422 to YC444 Conversion Method (RZA_RGB_BLD) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	The alpha value used in 32-bit output mode

6.4.44 RZA: SDRAM Base Address MSB (RZA_SDR_Y_BAD_H)

The RZA: SDRAM Base Address MSB (RZA_SDR_Y_BAD_H) register is shown in Figure 512 and described in Table 448.

Figure 512. RZA: SDRAM Base Address MSB (RZA_SDR_Y_BAD_H) Register

31-16
Reserved
R-0
15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 448. RZA: SDRAM Base Address MSB (RZA_SDR_Y_BAD_H) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Base Address. The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.4.45 RZA: SDRAM Base Address LSB (RZA_SDR_Y_BAD_L)

The RZA: SDRAM Base Address LSB (RZA_SDR_Y_BAD_L) register is shown in Figure 513 and described in Table 449.

Figure 513. RZA: SDRAM Base Address LSB (RZA_SDR_Y_BAD_L) Register

31-16
Reserved
R-0
15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 449. RZA: SDRAM Base Address LSB (RZA_SDR_Y_BAD_L) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Base Address. The lower 16 bits of the first address in the allowed memory space in SDRAM. In Resize mode, the lowest 2 bits should be "00" when horizontal reversal mode is off (SEQ[HRV] = NOFLIP). These 2 bits should be "11" when horizontal reversal mode is on (SEQ[HRV] = FLIP). In RGB-32 bit output mode, the lowest 3 bits must be "000".

6.4.46 RZA: SDRAM Start Address MSB (RZA_SDR_Y_SAD_H)

The RZA: SDRAM Start Address MSB (RZA_SDR_Y_SAD_H) register is shown in Figure 514 and described in Table 450.

Figure 514. RZA: SDRAM Start Address MSB (RZA_SDR_Y_SAD_H) Register

31-16
Reserved
R-0
15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 450. RZA: SDRAM Start Address MSB (RZA_SDR_Y_SAD_H) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Start Address. The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.4.47 RZA: SDRAM Start Address LSB (RZA_SDR_Y_SAD_L)

The RZA: SDRAM Start Address LSB (RZA_SDR_Y_SAD_L) register is shown in Figure 515 and described in Table 451.

Figure 515. RZA: SDRAM Start Address LSB (RZA_SDR_Y_SAD_L) Register

31-16
Reserved
R-0
15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 451. RZA: SDRAM Start Address LSB (RZA_SDR_Y_SAD_L) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Start Address. The lower 16 bits of the first address in the allowed memory space in SDRAM. In Resize mode, the lowest 2 bits should be "00" when horizontal reversal mode is off (SEQ[HRV] = NOFLIP). These 2 bits should be "11" when horizontal reversal mode is on (SEQ[HRV] = FLIP). In RGB-32 bit output mode, the lowest 3 bits must be "000".

6.4.48 RZA: SDRAM Line Offset (RZA_SDR_Y_OFT)

The RZA: SDRAM Line Offset (RZA_SDR_Y_OFT) register is shown in Figure 516 and described in Table 452.

Figure 516. RZA: SDRAM Line Offset (RZA_SDR_Y_OFT) Register

31-16
Reserved
R-0

15-0
OFT
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 452. RZA: SDRAM Line Offset (RZA_SDR_Y_OFT) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	OFT	0-FFFFh	The size of the memory space for each line (in bytes). The first address of each output line should be SAD+(line+OFT). Example: line 0: address = SAD + (0*OFT); line 1: address = SAD + (1*OFT); line 2: address = SAD + (2*OFT); line 3: address = SAD + (3*OFT) This register value is neglected in RGB output mode. The lower 5 bits are held low, so this value should be a multiple of 32 bytes.

6.4.49 RZA: Start Line of SDRAM Pointer (RZA_SDR_Y_PTR_S)

The RZA: Start Line of SDRAM Pointer (RZA_SDR_Y_PTR_S) register is shown in Figure 517 and described in Table 453.

Figure 517. RZA: Start Line of SDRAM Pointer (RZA_SDR_Y_PTR_S) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 453. RZA: Start Line of SDRAM Pointer (RZA_SDR_Y_PTR_S) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	The vertical position of the first output line in the output memory space. This value should be 0, when SAD=BAD In RGB output mode, this value should be multiple of 4 (the lowest two bits be "00").

6.4.50 RZA: End Line of SDRAM Pointer (RZA_SDR_Y_PTR_E)

The RZA: End Line of SDRAM Pointer (RZA_SDR_Y_PTR_E) register is shown in Figure 518 and described in Table 454.

Figure 518. RZA: End Line of SDRAM Pointer (RZA_SDR_Y_PTR_E) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-8191

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 454. RZA: End Line of SDRAM Pointer (RZA_SDR_Y_PTR_E) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	SDRAM Available Capacity: The maximum number of lines to be stored in the memory space in Buffer Memory or DRAM. When the number output lines exceeds this value, the address restarts from the first address in the memory space. Example: VAL=0x0003h line 0: address = SAD + (0*OFT) line 1: address = SAD + (1*OFT) line 2: address = SAD + (2*OFT) line 3: address = SAD + (3*OFT) line 4: address = SAD + (0*OFT) ≤ (Returned to the first address) line 5: address = SAD + (1*OFT) line 6: address = SAD + (2*OFT) line 7: address = SAD + (3*OFT) line 8: address = SAD + (0*OFT) ≤ (Returned to the first address) line 9: address = SAD + (1*OFT) line 10: address = SAD + (2*OFT) line 11: address = SAD + (3*OFT). In RGB output mode, this value should be multiple of 4 (the lowest two bits be "00") to ensure that the end of SDRAM region is aligned with line size.

6.4.51 RZA: SDRAM Base Address MSB (for 420 Chroma) (RZA_SDR_C_BAD_H)

The RZA: SDRAM Base Address MSB (for 420 Chroma) (RZA_SDR_C_BAD_H) register is shown in Figure 519 and described in Table 455.

Figure 519. RZA: SDRAM Base Address MSB (for 420 Chroma) (RZA_SDR_C_BAD_H) Register

31-16
Reserved
R-0
15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 455. RZA: SDRAM Base Address MSB (for 420 Chroma) (RZA_SDR_C_BAD_H) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Base Address. The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.4.52 RZA: SDRAM Base Address LSB (for 420 Chroma) (RZA_SDR_C_BAD_L)

The RZA: SDRAM Base Address LSB (for 420 Chroma) (RZA_SDR_C_BAD_L) register is shown in Figure 520 and described in Table 456.

Figure 520. RZA: SDRAM Base Address LSB (for 420 Chroma) (RZA_SDR_C_BAD_L) Register

31-16
Reserved
R-0
15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 456. RZA: SDRAM Base Address LSB (for 420 Chroma) (RZA_SDR_C_BAD_L) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Base Address. The lower 16 bits of the first address in the allowed memory space in SDRAM. In Resize mode, the lowest 2 bits should be "00" when horizontal reversal mode is off (SEQ[HRV] = NOFLIP). These 2 bits should be "11" when horizontal reversal mode is on (SEQ[HRV] = FLIP). In RGB-32bit output mode, the lowest 3 bits must be "000"

6.4.53 RZA: SDRAM Start Address MSB (for 420 Chroma) (RZA_SDR_C_SAD_H)

The RZA: SDRAM Start Address MSB (for 420 Chroma) (RZA_SDR_C_SAD_H) register is shown in Figure 521 and described in Table 457.

Figure 521. RZA: SDRAM Start Address MSB (for 420 Chroma) (RZA_SDR_C_SAD_H) Register

31-16
Reserved
R-0
15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 457. RZA: SDRAM Start Address MSB (for 420 Chroma) (RZA_SDR_C_SAD_H) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Start Address. The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.4.54 RZA: SDRAM Start Address LSB (for 420 Chroma) (RZA_SDR_C_SAD_L)

The RZA: SDRAM Start Address LSB (for 420 Chroma) (RZA_SDR_C_SAD_L) register is shown in Figure 522 and described in Table 458.

Figure 522. RZA: SDRAM Start Address LSB (for 420 Chroma) (RZA_SDR_C_SAD_L) Register

31-16
Reserved
R-0
15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 458. RZA: SDRAM Start Address LSB (for 420 Chroma) (RZA_SDR_C_SAD_L) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Start Address. The lower 16 bits of the first address in the allowed memory space in SDRAM. In Resize mode, the lowest 2 bits should be "00" when horizontal reversal mode is off (SEQ[HRV] = NOFLIP). These 2 bits should be "11" when horizontal reversal mode is on (SEQ[HRV] = FLIP). In RGB-32bit output mode, the lowest 3 bits must be "000"

6.4.55 RZA: SDRAM Line Offset (for 420 Chroma) (RZA_SDR_C_OFT)

The RZA: SDRAM Line Offset (for 420 Chroma) (RZA_SDR_C_OFT) register is shown in Figure 523 and described in Table 459.

Figure 523. RZA: SDRAM Line Offset (for 420 Chroma) (RZA_SDR_C_OFT)Register

31-16
Reserved
R-0

15-0
OFT
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 459. RZA: SDRAM Line Offset (for 420 Chroma) (RZA_SDR_C_OFT) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	OFT	0-FFFFh	The size of the memory space for each line (in bytes). The first address of each output line should be SAD+(line+OFT). Example: line 0: address = SAD + (0*OFT) line 1: address = SAD + (1*OFT) line 2: address = SAD + (2*OFT) line 3: address = SAD + (3*OFT) This register value is neglected in RGB output mode. The lower 5 bits are held low, so this value should be a multiple of 32 bytes.

6.4.56 RZA: Start Line of SDRAM Pointer (for 420 Chroma) (RZA_SDR_C_PTR_S)

RZA: Start Line of SDRAM Pointer (for 420 Chroma) (RZA_SDR_C_PTR_S) register is shown in Figure 524 and described in Table 460.

Figure 524. RZA: Start Line of SDRAM Pointer (for 420 Chroma) (RZA_SDR_C_PTR_S) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 460. RZA: Start Line of SDRAM Pointer (for 420 Chroma) (RZA_SDR_C_PTR_S) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	The vertical position of the first output line in the output memory space. This value should be 0, when SAD=BAD In RGB output mode, this value should be multiple of 4 (the lowest two bits be "00").

6.4.57 RZA: End Line of SDRAM Pointer (for 420 Chroma) (RZA_SDR_C_PTR_E)

The RZA: End Line of SDRAM Pointer (RZA_SDR_C_PTR_E) register is shown in Figure 525 and described in Table 461.

Figure 525. RZA: End Line of SDRAM Pointer (for 420 Chroma) (RZA_SDR_C_PTR_E) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-8191

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 461. RZA: End Line of SDRAM Pointer (for 420 Chroma) (RZA_SDR_C_PTR_E) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	SDRAM Available Capacity: The maximum number of lines to be stored in the memory space in Buffer Memory or DRAM. When the number output lines exceeds this value, the address restarts from the first address in the memory space. Example: VAL=0x0003h line 0: address = SAD + (0*OFT) line 1: address = SAD + (1*OFT) line 2: address = SAD + (2*OFT) line 3: address = SAD + (3*OFT) line 4: address = SAD + (0*OFT) ≤ (Returned to the first address) line 5: address = SAD + (1*OFT) line 6: address = SAD + (2*OFT) line 7: address = SAD + (3*OFT) line 8: address = SAD + (0*OFT) ≤ (Returned to the first address) line 9: address = SAD + (1*OFT) line 10: address = SAD + (2*OFT) line 11: address = SAD + (3*OFT). In RGB output mode, this value should be multiple of 4 (the lowest two bits be "00") to ensure that the end of SDRAM region is aligned with line size.

6.4.58 RZB: Enable (RZB_EN)

The Resizer Channel B (RZB): Enable (RZB_EN) register is shown in Figure 526 and described in Table 462.

Figure 526. RZB: Enable (RZB_EN) Register

31-16
Reserved
R-0

15-1	0
Reserved	EN
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 462. RZB: Enable (RZB_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		Resizer Enable. In one-shot mode, this bit is negated on VD.
		0	disable
		1	enable

6.4.59 RZB: One Shot Mode (RZB_MODE)

The RZB: One Shot Mode (RZB_MODE) register is shown in Figure 527 and described in Table 463.

Figure 527. RZB: One Shot Mode (RZB_MODE) Register

31-16
Reserved
R-0

15-1	0
Reserved	OST
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 463. RZB: One Shot Mode (RZB_MODE) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	OST		One Shot Mode Enable
		0	continuous mode
		1	one shot mode

6.4.60 RZB: 420 Output Format (RZB_420)

The RZB: 420 Output Format (RZB_420) register is shown in Figure 528 and described in Table 464.

Figure 528. RZB: 420 Output Format (RZB_420) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	CEN	YEN
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 464. RZB: 420 Output Format (RZB_420) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	CEN		Output Enable for Chrominance. This bit is valid in 422 input mode. When CEN=0 and YEN=0, output is 422.
		0	C output disable
		1	C output enable and 422 to 420 conversion enabled
0	YEN		Output Enable for Luminance. This bit is valid in 422 input mode. When CEN=0 and YEN=0, output is 422.
		0	Y output disable
		1	Y output enable and 422 to 420 conversion enabled

6.4.61 RZB: Vertical Start Position of the Input (RZB_I_VPS)

The RZB: Vertical Start Position of the Input (RZB_I_VPS) register is shown in Figure 529 and described in Table 465.

Figure 529. RZB: Vertical Start Position of the Input (RZB_I_VPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 465. RZB: Vertical Start Position of the Input (RZB_I_VPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical start position of image processing. After SRC_VPS, the VAL'th line is processed as the first line in each image.

6.4.62 RZB: Horizontal Start Position of the Input (RZB_I_HPS)

The RZB: Horizontal Start Position of the Input (RZB_I_HPS) register is shown in Figure 530 and described in Table 466.

Figure 530. RZB: Horizontal Start Position of the Input (RZB_I_HPS) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 466. RZB: Horizontal Start Position of the Input (RZB_I_HPS) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal start position of image processing. After SRC_HPS, the VAL'th pixel is processed as the first pixel. VAL[0] can not be written.

6.4.63 RZB: Vertical Size of the Output (RZB_O_VSZ)

The RZB: Vertical Size of the Output (RZB_O_VSZ) register is shown in Figure 531 and described in Table 467.

Figure 531. RZB: Vertical Size of the Output (RZB_O_VSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 467. RZB: Vertical Size of the Output (RZB_O_VSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Vertical size of the output image. The number of output lines is (VAL+1).

6.4.64 RZB: Horizontal Size of Output (RZB_O_HSZ)

The RZB: Horizontal Size of Output (RZB_O_HSZ) register is shown in Figure 532 and described in Table 468.

Figure 532. RZB: Horizontal Size of Output (RZB_O_HSZ) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 468. RZB: Horizontal Size of Output (RZB_O_HSZ) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	Horizontal size of output image. The number of pixels in each line is (VAL+1). VAL[0] can not be written. RZB_O_HSZ ≤ 1088 in normal mode RZB_O_HSZ ≤ 544 in down scale mode.

6.4.65 RZB: Initial Phase of Vertical Resizing Process for Luminance (RZB_V_PHS_Y)

The RZB: Initial Phase of Vertical Resizing Process for Luminance (RZB_V_PHS_Y) register is shown in Figure 533 and described in Table 469.

Figure 533. RZB: Initial Phase of Vertical Resizing Process for Luminance (RZB_V_PHS_Y) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 469. RZB: Initial Phase of Vertical Resizing Process for Luminance (RZB_V_PHS_Y) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Initial value for the phase value in vertical resizing process for Luminance (0-10000). Usually, this value is zero except in Frame Division Mode - V.

6.4.66 RZB: Initial Phase of Vertical Resizing Process for Chrominance (RZB_V_PHS_C)

The RZB: Initial Phase of Vertical Resizing Process for Chrominance (RZB_V_PHS_C) register is shown in Figure 534and described in Table 470.

Figure 534. RZB: Initial Phase of Vertical Resizing Process for Chrominance (RZB_V_PHS_C) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 470. RZB: Initial Phase of Vertical Resizing Process for Chrominance (RZB_V_PHS_C) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Initial value for the phase value in vertical resizing process for Chrominance (0-10000). Usually this values is zero except in Frame Division Operation - V.

6.4.67 RZB: Vertical Resize Parameter (RZB_V_DIF)

The RZB: Vertical Resize Parameter (RZB_V_DIF) register is shown in Figure 535and described in Table 471.

Figure 535. RZB: Vertical Resize Parameter (RZB_V_DIF) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-0	R/W-256

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 471. RZB: Vertical Resize Parameter (RZB_V_DIF) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Vertical Resize Parameter. The actual resizing ratio is 256/VAL. 16 ≤ VAL ≤ 4096 : Normal Mode; 256 ≤ VAL ≤ 4096 : Down Scale Mode

6.4.68 RZB: Interpolation Method for Vertical Rescaling (RZB_V_TYP)

The RZB: Interpolation Method for Vertical Rescaling (RZB_V_TYP) register is shown in Figure 536 and described in Table 472.

Figure 536. RZB: Interpolation Method for Vertical Rescaling (RZB_V_TYP) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	C	Y
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 472. RZB: Interpolation Method for Vertical Rescaling (RZB_V_TYP) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	C		Selection of resizing method for Chrominance in vertical direction.
		0	4-tap cubic convolution
		1	2-tap linear interpolation
0	Y		Selection of resizing method for Luminance in vertical direction.
		0	4-tap cubic convolution
		1	2-tap linear interpolation

6.4.69 RZB: Vertical LPF Intensity (RZB_V_LPF)

The RZB: Vertical LPF Intensity (RZB_V_LPF) register is shown in Figure 537 and described in Table 473.

Figure 537. RZB: Vertical LPF Intensity (RZB_V_LPF) Register

31-16
Reserved
R-0

15-12	11-6	5-0
Reserved	C	Y
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 473. RZB: Vertical LPF Intensity (RZB_V_LPF) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-6	C	0-3Fh	Vertical LPF Intensity for Chrominance (0-32)
5-0	Y	0-3Fh	Vertical LPF Intensity for Luminance (0-32)

6.4.70 RZB: Initial Phase of Horizontal Resizing Process (RZB_H_PHS)

The RZB: Initial Phase of Horizontal Resizing Process (RZB_H_PHS) register is shown in Figure 538and described in Table 474.

Figure 538. RZB: Initial Phase of Horizontal Resizing Process (RZB_H_PHS) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 474. RZB: Initial Phase of Horizontal Resizing Process (RZB_H_PHS) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Initial value for the phase value in horizontal resizing process (0-8704). Should be set to zero except in Frame Division Mode-H.

6.4.71 RZB: Additional Initial Phase of Horizontal Resizing Process for Luminance (RZB_H_PHS_ADJ)

The RZB: Additional Initial Phase of Horizontal Resizing Process for Luminance (RZB_H_PHS_ADJ) register is shown in Section 6.4.71 and described in Table 475.

Figure 539. RZB: Additional Initial Phase of Horizontal Resizing Process for Luminance (RZB_H_PHS_ADJ) Register

31-16
Reserved
R-0

15-9	8-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 475. RZB: Additional Initial Phase of Horizontal Resizing Process for Luminance (RZB_H_PHS_ADJ) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
8-0	VAL	0-1FFh	Additional Initial Phase of Horizontal Resizing Process for Luminance. This value is added to Horizontal Y phase.

6.4.72 RZB: Horizontal Resize Parameter (RZB_H_DIF)

The RZB: Horizontal Resize Parameter (RZB_H_DIF) register is shown in Figure 540 and described in Table 476.

Figure 540. RZB: Horizontal Resize Parameter (RZB_H_DIF) Register

31-16
Reserved
R-0

15-14	13-0
Reserved	VAL
R-0	R/W-256

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 476. RZB: Horizontal Resize Parameter (RZB_H_DIF) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	VAL	0-3FFFh	Horizontal Resize Parameter. The actual resizing ratio is 256/VAL. 16 ≤ VAL ≤ 4096 : Normal Mode; 256 ≤ VAL ≤ 4096 : Down Scale Mode

6.4.73 RZB: Interpolation Method for Horizontal Rescaling (RZB_H_TYP)

The RZB: Interpolation Method for Horizontal Rescaling (RZB_H_TYP) register is shown in Figure 541 and described in Table 477.

Figure 541. RZB: Interpolation Method for Horizontal Rescaling (RZB_H_TYP) Register

31-16
Reserved
R-0

15-2	1	0
Reserved	C	Y
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 477. RZB: Interpolation Method for Horizontal Rescaling (RZB_H_TYP) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	C		Selection of resizing method for Chrominance in horizontal direction.
		0	4-tap cubic convolution
		1	2-tap linear interpolation
0	Y		Selection of resizing method for Luminance in horizontal direction.
		0	4-tap cubic convolution
		1	2-tap linear interpolation

6.4.74 RZB: Horizontal LPF Intensity (RZB_H_LPF)

The RZB: Horizontal LPF Intensityy (RZB_H_LPF) register is shown in Figure 542 and described in Table 478.

Figure 542. RZB: Horizontal LPF Intensity (RZB_H_LPF) Register

31-16
Reserved
R-0

15-12	11-6	5-0
Reserved	C	Y
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 478. RZB: Horizontal LPF Intensity (RZB_H_LPF) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-6	C	0-3Fh	Horizontal LPF Intensity for Chrominance (0-32)
5-0	Y	0-3Fh	Horizontal LPF Intensity for Luminance (0-32)

6.4.75 RZB: Down Scale Mode Enable (RZB_DWN_EN)

The RZB: Down Scale Mode Enable (RZB_DWN_EN) register is shown in Figure 543 and described in Table 479.

Figure 543. RZB: Down Scale Mode Enable (RZB_DWN_EN) Register

31-16	
Reserved	
R-0	
15-1	**0**
Reserved	EN
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 479. RZB: Down Scale Mode Enable (RZB_DWN_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved		Any writes to these bit(s) must always have a value of 0.
0	EN		Down Scale Mode Enable
		0	down scale mode off
		1	down scale mode on

6.4.76 RZB: Down Scale Mode Averaging Size (RZB_DWN_AV)

The RZB: Down Scale Mode Averaging Size (RZB_DWN_AV) register is shown in Figure 544 and described in Table 480.

Figure 544. RZB: Down Scale Mode Averaging Size (RZB_DWN_AV) Register

31-16
Reserved
R-0

15-6	5-3	2-0
Reserved	V	H
R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 480. RZB: Down Scale Mode Averaging Size (RZB_DWN_AV) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved	0	Any writes to these bit(s) must always have a value of 0.
5-3	V		Down Scale Mode Averaging Size in Horizontal direction. If RZB_DWN_AV[H]=0, RZB_DWN_AV[V] must be either 0, 1, or 2.
		0	1/2 down scale
		1h	1/4 down scale
		2h	1/8 down scale
		3h	1/16 down scale
		4h	1/32 down scale
		5h	1/64 down scale
		6h	1/128 down scale
		7h	1/256 down scale
2-0	H		Down Scale Mode Averaging Size in horizontal direction.
		0	1/2 down scale
		1h	1/4 down scale
		2h	1/8 down scale
		3h	1/16 down scale
		4h	1/32 down scale
		5h	1/64 down scale
		6h	1/128 down scale
		7h	1/256 down scale

6.4.77 RZB: RGB Output Enable (RZB_RGB_EN)

The RZB: RGB Output Enable (RZB_RGB_EN) register is shown in Figure 545 and described in Table 481.

Figure 545. RZB: RGB Output Enable (RZB_RGB_EN) Register

31-16	
Reserved	
R-0	
15-1	**0**
Reserved	EN
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 481. RZB: RGB Output Enable (RZB_RGB_EN) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Any writes to these bit(s) must always have a value of 0.
0	EN		RGB Output Enable
		0	YCbCr output
		1	RGB output

6.4.78 RZB: RGB Output Bit Mode (RZB_RGB_TYP)

The RZB: RGB Output Bit Mode (RZB_RGB_TYP) register is shown in Figure 546 and described in Table 482.

Figure 546. RZB: RGB Output Bit Mode (RZB_RGB_TYP) Register

31-16
Reserved
R-0

15-3	2	1	0
Reserved	MSK1	MSK0	TYP
R-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 482. RZB: RGB Output Bit Mode (RZB_RGB_TYP) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Any writes to these bit(s) must always have a value of 0.
2	MSK1		Enable masking of the last 2 pixels. This bit is used to mask the 2 pixels at the boundary that are affected by 422 to 444 conversion.
		0	output the last 2 pixels
		1	mask the last 2 pixels (do not output)
1	MSK0		Enable masking of the first 2 pixels. This bit is used to mask the 2 pixels at the boundary that are affected by 422 to 444 conversion.
		0	output the first 2 pixels
		1	mask the first 2 pixels (do not output)
0	TYP		16bit/32bit output selection
		0	32 bit output; alpha + R + G + B (8 bit each)
		1	16 bit output; R(5bit) + G(6bit) + B(5bit)

6.4.79 RZB: YC422 to YC444 Conversion Method (RZB_RGB_BLD)

The RZB: YC422 to YC444 Conversion Method (RZB_RGB_BLD) register is shown in Figure 547 and described in Table 483.

Figure 547. RZB: YC422 to YC444 Conversion Method (RZB_RGB_BLD) Register

31-16
Reserved
R-0

15-8	7-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 483. RZB: YC422 to YC444 Conversion Method (RZB_RGB_BLD) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VAL	0-FFh	The alpha value used in 32-bit output mode

6.4.80 RZB: SDRAM Base Address MSB (RZB_SDR_Y_BAD_H)

The RZB: SDRAM Base Address MSB (RZB_SDR_Y_BAD_H) register is shown in Figure 548 and described in Table 484.

Figure 548. RZB: SDRAM Base Address MSB (RZB_SDR_Y_BAD_H) Register

31-16
Reserved
R-0
15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 484. RZB: SDRAM Base Address MSB (RZB_SDR_Y_BAD_H) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Base Address. The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.4.81 RZB: SDRAM Base Address LSB (RZB_SDR_Y_BAD_L)

The RZB: SDRAM Base Address LSB (RZB_SDR_Y_BAD_L) register is shown in Figure 549 and described in Table 485.

Figure 549. RZB: SDRAM Base Address LSB (RZB_SDR_Y_BAD_L) Register

31-16
Reserved
R-0
15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 485. RZB: SDRAM Base Address LSB (RZB_SDR_Y_BAD_L) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Base Address. The lower 16 bits of the first address in the allowed memory space in SDRAM. In Resize mode, the lowest 2 bits should be "00" when horizontal reversal mode is off (SEQ[HRV] = NOFLIP). These 2 bits should be "11" when horizontal reversal mode is on (SEQ[HRV] = FLIP). In RGB-32 bit output mode, the lowest 3 bits must be "000".

6.4.82 RZB: SDRAM Start Address MSB (RZB_SDR_Y_SAD_H)

The RZB: SDRAM Start Address MSB (RZB_SDR_Y_SAD_H) register is shown in Figure 550 and described in Table 486.

Figure 550. RZB: SDRAM Start Address MSB (RZB_SDR_Y_SAD_H) Register

31-16
Reserved
R-0
15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 486. RZB: SDRAM Start Address MSB (RZB_SDR_Y_SAD_H) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Start Address. The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.4.83 RZB: SDRAM Start Address LSB (RZB_SDR_Y_SAD_L)

The RZB: SDRAM Start Address LSB (RZB_SDR_Y_SAD_L) register is shown in Figure 551 and described in Table 487.

Figure 551. RZB: SDRAM Start Address LSB (RZB_SDR_Y_SAD_L) Register

31-16
Reserved
R-0
15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 487. RZB: SDRAM Start Address LSB (RZB_SDR_Y_SAD_L) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Start Address. The lower 16 bits of the first address in the allowed memory space in SDRAM. In Resize mode, the lowest 2 bits should be "00" when horizontal reversal mode is off (SEQ[HRV] = NOFLIP). These 2 bits should be "11" when horizontal reversal mode is on (SEQ[HRV] = FLIP). In RGB-32 bit output mode, the lowest 3 bits must be "000".

6.4.84 RZB: SDRAM Line Offset (RZB_SDR_Y_OFT)

The RZB: SDRAM Line Offset (RZB_SDR_Y_OFT) register is shown in Figure 552 and described in Table 488.

Figure 552. RZB: SDRAM Line Offset (RZB_SDR_Y_OFT) Register

31-16
Reserved
R-0
15-0
OFT
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 488. RZB: SDRAM Line Offset (RZB_SDR_Y_OFT) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	OFT	0-FFFFh	The size of the memory space for each line (in bytes). The first address of each output line should be SAD+(line+OFT). Example: line 0: address = SAD + (0*OFT) line 1: address = SAD + (1*OFT) line 2: address = SAD + (2*OFT) line 3: address = SAD + (3*OFT). This register value is neglected in RGB output mode. The lower 5 bits are held low, so this value should be a multiple of 32 bytes.

6.4.85 RZB: Start Line of SDRAM Pointer (RZB_SDR_Y_PTR_S)

The RZB: Start Line of SDRAM Pointer (RZB_SDR_Y_PTR_S) register is shown in Figure 553 and described in Table 489.

Figure 553. RZB: Start Line of SDRAM Pointer (RZB_SDR_Y_PTR_S) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 489. RZB: Start Line of SDRAM Pointer (RZB_SDR_Y_PTR_S) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	The vertical position of the first output line in the output memory space. This value should be 0, when SAD=BAD In RGB output mode, this value should be multiple of 4 (the lowest two bits be "00").

6.4.86 RZB: End Line of SDRAM Pointer (RZB_SDR_Y_PTR_E)

The RZB: End Line of SDRAM Pointer (RZB_SDR_Y_PTR_E) register is shown in Figure 554 and described in Table 490.

Figure 554. RZB: End Line of SDRAM Pointer (RZB_SDR_Y_PTR_E) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-8191

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 490. RZB: End Line of SDRAM Pointer (RZB_SDR_Y_PTR_E) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	SDRAM Available Capacity: The maximum number of lines to be stored in the memory space in Buffer Memory or DRAM. When the number output lines exceeds this value, the address restarts from the first address in the memory space. Example: VAL=0x0003h line 0: address = SAD + (0*OFT) line 1: address = SAD + (1*OFT) line 2: address = SAD + (2*OFT) line 3: address = SAD + (3*OFT) line 4: address = SAD + (0*OFT) ≤ (Returned to the first address) line 5: address = SAD + (1*OFT) line 6: address = SAD + (2*OFT) line 7: address = SAD + (3*OFT) line 8: address = SAD + (0*OFT) ≤ (Returned to the first address) line 9: address = SAD + (1*OFT) line 10: address = SAD + (2*OFT) line 11: address = SAD + (3*OFT). In RGB output mode, this value should be multiple of 4 (the lowest two bits be "00") to ensure that the end of SDRAM region is aligned with line size.

6.4.87 RZB: SDRAM Base Address MSB (for 420 Chroma) (RZB_SDR_C_BAD_H)

The RZB: SDRAM Base Address MSB (for 420 Chroma) (RZB_SDR_C_BAD_H) register is shown in Figure 555 and described in Table 491.

Figure 555. RZB: SDRAM Base Address MSB (for 420 Chroma) (RZB_SDR_C_BAD_H) Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 491. RZB: SDRAM Base Address MSB (for 420 Chroma) (RZB_SDR_C_BAD_H) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Base Address. The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.4.88 RZB: SDRAM Base Address LSB (for 420 Chroma) (RZB_SDR_C_BAD_L)

The RZB: SDRAM Base Address LSB (for 420 Chroma) (RZB_SDR_C_BAD_L) register is shown in Figure 556 and described in Table 492.

Figure 556. RZB: SDRAM Base Address LSB (for 420 Chroma) (RZB_SDR_C_BAD_L) Register

31-16
Reserved
R-0

15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 492. RZB: SDRAM Base Address LSB (for 420 Chroma) (RZB_SDR_C_BAD_L) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Base Address. The lower 16 bits of the first address in the allowed memory space in SDRAM. In Resize mode, the lowest 2 bits should be "00" when horizontal reversal mode is off (SEQ[HRV] = NOFLIP). These 2 bits should be "11" when horizontal reversal mode is on (SEQ[HRV] = FLIP). In RGB-32bit output mode, the lowest 3 bits must be "000".

6.4.89 RZB: SDRAM Start Address MSB (for 420 Chroma) (RZB_SDR_C_SAD_H)

The RZB: SDRAM Start Address MSB (for 420 Chroma) (RZB_SDR_C_SAD_H) register is shown in Figure 557 and described in Table 493.

Figure 557. RZB: SDRAM Start Address MSB (for 420 Chroma) (RZB_SDR_C_SAD_H) Register

31-16
Reserved
R-0
15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 493. RZB: SDRAM Start Address MSB (for 420 Chroma) (RZB_SDR_C_SAD_H) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Start Address. The upper 16 bits of the first address in the allowed memory space in SDRAM.

6.4.90 RZB: SDRAM Start Address LSB (for 420 Chroma) (RZB_SDR_C_SAD_L)

The RZB: SDRAM Start Address LSB (for 420 Chroma) (RZB_SDR_C_SAD_L) register is shown in Figure 558 and described in Table 494.

Figure 558. RZB: SDRAM Start Address LSB (for 420 Chroma) (RZB_SDR_C_SAD_L) Register

31-16
Reserved
R-0
15-0
VAL
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 494. RZB: SDRAM Start Address LSB (for 420 Chroma) (RZB_SDR_C_SAD_L) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	VAL	0-FFFFh	SDRAM Start Address. The lower 16 bits of the first address in the allowed memory space in SDRAM. In Resize mode, the lowest 2 bits should be "00" when horizontal reversal mode is off (SEQ[HRV] = NOFLIP). These 2 bits should be "11" when horizontal reversal mode is on (SEQ[HRV] = FLIP). In RGB-32bit output mode, the lowest 3 bits must be "000".

6.4.91 RZB: SDRAM Line Offset (for 420 Chroma) (RZB_SDR_C_OFT)

The RZB: SDRAM Line Offset (for 420 Chroma) (RZB_SDR_C_OFT) register is shown in Figure 559 and described in Table 495.

Figure 559. RZB: SDRAM Line Offset (for 420 Chroma) (RZB_SDR_C_OFT) Register

31-16
Reserved
R-0
15-0
OFT
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 495. RZB: SDRAM Line Offset (for 420 Chroma) (RZB_SDR_C_OFT) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	OFT	0-FFFFh	The size of the memory space for each line (in bytes). The first address of each output line should be SAD+(line+OFT). Example: line 0: address = SAD + (0*OFT) line 1: address = SAD + (1*OFT) line 2: address = SAD + (2*OFT) line 3: address = SAD + (3*OFT). This register value is neglected in RGB output mode. The lower 5 bits are held low, so this value should be a multiple of 32 bytes.

6.4.92 RZB: Start Line of SDRAM Pointer (for 420 Chroma) (RZB_SDR_C_PTR_S)

The RZB: Start Line of SDRAM Pointer (for 420 Chroma) (RZB_SDR_C_PTR_S) register is shown in Figure 560 and described in Table 496.

Figure 560. RZB: Start Line of SDRAM Pointer (for 420 Chroma) (RZB_SDR_C_PTR_S) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 496. RZB: Start Line of SDRAM Pointer (for 420 Chroma) (RZB_SDR_C_PTR_S) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-0	VAL	0-1FFFh	The vertical position of the first output line in the output memory space. This value should be 0, when SAD=BAD In RGB output mode, this value should be multiple of 4 (the lowest two bits be "00").

6.4.93 RZB: End Line of SDRAM Pointer (for 420 Chroma) (RZB_SDR_C_PTR_E)

The RZB: End Line of SDRAM Pointer (for 420 Chroma) (RZB_SDR_C_PTR_E) register is shown in Figure 561and described in Table 497.

Figure 561. RZB: End Line of SDRAM Pointer (for 420 Chroma) (RZB_SDR_C_PTR_E) Register

31-16
Reserved
R-0

15-13	12-0
Reserved	VAL
R-0	R/W-8191

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 497. RZB: End Line of SDRAM Pointer (for 420 Chroma) (RZB_SDR_C_PTR_E) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.

12-0	VAL	0-1FFFh	SDRAM Available Capacity: The maximum number of lines to be stored in the memory space in Buffer Memory or DRAM. When the number output lines exceeds this value, the address restarts from the first address in the memory space. Example: VAL=0x0003h
			line 0: address = SAD + (0*OFT); line 1: address = SAD + (1*OFT);
			line 2: address = SAD + (2*OFT); line 3: address = SAD + (3*OFT);
			line 4: address = SAD + (0*OFT) ≤ (Returned to the first address);
			line 5: address = SAD + (1*OFT); line 6: address = SAD + (2*OFT);
			line 7: address = SAD + (3*OFT);
			line 8: address = SAD + (0*OFT) ≤ (Returned to the first address);
			line 9: address = SAD + (1*OFT); line 10: address = SAD + (2*OFT);
			line 11: address = SAD + (3*OFT)
			In RGB output mode, this value should be multiple of 4 (the lowest two bits be "00") to ensure that the end of SDRAM region is aligned with line size.

6.5 Hardware 3A (H3A) Registers

Table 498 lists the memory-mapped registers for the Hardware 3A Statistics Generation (AE, AF, AWB) (H3A). See the device-specific data manual for the memory address of these registers.

Table 498. Hardware 3A Statistics Generation (AE, AF, AWB) (H3A) Registers

Offset	Acronym	Register Description	Section
0h	PID	Peripheral Revision and Class Information	Section 6.5.1
04h	PCR	Peripheral Control Register	Section 6.5.2
08h	AFPAX1	Setup for the AF Engine Paxel Configuration	Section 6.5.3
0Ch	AFPAX2	Setup for the AF Engine Paxel Configuration	Section 6.5.4
10h	AFPAXSTART	Start Position for AF Engine Paxels	Section 6.5.5
14h	AFIIRSH	Start Position for IIRSH	Section 6.5.6
18h	AFBUFST	SDRAM/DDRAM Start Address for AF Engine	Section 6.5.7
1Ch	AFCOEF010	IIR filter coefficient data for SET 0	Section 6.5.8
20h	AFCOEF032	IIR filter coefficient data for SET 0	Section 6.5.9
24h	AFCOEFF054	IIR filter coefficient data for SET 0	Section 6.5.10
28h	AFCOEFF076	IIR filter coefficient data for SET 0	Section 6.5.11
2Ch	AFCOEFF098	IIR filter coefficient data for SET 0	Section 6.5.12
30h	AFCOEFF0010	IIR filter coefficient data for SET 0	Section 6.5.13
34h	AFCOEF110	IIR filter coefficient data for SET 1	Section 6.5.14
38h	AFCOEF132	IIR filter coefficient data for SET 1	Section 6.5.15
3Ch	AFCOEFF154	IIR filter coefficient data for SET 1	Section 6.5.16
40h	AFCOEFF176	IIR filter coefficient data for SET 1	Section 6.5.17
44h	AFCOEFF198	IIR filter coefficient data for SET 1	Section 6.5.18
48h	AFCOEFF1010	IIR filter coefficient data for SET 1	Section 6.5.19
4Ch	AEWWIN1	Configuration for AE/AWB Windows	Section 6.5.20
50h	AEWINSTART	Start Position for AE/AWB Windows	Section 6.5.21
54h	AEWINBLK	Start Position and Height for Black Line of AE/AWB Windows	Section 6.5.22
58h	AEWSUBWIN	Configuration for Subsample data in AE/AWB Window	Section 6.5.23
5Ch	AEWBUFST	SDRAM/DDRAM Start Address for AE/AWB Engine Output Data	Section 6.5.24
60h	RSDR_ADDR	AE/AWB Engine Configuration	Section 6.5.25
64h	LINE_START	Line Start Position for ISIF Interface	Section 6.5.26
68h	VFV_CFG1	AF Vertical Focus Configuration 1 Register	Section 6.5.27
6Ch	VFV_CFG2	AF Vertical Focus Configuration 2 Register	Section 6.5.28
70h	VFV_CFG3	AF Vertical Focus Configuration 3 Register	Section 6.5.29
74h	VFV_CFG4	AF Vertical Focus Configuration 4 Register	Section 6.5.30
78h	HFV_THR	Configures the Horizontal Thresholds for the AF IIR filters	Section 6.5.31

6.5.1 Peripheral Revision and Class Information (PID)

The Peripheral Revision and Class Information (PID) register is shown in Figure 562 and described in Table 499.

Figure 562. Peripheral Revision and Class Information (PID) Register

31-30	29-28	27-16
SCHEME	Reserved	FUNC
R-1	R-0	R-3329

15-11	10-8	7-0
RTL	MAJOR	MINOR
R-0	R-0	R-0

LEGEND: R = Read only; -*n* = value after reset

Table 499. Peripheral Revision and Class Information (PID) Field Descriptions

Bit	Field	Value	Description
31-30	SCHEME	0-3h	Scheme used is PDR3.5
29-28	Reserved	0-3h	Any writes to these bit(s) must always have a value of 0.
27-16	FUNC	0-FFFh	Function h3A (AF, AE, and AWB)
15-11	RTL	0-1Fh	RTL Revision
10-8	MAJOR	0-7h	Major Version
7-6	Reserved	0-3h	Any writes to these bit(s) must always have a value of 0.
7-0	MINOR	0-FFh	Peripheral Revision Number Initial Revision

6.5.2 Peripheral Control Register (PCR)

The Peripheral Control (PCR) register is shown in Figure 563 and described in Table 500.

Figure 563. Peripheral Control Register (PCR)

31-24						
AVE2LMT						
R/W-1023						
23-22	21	20	19	18	17	16
AVE2LMT	Reserved	AF_VF_EN	AEW_MED_EN	BUSYAEAWB	AEW_ALAW_EN	AEW_EN
R/W-1023	R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0

15	14	13-11	10-8
BUSYAF	FVMODE	RGBPOS	MED_TH
R-0	R/W-0	R/W-0	R/W-255

7-3	2	1	0
MED_TH	AF_MED_EN	AF_ALAW_EN	AF_EN
R/W-255	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after resetR/W-0

Table 500. Peripheral Control Register (PCR) Field Descriptions

Bit	Field	Value	Description
31-22	AVE2LMT	0-3FFh	AE/AWB Saturation Limit. This is the value that all sub sampled pixels in the AE/AWB engine are compared to. If the data is greater or equal to this data then the block is considered saturated.
21	Reserved	0	Any writes to these bit(s) must always have a value of 0.
20	AF_VF_EN		AF Vertical Focus Enable
		0	4 Color Horizontal Only FV operation
		1	1 Color Horizontal and Vertical FV operation
19	AEW_MED_EN		AE/AWB Median filter Enable. If the median filter is enabled, then the 1st 2 and last 2 pixels in the frame are not filtered.
		0	Disable AE/AWB median filter
		1	Enable AE/AWB median filter
18	BUSYAEAWB		Busy bit for AE/AWB
17	AEW_ALAW_EN		AE/AWB A-law Enable
		0	Disable AE/AWB A-law table
		1	Enable AE/AWB A-law table
16	AEW_EN		AE/AWB Enable
		0	Disable AE/AWB Engine
		1	Enable AE/AWB Engine
15	BUSYAF		Busy bit for AF
14	FVMODE		Focus Value Accumulation Mode
		0	Sum Mode
		1	Peak Mode
13-11	RGBPOS		Red, Green, and Blue pixel location in the AF windows.
		0	GR and GB as Bayer pattern
		1h	RG and GB as Bayer pattern
		2h	GR and BG as Bayer pattern
		3h	RG and BG as Bayer pattern
		4h	GG and RB as custom pattern
		5h	RB and GG as custom pattern
		6h-7h	Reserved

Table 500. Peripheral Control Register (PCR) Field Descriptions (continued)

Bit	Field	Value	Description
10-3	MED_TH	0-FFh	Median filter threshold
2	AF_MED_EN		Auto Focus Median filter Enable. If the median filter is enabled, then the 1st 2 and last 2 pixels in the frame are not filtered.
		0	Disable Auto Focus median filter
		1	Enable Auto Focus median filter
1	AF_ALAW_EN		Auto Focus A-law table Enable
		0	Disable Auto Focus A-law table
		1	Enable Auto Focus A-law table
0	AF_EN		Auto Focus Enable
		0	Disable Auto Focus Engine
		1	Enable Auto Focus Engine

6.5.3 Setup for the AF Engine Paxel Configuration (AFPAX1)

The Setup for the AF Engine Paxel Configuration (AFPAX1) register is shown in Figure 564 and described in Table 501.

Figure 564. Setup for the AF Engine Paxel Configuration (AFPAX1) Register

31-24	23-16
Reserved	PAXW
R-0	R/W-0
15-8	7-0
Reserved	PAXH
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 501. Setup for the AF Engine Paxel Configuration (AFPAX1) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Any writes to these bit(s) must always have a value of 0.
23-16	PAXW	0-FFh	AF Engine Paxel Width. The width of the paxel is the value of this register plus 1 multiplied by 2. The minimum width is expected to be 8 pixels.
15-8	Reserved	0-FFh	Any writes to these bit(s) must always have a value of 0.
7-0	PAXH	0-FFh	AF Engine Paxel Height. The height of the paxel is the value of this register plus 1 multiplied by 2 with a final value of 2-256 (even).

6.5.4 Setup for the AF Engine Paxel Configuration (AFPAX2)

The Setup for the AF Engine Paxel Configuration (AFPAX2) register is shown in Figure 565 and described in Table 502.

Figure 565. Setup for the AF Engine Paxel Configuration (AFPAX2) Register

31-21	20-17	16
Reserved	AFINCH	AFINCV
R-0	R/W-0	R/W-0

15-13	12-6	5-0
AFINCV	PAXVC	PAXHC
R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 502. Setup for the AF Engine Paxel Configuration (AFPAX2) Field Descriptions

Bit	Field	Value	Description
31-21	Reserved	0	Any writes to these bit(s) must always have a value of 0.
20-17	AFINCH	0-Fh	AF Engine Column Increments Number of columns to increment in a Paxel plus 1 multiplied by 2. Thus, the number of columns that can be skipped between two processed line pairs is 0-30 (even). The starting two columns in a paxel are first processed before this field is applied. This must be set so that there are at least 4 samples on a line when combined with the number of horizontal paxels. This registered is shadowed and latched on the rising edge of VSYNC
16-13	AFINCV	0-Fh	AF Engine Line Increments Number of lines to increment in a Paxel plus 1 multiplied by 2. Incrementing the line in a paxel is always done on a line pair due to the fact that the RGB pattern falls in two lines. If all the lines are to be processed, this field should be set to zero, and thus line count is incremented by 2 following a line pair. Thus, the number of lines that can be skipped between two processed line pairs is 0-30 (even). The starting two lines in a paxel are first processed before this field is applied.
12-6	PAXVC	0-7Fh	AF Engine Vertical Paxel Count The number of paxels in the vertical direction plus 1. The maximum number of vertical paxels in a frame should not exceed 128. The value should be set to ensure that the bandwidth requirements and buffer size are not exceeded.
5-0	PAXHC	0-3Fh	AF Engine Horizontal Paxel Count The number of paxels in the horizontal direction plus 1. It is illegal to set a number that is greater than 35 (total of 36 paxels in the horizontal direction).

6.5.5 Start Position for AF Engine Paxels (AFPAXSTART)

The Start Position for AF Engine Paxels (AFPAXSTART) register is shown in Figure 566 and described in Table 503.

Figure 566. Start Position for AF Engine Paxels (AFPAXSTART) Register

31-28	27-16
Reserved	PAXSH
R-0	R/W-0
15-12	**11-0**
Reserved	PAXSV
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 503. Start Position for AF Engine Paxels (AFPAXSTART) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Any writes to these bit(s) must always have a value of 0.
27-16	PAXSH	0-FFFh	AF Engine Paxel Horizontal Start Position. Range: 2-4094. PAXSH must be equal to or greater than (IIRSH + 2) This value must be even.
15-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	PAXSV	0-FFFh	AF Engine Paxel Vertical Start Position. Range: 0-4095. Sets the vertical line for the first paxel.

6.5.6 IIRSH Start Position (AFIIRSH)

The IIRSH start position (AFIIRSH) register is shown in Figure 567 and described in Table 504.

Figure 567. IIRSH Start Position (AFIIRSH) Register

31-16
Reserved
R-00

15-12	11-0
Reserved	IIRSH
R-00	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 504. IIRSH Start Position (AFIIRSH) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	IIRSH	0-FFFh	AF Engine IIR Horizontal Start Position. Range from 0-4094. When the horizontal position of a line equals this value the shift registers are cleared on the next pixel. This value must be even.

6.5.7 SDRAM/DDRAM Start address for AF Engine (AFBUFST)

The SDRAM/DDRAM Start address for AF Engine (AFBUFST) is shown in Figure 568 and described in Table 505.

Figure 568. SDRAM/DDRAM Start Address for AF Engine (AFBUFST) Register

31-16
AFBUFST
R/W-0
15-0
AFBUFST
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 505. SDRAM/DDRAM Start Address for AF Engine (AFBUFST) Field Descriptions

Bit	Field	Value	Description
31-0	AFBUFST	0-FFFF FFFFh	AF Engine SDRAM/DDRAM Start Address. The starting location in the SDRAM/DDRAM. The 6 LSB are ignored, address should be on a 64-byte boundary. This field can be altered even when the AF is busy. Change will take place only for the next frame. However, note that reading this register will always give the latest value..

6.5.8 IIR Filter Coefficient Data for SET 0 (AFCOEF010)

The IIR filter coefficient data for SET 0 (AFCOEF010) register is shown in Figure 569and described in Table 506.

Figure 569. IIR Filter Coefficient Data for SET 0 (AFCOEF010) Register

31-28	27-16
Reserved	COEFF1
R-00	R/W-0
15-12	11-0
Reserved	COEFF0
R-00	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 506. IIR Filter Coefficient Data for SET 0 (AFCOEF010) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Any writes to these bit(s) must always have a value of 0.
27-16	COEFF1	0-FFFh	AF Engine IIR filter Coefficient #1 (Set 0). The range is signed -32 ≤ value ≤ 31 +63/64.
15-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	COEFF0	0-FFFh	AF Engine IIR filter Coefficient #0 (Set 0). The range is signed -32 ≤ value ≤ 31 +63/64.

6.5.9 IIR Filter Coefficient Data for SET 0 (AFCOEF032)

The IIR filter coefficient data for SET 0 (AFCOEF032) register is shown in Figure 570 and described in Table 507.

Figure 570. IIR Filter Coefficient Data for SET 0 (AFCOEF032)

31-28	27-16
Reserved	COEFF3
R-00	R/W-0
15-12	11-0
Reserved	COEFF2
R-00	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 507. IIR Filter Coefficient Data for SET 0 (AFCOEF032) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Any writes to these bit(s) must always have a value of 0.
27-16	COEFF3	0-FFFh	AF Engine IIR filter Coefficient #3 (Set 0). The range is signed -32 ≤ value ≤ 31 +63/64.
15-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	COEFF2	0-FFFh	AF Engine IIR filter Coefficient #2 (Set 0). The range is signed -32 ≤ value ≤ 31 +63/64.

6.5.10 IIR Filter Coefficient Data for SET 0 (AFCOEFF054)

The IIR filter coefficient data for SET 0 (AFCOEFF054) is shown in Figure 571 and described in Table 508.

Figure 571. IIR Filter Coefficient data for SET 0 (AFCOEFF054)

31-28	27-16
Reserved	COEFF5
R-00	R/W-0
15-12	11-0
Reserved	COEFF4
R-00	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 508. IIR Filter Coefficient Data for SET 0 (AFCOEFF054) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Any writes to these bit(s) must always have a value of 0.
27-16	COEFF5	0-FFFh	AF Engine IIR filter Coefficient #5 (Set 0). The range is signed -32 ≤ value ≤ 31 +63/64.
15-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	COEFF4	0-FFFh	AF Engine IIR filter Coefficient #4 (Set 0). The range is signed -32 ≤ value ≤ 31 +63/64.

6.5.11 IIR Filter Coefficient Data for SET 0 (AFCOEFF076)

The IIR filter coefficient data for SET 0 (AFCOEFF076) register is shown in Figure 572 and described in Table 509.

Figure 572. IIR Filter Coefficient Data for SET 0 (AFCOEFF076) Register

31-28	27-16
Reserved	COEFF7
R-00	R/W-0
15-12	**11-0**
Reserved	COEFF6
R-00	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 509. IIR Filter Coefficient Data for SET 0 (AFCOEFF076) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Any writes to these bit(s) must always have a value of 0.
27-16	COEFF7	0-FFFh	AF Engine IIR filter Coefficient #7 (Set 0). The range is signed -32 ≤ value ≤ 31 +63/64.
15-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	COEFF6	0-FFFh	AF Engine IIR filter Coefficient #6 (Set 0). The range is signed -32 ≤ value ≤ 31 +63/64.

6.5.12 IIR fFlter Coefficient Data for SET 0 (AFCOEFF098)

The IIR filter coefficient data for SET 0 (AFCOEFF098) register is shown in Figure 573 and described in Table 510.

Figure 573. IIR Filter Coefficient Data for SET 0 (AFCOEFF098) Register

31-28	27-16
Reserved	COEFF9
R-00	R/W-0
15-12	11-0
Reserved	COEFF8
R-00	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 510. IIR Filter Coefficient Data for SET 0 (AFCOEFF098) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Any writes to these bit(s) must always have a value of 0.
27-16	COEFF9	0-FFFh	AF Engine IIR filter Coefficient #9 (Set 0). The range is signed -32 ≤ value ≤ 31 +63/64.
15-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	COEFF8	0-FFFh	AF Engine IIR filter Coefficient #8 (Set 0). The range is signed -32 ≤ value ≤ 31 +63/64.

6.5.13 IIR Filter Coefficient Data for SET 0 (AFCOEFF0010)

The IIR filter coefficient data for SET 0 (AFCOEFF0010) register is shown in Figure 574 and described in Table 511.

Figure 574. IIR Filter Coefficient Data for SET 0 (AFCOEFF0010) Register

31-16
Reserved
R-00

15-12	11-0
Reserved	COEFF10
R-00	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 511. IIR Filter Coefficient Data for SET 0 (AFCOEFF0010) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	COEFF10	0-FFFh	AF Engine IIR filter Coefficient #10 (Set 0). The range is signed -32 ≤ value ≤ 31 +63/64.

6.5.14 IIR Filter Coefficient Data for SET 1 (AFCOEF110)

The IIR filter coefficient data for SET 1 (AFCOEF110) register is shown in Figure 575 and described in Table 512.

Figure 575. IIR Filter Coefficient Data for SET 1 (AFCOEF110) Register

31-28	27-16
Reserved	COEFF1
R-00	R/W-0
15-12	**11-0**
Reserved	COEFF0
R-00	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 512. IIR Filter coefficient data for SET 1 (AFCOEF110) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Any writes to these bit(s) must always have a value of 0.
27-16	COEFF1	0-FFFh	AF Engine IIR filter Coefficient #1 (Set 1). The range is signed -32 ≤ value ≤ 31 +63/64.
15-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	COEFF0	0-FFFh	AF Engine IIR filter Coefficient #0 (Set 1). The range is signed -32 ≤ value ≤ 31 +63/64.

6.5.15 IIR Filter Coefficient Data for SET 1 (AFCOEF132)

The IIR filter coefficient data for SET 1 (AFCOEF132) register is shown in Figure 576 and described in Table 513.

Figure 576. AFCOEF132 - IIR Filter Coefficient Data for SET 1 (AFCOEF132)

31-28	27-16
Reserved	COEFF3
R-00	R/W-0
15-12	11-0
Reserved	COEFF2
R-00	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 513. AFCOEF132 - IIR Filter Coefficient Data for SET 1 (AFCOEF132) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Any writes to these bit(s) must always have a value of 0.
27-16	COEFF3	0-FFFh	AF Engine IIR filter Coefficient #3 (Set 1). The range is signed -32 ≤ value ≤ 31 +63/64.
15-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	COEFF2	0-FFFh	AF Engine IIR filter Coefficient #2 (Set 1). The range is signed -32 ≤ value ≤ 31 +63/64.

6.5.16 IIR Filter Coefficient Data for SET 1 (AFCOEFF154)

The IIR filter coefficient data for SET 1 (AFCOEFF154) register is shown in Figure 577 and described in Table 514.

Figure 577. AFCOEFF154 - IIR Filter Coefficient Data for SET 1 (AFCOEFF154)

31-28	27-16
Reserved	COEFF5
R-00	R/W-0
15-12	11-0
Reserved	COEFF4
R-00	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 514. AFCOEFF154 - IIR Filter Coefficient Data for SET 1 (AFCOEFF154) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Any writes to these bit(s) must always have a value of 0.
27-16	COEFF5	0-FFFh	AF Engine IIR filter Coefficient #5 (Set 1). The range is signed -32 ≤ value ≤ 31 +63/64.
15-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	COEFF4	0-FFFh	AF Engine IIR filter Coefficient #4 (Set 1). The range is signed -32 ≤ value ≤ 31 +63/64.

6.5.17 IIR Filter Coefficient Data for SET 1 (AFCOEFF176)

The IIR filter coefficient data for SET 1 (AFCOEFF176) register is shown in Figure 578 and described in Table 515.

Figure 578. AFCOEFF176 - IIR Filter Coefficient Data for SET 1 (AFCOEFF176)

31-28	27-16
Reserved	COEFF7
R-00	R/W-0
15-12	11-0
Reserved	COEFF6
R-00	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 515. AFCOEFF176 - IIR Filter Coefficient Data for SET 1 (AFCOEFF176) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Any writes to these bit(s) must always have a value of 0.
27-16	COEFF7	0-FFFh	AF Engine IIR filter Coefficient #7 (Set 1). The range is signed -32 ≤ value ≤ 31 +63/64.
15-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	COEFF6	0-FFFh	AF Engine IIR filter Coefficient #6 (Set 1). The range is signed -32 ≤ value ≤ 31 +63/64.

6.5.18 IIR filter Coefficient Data for SET 1 (AFCOEFF198)

The IIR filter coefficient data for SET 1(AFCOEFF198) register is shown in Figure 579 and described in Table 516.

Figure 579. IIR Filter Coefficient Data for SET 1 (AFCOEFF198) Register

31-28	27-16
Reserved	COEFF9
R-00	R/W-0
15-12	11-0
Reserved	COEFF8
R-00	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 516. IIR Filter Coefficient Data for SET 1 (AFCOEFF198) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Any writes to these bit(s) must always have a value of 0.
27-16	COEFF9	0-FFFh	AF Engine IIR filter Coefficient #9 (Set 1). The range is signed -32 ≤ value ≤ 31 +63/64.
15-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	COEFF8	0-FFFh	AF Engine IIR filter Coefficient #8 (Set 1). The range is signed -32 ≤ value ≤ 31 +63/64.

6.5.19 IIR Filter Coefficient Data for SET 1 (AFCOEFF1010)

The IIR filter coefficient data for SET 1 (AFCOEFF1010) register is shown in Figure 580 and described in Table 517.

Figure 580. IIR Filter Coefficient Data for SET 1 (AFCOEFF1010) Register

31-16
Reserved
R-00

15-12	11-0
Reserved	COEFF10
R-00	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 517. IIR Filter Coefficient Data for SET 1 (AFCOEFF1010) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	COEFF10	0-FFFh	AF Engine IIR filter Coefficient #10 (Set 1). The range is signed -32 ≤ value ≤ 31 +63/64.

6.5.20 Configuration for AE/AWB Windows (AEWWIN1)

The Configuration for AE/AWB Windows (AEWWIN1) register is shown in Figure 581 and described in Table 518.

Figure 581. Configuration for AE/AWB Windows (AEWWIN1) Register

31-24	23-21	20-16
WINH	Reserved	WINW
R/W-0	R-0	R/W-0

15-13	12-6	5-0
WINW	WINVC	WINHC
R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 518. AEWWIN1 - Configuration for AE/AWB Windows (AEWWIN1) Field Descriptions

Bit	Field	Value	Description
31-24	WINH	0-FFh	AE/AWB Engine Window Height. This specifies the window height in an even number of pixels, the window height is the value plus 1 multiplied by 2. The final value can be from 2-512 (even).
23-21	Reserved	0	Any writes to these bit(s) must always have a value of 0.
20-13	WINW	0-FFh	AE/AWB Engine Window Width. This specifies the window width in an even number of pixels, the window width is the value plus 1 multiplied by 2. The minimum width is expected to be 8 pixels.
12-6	WINVC	0-7Fh	AE/AWB Engine Vertical Window Count. The number of windows in the vertical direction plus 1. The maximum number of vertical windows in a frame should not exceed 128. The value should be set to ensure that the bandwidth requirements and buffer size are not exceeded.
5-0	WINHC	0-3Fh	AE/AWB Engine Horizontal Window Count. The number of horizontal windows plus 1. The maximum number of horizontal windows is 35 plus 1 (36). The minimum number of windows should be 2 (valid range for the field is 1-35).

6.5.21 Start Position for AE/AWB Windows (AEWINSTART)

The Start Position for AE/AWB Windows (AEWINSTART) register is shown in Figure 582 and described in Table 519.

Figure 582. Start Position for AE/AWB Windows (AEWINSTART) Register

31-28	27-16
Reserved	WINSV
R-0	R/W-0

15-12	11-0
Reserved	WINSH
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 519. Start Position for AE/AWB Windows (AEWINSTART) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Any writes to these bit(s) must always have a value of 0.
27-16	WINSV	0-FFFh	AE/AWB Engine Vertical Window Start Position. Sets the first line for the first window. Range 0-4095.
15-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-0	WINSH	0-FFFh	AE/AWB Engine Horizontal Window Start Position. Sets the horizontal position for the first window on each line. Range 0-4095.

6.5.22 Start Position and Height for Black Line of AE/AWB Windows (AEWINBLK)

The Start Position and Height for Black Line of AE/AWB Windows (AEWINBLK) register is shown in Figure 583and described in Table 520.

Figure 583. Start Position and Height for Black Line of AE/AWB Windows (AEWINBLK) Register

31-28	27-16
Reserved	WINSV
R-0	R/W-0

15-7	6-0
Reserved	WINH
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 520. Start Position and Height for Black Line of AE/AWB Windows (AEWINBLK) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Any writes to these bit(s) must always have a value of 0.
27-16	WINSV	0-FFFh	AE/AWB Engine Vertical Window Start Position for single black line of windows. Sets the first line for the single black line of windows. Range 0-4095 Note that the horizontal start and the horizontal number of windows will be similar to the regular windows.
15-7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6-0	WINH	0-7Fh	AE/AWB Engine Window Height for the single black line of windows. This specifies the window height in an even number of pixels, the window height is the value plus 1 multiplied by 2. The final value can be from 2-256 (even).

6.5.23 Configuration for Subsample Data in AE/AWB Window (AEWSUBWIN)

The Configuration for Subsample Data in AE/AWB Window (AEWSUBWIN) register is shown in Figure 584 and described in Table 521.

Figure 584. Configuration for Subsample Data in AE/AWB Window (AEWSUBWIN) Register

31-16
Reserved
R-0

15-12	11-8	7-4	3-0
Reserved	AEWINCV	Reserved	AEWINCH
R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 521. Configuration for Subsample Data in AE/AWB Window (AEWSUBWIN) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Any writes to these bit(s) must always have a value of 0.
11-8	AEWINCV	0-Fh	AE/AWB Engine Vertical Sampling Point Increment. Sets vertical distance between sub-samples within a window plus 1 multiplied by 2. The final range is 2-32.
7-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.
3-0	AEWINCH	0-Fh	AE/AWB Engine Horizontal Sampling Point Increment. Sets horizontal distance between sub-samples within a window plus 1 multiplied by 2. The final range is 2-32.

6.5.24 SDRAM/DDRAM Start Address for AE/AWB Engine Output Data (AEWBUFST)

The SDRAM/DDRAM Start Address for AE/AWB Engine Output Data (AEWBUFST) register is shown in Figure 585 and described in Table 522.

Figure 585. SDRAM/DDRAM Start Address for AE/AWB Engine Output Data (AEWBUFST) Register

31-16
AEWBUFST
R/W-0

15-0
AEWBUFST
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 522. SDRAM/DDRAM Start Address for AE/AWB Engine Output Data (AEWBUFST) Field Descriptions

Bit	Field	Value	Description
31-0	AEWBUFST	0-FFFF FFFFh	AE/AWB Engine SDRAM/DDRAM Start Address. The starting location in the SDRAM/DDRAM for the AE/AWB data. The 6 LSB are ignored, address should be on a 64-byte boundary. This field can be altered even when the AE/AWB is busy. Change will take place only for the next frame. However, note that reading this register will always give the latest value.

6.5.25 AE/AWB Engine Configuration (RSDR_ADDR)

The AE/AWB Engine Configuration (RSDR_ADDR) register is shown in Figure 586 and described in Table 523.

Figure 586. AE/AWB Engine Configuration (RSDR_ADDR) Register

31-16
Reserved
R-0

15-10	9-8	7-4	3-0
Reserved	AEFMT	Reserved	SUMSFT
R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 523. AE/AWB Engine Configuration (RSDR_ADDR) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-8	AEFMT		AE/AWB OUTPUT Format.
		0	Sum of squares data along with accumulated data.
		1h	Min and max values of each color of each window.
		2h	Only send the accumulator values.
		3h	Reserved
7-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.
3-0	SUMSFT	0-Fh	AE/AWB Engine Shift Value for the sum of pixel values. The right shift value for the accumulated pixel values to avoid overflow when built into a packet. SUMSFT = right shift value. Range: 0 -15 This registered is shadowed and latched on the rising edge of VSYNC.

6.5.26 Line Start Position for ISIF Interface (LINE_START)

The Line Start Position for ISIF Interface (LINE_START) register is shown in Figure 587 and described in Table 524.

Figure 587. Line Start Position for ISIF Interface (LINE_START) Register

31-16
SLV
W-0
15-0
LINE_START
R/W-0

LEGEND: R/W = Read/Write; W = Write only; -*n* = value after reset

Table 524. Line Start Position for ISIF Interface (LINE_START) Field Descriptions

Bit	Field	Value	Description
31-16	SLV	0-FFFFh	Start Line Vertical. Specifies how many lines after the VD rising edge the real frame starts.
15-0	LINE_START	0-FFFFh	Line Start. Specifies the start pixel of the ISIF interface module into the line buffer.

6.5.27 AF Vertical Focus Configuration 1 (VFV_CFG1)

The AF Vertical Focus Configuration 1 (VFV_CFG1) register is shown in Figure 588 and described in Table 525.

Figure 588. AF Vertical Focus Configuration 1 (VFV_CFG1) Register

31-24	23-16
VCOEF1_3	VCOEF1_2
R/W-0	R/W-0
15-8	7-0
VCOEF1_1	VCOEF1_0
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 525. AF Vertical Focus Configuration 1 (VFV_CFG1) Field Descriptions

Bit	Field	Value	Description
31-24	VCOEF1_3	0-FFh	Vertical FV FIR 1 coefficient 3.
23-16	VCOEF1_2	0-FFh	Vertical FV FIR 1 coefficient 2.
15-8	VCOEF1_1	0-FFh	Vertical FV FIR 1 coefficient 1.
7-0	VCOEF1_0	0-FFh	Vertical FV FIR 1 coefficient 0.

6.5.28 AF Vertical Focus Configuration 2 (VFV_CFG2)

The AF Vertical Focus Configuration 2 (VFV_CFG2) register is shown in Figure 589 and described in Table 526.

Figure 589. AF Vertical Focus Configuration 2 (VFV_CFG2) Register

31-16	
VTHR1	
R/W-0	
15-8	7-0
Reserved	VCOEF1_4
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 526. AF Vertical Focus Configuration 2 (VFV_CFG2) Field Descriptions

Bit	Field	Value	Description
31-16	VTHR1	0-FFFFh	Threshold for Vertical FV FIR 1.
15-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	VCOEF1_4	0-FFh	Vertical FV FIR 1 coefficient 4.

6.5.29 Vertical Focus Configuration 3 (VFV_CFG3)

The AF Vertical Focus Configuration 3 (VFV_CFG3) register is shown in Figure 590 and described in Table 527.

Figure 590. AF Vertical Focus Configuration 3 (VFV_CFG3) Register

31-24	23-16
VCOEF2_3	VCOEF2_2
R/W-0	R/W-0
15-8	7-0
VCOEF2_1	VCOEF2_0
R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 527. AF Vertical Focus Configuration 3 (VFV_CFG3) Field Descriptions

Bit	Field	Value	Description
31-24	VCOEF2_3	0-FFh	Vertical FV FIR 2 coefficient 3.
23-16	VCOEF2_2	0-FFh	Vertical FV FIR 2 coefficient 2.
15-8	VCOEF2_1	0-FFh	Vertical FV FIR 2 coefficient 1.
7-0	VCOEF2_0	0-FFh	Vertical FV FIR 2 coefficient 0.

6.5.30 Vertical Focus Configuration 4 (VFV_CFG4)

The AF Vertical Focus Configuration 4 (VFV_CFG4) register is shown in Figure 591 and described in Table 528.

Figure 591. AF Vertical Focus Configuration 4 (VFV_CFG4) Register

31-16
VTHR2
R/W-0

15-8	7-0
Reserved	VCOEF2_4
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 528. AF Vertical Focus Configuration 4 (VFV_CFG4) Field Descriptions

Bit	Field	Value	Description
31-16	VTHR2	0-FFFFh	Threshold for Vertical FV FIR 2.
15-8	Reserved	0	Reserved
7-0	VCOEF2_4	0-FFh	Vertical FV FIR 2 coefficient 4.

6.5.31 Horizontal Threshold (HFV_THR)

The Horizontal Threshold (HFV_THR) register is shown in Figure 592 and described in Table 529.

Figure 592. Horizontal Threshold (HFV_THR) Register

31-16
HTHR2
R/W-0

15-0
HTHR1
R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 529. Horizontal Threshold (HFV_THR) Field Descriptions

Bit	Field	Value	Description
31-16	HTHR2	0-FFFFh	Threshold for Horizontal FV IIR 2.
15-0	HTHR1	0-FFFFh	Threshold for Horizontal FV IIR 1.

6.6 Lens Distortion Correction (LDC) Registers

The lens distortion correction (LDC) registers are shown in Table 530.

Table 530. LDC Registers

Offset	Acronym	Register Description	Section
0h	PID	Peripheral ID	Section 6.6.1
04h	PCR	Peripheral Control Register	Section 6.6.2
08h	RD_BASE	Read Frame Base	Section 6.6.3
0Ch	RD_OFST	Read Frame Line Offset	Section 6.6.4
10h	FRAME_SIZE	Frame Size	Section 6.6.5
14h	INITXY	Initial XY	Section 6.6.6
18h	WR_BASE	Write Frame Base	Section 6.6.8
1Ch	WR_OFST	Write Frame Line Offset	Section 6.6.8
20h	420C_RD_BASE	420 CbCr Read Frame Base	Section 6.6.9
24h	420C_WR_BASE	420 CbCr Write Frame Base	Section 6.6.10
28h	CONFIG	LD Configuration	Section 6.6.11
2Ch	CENTER	Lens Center	Section 6.6.12
30h	KHV	Horizontal/Vertical scaling factor	Section 6.6.13
34h	BLOCK	Block Size	Section 6.6.14
38h	LUT_ADDR	LUT initial address	Section 6.6.15
3Ch	LUT_WDATA	LUT write data	Section 6.6.16
40h	LUT_RDATA	LUT read data	Section 6.6.17
44h	AFFINE_AB	Affine Transform A/B	Section 6.6.18
48h	AFFINE_CD	Affine Transform C/D	Section 6.6.19
4Ch	AFFINE_EF	Affine Transform E/F	Section 6.6.20

6.6.1 Peripheral ID (PID)

The peripheral ID (PID) register is shown in Figure 593 and described in Table 531.

Figure 593. Peripheral ID (PID)

31-24	23-16
Reserved	TID
R-00	R-36
15-8	7-0
CID	PREV
R-254	R-5

LEGEND: R = Read only; -*n* = value after reset

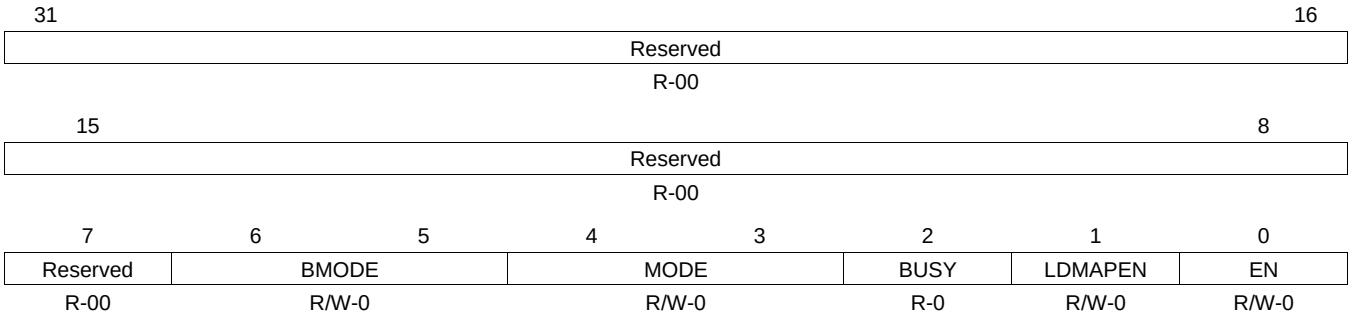
Table 531. Peripheral ID (PID) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Reserved
23-16	TID	0-FFh	Peripheral Identification LDC.
15-8	CID	0-FFh	Class Identification VPFE module.
7-0	PREV	0-FFh	Peripheral Revision Number Initial Revision.

6.6.2 Peripheral Control Register (PCR)

The peripheral control register (PCR) is shown in Figure 594 and described in Table 532.

Figure 594. Peripheral Control Register (PCR)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 532. Peripheral Control Register (PCR) Field Descriptions

Bit	Field	Value	Description
31-7	Reserved	0	Any writes to these bit(s) must always have a value of 0.
6-5	BMODE		Bayer Format Applicable when MODE = 1
		0	unpacked12
		1	packed12
		2	packed8
		3	A-Law
4-3	MODE		Input/Output Video Mode Type Bayer mode is for Chromatic Aberration Correction and Affine Transform Other modes are for Lens Distortion and Affine Transform
		0	yuv422
		1	bayer_cac
		2	yuv420
		3	mode_undefined
2	BUSY		Busy Status Asserted when LDC starts and clear when it completes
		0	idle
		1	busy
1	LDMAPEN		Lens Distortion Enabled If 0, Lens Distortion is not performed; Only Affine Transform Must be 1 for Bayer mode
		0	ldmap_disable
		1	ldmap_enable
0	EN		Enable Write '1' to start the LDC
		0	disable
		1	enable

6.6.3 Read Frame Base (RD_BASE)

The read frame base (RD_BASE) is shown in Figure 595 and described in Table 533.

Figure 595. Read Frame Base (RD_BASE) Register

31-16
RBASE
R/W-0
15-0
RBASE
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 533. Read Frame Base (RD_BASE) Field Descriptions

Bit	Field	Value	Description
31-0	RBASE	0-FFFF FFFFh	Read frame base/420 Y Read Base Must be 32-byte aligned

6.6.4 Read Frame Line Offset (RD_OFST)

The read frame line offset (RD_OFST) register is shown in Figure 596 and described in Table 534.

Figure 596. Read Frame Line Offset (RD_OFST) Register

31-16
Reserved
R-00
15-0
ROFST
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 534. RD_OFST - Read Frame Line Offset (RD_OFST) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	ROFST	0-FFFFh	Read frame line offset Must be 32-byte aligned In 420 mode, applies to both Y read data and CbCr read data

6.6.5 Frame Size (FRAME_SIZE)

The frame size (FRAME_SIZE) register is shown in Figure 597 and described in Table 535.

Figure 597. Frame Size (FRAME_SIZE)

31-30	29-16
Reserved	H
R-00	R/W-0
15-14	13-0
Reserved	W
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 535. Frame Size (FRAME_SIZE) Field Descriptions

Bit	Field	Value	Description
31-30	Reserved	0	Any writes to these bit(s) must always have a value of 0.
29-16	H	0-3FFFh	Frame number of lines
15-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	W	0-3FFFh	Frame width

6.6.6 LD Initial Coordinates (INITXY)

The LD initial coordinates (INITXY) register is shown in Figure 598 and described in Table 536.

Figure 598. LD Initial Coordinates (INITXY) Register

31-30	29-16
Reserved	INITY
R-00	R/W-0
15-14	13-0
Reserved	INITX
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 536. LD Initial Coordinates (INITXY) Field Descriptions

Bit	Field	Value	Description
31-30	Reserved	0	Any writes to these bit(s) must always have a value of 0.
29-16	INITY	0-3FFFh	Output starting Y coordinate.
15-14	Reserved	0	Reserved
13-0	INITX	0-3FFFh	Output starting X coordinate.

6.6.7 Write Frame Base (WR_BASE)

The write frame base (WR_BASE) register is shown in Figure 599 and described in Table 537.

Figure 599. Write Frame Base (WR_BASE) Register

31-16
WBASE
R/W-0
15-0
WBASE
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 537. Write Frame Base (WR_BASE) Field Descriptions

Bit	Field	Value	Description
31-0	WBASE	0-FFFF FFFFh	Write frame base/420 Y Write Base Must be 32-byte aligned

6.6.8 Write Frame Line Offset (WR_OFST)

The write frame line offset (WR_OFST) register is shown in Figure 600 and described in Table 538.

Figure 600. Write Frame Line Offset (WR_OFST) Register

31-16
Reserved
R-00

t

15-0
WOFST
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 538. Write Frame Line Offset (WR_OFST) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	WOFST	0-FFFFh	Write frame line offset Must be 32-byte aligned In 420 mode. Applies to both Y write data and CbCr write data.

6.6.9 420 CbCr Read Frame Base (420C_RD_BASE)

The 420 CbCr read frame Base (420C_RD_BASE) register is shown in Figure 601 and described in Table 539.

Figure 601. 420 CbCr Read Frame Base (420C_RD_BASE)

31-16
RBASE_420C
R/W-0

15-0
RBASE_420C
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 539. 4420 CbCr Read Frame Base (420C_RD_BASE) Field Descriptions

Bit	Field	Value	Description
31-0	RBASE_420C	0-FFFF FFFFh	420 CbCr Read frame base Must be 32-byte aligned. Only applies in MODE = 2 (420)

6.6.10 420 CbCr Write Frame Base (420C_WR_BASE)

The 420 CbCr write frame base (420C_WR_BASE) register is shown in Figure 602 and described in Table 540.

Figure 602. 420 CbCr Write Frame Base (420C_WR_BASE) Register

31-16
WBASE_420C
R/W-0
15-0
WBASE_420C
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 540. 420 CbCr Write Frame Base (420C_WR_BASE) Field Descriptions

Bit	Field	Value	Description
31-0	WBASE_420C	0-FFFF FFFFh	420 CbCr Write frame base Must be 32-byte aligned Only applies in MODE = 2 (420)

6.6.11 LD Configuration (CONFIG)

The LD Configuration (CONFIG) register is shown in Figure 603 and described in Table 541.

Figure 603. LD Configuration (CONFIG) Register

31-30	29-16
Reserved	RTH
R-00	R-0

15-8	7	6	5-4	3-0
Reserved	CNST_MD	YINT_TYPE	INITC	T
R-00	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 541. LD Configuration (CONFIG) Field Descriptions

Bit	Field	Value	Description
31-30	Reserved	0	Any writes to these bit(s) must always have a value of 0.
29-16	RTH	0-3FFFh	Threshold in LD back mapping
15-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7	CNST_MD		Constant Write Address Mode When 1, all output tiles are written to the write base address defined in WBASE and WBASE_420C (if 420). When 0, output addressing will start at the base addresses defined in WBASE and WBASE_420C (if 420), and automatically increment to the proper output address for each output tile in DDR (normal operation)
		0	Normal Write Address Mode
		1	Constant Write Address Mode
6	YINT_TYPE		Y Interpolation Type Applies to 422 and 420 modes only
		0	Y Bicubic Interpolation
		1	Y Bilinear Interpolation
5-4	INITC		Initial color in LD back mapping Only applies to Bayer mode
		0	red
		1	green on red row
		2	green on blue row
		3	blue
3-0	T	0-Fh	Right Shift Bits in LD back mapping

6.6.12 Lens Center (CENTER)

The lens center (CENTER) register is shown in Figure 604and described in Table 542 .

Figure 604. Lens Center (CENTER) Register

31-30	29-16
Reserved	V0
R-00	R/W-0
15-14	13-0
Reserved	H0
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 542. Lens Center (CENTER) Field Descriptions

Bit	Field	Value	Description
31-30	Reserved	0	Any writes to these bit(s) must always have a value of 0.
29-16	V0	0-3FFFh	Lens center Y coordinate
15-14	Reserved	0	Reserved
13-0	H0	0-3FFFh	Lens center X coordinate

6.6.13 Horizontal/Vertical Scaling Factor (KHV)

The horizontal/vertical scaling factor (KHV) register is shown in Figure 605 and described in Table 543.

Figure 605. Horizontal/Vertical Scaling Factor (KHV) Register

31-24	23-16
KVL	KVU
R/W-0	R/W-0
15-8	**7-0**
KHR	KHL
R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 543. Horizontal/Vertical scaling factor (KHV) Field Descriptions

Bit	Field	Value	Description
31-24	KVL	0-FFh	Vertical Lower scaling factor
23-16	KVU	0-FFh	Vertical Upper scaling factor
15-8	KHR	0-FFh	Horizontal Right scaling factor
7-0	KHL	0-FFh	Horizontal Left scaling factor

6.6.14 Block Size (BLOCK)

The block size (BLOCK) register is shown in Figure 606 and described in Table 544.

Figure 606. Block Size (BLOCK) Register

31-20	19-16
Reserved	PIXPAD
R-00	R/W-0

15-8	7-0
OBH	OBW
R/W-0	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 544. Block Size (BLOCK) Field Descriptions

Bit	Field	Value	Description
31-20	Reserved	0	Any writes to these bit(s) must always have a value of 0.
19-16	PIXPAD	0-Fh	Pixel Pad
15-8	OBH	0-FFh	Output block height
7-0	OBW	0-FFh	Output block width

6.6.15 LUT Initial Address (LUT_ADDR)

The LUT initial address (LUT_ADDR) register is shown in Figure 607 and described in Table 545.

Figure 607. LUT Initial Address (LUT_ADDR) Register

31-16
Reserved
R-00

15-8	7-0
Reserved	ADDR
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 545. LUT Initial Address (LUT_ADDR) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	ADDR	0-FFh	LD LUT initial address Range: 0-255

6.6.16 LUT Write Data (LUT_WDATA)

The LUT write data (LUT_WDATA) register is shown in Figure 608 and described in Table 546.

Figure 608. LUT Write Data (LUT_WDATA) Register

31-16
Reserved
R-00

15-14	13-0
Reserved	WDATA
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 546. LUT Write Data (LUT_WDATA) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	WDATA	0-3FFFh	Write data Writing to this register will write to an entry in LD LUT, pointed by LUT_ADDR, which is automatically incremented after each write.

6.6.17 LUT Read Data (LUT_RDATA)

The LUT read data (LUT_RDATA) is shown in Figure 609 and described in Table 547.

Figure 609. LUT Read Data (LUT_RDATA) Register

31-16
Reserved
R-00

15-14	13-0
Reserved	RDATA
R-00	R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 547. LUT Read Data (LUT_RDATA) Field Descriptions

Bit	Field	Value	Description
31-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	RDATA	0-3FFFh	Read data. Reading from this register will read from an entry in LD LUT, pointed by LUT_ADDR, which is automatically incremented after each read.

6.6.18 Affine Transform A/B (AFFINE_AB)

The affine transform A/B (AFFINE_AB) register is shown in Figure 610 and described in Table 548.

Figure 610. Affine Transform A/B (AFFINE_AB) Register

31-30	29-16
Reserved	B
R-00	R/W-0
15-14	13-0
Reserved	A
R-00	R/W-4096

LEGEND: R = Read only; -*n* = value after reset

Table 548. Affine Transform A/B (AFFINE_AB) Field Descriptions

Bit	Field	Value	Description
31-30	Reserved	0	Any writes to these bit(s) must always have a value of 0.
29-16	B	0-3FFh	Affine Transform B Register (S14Q12)
15-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	A	0-3FFFh	Affine Transform A Register (S14Q12)

6.6.19 Affine Transform C/D (AFFINE_CD)

The affine transform C/D (AFFINE_CD) register is shown in Figure 611 and described in Table 549.

Figure 611. Affine Transform C/D (AFFINE_CD) Register

31-30	29-16
Reserved	D
R-00	R/W-0

15-0
C
R/W-0

LEGEND: R = Read only; -*n* = value after reset

Table 549. Affine Transform C/D (AFFINE_CD) Field Descriptions

Bit	Field	Value	Description
31-30	Reserved	0	Any writes to these bit(s) must always have a value of 0.
29-16	D	0-3FFFh	Affine Transform D Register (S14Q12).
15-0	C	0-FFFFh	Affine Transform C Register (S16Q3).

6.6.20 Affine Transform E/F (AFFINE_EF)

The affine transform E/F (AFFINE_EF) register is shown in Figure 612and described in Table 550.

Figure 612. Affine Transform E/F (AFFINE_EF)

31-16
F
R/W-0

15-14	13-0
Reserved	E
R-00	R/W-4096

LEGEND: R = Read only; -*n* = value after reset

Table 550. Affine Transform E/F (AFFINE_EF) Field Descriptions

Bit	Field	Value	Description
31-16	F	0-FFFFh	Affine Transform F Register (S16Q3)
15-14	Reserved	0	Any writes to these bit(s) must always have a value of 0.
13-0	E	0-3FFFh	Affine Transform E Register (S14Q12)

6.7 ISP5 System Configuration (ISP) Registers

The ISP5 system configuration registers are listed here and described in the following sections.

Table 551. ISP5 System Configuration Registers

Offset	Acronym	Register Description	Section
0h	PID	Peripheral Revision and Class Information	Section 6.7.1
04h	PCCR	Peripheral Clock Control Register	Section 6.7.2
08h	BCR	Buffer Logic Control Register	Section 6.7.3
0Ch	INTSTAT	Interrupt Status Register	Section 6.7.4
10h	INTSEL1	Interrupt Selection Register 1	Section 6.7.5
14h	INTSEL2	Interrupt Selection Register 2	Section 6.7.6
18h	INTSEL3	Interrupt Selection Register 3	Section 6.7.7
1Ch	EVTSEL	Event Selection Register	Section 6.7.8
2Ch	MPSR	Memory Priority Select Register	Section 6.7.9

6.7.1 Peripheral Revision and Class Information (PID) Register

The Peripheral Revision and Class Information (PID) register is shown in Figure 613 and described in Table 552.

Figure 613. Peripheral Revision and Class Information (PID) Register

31-16
PREV
R-1276643328

15-0
PREV
R-1276643328

LEGEND: R = Read only; -*n* = value after reset

Table 552. Peripheral Revision and Class Information (PID) Field Descriptions

Bit	Field	Value	Description
31-0	PREV	0-FFFF FFFFh	Peripheral Revision Number Initial Revision

6.7.2 Peripheral Clock Control Register (PCCR)

The Peripheral Clock Control Register (PCCR) is shown in Figure 614 and described in Table 553.

Figure 614. Peripheral Clock Control Register (PCCR)

31-8							
Reserved							
R-0							
7	6	5	4	3	2	1	0
PSYNC_CLK_SEL	SYNC_ENABLE	IPIPEIF_CLK_ENABLE	IPIPE_CLK_ENABLE	RSZ_CLK_ENABLE	H3A_CLK_ENABLE	ISIF_CLK_ENABLE	BL_CLK_ENABLE
R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 553. Peripheral Clock Control Register (PCCR) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7	PSYNC_CLK_SEL	0-1	PSYNC enable 0: Disable 1:Enable
6	SYNC_ENABLE	0-1	SYNC enable 0: Disable 1:Enable
5	IPIPEIF_CLK_ENABLE	0-1	IPIPEIF clock enable 0: Disable 1:Enable
4	IPIPE_CLK_ENABLE	0-1	IPIPE clock enable 0: Disable 1:Enable
3	RSZ_CLK_ENABLE	0-1	RSZ clock enable 0: Disable 1:Enable
2	H3A_CLK_ENABLE	0-1	H3A clock enable 0: Disable 1:Enable
1	ISIF_CLK_ENABLE	0-1	ISIF clock enable 0: Disable 1:Enable
0	BL_CLK_ENABLE	0-1	BL clock enable 0: Disable 1:Enable (should be set to 1 for DDR R/W access)

6.7.3 Buffer Logic Control (BCR) Register

The Buffer Logic Control (BCR) register is shown in Figure 615 and described in Table 554.

Figure 615. Buffer Logic Control (BCR) Register

31-8			
Reserved			
R-0			
7-5	4-2	1	0
CPRIORITY_W	CPRIORITY_R	SRC_SEL_ISIF_IPIPE	SRC_SEL_IPIPE_LDC
R/W-0	R/W-0	R/W-1	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 554. Buffer Logic Control (BCR) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-5	CPRIORITY_W	0-7h	Sets Priority of VPSS. Should be set to highest priority (0) for best performance.
4-2	CPRIORITY_R	0-7h	Sets Priority of VPSS. Should be set to highest priority (0) for best performance.
1	SRC_SEL_ISIF_IPIPE		BL_WBL select (DDR write port mux b/w IPIPE boxcar output and ISIF output)
		0	IPIPE BOXCAR OUT
		1	ISIF OUT
0	SRC_SEL_IPIPE_LDC		BL_WBL select (DDR write port mux b/w IPIPE boxcar output and LDC output)
		0	LDC OUT
		1	IPIPE BOXCAR OUT

6.7.4 Interrupt Status (INTSTAT) Register

The Interrupt Status (INTSTAT) register is shown in Figure 616 and described in Table 555.

Figure 616. Interrupt Status (INTSTAT) Register

31-30	29	28	27	26	25	24
Reserved	IPIPE_INT_DPC_RNEW1	IPIPE_INT_DPC_RNEW0	IPIPE_INT_DPC_INI	LDC_INT_EOF	IPIPE_INT_EOF	H3A_INT_EOF
R/W-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0

23	22	21	20	19-18	17	16
RSZ_INT_EOF1	RSZ_INT_EOF0	VENC_INT	OSD_INT	Reserved	RSZ_INT_CYC_RZB	RSZ_INT_CYC_RZA
R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W-0	R/W1C-0	R/W1C-0

15	14	13	12	11	10	9	8
Reserved	RSZ_INT_LAST	RSZ_INT_REG	Reserved	AF_INT	AEW_INT	IPIPEIF_INT	IPIPE_INT_HST
R/W-0	R/W1C-0	R/W1C-0	R/W-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0

7	6	5	4	3	2	1	0
IPIPE_INT_BSC	Reserved	IPIPE_INT_LAST_PIX	IPIPE_INT_REG	ISIF_INT3	ISIF_INT2	ISIF_INT1	ISIF_INT0
R/W1C-0	R/W-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0	R/W1C-0

LEGEND: R/W = Read/Write; W1C = Write 1 to clear bit; -*n* = value after reset

Table 555. Interrupt Status (INTSTAT) Field Descriptions

Bit	Field	Value	Description
31-30	Reserved	0	Any writes to these bit(s) must always have a value of 0.
29	IPIPE_INT_DPC_RNEW1		Set when IPIPE_INT_DPC_RNEW1 is triggered, clear by writing 1.
		1	Clear bit
28	IPIPE_INT_DPC_RNEW0		Set when IPIPE_INT_DPC_RNEW0 is triggered, clear by writing 1.
		1	Clear bit
27	IPIPE_INT_DPC_INI		Set when IPIPE_INT_DPC_INI is triggered, clear by writing 1.
		1	Clear bit
26	LDC_INT_EOF		Set when LDC_INT_EOF is triggered, clear by writing 1.
		1	Clear bit
25	IPIPE_INT_EOF		Set when IPIPE_INT_EOF is triggered, clear by writing 1.
		1	Clear bit
24	H3A_INT_EOF		Set when H3A_INT_EOF is triggered, clear by writing 1.
		1	Clear bit
23	RSZ_INT_EOF1		Set when RSZ_INT_EOF1 is triggered, clear by writing 1.
		1	Clear bit
22	RSZ_INT_EOF0		Set when RSZ_INT_EOF0 is triggered, clear by writing 1.
		1	Clear bit
21	VENC_INT		Set when VENC_INT is triggered, clear by writing 1.
		1	Clear bit
20	OSD_INT		Set when OSD_INT is triggered, clear by writing 1.
		1	Clear bit
19-18	Reserved	0	Reserved.
17	RSZ_INT_CYC_RZB		Set when RSZ_INT_CYC_RZB is triggered, clear by writing 1.
		1	Clear bit
16	RSZ_INT_CYC_RZA		Set when RSZ_INT_CYC_RZA is triggered, clear by writing 1.
		1	Clear bit
15	Reserved	0	Reserved.

Table 555. Interrupt Status (INTSTAT) Field Descriptions (continued)

Bit	Field	Value	Description
14	RSZ_INT_LAST_PIX		Set when RSZ_INT_LAST_PIX is triggered, clear by writing 1.
		1	Clear bit
13	RSZ_INT_REG		Set when RSZ_INT_REG is triggered, clear by writing 1.
		1	Clear bit
12	Reserved	0	Reserved.
11	AF_INT		Set when AF_INT is triggered, clear by writing 1.
		1	Clear bit
10	AEW_INT		Set when AEW_INT is triggered, clear by writing 1.
		1	Clear bit
9	IPIPEIF_INT		Set when IPIPEIF_INT is triggered, clear by writing 1.
		1	Clear bit
8	IPIPE_INT_HST		Set when IPIPE_INT_HST is triggered, clear by writing 1.
		1	Clear bit
7	IPIPE_INT_BSC		Set when IPIPE_INT_BSC is triggered, clear by writing 1.
		1	Clear bit
6	Reserved	0	Reserved.
5	IPIPE_INT_LAST_PIX		Set when IPIPE_INT_LAST_PIX is triggered, clear by writing 1.
		1	Clear bit
4	IPIPE_INT_REG		Set when IPIPE_INT_REG is triggered, clear by writing 1.
		1	Clear bit
3	ISIF_INT3		Set when ISIF_INT3 is triggered, clear by writing 1.
		1	Clear bit
2	ISIF_INT2		Set when ISIF_INT2 is triggered, clear by writing 1.
		1	Clear bit
1	ISIF_INT1		Set when ISIF_INT1 is triggered, clear by writing 1.
		1	Clear bit
0	ISIF_INT0		Set when ISIF_INT0 is triggered, clear by writing 1.
		1	Clear bit

6.7.5 Interrupt Selection (INTSEL1) Register

The Interrupt Selection (INTSEL1) register is shown in Figure 617 and described in Table 556.

Figure 617. Interrupt Selection (INTSEL1) Register

31-29	28-24	23-21	20-16
Reserved	INTSEL3	Reserved	INTSEL2
R-0	R/W-0	R-0	R/W-0
15-13	12-8	7-5	4-0
Reserved	INTSEL1	Reserved	INTSEL0
R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 556. Interrupt Selection (INTSEL1) Field Descriptions

Bit	Field	Value	Description
31-29	Reserved	0	Any writes to these bit(s) must always have a value of 0.
28-24	INTSEL3		Selects the interrupt for vpss_int[3]
		0	ISIF_INT0
		1	ISIF_INT1
		2	ISIF_INT2
		3	ISIF_INT3
		4	IPIPE_INT_REG
		5	IPIPE_INT_LAST_PIX
		6	Reserved
		7	IPIPE_INT_BSC
		8	IPIPE_INT_HST
		9	IPIPEIF_INT
		10	AEW_INT
		11	AF_INT
		12	Reserved
		13	RSZ_INT_REG
		14	RSZ_INT_LAST_PIX
		15	Reserved
		16	RSZ_INT_CYC_RZA
		17	RSZ_INT_CYC_RZB
		18	Reserved
		19	Reserved
		20	OSD_INT
		21	VENC_INT
		22	RSZ_INT_EOF0
		23	RSZ_INT_EOF1
		24	H3A_INT_EOF
		25	IPIPE_INT_EOF
		26	LDC_INT_EOF
		27	IPIPE_INT_DPC_INI
		28	IPIPE_INT_DPC_RNEW0
		29	IPIPE_INT_DPC_RNEW1
		30-31	Reserved
23-21	Reserved	0	Any writes to these bit(s) must always have a value of 0.
20-16	INTSEL2	0-1Fh	Selects the interrupt for vpss_int[2]
15-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.

Table 556. Interrupt Selection (INTSEL1) Field Descriptions (continued)

Bit	Field	Value	Description
12-8	INTSEL1	0-1Fh	Selects the interrupt for vpss_int[1]
7-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4-0	INTSEL0	0-1Fh	Selects the interrupt for vpss_int[0]

6.7.6 Interrupt Selection (INTSEL2) Register

The Interrupt Selection (INTSEL2) register is shown in Figure 618 and described in Table 557.

Figure 618. Interrupt Selection (INTSEL2) Register

31-29	28-24	23-21	20-16
Reserved	INTSEL7	Reserved	INTSEL6
R-0	R/W-0	R-0	R/W-0
15-13	12-8	7-5	4-0
Reserved	INTSEL5	Reserved	INTSEL4
R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 557. Interrupt Selection (INTSEL2) Field Descriptions

Bit	Field	Value	Description
31-29	Reserved	0	Any writes to these bit(s) must always have a value of 0.
28-24	INTSEL7	0-1Fh	Selects the interrupt for vpss_int[7]
23-21	Reserved	0	Any writes to these bit(s) must always have a value of 0.
20-16	INTSEL6	0-1Fh	Selects the interrupt for vpss_int[6]
15-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.
12-8	INTSEL5	0-1Fh	Selects the interrupt for vpss_int[5]
7-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4-0	INTSEL4	0-1Fh	Selects the interrupt for vpss_int[4]

6.7.7 Interrupt Selection (INTSEL3) Register

The Interrupt Selection (INTSEL3) register is shown in Figure 619 and described in Table 558.

Figure 619. Interrupt Selection (INTSEL3) Register

31-16
Reserved
R-0

15-5	4-0
Reserved	INTSEL8
R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 558. Interrupt Selection (INTSEL3) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4-0	INTSEL8	0-1Fh	Selects the interrupt for vpss_int[8].

6.7.8 Event Selection (EVTSEL) Register

The Event Selection (EVTSEL) register is shown in Figure 620 and described in Table 559.

Figure 620. Event Selection (EVTSEL) Register

31-29	28-24	23-21	20-16
Reserved	EVTSEL3	Reserved	EVTSEL2
R-0	R/W-0	R-0	R/W-0
15-13	12-8	7-5	4-0
Reserved	EVTSEL1	Reserved	EVTSEL0
R-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 559. Event Selection (EVTSEL) Field Descriptions

Bit	Field	Value	Description
31-29	Reserved	0	Any writes to these bit(s) must always have a value of 0.
28-24	EVTSEL3		Selects the event for vpss_evt[3]
		0	ISIF_INT0
		1	ISIF_INT1
		2	ISIF_INT2
		3	ISIF_INT3
		4	IPIPE_INT_REG
		5	IPIPE_INT_LAST_PIX
		6	Reserved
		7	IPIPE_INT_BSC
		8	IPIPE_INT_HST
		9	IPIPEIF_INT
		10	AEW_INT
		11	AF_INT
		12	Reserved
		13	RSZ_INT_REG
		14	RSZ_INT_LAST_PIX
		15	Reserved
		16	RSZ_INT_CYC_RZA
		17	RSZ_INT_CYC_RZB
		18	Reserved
		19	Reserved
		20	OSD_INT
		21	VENC_INT
		22	RSZ_INT_EOF0
		23	RSZ_INT_EOF1
		24	H3A_INT_EOF
		25	IPIPE_INT_EOF
		26	LDC_INT_EOF
		27	IPIPE_INT_DPC_INI
		28	IPIPE_INT_DPC_RNEW0
		29	IPIPE_INT_DPC_RNEW1
		30-31	Reserved
23-21	Reserved	0	Any writes to these bit(s) must always have a value of 0.
20-16	EVTSEL2	0-1Fh	Selects the event for vpss_evt[2]
15-13	Reserved	0	Any writes to these bit(s) must always have a value of 0.

Table 559. Event Selection (EVTSEL) Field Descriptions (continued)

Bit	Field	Value	Description
12-8	EVTSEL1	0-1Fh	Selects the event for vpss_evt[1]
7-5	Reserved	0	Any writes to these bit(s) must always have a value of 0.
4-0	EVTSEL0	0-1Fh	Selects the event for vpss_evt[0]

6.7.9 Memory Priority Select (MPSR) Register

The Memory Priority Select (MPSR) register is shown in Figure 621 and described in Table 560.

Figure 621. Memory Priority Select (MPSR) Register

31-25	24
Reserved	RGBCOPY
R-0	R/W-0

23-21	20	19	18	17	16
Reserved	BSC_TB1	BSC_TB0	HST_TB3	HST_TB2	HST_TB1
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

15	14	13	12	11	10	9	8
HST_TB0	D3L_TB3	D3L_TB2	D3L_TB1	D3L_TB0	GBC_TB	YEE_TB	GMM_TBR
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
GMM_TBG	GMM_TBB	DPC_TB	DCLAMP	LS_TB1	LS_TB0	LIN_TB	Reserved
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 560. Memory Priority Select (MPSR) Field Descriptions

Bit	Field	Value	Description
31-25	Reserved	0	Any writes to these bit(s) must always have a value of 0.
24	RGBCOPY	0-1	RGB memory table copy enable 0: Disable 1:Enable
23-21	Reserved	0	Reserved
20	BSC_TB1	0-1	BSC_TB1 memory access priority
19	BSC_TB0	0-1	BSC_TB0 memory access priority
18	HST_TB3	0-1	HST_TB3 memory access priority
17	HST_TB2	0-1	HST_TB2 memory access priority
16	HST_TB1	0-1	HST_TB1 memory access priority
15	HST_TB0	0-1	HST_TB0 memory access priority
14	D3L_TB3	0-1	D3L_TB3 memory access priority
13	D3L_TB2	0-1	D3L_TB2 memory access priority
12	D3L_TB1	0-1	D3L_TB1 memory access priority
11	D3L_TB0	0-1	D3L_TB0 memory access priority
10	GBC_TB	0-1	GBC_TB memory access priority
9	YEE_TB	0-1	YEE_TB memory access priority
8	GMM_TBR	0-1	GMM_TBR memory access priority
7	GMM_TBG	0-1	GMM_TBG memory access priority
6	GMM_TBB	0-1	GMM_TBB memory access priority
5	DPC_TB	0-1	DPC_TB memory access priority
4	DCLAMP	0-1	DCLAMP memory access priority
3	LS_TB1	0-1	LS_TB1 memory access select
2	LS_TB0	0-1	LS_TB0 memory access select
1	LIN_TB	0-1	LIN_TB memory access priority
0	Reserved	0	Reserved

6.8 VPSS System Configuration (VPSS) Registers

This section contains information about the VPSS system configuration (VPSS) register.

Table 561. VPSS System Configuration (VPSS) Registers

Offset	Acronym	Register Description	Section
0h	VPBE_CLK_CTRL	VPBE Clock Control Register	Section 6.8.1

6.8.1 VPBE Clock Control (VPBE_CLK_CTRL) Register

The peripheral clock control register is shown in Figure 622 and described in Table 562.

Figure 622. VPBE Clock Control (VPBE_CLK_CTRL) Register

31-8							
Reserved							
R-0							
7	6	5	4	3	2	1	0
LDC_CLK_SEL	OSD_CLK_SEL	Rsvd	Rsvd	LDC_CLK_ ENABLE	CLKSEL_VENC	Rsvd	VPBE_CLK_ ENABLE
R/W-0	R/W-0	R-0	R/W-1	R/W-1	R/W-0	R-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 562. VPBE Clock Control (VPBE_CLK_CTRL) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0
7	LDC_CLK_SEL		LDC memory clock select
		0	LDC module has access to memory
		1	ARM has access to memory
6	OSD_CLK_SEL		OSD memory clock select
		0	OSD module has access to memory
		1	ARM has access to memory
5	Reserved	0	Reserved
4	Reserved	0	Reserved
3	LDC_CLK_ENABLE		LDC clock enable
		0	Disable
		1	Enable
2	CLKSEL_VENC		VENC clock select
		0	ENC_CLOCK 1
		1	ENC_CLOCK/2
1	Reserved	0	Any writes to these bit(s) must always have a value of 0
0	VPBE_CLK_ENABLE		OSD, VENC clock enable
		0	Disable
		1	Enable

Revision History

Changes from November 11, 2010 to June 17, 2016	Page
• Table 562: Corrected Description of LDC_CLK_SEL bit value = 0	571

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