Technical Reference Manual

AM261x Register Addendum

TEXAS INSTRUMENTS

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Table of Contents

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Read This First

About This Register Addendum

This Register Addendum (RA) provides detailed register references for each peripheral and subsystem in the device including:

- Register Address
- Register Name
- Register Types
- Register Reset Values
- Register Descriptions
- Bit-field Descriptions

This Register Addendum has been created in order to make the Technical Reference Manual a more effective and size-efficient collateral document. The AM263x Technical Reference Manual can be downloaded at https://www.ti.com/lit/SPRUJ17.

Note on Register Names

Note

This sections and the examples need to be read before proceeding to other chapters

Rev D now expands upon register name by prepending additional information to show where in the IP the register is located. There are three main types of locations. Examples are described below:

- Memory Related Registers
  - These registers are prefixed with *MEM*
  - Example: MEM_QSPI0_CSN0_CFG
- Configuration Related Registers
  - These registers are prefixed with *CFG*
  - Example: CFG0_ATTR_STATUS
- Region Specific Registers
  - These registers are prefixed with a name relating to the IP
  - Example 1: CPSW_VBUSP_REGS_INT_REGS_INT_SS_C0_TH_THRESH_PULSE_EN_REG means REGS_INT_REGS_INT_SS_C0_TH_THRESH_PULSE_EN_REG is related to CPSW_NCSS_VBUSP
  - Example 2: CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC_ECC_REV says CPSW's ECC_REG is related to CPSW_NCSS_VBUSP_CPSW_NC_CPSW_NC. Name to be shorter and aligned in a future revision.

This change in names is also followed by sub section headers and figure titles showing different naming conventions for the registers, but the header and figure are referring to the same register. The different naming conventions help legacy users search for registers. A future revision of this document can align the registers names.

Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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Related Documentation From Texas Instruments

For a complete listing of related documentation and development-support tools for the device, visit the Texas Instruments website at www.ti.com.

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AM263x Documentation

- AM263x Data sheet
- AM263x Errata
- AM263x Technical Reference Manual
  - Technical Reference Manual contains programming guides at the end of select IPs' chapters
- AM263x Register Addendum
- AM263x Hardware Design Guidelines

AM263x Software

- Sitara MCU+ Academy for AM263x
  - Texas Instruments offers the MCU+ Academy as a resource for designing with the MCU+ software and tools on supported devices.
  - The MCU+ Academy features easy-to-use training modules that range from the basics of getting started to advanced development topics.
- MCU-PLUS-SDK-AM263x

AM263x Product Folders

- AM2634 Product Folder
- AM2632 Product Folder
- AM2631 Product Folder

AM263x Evaluation Modules

- AM263x Control Card (TMDSCNCD263)
- AM263x LaunchPad (LP-AM263)

Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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Release History (Register Addendum)

The below table summarizes Register Addendum versions and changes.

Version	Literature Number	Date	Notes
*1	SPRUJ42*1	March 2022	Initial Creation
-	SPRUJ42	April 2022	Original Release Added Read This First Content

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Version	Literature Number	Date	Notes
A	SPRUJ42A	September 2022	Memory Map Updates: • Core-specific Memory Maps added Updates included for the following CTRLMMR Registers: • TOP_CTRL • MSS_CTRL • MSS_IOMUX • MSS_TOPRCM • MSS_RCM CONTROLSS_EPWM Register Descriptions Added Updates included for the following CONTROLSS Registers: • CONTROLSS_ADC* • CONTROLSS_CMPSS* • CONTROLSS_DAC • CONTROLSS_ECAP • CONTROLSS_EQEP • CONTROLSS_FSI* • CONTROLSS_GLOBAL_CTRL • CONTROLSS_*XBAR Updates included for the following SoC Registers • MSS_GPIO • MSS_LIN • MSS_SPINLOCK
B	SPRUJ42B	October 2022	Updates included for the following CTRLMMR Registers: • TOP_CTRL • MSS_CTRL • MSS_IOMUX • MSS_TOPRCM • MSS_RCM Updates included for the following CONTROLSS Registers: • CONTROLSS_CMPSS* • CONTROLSS_ECAP • CONTROLSS_EQEP • CONTROLSS_GLOBAL_CTRL • CONTROLSS_*XBAR Updates included for the following SoC Registers • XBAR and INTR Registers • MSS_*
C	SPRUJ42C	December 2022	Updates in general register description layout applied across document. PRU-ICSS Registers Added CONTROLSS_EPWM Registers Added Updates included for the following CTRLMMR Registers: • TOP_CTRL • MSS_CTRL • MSS_IOMUX • MSS_TOPRCM • MSS_RCM Updates included for the following SoC Registers • XBAR and INTR Registers • MSS_*

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Version	Literature Number	Date	Notes
D	SPRUJ42D	December 2023	• Aligned register reset values in tables and images • Update register names with nomenclature used in other register addendums – Uncompressed instances and registers in EPWM. – Removed "n" variable from register nomenclature from CMPSSA, CMPSSB, ECAP, EQEP, FSI_RX, FSI_TX, OTTOCAL, R5SS, DCC, MCAN, MCRC, RTI, UART, and SDFM • Adding missing figures. ESM, GPIO, I2C, and INPUTXBAR still need missing figures added • CPSW combined into one chapter • TCM, TCMA, TCMB, CCMR, and STC moved into R5SS_Core chapter • Combined TPTC and TPCC chapter into EDAM chapter • Removed chapter CTRLMMR_CONTROLSS_GLOBAL_CTRL which was one page linking to another chapter • MCAN chapters combined into one chapter • Changed AGG to AGGR • TSXBAR_INTR renamed to SoC_TIMESYNC_XBAR0 • SOC_TSXBAR_INTR chapter renamed to SoC_TIMESYNC_XBAR1 and moved to 3.24 • TOP PBIST renamed to PBIST with instance name of PBIST0 • CMPSS instances renamed to CMPSS12B. Names to align with CMPSSA in future revision • Global Control Registers have register name changes from epwm to etpwm and cmpssb to cmpss*b0. • Added GPMC, ELM, and WDT chatpers

1 Memory Map

This chapter summarizes the memory map address regions for the device.

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1.1 Device Memory Map

This section describes the device memory map.

Note

The memory locations not shown are either unallocated or reserved and not used.

Accesses to these locations are not recommended and must be avoided.

Table 1-1. AM263x Memory Map

Region Name	Start Address	End Address	Size
Core-specific Internal Memory Map [1]	0x0000 0000	0x1FFF FFFF	512MB
MCRC0	0x3500 0000	0x3500 03FF	1 KB
MPU_L2OCRAM_BANK0	0x4002 0000	0x4002 0FFF	4 KB
MPU_L2OCRAM_BANK1	0x4004 0000	0x4004 0FFF	4 KB
MPU_L2OCRAM_BANK2	0x4006 0000	0x4006 0FFF	4 KB
MPU_L2OCRAM_BANK3	0x4008 0000	0x4008 0FFF	4 KB
MPU_R5FSS0_CORE0_AXIS	0x400A 0000	0x400A 0FFF	4 KB
MPU_R5FSS0_CORE1_AXIS	0x400C 0000	0x400C 0FFF	4 KB
MPU_R5FSS1_CORE0_AXIS	0x400E 0000	0x400E 0FFF	4 KB
MPU_R5FSS1_CORE1_AXIS	0x4010 0000	0x4010 0FFF	4 KB
MPU_MBOX_SRAM	0x4014 0000	0x4014 0FFF	4 KB
MPU_QSPI0	0x4016 0000	0x4016 0FFF	4 KB
MPU_SCRM2SCRP0	0x4018 0000	0x4018 0FFF	4 KB
MPU_SCRM2SCRP1	0x401A 0000	0x401A 0FFF	4 KB
MPU_R5FSS0_CORE0_AHB	0x401C 0000	0x401C 0FFF	4 KB
MPU_R5FSS0_CORE1_AHB	0x401E 0000	0x401E 0FFF	4 KB
MPU_R5FSS1_CORE0_AHB	0x4020 0000	0x4020 0FFF	4 KB
MPU_R5FSS1_CORE1_AHB	0x4022 0000	0x4022 0FFF	4 KB
ICSS0_INTERNAL [1]	0x4800 0000	0x4803 FFFF	256 KB
ICSS0_ECC	0x4810 0000	0x4810 03FF	1 KB
QSPI0	0x4820 0000	0x4820 01FF	512 Bytes
MMC0	0x4830 0000	0x4830 1FFF	8 KB
GPMC0_CFG	0x4840 0000	0x4840 03FF	1 KB
CONTROLSS_G0_EPWM0	0x5000 0000	0x5000 0FFF	4 KB
CONTROLSS_G0_EPWM1	0x5000 1000	0x5000 1FFF	4 KB
CONTROLSS_G0_EPWM2	0x5000 2000	0x5000 2FFF	4 KB
CONTROLSS_G0_EPWM3	0x5000 3000	0x5000 3FFF	4 KB
CONTROLSS_G0_EPWM4	0x5000 4000	0x5000 4FFF	4 KB
CONTROLSS_G0_EPWM5	0x5000 5000	0x5000 5FFF	4 KB
CONTROLSS_G0_EPWM6	0x5000 6000	0x5000 6FFF	4 KB
CONTROLSS_G0_EPWM7	0x5000 7000	0x5000 7FFF	4 KB
CONTROLSS_G0_EPWM8	0x5000 8000	0x5000 8FFF	4 KB
CONTROLSS_G0_EPWM9	0x5000 9000	0x5000 9FFF	4 KB
CONTROLSS_G0_EPWM10	0x5000 A000	0x5000 AFFF	4 KB
CONTROLSS_G0_EPWM11	0x5000 B000	0x5000 BFFF	4 KB
CONTROLSS_G0_EPWM12	0x5000 C000	0x5000 CFFF	4 KB
CONTROLSS_G0_EPWM13	0x5000 D000	0x5000 DFFF	4 KB
CONTROLSS_G0_EPWM14	0x5000 E000	0x5000 EFFF	4 KB
CONTROLSS_G0_EPWM15	0x5000 F000	0x5000 FFFF	4 KB

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Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
CONTROLSS_G0_EPWM16	0x5001 0000	0x5001 0FFF	4 KB
CONTROLSS_G0_EPWM17	0x5001 1000	0x5001 1FFF	4 KB
CONTROLSS_G0_EPWM18	0x5001 2000	0x5001 2FFF	4 KB
CONTROLSS_G0_EPWM19	0x5001 3000	0x5001 3FFF	4 KB
CONTROLSS_G0_EPWM20	0x5001 4000	0x5001 4FFF	4 KB
CONTROLSS_G0_EPWM21	0x5001 5000	0x5001 5FFF	4 KB
CONTROLSS_G0_EPWM22	0x5001 6000	0x5001 6FFF	4 KB
CONTROLSS_G0_EPWM23	0x5001 7000	0x5001 7FFF	4 KB
CONTROLSS_G0_EPWM24	0x5001 8000	0x5001 8FFF	4 KB
CONTROLSS_G0_EPWM25	0x5001 9000	0x5001 9FFF	4 KB
CONTROLSS_G0_EPWM26	0x5001 A000	0x5001 AFFF	4 KB
CONTROLSS_G0_EPWM27	0x5001 B000	0x5001 BFFF	4 KB
CONTROLSS_G0_EPWM28	0x5001 C000	0x5001 CFFF	4 KB
CONTROLSS_G0_EPWM29	0x5001 D000	0x5001 DFFF	4 KB
CONTROLSS_G0_EPWM30	0x5001 E000	0x5001 EFFF	4 KB
CONTROLSS_G0_EPWM31	0x5001 F000	0x5001 FFFF	4 KB
CONTROLSS_G1_EPWM0	0x5004 0000	0x5004 0FFF	4 KB
CONTROLSS_G1_EPWM1	0x5004 1000	0x5004 1FFF	4 KB
CONTROLSS_G1_EPWM2	0x5004 2000	0x5004 2FFF	4 KB
CONTROLSS_G1_EPWM3	0x5004 3000	0x5004 3FFF	4 KB
CONTROLSS_G1_EPWM4	0x5004 4000	0x5004 4FFF	4 KB
CONTROLSS_G1_EPWM5	0x5004 5000	0x5004 5FFF	4 KB
CONTROLSS_G1_EPWM6	0x5004 6000	0x5004 6FFF	4 KB
CONTROLSS_G1_EPWM7	0x5004 7000	0x5004 7FFF	4 KB
CONTROLSS_G1_EPWM8	0x5004 8000	0x5004 8FFF	4 KB
CONTROLSS_G1_EPWM9	0x5004 9000	0x5004 9FFF	4 KB
CONTROLSS_G1_EPWM10	0x5004 A000	0x5004 AFFF	4 KB
CONTROLSS_G1_EPWM11	0x5004 B000	0x5004 BFFF	4 KB
CONTROLSS_G1_EPWM12	0x5004 C000	0x5004 CFFF	4 KB
CONTROLSS_G1_EPWM13	0x5004 D000	0x5004 DFFF	4 KB
CONTROLSS_G1_EPWM14	0x5004 E000	0x5004 EFFF	4 KB
CONTROLSS_G1_EPWM15	0x5004 F000	0x5004 FFFF	4 KB
CONTROLSS_G1_EPWM16	0x5005 0000	0x5005 0FFF	4 KB
CONTROLSS_G1_EPWM17	0x5005 1000	0x5005 1FFF	4 KB
CONTROLSS_G1_EPWM18	0x5005 2000	0x5005 2FFF	4 KB
CONTROLSS_G1_EPWM19	0x5005 3000	0x5005 3FFF	4 KB
CONTROLSS_G1_EPWM20	0x5005 4000	0x5005 4FFF	4 KB
CONTROLSS_G1_EPWM21	0x5005 5000	0x5005 5FFF	4 KB
CONTROLSS_G1_EPWM22	0x5005 6000	0x5005 6FFF	4 KB
CONTROLSS_G1_EPWM23	0x5005 7000	0x5005 7FFF	4 KB
CONTROLSS_G1_EPWM24	0x5005 8000	0x5005 8FFF	4 KB
CONTROLSS_G1_EPWM25	0x5005 9000	0x5005 9FFF	4 KB
CONTROLSS_G1_EPWM26	0x5005 A000	0x5005 AFFF	4 KB
CONTROLSS_G1_EPWM27	0x5005 B000	0x5005 BFFF	4 KB
CONTROLSS_G1_EPWM28	0x5005 C000	0x5005 CFFF	4 KB
CONTROLSS_G1_EPWM29	0x5005 D000	0x5005 DFFF	4 KB
CONTROLSS_G1_EPWM30	0x5005 E000	0x5005 EFFF	4 KB

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Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
CONTROLSS_G1_EPWM31	0x5005 F000	0x5005 FFFF	4 KB
CONTROLSS_G2_EPWM0	0x5008 0000	0x5008 0FFF	4 KB
CONTROLSS_G2_EPWM1	0x5008 1000	0x5008 1FFF	4 KB
CONTROLSS_G2_EPWM2	0x5008 2000	0x5008 2FFF	4 KB
CONTROLSS_G2_EPWM3	0x5008 3000	0x5008 3FFF	4 KB
CONTROLSS_G2_EPWM4	0x5008 4000	0x5008 4FFF	4 KB
CONTROLSS_G2_EPWM5	0x5008 5000	0x5008 5FFF	4 KB
CONTROLSS_G2_EPWM6	0x5008 6000	0x5008 6FFF	4 KB
CONTROLSS_G2_EPWM7	0x5008 7000	0x5008 7FFF	4 KB
CONTROLSS_G2_EPWM8	0x5008 8000	0x5008 8FFF	4 KB
CONTROLSS_G2_EPWM9	0x5008 9000	0x5008 9FFF	4 KB
CONTROLSS_G2_EPWM10	0x5008 A000	0x5008 AFFF	4 KB
CONTROLSS_G2_EPWM11	0x5008 B000	0x5008 BFFF	4 KB
CONTROLSS_G2_EPWM12	0x5008 C000	0x5008 CFFF	4 KB
CONTROLSS_G2_EPWM13	0x5008 D000	0x5008 DFFF	4 KB
CONTROLSS_G2_EPWM14	0x5008 E000	0x5008 EFFF	4 KB
CONTROLSS_G2_EPWM15	0x5008 F000	0x5008 FFFF	4 KB
CONTROLSS_G2_EPWM16	0x5009 0000	0x5009 0FFF	4 KB
CONTROLSS_G2_EPWM17	0x5009 1000	0x5009 1FFF	4 KB
CONTROLSS_G2_EPWM18	0x5009 2000	0x5009 2FFF	4 KB
CONTROLSS_G2_EPWM19	0x5009 3000	0x5009 3FFF	4 KB
CONTROLSS_G2_EPWM20	0x5009 4000	0x5009 4FFF	4 KB
CONTROLSS_G2_EPWM21	0x5009 5000	0x5009 5FFF	4 KB
CONTROLSS_G2_EPWM22	0x5009 6000	0x5009 6FFF	4 KB
CONTROLSS_G2_EPWM23	0x5009 7000	0x5009 7FFF	4 KB
CONTROLSS_G2_EPWM24	0x5009 8000	0x5009 8FFF	4 KB
CONTROLSS_G2_EPWM25	0x5009 9000	0x5009 9FFF	4 KB
CONTROLSS_G2_EPWM26	0x5009 A000	0x5009 AFFF	4 KB
CONTROLSS_G2_EPWM27	0x5009 B000	0x5009 BFFF	4 KB
CONTROLSS_G2_EPWM28	0x5009 C000	0x5009 CFFF	4 KB
CONTROLSS_G2_EPWM29	0x5009 D000	0x5009 DFFF	4 KB
CONTROLSS_G2_EPWM30	0x5009 E000	0x5009 EFFF	4 KB
CONTROLSS_G2_EPWM31	0x5009 F000	0x5009 FFFF	4 KB
CONTROLSS_G3_EPWM0	0x500C 0000	0x500C 0FFF	4 KB
CONTROLSS_G3_EPWM1	0x500C 1000	0x500C 1FFF	4 KB
CONTROLSS_G3_EPWM2	0x500C 2000	0x500C 2FFF	4 KB
CONTROLSS_G3_EPWM3	0x500C 3000	0x500C 3FFF	4 KB
CONTROLSS_G3_EPWM4	0x500C 4000	0x500C 4FFF	4 KB
CONTROLSS_G3_EPWM5	0x500C 5000	0x500C 5FFF	4 KB
CONTROLSS_G3_EPWM6	0x500C 6000	0x500C 6FFF	4 KB
CONTROLSS_G3_EPWM7	0x500C 7000	0x500C 7FFF	4 KB
CONTROLSS_G3_EPWM8	0x500C 8000	0x500C 8FFF	4 KB
CONTROLSS_G3_EPWM9	0x500C 9000	0x500C 9FFF	4 KB
CONTROLSS_G3_EPWM10	0x500C A000	0x500C AFFF	4 KB
CONTROLSS_G3_EPWM11	0x500C B000	0x500C BFFF	4 KB
CONTROLSS_G3_EPWM12	0x500C C000	0x500C CFFF	4 KB
CONTROLSS_G3_EPWM13	0x500C D000	0x500C DFFF	4 KB

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Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
CONTROLSS_G3_EPWM14	0x500C E000	0x500C EFFF	4 KB
CONTROLSS_G3_EPWM15	0x500C F000	0x500C FFFF	4 KB
CONTROLSS_G3_EPWM16	0x500D 0000	0x500D 0FFF	4 KB
CONTROLSS_G3_EPWM17	0x500D 1000	0x500D 1FFF	4 KB
CONTROLSS_G3_EPWM18	0x500D 2000	0x500D 2FFF	4 KB
CONTROLSS_G3_EPWM19	0x500D 3000	0x500D 3FFF	4 KB
CONTROLSS_G3_EPWM20	0x500D 4000	0x500D 4FFF	4 KB
CONTROLSS_G3_EPWM21	0x500D 5000	0x500D 5FFF	4 KB
CONTROLSS_G3_EPWM22	0x500D 6000	0x500D 6FFF	4 KB
CONTROLSS_G3_EPWM23	0x500D 7000	0x500D 7FFF	4 KB
CONTROLSS_G3_EPWM24	0x500D 8000	0x500D 8FFF	4 KB
CONTROLSS_G3_EPWM25	0x500D 9000	0x500D 9FFF	4 KB
CONTROLSS_G3_EPWM26	0x500D A000	0x500D AFFF	4 KB
CONTROLSS_G3_EPWM27	0x500D B000	0x500D BFFF	4 KB
CONTROLSS_G3_EPWM28	0x500D C000	0x500D CFFF	4 KB
CONTROLSS_G3_EPWM29	0x500D D000	0x500D DFFF	4 KB
CONTROLSS_G3_EPWM30	0x500D E000	0x500D EFFF	4 KB
CONTROLSS_G3_EPWM31	0x500D F000	0x500D FFFF	4 KB
CONTROLSS_ADC0_RESULT	0x5010 0000	0x5010 0FFF	4 KB
CONTROLSS_ADC1_RESULT	0x5010 1000	0x5010 1FFF	4 KB
CONTROLSS_ADC2_RESULT	0x5010 2000	0x5010 2FFF	4 KB
CONTROLSS_ADC3_RESULT	0x5010 3000	0x5010 3FFF	4 KB
CONTROLSS_ADC4_RESULT	0x5010 4000	0x5010 4FFF	4 KB
CONTROLSS_CMPSSA0	0x5020 0000	0x5020 0FFF	4 KB
CONTROLSS_CMPSSA1	0x5020 1000	0x5020 1FFF	4 KB
CONTROLSS_CMPSSA2	0x5020 2000	0x5020 2FFF	4 KB
CONTROLSS_CMPSSA3	0x5020 3000	0x5020 3FFF	4 KB
CONTROLSS_CMPSSA4	0x5020 4000	0x5020 4FFF	4 KB
CONTROLSS_CMPSSA5	0x5020 5000	0x5020 5FFF	4 KB
CONTROLSS_CMPSSA6	0x5020 6000	0x5020 6FFF	4 KB
CONTROLSS_CMPSSA7	0x5020 7000	0x5020 7FFF	4 KB
CONTROLSS_CMPSSA8	0x5020 8000	0x5020 8FFF	4 KB
CONTROLSS_CMPSSA9	0x5020 9000	0x5020 9FFF	4 KB
CONTROLSS_CMPSSB0	0x5022 0000	0x5022 0FFF	4 KB
CONTROLSS_CMPSSB1	0x5022 1000	0x5022 1FFF	4 KB
CONTROLSS_CMPSSB2	0x5022 2000	0x5022 2FFF	4 KB
CONTROLSS_CMPSSB3	0x5022 3000	0x5022 3FFF	4 KB
CONTROLSS_CMPSSB4	0x5022 4000	0x5022 4FFF	4 KB
CONTROLSS_CMPSSB5	0x5022 5000	0x5022 5FFF	4 KB
CONTROLSS_CMPSSB6	0x5022 6000	0x5022 6FFF	4 KB
CONTROLSS_CMPSSB7	0x5022 7000	0x5022 7FFF	4 KB
CONTROLSS_CMPSSB8	0x5022 8000	0x5022 8FFF	4 KB
CONTROLSS_CMPSSB9	0x5022 9000	0x5022 9FFF	4 KB
CONTROLSS_ECAP0	0x5024 0000	0x5024 0FFF	4 KB
CONTROLSS_ECAP1	0x5024 1000	0x5024 1FFF	4 KB
CONTROLSS_ECAP2	0x5024 2000	0x5024 2FFF	4 KB
CONTROLSS_ECAP3	0x5024 3000	0x5024 3FFF	4 KB

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Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
CONTROLSS_ECAP4	0x5024 4000	0x5024 4FFF	4 KB
CONTROLSS_ECAP5	0x5024 5000	0x5024 5FFF	4 KB
CONTROLSS_ECAP6	0x5024 6000	0x5024 6FFF	4 KB
CONTROLSS_ECAP7	0x5024 7000	0x5024 7FFF	4 KB
CONTROLSS_ECAP8	0x5024 8000	0x5024 8FFF	4 KB
CONTROLSS_ECAP9	0x5024 9000	0x5024 9FFF	4 KB
CONTROLSS_DAC0	0x5026 0000	0x5026 0FFF	4 KB
CONTROLSS_SDFM0	0x5026 8000	0x5026 8FFF	4 KB
CONTROLSS_SDFM1	0x5026 9000	0x5026 9FFF	4 KB
CONTROLSS_EQEP0	0x5027 0000	0x5027 0FFF	4 KB
CONTROLSS_EQEP1	0x5027 1000	0x5027 1FFF	4 KB
CONTROLSS_EQEP2	0x5027 2000	0x5027 2FFF	4 KB
CONTROLSS_FSI0_TX0	0x5028 0000	0x5028 0FFF	4 KB
CONTROLSS_FSI0_TX1	0x5028 1000	0x5028 1FFF	4 KB
CONTROLSS_FSI0_RX0	0x5029 0000	0x5029 0FFF	4 KB
CONTROLSS_FSI0_RX1	0x5029 1000	0x5029 1FFF	4 KB
CONTROLSS_FSI1_TX2	0x502A 0000	0x502A 0FFF	4 KB
CONTROLSS_FSI1_TX3	0x502A 1000	0x502A 1FFF	4 KB
CONTROLSS_FSI1_RX2	0x502B 0000	0x502B 0FFF	4 KB
CONTROLSS_FSI1_RX3	0x502B 1000	0x502B 1FFF	4 KB
CONTROLSS_ADC0_CFG	0x502C 0000	0x502C 0FFF	4 KB
CONTROLSS_ADC1_CFG	0x502C 1000	0x502C 1FFF	4 KB
CONTROLSS_ADC2_CFG	0x502C 2000	0x502C 2FFF	4 KB
CONTROLSS_ADC3_CFG	0x502C 3000	0x502C 3FFF	4 KB
CONTROLSS_ADC4_CFG	0x502C 4000	0x502C 4FFF	4 KB
CONTROLSS_INPUTXBAR	0x502D 0000	0x502D 0FFF	4 KB
CONTROLSS_PWMXBAR	0x502D 1000	0x502D 1FFF	4 KB
CONTROLSS_PWMSYNCOUTXBAR	0x502D 2000	0x502D 2FFF	4 KB
CONTROLSS_MDLXBAR	0x502D 3000	0x502D 3FFF	4 KB
CONTROLSS_ICLXBAR	0x502D 4000	0x502D 4FFF	4 KB
CONTROLSS_INTXBAR	0x502D 5000	0x502D 5FFF	4 KB
CONTROLSS_DMAXBAR	0x502D 6000	0x502D 6FFF	4 KB
CONTROLSS_OUTPUTXBAR	0x502D 8000	0x502D 8FFF	4 KB
CONTROLSS_OTTOCAL0	0x502E 0000	0x502E 0FFF	4 KB
CONTROLSS_OTTOCAL1	0x502E 1000	0x502E 1FFF	4 KB
CONTROLSS_OTTOCAL2	0x502E 2000	0x502E 2FFF	4 KB
CONTROLSS_OTTOCAL3	0x502E 3000	0x502E 3FFF	4 KB
CONTROLSS_CTRL	0x502F 0000	0x502F 7FFF	32 KB
DEBUGSS	0x5080 0000	0x508F FFFF	1024 KB
MSS_CTRL	0x50D0 0000	0x50D3 FFFF	256 KB
TOP_CTRL	0x50D8 0000	0x50D8 7FFF	32 KB
SPINLOCK0	0x50E0 0000	0x50E0 7FFF	32 KB
VIM	0x50F0 0000	0x50F0 3FFF	16 KB
GPIO0	0x5200 0000	0x5200 00FF	256 Bytes
GPIO1	0x5200 1000	0x5200 10FF	256 Bytes
GPIO2	0x5200 2000	0x5200 20FF	256 Bytes
GPIO3	0x5200 3000	0x5200 30FF	256 Bytes

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Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
WDT0	0x5210 0000	0x5210 00FF	256 Bytes
WDT1	0x5210 1000	0x5210 10FF	256 Bytes
WDT2	0x5210 2000	0x5210 20FF	256 Bytes
WDT3	0x5210 3000	0x5210 30FF	256 Bytes
RTI0	0x5218 0000	0x5218 03FF	1 KB
RTI1	0x5218 1000	0x5218 13FF	1 KB
RTI2	0x5218 2000	0x5218 23FF	1 KB
RTI3	0x5218 3000	0x5218 33FF	1 KB
MCSPI0	0x5220 0000	0x5220 01FF	512 Bytes
MCSPI1	0x5220 1000	0x5220 11FF	512 Bytes
MCSPI2	0x5220 2000	0x5220 21FF	512 Bytes
MCSPI3	0x5220 3000	0x5220 31FF	512 Bytes
MCSPI4	0x5220 4000	0x5220 41FF	512 Bytes
UART0	0x5230 0000	0x5230 01FF	512 Bytes
UART1	0x5230 1000	0x5230 11FF	512 Bytes
UART2	0x5230 2000	0x5230 21FF	512 Bytes
UART3	0x5230 3000	0x5230 31FF	512 Bytes
UART4	0x5230 4000	0x5230 41FF	512 Bytes
UART5	0x5230 5000	0x5230 51FF	512 Bytes
LIN0	0x5240 0000	0x5240 00FF	256 Bytes
LIN1	0x5240 1000	0x5240 10FF	256 Bytes
LIN2	0x5240 2000	0x5240 20FF	256 Bytes
LIN3	0x5240 3000	0x5240 30FF	256 Bytes
LIN4	0x5240 4000	0x5240 40FF	256 Bytes
I2C0	0x5250 0000	0x5250 00FF	256 Bytes
I2C1	0x5250 1000	0x5250 10FF	256 Bytes
I2C2	0x5250 2000	0x5250 20FF	256 Bytes
I2C3	0x5250 3000	0x5250 30FF	256 Bytes
MCAN0_MSG_RAM	0x5260 0000	0x5260 7FFF	32 KB
MCAN0_CFG	0x5260 8000	0x5260 83FF	1 KB
MCAN1_MSG_RAM	0x5261 0000	0x5261 7FFF	32 KB
MCAN1_CFG	0x5261 8000	0x5261 83FF	1 KB
MCAN2_MSG_RAM	0x5262 0000	0x5262 7FFF	32 KB
MCAN2_CFG	0x5262 8000	0x5262 83FF	1 KB
MCAN3_MSG_RAM	0x5263 0000	0x5263 7FFF	32 KB
MCAN3_CFG	0x5263 8000	0x5263 83FF	1 KB
MCAN0_ECC	0x5270 0000	0x5270 03FF	1 KB
MCAN1_ECC	0x5270 1000	0x5270 13FF	1 KB
MCAN2_ECC	0x5270 2000	0x5270 23FF	1 KB
MCAN3_ECC	0x5270 3000	0x5270 33FF	1 KB
ELM0	0x527F 0000	0x527F 0FFF	4 KB
CPSW0	0x5280 0000	0x529F FFFF	2 MB
TPCC0	0x52A0 0000	0x52A0 7FFF	32 KB
TPTC00	0x52A4 0000	0x52A4 0FFF	4 KB
TPTC01	0x52A6 0000	0x52A6 0FFF	4 KB
DCC0	0x52B0 0000	0x52B0 00FF	256 Bytes
DCC1	0x52B0 1000	0x52B0 10FF	256 Bytes

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Table 1-1. AM263x Memory Map (continued)

Region Name	Start Address	End Address	Size
DCC2	0x52B0 2000	0x52B0 20FF	256 Bytes
DCC3	0x52B0 3000	0x52B0 30FF	256 Bytes
TOP_ESM	0x52D0 0000	0x52D0 0FFF	4 KB
SOC_TIMESYNC_XBAR0	0x52E0 0000	0x52E0 00FF	256 Bytes
EDMA_TRIG_XBAR	0x52E0 1000	0x52E0 11FF	512 Bytes
GPIO_INTR_XBAR	0x52E0 2000	0x52E0 23FF	1 KB
ICSS_INTR_XBAR	0x52E0 3000	0x52E0 30FF	256 Bytes
SOC_TIMESYNC_XBAR1	0x52E0 4000	0x52E0 43FF	1 KB
ECC_AGG_R5FSS0_CORE0	0x5300 0000	0x5300 03FF	1 KB
ECC_AGG_R5FSS0_CORE1	0x5300 3000	0x5300 33FF	1 KB
ECC_AGG_R5FSS1_CORE0	0x5300 4000	0x5300 43FF	1 KB
ECC_AGG_R5FSS1_CORE1	0x5300 7000	0x5300 73FF	1 KB
ECC_AGG_TOP	0x5301 0000	0x5301 03FF	1 KB
IOMUX	0x5310 0000	0x5310 0FFF	4 KB
TOP_RCM	0x5320 0000	0x5320 7FFF	32 KB
MSS_RCM	0x5320 8000	0x5320 FFFF	32 KB
R5FSS0_CCMR	0x5321 0000	0x5321 0FFF	4 KB
R5FSS1_CCMR	0x5321 1000	0x5321 1FFF	4 KB
TOP_PBIST	0x5330 0000	0x5330 03FF	1 KB
R5FSS0_STC	0x5350 0000	0x5350 01FF	512 Bytes
R5FSS1_STC	0x5351 0000	0x5351 01FF	512 Bytes
EXT_FLASH0	0x6000 0000	0x61FF FFFF	32 MB
EXT_FLASH1	0x6200 0000	0x63FF FFFF	32 MB
GPMC0_MEM	0x6800 0000	0x6FFF FFFF	128 MB
L2OCRAM	0x7000 0000	0x701F FFFF	2 MB
MBOX_SRAM	0x7200 0000	0x7200 3FFF	16 KB
R5FSS0_CORE0_ICACHE (4)	0x7400 0000	0x747F FFFF	16 KB (8 MB) (5)
R5FSS0_CORE0_DCACHE (4)	0x7480 0000	0x74FF FFFF	16 KB (8 MB) (5)
R5FSS0_CORE1_ICACHE (2) (4)	0x7500 0000	0x757F FFFF	16 KB (8 MB) (5)
R5FSS0_CORE1_DCACHE (2) (4)	0x7580 0000	0x75FF FFFF	16 KB (8 MB) (5)
R5FSS1_CORE0_ICACHE (4)	0x7600 0000	0x767F FFFF	16 KB (8 MB) (5)
R5FSS1_CORE0_DCACHE (4)	0x7680 0000	0x76FF FFFF	16 KB (8 MB) (5)
R5FSS1_CORE1_ICACHE (2) (4)	0x7700 0000	0x777F FFFF	16 KB (8 MB) (5)
R5FSS1_CORE1_DCACHE (2) (4)	0x7780 0000	0x77FF FFFF	16 KB (8 MB) (5)
R5FSS0_CORE0_TCMA (3) (4)	0x7800 0000	0x7800 FFFF (Lockstep) 0x7800 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5FSS0_CORE0_TCMB (3) (4)	0x7810 0000	0x7810 FFFF (Lockstep) 0x7810 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5FSS0_CORE1_TCMA (2) (4)	0x7820 0000	0x7820 7FFF	32 KB
R5FSS0_CORE1_TCMB (2) (4)	0x7830 0000	0x7830 7FFF	32 KB
R5FSS1_CORE0_TCMA (3) (4)	0x7840 0000	0x7840 FFFF (Lockstep) 0x7840 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5FSS1_CORE0_TCMB (3) (4)	0x7850 0000	0x7850 FFFF (Lockstep) 0x7850 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5FSS1_CORE1_TCMA (2) (4)	0x7860 0000	0x7860 7FFF	32 KB
R5FSS1_CORE1_TCMB (2) (4)	0x7870 0000	0x7870 7FFF	32 KB

(1) See core-specific tables for the internal memory map.

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(2) In Lockstep mode, the R5FSS*x* CORE**1** memory region is not accessible.
(3) The size of these memories changes based on Dual-Core vs Lockstep operation.
For more information about Dual-Core and Lockstep modes, see the *R5FSS* chapter.
For more information about ATCM and BTCM, see the *Tightly-Coupled Memories (TCM)* section within the *R5FSS* chapter.
(4) This memory region is used by each CPU core to access the TCM/Cache memory space of other CPU cores.
(5) Each R5FSS contains 16 KB i-cache and 16 KB d-cache. However, the system interconnect sees an 8 MB address range at ICACHE/DCACHE. Any core attempting to access more than 16 KB will wrap around and access the same cache multiple times.

1.2 R5FSS Memory Map

Table 1-2. R5FSS0-0 Memory Map

Region Name	Start Address	End Address	Size
R5SS0_CORE0_TCMA_ROM	0x0000 0000	0x0001 FFFF	128 KB
R5SS0_CORE0_TCMA_RAM	0x0002 0000	0x0002 FFFF (Lockstep) 0x0002 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5SS0_CORE0_TCMB_RAM	0x0008 0000	0x0008 FFFF (Lockstep) 0x0008 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5SS0_CORE0_VIM	0x50F0 0000	0x50F0 3FFF	16 KB
R5SS0_CORE0_WWDT (WDT0)	0x5210 0000	0x5210 00FF	256 Bytes
ROM to RAM Swap			
R5SS0_CORE0_TCMA_ROM	NA	NA	NA
R5SS0_CORE0_TCMA_RAM	0x0000 0000	0x0000 FFFF (Lockstep) 0x0000 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5SS0_CORE0_TCMB_RAM	0x0008 0000	0x0008 FFFF (Lockstep) 0x0008 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5SS0_CORE0_VIM	0x50F0 0000	0x50F0 3FFF	16 KB
R5SS0_CORE0_WWDT (WDT0)	0x5210 0000	0x5210 00FF	256 Bytes

Table 1-3. R5FSS0-1 Memory Map

Region Name	Start Address	End Address	Size
R5SS0_CORE1_TCMA_RAM	0x0000 0000	0x0000 7FFF	32 KB
R5SS0_CORE1_TCMB_RAM	0x0008 0000	0x0008 7FFF	32 KB
R5SS0_CORE1_VIM	0x50F0 0000	0x50F0 3FFF	16 KB
R5SS0_CORE1_WWDT (WDT1)	0x5210 1000	0x5210 10FF	256 Bytes

Table 1-4. R5FSS1-0 Memory Map

Region Name	Start Address	End Address	Size
R5SS1_CORE0_TCMA_RAM	0x0000 0000	0x0000 FFFF (Lockstep) 0x0000 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5SS1_CORE0_TCMB_RAM	0x0008 0000	0x0008 FFFF (Lockstep) 0x0008 7FFF (Dual Core)	64 KB (Lockstep) 32 KB (Dual Core)
R5SS1_CORE0_VIM	0x50F0 0000	0x50F0 3FFF	16 KB
R5SS1_CORE0_WWDT (WDT2)	0x5210 2000	0x5210 20FF	256 Bytes

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Table 1-5. R5FSS1-1 Memory Map

Region Name	Start Address	End Address	Size
R5SS1_CORE1_TCMA_RAM	0x0000 0000	0x0000 7FFF	32 KB
R5SS1_CORE1_TCMB_RAM	0x0008 0000	0x0008 7FFF	32 KB
R5SS1_CORE1_VIM	0x50F0 0000	0x50F0 3FFF	16 KB
R5SS1_CORE1_WWDT (WDT3)	0x5210 3000	0x5210 30FF	256 Bytes

1.3 PRU-ICSS Memory Map

Region Name	Start Address	End Address	Size
PRU-ICSS Data RAM0 (DRAM0)	0x0000 0000	0x0000 1FFF	8 KB
PRU-ICSS Data RAM1 (DRAM1)	0x0000 2000	0x0000 3FFF	8 KB
PRU-ICSS Data RAM2 (Shared DRAM2)	0x0001 0000	0x0001 FFFF	64 KB
PRU-ICSS INTC	0x0002 0000	0x0002 1FFF	8 KB
PRU-ICSS PRU0 Control	0x0002 2000	0x0002 23FF	1 KB
PRU-ICSS PRU0 Debug	0x0002 2400	0x0002 3FFF	7 KB
PRU-ICSS PRU1 Control	0x0002 4000	0x0002 43FF	1 KB
PRU-ICSS PRU1 Debug	0x0002 4400	0x0002 5FFF	7 KB
PRU-ICSS CFG	0x0002 6000	0x0002 6FFF	4 KB
PRU-ICSS ECC_CFG	0x0002 7000	0x0002 7FFF	4 KB
PRU-ICSS UART0	0x0002 8000	0x0002 9FFF	8 KB
PRU-ICSS Reserved	0x0002 A000	0x0002 BFFF	8 KB
PRU-ICSS Reserved	0x0002 C000	0x0002 DFFF	8 KB
PRU-ICSS IEP	0x0002 E000	0x0002 EFFF	8 KB
PRU-ICSS ECAP0	0x0003 0000	0x0003 1FFF	8 KB
PRU-ICSS MII_RT_CFG	0x0003 2000	0x0003 23FF	1 KB
PRU-ICSS MII_MDIO	0x0003 2400	0x0003 3FFF	7 KB
PRU-ICSS PRU0 IRAM	0x0003 4000	0x0003 7FFF	16 KB
PRU-ICSS PRU1 IRAM	0x0003 8000	0x0003 BFFF	16 KB

2 Control Module (CTRLMMR) Registers

The Control module is the main controller for top-level device behavior in various states. Module contains registers for configuration, bootstrap (SOP) signals, I/O terminal pad multiplexing, clock selection, and many others. There are various Control or (CTRLMMR) modules defined in this device:

General SoC Control Modules

- TOP_CTRL (CTRLMMR0): SoC-level configuration registers
- MSS_CTRL (CTRLMMR1): SoC and Peripheral-level configuration registers
- CONTROLSS_GLOBAL_CTRL (CTRLMMR2): CONTROLSS-level configuration registers including general control, reset, and clocking-related functions for the real time control subsystem (CONTROLSS))

Pad Configuration Control Modules

- MSS_IOMUX (PADCFG_CTRLMMR0): SoC-level terminal configuration control registers

Reset and Clocking Control Modules

- MSS_TOPRCM (RCM_CTRLMMR0): SoC-level Clock and Reset control registers
- MSS_RCM (RCM_CTRLMMR1): SoC and Peripheral-level Clock and Reset control registers

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2.1 MMR Write Protection

All Control Module MMR have a protection mechanism which prevents spurious writes from changing register values. LOCK0_KICK0 and LOCK0_KICK1 registers are used for this purpose. The sequence to unlock these MMR is as follows:

1. Write exact unlock value (Table 2-1) to <Control Module>LOCK0_KICK0:KEY field
2. Write exact unlock value (Table 2-1) to <Control Module>LOCK0_KICK1:KEY field

The sequence to lock the MMR is as follows:

1. Write zero (or anyother value other than the unlock value)Table 2-1) to <Control Module>LOCK0_KICK1:KEY field
2. Write zero (or anyother value other than the unlock value)Table 2-1) to <Control Module>LOCK0_KICK0:KEY field

- **Note**

  If the above sequence for locking the IOMUX is not followed, an AHB_WRITE_ERROR interrupt will occur (if enabled).

For example, to unlock Control Module MSS_CTRL the sequence is as below:

1. Write 0x01234567 to MSS_CTRL.LOCK0_KICK0:KEY
2. Write 0xFEDCBA8 to MSS_CTRL.LOCK0_KICK1:KEY

To lock the Control Module MSS_CTRL the sequence is as below:

1. Write 0x0 to MSS_CTRL.LOCK0_KICK1:KEY
2. Write 0x0 to MSS_CTRL.LOCK0_KICK0:KEY

Any writes to locked memory region will result in assertion of the MMR_ACCESS_ERR_WR event by the respective control modules. This assertion can be enabled or disabled by writing the appropriate value to <Control Module>.INTR_ENABLE.KICK_ERR_EN field.

The table below shows the values that must be written to the LOCK0_KICK0 and LOCK0_KICK1 registers to unlock the various Control modules' MMR.

Table 2-1. Kick Protection Register Unlock Values

Protected Register	LockKick Register	Unlock Value
TOP_CTRL	LOCK0_KICK0	0x01234567
	LOCK0_KICK1	0xFEDCBA8
MSS_CTRL	LOCK0_KICK0	0x01234567
	LOCK0_KICK1	0xFEDCBA8
CONTROLSS_CTRL	LOCK0_KICK0	0x01234567
	LOCK0_KICK1	0xFEDCBA8
TOP_RCM	LOCK0_KICK0	0x01234567
	LOCK0_KICK1	0xFEDCBA8
MSS_RCM	LOCK0_KICK0	0x01234567
	LOCK0_KICK1	0xFEDCBA8
IOMUX	LOCK0_KICK0	0x83E70B13
	LOCK0_KICK1	0x95A4F1E0

Note

To ensure that all registers from a given partition are write protected, software must always re-lock the protection mechanism after completing the register writes.

The kick protection registers described in this section are an exception and are not write protected by the protection mechanism.

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2.2 TOP_CTRL Registers

Table 2-2. TOP_CTRL Registers Base Address Table

Offset	Length	Acronym	TOP_CTRL Physical Address
20h	32	TOP_CTRL_EFUSE_UID0	50D8 0020h
24h	32	TOP_CTRL_EFUSE_UID1	50D8 0024h
28h	32	TOP_CTRL_EFUSE_UID2	50D8 0028h
2Ch	24	TOP_CTRL_EFUSE_UID3	50D8 002Ch
30h	16	TOP_CTRL_EFUSE_DEVICE_TYPE	50D8 0030h
38h	32	TOP_CTRL_EFUSE_JTAG_USERCODE_ID	50D8 0038h
500h	32	TOP_CTRL_MAC_ID0	50D8 0500h
504h	16	TOP_CTRL_MAC_ID1	50D8 0504h
C00h	8	TOP_CTRL_ADC_REFBUF0_CTRL	50D8 0C00h
C04h	8	TOP_CTRL_ADC_REFBUF1_CTRL	50D8 0C04h
C08h	16	TOP_CTRL_ADC_REF_COMP_CTRL	50D8 0C08h
C0Ch	8	TOP_CTRL_ADC_REF_GOOD_STATUS	50D8 0C0Ch
C10h	32	TOP_CTRL_VMON_CTRL	50D8 0C10h
C14h	16	TOP_CTRL_VMON_STAT	50D8 0C14h
C18h	8	TOP_CTRL_PMU_COARSE_STAT	50D8 0C18h
C20h	16	TOP_CTRL_MASK_VMON_ERROR_ESM_H	50D8 0C20h
C24h	16	TOP_CTRL_MASK_VMON_ERROR_ESM_L	50D8 0C24h
C30h	8	TOP_CTRL_MASK_ANA_ISO	50D8 0C30h
C34h	8	TOP_CTRL_VMON_FILTER_CTRL	50D8 0C34h
D00h	32	TOP_CTRL_TSENSE_CFG	50D8 0D00h
D04h	8	TOP_CTRL_TSENSE_STATUS	50D8 0D04h
D08h	8	TOP_CTRL_TSENSE_STATUS_RAW	50D8 0D08h
D14h	24	TOP_CTRL_TSENSE0_ALERT	50D8 0D14h
D18h	24	TOP_CTRL_TSENSE0_CNTL	50D8 0D18h
D1Ch	16	TOP_CTRL_TSENSE0_RESULT	50D8 0D1Ch
D20h	32	TOP_CTRL_TSENSE0_DATA0	50D8 0D20h
D24h	32	TOP_CTRL_TSENSE0_DATA1	50D8 0D24h
D28h	32	TOP_CTRL_TSENSE0_DATA2	50D8 0D28h
D2Ch	32	TOP_CTRL_TSENSE0_DATA3	50D8 0D2Ch
D30h	32	TOP_CTRL_TSENSE0_ACCU	50D8 0D30h
D44h	24	TOP_CTRL_TSENSE1_ALERT	50D8 0D44h
D48h	24	TOP_CTRL_TSENSE1_CNTL	50D8 0D48h
D4Ch	16	TOP_CTRL_TSENSE1_RESULT	50D8 0D4Ch
D50h	32	TOP_CTRL_TSENSE1_DATA0	50D8 0D50h
D54h	32	TOP_CTRL_TSENSE1_DATA1	50D8 0D54h
D58h	32	TOP_CTRL_TSENSE1_DATA2	50D8 0D58h
D5Ch	32	TOP_CTRL_TSENSE1_DATA3	50D8 0D5Ch
D60h	32	TOP_CTRL_TSENSE1_ACCU	50D8 0D60h
D7Ch	16	TOP_CTRL_TSENSE2_RESULT	50D8 0D7Ch
DACh	16	TOP_CTRL_TSENSE3_RESULT	50D8 0DACh
1008h	8	TOP_CTRL_LOCK0_KICK0	50D8 1008h
100Ch	8	TOP_CTRL_LOCK0_KICK1	50D8 100Ch
1010h	8	TOP_CTRL_INTR_RAW_STATUS	50D8 1010h
1014h	8	TOP_CTRL_INTR_ENABLED_STATUS_CLEAR	50D8 1014h
1018h	8	TOP_CTRL_INTR_ENABLE	50D8 1018h

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Table 2-2. TOP_CTRL Registers Base Address Table (continued)

Offset	Length	Acronym	TOP_CTRL Physical Address
101Ch	32	TOP_CTRL_INTR_ENABLE_CLEAR	50D8 101Ch
1020h	8	TOP_CTRL_EOI	50D8 1020h
1024h	32	TOP_CTRL_FAULT_ADDRESS	50D8 1024h
1028h	0	TOP_CTRL_FAULT_TYPE_STATUS	50D8 1028h

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2.2.1 TOP_CTRL_EFUSE_UID0 Registers

2.2.1.1 TOP_EFUSE_UID0 Register (Offset = 20h) [reset = h]

Short Description: EFUSE_UID0 register

Long Description:

Return to Summary Table

Table 2-3. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0020h

Access Types Legend

Table 2-4. EFUSE_UID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RO	0h	EFUSE UID[31:0]

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2.2.2 TOP_CTRL_EFUSE_UID1 Registers

2.2.2.1 TOP_EFUSE_UID1 Register (Offset = 24h) [reset = h]

Short Description: EFUSE_UID1 register

Long Description:

Return to Summary Table

Table 2-5. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0024h

Access Types Legend

Table 2-6. EFUSE_UID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RO	0h	EFUSE UID[63:32]

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2.2.3 TOP_CTRL_EFUSE_UID2 Registers

2.2.3.1 TOP_EFUSE_UID2 Register (Offset = 28h) [reset = h]

Short Description: EFUSE_UID2 register

Long Description:

Return to Summary Table

Table 2-7. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0028h

Access Types Legend

Table 2-8. EFUSE_UID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RO	0h	EFUSE UID[95:64]

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2.2.4 TOP_CTRL_EFUSE_UID3 Registers

2.2.4.1 TOP_EFUSE_UID3 Register (Offset = 2Ch) [reset = h]

Short Description: EFUSE_UID3 register

Long Description:

Return to Summary Table

Table 2-9. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 002Ch

Access Types Legend

Table 2-10. EFUSE_UID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	VAL	RO	0h	EFUSE UID[120:96]

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2.2.5 TOP_CTRL_EFUSE_DEVICE_TYPE Registers

2.2.5.1 TOP_EFUSE_DEVICE_TYPE Register (Offset = 30h) [reset = h]

Short Description: EFUSE_DEVICE_TYPE register

Long Description:

Return to Summary Table

Table 2-11. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0030h

Access Types Legend

Table 2-12. EFUSE_DEVICE_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	VAL	RO	0h	EFUSE Device Type

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2.2.6 TOP_CTRL_EFUSE_JTAG_USERCODE_ID Registers

2.2.6.1 TOP_EFUSE_JTAG_USERCODE_ID Register (Offset = 38h) [reset = h]

Short Description: EFUSE_JTAG_USERCODE_ID register

Long Description:

Return to Summary Table

Table 2-13. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0038h

Access Types Legend

Table 2-14. EFUSE_JTAG_USERCODE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RO	0h	EFUSE JTAG_USER_CODE_ID[31:0];. Denotes part variant

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2.2.7 TOP_CTRL_MAC_ID0 Registers

2.2.7.1 TOP_MAC_ID0 Register (Offset = 500h) [reset = h]

Short Description: MAC_ID0 register

Long Description:

Return to Summary Table

Table 2-15. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0500h

Access Types Legend

Table 2-16. MAC_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MACID_LO	RO	0h	MAC ID low [32bits]

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2.2.8 TOP_CTRL_MAC_ID1 Registers

2.2.8.1 TOP_MAC_ID1 Register (Offset = 504h) [reset = h]

Short Description: MAC_ID1 register

Long Description:

Return to Summary Table

Table 2-17. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0504h

Access Types Legend

Table 2-18. MAC_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	MACID_HI	RO	0h	MAC ID high [16bits]

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2.2.9 TOP_CTRL_ADC_REFBUF0_CTRL Registers

2.2.9.1 TOP_ADC_REFBUF0_CTRL Register (Offset = C00h) [reset = h]

Short Description: ADC_REFBUF0_CTRL register

Long Description:

Return to Summary Table

Table 2-19. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C00h

Access Types Legend

Table 2-20. ADC_REFBUF0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ENABLE	RW	0h	Enables adc reference 0, mask hhv before enable 000: Disable 111: Enable

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2.2.10 TOP_CTRL_ADC_REFBUF1_CTRL Registers

2.2.10.1 TOP_ADC_REFBUF1_CTRL Register (Offset = C04h) [reset = h]

Short Description: ADC_REFBUF1_CTRL register

Long Description:

Return to Summary Table

Table 2-21. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C04h

Access Types Legend

Table 2-22. ADC_REFBUF1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ENABLE	RW	0h	Enables adc reference 0, mask hhv before enable 000: Disable 111: Enable

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2.2.11 TOP_CTRL_ADC_REF_COMP_CTRL Registers

2.2.11.1 TOP_ADC_REF_COMP_CTRL Register (Offset = C08h) [reset = h]

Short Description: ADC_REF_COMP_CTRL register

Long Description:

Return to Summary Table

Table 2-23. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C08h

Access Types Legend

Table 2-24. ADC_REF_COMP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 8	ADC34_REFOK_EN	RW	0h	enables reference comparators (ROK1). This monitors adc3 & adc4 refernc
	RESERVED	NONE		Reserved
6 - 4	ADC12_REFOK_EN	RW	0h	enables reference comparators (ROK0B). This monitors adc1 & adc2 refernce
	RESERVED	NONE		Reserved
2 - 0	ADC0_REFOK_EN	RW	0h	enables reference comparators (ROK0). This monitors adc0 refernce

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2.2.12 TOP_CTRL_ADC_REF_GOOD_STATUS Registers

2.2.12.1 TOP_ADC_REF_GOOD_STATUS Register (Offset = C0Ch) [reset = h]

Short Description: ADC_REF_GOOD_STATUS register

Long Description:

Return to Summary Table

Table 2-25. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C0Ch

Access Types Legend

Table 2-26. ADC_REF_GOOD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
5	ADC34_REF_UV_GOOD	RO	1h	Under Voltage check OK
4	ADC34_REF_OV_GOOD	RO	1h	Over voltage check OK
3	ADC12_REF_UV_GOOD	RO	1h	Under Voltage check OK
2	ADC12_REF_OV_GOOD	RO	1h	Over voltage check OK
1	ADC0_REF_UV_GOOD	RO	1h	Under Voltage check OK
0	ADC0_REF_OV_GOOD	RO	1h	Over voltage check OK

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2.2.13 TOP_CTRL_VMON_CTRL Registers

2.2.13.1 TOP_VMON_CTRL Register (Offset = C10h) [reset = h]

Short Description: VMON_CTRL register

Long Description:

Return to Summary Table

Table 2-27. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C10h

Access Types Legend

Table 2-28. VMON_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
26 - 24	CMP8_EN	RW	6Fh	VMON EN
	RESERVED	NONE		Reserved
22 - 20	CMP7_EN	RW	6Fh	VMON EN
	RESERVED	NONE		Reserved
18 - 16	CMP5_EN	RW	6Fh	VMON EN
	RESERVED	NONE		Reserved
14 - 12	CMP3_EN	RW	6Fh	VMON EN
	RESERVED	NONE		Reserved
10 - 8	CMP2_EN	RW	6Fh	VMON EN
	RESERVED	NONE		Reserved
6 - 4	CMP1_EN	RW	6Fh	VMON EN
	RESERVED	NONE		Reserved
2 - 0	CMP0_EN	RW	6Fh	VMON EN

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2.2.14 TOP_CTRL_VMON_STAT Registers

2.2.14.1 TOP_VMON_STAT Register (Offset = C14h) [reset = h]

Short Description: VMON_STAT register

Long Description:

Return to Summary Table

Table 2-29. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C14h

Access Types Legend

Table 2-30. VMON_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10	CMP8_UV_OK	RO	1h	VMON OK
9	CMP7_UV_OK	RO	1h	VMON OK
8	CMP5_UV_OK	RO	1h	VMON OK
7	CMP5_OV_OK	RO	1h	VMON OK
6	CMP3_UV_OK	RO	1h	VMON OK
5	CMP3_OV_OK	RO	1h	VMON OK
4	CMP2_UV_OK	RO	1h	VMON OK
3	CMP2_OV_OK	RO	1h	VMON OK
2	CMP1_UV_OK	RO	1h	VMON OK
1	CMP1_OV_OK	RO	1h	VMON OK
0	CMP0_UV_OK	RO	1h	VMON OK

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2.2.15 TOP_CTRL_PMU_COARSE_STAT Registers

2.2.15.1 TOP_PMU_COARSE_STAT Register (Offset = C18h) [reset = h]

Short Description: PMU_COARSE_STAT register

Long Description:

Return to Summary Table

Table 2-31. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C18h

Access Types Legend

Table 2-32. PMU_COARSE_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	VSUP18_RDY	RO	1h	Coarse VMON OK
2	VCORE_RDY	RO	1h	Coarse VMON OK
1	LDO_RDY	RO	1h	Coarse VMON OK
0	BG_RDY	RO	1h	Coarse VMON OK

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2.2.16 TOP_CTRL_MASK_VMON_ERROR_ESM_H Registers

2.2.16.1 TOP_MASK_VMON_ERROR_ESM_H Register (Offset = C20h) [reset = h]

Short Description: MASK_VMON_ERROR_ESM_H register

Long Description:

Return to Summary Table

Table 2-33. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C20h

Access Types Legend

Table 2-34. MASK_VMON_ERROR_ESM_H Register Field Descriptions

Bit	Field	Type	Reset	Description
16	ADC34_REF_UV_MASK	RW	1h	VMON Error Mask to ESM
15	ADC34_REF_OV_MASK	RW	1h	VMON Error Mask to ESM
14	ADC12_REF_UV_MASK	RW	1h	VMON Error Mask to ESM
13	ADC12_REF_OV_MASK	RW	1h	VMON Error Mask to ESM
12	ADC0_REF_UV_MASK	RW	1h	VMON Error Mask to ESM
11	ADC0_REF_OV_MASK	RW	1h	VMON Error Mask to ESM
10	CMP8_UV_ERR_MASK	RW	1h	VMON Error Mask to ESM
9	CMP7_UV_ERR_MASK	RW	1h	VMON Error Mask to ESM
8	CMP5_UV_ERR_MASK	RW	1h	VMON Error Mask to ESM
7	CMP5_OV_ERR_MASK	RW	1h	VMON Error Mask to ESM
6	CMP3_UV_ERR_MASK	RW	1h	VMON Error Mask to ESM
5	CMP3_OV_ERR_MASK	RW	1h	VMON Error Mask to ESM
4	CMP2_UV_ERR_MASK	RW	1h	VMON Error Mask to ESM
3	CMP2_OV_ERR_MASK	RW	1h	VMON Error Mask to ESM
2	CMP1_UV_ERR_NASK	RW	1h	VMON Error Mask to ESM
1	CMP1_OV_ERR_MASK	RW	1h	VMON Error Mask to ESM
0	CMP0_UV_ERR_MASK	RW	1h	VMON Error Mask to ESM

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2.2.17 TOP_CTRL_MASK_VMON_ERROR_ESM_L Registers

2.2.17.1 TOP_MASK_VMON_ERROR_ESM_L Register (Offset = C24h) [reset = h]

Short Description: MASK_VMON_ERROR_ESM_L register

Long Description:

Return to Summary Table

Table 2-35. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C24h

Access Types Legend

Table 2-36. MASK_VMON_ERROR_ESM_L Register Field Descriptions

Bit	Field	Type	Reset	Description
16	ADC34_REF_UV_MASK	RW	1h	VMON Error Mask to INTR
15	ADC34_REF_OV_MASK	RW	1h	VMON Error Mask to INTR
14	ADC12_REF_UV_MASK	RW	1h	VMON Error Mask to INTR
13	ADC12_REF_OV_MASK	RW	1h	VMON Error Mask to INTR
12	ADC0_REF_UV_MASK	RW	1h	VMON Error Mask to INTR
11	ADC0_REF_OV_MASK	RW	1h	VMON Error Mask to INTR
10	CMP8_UV_ERR_MASK	RW	1h	VMON Error Mask to INTR
9	CMP7_UV_ERR_MASK	RW	1h	VMON Error Mask to INTR
8	CMP5_UV_ERR_MASK	RW	1h	VMON Error Mask to INTR
7	CMP5_OV_ERR_MASK	RW	1h	VMON Error Mask to INTR
6	CMP3_UV_ERR_MASK	RW	1h	VMON Error Mask to INTR
5	CMP3_OV_ERR_MASK	RW	1h	VMON Error Mask to INTR
4	CMP2_UV_ERR_MASK	RW	1h	VMON Error Mask to INTR
3	CMP2_OV_ERR_MASK	RW	1h	VMON Error Mask to INTR
2	CMP1_UV_ERR_NASK	RW	1h	VMON Error Mask to INTR
1	CMP1_OV_ERR_MASK	RW	1h	VMON Error Mask to INTR
0	CMP0_UV_ERR_MASK	RW	1h	VMON Error Mask to INTR

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2.2.18 TOP_CTRL_MASK_ANA_ISO Registers

2.2.18.1 TOP_MASK_ANA_ISO Register (Offset = C30h) [reset = h]

Short Description: MASK_ANA_ISO register

Long Description:

Return to Summary Table

Table 2-37. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C30h

Access Types Legend

Table 2-38. MASK_ANA_ISO Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	MASK	RW	0h	Mask the Ana ISO generating SOC reset due to a glitch on VDD OK.Used during Trim updates to the analog or during ADC Refbuf enable

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2.2.19 TOP_CTRL_VMON_FILTER_CTRL Registers

2.2.19.1 TOP_VMON_FILTER_CTRL Register (Offset = C34h) [reset = h]

Short Description: VMON_FILTER_CTRL register

Long Description:

Return to Summary Table

Table 2-39. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0C34h

Access Types Legend

Table 2-40. VMON_FILTER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1 - 0	SELECT_VALUE	RW	0h	VMON FILTER control select00 : no filtering (default)01 : filtering for 4.8us10 : filtering for 9.6us11 : filtering for 14.4us

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2.2.20 TOP_CTRL_TSENSE_CFG Registers

2.2.20.1 TOP_TSENSE_CFG Register (Offset = D00h) [reset = h]

Short Description: TSENSE_CFG register

Long Description:

Return to Summary Table

Table 2-41. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D00h

Access Types Legend

Table 2-42. TSENSE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	TMPSOFF	RW	1h	Temperature sensor off 0 : on 1 : off
	RESERVED	NONE		Reserved
24	BGROFF	RW	1h	BandGap on/off control 0 : on 1 : off
	RESERVED	NONE		Reserved
20	AIPOFF	RW	1h	1 : iddq mode select 0 : normal mode
	RESERVED	NONE		Reserved
16	SNSR_MX_HIZ	RW	1h	sensor mux hiz control >0: normal operation. Mux will select either one of the analog sensor 1 : mux will be high impedance
	RESERVED	NONE		Reserved
13 - 8	DELAY	RW	0h	number of wait clock cycles between each TMPS Readout. Configure a Non zero value as delay value since configuring 0 is not allowed
7 - 4	SENSOR_SEL	RW	0h	Sensor Selection sensor enable bits for each sensor 0 : sensor disable 1 : sensor enablebit 3: temp_sensor3bit 2: temp_sensor2bit 1: temp_sensor1bit 0: temp_sensor0
	RESERVED	NONE		Reserved
0	ENABLE	RW	0h	Temperature controller enable

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2.2.21 TOP_CTRL_TSENSE_STATUS Registers

2.2.21.1 TOP_TSENSE_STATUS Register (Offset = D04h) [reset = h]

Short Description: TSENSE_STATUS register

Long Description:

Return to Summary Table

Table 2-43. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D04h

Access Types Legend

Table 2-44. TSENSE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	S1_COLD	RO	0h	Temperature Sensor 1 cold event detect 0: event not occurred 1: event occurred
5	S1_HOT	RO	0h	Temperature Sensor 1 hot event detect 0: event not occurred 1: event occurred
4	S1_LOW_THRHLD	RO	0h	Temperature Sensor 1 low event detect 0: event not occurred 1: event occurred
	RESERVED	NONE		Reserved
2	S0_COLD	RO	0h	Temperature Sensor 0 cold event detect 0: event not occurred 1: event occurred
1	S0_HOT	RO	0h	Temperature Sensor 0 hot event detect 0: event not occurred 1: event occurred
0	S0_LOW_THRHLD	RO	0h	Temperature Sensor 0 low event detect 0: event not occurred 1: event occurred

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2.2.22 TOP_CTRL_TSENSE_STATUS_RAW Registers

2.2.22.1 TOP_TSENSE_STATUS_RAW Register (Offset = D08h) [reset = h]

Short Description: TSENSE_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-45. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D08h

Access Types Legend

Table 2-46. TSENSE_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	S1_COLD	RO	0h	Temperature Sensor 1 cold event detect 0: event not occurred 1: event occurred
5	S1_HOT	RO	0h	Temperature Sensor 1 hot event detect 0: event not occurred 1: event occurred
4	S1_LOW_THRHLD	RO	0h	Temperature Sensor 1 low event detect 0: event not occurred 1: event occurred
	RESERVED	NONE		Reserved
2	S0_COLD	RO	0h	Temperature Sensor 0 cold event detect 0: event not occurred 1: event occurred
1	S0_HOT	RO	0h	Temperature Sensor 0 hot event detect 0: event not occurred 1: event occurred
0	S0_LOW_THRHLD	RO	0h	Temperature Sensor 1 low event detect 0: event not occurred 1: event occurred

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2.2.23 TOP_CTRL_TSENSE0_ALERT Registers

2.2.23.1 TOP_TSENSE0_ALERT Register (Offset = D14h) [reset = h]

Short Description: TSENSE0_ALERT register

Long Description:

Return to Summary Table

Table 2-47. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D14h

Access Types Legend

Table 2-48. TSENSE0_ALERT Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 16	ALERT_THRHLD_HOT	RW	0h	hot threshold/high temp threshold
	RESERVED	NONE		Reserved
7 - 0	ALERT_THRHLD_COLD	RW	0h	cold threshold/low temp threshold

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2.2.24 TOP_CTRL_TSENSE0_CNTL Registers

2.2.24.1 TOP_TSENSE0_CNTL Register (Offset = D18h) [reset = h]

Short Description: TSENSE0_CNTL register

Long Description:

Return to Summary Table

Table 2-49. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D18h

Access Types Legend

Table 2-50. TSENSE0_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
24	MASK_LOW_THRHLD	RW	0h	mask low threshold comparator output
	RESERVED	NONE		Reserved
20	MASK_COLD	RW	1h	mask cold comparator output
	RESERVED	NONE		Reserved
16	MASK_HOT	RW	0h	Mask hot comparator output
	RESERVED	NONE		Reserved
8	ACCU_CLEAR	RW	0h	accumulator clear
	RESERVED	NONE		Reserved
4	FIFO_FREEZE	RW	0h	fifo freeze
	RESERVED	NONE		Reserved
0	FIFO_CLEAR	RW	0h	fifo clear

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2.2.25 TOP_CTRL_TSENSE0_RESULT Registers

2.2.25.1 TOP_TSENSE0_RESULT Register (Offset = D1Ch) [reset = h]

Short Description: TSENSE0_RESULT register

Long Description:

Return to Summary Table

Table 2-51. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D1Ch

Access Types Legend

Table 2-52. TSENSE0_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
16	ECOZ	RO	0h	Conversion in Progress. 1: Conversion on going 0: Conversion completed
	RESERVED	NONE		Reserved
7 - 0	DTEMP	RO	0h	Temp Code readout

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2.2.26 TOP_CTRL_TSENSE0_DATA0 Registers

2.2.26.1 TOP_TSENSE0_DATA0 Register (Offset = D20h) [reset = h]

Short Description: TSENSE0_DATA0 register

Long Description:

Return to Summary Table

Table 2-53. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D20h

Access Types Legend

Table 2-54. TSENSE0_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	TAG	RO	0h	tag 0
7 - 0	DATA	RO	0h	fifo data 0

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2.2.27 TOP_CTRL_TSENSE0_DATA1 Registers

2.2.27.1 TOP_TSENSE0_DATA1 Register (Offset = D24h) [reset = h]

Short Description: TSENSE0_DATA1 register

Long Description:

Return to Summary Table

Table 2-55. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D24h

Access Types Legend

Table 2-56. TSENSE0_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	TAG	RO	0h	tag 1
7 - 0	DATA	RO	0h	fifo data 1

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2.2.28 TOP_CTRL_TSENSE0_DATA2 Registers

2.2.28.1 TOP_TSENSE0_DATA2 Register (Offset = D28h) [reset = h]

Short Description: TSENSE0_DATA2 register

Long Description:

Return to Summary Table

Table 2-57. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D28h

Access Types Legend

Table 2-58. TSENSE0_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	TAG	RO	0h	tag 2
7 - 0	DATA	RO	0h	fifo data 2

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2.2.29 TOP_CTRL_TSENSE0_DATA3 Registers

2.2.29.1 TOP_TSENSE0_DATA3 Register (Offset = D2Ch) [reset = h]

Short Description: TSENSE0_DATA3 register

Long Description:

Return to Summary Table

Table 2-59. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D2Ch

Access Types Legend

Table 2-60. TSENSE0_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	TAG	RO	0h	tag 3
7 - 0	DATA	RO	0h	fifo data 3

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2.2.30 TOP_CTRL_TSENSE0_ACCU Registers

2.2.30.1 TOP_TSENSE0_ACCU Register (Offset = D30h) [reset = h]

Short Description: TSENSE0_ACCU register

Long Description:

Return to Summary Table

Table 2-61. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D30h

Access Types Legend

Table 2-62. TSENSE0_ACCU Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CUMUL	RO	0h	cumulative sum of past DTEMPs

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2.2.31 TOP_CTRL_TSENSE1_ALERT Registers

2.2.31.1 TOP_TSENSE1_ALERT Register (Offset = D44h) [reset = h]

Short Description: TSENSE1_ALERT register

Long Description:

Return to Summary Table

Table 2-63. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D44h

Access Types Legend

Table 2-64. TSENSE1_ALERT Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 16	ALERT_THRHLD_HOT	RW	0h	hot threshold/high temp threshold
	RESERVED	NONE		Reserved
7 - 0	ALERT_THRHLD_COLD	RW	0h	cold threshold/low temp threshold

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2.2.32 TOP_CTRL_TSENSE1_CNTL Registers

2.2.32.1 TOP_TSENSE1_CNTL Register (Offset = D48h) [reset = h]

Short Description: TSENSE1_CNTL register

Long Description:

Return to Summary Table

Table 2-65. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D48h

Access Types Legend

Table 2-66. TSENSE1_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
24	MASK_LOW_THRHLD	RW	0h	mask low threshold comparator output
	RESERVED	NONE		Reserved
20	MASK_COLD	RW	1h	mask cold comparator output
	RESERVED	NONE		Reserved
16	MASK_HOT	RW	0h	Mask hot comparator output
	RESERVED	NONE		Reserved
8	ACCU_CLEAR	RW	0h	accumulator clear
	RESERVED	NONE		Reserved
4	FIFO_FREEZE	RW	0h	fifo freeze
	RESERVED	NONE		Reserved
0	FIFO_CLEAR	RW	0h	fifo clear

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2.2.33 TOP_CTRL_TSENSE1_RESULT Registers

2.2.33.1 TOP_TSENSE1_RESULT Register (Offset = D4Ch) [reset = h]

Short Description: TSENSE1_RESULT register

Long Description:

Return to Summary Table

Table 2-67. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D4Ch

Access Types Legend

Table 2-68. TSENSE1_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
16	ECOZ	RO	0h	Conversion in Progress. 1: Conversion on going 0: Conversion completed
	RESERVED	NONE		Reserved
7 - 0	DTEMP	RO	0h	Temp Code readout

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2.2.34 TOP_CTRL_TSENSE1_DATA0 Registers

2.2.34.1 TOP_TSENSE1_DATA0 Register (Offset = D50h) [reset = h]

Short Description: TSENSE1_DATA0 register

Long Description:

Return to Summary Table

Table 2-69. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D50h

Access Types Legend

Table 2-70. TSENSE1_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	TAG	RO	0h	tag 0
7 - 0	DATA	RO	0h	fifo data 0

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2.2.35 TOP_CTRL_TSENSE1_DATA1 Registers

2.2.35.1 TOP_TSENSE1_DATA1 Register (Offset = D54h) [reset = h]

Short Description: TSENSE1_DATA1 register

Long Description:

Return to Summary Table

Table 2-71. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D54h

Access Types Legend

Table 2-72. TSENSE1_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	TAG	RO	0h	tag 1
7 - 0	DATA	RO	0h	fifo data 1

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2.2.36 TOP_CTRL_TSENSE1_DATA2 Registers

2.2.36.1 TOP_TSENSE1_DATA2 Register (Offset = D58h) [reset = h]

Short Description: TSENSE1_DATA2 register

Long Description:

Return to Summary Table

Table 2-73. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D58h

Access Types Legend

Table 2-74. TSENSE1_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	TAG	RO	0h	tag 2
7 - 0	DATA	RO	0h	fifo data 2

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2.2.37 TOP_CTRL_TSENSE1_DATA3 Registers

2.2.37.1 TOP_TSENSE1_DATA3 Register (Offset = D5Ch) [reset = h]

Short Description: TSENSE1_DATA3 register

Long Description:

Return to Summary Table

Table 2-75. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D5Ch

Access Types Legend

Table 2-76. TSENSE1_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	TAG	RO	0h	tag 3
7 - 0	DATA	RO	0h	fifo data 3

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2.2.38 TOP_CTRL_TSENSE1_ACCU Registers

2.2.38.1 TOP_TSENSE1_ACCU Register (Offset = D60h) [reset = h]

Short Description: TSENSE1_ACCU register

Long Description:

Return to Summary Table

Table 2-77. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D60h

Access Types Legend

Table 2-78. TSENSE1_ACCU Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CUMUL	RO	0h	cumulative sum of past DTEMPs

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2.2.39 TOP_CTRL_TSENSE2_RESULT Registers

2.2.39.1 TOP_TSENSE2_RESULT Register (Offset = D7Ch) [reset = h]

Short Description: TSENSE2_RESULT register

Long Description:

Return to Summary Table

Table 2-79. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0D7Ch

Access Types Legend

Table 2-80. TSENSE2_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
16	ECOZ	RO	0h	Conversion in Progress. 1: Conversion on going 0: Conversion completed
	RESERVED	NONE		Reserved
7 - 0	DTEMP	RO	0h	Temp Code readout

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2.2.40 TOP_CTRL_TSENSE3_RESULT Registers

2.2.40.1 TOP_TSENSE3_RESULT Register (Offset = DACh) [reset = h]

Short Description: TSENSE3_RESULT register

Long Description:

Return to Summary Table

Table 2-81. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 0DACh

Access Types Legend

Table 2-82. TSENSE3_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
16	ECOZ	RO	0h	Conversion in Progress. 1: Conversion on going 0: conversion completed
	RESERVED	NONE		Reserved
7 - 0	DTEMP	RO	0h	Temp Code readout

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2.2.41 TOP_CTRL_LOCK0_KICK0 Registers

2.2.41.1 TOP_LOCK0_KICK0 Register (Offset = 1008h) [reset = h]

Short Description: - KICK0 component

Long Description:

Return to Summary Table

Table 2-83. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 1008h

Access Types Legend

Table 2-84. LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR	RW	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
2	KICK_ERR	RW	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
1	ADDR_ERR	RW	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
0	PROT_ERR	RW	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.

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2.2.42 TOP_CTRL_LOCK0_KICK1 Registers

2.2.42.1 TOP_LOCK0_KICK1 Register (Offset = 100Ch) [reset = h]

Short Description: - KICK1 component

Long Description:

Return to Summary Table

Table 2-85. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 100Ch

Access Types Legend

Table 2-86. LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	ENABLED_PROXY_ERR	RW	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
2	ENABLED_KICK_ERR	RW	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
1	ENABLED_ADDR_ERR	RW	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
0	ENABLED_PROT_ERR	RW	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.

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2.2.43 TOP_CTRL_INTR_RAW_STATUS Registers

2.2.43.1 TOP_INTR_RAW_STATUS Register (Offset = 1010h) [reset = h]

Short Description: Interrupt Raw Status/Set Register

Long Description:

Return to Summary Table

Table 2-87. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 1010h

Access Types Legend

Table 2-88. INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR_EN	RW	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
2	KICK_ERR_EN	RW	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN	RW	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
0	PROT_ERR_EN	RW	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.

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2.2.44 TOP_CTRL_INTR_ENABLED_STATUS_CLEAR Registers

2.2.44.1 TOP_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = h]

Short Description: Interrupt Enabled Status/Clear register

Long Description:

Return to Summary Table

Table 2-89. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 1014h

Access Types Legend

Table 2-90. INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR_EN_CLR	RW	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
2	KICK_ERR_EN_CLR	RW	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN_CLR	RW	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
0	PROT_ERR_EN_CLR	RW	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.

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2.2.45 TOP_CTRL_INTR_ENABLE Registers

2.2.45.1 TOP_INTR_ENABLE Register (Offset = 1018h) [reset = h]

Short Description: Interrupt Enable register

Long Description:

Return to Summary Table

Table 2-91. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 1018h

Access Types Legend

Table 2-92. INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	EOI_VECTOR	RW	0h	EOI vector value. Write this with interrupt distribution value in the chip.

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2.2.46 TOP_CTRL_INTR_ENABLE_CLEAR Registers

2.2.46.1 TOP_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = h]

Short Description: Interrupt Enable Clear register

Long Description:

Return to Summary Table

Table 2-93. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 101Ch

Access Types Legend

Table 2-94. INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FAULT_ADDR	RO	0h	Fault Address.

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2.2.47 TOP_CTRL_EOI Registers

2.2.47.1 TOP_EOI Register (Offset = 1020h) [reset = h]

Short Description: EOI register

Long Description:

Return to Summary Table

Table 2-95. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 1020h

Access Types Legend

Table 2-96. EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	FAULT_NS	RO	0h	Non-secure access.
5 - 0	FAULT_TYPE	RO	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype ! = 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault

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2.2.48 TOP_CTRL_FAULT_ADDRESS Registers

2.2.48.1 TOP_FAULT_ADDRESS Register (Offset = 1024h) [reset = h]

Short Description: Fault Address register

Long Description:

Return to Summary Table

Table 2-97. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 1024h

Access Types Legend

Table 2-98. FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	FAULT_XID	RO	0h	XID.
19 - 8	FAULT_ROUTEID	RO	0h	Route ID.
7 - 0	FAULT_PRIVID	RO	0h	Privilege ID.

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2.2.49 TOP_CTRL_FAULT_TYPE_STATUS Registers

2.2.49.1 TOP_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = h]

Short Description: Fault Type Status register

Long Description:

Return to Summary Table

Table 2-99. Instance Table

Instance Name	Physical Address
TOP_CTRL	50D8 1028h

Access Types Legend

Table 2-100. FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
0	FAULT_CLR	WO	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect.

2.2.50 Access Table

Table 2-101. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
WO	WO	Write

2.3 MSS_CTRL Registers

Table 2-102. MSS_CTRL Registers Base Address Table

Offset	Length	Acronym	MSS_CTRL Physical Address
20h	32	MSS_CTRL_R5SS0_CONTROL	50D0 0020h
24h	8	MSS_CTRL_R5SS0_CORE0_HALT	50D0 0024h
28h	8	MSS_CTRL_R5SS0_CORE1_HALT	50D0 0028h
2Ch	8	MSS_CTRL_R5SS0_STATUS_REG	50D0 002Ch
30h	8	MSS_CTRL_R5SS0_CORE0_STAT	50D0 0030h
34h	8	MSS_CTRL_R5SS0_CORE1_STAT	50D0 0034h
38h	8	MSS_CTRL_R5SS0_FORCE_WFI	50D0 0038h
40h	24	MSS_CTRL_R5SS1_CONTROL	50D0 0040h
44h	8	MSS_CTRL_R5SS1_CORE0_HALT	50D0 0044h
48h	8	MSS_CTRL_R5SS1_CORE1_HALT	50D0 0048h
4Ch	8	MSS_CTRL_R5SS1_STATUS_REG	50D0 004Ch
50h	8	MSS_CTRL_R5SS1_CORE0_STAT	50D0 0050h
54h	8	MSS_CTRL_R5SS1_CORE1_STAT	50D0 0054h
58h	8	MSS_CTRL_R5SS1_FORCE_WFI	50D0 0058h
80h	16	MSS_CTRL_R5SS0_ROM_ECLIPSE	50D0 0080h
90h	0	MSS_CTRL_R5SS0_TEINIT	50D0 0090h
94h	0	MSS_CTRL_R5SS1_TEINIT	50D0 0094h
D8h	24	MSS_CTRL_R5SS0_TCM_ECC_WRENZ_EN	50D0 00D8h
DCh	24	MSS_CTRL_R5SS1_TCM_ECC_WRENZ_EN	50D0 00DCh
200h	0	MSS_CTRL_R5SS0_ATCM_MEM_INIT	50D0 0200h
204h	0	MSS_CTRL_R5SS0_ATCM_MEM_INIT_DONE	50D0 0204h

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Table 2-102. MSS_CTRL Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_CTRL Physical Address
208h	0	MSS_CTRL_R5SS0_ATCM_MEM_INIT_STATUS	50D0 0208h
210h	0	MSS_CTRL_R5SS0_BTCM_MEM_INIT	50D0 0210h
214h	0	MSS_CTRL_R5SS0_BTCM_MEM_INIT_DONE	50D0 0214h
218h	0	MSS_CTRL_R5SS0_BTCM_MEM_INIT_STATUS	50D0 0218h
220h	0	MSS_CTRL_R5SS1_ATCM_MEM_INIT	50D0 0220h
224h	0	MSS_CTRL_R5SS1_ATCM_MEM_INIT_DONE	50D0 0224h
228h	0	MSS_CTRL_R5SS1_ATCM_MEM_INIT_STATUS	50D0 0228h
230h	0	MSS_CTRL_R5SS1_BTCM_MEM_INIT	50D0 0230h
234h	0	MSS_CTRL_R5SS1_BTCM_MEM_INIT_DONE	50D0 0234h
238h	0	MSS_CTRL_R5SS1_BTCM_MEM_INIT_STATUS	50D0 0238h
240h	8	MSS_CTRL_L2IOCRAM_MEM_INIT	50D0 0240h
244h	8	MSS_CTRL_L2OCRAM_MEM_INIT_DONE	50D0 0244h
248h	8	MSS_CTRL_L2OCRAM_MEM_INIT_STATUS	50D0 0248h
250h	0	MSS_CTRL_MAILBOXRAM_MEM_INIT	50D0 0250h
254h	0	MSS_CTRL_MAILBOXRAM_MEM_INIT_DONE	50D0 0254h
258h	0	MSS_CTRL_MAILBOXRAM_MEM_INIT_STATUS	50D0 0258h
260h	0	MSS_CTRL_TPCC_MEM_INIT	50D0 0260h
264h	0	MSS_CTRL_TPCC_MEM_INIT_DONE	50D0 0264h
268h	0	MSS_CTRL_TPCC_MEMINIT_STATUS	50D0 0268h
300h	8	MSS_CTRL_TOP_PBIST_KEY_RST	50D0 0300h
304h	32	MSS_CTRL_TOP_PBIST_REG0	50D0 0304h
308h	32	MSS_CTRL_TOP_PBIST_REG1	50D0 0308h
30Ch	32	MSS_CTRL_TOP_PBIST_REG2	50D0 030Ch
400h	16	MSS_CTRL_R5SS0_CTI_TRIG_SEL	50D0 0400h
404h	16	MSS_CTRL_R5SS1_CTI_TRIG_SEL	50D0 0404h
408h	32	MSS_CTRL_DBGSS_CTI_TRIG_SEL	50D0 0408h
40Ch	16	MSS_CTRL_DEBUGSS_CSETB_FLUSH	50D0 040Ch
410h	16	MSS_CTRL_DEBUGSS_STM_NSGUAREN	50D0 0410h
420h	8	MSS_CTRL_MCAN0_HALTEN	50D0 0420h
424h	8	MSS_CTRL_MCAN1_HALTEN	50D0 0424h
428h	8	MSS_CTRL_MCAN2_HALTEN	50D0 0428h
42Ch	8	MSS_CTRL_MCAN3_HALTEN	50D0 042Ch
430h	8	MSS_CTRL_LIN0_HALTEN	50D0 0430h
434h	8	MSS_CTRL_LIN1_HALTEN	50D0 0434h
438h	8	MSS_CTRL_LIN2_HALTEN	50D0 0438h
43Ch	8	MSS_CTRL_LIN3_HALTEN	50D0 043Ch
440h	8	MSS_CTRL_LIN4_HALTEN	50D0 0440h
444h	8	MSS_CTRL_I2C0_HALTEN	50D0 0444h
448h	8	MSS_CTRL_I2C1_HALTEN	50D0 0448h
44Ch	8	MSS_CTRL_I2C2_HALTEN	50D0 044Ch
450h	8	MSS_CTRL_I2C3_HALTEN	50D0 0450h
454h	8	MSS_CTRL_RTI0_HALTEN	50D0 0454h
458h	8	MSS_CTRL_RTI1_HALTEN	50D0 0458h
45Ch	8	MSS_CTRL_RTI2_HALTEN	50D0 045Ch
460h	8	MSS_CTRL_RTI3_HALTEN	50D0 0460h
474h	8	MSS_CTRL_CPSW_HALTEN	50D0 0474h
478h	8	MSS_CTRL_MCRC0_HALTEN	50D0 0478h

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Table 2-102. MSS_CTRL Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_CTRL Physical Address
800h	8	MSS_CTRL_TPTC_DBS_CONFIG	50D0 0800h
804h	16	MSS_CTRL_TPTC_BOUNDARY_CFG	50D0 0804h
808h	8	MSS_CTRL_TPTC_XID_REORDER_CFG	50D0 0808h
810h	24	MSS_CTRL_CPSW_CONTROL	50D0 0810h
814h	8	MSS_CTRL_QSPI_CONFIG	50D0 0814h
818h	0	MSS_CTRL_ICSSM_IDLE_CONTROL	50D0 0818h
81Ch	32	MSS_CTRL_ICSSM_PRU0_GPI_SEL	50D0 081Ch
820h	32	MSS_CTRL_ICSSM_PRU1_GPI_SEL	50D0 0820h
824h	32	MSS_CTRL_ICSSM_PRU0_GPIO_OUT_CTRL	50D0 0824h
828h	32	MSS_CTRL_ICSSM_PRU1_GPIO_OUT_CTRL	50D0 0828h
82Ch	16	MSS_CTRL_GPMC_CONTROL	50D0 082Ch
830h	24	MSS_CTRL_TPCC0_INTAGG_MASK	50D0 0830h
834h	24	MSS_CTRL_TPCC0_INTAGG_STATUS	50D0 0834h
838h	24	MSS_CTRL_TPCC0_INTAGG_STATUS_RAW	50D0 0838h
1008h	32	MSS_CTRL_LOCK0_KICK0	50D0 1008h
100Ch	32	MSS_CTRL_LOCK0_KICK1	50D0 100Ch
1010h	8	MSS_CTRL_INTR_RAW_STATUS	50D0 1010h
1014h	8	MSS_CTRL_INTR_ENABLED_STATUS_CLEAR	50D0 1014h
1018h	8	MSS_CTRL_INTR_ENABLE	50D0 1018h
101Ch	8	MSS_CTRL_INTR_ENABLE_CLEAR	50D0 101Ch
1020h	8	MSS_CTRL_EOI	50D0 1020h
1024h	32	MSS_CTRL_FAULT_ADDRESS	50D0 1024h
1028h	8	MSS_CTRL_FAULT_TYPE_STATUS	50D0 1028h
102Ch	32	MSS_CTRL_FAULT_ATTR_STATUS	50D0 102Ch
1030h	0	MSS_CTRL_FAULT_CLEAR	50D0 1030h
4000h	32	MSS_CTRL_R5SS0_CORE0_MBOX_WRITE_DONE	50D0 4000h
4004h	32	MSS_CTRL_R5SS0_CORE0_MBOX_READ_REQ	50D0 4004h
4008h	8	MSS_CTRL_R5SS0_CORE0_MBOX_READ_DONE_ACK	50D0 4008h
400Ch	32	MSS_CTRL_R5SS0_CORE0_MBOX_READ_DONE	50D0 400Ch
4010h	0	MSS_CTRL_R5SS0_CORE0_SW_INT	50D0 4010h
4020h	24	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK	50D0 4020h
4024h	24	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS	50D0 4024h
4028h	24	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW	50D0 4028h
4030h	24	MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CPU0_MASK	50D0 4030h
4034h	24	MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS	50D0 4034h
4038h	24	MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW	50D0 4038h
8000h	32	MSS_CTRL_R5SS0_CORE1_MBOX_WRITE_DONE	50D0 8000h
8004h	32	MSS_CTRL_R5SS0_CORE1_MBOX_READ_REQ	50D0 8004h
8008h	8	MSS_CTRL_R5SS0_CORE1_MBOX_READ_DONE_ACK	50D0 8008h
800Ch	32	MSS_CTRL_R5SS0_CORE1_MBOX_READ_DONE	50D0 800Ch
8010h	0	MSS_CTRL_R5SS0_CORE1_SW_INT	50D0 8010h
8020h	24	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK	50D0 8020h
8024h	24	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS	50D0 8024h

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Table 2-102. MSS_CTRL Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_CTRL Physical Address
8028h	24	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW	50D0 8028h
8030h	24	MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CPU1_MASK	50D0 8030h
8034h	24	MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS	50D0 8034h
8038h	24	MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW	50D0 8038h
C000h	32	MSS_CTRL_R5SS1_CORE0_MBOX_WRITE_DONE	50D0 C000h
C004h	32	MSS_CTRL_R5SS1_CORE0_MBOX_READ_REQ	50D0 C004h
C008h	8	MSS_CTRL_R5SS1_CORE0_MBOX_READ_DONE_ACK	50D0 C008h
C00Ch	32	MSS_CTRL_R5SS1_CORE0_MBOX_READ_DONE	50D0 C00Ch
C010h	0	MSS_CTRL_R5SS1_CORE0_SW_INT	50D0 C010h
C020h	24	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK	50D0 C020h
C024h	24	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS	50D0 C024h
C028h	24	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW	50D0 C028h
C030h	24	MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CPU0_MASK	50D0 C030h
C034h	24	MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS	50D0 C034h
C038h	24	MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW	50D0 C038h
10000h	32	MSS_CTRL_R5SS1_CORE1_MBOX_WRITE_DONE	50D1 0000h
10004h	32	MSS_CTRL_R5SS1_CORE1_MBOX_READ_REQ	50D1 0004h
10008h	8	MSS_CTRL_R5SS1_CORE1_MBOX_READ_DONE_ACK	50D1 0008h
1000Ch	32	MSS_CTRL_R5SS1_CORE1_MBOX_READ_DONE	50D1 000Ch
10010h	0	MSS_CTRL_R5SS1_CORE1_SW_INT	50D1 0010h
10020h	24	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK	50D1 0020h
10024h	24	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS	50D1 0024h
10028h	24	MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW	50D1 0028h
10030h	24	MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CPU1_MASK	50D1 0030h
10034h	24	MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS	50D1 0034h
10038h	24	MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW	50D1 0038h
14000h	32	MSS_CTRL_ICSSM_PRU0_MBOX_WRITE_DONE	50D1 4000h
14004h	32	MSS_CTRL_ICSSM_PRU0_MBOX_READ_REQ	50D1 4004h
14008h	8	MSS_CTRL_ICSSM_PRU0_MBOX_READ_DONE_ACK	50D1 4008h
1400Ch	32	MSS_CTRL_ICSSM_PRU0_MBOX_READ_DONE	50D1 400Ch
14010h	32	MSS_CTRL_ICSSM_PRU1_MBOX_WRITE_DONE	50D1 4010h
14014h	32	MSS_CTRL_ICSSM_PRU1_MBOX_READ_REQ	50D1 4014h
14018h	8	MSS_CTRL_ICSSM_PRU1_MBOX_READ_DONE_ACK	50D1 4018h
1401Ch	32	MSS_CTRL_ICSSM_PRU1_MBOX_READ_DONE	50D1 401Ch
18000h	32	MSS_CTRL_TPCC0_ERRAGG_MASK	50D1 8000h
18004h	32	MSS_CTRL_TPCC0_ERRAGG_STATUS	50D1 8004h
18008h	32	MSS_CTRL_TPCC0_ERRAGG_STATUS_RAW	50D1 8008h
18010h	16	MSS_CTRL_MMR_ACCESS_ERRAGG_MASK0	50D1 8010h
18014h	16	MSS_CTRL_MMR_ACCESS_ERRAGG_STATUS0	50D1 8014h

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Table 2-102. MSS_CTRL Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_CTRL Physical Address
18018h	16	MSS_CTRL_MMR_ACCESS_ERRAGG_STATUS_RAW0	50D1 8018h
18080h	8	MSS_CTRL_R5SS0_CPU0_ECC_CORR_ERRAGG_MASK	50D1 8080h
18084h	8	MSS_CTRL_R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS	50D1 8084h
18088h	8	MSS_CTRL_R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW	50D1 8088h
18090h	8	MSS_CTRL_R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK	50D1 8090h
18094h	8	MSS_CTRL_R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS	50D1 8094h
18098h	8	MSS_CTRL_R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW	50D1 8098h
180A0h	8	MSS_CTRL_R5SS0_CPU1_ECC_CORR_ERRAGG_MASK	50D1 80A0h
180A4h	8	MSS_CTRL_R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS	50D1 80A4h
180A8h	8	MSS_CTRL_R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW	50D1 80A8h
180B0h	8	MSS_CTRL_R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK	50D1 80B0h
180B4h	8	MSS_CTRL_R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS	50D1 80B4h
180B8h	8	MSS_CTRL_R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW	50D1 80B8h
180C0h	8	MSS_CTRL_R5SS1_CPU0_ECC_CORR_ERRAGG_MASK	50D1 80C0h
180C4h	8	MSS_CTRL_R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS	50D1 80C4h
180C8h	8	MSS_CTRL_R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW	50D1 80C8h
180D0h	8	MSS_CTRL_R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK	50D1 80D0h
180D4h	8	MSS_CTRL_R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS	50D1 80D4h
180D8h	8	MSS_CTRL_R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW	50D1 80D8h
180E0h	8	MSS_CTRL_R5SS1_CPU1_ECC_CORR_ERRAGG_MASK	50D1 80E0h
180E4h	8	MSS_CTRL_R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS	50D1 80E4h
180E8h	8	MSS_CTRL_R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW	50D1 80E8h
180F0h	8	MSS_CTRL_R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK	50D1 80F0h
180F4h	8	MSS_CTRL_R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS	50D1 80F4h
180F8h	8	MSS_CTRL_R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW	50D1 80F8h
18100h	8	MSS_CTRL_R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK	50D1 8100h
18104h	8	MSS_CTRL_R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS	50D1 8104h
18108h	8	MSS_CTRL_R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	50D1 8108h
18110h	8	MSS_CTRL_R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK	50D1 8110h

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Table 2-102. MSS_CTRL Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_CTRL Physical Address
18114h	8	MSS_CTRL_R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS	50D1 8114h
18118h	8	MSS_CTRL_R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	50D1 8118h
18120h	24	MSS_CTRL_R5SS0_TCM_ADDRPARITY_CLR	50D1 8120h
18124h	24	MSS_CTRL_R5SS0_CORE0_ADDRPARITY_ERR_ATCM	50D1 8124h
18128h	24	MSS_CTRL_R5SS0_CORE1_ADDRPARITY_ERR_ATCM	50D1 8128h
1812Ch	24	MSS_CTRL_R5SS0_CORE0_ERR_ADDRPARITY_B0TCM	50D1 812Ch
18130h	24	MSS_CTRL_R5SS0_CORE1_ERR_ADDRPARITY_B0TCM	50D1 8130h
18134h	24	MSS_CTRL_R5SS0_CORE0_ERR_ADDRPARITY_B1TCM	50D1 8134h
18138h	24	MSS_CTRL_R5SS0_CORE1_ERR_ADDRPARITY_B1TCM	50D1 8138h
1813Ch	24	MSS_CTRL_R5SS0_TCM_ADDRPARITY_ERRFORCE	50D1 813Ch
18140h	8	MSS_CTRL_R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK	50D1 8140h
18144h	8	MSS_CTRL_R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS	50D1 8144h
18148h	8	MSS_CTRL_R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	50D1 8148h
18150h	8	MSS_CTRL_R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK	50D1 8150h
18154h	8	MSS_CTRL_R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS	50D1 8154h
18158h	8	MSS_CTRL_R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	50D1 8158h
18160h	24	MSS_CTRL_R5SS1_TCM_ADDRPARITY_CLR	50D1 8160h
18164h	24	MSS_CTRL_R5SS1_CORE0_ADDRPARITY_ERR_ATCM	50D1 8164h
18168h	24	MSS_CTRL_R5SS1_CORE1_ADDRPARITY_ERR_ATCM	50D1 8168h
1816Ch	24	MSS_CTRL_R5SS1_CORE0_ERR_ADDRPARITY_B0TCM	50D1 816Ch
18170h	24	MSS_CTRL_R5SS1_CORE1_ERR_ADDRPARITY_B0TCM	50D1 8170h
18174h	24	MSS_CTRL_R5SS1_CORE0_ERR_ADDRPARITY_B1TCM	50D1 8174h
18178h	24	MSS_CTRL_R5SS1_CORE1_ERR_ADDRPARITY_B1TCM	50D1 8178h
1817Ch	24	MSS_CTRL_R5SS1_TCM_ADDRPARITY_ERRFORCE	50D1 817Ch
18180h	16	MSS_CTRL_TPCC0_PARITY_CTRL	50D1 8180h
18184h	8	MSS_CTRL_TPCC0_PARITY_STATUS	50D1 8184h

2.3.1 MSS_CTRL Registers

Address Offset	ShortName	Alternate Software Name	LongName	Description
0x20	R5SS0_CONTROL		R5SS0 Lock Step configure register	This register is used to configure R5SS0 in Lock step or Dual core mode. The mode change can be affected only once in a SOC power cycle
0x024	R5SS0_COREA_HALT	R5SS0_CORE0_HALT	R5SS0 Core 0 Halt Register	This register is used to Halt or Unhalt R5SS0 Core 0
0x028	R5SS0_COREB_HALT	R5SS0_CORE1_HALT	R5SS0 Core 1 Halt Register	This register is used to Halt or Unhalt R5SS0 Core 1
0x02C	R5SS0_STATUS_REG		R5SS0 Lock step Status register	This register shows whether R5SS0 is in Lock step or Dual core mode
0x030	R5SS0_CORE0_STAT		R5SS0 Core 0 Idle Status register	This register shows the WFI WFE status of R5SS0 Core 0
0x034	R5SS0_CORE1_STAT		R5SS0 Core 1 Idle Status register	This register shows the WFI WFE status of R5SS0 Core 1

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Address Offset	ShortName	Alternate Software Name	LongName	Description
0x038	MSS_STC_CONTROL0	R5SS0_FORCE_WFI	R5SS0 Force WFI register	This register is used to override and force WFI from R5SS0 to RCM
0x040	R5SS1_CONTROL		R5SS1 Lock Step configure register	This register is used to configure R5SS1 in Lock step or Dual core mode. The mode change can be affected only once in a SOC power cycle
0x044	R5SS1_COREA_HALT	R5SS1_CORE0_HALT	R5SS1 Core 0 Halt Register	This register is used to Halt or Unhalt R5SS1 Core 0
0x048	R5SS1_COREB_HALT	R5SS1_CORE1_HALT	R5SS1 Core 1 Halt Register	This register is used to Halt or Unhalt R5SS1 Core 1
0x04C	R5SS1_STATUS_REG		R5SS1 Lock step Status register	This register shows whether R5SS1 is in Lock step or Dual core mode
0x050	R5SS1_CORE0_STAT		R5SS1 Core 0 Idle Status register	This register shows the WFI WFE status of R5SS1 Core 0
0x054	R5SS1_CORE1_STAT		R5SS1 Core 1 Idle Status register	This register shows the WFI WFE status of R5SS1 Core 1
0x058	MSS_STC_CONTROL1	R5SS1_FORCE_WFI	R5SS1 Force WFI register	This register is used to override and force WFI from R5SS1 to RCM
0x090	R5SS[0]_GLOBAL_CONFIG	R5SS[0]_TEINIT	R5SS[0] Default exception state Register	This register is used to set the Exception state of R5SS[0] at reset
0x200	MSS_ATCM0_MEM_INIT	R5SS0_ATCM_MEM_INIT	R5SS0 ATCM Memory Initialisation Trigger Register	This register is used to initialise the data and ECC of ATCM memory of R5SS0
0x204	MSS_ATCM0_MEM_INIT_DONE	R5SS0_ATCM_MEM_INIT_DONE	R5SS0 ATCM Memory Initialisation Completion Register	This register is used to indicate the ATCM memory initialisation completion for R5SS0
0x208	MSS_ATCM0_MEM_INIT_STATUS	R5SS0_ATCM_MEM_INIT_STATUS	R5SS0 ATCM Memory Initialisation Status Register	This register is used to indicate the status of ongoing memory initialisation for ATCM memory of R5SS0
0x210	MSS_BTCM0_MEM_INIT	R5SS0_BTCM_MEM_INIT	R5SS0 BTCM Memory Initialisation Trigger Register	This register is used to initialise the data and ECC of BTCM memory of R5SS0
0x214	MSS_BTCM0_MEM_INIT_DONE	R5SS0_BTCM_MEM_INIT_DONE	R5SS0 BTCM Memory Initialisation Completion Register	This register is used to indicate the BTCM memory initialisation completion for R5SS0
0x218	MSS_BTCM0_MEM_INIT_STATUS	R5SS0_BTCM_MEM_INIT_STATUS	R5SS0 BTCM Memory Initialisation Status Register	This register is used to indicate the status of ongoing memory initialisation for BTCM memory of R5SS0
0x220	MSS_ATCM1_MEM_INIT	R5SS1_ATCM_MEM_INIT	R5SS1 ATCM Memory Initialisation Trigger Register	This register is used to initialise the data and ECC of ATCM memory of R5SS1
0x224	MSS_ATCM1_MEM_INIT_DONE	R5SS1_ATCM_MEM_INIT_DONE	R5SS1 ATCM Memory Initialisation Completion Register	This register is used to indicate the ATCM memory initialisation completion for R5SS1
0x228	MSS_ATCM1_MEM_INIT_STATUS	R5SS1_ATCM_MEM_INIT_STATUS	R5SS1 ATCM Memory Initialisation Status Register	This register is used to indicate the status of ongoing memory initialisation for ATCM memory of R5SS1
0x230	MSS_BTCM1_MEM_INIT	R5SS1_BTCM_MEM_INIT	R5SS1 BTCM Memory Initialisation Trigger Register	This register is used to initialise the data and ECC of BTCM memory of R5SS1
0x234	MSS_BTCM1_MEM_INIT_DONE	R5SS1_BTCM_MEM_INIT_DONE	R5SS1 BTCM Memory Initialisation Completion Register	This register is used to indicate the BTCM memory initialisation completion for R5SS1
0x238	MSS_BTCM1_MEM_INIT_STATUS	R5SS1_BTCM_MEM_INIT_STATUS	R5SS1 BTCM Memory Initialisation Status Register	This register is used to indicate the status of ongoing memory initialisation for BTCM memory of R5SS1
0x240	MSS_L2_MEM_INIT	L2IOCRAM_MEM_INIT	L2OCRAM Memory Initialisation Trigger Register	This register is used to initialise the data and ECC of L2OCRAM

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Address Offset	ShortName	Alternate Software Name	LongName	Description
0x244	MSS_L2_MEM_INIT_DONE	L2OCRAM_MEM_INIT_DONE	L2OCRAM Memory Initialisation Completion Register	This register is used to indicate the L2OCRAM memory initialisation completion
0x248	MSS_L2_MEM_INIT_STATUS	L2OCRAM_MEM_INIT_STATUS	L2OCRAM Memory Initialisation Status Register	This register is used to indicate the status of ongoing memory initialisation for L2OCRAM
0x250	MSS_MAILBOX_MEM_INIT	MAILBOXRAM_MEM_INIT	MBOX_SRAM Memory Initialisation Trigger Register	This register is used to initialise the data and ECC of MBOX_SRAM
0x254	MSS_MAILBOX_MEM_INIT_DONE	MAILBOXRAM_MEM_INIT_DONE	MBOX_SRAM Memory Initialisation Completion Register	This register is used to indicate the MBOX_SRAM memory initialisation completion
0x258	MSS_MAILBOX_MEM_INIT_STATUS	MAILBOXRAM_MEM_INIT_STATUS	MBOX_SRAM Memory Initialisation Status Register	This register is used to indicate the status of ongoing memory initialisation for MBOX_SRAM
0x260	MSS_TPCC_MEMINIT_START	TPCC_MEM_INIT	EDMA_TPCC Memory Initialisation Trigger Register	This register is used to initialise the data and ECC of EDMA_TPCC RAM
0x264	MSS_TPCC_MEMINIT_DONE	TPCC_MEM_INIT_DONE	EDMA_TPCC Memory Initialisation Completion Register	This register is used to indicate the EDMA_TPCC memory initialisation completion
0x268	MSS_TPCC_MEMINIT_STATUS	TPCC_MEMINIT_STATUS	EDMA_TPCC Memory Initialisation Status Register	This register is used to indicate the status of ongoing memory initialisation for EDMA_TPCC RAM
0x300	MSS_PBIST_KEY_RST	TOP_PBIST_KEY_RST	TOP Pbist Enable Register	This register is used to enable Top Pbist module
0x400	MSS_R5SS[0]_CTI_TRIG_SEL	R5SS[0]_CTI_TRIG_SEL	R5SS[0] CTI Trigger Selection Register	This register is used to select the two CTI trigger sources for R5SS[0]
0x408	MSS_DBGSS_CTI_TRIG_SEL	DBGSS_CTI_TRIG_SEL	DBGSS CTI Trigger Selection Register	This register is used to select thefour CTI trigger sources for DEBUGSS
0x40C	DEBUGSS_CSETB_FLUSH		ETB Control and Status Register	This register is used to generte the ETB flush request and indicate the ETB status
0x410	DEBUGSS_STM_NSGUAREN		STM Non Secure Gaurenteted Access Register	This register controls the behaviour of STM for Non secure guarenteed AXI access
0x420	CAN[0]_HALTEN	MCAN[0]_HALTEN	CAN[0] Halt Control Register	This register selects which R5 CPU when debug halted shall halt MCAN[0] Peripheral
0x430	LIN[0]_HALTEN		LIN[0]_HALTEN	This register selects which R5 CPU when debug halted shall halt LIN[0] Peripheral
0x444	I2C[0]_HALTEN		I2C[0]_HALTEN	This register selects which R5 CPU when debug halted shall halt I2C[0] Peripheral
0x454	RTI[0]_HALTEN		RTI[0]_HALTEN	This register selects which R5 CPU when debug halted shall halt RTI[0] Peripheral
0x474	CPSW_HALTEN		CPSW_HALTEN	This register selects which R5 CPU when debug halted shall halt CPSW Peripheral
0x478	CRC_HALTEN	MCRC0_HALTEN	CRC_HALTEN	This register selects which R5 CPU when debug halted shall halt MCRC Peripheral
0x800	TPTC_DBS_CONFIG		EDMA TCTC Default Burst size configuration Register	This register controls the default burst size of EDMA TPTC
0x810	CPSW_CONTROL		CPSW Mode Register	This register is used to control the CPSW Ethernet modes and additional controls on the IO
0x818	GLOBAL_CONTROLS	ICSSM_IDLE_CONTROL	ICSSM Idle Config Register	This register cofigures the Idle mode behaviour of ICSSM
0x81C	ICSSM_PRU0_GPI_SEL		PRU0 GPI SEL	Selects b/w Chip input or Control peripheral for ICSSM PRU0 GPI source
0x820	ICSSM_PRU1_GPI_SEL		PRU1 GPI SEL	Selects b/w Chip input or Control peripheral for ICSSM PRU1 GPI source

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Address Offset	ShortName	Alternate Software Name	LongName	Description
0x824	ICSSM_PRU0_GPIO_OUT_CTRL		ICSSM_PRU0_GPIO_OUT_CTRL	Controls the Output enable of the ICSSM PRU0 GPIO pins
0x828	ICSSM_PRU1_GPIO_OUT_CTRL		ICSSM_PRU1_GPIO_OUT_CTRL	Controls the Output enable of the ICSSM PRU1 GPIO pins
0x82C	GPMC_CONTROL		GPMC Clock Configuration Register	This register is used to configure the GPMC Clock source and Loop Back clock Source
0x830	MSS_TPCC_A_INTAGG_MASK	TPCC0_INTAGG_MASK	TPCC0 Aggregated Interrupt Mask Register	This register Masks selected interrupt soures from the Aggregated TPCC0 interrupt
0x834	MSS_TPCC_A_INTAGG_STATUS	TPCC0_INTAGG_STATUS	TPCC0 Aggregated Interrupt Status Register	This register shows the Status of Unmasked Interrupts from TPCC0
0x838	MSS_TPCC_A_INTAGG_STATUS_RAW	TPCC0_INTAGG_STATUS_RAW	TPCC0 Aggregated Interrupt Raw Status Register	This register shows the Status of all Interrupts from TPCC0
0x0	MSS_CR5A0_MBOX_WRITE_DONE	R5SS0_CORE0_MBOX_WRITE_DONE	R5SS0 CORE0 Mailbox Write Done Register	This register is used by R5SS0 Core 0 to generate Mailbox interrupt to Recipent CPU
0x04	MSS_CR5A0_MBOX_READ_REQ	R5SS0_CORE0_MBOX_READ_REQ	R5SS0 CORE0 Mailbox Read Request Register	This register is used by R5SS0 Core 0 to know the Sender of Mailbox Interrupt as well as clear it
0x08	MSS_CR5A0_MBOX_READ_DONE_ACK	R5SS0_CORE0_MBOX_READ_DONE_ACK	R5SS0 CORE0 Mailbox Read Acknowledge Register	This register is used by R5SS0 Core 0 to generate Mailbox Read acknowledgement to the Sender CPU
0x0C	MSS_CR5A0_MBOX_READ_DONE	R5SS0_CORE0_MBOX_READ_DONE	R5SS0 CORE0 Mailbox Read Completed Register	This register is used by R5SS0 Core 0 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt
0x10	MSS_SW_INT_R5SS0_CORE0	R5SS0_CORE0_SW_INT	R5SS0 CORE0 SW Interrupt Trigger Register	This Register is used to generate a S/W Triggered Interrupt to R5SS0 Core0
0x20	MPU_ADDR_INTR_ERRAGG0_MASK	MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK	MPU Aggregated Addr Error to R5SS0 CORE0 Mask Register	This register Masks selected interrupt soures from generating MPU Address Error Interrupt to R5SS0 CORE0
0x24	MPU_ADDR_INTR_ERRAGG0_STATUS	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS	MPU Aggregated Addr Error to R5SS0 CORE0 Status Register	This register shows the Status of Unmasked MPU Address Errors to R5SS0 Core0
0x28	MPU_ADDR_INTR_ERRAGG0_STATUS_RAW	MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW	MPU Aggregated Addr Error to R5SS0 CORE0 Raw Status Register	This register shows the Status of all MPU Address Errors
0x30	MPU_PROT_INTR_ERRAGG0_MASK	MPU_PROT_ERRAGG_R5SS0_CPU0_MASK	MPU Aggregated Prot Error to R5SS0 CORE0 Mask Register	This register Masks selected interrupt soures from generating MPU Protection Error Interrupt to R5SS0 CORE0
0x34	MPU_PROT_INTR_ERRAGG0_STATUS	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS	MPU Aggregated Prot Error to R5SS0 CORE0 Status Register	This register shows the Status of Unmasked MPU Protection Errors to R5SS0 Core0
0x38	MPU_PROT_INTR_ERRAGG0_STATUS_RAW	MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW	MPU Aggregated Prot Error to R5SS0 CORE0 Raw Status Register	This register shows the Status of all MPU Protection Errors
0x0	MSS_CR5B0_MBOX_WRITE_DONE	R5SS0_CORE1_MBOX_WRITE_DONE	R5SS0 CORE1 Mailbox Write Done Register	This register is used by R5SS0 Core 1 to generate Mailbox interrupt to Recipent CPU
0x04	MSS_CR5B0_MBOX_READ_REQ	R5SS0_CORE1_MBOX_READ_REQ	R5SS0 CORE1 Mailbox Read Request Register	This register is used by R5SS0 Core 1 to know the Sender of Mailbox Interrupt as well as clear it
0x08	MSS_CR5B0_MBOX_READ_DONE_ACK	R5SS0_CORE1_MBOX_READ_DONE_ACK	R5SS0 CORE1 Mailbox Read Acknowledge Register	This register is used by R5SS0 Core 1 to generate Mailbox Read acknowledgement to the Sender CPU

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Address Offset	ShortName	Alternate Software Name	LongName	Description
0x0C	MSS_CR5B0_MBOX_READ_DONE	R5SS0_CORE1_MBOX_READ_DONE	R5SS0 CORE1 Mailbox Read Completed Register	This register is used by R5SS0 Core 1 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt
0x10	MSS_SW_INT_R5SS0_CORE1	R5SS0_CORE1_SW_INT	R5SS0 CORE1 SW Interrupt Trigger Register	This Register is used to generate a S/W Triggered Interrupt to R5SS0 Core1
0x20	MPU_ADDR_INTR_ERRAGG1_MASK	MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK	MPU Aggregated Addr Error to R5SS0 CORE1 Mask Register	This register Masks selected interrupt soures from generating MPU Address Error Interrupt to R5SS0 CORE1
0x24	MPU_ADDR_INTR_ERRAGG1_STATUS	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS	MPU Aggregated Addr Error to R5SS0 CORE1 Status Register	This register shows the Status of Unmasked MPU Address Errors to R5SS0 CORE1
0x28	MPU_ADDR_INTR_ERRAGG1_STATUS_RAW	MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW	MPU Aggregated Addr Error to R5SS0 CORE1 Raw Status Register	This register shows the Status of all MPU Address Errors
0x30	MPU_PROT_INTR_ERRAGG1_MASK	MPU_PROT_ERRAGG_R5SS0_CPU1_MASK	MPU Aggregated Prot Error to R5SS0 CORE1 Mask Register	This register Masks selected interrupt soures from generating MPU Protection Error Interrupt to R5SS0 CORE1
0x34	MPU_PROT_INTR_ERRAGG1_STATUS	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS	MPU Aggregated Prot Error to R5SS0 CORE1 Status Register	This register shows the Status of Unmasked MPU Protection Errors to R5SS0 CORE1
0x38	MPU_PROT_INTR_ERRAGG1_STATUS_RAW	MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW	MPU Aggregated Prot Error to R5SS0 CORE1 Raw Status Register	This register shows the Status of all MPU Protection Errors
0x0	MSS_CR5A1_MBOX_WRITE_DONE	R5SS1_CORE0_MBOX_WRITE_DONE	R5SS1 CORE0 Mailbox Write Done Register	This register is used by R5SS1 Core 0 to generate Mailbox interrupt to Recipent CPU
0x04	MSS_CR5A1_MBOX_READ_REQ	R5SS1_CORE0_MBOX_READ_REQ	R5SS1 CORE0 Mailbox Read Request Register	This register is used by R5SS1 Core 0 to know the Sender of Mailbox Interrupt as well as clear it
0x08	MSS_CR5A1_MBOX_READ_DONE_ACK	R5SS1_CORE0_MBOX_READ_DONE_ACK	R5SS1 CORE0 Mailbox Read Acknowledge Register	This register is used by R5SS1 Core 0 to generate Mailbox Read acknowledgement to the Sender CPU
0x0C	MSS_CR5A1_MBOX_READ_DONE	R5SS1_CORE0_MBOX_READ_DONE	R5SS1 CORE0 Mailbox Read Completed Register	This register is used by R5SS1 Core 0 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt
0x10	MSS_SW_INT_R5SS1_CORE0	R5SS1_CORE0_SW_INT	R5SS1 CORE0 SW Interrupt Trigger Register	This Register is used to generate a S/W Triggered Interrupt to R5SS1 Core0
0x20	MPU_ADDR_INTR_ERRAGG2_MASK	MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK	MPU Aggregated Addr Error to R5SS1 CORE0 Mask Register	This register Masks selected interrupt soures from generating MPU Address Error Interrupt to R5SS1 CORE0
0x24	MPU_ADDR_INTR_ERRAGG2_STATUS	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS	MPU Aggregated Addr Error to R5SS1 CORE0 Status Register	This register shows the Status of Unmasked MPU Address Errors to R5SS1 Core0
0x28	MPU_ADDR_INTR_ERRAGG2_STATUS_RAW	MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW	MPU Aggregated Addr Error to R5SS1 CORE0 Raw Status Register	This register shows the Status of all MPU Address Errors
0x30	MPU_PROT_INTR_ERRAGG2_MASK	MPU_PROT_ERRAGG_R5SS1_CPU0_MASK	MPU Aggregated Prot Error to R5SS1 CORE0 Mask Register	This register Masks selected interrupt soures from generating MPU Protection Error Interrupt to R5SS1 CORE0
0x34	MPU_PROT_INTR_ERRAGG2_STATUS	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS	MPU Aggregated Prot Error to R5SS1 CORE0 Status Register	This register shows the Status of Unmasked MPU Protection Errors to R5SS1 Core0
0x38	MPU_PROT_INTR_ERRAGG2_STATUS_RAW	MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW	MPU Aggregated Prot Error to R5SS1 CORE0 Raw Status Register	This register shows the Status of all MPU Protection Errors

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Address Offset	ShortName	Alternate Software Name	LongName	Description
0x0	MSS_CR5B1_MBOX_WRITE_DONE	R5SS1_CORE1_MBOX_WRITE_DONE	R5SS1 CORE1 Mailbox Write Done Register	This register is used by R5SS1 Core 1 to generate Mailbox interrupt to Recipent CPU
0x04	MSS_CR5B1_MBOX_READ_REQ	R5SS1_CORE1_MBOX_READ_REQ	R5SS1 CORE1 Mailbox Read Request Register	This register is used by R5SS1 Core 1 to know the Sender of Mailbox Interrupt as well as clear it
0x08	MSS_CR5B1_MBOX_READ_DONE_ACK	R5SS1_CORE1_MBOX_READ_DONE_ACK	R5SS1 CORE1 Mailbox Read Acknowledge Register	This register is used by R5SS1 Core 1 to generate Mailbox Read acknowledgement to the Sender CPU
0x0C	MSS_CR5B1_MBOX_READ_DONE	R5SS1_CORE1_MBOX_READ_DONE	R5SS1 CORE1 Mailbox Read Completed Register	This register is used by R5SS1 Core 1 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt
0x10	MSS_SW_INT_R5SS1_CORE1	R5SS1_CORE1_SW_INT	R5SS1 CORE1 SW Interrupt Trigger Register	This Register is used to generate a S/W Triggered Interrupt to R5SS1 Core1
0x20	MPU_ADDR_INTR_ERRAGG3_MASK	MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK	MPU Aggregated Addr Error to R5SS1 CORE1 Mask Register	This register Masks selected interrupt soures from generating MPU Address Error Interrupt to R5SS1 CORE1
0x24	MPU_ADDR_INTR_ERRAGG3_STATUS	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS	MPU Aggregated Addr Error to R5SS1 CORE1 Status Register	This register shows the Status of Unmasked MPU Address Errors to R5SS1 CORE1
0x28	MPU_ADDR_INTR_ERRAGG3_STATUS_RAW	MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW	MPU Aggregated Addr Error to R5SS1 CORE1 Raw Status Register	This register shows the Status of all MPU Address Errors
0x30	MPU_PROT_INTR_ERRAGG3_MASK	MPU_PROT_ERRAGG_R5SS1_CPU1_MASK	MPU Aggregated Prot Error to R5SS1 CORE1 Mask Register	This register Masks selected interrupt soures from generating MPU Protection Error Interrupt to R5SS1 CORE1
0x34	MPU_PROT_INTR_ERRAGG3_STATUS	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS	MPU Aggregated Prot Error to R5SS1 CORE1 Status Register	This register shows the Status of Unmasked MPU Protection Errors to R5SS1 CORE1
0x38	MPU_PROT_INTR_ERRAGG3_STATUS_RAW	MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW	MPU Aggregated Prot Error to R5SS1 CORE1 Raw Status Register	This register shows the Status of all MPU Protection Errors
0x0	ICSSM_PRU0_MBOX_WRITE_DONE	ICSSM_PRU0_MBOX_WRITE_DONE	ICSSM PRU0 Mailbox Write Done Register	This register is used by ICSSM PRU0 to generate Mailbox interrupt to Recipent CPU
0x04	ICSSM_PRU0_MBOX_READ_REQ	ICSSM_PRU0_MBOX_READ_REQ	ICSSM PRU0 Mailbox Read Request Register	This register is used by ICSSM PRU0 to know the Sender of Mailbox Interrupt as well as clear it
0x08	ICSSM_PRU0_MBOX_READ_DONE_ACK	ICSSM_PRU0_MBOX_READ_DONE_ACK	ICSSM PRU0 Mailbox Read Acknowledge Register	This register is used by ICSSM PRU0 to generate Mailbox Read acknowledgement to the Sender CPU
0x0C	ICSSM_PRU0_MBOX_READ_DONE	ICSSM_PRU0_MBOX_READ_DONE	ICSSM PRU0 Mailbox Read Completed Register	This register is used by ICSSM PRU0 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt
0x10	ICSSM_PRU1_MBOX_WRITE_DONE	ICSSM_PRU1_MBOX_WRITE_DONE	ICSSM PRU1 Mailbox Write Done Register	This register is used by ICSSM PRU1 to generate Mailbox interrupt to Recipent CPU
0x14	ICSSM_PRU1_MBOX_READ_REQ	ICSSM_PRU1_MBOX_READ_REQ	ICSSM PRU1 Mailbox Read Request Register	This register is used by ICSSM PRU1 to know the Sender of Mailbox Interrupt as well as clear it
0x18	ICSSM_PRU1_MBOX_READ_DONE_ACK	ICSSM_PRU1_MBOX_READ_DONE_ACK	ICSSM PRU1 Mailbox Read Acknowledge Register	This register is used by ICSSM PRU1 to generate Mailbox Read acknowledgement to the Sender CPU
0x1C	ICSSM_PRU1_MBOX_READ_DONE	ICSSM_PRU1_MBOX_READ_DONE	ICSSM PRU1 Mailbox Read Completed Register	This register is used by ICSSM PRU1 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt

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Address Offset	ShortName	Alternate Software Name	LongName	Description
0x0	MSS_TPCC_A_ERRAGG_MASK	TPCC0_ERRAGG_MASK	TPCC0 Aggregated Error Mask Register	This register Masks selected interrupt soures from generating the Aggregated TPCC0 Error Interrupt
0x04	MSS_TPCC_A_ERRAGG_STATUS	TPCC0_ERRAGG_STATUS	TPCC0 Aggregated Error Status Register	This register shows the Status of Unmasked Errors from TPCC0
0x08	MSS_TPCC_A_ERRAGG_STATUS_RAW	TPCC0_ERRAGG_STATUS_RAW	TPCC0 Aggregated Error Raw Status Register	This register shows the Status of all Errors from TPCC0
0x10	MSS_PERIPH_ERRAGG_MASK0	MMR_ACCESS_ERRAGG_MASK	Aggregated MMR Access Error Mask Register	This register Masks selected interrupt soures from generating the Aggregated MMR Access Error Interrupt
0x14	MSS_PERIPH_ERRAGG_STATUS0	MMR_ACCESS_ERRAGG_STATUS	Aggregated MMR Access Error Status Register	This register shows the Status of Unmasked MMR Access Errors
0x18	MSS_PERIPH_ERRAGG_STATUS_RAW0	MMR_ACCESS_ERRAGG_STATUS_RAW	Aggregated MMR Access Error Raw Status Register	This register shows the Status of all MMR Access Errors
0x80	R5SS0_CPU0_ECC_CORR_ERRAGG_MASK	R5SS0_CORE0_ECC_CORR_ERRAGG_MASK	R5SS0 CORE0 Correctable ECC Error Mask Register	Register to Mask Correctable error from R5SS0 CORE0 Memories
0x84	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS	R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS	R5SS0 CORE0 Correctable ECC Error Status Register	Status register based on mask for correctable error R5SS0 CORE0 Memories
0x88	R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW	R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS_RAW	R5SS0 CORE0 Correctable ECC Error Raw Status Register	Raw status for correctable error from R5SS0 CORE0 Memories
0x90	R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK	R5SS0_CORE0_ECC_UNCORR_ERRAGG_MASK	R5SS0 CORE0 Uncorrectable ECC Error Mask Register	Register to Mask Uncorrectable error from R5SS0 CORE0 Memories
0x94	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS	R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS	R5SS0 CORE0 Uncorrectable ECC Error Status Register	Status register based on mask for uncorrectable error R5SS0 CORE0 Memories
0x98	R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW	R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW	R5SS0 CORE0 Uncorrectable ECC Error Raw Status Register	Raw status for uncorrectable error from R5SS0 CORE0 Memories
0xA0	R5SS0_CPU1_ECC_CORR_ERRAGG_MASK	R5SS0_CORE1_ECC_CORR_ERRAGG_MASK	R5SS0 CORE1 Correctable ECC Error Mask Register	Register to Mask Correctable error from R5SS0 CORE1 Memories
0xA4	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS	R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS	R5SS0 CORE1 Correctable ECC Error Status Register	Status register based on mask for correctable error R5SS0 CORE1 Memories
0xA8	R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW	R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS_RAW	R5SS0 CORE1 Correctable ECC Error Raw Status Register	Raw status for correctable error from R5SS0 CORE1 Memories
0xB0	R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK	R5SS0_CORE1_ECC_UNCORR_ERRAGG_MASK	R5SS0 CORE1 Uncorrectable ECC Error Mask Register	Register to Mask Uncorrectable error from R5SS0 CORE1 Memories
0xB4	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS	R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS	R5SS0 CORE1 Uncorrectable ECC Error Status Register	Status register based on mask for uncorrectable error R5SS0 CORE1 Memories

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Address Offset	ShortName	Alternate Software Name	LongName	Description
0xB8	R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW	R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW	R5SS0 CORE1 Uncorrectable ECC Error Raw Status Register	Raw status for uncorrectable error from R5SS0 CORE1 Memories
0xC0	R5SS1_CPU0_ECC_CORR_ERRAGG_MASK	R5SS1_CORE0_ECC_CORR_ERRAGG_MASK	R5SS1 CORE0 Correctable ECC Error Mask Register	Register to Mask Correctable error from R5SS1 CORE0 Memories
0xC4	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS	R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS	R5SS1 CORE0 Correctable ECC Error Status Register	Status register based on mask for correctable error R5SS1 CORE0 Memories
0xC8	R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW	R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS_RAW	R5SS1 CORE0 Correctable ECC Error Raw Status Register	Raw status for correctable error from R5SS1 CORE0 Memories
0xD0	R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK	R5SS1_CORE0_ECC_UNCORR_ERRAGG_MASK	R5SS1 CORE0 Uncorrectable ECC Error Mask Register	Register to Mask Uncorrectable error from R5SS1 CORE0 Memories
0xD4	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS	R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS	R5SS1 CORE0 Uncorrectable ECC Error Status Register	Status register based on mask for uncorrectable error R5SS1 CORE0 Memories
0xD8	R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW	R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW	R5SS1 CORE0 Uncorrectable ECC Error Raw Status Register	Raw status for uncorrectable error from R5SS1 CORE0 Memories
0xE0	R5SS1_CPU1_ECC_CORR_ERRAGG_MASK	R5SS1_CORE1_ECC_CORR_ERRAGG_MASK	R5SS1 CORE1 Correctable ECC Error Mask Register	Register to Mask Correctable error from R5SS1 CORE1 Memories
0xE4	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS	R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS	R5SS1 CORE1 Correctable ECC Error Status Register	Status register based on mask for correctable error R5SS1 CORE1 Memories
0xE8	R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW	R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS_RAW	R5SS1 CORE1 Correctable ECC Error Raw Status Register	Raw status for correctable error from R5SS1 CORE1 Memories
0xF0	R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK	R5SS1_CORE1_ECC_UNCORR_ERRAGG_MASK	R5SS1 CORE1 Uncorrectable ECC Error Mask Register	Register to Mask Uncorrectable error from R5SS1 CORE1 Memories
0xF4	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS	R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS	R5SS1 CORE1 Uncorrectable ECC Error Status Register	Status register based on mask for uncorrectable error R5SS1 CORE1 Memories
0xF8	R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW	R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW	R5SS1 CORE1 Uncorrectable ECC Error Raw Status Register	Raw status for uncorrectable error from R5SS1 CORE1 Memories
0x100	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK	R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_MASK	R5SS0 CORE0 TCM Address Parity Error Mask Register	Register to Mask TCM address parity errors from R5SS0 CORE0
0x104	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS	R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS	R5SS0 CORE0 TCM Address Parity Error Status Register	Status register based on mask for TCM address parity errors from R5SS0 CORE0

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Address Offset	ShortName	Alternate Software Name	LongName	Description
0x108	R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	R5SS0 CORE0 TCM Address Parity Error Raw Status Register	Raw status for TCM address parity errors from R5SS0 CORE0
0x110	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK	R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_MASK	R5SS0 CORE1 TCM Address Parity Error Mask Register	Register to Mask TCM address parity errors from R5SS0 CORE1
0x114	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS	R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS	R5SS0 CORE1 TCM Address Parity Error Status Register	Status register based on mask for TCM address parity errors from R5SS0 CORE1
0x118	R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	R5SS0 CORE1 TCM Address Parity Error Raw Status Register	Raw status for TCM address parity errors from R5SS0 CORE1
0x120	TCM0_PARITY_CTRL	R5SS0_TCM_ADDRPARITY_CLR	R5SS0 TCM Address Parity Error Clear Register	This register clears the TCM Address Parity Errors of R5SS0
0x124	ERR_PARITY_ATCM0_R5SS0	R5SS0_CORE0_ADDRPARITY_ERR_ATCM	R5SS0 CORE0 ATCM Address Parity Error Location Register	This register latches the ATCM Address where the Address Parity Error occurred in R5SS0 CORE0
0x128	ERR_PARITY_ATCM1_R5SS0	R5SS0_CORE1_ADDRPARITY_ERR_ATCM	R5SS0 CORE1 ATCM Address Parity Error Location Register	This register latches the ATCM Address where the Address Parity Error occurred in R5SS0 CORE1
0x12C	ERR_PARITY_B0TCM0_R5SS0	R5SS0_CORE0_ERR_ADDRPARITY_B0TCM	R5SS0 CORE0 B0TCM Address Parity Error Location Register	This register latches the B0TCM Address where the Address Parity Error occurred in R5SS0 CORE0
0x130	ERR_PARITY_B0TCM1_R5SS0	R5SS0_CORE1_ERR_ADDRPARITY_B0TCM	R5SS0 CORE1 B0TCM Address Parity Error Location Register	This register latches the B0TCM Address where the Address Parity Error occurred in R5SS0 CORE1
0x134	ERR_PARITY_B1TCM0_R5SS0	R5SS0_CORE0_ERR_ADDRPARITY_B1TCM	R5SS0 CORE0 B1TCM Address Parity Error Location Register	This register latches the B1TCM Address where the Address Parity Error occurred in R5SS0 CORE0
0x138	ERR_PARITY_B1TCM1_R5SS0	R5SS0_CORE1_ERR_ADDRPARITY_B1TCM	R5SS0 CORE1 B1TCM Address Parity Error Location Register	This register latches the B1TCM Address where the Address Parity Error occurred in R5SS0 CORE1
0x13C	TCM0_PARITY_ERRFRC	R5SS0_TCM_ADDRPARITY_ERRFORCE	R5SS0 TCM Address Parity Error Force Register	This register is used to Inject fault in the TCM Address Parity Error detection logic of R5SS0
0x140	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK	R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_MASK	R5SS1 CORE0 TCM Address Parity Error Mask Register	Register to Mask TCM address parity errors from R5SS1 CORE0
0x144	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS	R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS	R5SS1 CORE0 TCM Address Parity Error Status Register	Status register based on mask for TCM address parity errors from R5SS1 CORE0
0x148	R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	R5SS1_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	R5SS1 CORE0 TCM Address Parity Error Raw Status Register	Raw status for TCM address parity errors from R5SS1 CORE0
0x150	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK	R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_MASK	R5SS1 CORE1 TCM Address Parity Error Mask Register	Register to Mask TCM address parity errors from R5SS1 CORE1
0x154	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS	R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS	R5SS1 CORE1 TCM Address Parity Error Status Register	Status register based on mask for TCM address parity errors from R5SS1 CORE1

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0x158	R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	R5SS1_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW	R5SS1 CORE1 TCM Address Parity Error Raw Status Register	Raw status for TCM address parity errors from R5SS1 CORE1
0x160	TCM1_PARITY_CTRL	R5SS1_TCM_ADDRPARITY_CLR	R5SS1 TCM Address Parity Error Clear Register	This register clears the TCM Address Parity Errors of R5SS1
0x164	ERR_PARITY_ATCM0_R5SS1	R5SS1_CORE0_ADDRPARITY_ERR_ATCM	R5SS1 CORE0 ATCM Address Parity Error Location Register	This register latches the ATCM Address where the Address Parity Error occurred in R5SS1 CORE0
0x168	ERR_PARITY_ATCM1_R5SS1	R5SS1_CORE1_ADDRPARITY_ERR_ATCM	R5SS1 CORE1 ATCM Address Parity Error Location Register	This register latches the ATCM Address where the Address Parity Error occurred in R5SS1 CORE1
0x16C	ERR_PARITY_B0TCM0_R5SS1	R5SS1_CORE0_ERR_ADDRPARITY_B0TCM	R5SS1 CORE0 B0TCM Address Parity Error Location Register	This register latches the B0TCM Address where the Address Parity Error occurred in R5SS1 CORE0
0x170	ERR_PARITY_B0TCM1_R5SS1	R5SS1_CORE1_ERR_ADDRPARITY_B0TCM	R5SS1 CORE1 B0TCM Address Parity Error Location Register	This register latches the B0TCM Address where the Address Parity Error occurred in R5SS1 CORE1
0x174	ERR_PARITY_B1TCM0_R5SS1	R5SS1_CORE0_ERR_ADDRPARITY_B1TCM	R5SS1 CORE0 B1TCM Address Parity Error Location Register	This register latches the B1TCM Address where the Address Parity Error occurred in R5SS1 CORE0
0x178	ERR_PARITY_B1TCM1_R5SS1	R5SS1_CORE1_ERR_ADDRPARITY_B1TCM	R5SS1 CORE1 B1TCM Address Parity Error Location Register	This register latches the B1TCM Address where the Address Parity Error occurred in R5SS1 CORE1
0x17C	TCM1_PARITY_ERRFRC	R5SS1_TCM_ADDRPARITY_ERRFORCE	R5SS1 TCM Address Parity Error Force Register	This register is used to Inject fault in the TCM Address Parity Error detection logic of R5SS1
0x180	TPCC_PARITY_CTRL	TPCC0_PARITY_CTRL	EDMA TPCC0 Memory Parity Error Control Register	This register Controls the Parity Error detection logic of EDMA TPCC0 Memories
0x184	TPCC_PARITY_STATUS	TPCC0_PARITY_STATUS	EDMA TPCC0 Memory Parity Error Status Register	This register indicates the Address where the Parity Error occurred in TPCC0 Memory
0x200	MSS_BUS_SAFETY_CTRL	BUS_SAFETY_CTRL	Interconnect Safety Enable Register	This register is used to Globally enable Interconnect Safety
0x220	MSS_CR5A0_AXI_RD_BUS_SAFETY_CTRL	R5SS0_CORE0_AXI_RD_BUS_SAFETY_CTRL	R5SS0 CORE0 AXI_RD Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE0 AXI RD Initiator Port
0x224	MSS_CR5A0_AXI_RD_BUS_SAFETY_FI	R5SS0_CORE0_AXI_RD_BUS_SAFETY_FI	R5SS0 CORE0 AXI_RD Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE0 AXI RD Initiator Port
0x228	MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR	R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR	R5SS0 CORE0 AXI_RD Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE0 AXI RD Initiator port
0x22C	MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	R5SS0 CORE0 AXI_RD Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE0 AXI RD Initiator Port
0x230	MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	R5SS0 CORE0 AXI_RD Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE0 AXI RD Initiator Port
0x234	MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_STAT_READ	R5SS0_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ	R5SS0 CORE0 AXI_RD Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS0 CORE0 AXI RD Initiator Port
0x240	MSS_CR5B0_AXI_RD_BUS_SAFETY_CTRL	R5SS0_CORE1_AXI_RD_BUS_SAFETY_CTRL	R5SS0 CORE1 AXI_RD Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE1 AXI RD Initiator Port

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0x244	MSS_CR5B0_AXI_RD_BUS_SAFETY_FI	R5SS0_CORE1_AXI_RD_BUS_SAFETY_FI	R5SS0 CORE1 AXI_RD Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE1 AXI RD Initiator Port
0x248	MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR	R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR	R5SS0 CORE1 AXI_RD Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE1 AXI RD Initiator port
0x24C	MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	R5SS0 CORE1 AXI_RD Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE1 AXI RD Initiator Port
0x250	MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	R5SS0 CORE1 AXI_RD Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE1 AXI RD Initiator Port
0x254	MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_STAT_READ	R5SS0_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_READ	R5SS0 CORE1 AXI_RD Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS0 CORE1 AXI RD Initiator Port
0x260	MSS_CR5A1_AXI_RD_BUS_SAFETY_CTRL	R5SS1_CORE0_AXI_RD_BUS_SAFETY_CTRL	R5SS1 CORE0 AXI_RD Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE0 AXI RD Initiator Port
0x264	MSS_CR5A1_AXI_RD_BUS_SAFETY_FI	R5SS1_CORE0_AXI_RD_BUS_SAFETY_FI	R5SS1 CORE0 AXI_RD Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE0 AXI RD Initiator Port
0x268	MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR	R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR	R5SS1 CORE0 AXI_RD Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE0 AXI RD Initiator port
0x26C	MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	R5SS1 CORE0 AXI_RD Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE0 AXI RD Initiator Port
0x270	MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	R5SS1 CORE0 AXI_RD Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE0 AXI RD Initiator Port
0x274	MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_STAT_READ	R5SS1_CORE0_AXI_RD_BUS_SAFETY_ERR_STAT_READ	R5SS1 CORE0 AXI_RD Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS1 CORE0 AXI RD Initiator Port
0x280	MSS_CR5B1_AXI_RD_BUS_SAFETY_CTRL	R5SS1_CORE1_AXI_RD_BUS_SAFETY_CTRL	R5SS1 CORE1 AXI_RD Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE1 AXI RD Initiator Port
0x284	MSS_CR5B1_AXI_RD_BUS_SAFETY_FI	R5SS1_CORE1_AXI_RD_BUS_SAFETY_FI	R5SS1 CORE1 AXI_RD Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE1 AXI RD Initiator Port
0x288	MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR	R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR	R5SS1 CORE1 AXI_RD Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE1 AXI RD Initiator port
0x28C	MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0	R5SS1 CORE1 AXI_RD Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE1 AXI RD Initiator Port
0x290	MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD	R5SS1 CORE1 AXI_RD Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE1 AXI RD Initiator Port
0x294	MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_STAT_READ	R5SS1_CORE1_AXI_RD_BUS_SAFETY_ERR_STAT_READ	R5SS1 CORE1 AXI_RD Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS1 CORE1 AXI RD Initiator Port

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0x2A0	MSS_CR5A0_AXI_WR_BUS_SAFETY_CTRL	R5SS0_CORE0_AXI_WR_BUS_SAFETY_CTRL	R5SS0 CORE0 AXI_WR Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE0 AXI WR Initiator Port
0x2A4	MSS_CR5A0_AXI_WR_BUS_SAFETY_FI	R5SS0_CORE0_AXI_WR_BUS_SAFETY_FI	R5SS0 CORE0 AXI_WR Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE0 AXI WR Initiator Port
0x2A8	MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR	R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR	R5SS0 CORE0 AXI_WR Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE0 AXI WR Initiator port
0x2AC	MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	R5SS0 CORE0 AXI_WR Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE0 AXI WR Initiator Port
0x2B0	MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	R5SS0 CORE0 AXI_WR Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE0 AXI WR Initiator Port
0x2B4	MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	R5SS0 CORE0 AXI_WR Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS0 CORE0 AXI WR Initiator Port
0x2B8	MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS0_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS0 CORE0 AXI_WR Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of Write Response errors in Bus Safety Comparator of R5SS0 CORE0 AXI WR Initiator Port
0x2C0	MSS_CR5B0_AXI_WR_BUS_SAFETY_CTRL	R5SS0_CORE1_AXI_WR_BUS_SAFETY_CTRL	R5SS0 CORE1 AXI_WR Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE1 AXI WR Initiator Port
0x2C4	MSS_CR5B0_AXI_WR_BUS_SAFETY_FI	R5SS0_CORE1_AXI_WR_BUS_SAFETY_FI	R5SS0 CORE1 AXI_WR Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE1 AXI WR Initiator Port
0x2C8	MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR	R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR	R5SS0 CORE1 AXI_WR Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE1 AXI WR Initiator port
0x2CC	MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	R5SS0 CORE1 AXI_WR Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE1 AXI WR Initiator Port
0x2D0	MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	R5SS0 CORE1 AXI_WR Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE1 AXI WR Initiator Port
0x2D4	MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	R5SS0 CORE1 AXI_WR Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS0 CORE1 AXI WR Initiator Port
0x2D8	MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS0_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS0 CORE1 AXI_WR Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of Write Response errors in Bus Safety Comparator of R5SS0 CORE1 AXI WR Initiator Port
0x2E0	MSS_CR5A1_AXI_WR_BUS_SAFETY_CTRL	R5SS1_CORE0_AXI_WR_BUS_SAFETY_CTRL	R5SS1 CORE0 AXI_WR Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE0 AXI WR Initiator Port
0x2E4	MSS_CR5A1_AXI_WR_BUS_SAFETY_FI	R5SS1_CORE0_AXI_WR_BUS_SAFETY_FI	R5SS1 CORE0 AXI_WR Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE0 AXI WR Initiator Port

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0x2E8	MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR	R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR	R5SS1 CORE0 AXI_WR Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE0 AXI WR Initiator port
0x2EC	MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	R5SS1 CORE0 AXI_WR Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE0 AXI WR Initiator Port
0x2F0	MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	R5SS1 CORE0 AXI_WR Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE0 AXI WR Initiator Port
0x2F4	MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	R5SS1 CORE0 AXI_WR Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS1 CORE0 AXI WR Initiator Port
0x2F8	MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS1_CORE0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS1 CORE0 AXI_WR Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of Write Response errors in Bus Safety Comparator of R5SS1 CORE0 AXI WR Initiator Port
0x300	MSS_CR5B1_AXI_WR_BUS_SAFETY_CTRL	R5SS1_CORE1_AXI_WR_BUS_SAFETY_CTRL	R5SS1 CORE1 AXI_WR Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE1 AXI WR Initiator Port
0x304	MSS_CR5B1_AXI_WR_BUS_SAFETY_FI	R5SS1_CORE1_AXI_WR_BUS_SAFETY_FI	R5SS1 CORE1 AXI_WR Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE1 AXI WR Initiator Port
0x308	MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR	R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR	R5SS1 CORE1 AXI_WR Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE1 AXI WR Initiator port
0x30C	MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0	R5SS1 CORE1 AXI_WR Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE1 AXI WR Initiator Port
0x310	MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD	R5SS1 CORE1 AXI_WR Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE1 AXI WR Initiator Port
0x314	MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE	R5SS1 CORE1 AXI_WR Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS1 CORE1 AXI WR Initiator Port
0x318	MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS1_CORE1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS1 CORE1 AXI_WR Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of Write Response errors in Bus Safety Comparator of R5SS1 CORE1 AXI WR Initiator Port
0x320	MSS_CR5A0_AXI_S_BUS_SAFETY_CTRL	R5SS0_CORE0_AXI_S_BUS_SAFETY_CTRL	R5SS0 CORE0 AXI_S Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE0 AXI Target Port
0x324	MSS_CR5A0_AXI_S_BUS_SAFETY_FI	R5SS0_CORE0_AXI_S_BUS_SAFETY_FI	R5SS0 CORE0 AXI_S Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE0 AXI Target Port
0x328	MSS_CR5A0_AXI_S_BUS_SAFETY_ERR	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR	R5SS0 CORE0 AXI_S Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE0 AXI Target Port
0x32C	MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	R5SS0 CORE0 AXI_S Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE0 AXI Target Port

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0x330	MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_CMD	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD	R5SS0 CORE0 AXI_S Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE0 AXI Target Port
0x334	MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	R5SS0 CORE0 AXI_S Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS0 CORE0 AXI Target Port
0x338	MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_READ	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ	R5SS0 CORE0 AXI_S Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS0 CORE0 AXI Target Port
0x33C	MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS0_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS0 CORE0 AXI_S Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of R5SS0 CORE0 AXI Target Port
0x340	MSS_CR5B0_AXI_S_BUS_SAFETY_CTRL	R5SS0_CORE1_AXI_S_BUS_SAFETY_CTRL	R5SS0 CORE1 AXI_S Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE1 AXI Target Port
0x344	MSS_CR5B0_AXI_S_BUS_SAFETY_FI	R5SS0_CORE1_AXI_S_BUS_SAFETY_FI	R5SS0 CORE1 AXI_S Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE1 AXI Target Port
0x348	MSS_CR5B0_AXI_S_BUS_SAFETY_ERR	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR	R5SS0 CORE1 AXI_S Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE1 AXI Target Port
0x34C	MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	R5SS0 CORE1 AXI_S Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE1 AXI Target Port
0x350	MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_CMD	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_CMD	R5SS0 CORE1 AXI_S Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE1 AXI Target Port
0x354	MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	R5SS0 CORE1 AXI_S Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS0 CORE1 AXI Target Port
0x358	MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_READ	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_READ	R5SS0 CORE1 AXI_S Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS0 CORE1 AXI Target Port
0x35C	MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS0 CORE1 AXI_S Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of R5SS0 CORE1 AXI Target Port
0x360	MSS_CR5A1_AXI_S_BUS_SAFETY_CTRL	R5SS1_CORE0_AXI_S_BUS_SAFETY_CTRL	R5SS1 CORE0 AXI_S Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE0 AXI Target Port
0x364	MSS_CR5A1_AXI_S_BUS_SAFETY_FI	R5SS1_CORE0_AXI_S_BUS_SAFETY_FI	R5SS1 CORE0 AXI_S Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE0 AXI Target Port
0x368	MSS_CR5A1_AXI_S_BUS_SAFETY_ERR	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR	R5SS1 CORE0 AXI_S Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE0 AXI Target Port
0x36C	MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	R5SS1 CORE0 AXI_S Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE0 AXI Target Port

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0x370	MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_CMD	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD	R5SS1 CORE0 AXI_S Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE0 AXI Target Port
0x374	MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	R5SS1 CORE0 AXI_S Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS1 CORE0 AXI Target Port
0x378	MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_READ	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ	R5SS1 CORE0 AXI_S Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS1 CORE0 AXI Target Port
0x37C	MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS1 CORE0 AXI_S Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of R5SS1 CORE0 AXI Target Port
0x380	MSS_CR5B1_AXI_S_BUS_SAFETY_CTRL	R5SS1_CORE1_AXI_S_BUS_SAFETY_CTRL	R5SS1 CORE1 AXI_S Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE1 AXI Target Port
0x384	MSS_CR5B1_AXI_S_BUS_SAFETY_FI	R5SS1_CORE1_AXI_S_BUS_SAFETY_FI	R5SS1 CORE1 AXI_S Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE1 AXI Target Port
0x388	MSS_CR5B1_AXI_S_BUS_SAFETY_ERR	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR	R5SS1 CORE1 AXI_S Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE1 AXI Target Port
0x38C	MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0	R5SS1 CORE1 AXI_S Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE1 AXI Target Port
0x390	MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_CMD	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_CMD	R5SS1 CORE1 AXI_S Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE1 AXI Target Port
0x394	MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE	R5SS1 CORE1 AXI_S Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS1 CORE1 AXI Target Port
0x398	MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_READ	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_READ	R5SS1 CORE1 AXI_S Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS1 CORE1 AXI Target Port
0x39C	MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP	R5SS1 CORE1 AXI_S Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of R5SS1 CORE1 AXI Target Port
0x3A0	MSS_TPTC_A0_RD_BUS_SAFETY_CTRL	TPTC00_RD_BUS_SAFETY_CTRL	TPTC00_RD Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of TPTC00_RD Initiator Port
0x3A4	MSS_TPTC_A0_RD_BUS_SAFETY_FI	TPTC00_RD_BUS_SAFETY_FI	TPTC00_RD Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of TPTC00_RD Initiator Port
0x3A8	MSS_TPTC_A0_RD_BUS_SAFETY_ERR	TPTC00_RD_BUS_SAFETY_ERR	TPTC00_RD Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of TPTC00_RD Initiator Port
0x3AC	MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0	TPTC00_RD_BUS_SAFETY_ERR_STAT_DATA0	TPTC00_RD Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of TPTC00_RD Initiator Port

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0x3B0	MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD	TPTC00_RD_BUS_SAFETY_ERR_STAT_CMD	TPTC00_RD Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of TPTC00_RD Initiator Port
0x3B4	MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ	TPTC00_RD_BUS_SAFETY_ERR_STAT_READ	TPTC00_RD Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of TPTC00_RD Initiator Port
0x3C0	MSS_TPTC_A1_RD_BUS_SAFETY_CTRL	TPTC01_RD_BUS_SAFETY_CTRL	TPTC01_RD Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of TPTC01_RD Initiator Port
0x3C4	MSS_TPTC_A1_RD_BUS_SAFETY_FI	TPTC01_RD_BUS_SAFETY_FI	TPTC01_RD Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of TPTC01_RD Initiator Port
0x3C8	MSS_TPTC_A1_RD_BUS_SAFETY_ERR	TPTC01_RD_BUS_SAFETY_ERR	TPTC01_RD Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of TPTC01_RD Initiator Port
0x3CC	MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0	TPTC01_RD_BUS_SAFETY_ERR_STAT_DATA0	TPTC01_RD Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of TPTC01_RD Initiator Port
0x3D0	MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD	TPTC01_RD_BUS_SAFETY_ERR_STAT_CMD	TPTC01_RD Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of TPTC01_RD Initiator Port
0x3D4	MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ	TPTC01_RD_BUS_SAFETY_ERR_STAT_READ	TPTC01_RD Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of TPTC01_RD Initiator Port
0x3E0	MSS_TPTC_A0_WR_BUS_SAFETY_CTRL	TPTC00_WR_BUS_SAFETY_CTRL	TPTC00_WR Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of TPTC00_WR Initiator Port
0x3E4	MSS_TPTC_A0_WR_BUS_SAFETY_FI	TPTC00_WR_BUS_SAFETY_FI	TPTC00_WR Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of TPTC00_WR Initiator Port
0x3E8	MSS_TPTC_A0_WR_BUS_SAFETY_ERR	TPTC00_WR_BUS_SAFETY_ERR	TPTC00_WR Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of TPTC00_WR Initiator Port
0x3EC	MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0	TPTC00_WR_BUS_SAFETY_ERR_STAT_DATA0	TPTC00_WR Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of TPTC00_WR Initiator Port
0x3F0	MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD	TPTC00_WR_BUS_SAFETY_ERR_STAT_CMD	TPTC00_WR Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of TPTC00_WR Initiator Port
0x3F4	MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE	TPTC00_WR_BUS_SAFETY_ERR_STAT_WRITE	TPTC00_WR Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of TPTC00_WR Initiator Port
0x3F8	MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP	TPTC00_WR_BUS_SAFETY_ERR_STAT_WRITERESP	TPTC00_WR Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of TPTC00_WR Initiator Port
0x400	MSS_TPTC_A1_WR_BUS_SAFETY_CTRL	TPTC01_WR_BUS_SAFETY_CTRL	TPTC01_WR Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of TPTC01_WR Initiator Port
0x404	MSS_TPTC_A1_WR_BUS_SAFETY_FI	TPTC01_WR_BUS_SAFETY_FI	TPTC01_WR Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of TPTC01_WR Initiator Port

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0x408	MSS_TPTC_A1_WR_BUS_SAFETY_ERR	TPTC01_WR_BUS_SAFETY_ERR	TPTC01_WR Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of TPTC01_WR Initiator Port
0x40C	MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0	TPTC01_WR_BUS_SAFETY_ERR_STAT_DATA0	TPTC01_WR Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of TPTC01_WR Initiator Port
0x410	MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD	TPTC01_WR_BUS_SAFETY_ERR_STAT_CMD	TPTC01_WR Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of TPTC01_WR Initiator Port
0x414	MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE	TPTC01_WR_BUS_SAFETY_ERR_STAT_WRITE	TPTC01_WR Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of TPTC01_WR Initiator Port
0x418	MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP	TPTC01_WR_BUS_SAFETY_ERR_STAT_WRITERESP	TPTC01_WR Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of TPTC01_WR Initiator Port
0x420	HSM_TPTC_A0_RD_BUS_SAFETY_CTRL	HSM_TPTC0_RD_BUS_SAFETY_CTRL	HSM_TPTC0_RD Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of HSM_TPTC0_RD Initiator Port
0x424	HSM_TPTC_A0_RD_BUS_SAFETY_FI	HSM_TPTC0_RD_BUS_SAFETY_FI	HSM_TPTC0_RD Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of HSM_TPTC0_RD Initiator Port
0x428	HSM_TPTC_A0_RD_BUS_SAFETY_ERR	HSM_TPTC0_RD_BUS_SAFETY_ERR	HSM_TPTC0_RD Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of HSM_TPTC0_RD Initiator Port
0x42C	HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0	HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_DATA0	HSM_TPTC0_RD Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM_TPTC0_RD Initiator Port
0x430	HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD	HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_CMD	HSM_TPTC0_RD Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM_TPTC0_RD Initiator Port
0x434	HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ	HSM_TPTC0_RD_BUS_SAFETY_ERR_STAT_READ	HSM_TPTC0_RD Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of HSM_TPTC0_RD Initiator Port
0x440	HSM_TPTC_A1_RD_BUS_SAFETY_CTRL	HSM_TPTC1_RD_BUS_SAFETY_CTRL	HSM_TPTC1_RD Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of HSM_TPTC1_RD Initiator Port
0x444	HSM_TPTC_A1_RD_BUS_SAFETY_FI	HSM_TPTC1_RD_BUS_SAFETY_FI	HSM_TPTC1_RD Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of HSM_TPTC1_RD Initiator Port
0x448	HSM_TPTC_A1_RD_BUS_SAFETY_ERR	HSM_TPTC1_RD_BUS_SAFETY_ERR	HSM_TPTC1_RD Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of HSM_TPTC1_RD Initiator Port
0x44C	HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0	HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_DATA0	HSM_TPTC1_RD Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM_TPTC1_RD Initiator Port
0x450	HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD	HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_CMD	HSM_TPTC1_RD Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM_TPTC1_RD Initiator Port

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0x454	HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ	HSM_TPTC1_RD_BUS_SAFETY_ERR_STAT_READ	HSM_TPTC1_RD Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of HSM_TPTC1_RD Initiator Port
0x460	HSM_TPTC_A0_WR_BUS_SAFETY_CTRL	HSM_TPTC0_WR_BUS_SAFETY_CTRL	HSM_TPTC0_WR Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of HSM_TPTC0_WR Initiator Port
0x464	HSM_TPTC_A0_WR_BUS_SAFETY_FI	HSM_TPTC0_WR_BUS_SAFETY_FI	HSM_TPTC0_WR Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of HSM_TPTC0_WR Initiator Port
0x468	HSM_TPTC_A0_WR_BUS_SAFETY_ERR	HSM_TPTC0_WR_BUS_SAFETY_ERR	HSM_TPTC0_WR Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of HSM_TPTC0_WR Initiator Port
0x46C	HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0	HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_DATA0	HSM_TPTC0_WR Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM_TPTC0_WR Initiator Port
0x470	HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD	HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_CMD	HSM_TPTC0_WR Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM_TPTC0_WR Initiator Port
0x474	HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE	HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_WRITE	HSM_TPTC0_WR Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of HSM_TPTC0_WR Initiator Port
0x478	HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP	HSM_TPTC0_WR_BUS_SAFETY_ERR_STAT_WRITERESP	HSM_TPTC0_WR Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of HSM_TPTC0_WR Initiator Port
0x480	HSM_TPTC_A1_WR_BUS_SAFETY_CTRL	HSM_TPTC1_WR_BUS_SAFETY_CTRL	HSM_TPTC1_WR Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of HSM_TPTC1_WR Initiator Port
0x484	HSM_TPTC_A1_WR_BUS_SAFETY_FI	HSM_TPTC1_WR_BUS_SAFETY_FI	HSM_TPTC1_WR Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of HSM_TPTC1_WR Initiator Port
0x488	HSM_TPTC_A1_WR_BUS_SAFETY_ERR	HSM_TPTC1_WR_BUS_SAFETY_ERR	HSM_TPTC1_WR Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of HSM_TPTC1_WR Initiator Port
0x48C	HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0	HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_DATA0	HSM_TPTC1_WR Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM_TPTC1_WR Initiator Port
0x490	HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD	HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_CMD	HSM_TPTC1_WR Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM_TPTC1_WR Initiator Port
0x494	HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE	HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_WRITE	HSM_TPTC1_WR Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of HSM_TPTC1_WR Initiator Port
0x498	HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP	HSM_TPTC1_WR_BUS_SAFETY_ERR_STAT_WRITERESP	HSM_TPTC1_WR Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of HSM_TPTC1_WR Initiator Port
0x4A0	MSS_QSPI_BUS_SAFETY_CTRL	QSPI0_BUS_SAFETY_CTRL	QSPI Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of QSPI Target Port
0x4A4	MSS_QSPI_BUS_SAFETY_FI	QSPI0_BUS_SAFETY_FI	QSPI Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of QSPI Target Port

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0x4A8	MSS_QSPI_BUS_SAFETY_ERR	QSPI0_BUS_SAFETY_ERR	QSPI Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of QSPI Target Port
0x4AC	MSS_QSPI_BUS_SAFETY_ERR_STAT_DATA0	QSPI0_BUS_SAFETY_ERR_STAT_DATA0	QSPI Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of QSPI Target Port
0x4B0	MSS_QSPI_BUS_SAFETY_ERR_STAT_CMD	QSPI0_BUS_SAFETY_ERR_STAT_CMD	QSPI Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of QSPI Target Port
0x4B4	MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITE	QSPI0_BUS_SAFETY_ERR_STAT_WRITE	QSPI Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of QSPI Target Port
0x4B8	MSS_QSPI_BUS_SAFETY_ERR_STAT_READ	QSPI0_BUS_SAFETY_ERR_STAT_READ	QSPI Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of QSPI Target Port
0x4BC	MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITERESP	QSPI0_BUS_SAFETY_ERR_STAT_WRITERESP	QSPI Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of QSPI Target Port
0x4C0	HSM_DTHE_BUS_SAFETY_CTRL		HSM_DTHE Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of HSM_DTHE Target Port
0x4C4	HSM_DTHE_BUS_SAFETY_FI		HSM_DTHE Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of HSM_DTHE Target Port
0x4C8	HSM_DTHE_BUS_SAFETY_ERR		HSM_DTHE Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of HSM_DTHE Target Port
0x4CC	HSM_DTHE_BUS_SAFETY_ERR_STAT_DATA0		HSM_DTHE Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM_DTHE Target Port
0x4D0	HSM_DTHE_BUS_SAFETY_ERR_STAT_CMD		HSM_DTHE Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM_DTHE Target Port
0x4D4	HSM_DTHE_BUS_SAFETY_ERR_STAT_WRITE		HSM_DTHE Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of HSM_DTHE Target Port
0x4D8	HSM_DTHE_BUS_SAFETY_ERR_STAT_READ		HSM_DTHE Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of HSM_DTHE Target Port
0x4DC	HSM_DTHE_BUS_SAFETY_ERR_STAT_WRITERESP		HSM_DTHE Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of HSM_DTHE Target Port
0x4E0	MSS_CPSW_BUS_SAFETY_CTRL		CPSW Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of CPSW Initiator Port
0x4E4	MSS_CPSW_BUS_SAFETY_FI		CPSW Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of CPSW Initiator Port
0x4E8	MSS_CPSW_BUS_SAFETY_ERR		CPSW Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of CPSW Initiator Port
0x4EC	MSS_CPSW_BUS_SAFETY_ERR_STAT_DATA0		CPSW Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of CPSW Initiator Port
0x4F0	MSS_CPSW_BUS_SAFETY_ERR_STAT_CMD		CPSW Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of CPSW Initiator Port

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0x4F4	MSS_CPSW_BUS_SAFETY_ERR_STAT_WRITE		CPSW Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of CPSW Initiator Port
0x4F8	MSS_CPSW_BUS_SAFETY_ERR_STAT_READ		CPSW Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of CPSW Initiator Port
0x4FC	MSS_CPSW_BUS_SAFETY_ERR_STAT_WRITERESP		CPSW Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of CPSW Initiator Port
0x500	ICSSM_PDSP0_BUS_SAFETY_CTRL		ICSSM_PDSP0 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of ICSSM_PDSP0 Initiator Port
0x504	ICSSM_PDSP0_BUS_SAFETY_FI		ICSSM_PDSP0 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of ICSSM_PDSP0 Initiator Port
0x508	ICSSM_PDSP0_BUS_SAFETY_ERR		ICSSM_PDSP0 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of ICSSM_PDSP0 Initiator Port
0x50C	ICSSM_PDSP0_BUS_SAFETY_ERR_STAT_DATA0		ICSSM_PDSP0 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of ICSSM_PDSP0 Initiator Port
0x510	ICSSM_PDSP0_BUS_SAFETY_ERR_STAT_CMD		ICSSM_PDSP0 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of ICSSM_PDSP0 Initiator Port
0x514	ICSSM_PDSP0_BUS_SAFETY_ERR_STAT_WRITE		ICSSM_PDSP0 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of ICSSM_PDSP0 Initiator Port
0x518	ICSSM_PDSP0_BUS_SAFETY_ERR_STAT_READ		ICSSM_PDSP0 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of ICSSM_PDSP0 Initiator Port
0x51C	ICSSM_PDSP0_BUS_SAFETY_ERR_STAT_WRITERESP		ICSSM_PDSP0 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of ICSSM_PDSP0 Initiator Port
0x520	ICSSM_PDSP1_BUS_SAFETY_CTRL		ICSSM_PDSP1 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of ICSSM_PDSP1 Initiator Port
0x524	ICSSM_PDSP1_BUS_SAFETY_FI		ICSSM_PDSP1 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of ICSSM_PDSP1 Initiator Port
0x528	ICSSM_PDSP1_BUS_SAFETY_ERR		ICSSM_PDSP1 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of ICSSM_PDSP1 Initiator Port
0x52C	ICSSM_PDSP1_BUS_SAFETY_ERR_STAT_DATA0		ICSSM_PDSP1 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of ICSSM_PDSP1 Initiator Port
0x530	ICSSM_PDSP1_BUS_SAFETY_ERR_STAT_CMD		ICSSM_PDSP1 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of ICSSM_PDSP1 Initiator Port

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0x534	ICSSM_PDSP1_BUS_SAFETY_ERR_STAT_WRITE		ICSSM_PDSP1 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of ICSSM_PDSP1 Initiator Port
0x538	ICSSM_PDSP1_BUS_SAFETY_ERR_STAT_READ		ICSSM_PDSP1 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of ICSSM_PDSP1 Initiator Port
0x53C	ICSSM_PDSP1_BUS_SAFETY_ERR_STAT_WRITERESP		ICSSM_PDSP1 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of ICSSM_PDSP1 Initiator Port
0x540	MSS_MCRC_BUS_SAFETY_CTRL	MCRC0_BUS_SAFETY_CTRL	MCRC Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of MCRC Target Port
0x544	MSS_MCRC_BUS_SAFETY_FI	MCRC0_BUS_SAFETY_FI	MCRC Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of MCRC Target Port
0x548	MSS_MCRC_BUS_SAFETY_ERR	MCRC0_BUS_SAFETY_ERR	MCRC Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of MCRC Target Port
0x54C	MSS_MCRC_BUS_SAFETY_ERR_STAT_DATA0	MCRC0_BUS_SAFETY_ERR_STAT_DATA0	MCRC Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of MCRC Target Port
0x550	MSS_MCRC_BUS_SAFETY_ERR_STAT_CMD	MCRC0_BUS_SAFETY_ERR_STAT_CMD	MCRC Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of MCRC Target Port
0x554	MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITE	MCRC0_BUS_SAFETY_ERR_STAT_WRITE	MCRC Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of MCRC Target Port
0x558	MSS_MCRC_BUS_SAFETY_ERR_STAT_READ	MCRC0_BUS_SAFETY_ERR_STAT_READ	MCRC Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of MCRC Target Port
0x55C	MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITERESP	MCRC0_BUS_SAFETY_ERR_STAT_WRITERESP	MCRC Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of MCRC Target Port
0x560	SCRM2SCRP_0_BUS_SAFETY_CTRL		M2P0 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of M2P0 Bridge Target Port
0x564	SCRM2SCRP_0_BUS_SAFETY_FI		M2P0 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of M2P0 Bridge Target Port
0x568	SCRM2SCRP_0_BUS_SAFETY_ERR		M2P0 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of M2P0 Bridge Target Port
0x56C	SCRM2SCRP_0_BUS_SAFETY_ERR_STAT_DATA0		M2P0 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of M2P0 Bridge Target Port
0x570	SCRM2SCRP_0_BUS_SAFETY_ERR_STAT_CMD		M2P0 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of M2P0 Bridge Target Port
0x574	SCRM2SCRP_0_BUS_SAFETY_ERR_STAT_WRITE		M2P0 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of M2P0 Bridge Target Port

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0x578	SCRM2SCRP_0_BUS_SAFETY_ERR_STAT_READ		M2P0 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of M2P0 Bridge Target Port
0x57C	SCRM2SCRP_0_BUS_SAFETY_ERR_STAT_WRITERESP		M2P0 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of M2P0 Bridge Target Port
0x580	SCRM2SCRP_1_BUS_SAFETY_CTRL		M2P1 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of M2P1 Bridge Target Port
0x584	SCRM2SCRP_1_BUS_SAFETY_FI		M2P1 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of M2P1 Bridge Target Port
0x588	SCRM2SCRP_1_BUS_SAFETY_ERR		M2P1 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of M2P1 Bridge Target Port
0x58C	SCRM2SCRP_1_BUS_SAFETY_ERR_STAT_DATA0		M2P1 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of M2P1 Bridge Target Port
0x590	SCRM2SCRP_1_BUS_SAFETY_ERR_STAT_CMD		M2P1 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of M2P1 Bridge Target Port
0x594	SCRM2SCRP_1_BUS_SAFETY_ERR_STAT_WRITE		M2P1 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of M2P1 Bridge Target Port
0x598	SCRM2SCRP_1_BUS_SAFETY_ERR_STAT_READ		M2P1 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of M2P1 Bridge Target Port
0x59C	SCRM2SCRP_1_BUS_SAFETY_ERR_STAT_WRITERESP		M2P1 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of M2P1 Bridge Target Port
0x5A0	HSM_M_BUS_SAFETY_CTRL		HSM Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of HSM Initiator Port
0x5A4	HSM_M_BUS_SAFETY_FI		HSM Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of HSM Initiator Port
0x5A8	HSM_M_BUS_SAFETY_ERR		HSM Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of HSM Initiator Port
0x5AC	HSM_M_BUS_SAFETY_ERR_STAT_DATA0		HSM Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM Initiator Port
0x5B0	HSM_M_BUS_SAFETY_ERR_STAT_CMD		HSM Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM Initiator Port
0x5B4	HSM_M_BUS_SAFETY_ERR_STAT_WRITE		HSM Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of HSM Initiator Port
0x5B8	HSM_M_BUS_SAFETY_ERR_STAT_READ		HSM Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of HSM Initiator Port
0x5BC	HSM_M_BUS_SAFETY_ERR_STAT_WRITERESP		HSM Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of HSM Initiator Port

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Address Offset	ShortName	Alternate Software Name	LongName	Description
0x5C0	HSM_S_BUS_SAFETY_CTRL		HSM_S Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of HSM Target Port
0x5C4	HSM_S_BUS_SAFETY_FI		HSM_S Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of HSM Target Port
0x5C8	HSM_S_BUS_SAFETY_ERR		HSM_S Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of HSM Target Port
0x5CC	HSM_S_BUS_SAFETY_ERR_STAT_DATA0		HSM_S Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM Target Port
0x5D0	HSM_S_BUS_SAFETY_ERR_STAT_CMD		HSM_S Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM Target Port
0x5D4	HSM_S_BUS_SAFETY_ERR_STAT_WRITE		HSM_S Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of HSM Target Port
0x5D8	HSM_S_BUS_SAFETY_ERR_STAT_READ		HSM_S Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of HSM Target Port
0x5DC	HSM_S_BUS_SAFETY_ERR_STAT_WRITERESP		HSM_S Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of HSM Target Port
0x5E0	ICSSMSLAVE_BUS_SAFETY_CTRL	ICSSM_S_BUS_SAFETY_CTRL	ICSSM_S Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of ICSSM Target Port
0x5E4	ICSSMSLAVE_BUS_SAFETY_FI	ICSSM_S_BUS_SAFETY_FI	ICSSM_S Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of ICSSM Target Port
0x5E8	ICSSMSLAVE_BUS_SAFETY_ERR	ICSSM_S_BUS_SAFETY_ERR	ICSSM_S Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of ICSSM Target Port
0x5EC	ICSSMSLAVE_BUS_SAFETY_ERR_STAT_DATA0	ICSSM_S_BUS_SAFETY_ERR_STAT_DATA0	ICSSM_S Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of ICSSM Target Port
0x5F0	ICSSMSLAVE_BUS_SAFETY_ERR_STAT_CMD	ICSSM_S_BUS_SAFETY_ERR_STAT_CMD	ICSSM_S Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of ICSSM Target Port
0x5F4	ICSSMSLAVE_BUS_SAFETY_ERR_STAT_WRITE	ICSSM_S_BUS_SAFETY_ERR_STAT_WRITE	ICSSM_S Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of ICSSM Target Port
0x5F8	ICSSMSLAVE_BUS_SAFETY_ERR_STAT_READ	ICSSM_S_BUS_SAFETY_ERR_STAT_READ	ICSSM_S Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of ICSSM Target Port
0x5FC	ICSSMSLAVE_BUS_SAFETY_ERR_STAT_WRITERESP	ICSSM_S_BUS_SAFETY_ERR_STAT_WRITERESP	ICSSM_S Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of ICSSM Target Port
0x600	DAP_BUS_SAFETY_CTRL		DAP Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of DAP Initiator Port
0x604	DAP_BUS_SAFETY_FI		DAP Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of DAP Initiator Port
0x608	DAP_BUS_SAFETY_ERR		DAP Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of DAP Initiator Port
0x60C	DAP_BUS_SAFETY_ERR_STAT_DATA0		DAP Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of DAP Initiator Port

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Address Offset	ShortName	Alternate Software Name	LongName	Description
0x610	DAP_BUS_SAFETY_ERR_STAT_CMD		DAP Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of DAP Initiator Port
0x614	DAP_BUS_SAFETY_ERR_STAT_WRITE		DAP Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of DAP Initiator Port
0x618	DAP_BUS_SAFETY_ERR_STAT_READ		DAP Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of DAP Initiator Port
0x61C	DAP_BUS_SAFETY_ERR_STAT_WRITERESP		DAP Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of DAP Initiator Port
0x620	MSS_L2_A_BUS_SAFETY_CTRL	L2OCRAM_BANK0_BUS_SAFETY_CTRL	L2 BANK0 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of L2 BANK0 Target Port
0x624	MSS_L2_A_BUS_SAFETY_FI	L2OCRAM_BANK0_BUS_SAFETY_FI	L2 BANK0 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of L2 BANK0 Target Port
0x628	MSS_L2_A_BUS_SAFETY_ERR	L2OCRAM_BANK0_BUS_SAFETY_ERR	L2 BANK0 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of L2 BANK0 Target Port
0x62C	MSS_L2_A_BUS_SAFETY_ERR_STAT_DATA0	L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_DATA0	L2 BANK0 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of L2 BANK0 Target Port
0x630	MSS_L2_A_BUS_SAFETY_ERR_STAT_CMD	L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_CMD	L2 BANK0 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of L2 BANK0 Target Port
0x634	MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITE	L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_WRITE	L2 BANK0 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of L2 BANK0 Target Port
0x638	MSS_L2_A_BUS_SAFETY_ERR_STAT_READ	L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_READ	L2 BANK0 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of L2 BANK0 Target Port
0x63C	MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITERESP	L2OCRAM_BANK0_BUS_SAFETY_ERR_STAT_WRITERESP	L2 BANK0 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of L2 BANK0 Target Port
0x640	MSS_L2_B_BUS_SAFETY_CTRL	L2OCRAM_BANK1_BUS_SAFETY_CTRL	L2 BANK1 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of L2 BANK1 Target Port
0x644	MSS_L2_B_BUS_SAFETY_FI	L2OCRAM_BANK1_BUS_SAFETY_FI	L2 BANK1 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of L2 BANK1 Target Port
0x648	MSS_L2_B_BUS_SAFETY_ERR	L2OCRAM_BANK1_BUS_SAFETY_ERR	L2 BANK1 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of L2 BANK1 Target Port
0x64C	MSS_L2_B_BUS_SAFETY_ERR_STAT_DATA0	L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_DATA0	L2 BANK1 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of L2 BANK1 Target Port
0x650	MSS_L2_B_BUS_SAFETY_ERR_STAT_CMD	L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_CMD	L2 BANK1 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of L2 BANK1 Target Port

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Address Offset	ShortName	Alternate Software Name	LongName	Description
0x654	MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITE	L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_WRITE	L2 BANK1 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of L2 BANK1 Target Port
0x658	MSS_L2_B_BUS_SAFETY_ERR_STAT_READ	L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_READ	L2 BANK1 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of L2 BANK1 Target Port
0x65C	MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITERESP	L2OCRAM_BANK1_BUS_SAFETY_ERR_STAT_WRITERESP	L2 BANK1 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of L2 BANK1 Target Port
0x660	MSS_L2_C_BUS_SAFETY_CTRL	L2OCRAM_BANK2_BUS_SAFETY_CTRL	L2 BANK2 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of L2 BANK2 Target Port
0x664	MSS_L2_C_BUS_SAFETY_FI	L2OCRAM_BANK2_BUS_SAFETY_FI	L2 BANK2 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of L2 BANK2 Target Port
0x668	MSS_L2_C_BUS_SAFETY_ERR	L2OCRAM_BANK2_BUS_SAFETY_ERR	L2 BANK2 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of L2 BANK2 Target Port
0x66C	MSS_L2_C_BUS_SAFETY_ERR_STAT_DATA0	L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_DATA0	L2 BANK2 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of L2 BANK2 Target Port
0x670	MSS_L2_C_BUS_SAFETY_ERR_STAT_CMD	L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_CMD	L2 BANK2 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of L2 BANK2 Target Port
0x674	MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITE	L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_WRITE	L2 BANK2 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of L2 BANK2 Target Port
0x678	MSS_L2_C_BUS_SAFETY_ERR_STAT_READ	L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_READ	L2 BANK2 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of L2 BANK2 Target Port
0x67C	MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITERESP	L2OCRAM_BANK2_BUS_SAFETY_ERR_STAT_WRITERESP	L2 BANK2 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of L2 BANK2 Target Port
0x680	MSS_L2_D_BUS_SAFETY_CTRL	L2OCRAM_BANK3_BUS_SAFETY_CTRL	L2 BANK3 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of L2 BANK3 Target Port
0x684	MSS_L2_D_BUS_SAFETY_FI	L2OCRAM_BANK3_BUS_SAFETY_FI	L2 BANK3 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of L2 BANK3 Target Port
0x688	MSS_L2_D_BUS_SAFETY_ERR	L2OCRAM_BANK3_BUS_SAFETY_ERR	L2 BANK3 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of L2 BANK3 Target Port
0x68C	MSS_L2_D_BUS_SAFETY_ERR_STAT_DATA0	L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_DATA0	L2 BANK3 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of L2 BANK3 Target Port
0x690	MSS_L2_D_BUS_SAFETY_ERR_STAT_CMD	L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_CMD	L2 BANK3 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of L2 BANK3 Target Port

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0x694	MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITE	L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_WRITE	L2 BANK3 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of L2 BANK3 Target Port
0x698	MSS_L2_D_BUS_SAFETY_ERR_STAT_READ	L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_READ	L2 BANK3 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of L2 BANK3 Target Port
0x69C	MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITERESP	L2OCRAM_BANK3_BUS_SAFETY_ERR_STAT_WRITERESP	L2 BANK3 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of L2 BANK3 Target Port
0x6A0	MSS_MBOX_BUS_SAFETY_CTRL	MBOX_SRAM_BUS_SAFETY_CTRL	MBOX SRAM Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of MBOX SRAM Target Port
0x6A4	MSS_MBOX_BUS_SAFETY_FI	MBOX_SRAM_BUS_SAFETY_FI	MBOX SRAM Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of MBOX SRAM Target Port
0x6A8	MSS_MBOX_BUS_SAFETY_ERR	MBOX_SRAM_BUS_SAFETY_ERR	MBOX SRAM Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of MBOX SRAM Target Port
0x6AC	MSS_MBOX_BUS_SAFETY_ERR_STAT_DATA0	MBOX_SRAM_BUS_SAFETY_ERR_STAT_DATA0	MBOX SRAM Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of MBOX SRAM Target Port
0x6B0	MSS_MBOX_BUS_SAFETY_ERR_STAT_CMD	MBOX_SRAM_BUS_SAFETY_ERR_STAT_CMD	MBOX SRAM Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of MBOX SRAM Target Port
0x6B4	MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITE	MBOX_SRAM_BUS_SAFETY_ERR_STAT_WRITE	MBOX SRAM Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of MBOX SRAM Target Port
0x6B8	MSS_MBOX_BUS_SAFETY_ERR_STAT_READ	MBOX_SRAM_BUS_SAFETY_ERR_STAT_READ	MBOX SRAM Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of MBOX SRAM Target Port
0x6BC	MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITERESP	MBOX_SRAM_BUS_SAFETY_ERR_STAT_WRITERESP	MBOX SRAM Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of MBOX SRAM Target Port
0x6C0	MSS_STM_STIM_BUS_SAFETY_CTRL	STM_STIM_BUS_SAFETY_CTRL	STM Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of STM Target Port
0x6C4	MSS_STM_STIM_BUS_SAFETY_FI	STM_STIM_BUS_SAFETY_FI	STM Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of STM Target Port
0x6C8	MSS_STM_STIM_BUS_SAFETY_ERR	STM_STIM_BUS_SAFETY_ERR	STM Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of STM Target Port
0x6CC	MSS_STM_STIM_BUS_SAFETY_ERR_STAT_DATA0	STM_STIM_BUS_SAFETY_ERR_STAT_DATA0	STM Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of STM Target Port
0x6D0	MSS_STM_STIM_BUS_SAFETY_ERR_STAT_CMD	STM_STIM_BUS_SAFETY_ERR_STAT_CMD	STM Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of STM Target Port
0x6D4	MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITE	STM_STIM_BUS_SAFETY_ERR_STAT_WRITE	STM Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of STM Target Port

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Address Offset	ShortName	Alternate Software Name	LongName	Description
0x6D8	MSS_STM_STIM_BUS_SAFETY_ERR_STAT_READ	STM_STIM_BUS_SAFETY_ERR_STAT_READ	STM Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of STM Target Port
0x6DC	MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITERESP	STM_STIM_BUS_SAFETY_ERR_STAT_WRITERESP	STM Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of STM Target Port
0x6E0	MSS_MMC_BUS_SAFETY_CTRL	MMC0_BUS_SAFETY_CTRL	MMC0 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of MMC0 Target Port
0x6E4	MSS_MMC_BUS_SAFETY_FI	MMC0_BUS_SAFETY_FI	MMC0 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of MMC0 Target Port
0x6E8	MSS_MMC_BUS_SAFETY_ERR	MMC0_BUS_SAFETY_ERR	MMC0 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of MMC0 Target Port
0x6EC	MSS_MMC_BUS_SAFETY_ERR_STAT_DATA0	MMC0_BUS_SAFETY_ERR_STAT_DATA0	MMC0 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of MMC0 Target Port
0x6F0	MSS_MMC_BUS_SAFETY_ERR_STAT_CMD	MMC0_BUS_SAFETY_ERR_STAT_CMD	MMC0 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of MMC0 Target Port
0x6F4	MSS_MMC_BUS_SAFETY_ERR_STAT_WRITE	MMC0_BUS_SAFETY_ERR_STAT_WRITE	MMC0 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of MMC0 Target Port
0x6F8	MSS_MMC_BUS_SAFETY_ERR_STAT_READ	MMC0_BUS_SAFETY_ERR_STAT_READ	MMC0 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of MMC0 Target Port
0x6FC	MSS_MMC_BUS_SAFETY_ERR_STAT_WRITERESP	MMC0_BUS_SAFETY_ERR_STAT_WRITERESP	MMC0 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of MMC0 Target Port
0x700	MSS_GPMC_BUS_SAFETY_CTRL	GPMC0_BUS_SAFETY_CTRL	GPMC0 Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of GPMC0 Target Port
0x704	MSS_GPMC_BUS_SAFETY_FI	GPMC0_BUS_SAFETY_FI	GPMC0 Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of GPMC0 Target Port
0x708	MSS_GPMC_BUS_SAFETY_ERR	GPMC0_BUS_SAFETY_ERR	GPMC0 Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of GPMC0 Target Port
0x70C	MSS_GPMC_BUS_SAFETY_ERR_STAT_DATA0	GPMC0_BUS_SAFETY_ERR_STAT_DATA0	GPMC0 Bus Safety Data Error Syndrome Register	This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of GPMC0 Target Port
0x710	MSS_GPMC_BUS_SAFETY_ERR_STAT_CMD	GPMC0_BUS_SAFETY_ERR_STAT_CMD	GPMC0 Bus Safety Cmd Error Syndrome Register	This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of GPMC0 Target Port
0x714	MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITE	GPMC0_BUS_SAFETY_ERR_STAT_WRITE	GPMC0 Bus Safety Write Error Syndrome Register	This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of GPMC0 Target Port
0x718	MSS_GPMC_BUS_SAFETY_ERR_STAT_READ	GPMC0_BUS_SAFETY_ERR_STAT_READ	GPMC0 Bus Safety Read Error Syndrome Register	This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of GPMC0 Target Port
0x71C	MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITERESP	GPMC0_BUS_SAFETY_ERR_STAT_WRITERESP	GPMC0 Bus Safety WriteResp Error Syndrome Register	This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of GPMC0 Target Port

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0x720	MAIN_VBUSP_BUS_SAFETY_CTRL		Main Vbusp Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of Main VBUSP Interconnect
0x724	MAIN_VBUSP_BUS_SAFETY_FI		Main Vbusp Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of Main VBUSP Interconnect
0x728	MAIN_VBUSP_BUS_SAFETY_ERR		Main Vbusp Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of Main VBUSP Interconnect
0x740	MSS_CR5A0_AHB_BUS_SAFETY_CTRL	R5SS0_CORE0_AHB_BUS_SAFETY_CTRL	R5SS0 CORE0 Peripheral Port Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE0 Peripheral Port
0x744	MSS_CR5A0_AHB_BUS_SAFETY_FI	R5SS0_CORE0_AHB_BUS_SAFETY_FI	R5SS0 CORE0 Peripheral Port Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE0 Peripheral Port
0x748	MSS_CR5A0_AHB_BUS_SAFETY_ERR	R5SS0_CORE0_AHB_BUS_SAFETY_ERR	R5SS0 CORE0 Peripheral Port Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE0 Peripheral Port
0x760	MSS_CR5B0_AHB_BUS_SAFETY_CTRL	R5SS0_CORE1_AHB_BUS_SAFETY_CTRL	R5SS0 CORE1 Peripheral Port Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE1 Peripheral Port
0x764	MSS_CR5B0_AHB_BUS_SAFETY_FI	R5SS0_CORE1_AHB_BUS_SAFETY_FI	R5SS0 CORE1 Peripheral Port Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE1 Peripheral Port
0x768	MSS_CR5B0_AHB_BUS_SAFETY_ERR	R5SS0_CORE1_AHB_BUS_SAFETY_ERR	R5SS0 CORE1 Peripheral Port Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE1 Peripheral Port
0x780	MSS_CR5A1_AHB_BUS_SAFETY_CTRL	R5SS1_CORE0_AHB_BUS_SAFETY_CTRL	R5SS1 CORE0 Peripheral Port Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE0 Peripheral Port
0x784	MSS_CR5A1_AHB_BUS_SAFETY_FI	R5SS1_CORE0_AHB_BUS_SAFETY_FI	R5SS1 CORE0 Peripheral Port Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE0 Peripheral Port
0x788	MSS_CR5A1_AHB_BUS_SAFETY_ERR	R5SS1_CORE0_AHB_BUS_SAFETY_ERR	R5SS1 CORE0 Peripheral Port Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE0 Peripheral Port
0x7A0	MSS_CR5B1_AHB_BUS_SAFETY_CTRL	R5SS1_CORE1_AHB_BUS_SAFETY_CTRL	R5SS1 CORE1 Peripheral Port Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE1 Peripheral Port
0x7A4	MSS_CR5B1_AHB_BUS_SAFETY_FI	R5SS1_CORE1_AHB_BUS_SAFETY_FI	R5SS1 CORE1 Peripheral Port Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE1 Peripheral Port
0x7A8	MSS_CR5B1_AHB_BUS_SAFETY_ERR	R5SS1_CORE1_AHB_BUS_SAFETY_ERR	R5SS1 CORE1 Peripheral Port Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE1 Peripheral Port
0x7C0	PERI_VBUSP_BUS_SAFETY_CTRL		Peri Vbusp Bus Safety Control Register	This register is used to Control and Configure the Interconnect Safety Behaviour of Peri VBUSP Interconnect
0x7C4	PERI_VBUSP_BUS_SAFETY_FI		Peri Vbusp Bus Safety Fault Injection Register	This register is used to Inject fault on the Interconnect Safety comparator of Peri VBUSP Interconnect
0x7C8	PERI_VBUSP_BUS_SAFETY_ERR		Peri Vbusp Bus Safety Error Status Register	This Register provides the Error Status of Bus Safety Comparator of Peri VBUSP Interconnect
0x820	NERROR_MASK		ESM Error Mask Register	This register is used to Mask ESM Error signaling on the nERROR IO
0x834	MSS_VBUSM_SAFETY_H0_ERRAGG_MASK	VBUSM_SAFETY_H_ERRAGG_MASK0	VBUSM Safety High Error Mask Register0	Register to Mask VBUSM Safety High errors

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Address Offset	ShortName	Alternate Software Name	LongName	Description
0x838	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS	VBUSM_SAFETY_H_ERRAGG_STATUS0	VBUSM Safety High Error Status Register0	Status register based on mask for VBUSM Safey High Errors
0x83C	MSS_VBUSM_SAFETY_H0_ERRAGG_STATUS_RAW	VBUSM_SAFETY_H_ERRAGG_STATUS_RAW0	VBUSM Safety High Error Raw Status Register0	Raw status Register for VBUSM Safety High Errors
0x844	MSS_VBUSM_SAFETY_H1_ERRAGG_MASK	VBUSM_SAFETY_H_ERRAGG_MASK1	VBUSM Safety High Error Mask Register1	Register to Mask VBUSM Safety High errors
0x848	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS	VBUSM_SAFETY_H_ERRAGG_STATUS1	VBUSM Safety High Error Status Register1	Status register based on mask for VBUSM Safety High Errors
0x84C	MSS_VBUSM_SAFETY_H1_ERRAGG_STATUS_RAW	VBUSM_SAFETY_H_ERRAGG_STATUS_RAW1	VBUSM Safety High Error Raw Status Register1	Raw status Register for VBUSM Safety High Errors
0x854	MSS_VBUSM_SAFETY_L0_ERRAGG_MASK	VBUSM_SAFETY_L_ERRAGG_MASK0	VBUSM Safety Low Error Mask Register0	Register to Mask VBUSM Safety Low errors
0x858	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS	VBUSM_SAFETY_L_ERRAGG_STATUS0	VBUSM Safety Low Error Status Register0	Status register based on mask for VBUSM Safety Low Errors
0x85C	MSS_VBUSM_SAFETY_L0_ERRAGG_STATUS_RAW	VBUSM_SAFETY_L_ERRAGG_STATUS_RAW0	VBUSM Safety Low Error Raw Status Register0	Raw status Register for VBUSM Safety Low Errors
0x864	MSS_VBUSM_SAFETY_L1_ERRAGG_MASK	VBUSM_SAFETY_L_ERRAGG_MASK1	VBUSM Safety Low Error Mask Register1	Register to Mask VBUSM Safety Low errors
0x868	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS	VBUSM_SAFETY_L_ERRAGG_STATUS1	VBUSM Safety Low Error Status Register1	Status register based on mask for VBUSM Safety Low Errors
0x86C	MSS_VBUSM_SAFETY_L1_ERRAGG_STATUS_RAW	VBUSM_SAFETY_L_ERRAGG_STATUS_RAW1	VBUSM Safety Low Error Raw Status Register1	Raw status Register for VBUSM Safety Low Errors
0x874	MSS_VBUSP_SAFETY_H_ERRAGG_MASK	VBUSP_SAFETY_H_ERRAGG_MASK	VBUSP Safety High Error Mask Register	Register to Mask VBUSP Interconnect Safety High errors
0x878	MSS_VBUSP_SAFETY_H_ERRAGG_STATUS	VBUSP_SAFETY_H_ERRAGG_STATUS	VBUSP Safety High Error Status Register	Status register based on mask for VBUSP Interconnect Safey High Errors
0x87C	MSS_VBUSP_SAFETY_H_ERRAGG_STATUS_RAW	VBUSP_SAFETY_H_ERRAGG_STATUS_RAW	VBUSP Safety High Error Raw Status Register	Raw status Register for VBUSP Interconnect Safety High Errors

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2.3.2 MSS_CTRL_R5SS0_CONTROL Registers

2.3.2.1 MSS_R5SS0_CONTROL Register (Offset = 20h) [reset = h]

Short Description: R5SS0_CONTROL register

Long Description:

Return to Summary Table

Table 2-103. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0020h

Access Types Legend

Table 2-104. R5SS0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
26 - 24	ROM_WAIT_STATE	RW	0h	Writing '111' enables a single cycle wait state with respect to CR5A_clk for rom access.This needs to be set when R5 clock is at 400MHZ and Interconnect-clk is at 200MHZ. (because it is a timing issue in this scenario)
	RESERVED	NONE		Reserved
18 - 16	RESET_FSM_TRIGGER	RW	0h	Write pulse bit field : Writing 3'b111 will trigger the reset FSM. Reset FSM ensures reset to R5SS and inturn ensures the latching of lock_step and also mem_swap bit
	RESERVED	NONE		Reserved
10 - 8	LOCK_STEP_SWITCH_WAIT	RW	6Fh	Writing 3'b111 ensures switch happens only after R5SS reset. Or else it will be a immediate switch.
	RESERVED	NONE		Reserved
2 - 0	LOCK_STEP	RW	6Fh	Writing 3'b000 ensures R5 to be in Dual-Core mode. Note: The change happens after the R5SS reset assertion if R5_CONTROL_lock_step_switch_wait is set. Or else the switiching to Dual-core happens on the fly.

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2.3.3 MSS_CTRL_R5SS0_CORE0_HALT Registers

2.3.3.1 MSS_R5SS0_CORE0_HALT Register (Offset = 24h) [reset = h]

Short Description: R5SS0_CORE0_HALT register

Long Description:

Return to Summary Table

Table 2-105. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0024h

Access Types Legend

Table 2-106. R5SS0_CORE0_HALT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	HALT	RW	6Fh	Writing '000' will unhalt CR5A. This register should be written only once.

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2.3.4 MSS_CTRL_R5SS0_CORE1_HALT Registers

2.3.4.1 MSS_R5SS0_CORE1_HALT Register (Offset = 28h) [reset = h]

Short Description: R5SS0_CORE1_HALT register

Long Description:

Return to Summary Table

Table 2-107. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0028h

Access Types Legend

Table 2-108. R5SS0_CORE1_HALT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	HALT	RW	6Fh	Writing '000' will unhalt for CR5B. This register should be written only once.

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2.3.5 MSS_CTRL_R5SS0_STATUS_REG Registers

2.3.5.1 MSS_R5SS0_STATUS_REG Register (Offset = 2Ch) [reset = h]

Short Description: R5SS0_STATUS_REG register

Long Description:

Return to Summary Table

Table 2-109. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 002Ch

Access Types Legend

Table 2-110. R5SS0_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
8	LOCK_STEP	RO	0h	Reading 1: confirms R5SS is in lockstep mode. Reading 0: confirms R5SS is in Dual-core mode.
	RESERVED	NONE		Reserved
0	MEMSWAP	RO	0h	Reading 1: confirms ROM is Eclipsed from with RAM for R5.

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2.3.6 MSS_CTRL_R5SS0_CORE0_STAT Registers

2.3.6.1 MSS_R5SS0_CORE0_STAT Register (Offset = 30h) [reset = h]

Short Description: R5SS0_CORE0_STAT register

Long Description:

Return to Summary Table

Table 2-111. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0030h

Access Types Legend

Table 2-112. R5SS0_CORE0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4	WFE_STAT	RO	0h	WFE Status
	RESERVED	NONE		Reserved
0	WFI_STAT	RO	0h	WFI Status

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2.3.7 MSS_CTRL_R5SS0_CORE1_STAT Registers

2.3.7.1 MSS_R5SS0_CORE1_STAT Register (Offset = 34h) [reset = h]

Short Description: R5SS0_CORE1_STAT register

Long Description:

Return to Summary Table

Table 2-113. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0034h

Access Types Legend

Table 2-114. R5SS0_CORE1_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4	WFE_STAT	RO	0h	WFE Status
	RESERVED	NONE		Reserved
0	WFI_STAT	RO	0h	WFI Status

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2.3.8 MSS_CTRL_R5SS0_FORCE_WFI Registers

2.3.8.1 MSS_R5SS0_FORCE_WFI Register (Offset = 38h) [reset = h]

Short Description: R5SS0_FORCE_WFI register

Long Description:

Return to Summary Table

Table 2-115. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0038h

Access Types Legend

Table 2-116. R5SS0_FORCE_WFI Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CR5_WFI_OVERIDE	RW	0h	Writing 3'b111 will force the wfi signals of R5SS to 1

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2.3.9 MSS_CTRL_R5SS1_CONTROL Registers

2.3.9.1 MSS_R5SS1_CONTROL Register (Offset = 40h) [reset = h]

Short Description: R5SS1_CONTROL register

Long Description:

Return to Summary Table

Table 2-117. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0040h

Access Types Legend

Table 2-118. R5SS1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
18 - 16	RESET_FSM_TRIGGER	RW	0h	Write pulse bit field : Writing 3'b111 will trigger the reset FSM. Reset FSM ensures reset to R5SS and inturn ensures the latching of lock_step and also mem_swap bit
	RESERVED	NONE		Reserved
10 - 8	LOCK_STEP_SWITCH_WAIT	RW	6Fh	Writing 3'b111 ensures switch happens only after R5SS reset. Or else it will be a immediate switch.
	RESERVED	NONE		Reserved
2 - 0	LOCK_STEP	RW	6Fh	Writing 3'b000 ensures R5 to be in Dual-Core mode. Note: The change happens after the R5SS reset assertion if R5_CONTROL_lock_step_switch_wait is set. Or else the switiching to Dual-core happens on the fly.

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2.3.10 MSS_CTRL_R5SS1_CORE0_HALT Registers

2.3.10.1 MSS_R5SS1_CORE0_HALT Register (Offset = 44h) [reset = h]

Short Description: R5SS1_CORE0_HALT register

Long Description:

Return to Summary Table

Table 2-119. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0044h

Access Types Legend

Table 2-120. R5SS1_CORE0_HALT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	HALT	RW	6Fh	Writing '000' will unhalt CR5A. This register should be written only once.

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2.3.11 MSS_CTRL_R5SS1_CORE1_HALT Registers

2.3.11.1 MSS_R5SS1_CORE1_HALT Register (Offset = 48h) [reset = h]

Short Description: R5SS1_CORE1_HALT register

Long Description:

Return to Summary Table

Table 2-121. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0048h

Access Types Legend

Table 2-122. R5SS1_CORE1_HALT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	HALT	RW	6Fh	Writing '000' will unhalt for CR5B. This register should be written only once.

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2.3.12 MSS_CTRL_R5SS1_STATUS_REG Registers

2.3.12.1 MSS_R5SS1_STATUS_REG Register (Offset = 4Ch) [reset = h]

Short Description: R5SS1_STATUS_REG register

Long Description:

Return to Summary Table

Table 2-123. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 004Ch

Access Types Legend

Table 2-124. R5SS1_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
8	LOCK_STEP	RO	0h	Reading 1: confirms R5SS is in lockstep mode. Reading 0: confirms R5SS is in Dual-core mode.
	RESERVED	NONE		Reserved

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2.3.13 MSS_CTRL_R5SS1_CORE0_STAT Registers

2.3.13.1 MSS_R5SS1_CORE0_STAT Register (Offset = 50h) [reset = h]

Short Description: R5SS1_CORE0_STAT register

Long Description:

Return to Summary Table

Table 2-125. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0050h

Access Types Legend

Table 2-126. R5SS1_CORE0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4	WFE_STAT	RO	0h	WFE Status
	RESERVED	NONE		Reserved
0	WFI_STAT	RO	0h	WFI Status

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2.3.14 MSS_CTRL_R5SS1_CORE1_STAT Registers

2.3.14.1 MSS_R5SS1_CORE1_STAT Register (Offset = 54h) [reset = h]

Short Description: R5SS1_CORE1_STAT register

Long Description:

Return to Summary Table

Table 2-127. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0054h

Access Types Legend

Table 2-128. R5SS1_CORE1_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4	WFE_STAT	RO	0h	WFE Status
	RESERVED	NONE		Reserved
0	WFI_STAT	RO	0h	WFI Status

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2.3.15 MSS_CTRL_R5SS1_FORCE_WFI Registers

2.3.15.1 MSS_R5SS1_FORCE_WFI Register (Offset = 58h) [reset = h]

Short Description: R5SS1_FORCE_WFI register

Long Description:

Return to Summary Table

Table 2-129. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0058h

Access Types Legend

Table 2-130. R5SS1_FORCE_WFI Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CR5_WFI_OVERIDE	RW	0h	Writing 3'b111 will force the wfi signals of R5SS to 1

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2.3.16 MSS_CTRL_R5SS0_ROM_ECLIPSE Registers

2.3.16.1 MSS_R5SS0_ROM_ECLIPSE Register (Offset = 80h) [reset = h]

Short Description: R5SS0_ROM_ECLIPSE register

Long Description:

Return to Summary Table

Table 2-131. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0080h

Access Types Legend

Table 2-132. R5SS0_ROM_ECLIPSE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 8	MEMSWAP_WAIT	RW	6Fh	Writing 3'b111 ensures ROM-Eclipsing happens only after R5SS reset. Or else it will be a immediate change.
	RESERVED	NONE		Reserved
2 - 0	MEMSWAP	RW	0h	Writing '111' ensures eclipsing of CR5A_ROM immediately if memswap_wait is not set. If memswap_wait is set then ROM is eclipsed after R5SS reset assertion.

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2.3.17 MSS_CTRL_R5SS0_TEINIT Registers

2.3.17.1 MSS_R5SS0_TEINIT Register (Offset = 90h) [reset = h]

Short Description: R5SS0_TEINIT register

Long Description:

Return to Summary Table

Table 2-133. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0090h

Access Types Legend

Table 2-134. R5SS0_TEINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	TEINIT	RW	0h	Exception handling state at reset. 0-ARM 1-Thumb

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2.3.18 MSS_CTRL_R5SS1_TEINIT Registers

2.3.18.1 MSS_R5SS1_TEINIT Register (Offset = 94h) [reset = h]

Short Description: R5SS1_TEINIT register

Long Description:

Return to Summary Table

Table 2-135. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0094h

Access Types Legend

Table 2-136. R5SS1_TEINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	TEINIT	RW	0h	Exception handling state at reset. 0-ARM 1-Thumb

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2.3.19 MSS_CTRL_R5SS0_TCM_ECC_WRENZ_EN Registers

2.3.19.1 MSS_R5SS0_TCM_ECC_WRENZ_EN Register (Offset = D8h) [reset = h]

Short Description: R5SS0_TCM_ECC_WRENZ_EN register

Long Description:

Return to Summary Table

Table 2-137. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 00D8h

Access Types Legend

Table 2-138. R5SS0_TCM_ECC_WRENZ_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 20	CPU1_TCMB1_WRENZ_EN	RW	6Fh	Writing '000' blocks the writes to ECC-bits of TCMB0-RAM of CR5B. Writing '111' unblocks the writes to ECC-bits of TCMB1-RAM of CR5B
	RESERVED	NONE		Reserved
18 - 16	CPU1_TCMB0_WRENZ_EN	RW	6Fh	Writing '000' blocks the writes to ECC-bits of TCMB0-RAM of CR5B. Writing '111' unblocks the writes to ECC-bits of TCMB0-RAM of CR5B
	RESERVED	NONE		Reserved
14 - 12	CPU1_TCMA_WRENZ_EN	RW	6Fh	Writing '000' blocks the writes to ECC-bits of TCMA-RAM of CR5B. Writing '111' unblocks the writes to ECC-bits of TCMA-RAM of CR5B
	RESERVED	NONE		Reserved
10 - 8	CPU0_TCMB1_WRENZ_EN	RW	6Fh	Writing '000' blocks the writes to ECC-bits of TCMB0-RAM of CR5A. Writing '111' unblocks the writes to ECC-bits of TCMB1-RAM of CR5A
	RESERVED	NONE		Reserved
6 - 4	CPU0_TCMB0_WRENZ_EN	RW	6Fh	Writing '000' blocks the writes to ECC-bits of TCMB0-RAM of CR5A. Writing '111' unblocks the writes to ECC-bits of TCMB0-RAM of CR5A
	RESERVED	NONE		Reserved
2 - 0	CPU0_TCMA_WRENZ_EN	RW	6Fh	Writing '000' blocks the writes to ECC-bits of TCMA-RAM of CR5A. Writing '111' unblocks the writes to ECC-bits of TCMA-RAM of CR5A

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2.3.20 MSS_CTRL_R5SS1_TCM_ECC_WRENZ_EN Registers

2.3.20.1 MSS_R5SS1_TCM_ECC_WRENZ_EN Register (Offset = DCh) [reset = h]

Short Description: R5SS1_TCM_ECC_WRENZ_EN register

Long Description:

Return to Summary Table

Table 2-139. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 00DCh

Access Types Legend

Table 2-140. R5SS1_TCM_ECC_WRENZ_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 20	CPU1_TCMB1_WRENZ_EN	RW	6Fh	Writing '000' blocks the writes to ECC-bits of TCMB0-RAM of CR5B. Writing '111' unblocks the writes to ECC-bits of TCMB1-RAM of CR5B
	RESERVED	NONE		Reserved
18 - 16	CPU1_TCMB0_WRENZ_EN	RW	6Fh	Writing '000' blocks the writes to ECC-bits of TCMB0-RAM of CR5B. Writing '111' unblocks the writes to ECC-bits of TCMB0-RAM of CR5B
	RESERVED	NONE		Reserved
14 - 12	CPU1_TCMA_WRENZ_EN	RW	6Fh	Writing '000' blocks the writes to ECC-bits of TCMA-RAM of CR5B. Writing '111' unblocks the writes to ECC-bits of TCMA-RAM of CR5B
	RESERVED	NONE		Reserved
10 - 8	CPU0_TCMB1_WRENZ_EN	RW	6Fh	Writing '000' blocks the writes to ECC-bits of TCMB0-RAM of CR5A. Writing '111' unblocks the writes to ECC-bits of TCMB1-RAM of CR5A
	RESERVED	NONE		Reserved
6 - 4	CPU0_TCMB0_WRENZ_EN	RW	6Fh	Writing '000' blocks the writes to ECC-bits of TCMB0-RAM of CR5A. Writing '111' unblocks the writes to ECC-bits of TCMB0-RAM of CR5A
	RESERVED	NONE		Reserved
2 - 0	CPU0_TCMA_WRENZ_EN	RW	6Fh	Writing '000' blocks the writes to ECC-bits of TCMA-RAM of CR5A. Writing '111' unblocks the writes to ECC-bits of TCMA-RAM of CR5A

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2.3.21 MSS_CTRL_R5SS0_ATCM_MEM_INIT Registers

2.3.21.1 MSS_R5SS0_ATCM_MEM_INIT Register (Offset = 200h) [reset = h]

Short Description: R5SS0_ATCM_MEM_INIT register

Long Description:

Return to Summary Table

Table 2-141. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0200h

Access Types Legend

Table 2-142. R5SS0_ATCM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	MEM_INIT	RW	0h	Write_pulse bit field : Writing 1'b1 will start initializing the ATCM banks of CR5A/B. Value in each row is initialized to 0x0C_0000_0000

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2.3.22 MSS_CTRL_R5SS0_ATCM_MEM_INIT_DONE Registers

2.3.22.1 MSS_R5SS0_ATCM_MEM_INIT_DONE Register (Offset = 204h) [reset = h]

Short Description: R5SS0_ATCM_MEM_INIT_DONE register

Long Description:

Return to Summary Table

Table 2-143. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0204h

Access Types Legend

Table 2-144. R5SS0_ATCM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
0	MEM_INIT_DONE	RW	0h	This field will be high once initialization of ATCM banks is finished. Writing 1'b1 would clear the bit.

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2.3.23 MSS_CTRL_R5SS0_ATCM_MEM_INIT_STATUS Registers

2.3.23.1 MSS_R5SS0_ATCM_MEM_INIT_STATUS Register (Offset = 208h) [reset = h]

Short Description: R5SS0_ATCM_MEM_INIT_STATUS register

Long Description:

Return to Summary Table

Table 2-145. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0208h

Access Types Legend

Table 2-146. R5SS0_ATCM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
0	MEM_STATUS	RO	0h	1'b0: No initialization is happening for ATCM banks of CR5A/B 1'b1: Initialization is in progress for ATCM banks of CR5A/B

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2.3.24 MSS_CTRL_R5SS0_BTCM_MEM_INIT Registers

2.3.24.1 MSS_R5SS0_BTCM_MEM_INIT Register (Offset = 210h) [reset = h]

Short Description: R5SS0_BTCM_MEM_INIT register

Long Description:

Return to Summary Table

Table 2-147. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0210h

Access Types Legend

Table 2-148. R5SS0_BTCM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	MEM_INIT	RW	0h	Write_pulse bit field : Writing 1'b1 will start initializing the B0/1TCM banks of CR5A/B

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2.3.25 MSS_CTRL_R5SS0_BTCM_MEM_INIT_DONE Registers

2.3.25.1 MSS_R5SS0_BTCM_MEM_INIT_DONE Register (Offset = 214h) [reset = h]

Short Description: R5SS0_BTCM_MEM_INIT_DONE register

Long Description:

Return to Summary Table

Table 2-149. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0214h

Access Types Legend

Table 2-150. R5SS0_BTCM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
0	MEM_INIT_DONE	RW	0h	This field will be high once initialization of B0/1TCM banks is finished. Writing 1'b1 would clear the bit.

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2.3.26 MSS_CTRL_R5SS0_BTCM_MEM_INIT_STATUS Registers

2.3.26.1 MSS_R5SS0_BTCM_MEM_INIT_STATUS Register (Offset = 218h) [reset = h]

Short Description: R5SS0_BTCM_MEM_INIT_STATUS register

Long Description:

Return to Summary Table

Table 2-151. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0218h

Access Types Legend

Table 2-152. R5SS0_BTCM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
0	MEM_STATUS	RO	0h	1'b0: No initialization is happening for B0/1TCM banks of CR5A/B 1'b1: Initialization is in progress for B0/1TCM banks of CR5A/B

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2.3.27 MSS_CTRL_R5SS1_ATCM_MEM_INIT Registers

2.3.27.1 MSS_R5SS1_ATCM_MEM_INIT Register (Offset = 220h) [reset = h]

Short Description: R5SS1_ATCM_MEM_INIT register

Long Description:

Return to Summary Table

Table 2-153. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0220h

Access Types Legend

Table 2-154. R5SS1_ATCM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	MEM_INIT	RW	0h	Write_pulse bit field : Writing 1'b1 will start initializing the ATCM banks of CR5A/B. Value in each row is initialized to 0x0C_0000_0000

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2.3.28 MSS_CTRL_R5SS1_ATCM_MEM_INIT_DONE Registers

2.3.28.1 MSS_R5SS1_ATCM_MEM_INIT_DONE Register (Offset = 224h) [reset = h]

Short Description: R5SS1_ATCM_MEM_INIT_DONE register

Long Description:

Return to Summary Table

Table 2-155. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0224h

Access Types Legend

Table 2-156. R5SS1_ATCM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
0	MEM_INIT_DONE	RW	0h	This field will be high once initialization of ATCM banks is finished. Writing 1'b1 would clear the bit.

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2.3.29 MSS_CTRL_R5SS1_ATCM_MEM_INIT_STATUS Registers

2.3.29.1 MSS_R5SS1_ATCM_MEM_INIT_STATUS Register (Offset = 228h) [reset = h]

Short Description: R5SS1_ATCM_MEM_INIT_STATUS register

Long Description:

Return to Summary Table

Table 2-157. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0228h

Access Types Legend

Table 2-158. R5SS1_ATCM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
0	MEM_STATUS	RO	0h	1'b0: No initialization is happening for ATCM banks of CR5A/B 1'b1: Initialization is in progress for ATCM banks of CR5A/B

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2.3.30 MSS_CTRL_R5SS1_BTCM_MEM_INIT Registers

2.3.30.1 MSS_R5SS1_BTCM_MEM_INIT Register (Offset = 230h) [reset = h]

Short Description: R5SS1_BTCM_MEM_INIT register

Long Description:

Return to Summary Table

Table 2-159. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0230h

Access Types Legend

Table 2-160. R5SS1_BTCM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	MEM_INIT	RW	0h	Write_pulse bit field : Writing 1'b1 will start initializing the B0/1TCM banks of CR5A/B

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2.3.31 MSS_CTRL_R5SS1_BTCM_MEM_INIT_DONE Registers

2.3.31.1 MSS_R5SS1_BTCM_MEM_INIT_DONE Register (Offset = 234h) [reset = h]

Short Description: R5SS1_BTCM_MEM_INIT_DONE register

Long Description:

Return to Summary Table

Table 2-161. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0234h

Access Types Legend

Table 2-162. R5SS1_BTCM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
0	MEM_INIT_DONE	RW	0h	This field will be high once initialization of B0/1TCM banks is finished. Writing 1'b1 would clear the bit.

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2.3.32 MSS_CTRL_R5SS1_BTCM_MEM_INIT_STATUS Registers

2.3.32.1 MSS_R5SS1_BTCM_MEM_INIT_STATUS Register (Offset = 238h) [reset = h]

Short Description: R5SS1_BTCM_MEM_INIT_STATUS register

Long Description:

Return to Summary Table

Table 2-163. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0238h

Access Types Legend

Table 2-164. R5SS1_BTCM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
0	MEM_STATUS	RO	0h	1'b0: No initialization is happening for B0/1TCM banks of CR5A/B 1'b1: Initialization is in progress for B0/1TCM banks of CR5A/B

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2.3.33 MSS_CTRL_L2IOCRAM_MEM_INIT Registers

2.3.33.1 MSS_L2IOCRAM_MEM_INIT Register (Offset = 240h) [reset = h]

Short Description: L2IOCRAM_MEM_INIT register

Long Description:

Return to Summary Table

Table 2-165. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0240h

Access Types Legend

Table 2-166. L2IOCRAM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PARTITION3	RW	0h	Write_pulse bit field : Writing 1'b1 will start initializing the L2 Bank3. Value in each row is initialized to 0x0
2	PARTITION2	RW	0h	Write_pulse bit field : Writing 1'b1 will start initializing the L2 Bank2. Value in each row is initialized to 0x0
1	PARTITION1	RW	0h	Write_pulse bit field : Writing 1'b1 will start initializing the L2 Bank1. Value in each row is initialized to 0x0
0	PARTITION0	RW	0h	Write_pulse bit field : Writing 1'b1 will start initializing the L2 Bank0. Value in each row is initialized to 0x0

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2.3.34 MSS_CTRL_L2OCRAM_MEM_INIT_DONE Registers

2.3.34.1 MSS_L2OCRAM_MEM_INIT_DONE Register (Offset = 244h) [reset = h]

Short Description: L2OCRAM_MEM_INIT_DONE register

Long Description:

Return to Summary Table

Table 2-167. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0244h

Access Types Legend

Table 2-168. L2OCRAM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PARTITION3	RW	0h	This field will be high once intialization of L2 bank3 is finished. Writing 1'b1 would clear the bit
2	PARTITION2	RW	0h	This field will be high once intialization of L2 bank2 is finished. Writing 1'b1 would clear the bit
1	PARTITION1	RW	0h	This field will be high once intialization of L2 bank1 is finished. Writing 1'b1 would clear the bit
0	PARTITION0	RW	0h	This field will be high once intialization of L2 bank0 is finished. Writing 1'b1 would clear the bit

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2.3.35 MSS_CTRL_L2OCRAM_MEM_INIT_STATUS Registers

2.3.35.1 MSS_L2OCRAM_MEM_INIT_STATUS Register (Offset = 248h) [reset = h]

Short Description: L2OCRAM_MEM_INIT_STATUS register

Long Description:

Return to Summary Table

Table 2-169. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0248h

Access Types Legend

Table 2-170. L2OCRAM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PARTITION3	RO	0h	1'b0: No initialization is happening for L2 bank3 1'b1: Initialization is in progress for L2 bank3
2	PARTITION2	RO	0h	1'b0: No initialization is happening for L2 bank2 1'b1: Initialization is in progress for L2 bank2
1	PARTITION1	RO	0h	1'b0: No initialization is happening for L2 bank1 1'b1: Initialization is in progress for L2 bank1
0	PARTITION0	RO	0h	1'b0: No initialization is happening for L2 bank0 1'b1: Initialization is in progress for L2 bank0

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2.3.36 MSS_CTRL_MAILBOXRAM_MEM_INIT Registers

2.3.36.1 MSS_MAILBOXRAM_MEM_INIT Register (Offset = 250h) [reset = h]

Short Description: MAILBOXRAM_MEM_INIT register

Long Description:

Return to Summary Table

Table 2-171. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0250h

Access Types Legend

Table 2-172. MAILBOXRAM_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	MEM0_INIT	RW	0h	Write_pulse bit field : Writing 1'b1 will start initializing the MSS_MBOX. Value in each row is initialized to 0x0

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2.3.37 MSS_CTRL_MAILBOXRAM_MEM_INIT_DONE Registers

2.3.37.1 MSS_MAILBOXRAM_MEM_INIT_DONE Register (Offset = 254h) [reset = h]

Short Description: MAILBOXRAM_MEM_INIT_DONE register

Long Description:

Return to Summary Table

Table 2-173. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0254h

Access Types Legend

Table 2-174. MAILBOXRAM_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
0	MEM0_DONE	RW	0h	This field will be high once intialization of MSS_MBOX is finished. Writing 1'b1 would clear the bit

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2.3.38 MSS_CTRL_MAILBOXRAM_MEM_INIT_STATUS Registers

2.3.38.1 MSS_MAILBOXRAM_MEM_INIT_STATUS Register (Offset = 258h) [reset = h]

Short Description: MAILBOXRAM_MEM_INIT_STATUS register

Long Description:

Return to Summary Table

Table 2-175. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0258h

Access Types Legend

Table 2-176. MAILBOXRAM_MEM_INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
0	MEM0_STATUS	RO	0h	1'b0: No initialization is happening for MSS_MBOX 1'b1: Initialization is in progress for MSS_MBOX

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2.3.39 MSS_CTRL_TPCC_MEM_INIT Registers

2.3.39.1 MSS_TPCC_MEM_INIT Register (Offset = 260h) [reset = h]

Short Description: TPCC_MEM_INIT register

Long Description:

Return to Summary Table

Table 2-177. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0260h

Access Types Legend

Table 2-178. TPCC_MEM_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	TPCC_A_MEMINIT_START	RW	0h	Write_pulse bit field : Writing 1'b1 will start initializing the MSS_TPCCA

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2.3.40 MSS_CTRL_TPCC_MEM_INIT_DONE Registers

2.3.40.1 MSS_TPCC_MEM_INIT_DONE Register (Offset = 264h) [reset = h]

Short Description: TPCC_MEM_INIT_DONE register

Long Description:

Return to Summary Table

Table 2-179. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0264h

Access Types Legend

Table 2-180. TPCC_MEM_INIT_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
0	TPCC_A_MEMINIT_DONE	RW	0h	This field will be high once intialization of MSS_TPCCA is finished. Writing 1'b1 would clear the bit

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2.3.41 MSS_CTRL_TPCC_MEMINIT_STATUS Registers

2.3.41.1 MSS_TPCC_MEMINIT_STATUS Register (Offset = 268h) [reset = h]

Short Description: TPCC_MEMINIT_STATUS register

Long Description:

Return to Summary Table

Table 2-181. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0268h

Access Types Legend

Table 2-182. TPCC_MEMINIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
0	TPCC_A_MEMINIT_STATUS	RO	0h	1'b0: No initialization is happening for MSS_TPCCA 1'b1: Initialization is in progress for MSS_TPCCB

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2.3.42 MSS_CTRL_TOP_PBIST_KEY_RST Registers

2.3.42.1 MSS_TOP_PBIST_KEY_RST Register (Offset = 300h) [reset = h]

Short Description: TOP_PBIST_KEY_RST register

Long Description:

Return to Summary Table

Table 2-183. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0300h

Access Types Legend

Table 2-184. TOP_PBIST_KEY_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 4	PBIST_ST_RST	RW	0h	MSS PBIST controller will be brought out of reset when value is 0xA
3 - 0	PBIST_ST_KEY	RW	0h	Top PBIST Selftest Key. Valid value is 0x5

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2.3.43 MSS_CTRL_TOP_PBIST_REG0 Registers

2.3.43.1 MSS_TOP_PBIST_REG0 Register (Offset = 304h) [reset = h]

Short Description: TOP_PBIST_REG0 register

Long Description:

Return to Summary Table

Table 2-185. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0304h

Access Types Legend

Table 2-186. TOP_PBIST_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PBIST_REG	RW	0h	Not Defined

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2.3.44 MSS_CTRL_TOP_PBIST_REG1 Registers

2.3.44.1 MSS_TOP_PBIST_REG1 Register (Offset = 308h) [reset = h]

Short Description: TOP_PBIST_REG1 register

Long Description:

Return to Summary Table

Table 2-187. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0308h

Access Types Legend

Table 2-188. TOP_PBIST_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PBIST_REG	RW	0h	Not Defined

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2.3.45 MSS_CTRL_TOP_PBIST_REG2 Registers

2.3.45.1 MSS_TOP_PBIST_REG2 Register (Offset = 30Ch) [reset = h]

Short Description: TOP_PBIST_REG2 register

Long Description:

Return to Summary Table

Table 2-189. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 030Ch

Access Types Legend

Table 2-190. TOP_PBIST_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PBIST_REG	RW	0h	Not Defined

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2.3.46 MSS_CTRL_R5SS0_CTI_TRIG_SEL Registers

2.3.46.1 MSS_R5SS0_CTI_TRIG_SEL Register (Offset = 400h) [reset = h]

Short Description: R5SS0_CTI_TRIG_SEL register

Long Description:

Return to Summary Table

Table 2-191. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0400h

Access Types Legend

Table 2-192. R5SS0_CTI_TRIG_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	TRIG1	RW	0h	Used for selecting the trigger source for 1st trigger of MSS_R5SS
7 - 0	TRIG0	RW	0h	Used for selecting the trigger source for 0th trigger of MSS_R5SS

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2.3.47 MSS_CTRL_R5SS1_CTI_TRIG_SEL Registers

2.3.47.1 MSS_R5SS1_CTI_TRIG_SEL Register (Offset = 404h) [reset = h]

Short Description: R5SS1_CTI_TRIG_SEL register

Long Description:

Return to Summary Table

Table 2-193. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0404h

Access Types Legend

Table 2-194. R5SS1_CTI_TRIG_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	TRIG1	RW	0h	Used for selecting the trigger source for 1st trigger of MSS_R5SS
7 - 0	TRIG0	RW	0h	Used for selecting the trigger source for 0th trigger of MSS_R5SS

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2.3.48 MSS_CTRL_DBGSS_CTI_TRIG_SEL Registers

2.3.48.1 MSS_DBGSS_CTI_TRIG_SEL Register (Offset = 408h) [reset = h]

Short Description: DBGSS_CTI_TRIG_SEL register

Long Description:

Return to Summary Table

Table 2-195. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0408h

Access Types Legend

Table 2-196. DBGSS_CTI_TRIG_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	TRIG3	RW	0h	Used for selecting the trigger source for 3rd trigger of ONE_MCU_CTI
23 - 16	TRIG2	RW	0h	Used for selecting the trigger source for 2nd trigger of ONE_MCU_CTI
15 - 8	TRIG1	RW	0h	Used for selecting the trigger source for 1st trigger of ONE_MCU_CTI
7 - 0	TRIG0	RW	0h	Used for selecting the trigger source for 0th trigger of ONE_MCU_CTI

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2.3.49 MSS_CTRL_DEBUGSS_CSETB_FLUSH Registers

2.3.49.1 MSS_DEBUGSS_CSETB_FLUSH Register (Offset = 40Ch) [reset = h]

Short Description: DEBUGSS_CSETB_FLUSH register

Long Description:

Return to Summary Table

Table 2-197. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 040Ch

Access Types Legend

Table 2-198. DEBUGSS_CSETB_FLUSH Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10	CSETB_FULL	RO	0h	When HIGH indicates that the ETB RAM has overflowed or wrapped around to address zero
9	CSETB_ACQ_COMPLETE	RO	0h	When HIGH, indicates that trace acquisition is complete by ETB, that is, the trigger counter is at zero
8	CSETB_FLUSHINACK	RO	0h	Return acknowledgement to CSETBFLUSHIN
	RESERVED	NONE		Reserved
0	CSETB_FLUSHIN	RW	0h	External control used to assert the ATB signal AFVALIDS and drain any historical FIFO information on the bus

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2.3.50 MSS_CTRL_DEBUGSS_STM_NSGUAREN Registers

2.3.50.1 MSS_DEBUGSS_STM_NSGUAREN Register (Offset = 410h) [reset = h]

Short Description: DEBUGSS_STM_NSGUAREN register

Long Description:

Return to Summary Table

Table 2-199. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0410h

Access Types Legend

Table 2-200. DEBUGSS_STM_NSGUAREN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10	ENABLE	RW	0h	Non secure guarenteed access control0:Access does not stall the CPU. Trace not guarenteed1: Access may stall. Trace guarenteed
	RESERVED	NONE		Reserved

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2.3.51 MSS_CTRL_MCAN0_HALTEN Registers

2.3.51.1 MSS_MCAN0_HALTEN Register (Offset = 420h) [reset = h]

Short Description: MCAN0_HALTEN register

Long Description:

Return to Summary Table

Table 2-201. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0420h

Access Types Legend

Table 2-202. MCAN0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.52 MSS_CTRL_MCAN1_HALTEN Registers

2.3.52.1 MSS_MCAN1_HALTEN Register (Offset = 424h) [reset = h]

Short Description: MCAN1_HALTEN register

Long Description:

Return to Summary Table

Table 2-203. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0424h

Access Types Legend

Table 2-204. MCAN1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.53 MSS_CTRL_MCAN2_HALTEN Registers

2.3.53.1 MSS_MCAN2_HALTEN Register (Offset = 428h) [reset = h]

Short Description: MCAN2_HALTEN register

Long Description:

Return to Summary Table

Table 2-205. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0428h

Access Types Legend

Table 2-206. MCAN2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.54 MSS_CTRL_MCAN3_HALTEN Registers

2.3.54.1 MSS_MCAN3_HALTEN Register (Offset = 42Ch) [reset = h]

Short Description: MCAN3_HALTEN register

Long Description:

Return to Summary Table

Table 2-207. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 042Ch

Access Types Legend

Table 2-208. MCAN3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.55 MSS_CTRL_LIN0_HALTEN Registers

2.3.55.1 MSS_LIN0_HALTEN Register (Offset = 430h) [reset = h]

Short Description: LIN0_HALTEN register

Long Description:

Return to Summary Table

Table 2-209. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0430h

Access Types Legend

Table 2-210. LIN0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.56 MSS_CTRL_LIN1_HALTEN Registers

2.3.56.1 MSS_LIN1_HALTEN Register (Offset = 434h) [reset = h]

Short Description: LIN1_HALTEN register

Long Description:

Return to Summary Table

Table 2-211. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0434h

Access Types Legend

Table 2-212. LIN1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.57 MSS_CTRL_LIN2_HALTEN Registers

2.3.57.1 MSS_LIN2_HALTEN Register (Offset = 438h) [reset = h]

Short Description: LIN2_HALTEN register

Long Description:

Return to Summary Table

Table 2-213. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0438h

Access Types Legend

Table 2-214. LIN2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.58 MSS_CTRL_LIN3_HALTEN Registers

2.3.58.1 MSS_LIN3_HALTEN Register (Offset = 43Ch) [reset = h]

Short Description: LIN3_HALTEN register

Long Description:

Return to Summary Table

Table 2-215. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 043Ch

Access Types Legend

Table 2-216. LIN3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.59 MSS_CTRL_LIN4_HALTEN Registers

2.3.59.1 MSS_LIN4_HALTEN Register (Offset = 440h) [reset = h]

Short Description: LIN4_HALTEN register

Long Description:

Return to Summary Table

Table 2-217. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0440h

Access Types Legend

Table 2-218. LIN4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.60 MSS_CTRL_I2C0_HALTEN Registers

2.3.60.1 MSS_I2C0_HALTEN Register (Offset = 444h) [reset = h]

Short Description: I2C0_HALTEN register

Long Description:

Return to Summary Table

Table 2-219. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0444h

Access Types Legend

Table 2-220. I2C0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.61 MSS_CTRL_I2C1_HALTEN Registers

2.3.61.1 MSS_I2C1_HALTEN Register (Offset = 448h) [reset = h]

Short Description: I2C1_HALTEN register

Long Description:

Return to Summary Table

Table 2-221. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0448h

Access Types Legend

Table 2-222. I2C1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.62 MSS_CTRL_I2C2_HALTEN Registers

2.3.62.1 MSS_I2C2_HALTEN Register (Offset = 44Ch) [reset = h]

Short Description: I2C2_HALTEN register

Long Description:

Return to Summary Table

Table 2-223. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 044Ch

Access Types Legend

Table 2-224. I2C2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.63 MSS_CTRL_I2C3_HALTEN Registers

2.3.63.1 MSS_I2C3_HALTEN Register (Offset = 450h) [reset = h]

Short Description: I2C3_HALTEN register

Long Description:

Return to Summary Table

Table 2-225. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0450h

Access Types Legend

Table 2-226. I2C3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.64 MSS_CTRL_RTI0_HALTEN Registers

2.3.64.1 MSS_RTI0_HALTEN Register (Offset = 454h) [reset = h]

Short Description: RTI0_HALTEN register

Long Description:

Return to Summary Table

Table 2-227. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0454h

Access Types Legend

Table 2-228. RTI0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.65 MSS_CTRL_RTI1_HALTEN Registers

2.3.65.1 MSS_RTI1_HALTEN Register (Offset = 458h) [reset = h]

Short Description: RTI1_HALTEN register

Long Description:

Return to Summary Table

Table 2-229. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0458h

Access Types Legend

Table 2-230. RTI1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.66 MSS_CTRL_RTI2_HALTEN Registers

2.3.66.1 MSS_RTI2_HALTEN Register (Offset = 45Ch) [reset = h]

Short Description: RTI2_HALTEN register

Long Description:

Return to Summary Table

Table 2-231. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 045Ch

Access Types Legend

Table 2-232. RTI2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.67 MSS_CTRL_RTI3_HALTEN Registers

2.3.67.1 MSS_RTI3_HALTEN Register (Offset = 460h) [reset = h]

Short Description: RTI3_HALTEN register

Long Description:

Return to Summary Table

Table 2-233. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0460h

Access Types Legend

Table 2-234. RTI3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt t
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.68 MSS_CTRL_CPSW_HALTEN Registers

2.3.68.1 MSS_CPSW_HALTEN Register (Offset = 474h) [reset = h]

Short Description: CPSW_HALTEN register

Long Description:

Return to Summary Table

Table 2-235. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0474h

Access Types Legend

Table 2-236. CPSW_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.69 MSS_CTRL_MCRC0_HALTEN Registers

2.3.69.1 MSS_MCRC0_HALTEN Register (Offset = 478h) [reset = h]

Short Description: MCRC0_HALTEN register

Long Description:

Return to Summary Table

Table 2-237. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0478h

Access Types Legend

Table 2-238. MCRC0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0_HALTEN	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt 1'b1: IP Halt enabled with corresponding CPU halt

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2.3.70 MSS_CTRL_TPTC_DBS_CONFIG Registers

2.3.70.1 MSS_TPTC_DBS_CONFIG Register (Offset = 800h) [reset = h]

Short Description: TPTC_DBS_CONFIG register

Long Description:

Return to Summary Table

Table 2-239. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0800h

Access Types Legend

Table 2-240. TPTC_DBS_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
5 - 4	TPTC_A1	RW	1h	Default burst size tieoff value for TPTC_A1
	RESERVED	NONE		Reserved
1 - 0	TPTC_A0	RW	1h	Default burst size tieoff value for TPTC_A0

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2.3.71 MSS_CTRL_TPTC_BOUNDARY_CFG Registers

2.3.71.1 MSS_TPTC_BOUNDARY_CFG Register (Offset = 804h) [reset = h]

Short Description: TPTC_BOUNDARY_CFG register

Long Description:

Return to Summary Table

Table 2-241. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0804h

Access Types Legend

Table 2-242. TPTC_BOUNDARY_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
13 - 8	TPTC_A1_SIZE	RW	271Bh	6 bit signal used for deciding the boundary crossing size for CID-RID-SID reordering of MSS_TPTC_A1Example: Writing 6'd19 decidies boundary to be 2^19 i.e. 512 KB
	RESERVED	NONE		Reserved
5 - 0	TPTC_A0_SIZE	RW	271Bh	6 bit signal used for deciding the boundary crossing size for CID-RID-SID reordering of MSS_TPTC_A0Example: Writing 6'd19 decidies boundary to be 2^19 i.e. 512 KB

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2.3.72 MSS_CTRL_TPTC_XID_REORDER_CFG Registers

2.3.72.1 MSS_TPTC_XID_REORDER_CFG Register (Offset = 808h) [reset = h]

Short Description: TPTC_XID_REORDER_CFG register

Long Description:

Return to Summary Table

Table 2-243. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0808h

Access Types Legend

Table 2-244. TPTC_XID_REORDER_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
8	TPTC_A1_DISABLE	RW	0h	Writing 1'b1 will disable the CID-RID-SID reodering feature for MSS_TPTC_A1
	RESERVED	NONE		Reserved
0	TPTC_A0_DISABLE	RW	0h	Writing 1'b1 will disable the CID-RID-SID reodering feature for MSS_TPTC_A0

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2.3.73 MSS_CTRL_CPSW_CONTROL Registers

2.3.73.1 MSS_CPSW_CONTROL Register (Offset = 810h) [reset = h]

Short Description: CPSW_CONTROL register

Long Description:

Return to Summary Table

Table 2-245. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0810h

Access Types Legend

Table 2-246. CPSW_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
24	RGMII2_ID_MODE	RW	1h	Internal delay mode for port 2. Only for TX0 : ID mode is disabled1 : ID mode is enabled
	RESERVED	NONE		Reserved
22	RMII2_REF_CLK_SEL	RW	0h	To select the rmii_ref_clk loopback mux output either from PAD or from MSS_RCM. Write 0 to get clock will be from IO pad(pad loopback). Write 1 to get clock from internal loopback.
	RESERVED	NONE		Reserved
20	RMII2_REF_CLK_OE_N	RW	0h	RMII_REF_CLK IO Output enable control0: Output enable1: Output Disable
	RESERVED	NONE		Reserved
18 - 16	PORT2_MODE_SEL	RW	0h	Port 2 Interface 000 = MII001 = RMII010 = RGMII011 - 111 = Not Supported
	RESERVED	NONE		Reserved
8	RGMII1_ID_MODE	RW	1h	Internal delay mode for port 1. Only for TX0 : ID mode is disabled1 : ID mode is enabled
	RESERVED	NONE		Reserved
6	RMII1_REF_CLK_SEL	RW	0h	To select the rmii_ref_clk loopback mux output either from PAD or from MSS_RCM. Write 0 to get clock will be from IO pad(pad loopback). Write 1 to get clock from internal source
	RESERVED	NONE		Reserved
4	RMII1_REF_CLK_OE_N	RW	0h	RMII_REF_CLK IO Output enable control0: Output enable1: Output Disable
	RESERVED	NONE		Reserved
2 - 0	PORT1_MODE_SEL	RW	0h	Port 1 Interface 000 = MII001 = RMII010 = RGMII011 - 111 = Not Supported

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2.3.74 MSS_CTRL_QSPI_CONFIG Registers

2.3.74.1 MSS_QSPI_CONFIG Register (Offset = 814h) [reset = h]

Short Description: QSPI_CONFIG register

Long Description:

Return to Summary Table

Table 2-247. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0814h

Access Types Legend

Table 2-248. QSPI_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	EXT_CLK	RW	0h	Write 3'b111 to external clock as QSPI baud clock source needed for DFT IO char.

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2.3.75 MSS_CTRL_ICSSM_IDLE_CONTROL Registers

2.3.75.1 MSS_ICSSM_IDLE_CONTROL Register (Offset = 818h) [reset = h]

Short Description: ICSSM_IDLE_CONTROL register

Long Description:

Return to Summary Table

Table 2-249. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0818h

Access Types Legend

Table 2-250. ICSSM_IDLE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	NOGATE	RW	1h	Writing 1'b0 will enable local auto-clock gating (lower power) at IP level with increase in access/functional latency. Following IPs are controlled with this signalICSSM

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2.3.76 MSS_CTRL_ICSSM_PRU0_GPI_SEL Registers

2.3.76.1 MSS_ICSSM_PRU0_GPI_SEL Register (Offset = 81Ch) [reset = h]

Short Description: ICSSM_PRU0_GPI_SEL register

Long Description:

Return to Summary Table

Table 2-251. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 081Ch

Access Types Legend

Table 2-252. ICSSM_PRU0_GPI_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 0	SEL	RW	0h	GPI or PWMXBar select for ICSM Port0 0: GPI 1: PWMXBAR

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2.3.77 MSS_CTRL_ICSSM_PRU1_GPI_SEL Registers

2.3.77.1 MSS_ICSSM_PRU1_GPI_SEL Register (Offset = 820h) [reset = h]

Short Description: ICSSM_PRU1_GPI_SEL register

Long Description:

Return to Summary Table

Table 2-253. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0820h

Access Types Legend

Table 2-254. ICSSM_PRU1_GPI_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 0	SEL	RW	0h	GPI or PWMXBar select for ICSM Port0 0: GPI 1: PWMXBAR

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2.3.78 MSS_CTRL_ICSSM_PRU0_GPIO_OUT_CTRL Registers

2.3.78.1 MSS_ICSSM_PRU0_GPIO_OUT_CTRL Register (Offset = 824h) [reset = h]

Short Description: ICSSM_PRU0_GPIO_OUT_CTRL register

Long Description:

Return to Summary Table

Table 2-255. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0824h

Access Types Legend

Table 2-256. ICSSM_PRU0_GPIO_OUT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 0	OUTDISABLE	RW	0h	GPO output disable for ICSSM Port 0 IO. Disable output for using the pin as input. Each Bit maps to the corresponding bit in the IO 0: Output Enable 1: Output Disable

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2.3.79 MSS_CTRL_ICSSM_PRU1_GPIO_OUT_CTRL Registers

2.3.79.1 MSS_ICSSM_PRU1_GPIO_OUT_CTRL Register (Offset = 828h) [reset = h]

Short Description: ICSSM_PRU1_GPIO_OUT_CTRL register

Long Description:

Return to Summary Table

Table 2-257. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0828h

Access Types Legend

Table 2-258. ICSSM_PRU1_GPIO_OUT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 0	OUTDISABLE	RW	0h	GPO output disable for ICSSM Port 1 IO. Disable output for using the pin as input. Each Bit maps to the corresponding bit in the IO 0: Output Enable 1: Output Disable

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2.3.80 MSS_CTRL_GPMC_CONTROL Registers

2.3.80.1 MSS_GPMC_CONTROL Register (Offset = 82Ch) [reset = h]

Short Description: GPMC_CONTROL register

Long Description:

Return to Summary Table

Table 2-259. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 082Ch

Access Types Legend

Table 2-260. GPMC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
12	CLK_LB_OE_N	RW	0h	GPMC_CLK_LB oe_n 1: GPMC_dev_clk is driven to pad 0: GPMC_dev_clk is not driven to pad
	RESERVED	NONE		Reserved
8	CLK_OE_N	RW	1h	GPMC_CLKOUT oe_n 1: GPMC_dev_clk mux output is driven to pad 0: GPMC_dev_clk mux output is not driven to pad
	RESERVED	NONE		Reserved
4	CLK_LB_SEL	RW	0h	GPMC_CLK_LB sel 0: GPMC_CLK_LB pad clock 1: GPMC_CLK pad clock
	RESERVED	NONE		Reserved
0	CLKOUT_SEL	RW	0h	GPMC_CLKOUT sel 0: GPMC_func_clock 1: GPMC_dev clock

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2.3.81 MSS_CTRL_TPCC0_INTAGG_MASK Registers

2.3.81.1 MSS_TPCC0_INTAGG_MASK Register (Offset = 830h) [reset = h]

Short Description: TPCC0_INTAGG_MASK register

Long Description:

Return to Summary Table

Table 2-261. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0830h

Access Types Legend

Table 2-262. TPCC0_INTAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	TPTC_A1	RW	0h	Mask Interrupt from TPTC A1 to aggregated Interrupt MSS_TPCC_A_INTAGG 1: Interrupt is Masked 0: Interrupt is Unmasked
16	TPTC_A0	RW	0h	Mask Interrupt from TPTC A0 to aggregated Interrupt MSS_TPCC_A_INTAGG 1: Interrupt is Masked 0: Interrupt is Unmasked
	RESERVED	NONE		Reserved
8	TPCC_A_INT7	RW	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1: Interrupt is Masked 0: Interrupt is Unmasked
7	TPCC_A_INT6	RW	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1: Interrupt is Masked 0: Interrupt is Unmasked
6	TPCC_A_INT5	RW	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1: Interrupt is Masked 0: Interrupt is Unmasked
5	TPCC_A_INT4	RW	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1: Interrupt is Masked 0: Interrupt is Unmasked
4	TPCC_A_INT3	RW	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1: Interrupt is Masked 0: Interrupt is Unmasked
3	TPCC_A_INT2	RW	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAG 1: Interrupt is Masked 0: Interrupt is Unmasked

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Table 2-262. TPCC0_INTAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TPCC_A_INT1	RW	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1: Interrupt is Masked 0: Interrupt is Unmasked
1	TPCC_A_INT0	RW	0h	Mask Interrupt from TPCC A to aggregated Interrupt MSS_TPCC_A_INTAGG 1: Interrupt is Masked 0: Interrupt is Unmasked
0	TPCC_A_INTG	RW	0h	Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG 1: Interrupt is Masked 0: Interrupt is Unmasked

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2.3.82 MSS_CTRL_TPCC0_INTAGG_STATUS Registers

2.3.82.1 MSS_TPCC0_INTAGG_STATUS Register (Offset = 834h) [reset = h]

Short Description: TPCC0_INTAGG_STATUS register

Long Description:

Return to Summary Table

Table 2-263. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0834h

Access Types Legend

Table 2-264. TPCC0_INTAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	TPTC_A1	RW	0h	Status of Interrupt from TPTC A1. Set only if Interrupt is unmasked in MSS_TPCC_A_INTAGG_MASK. Write 0x1 to clear this interrupt.
16	TPTC_A0	RW	0h	Status of Interrupt from TPTC A0. Set only if Interrupt is unmasked in MSS_TPCC_A_INTAGG_MASK. Write 0x1 to clear this interrupt.
	RESERVED	NONE		Reserved
8	TPCC_A_INT7	RW	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interrupt is unmasked in MSS_TPCC_A_INTAGG_MASK. Write 0x1 to clear this interrupt.
7	TPCC_A_INT6	RW	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interrupt is unmasked in MSS_TPCC_A_INTAGG_MASK. Write 0x1 to clear this interrupt.
6	TPCC_A_INT5	RW	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interrupt is unmasked in MSS_TPCC_A_INTAGG_MASK. Write 0x1 to clear this interrupt.
5	TPCC_A_INT4	RW	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interrupt is unmasked in MSS_TPCC_A_INTAGG_MASK. Write 0x1 to clear this interrupt.
4	TPCC_A_INT3	RW	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interrupt is unmasked in MSS_TPCC_A_INTAGG_MASK. Write 0x1 to clear this interrupt.
3	TPCC_A_INT2	RW	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interrupt is unmasked in MSS_TPCC_A_INTAGG_MASK. Write 0x1 to clear this interrupt.
2	TPCC_A_INT1	RW	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interrupt is unmasked in MSS_TPCC_A_INTAGG_MASK. Write 0x1 to clear this interrupt.
1	TPCC_A_INT0	RW	0h	Status of Interrupt from TPCC A Set only if Interrupt is unmasked in MSS_TPCC_A_INTAGG_MASK. Write 0x1 to clear this interrupt.
0	TPCC_A_INTG	RW	0h	Status of Interrupt from MSS_TPCC_A. Set only if Interrupt is unmasked in MSS_TPCC_A_INTAGG_MASK. Write 0x1 to clear this interrupt.

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2.3.83 MSS_CTRL_TPCC0_INTAGG_STATUS_RAW Registers

2.3.83.1 MSS_TPCC0_INTAGG_STATUS_RAW Register (Offset = 838h) [reset = h]

Short Description: TPCC0_INTAGG_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-265. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 0838h

Access Types Legend

Table 2-266. TPCC0_INTAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	TPTC_A1	RW	0h	Raw Status of Interrupt from TPTC A1. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_INTAGG_MASK
16	TPTC_A0	RW	0h	Raw Status of Interrupt from TPTC A0. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_INTAGG_MASK
	RESERVED	NONE		Reserved
8	TPCC_A_INT7	RW	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK
7	TPCC_A_INT6	RW	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK
6	TPCC_A_INT5	RW	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK
5	TPCC_A_INT4	RW	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK
4	TPCC_A_INT3	RW	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK
3	TPCC_A_INT2	RW	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK
2	TPCC_A_INT1	RW	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK
1	TPCC_A_INT0	RW	0h	Raw Status of Interrupt from TPCC A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_INTAGG_MASK
0	TPCC_A_INTG	RW	0h	Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK

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2.3.84 MSS_CTRL_LOCK0_KICK0 Registers

2.3.84.1 MSS_LOCK0_KICK0 Register (Offset = 1008h) [reset = h]

Short Description: - KICK0 component

Long Description:

Return to Summary Table

Table 2-267. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 1008h

Access Types Legend

Table 2-268. LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	LOCK0_KICK0	RW	0h	- KICK0 component

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2.3.85 MSS_CTRL_LOCK0_KICK1 Registers

2.3.85.1 MSS_LOCK0_KICK1 Register (Offset = 100Ch) [reset = h]

Short Description: - KICK1 component

Long Description:

Return to Summary Table

Table 2-269. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 100Ch

Access Types Legend

Table 2-270. LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	LOCK0_KICK1	RW	0h	- KICK1 component

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2.3.86 MSS_CTRL_INTR_RAW_STATUS Registers

2.3.86.1 MSS_INTR_RAW_STATUS Register (Offset = 1010h) [reset = h]

Short Description: Interrupt Raw Status/Set Register

Long Description:

Return to Summary Table

Table 2-271. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 1010h

Access Types Legend

Table 2-272. INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR	RW	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
2	KICK_ERR	RW	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
1	ADDR_ERR	RW	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
0	PROT_ERR	RW	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.

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2.3.87 MSS_CTRL_INTR_ENABLED_STATUS_CLEAR Registers

2.3.87.1 MSS_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = h]

Short Description: Interrupt Enabled Status/Clear register

Long Description:

Return to Summary Table

Table 2-273. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 1014h

Access Types Legend

Table 2-274. INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	ENABLED_PROXY_ERR	RW	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
2	ENABLED_KICK_ERR	RW	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
1	ENABLED_ADDR_ERR	RW	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
0	ENABLED_PROT_ERR	RW	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.

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2.3.88 MSS_CTRL_INTR_ENABLE Registers

2.3.88.1 MSS_INTR_ENABLE Register (Offset = 1018h) [reset = h]

Short Description: Interrupt Enable register

Long Description:

Return to Summary Table

Table 2-275. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 1018h

Access Types Legend

Table 2-276. INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR_EN	RW	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
2	KICK_ERR_EN	RW	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN	RW	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
0	PROT_ERR_EN	RW	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.

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2.3.89 MSS_CTRL_INTR_ENABLE_CLEAR Registers

2.3.89.1 MSS_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = h]

Short Description: Interrupt Enable Clear register

Long Description:

Return to Summary Table

Table 2-277. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 101Ch

Access Types Legend

Table 2-278. INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR_EN_CLR	RW	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
2	KICK_ERR_EN_CLR	RW	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN_CLR	RW	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
0	PROT_ERR_EN_CLR	RW	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.

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2.3.90 MSS_CTRL_EOI Registers

2.3.90.1 MSS_EOI Register (Offset = 1020h) [reset = h]

Short Description: EOI register

Long Description:

Return to Summary Table

Table 2-279. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 1020h

Access Types Legend

Table 2-280. EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	EOI_VECTOR	RW	0h	EOI vector value. Write this with interrupt distribution value in the chip.

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2.3.91 MSS_CTRL_FAULT_ADDRESS Registers

2.3.91.1 MSS_FAULT_ADDRESS Register (Offset = 1024h) [reset = h]

Short Description: Fault Address register

Long Description:

Return to Summary Table

Table 2-281. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 1024h

Access Types Legend

Table 2-282. FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FAULT_ADDR	RO	0h	Fault Address.

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2.3.92 MSS_CTRL_FAULT_TYPE_STATUS Registers

2.3.92.1 MSS_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = h]

Short Description: Fault Type Status register

Long Description:

Return to Summary Table

Table 2-283. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 1028h

Access Types Legend

Table 2-284. FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	FAULT_NS	RO	0h	Non-secure access.
5 - 0	FAULT_TYPE	RO	0h	Fault Type: • 10_0000 = Supervisor read fault - priv = 1, dir = 1, dtype != 1 • 01_0000 = Supervisor write fault - priv = 1, dir = 0 • 00_1000 = Supervisor execute fault - priv = 1, dir = 1, dtype = 1 • 00_0100 = User read fault - priv = 0, dir = 1, dtype = 1 • 00_0010 = User write fault - priv = 0, dir = 0 • 00_0001 = User execute fault - priv = 0, dir = 1, dtype = 1 • 00_0000 = No fault

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2.3.93 MSS_CTRL_FAULT_ATTR_STATUS Registers

2.3.93.1 MSS_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = h]

Short Description: Fault Attribute Status register

Long Description:

Return to Summary Table

Table 2-285. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 102Ch

Access Types Legend

Table 2-286. FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	FAULT_XID	RO	0h	XID.
19 - 8	FAULT_ROUTEID	RO	0h	Route ID.
7 - 0	FAULT_PRIVID	RO	0h	Privilege ID.

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2.3.94 MSS_CTRL_FAULT_CLEAR Registers

2.3.94.1 MSS_FAULT_CLEAR Register (Offset = 1030h) [reset = h]

Short Description: Fault Clear register

Long Description:

Return to Summary Table

Table 2-287. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 1030h

Access Types Legend

Table 2-288. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
0	FAULT_CLR	WO	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect.

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2.3.95 MSS_CTRL_R5SS0_CORE0_MBOX_WRITE_DONE Registers

2.3.95.1 MSS_R5SS0_CORE0_MBOX_WRITE_DONE Register (Offset = 4000h) [reset = h]

Short Description: R5SS0_CORE0_MBOX_WRITE_DONE register

Long Description:

Return to Summary Table

Table 2-289. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4000h

Access Types Legend

Table 2-290. R5SS0_CORE0_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 7
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 6
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 5
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 4
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 3
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 2
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 1
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 0

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2.3.96 MSS_CTRL_R5SS0_CORE0_MBOX_READ_REQ Registers

2.3.96.1 MSS_R5SS0_CORE0_MBOX_READ_REQ Register (Offset = 4004h) [reset = h]

Short Description: R5SS0_CORE0_MBOX_READ_REQ register

Long Description:

Return to Summary Table

Table 2-291. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4004h

Access Types Legend

Table 2-292. R5SS0_CORE0_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	This is request from processor 7 to mss_cr5a. Mailbox Read Request.
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	This is request from processor 6 to mss_cr5a. Mailbox Read Request.
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	This is request from processor 5 to mss_cr5a. Mailbox Read Request.
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	This is request from processor 4 to mss_cr5a. Mailbox Read Request.
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	This is request from processor 3 to mss_cr5a. Mailbox Read Request.
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	This is request from processor 2 to mss_cr5a. Mailbox Read Request.
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	This is request from processor 1 to mss_cr5a. Mailbox Read Request.
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	This is request from processor 0 to mss_cr5a. Mailbox Read Request.

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2.3.97 MSS_CTRL_R5SS0_CORE0_MBOX_READ_DONE_ACK Registers

2.3.97.1 MSS_R5SS0_CORE0_MBOX_READ_DONE_ACK Register (Offset = 4008h) [reset = h]

Short Description: R5SS0_CORE0_MBOX_READ_DONE_ACK register

Long Description:

Return to Summary Table

Table 2-293. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4008h

Access Types Legend

Table 2-294. R5SS0_CORE0_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	PROC	RW	0h	Write pulse bit field: For bits 0 to 7: Writing 1'b1 generates pulse interrupt to corresponding processors from MSS_CR5

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2.3.98 MSS_CTRL_R5SS0_CORE0_MBOX_READ_DONE Registers

2.3.98.1 MSS_R5SS0_CORE0_MBOX_READ_DONE Register (Offset = 400Ch) [reset = h]

Short Description: R5SS0_CORE0_MBOX_READ_DONE register

Long Description:

Return to Summary Table

Table 2-295. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 400Ch

Access Types Legend

Table 2-296. R5SS0_CORE0_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	This register should be written once read is complete from CR5A's mailbox written by processors 7
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	This register should be written once read is complete from CR5A's mailbox written by processors 6
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	This register should be written once read is complete from CR5A's mailbox written by processors 5
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	This register should be written once read is complete from CR5A's mailbox written by processors 4
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	This register should be written once read is complete from CR5A's mailbox written by processors 3
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	This register should be written once read is complete from CR5A's mailbox written by processors 2
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	This register should be written once read is complete from CR5A's mailbox written by processors 1
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	This register should be written once read is complete from CR5A's mailbox written by processors 0

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2.3.99 MSS_CTRL_R5SS0_CORE0_SW_INT Registers

2.3.99.1 MSS_R5SS0_CORE0_SW_INT Register (Offset = 4010h) [reset = h]

Short Description: R5SS0_CORE0_SW_INT register

Long Description:

Return to Summary Table

Table 2-297. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4010h

Access Types Legend

Table 2-298. R5SS0_CORE0_SW_INT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	PULSE	RW	0h	Write_pulse bit field : Writing 1'b1 to each bit will trigger MSS_SW_INT respectively to CR5A/B.

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2.3.100 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK Registers

2.3.100.1 MSS_MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK Register (Offset = 4020h) [reset = h]

Short Description: MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK register

Long Description:

Return to Summary Table

Table 2-299. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4020h

Access Types Legend

Table 2-300. MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
16	MPU_CR5B1_AHB_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG1 • 1" Error is Masked • 0: Error is Unmasked
15	MPU_CR5A1_AHB_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
14	MPU_CR5B0_AHB_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
13	MPU_CR5A0_AHB_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
12	MPU_SCRM2SCRP1_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
11	MPU_SCRM2SCRP0_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
10	MPU_QSPI_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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Table 2-300. MPU_ADDR_ERRAGG_R5SS0_CPU0_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	MPU_MBOX_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
8	MPU_DTHE_A_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
7	MPU_CR5B1_AXIS_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
6	MPU_CR5A1_AXIS_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
5	MPU_CR5B0_AXIS_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
4	MPU_CR5A0_AXIS_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
3	MPU_L2_BANK_D_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
2	MPU_L2_BANK_C_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
1	MPU_L2_BANK_B_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
0	MPU_L2_BANK_A_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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2.3.101 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS Registers

2.3.101.1 MSS_MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS Register (Offset = 4024h) [reset = h]

Short Description: MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS register

Long Description:

Return to Summary Table

Table 2-301. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4024h

Access Types Legend

Table 2-302. MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
16	MPU_CR5B1_AHB_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
15	MPU_CR5A1_AHB_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
14	MPU_CR5B0_AHB_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
13	MPU_CR5A0_AHB_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
12	MPU_SCRM2SCRP1_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
11	MPU_SCRM2SCRP0_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
10	MPU_QSPI_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
9	MPU_MBOX_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
8	MPU_DTHE_A_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
7	MPU_CR5B1_AXIS_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
6	MPU_CR5A1_AXIS_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
5	MPU_CR5B0_AXIS_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
4	MPU_CR5A0_AXIS_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.

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Table 2-302. MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MPU_L2_BANK_D_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
2	MPU_L2_BANK_C_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
1	MPU_L2_BANK_B_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
0	MPU_L2_BANK_A_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.

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2.3.102 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW Registers

2.3.102.1 MSS_MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW Register (Offset = 4028h) [reset = h]

Short Description: MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-303. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4028h

Access Types Legend

Table 2-304. MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
16	MPU_CR5B1_AHB_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
15	MPU_CR5A1_AHB_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
14	MPU_CR5B0_AHB_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
13	MPU_CR5A0_AHB_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
12	MPU_SCRM2SCRP1_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
11	MPU_SCRM2SCRP0_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
10	MPU_QSPI_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
9	MPU_MBOX_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
8	MPU_DTHE_A_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
7	MPU_CR5B1_AXIS_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
6	MPU_CR5A1_AXIS_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
5	MPU_CR5B0_AXIS_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
4	MPU_CR5A0_AXIS_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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Table 2-304. MPU_ADDR_ERRAGG_R5SS0_CPU0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MPU_L2_BANK_D_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
2	MPU_L2_BANK_C_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
1	MPU_L2_BANK_B_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
0	MPU_L2_BANK_A_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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2.3.103 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CPU0_MASK Registers

2.3.103.1 MSS_MPU_PROT_ERRAGG_R5SS0_CPU0_MASK Register (Offset = 4030h) [reset = h]

Short Description: MPU_PROT_ERRAGG_R5SS0_CPU0_MASK register

Long Description:

Return to Summary Table

Table 2-305. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4030h

Access Types Legend

Table 2-306. MPU_PROT_ERRAGG_R5SS0_CPU0_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
16	MPU_CR5B1_AHB_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
15	MPU_CR5A1_AHB_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
14	MPU_CR5B0_AHB_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
13	MPU_CR5A0_AHB_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
12	MPU_SCRM2SCRP1_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
11	MPU_SCRM2SCRP0_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
10	MPU_QSPI_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
9	MPU_MBOX_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG#br#1 : Error is Masked#br#0 : Error is Unmasked

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Table 2-306. MPU_PROT_ERRAGG_R5SS0_CPU0_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	MPU_DTHE_A_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
7	MPU_CR5B1_AXIS_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
6	MPU_CR5A1_AXIS_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
5	MPU_CR5B0_AXIS_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
4	MPU_CR5A0_AXIS_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
3	MPU_L2_BANK_D_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
2	MPU_L2_BANK_C_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
1	MPU_L2_BANK_B_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
0	MPU_L2_BANK_A_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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2.3.104 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS Registers

2.3.104.1 MSS_MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS Register (Offset = 4034h) [reset = h]

Short Description: MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS register

Long Description:

Return to Summary Table

Table 2-307. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4034h

Access Types Legend

Table 2-308. MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
16	MPU_CR5B1_AHB_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
15	MPU_CR5A1_AHB_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
14	MPU_CR5B0_AHB_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
13	MPU_CR5A0_AHB_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
12	MPU_SCRM2SCRP1_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
11	MPU_SCRM2SCRP0_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
10	MPU_QSPI_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
9	MPU_MBOX_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
8	MPU_DTHE_A_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
7	MPU_CR5B1_AXIS_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
6	MPU_CR5A1_AXIS_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
5	MPU_CR5B0_AXIS_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
4	MPU_CR5A0_AXIS_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.

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Table 2-308. MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MPU_L2_BANK_D_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
2	MPU_L2_BANK_C_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
1	MPU_L2_BANK_B_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
0	MPU_L2_BANK_A_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.

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2.3.105 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW Registers

2.3.105.1 MSS_MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW Register (Offset = 4038h) [reset = h]

Short Description: MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-309. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 4038h

Access Types Legend

Table 2-310. MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
16	MPU_CR5B1_AHB_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
15	MPU_CR5A1_AHB_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
14	MPU_CR5B0_AHB_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
13	MPU_CR5A0_AHB_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
12	MPU_SCRM2SCRP1_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
11	MPU_SCRM2SCRP0_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
10	MPU_QSPI_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
9	MPU_MBOX_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
8	MPU_DTHE_A_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
7	MPU_CR5B1_AXIS_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
6	MPU_CR5A1_AXIS_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
5	MPU_CR5B0_AXIS_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
4	MPU_CR5A0_AXIS_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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Table 2-310. MPU_PROT_ERRAGG_R5SS0_CPU0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MPU_L2_BANK_D_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
2	MPU_L2_BANK_C_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
1	MPU_L2_BANK_B_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
0	MPU_L2_BANK_A_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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2.3.106 MSS_CTRL_R5SS0_CORE1_MBOX_WRITE_DONE Registers

2.3.106.1 MSS_R5SS0_CORE1_MBOX_WRITE_DONE Register (Offset = 8000h) [reset = h]

Short Description: R5SS0_CORE1_MBOX_WRITE_DONE register

Long Description:

Return to Summary Table

Table 2-311. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8000h

Access Types Legend

Table 2-312. R5SS0_CORE1_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 7
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 6
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 5
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 4
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 3
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 2
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	Write pulse bit field: This register should be written once finishing Writing into the mailbox memory of processor 1
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 0

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2.3.107 MSS_CTRL_R5SS0_CORE1_MBOX_READ_REQ Registers

2.3.107.1 MSS_R5SS0_CORE1_MBOX_READ_REQ Register (Offset = 8004h) [reset = h]

Short Description: R5SS0_CORE1_MBOX_READ_REQ register

Long Description:

Return to Summary Table

Table 2-313. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8004h

Access Types Legend

Table 2-314. R5SS0_CORE1_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	This is request from processor 7 to mss_CR5B. Mailbox Read Request.
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	This is request from processor 6 to mss_CR5B. Mailbox Read Request.
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	This is request from processor 5 to mss_CR5B. Mailbox Read Request.
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	This is request from processor 4 to mss_CR5B. Mailbox Read Request.
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	This is request from processor 3 to mss_CR5B. Mailbox Read Request.
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	This is request from processor 2 to mss_CR5B. Mailbox Read Request.
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	This is request from processor 1 to mss_CR5B. Mailbox Read Request.
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	This is request from processor 0 to mss_CR5B. Mailbox Read Request.

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2.3.108 MSS_CTRL_R5SS0_CORE1_MBOX_READ_DONE_ACK Registers

2.3.108.1 MSS_R5SS0_CORE1_MBOX_READ_DONE_ACK Register (Offset = 8008h) [reset = h]

Short Description: R5SS0_CORE1_MBOX_READ_DONE_ACK register

Long Description:

Return to Summary Table

Table 2-315. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8008h

Access Types Legend

Table 2-316. R5SS0_CORE1_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	PROC	RW	0h	Write pulse bit field: For bits 0 to 7:Writing 1'b1 generates pulse interrupt to corresponding processors from MSS_CR5

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2.3.109 MSS_CTRL_R5SS0_CORE1_MBOX_READ_DONE Registers

2.3.109.1 MSS_R5SS0_CORE1_MBOX_READ_DONE Register (Offset = 800Ch) [reset = h]

Short Description: R5SS0_CORE1_MBOX_READ_DONE register

Long Description:

Return to Summary Table

Table 2-317. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 800Ch

Access Types Legend

Table 2-318. R5SS0_CORE1_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	This register should be written once read is complete from CR5B's mailbox written by processors 7
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	This register should be written once read is complete from CR5B's mailbox written by processors 6
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	This register should be written once read is complete from CR5B's mailbox written by processors 5
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	This register should be written once read is complete from CR5B's mailbox written by processors 4
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	This register should be written once read is complete from CR5B's mailbox written by processors 3
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	This register should be written once read is complete from CR5B's mailbox written by processors 2
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	This register should be written once read is complete from CR5B's mailbox written by processors 1
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	This register should be written once read is complete from CR5B's mailbox written by processors 0

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2.3.110 MSS_CTRL_R5SS0_CORE1_SW_INT Registers

2.3.110.1 MSS_R5SS0_CORE1_SW_INT Register (Offset = 8010h) [reset = h]

Short Description: R5SS0_CORE1_SW_INT register

Long Description:

Return to Summary Table

Table 2-319. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8010h

Access Types Legend

Table 2-320. R5SS0_CORE1_SW_INT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	PULSE	RW	0h	Write_pulse bit field : Writing 1'b1 to each bit will trigger MSS_SW_INT respectively to CR5A/B.

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2.3.111 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK Registers

2.3.111.1 MSS_MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK Register (Offset = 8020h) [reset = h]

Short Description: MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK register

Long Description:

Return to Summary Table

Table 2-321. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8020h

Access Types Legend

Table 2-322. MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
16	MPU_CR5B1_AHB_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
15	MPU_CR5A1_AHB_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
14	MPU_CR5B0_AHB_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
13	MPU_CR5A0_AHB_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
12	MPU_SCRM2SCRP1_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
11	MPU_SCRM2SCRP0_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
10	MPU_QSPI_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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Table 2-322. MPU_ADDR_ERRAGG_R5SS0_CPU1_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	MPU_MBOX_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
8	MPU_DTHE_A_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
7	MPU_CR5B1_AXIS_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
6	MPU_CR5A1_AXIS_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
5	MPU_CR5B0_AXIS_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
4	MPU_CR5A0_AXIS_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
3	MPU_L2_BANK_D_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
2	MPU_L2_BANK_C_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
1	MPU_L2_BANK_B_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
0	MPU_L2_BANK_A_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG#br#1 : Error is Masked • 1: Error is Masked • 0: Error is Unmasked

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2.3.112 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS Registers

2.3.112.1 MSS_MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS Register (Offset = 8024h) [reset = h]

Short Description: MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS register

Long Description:

Return to Summary Table

Table 2-323. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8024h

Access Types Legend

Table 2-324. MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
16	MPU_CR5B1_AHB_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
15	MPU_CR5A1_AHB_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
14	MPU_CR5B0_AHB_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
13	MPU_CR5A0_AHB_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
12	MPU_SCRM2SCRP1_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
11	MPU_SCRM2SCRP0_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
10	MPU_QSPI_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
9	MPU_MBOX_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
8	MPU_DTHE_A_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
7	MPU_CR5B1_AXIS_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
6	MPU_CR5A1_AXIS_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
5	MPU_CR5B0_AXIS_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
4	MPU_CR5A0_AXIS_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.

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Table 2-324. MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MPU_L2_BANK_D_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
2	MPU_L2_BANK_C_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
1	MPU_L2_BANK_B_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
0	MPU_L2_BANK_A_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.

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2.3.113 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW Registers

2.3.113.1 MSS_MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW Register (Offset = 8028h) [reset = h]

Short Description: MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-325. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8028h

Access Types Legend

Table 2-326. MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
16	MPU_CR5B1_AHB_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
15	MPU_CR5A1_AHB_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
14	MPU_CR5B0_AHB_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
13	MPU_CR5A0_AHB_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
12	MPU_SCRM2SCRP1_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
11	MPU_SCRM2SCRP0_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
10	MPU_QSPI_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
9	MPU_MBOX_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
8	MPU_DTHE_A_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
7	MPU_CR5B1_AXIS_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
6	MPU_CR5A1_AXIS_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
5	MPU_CR5B0_AXIS_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
4	MPU_CR5A0_AXIS_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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Table 2-326. MPU_ADDR_ERRAGG_R5SS0_CPU1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MPU_L2_BANK_D_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
2	MPU_L2_BANK_C_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
1	MPU_L2_BANK_B_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
0	MPU_L2_BANK_A_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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2.3.114 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CPU1_MASK Registers

2.3.114.1 MSS_MPU_PROT_ERRAGG_R5SS0_CPU1_MASK Register (Offset = 8030h) [reset = h]

Short Description: MPU_PROT_ERRAGG_R5SS0_CPU1_MASK register

Long Description:

Return to Summary Table

Table 2-327. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8030h

Access Types Legend

Table 2-328. MPU_PROT_ERRAGG_R5SS0_CPU1_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
16	MPU_CR5B1_AHB_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
15	MPU_CR5A1_AHB_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
14	MPU_CR5B0_AHB_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
13	MPU_CR5A0_AHB_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
12	MPU_SCRM2SCRP1_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
11	MPU_SCRM2SCRP0_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
10	MPU_QSPI_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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Table 2-328. MPU_PROT_ERRAGG_R5SS0_CPU1_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	MPU_MBOX_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
8	MPU_DTHE_A_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
7	MPU_CR5B1_AXIS_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
6	MPU_CR5A1_AXIS_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
5	MPU_CR5B0_AXIS_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
4	MPU_CR5A0_AXIS_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
3	MPU_L2_BANK_D_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
2	MPU_L2_BANK_C_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
1	MPU_L2_BANK_B_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
0	MPU_L2_BANK_A_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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2.3.115 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS Registers

2.3.115.1 MSS_MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS Register (Offset = 8034h) [reset = h]

Short Description: MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS register

Long Description:

Return to Summary Table

Table 2-329. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8034h

Access Types Legend

Table 2-330. MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
16	MPU_CR5B1_AHB_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
15	MPU_CR5A1_AHB_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
14	MPU_CR5B0_AHB_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
13	MPU_CR5A0_AHB_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
12	MPU_SCRM2SCRP1_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
11	MPU_SCRM2SCRP0_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
10	MPU_QSPI_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
9	MPU_MBOX_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
8	MPU_DTHE_A_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
7	MPU_CR5B1_AXIS_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
6	MPU_CR5A1_AXIS_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
5	MPU_CR5B0_AXIS_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
4	MPU_CR5A0_AXIS_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.

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Table 2-330. MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MPU_L2_BANK_D_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
2	MPU_L2_BANK_C_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
1	MPU_L2_BANK_B_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
0	MPU_L2_BANK_A_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.

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2.3.116 MSS_CTRL_MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW Registers

2.3.116.1 MSS_MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW Register (Offset = 8038h) [reset = h]

Short Description: MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-331. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 8038h

Access Types Legend

Table 2-332. MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
16	MPU_CR5B1_AHB_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
15	MPU_CR5A1_AHB_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
14	MPU_CR5B0_AHB_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
13	MPU_CR5A0_AHB_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
12	MPU_SCRM2SCRP1_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
11	MPU_SCRM2SCRP0_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
10	MPU_QSPI_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
9	MPU_MBOX_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
8	MPU_DTHE_A_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
7	MPU_CR5B1_AXIS_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
6	MPU_CR5A1_AXIS_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
5	MPU_CR5B0_AXIS_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
4	MPU_CR5A0_AXIS_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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Table 2-332. MPU_PROT_ERRAGG_R5SS0_CPU1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MPU_L2_BANK_D_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
2	MPU_L2_BANK_C_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
1	MPU_L2_BANK_B_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
0	MPU_L2_BANK_A_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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2.3.117 MSS_CTRL_R5SS1_CORE0_MBOX_WRITE_DONE Registers

2.3.117.1 MSS_R5SS1_CORE0_MBOX_WRITE_DONE Register (Offset = C000h) [reset = h]

Short Description: R5SS1_CORE0_MBOX_WRITE_DONE register

Long Description:

Return to Summary Table

Table 2-333. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C000h

Access Types Legend

Table 2-334. R5SS1_CORE0_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 7
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 6
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 5
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 4
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 3
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 2
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 1
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 0

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2.3.118 MSS_CTRL_R5SS1_CORE0_MBOX_READ_REQ Registers

2.3.118.1 MSS_R5SS1_CORE0_MBOX_READ_REQ Register (Offset = C004h) [reset = h]

Short Description: R5SS1_CORE0_MBOX_READ_REQ register

Long Description:

Return to Summary Table

Table 2-335. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C004h

Access Types Legend

Table 2-336. R5SS1_CORE0_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	This is request from processor 7 to mss_cr5a. Mailbox Read Request.
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	This is request from processor 6 to mss_cr5a. Mailbox Read Request.
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	This is request from processor 5 to mss_cr5a. Mailbox Read Request.
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	This is request from processor 4 to mss_cr5a. Mailbox Read Request.
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	This is request from processor 3 to mss_cr5a. Mailbox Read Request.
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	This is request from processor 2 to mss_cr5a. Mailbox Read Request.
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	This is request from processor 1 to mss_cr5a. Mailbox Read Request.
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	This is request from processor 0 to mss_cr5a. Mailbox Read Request.

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2.3.119 MSS_CTRL_R5SS1_CORE0_MBOX_READ_DONE_ACK Registers

2.3.119.1 MSS_R5SS1_CORE0_MBOX_READ_DONE_ACK Register (Offset = C008h) [reset = h]

Short Description: R5SS1_CORE0_MBOX_READ_DONE_ACK register

Long Description:

Return to Summary Table

Table 2-337. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C008h

Access Types Legend

Table 2-338. R5SS1_CORE0_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	PROC	RW	0h	Write pulse bit field: For bits 0 to 7: Writing 1'b1 generates pulse interrupt to corresponding processors from MSS_CR5

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2.3.120 MSS_CTRL_R5SS1_CORE0_MBOX_READ_DONE Registers

2.3.120.1 MSS_R5SS1_CORE0_MBOX_READ_DONE Register (Offset = C00Ch) [reset = h]

Short Description: R5SS1_CORE0_MBOX_READ_DONE register

Long Description:

Return to Summary Table

Table 2-339. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C00Ch

Access Types Legend

Table 2-340. R5SS1_CORE0_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	This register should be written once read is complete from CR5A's mailbox written by processors 7
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	This register should be written once read is complete from CR5A's mailbox written by processors 6
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	This register should be written once read is complete from CR5A's mailbox written by processors 5
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	This register should be written once read is complete from CR5A's mailbox written by processors 4
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	This register should be written once read is complete from CR5A's mailbox written by processors 3
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	This register should be written once read is complete from CR5A's mailbox written by processors 2
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	This register should be written once read is complete from CR5A's mailbox written by processors 1
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	This register should be written once read is complete from CR5A's mailbox written by processors 0

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2.3.121 MSS_CTRL_R5SS1_CORE0_SW_INT Registers

2.3.121.1 MSS_R5SS1_CORE0_SW_INT Register (Offset = C010h) [reset = h]

Short Description: R5SS1_CORE0_SW_INT register

Long Description:

Return to Summary Table

Table 2-341. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C010h

Access Types Legend

Table 2-342. R5SS1_CORE0_SW_INT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	PULSE	RW	0h	Write_pulse bit field : Writing 1'b1 to each bit will trigger MSS_SW_INT respectively to CR5A/B.

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2.3.122 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK Registers

2.3.122.1 MSS_MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK Register (Offset = C020h) [reset = h]

Short Description: MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK register

Long Description:

Return to Summary Table

Table 2-343. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C020h

Access Types Legend

Table 2-344. MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
16	MPU_CR5B1_AHB_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
15	MPU_CR5A1_AHB_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
14	MPU_CR5B0_AHB_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
13	MPU_CR5A0_AHB_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
12	MPU_SCRM2SCRP1_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
11	MPU_SCRM2SCRP0_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
10	MPU_QSPI_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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Table 2-344. MPU_ADDR_ERRAGG_R5SS1_CPU0_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	MPU_MBOX_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
8	MPU_DTHE_A_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
7	MPU_CR5B1_AXIS_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
6	MPU_CR5A1_AXIS_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
5	MPU_CR5B0_AXIS_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
4	MPU_CR5A0_AXIS_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
3	MPU_L2_BANK_D_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
2	MPU_L2_BANK_C_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
1	MPU_L2_BANK_B_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
0	MPU_L2_BANK_A_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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2.3.123 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS Registers

2.3.123.1 MSS_MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS Register (Offset = C024h) [reset = h]

Short Description: MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS register

Long Description:

Return to Summary Table

Table 2-345. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C024h

Access Types Legend

Table 2-346. MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
16	MPU_CR5B1_AHB_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
15	MPU_CR5A1_AHB_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
14	MPU_CR5B0_AHB_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
13	MPU_CR5A0_AHB_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
12	MPU_SCRM2SCRP1_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
11	MPU_SCRM2SCRP0_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
10	MPU_QSPI_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
9	MPU_MBOX_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
8	MPU_DTHE_A_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
7	MPU_CR5B1_AXIS_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
6	MPU_CR5A1_AXIS_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
5	MPU_CR5B0_AXIS_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
4	MPU_CR5A0_AXIS_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.

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Table 2-346. MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MPU_L2_BANK_D_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
2	MPU_L2_BANK_C_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
1	MPU_L2_BANK_B_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
0	MPU_L2_BANK_A_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.

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2.3.124 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW Registers

2.3.124.1 MSS_MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW Register (Offset = C028h) [reset = h]

Short Description: MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-347. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C028h

Access Types Legend

Table 2-348. MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
16	MPU_CR5B1_AHB_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
15	MPU_CR5A1_AHB_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
14	MPU_CR5B0_AHB_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
13	MPU_CR5A0_AHB_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
12	MPU_SCRM2SCRP1_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
11	MPU_SCRM2SCRP0_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
10	MPU_QSPI_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
9	MPU_MBOX_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
8	MPU_DTHE_A_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
7	MPU_CR5B1_AXIS_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
6	MPU_CR5A1_AXIS_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
5	MPU_CR5B0_AXIS_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
4	MPU_CR5A0_AXIS_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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Table 2-348. MPU_ADDR_ERRAGG_R5SS1_CPU0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MPU_L2_BANK_D_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
2	MPU_L2_BANK_C_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
1	MPU_L2_BANK_B_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
0	MPU_L2_BANK_A_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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2.3.125 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CPU0_MASK Registers

2.3.125.1 MSS_MPU_PROT_ERRAGG_R5SS1_CPU0_MASK Register (Offset = C030h) [reset = h]

Short Description: MPU_PROT_ERRAGG_R5SS1_CPU0_MASK register

Long Description:

Return to Summary Table

Table 2-349. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C030h

Access Types Legend

Table 2-350. MPU_PROT_ERRAGG_R5SS1_CPU0_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
16	MPU_CR5B1_AHB_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
15	MPU_CR5A1_AHB_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
14	MPU_CR5B0_AHB_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
13	MPU_CR5A0_AHB_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
12	MPU_SCRM2SCRP1_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
11	MPU_SCRM2SCRP0_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
10	MPU_QSPI_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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Table 2-350. MPU_PROT_ERRAGG_R5SS1_CPU0_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	MPU_MBOX_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
8	MPU_DTHE_A_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
7	MPU_CR5B1_AXIS_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
6	MPU_CR5A1_AXIS_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
5	MPU_CR5B0_AXIS_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
4	MPU_CR5A0_AXIS_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
3	MPU_L2_BANK_D_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
2	MPU_L2_BANK_C_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
1	MPU_L2_BANK_B_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
0	MPU_L2_BANK_A_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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2.3.126 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS Registers

2.3.126.1 MSS_MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS Register (Offset = C034h) [reset = h]

Short Description: MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS register

Long Description:

Return to Summary Table

Table 2-351. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C034h

Access Types Legend

Table 2-352. MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
16	MPU_CR5B1_AHB_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
15	MPU_CR5A1_AHB_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
14	MPU_CR5B0_AHB_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
13	MPU_CR5A0_AHB_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
12	MPU_SCRM2SCRP1_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
11	MPU_SCRM2SCRP0_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
10	MPU_QSPI_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
9	MPU_MBOX_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
8	MPU_DTHE_A_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
7	MPU_CR5B1_AXIS_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
6	MPU_CR5A1_AXIS_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
5	MPU_CR5B0_AXIS_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
4	MPU_CR5A0_AXIS_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.

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Table 2-352. MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MPU_L2_BANK_D_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
2	MPU_L2_BANK_C_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
1	MPU_L2_BANK_B_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
0	MPU_L2_BANK_A_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.

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2.3.127 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW Registers

2.3.127.1 MSS_MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW Register (Offset = C038h) [reset = h]

Short Description: MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-353. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D0 C038h

Access Types Legend

Table 2-354. MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
16	MPU_CR5B1_AHB_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
15	MPU_CR5A1_AHB_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
14	MPU_CR5B0_AHB_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
13	MPU_CR5A0_AHB_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
12	MPU_SCRM2SCRP1_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
11	MPU_SCRM2SCRP0_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
10	MPU_QSPI_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
9	MPU_MBOX_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
8	MPU_DTHE_A_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
7	MPU_CR5B1_AXIS_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
6	MPU_CR5A1_AXIS_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
5	MPU_CR5B0_AXIS_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
4	MPU_CR5A0_AXIS_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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Table 2-354. MPU_PROT_ERRAGG_R5SS1_CPU0_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MPU_L2_BANK_D_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
2	MPU_L2_BANK_C_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
1	MPU_L2_BANK_B_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
0	MPU_L2_BANK_A_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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2.3.128 MSS_CTRL_R5SS1_CORE1_MBOX_WRITE_DONE Registers

2.3.128.1 MSS_R5SS1_CORE1_MBOX_WRITE_DONE Register (Offset = 10000h) [reset = h]

Short Description: R5SS1_CORE1_MBOX_WRITE_DONE register

Long Description:

Return to Summary Table

Table 2-355. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0000h

Access Types Legend

Table 2-356. R5SS1_CORE1_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 7
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 6
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 5
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 4
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 3
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 2
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 1
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 0

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2.3.129 MSS_CTRL_R5SS1_CORE1_MBOX_READ_REQ Registers

2.3.129.1 MSS_R5SS1_CORE1_MBOX_READ_REQ Register (Offset = 10004h) [reset = h]

Short Description: R5SS1_CORE1_MBOX_READ_REQ register

Long Description:

Return to Summary Table

Table 2-357. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0004h

Access Types Legend

Table 2-358. R5SS1_CORE1_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	This is request from processor 7 to mss_CR5B. Mailbox Read Request.
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	This is request from processor 6 to mss_CR5B. Mailbox Read Request.
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	This is request from processor 5 to mss_CR5B. Mailbox Read Request.
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	This is request from processor 4 to mss_CR5B. Mailbox Read Request.
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	This is request from processor 3 to mss_CR5B. Mailbox Read Request.
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	This is request from processor 2 to mss_CR5B. Mailbox Read Request.
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	This is request from processor 1 to mss_CR5B. Mailbox Read Request.
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	This is request from processor 0 to mss_CR5B. Mailbox Read Request.

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2.3.130 MSS_CTRL_R5SS1_CORE1_MBOX_READ_DONE_ACK Registers

2.3.130.1 MSS_R5SS1_CORE1_MBOX_READ_DONE_ACK Register (Offset = 10008h) [reset = h]

Short Description: R5SS1_CORE1_MBOX_READ_DONE_ACK register

Long Description:

Return to Summary Table

Table 2-359. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0008h

Access Types Legend

Table 2-360. R5SS1_CORE1_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	PROC	RW	0h	Write pulse bit field: For bits 0 to 7. Writing 1'b1 generates pulse interrupt to corresponding processors from MSS_CR5

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2.3.131 MSS_CTRL_R5SS1_CORE1_MBOX_READ_DONE Registers

2.3.131.1 MSS_R5SS1_CORE1_MBOX_READ_DONE Register (Offset = 1000Ch) [reset = h]

Short Description: R5SS1_CORE1_MBOX_READ_DONE register

Long Description:

Return to Summary Table

Table 2-361. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 000Ch

Access Types Legend

Table 2-362. R5SS1_CORE1_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	This register should be written once read is complete from CR5B's mailbox written by processors 7
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	This register should be written once read is complete from CR5B's mailbox written by processors 6
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	This register should be written once read is complete from CR5B's mailbox written by processors 5
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	This register should be written once read is complete from CR5B's mailbox written by processors 4
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	This register should be written once read is complete from CR5B's mailbox written by processors 3
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	This register should be written once read is complete from CR5B's mailbox written by processors 2
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	This register should be written once read is complete from CR5B's mailbox written by processors 1
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	This register should be written once read is complete from CR5B's mailbox written by processors 0

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2.3.132 MSS_CTRL_R5SS1_CORE1_SW_INT Registers

2.3.132.1 MSS_R5SS1_CORE1_SW_INT Register (Offset = 10010h) [reset = h]

Short Description: R5SS1_CORE1_SW_INT register

Long Description:

Return to Summary Table

Table 2-363. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0010h

Access Types Legend

Table 2-364. R5SS1_CORE1_SW_INT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	PULSE	RW	0h	Write_pulse bit field : Writing 1'b1 to each bit will trigger MSS_SW_INT respectively to CR5A/B.

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2.3.133 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK Registers

2.3.133.1 MSS_MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK Register (Offset = 10020h) [reset = h]

Short Description: MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK register

Long Description:

Return to Summary Table

Table 2-365. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0020h

Access Types Legend

Table 2-366. MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
16	MPU_CR5B1_AHB_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
15	MPU_CR5A1_AHB_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
14	MPU_CR5B0_AHB_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
13	MPU_CR5A0_AHB_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
12	MPU_SCRM2SCRP1_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
11	MPU_SCRM2SCRP0_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
10	MPU_QSPI_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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Table 2-366. MPU_ADDR_ERRAGG_R5SS1_CPU1_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	MPU_MBOX_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
8	MPU_DTHE_A_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
7	MPU_CR5B1_AXIS_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
6	MPU_CR5A1_AXIS_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
5	MPU_CR5B0_AXIS_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
4	MPU_CR5A0_AXIS_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
3	MPU_L2_BANK_D_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
2	MPU_L2_BANK_C_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
1	MPU_L2_BANK_B_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
0	MPU_L2_BANK_A_ADDR_ERR	RW	0h	Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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2.3.134 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS Registers

2.3.134.1 MSS_MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS Register (Offset = 10024h) [reset = h]

Short Description: MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS register

Long Description:

Return to Summary Table

Table 2-367. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0024h

Access Types Legend

Table 2-368. MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
16	MPU_CR5B1_AHB_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
15	MPU_CR5A1_AHB_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
14	MPU_CR5B0_AHB_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
13	MPU_CR5A0_AHB_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
12	MPU_SCRM2SCRP1_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
11	MPU_SCRM2SCRP0_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
10	MPU_QSPI_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
9	MPU_MBOX_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
8	MPU_DTHE_A_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
7	MPU_CR5B1_AXIS_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
6	MPU_CR5A1_AXIS_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
5	MPU_CR5B0_AXIS_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
4	MPU_CR5A0_AXIS_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.

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Table 2-368. MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MPU_L2_BANK_D_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
2	MPU_L2_BANK_C_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
1	MPU_L2_BANK_B_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
0	MPU_L2_BANK_A_ADDR_ERR	RW	0h	Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.

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2.3.135 MSS_CTRL_MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW Registers

2.3.135.1 MSS_MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW Register (Offset = 10028h) [reset = h]

Short Description: MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-369. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0028h

Access Types Legend

Table 2-370. MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
16	MPU_CR5B1_AHB_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
15	MPU_CR5A1_AHB_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
14	MPU_CR5B0_AHB_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
13	MPU_CR5A0_AHB_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
12	MPU_SCRM2SCRP1_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
11	MPU_SCRM2SCRP0_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
10	MPU_QSPI_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
9	MPU_MBOX_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
8	MPU_DTHE_A_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
7	MPU_CR5B1_AXIS_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
6	MPU_CR5A1_AXIS_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
5	MPU_CR5B0_AXIS_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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Table 2-370. MPU_ADDR_ERRAGG_R5SS1_CPU1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	MPU_CR5A0_AXIS_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
3	MPU_L2_BANK_D_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
2	MPU_L2_BANK_C_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
1	MPU_L2_BANK_B_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK
0	MPU_L2_BANK_A_ADDR_ERR	RW	0h	Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK

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2.3.136 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CPU1_MASK Registers

2.3.136.1 MSS_MPU_PROT_ERRAGG_R5SS1_CPU1_MASK Register (Offset = 10030h) [reset = h]

Short Description: MPU_PROT_ERRAGG_R5SS1_CPU1_MASK register

Long Description:

Return to Summary Table

Table 2-371. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0030h

Access Types Legend

Table 2-372. MPU_PROT_ERRAGG_R5SS1_CPU1_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
16	MPU_CR5B1_AHB_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
15	MPU_CR5A1_AHB_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
14	MPU_CR5B0_AHB_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
13	MPU_CR5A0_AHB_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
12	MPU_SCRM2SCRP1_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
11	MPU_SCRM2SCRP0_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
10	MPU_QSPI_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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Table 2-372. MPU_PROT_ERRAGG_R5SS1_CPU1_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	MPU_MBOX_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
8	MPU_DTHE_A_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
7	MPU_CR5B1_AXIS_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
6	MPU_CR5A1_AXIS_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
5	MPU_CR5B0_AXIS_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
4	MPU_CR5A0_AXIS_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
3	MPU_L2_BANK_D_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
2	MPU_L2_BANK_C_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
1	MPU_L2_BANK_B_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
0	MPU_L2_BANK_A_PROT_ERR	RW	0h	Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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2.3.137 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS Registers

2.3.137.1 MSS_MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS Register (Offset = 10034h) [reset = h]

Short Description: MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS register

Long Description:

Return to Summary Table

Table 2-373. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0034h

Access Types Legend

Table 2-374. MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
16	MPU_CR5B1_AHB_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
15	MPU_CR5A1_AHB_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
14	MPU_CR5B0_AHB_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
13	MPU_CR5A0_AHB_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
12	MPU_SCRM2SCRP1_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
11	MPU_SCRM2SCRP0_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
10	MPU_QSPI_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
9	MPU_MBOX_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
8	MPU_DTHE_A_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
7	MPU_CR5B1_AXIS_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
6	MPU_CR5A1_AXIS_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
5	MPU_CR5B0_AXIS_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
4	MPU_CR5A0_AXIS_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.

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Table 2-374. MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MPU_L2_BANK_D_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
2	MPU_L2_BANK_C_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
1	MPU_L2_BANK_B_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.
0	MPU_L2_BANK_A_PROT_ERR	RW	0h	Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error.

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2.3.138 MSS_CTRL_MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW Registers

2.3.138.1 MSS_MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW Register (Offset = 10038h) [reset = h]

Short Description: MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-375. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 0038h

Access Types Legend

Table 2-376. MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	MPU_HSM_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
16	MPU_CR5B1_AHB_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
15	MPU_CR5A1_AHB_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
14	MPU_CR5B0_AHB_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
13	MPU_CR5A0_AHB_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
12	MPU_SCRM2SCRP1_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
11	MPU_SCRM2SCRP0_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
10	MPU_QSPI_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
9	MPU_MBOX_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
8	MPU_DTHE_A_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
7	MPU_CR5B1_AXIS_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
6	MPU_CR5A1_AXIS_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
5	MPU_CR5B0_AXIS_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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Table 2-376. MPU_PROT_ERRAGG_R5SS1_CPU1_STATUS_RAW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	MPU_CR5A0_AXIS_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
3	MPU_L2_BANK_D_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
2	MPU_L2_BANK_C_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
1	MPU_L2_BANK_B_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK
0	MPU_L2_BANK_A_PROT_ERR	RW	0h	Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK

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2.3.139 MSS_CTRL_ICSSM_PRU0_MBOX_WRITE_DONE Registers

2.3.139.1 MSS_ICSSM_PRU0_MBOX_WRITE_DONE Register (Offset = 14000h) [reset = h]

Short Description: ICSSM_PRU0_MBOX_WRITE_DONE register

Long Description:

Return to Summary Table

Table 2-377. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 4000h

Access Types Legend

Table 2-378. ICSSM_PRU0_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 7
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 6
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 5
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 4
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 3
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 2
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 1
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 0

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2.3.140 MSS_CTRL_ICSSM_PRU0_MBOX_READ_REQ Registers

2.3.140.1 MSS_ICSSM_PRU0_MBOX_READ_REQ Register (Offset = 14004h) [reset = h]

Short Description: ICSSM_PRU0_MBOX_READ_REQ register

Long Description:

Return to Summary Table

Table 2-379. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 4004h

Access Types Legend

Table 2-380. ICSSM_PRU0_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	This is request from processor 7 to corresponding ICSSM_PRU. Mailbox Read Request.
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	This is request from processor 6 to corresponding ICSSM_PRU. Mailbox Read Request.
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	This is request from processor 5 to corresponding ICSSM_PRU. Mailbox Read Request.
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	This is request from processor 4 to corresponding ICSSM_PRU. Mailbox Read Request.
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	This is request from processor 3 to corresponding ICSSM_PRU. Mailbox Read Request.
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	This is request from processor 2 to corresponding ICSSM_PRU. Mailbox Read Request.
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	This is request from processor 1 to corresponding ICSSM_PRU. Mailbox Read Request.
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	This is request from processor 0 to corresponding ICSSM_PRU. Mailbox Read Request.

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2.3.141 MSS_CTRL_ICSSM_PRU0_MBOX_READ_DONE_ACK Registers

2.3.141.1 MSS_ICSSM_PRU0_MBOX_READ_DONE_ACK Register (Offset = 14008h) [reset = h]

Short Description: ICSSM_PRU0_MBOX_READ_DONE_ACK register

Long Description:

Return to Summary Table

Table 2-381. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 4008h

Access Types Legend

Table 2-382. ICSSM_PRU0_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	PROC	RW	0h	Write pulse bit field: For bits 0 to 7:Writing 1'b1 : Generates pulse interrupt to corresponding processors from ICSSM_PRU0. For bits 8 to 15:Writing 1'b1 : Generates pulse interrupt to corresponding processors from ICSSM_PRU1.

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2.3.142 MSS_CTRL_ICSSM_PRU0_MBOX_READ_DONE Registers

2.3.142.1 MSS_ICSSM_PRU0_MBOX_READ_DONE Register (Offset = 1400Ch) [reset = h]

Short Description: ICSSM_PRU0_MBOX_READ_DONE register

Long Description:

Return to Summary Table

Table 2-383. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 400Ch

Access Types Legend

Table 2-384. ICSSM_PRU0_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	This register should be written once read is complete from corresponding ICSSM_PRU's mailbox written by processors 7
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	This register should be written once read is complete from corresponding ICSSM_PRU's mailbox written by processors 6
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	This register should be written once read is complete from corresponding ICSSM_PRU's mailbox written by processors 5
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	This register should be written once read is complete from corresponding ICSSM_PRU's mailbox written by processors 4
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	This register should be written once read is complete from corresponding ICSSM_PRU's mailbox written by processors 3
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	This register should be written once read is complete from corresponding ICSSM_PRU's mailbox written by processors 2
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	This register should be written once read is complete from corresponding ICSSM_PRU's mailbox written by processors 1
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	This register should be written once read is complete from corresponding ICSSM_PRU's mailbox written by processors 0

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2.3.143 MSS_CTRL_ICSSM_PRU1_MBOX_WRITE_DONE Registers

2.3.143.1 MSS_ICSSM_PRU1_MBOX_WRITE_DONE Register (Offset = 14010h) [reset = h]

Short Description: ICSSM_PRU1_MBOX_WRITE_DONE register

Long Description:

Return to Summary Table

Table 2-385. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 4010h

Access Types Legend

Table 2-386. ICSSM_PRU1_MBOX_WRITE_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 7
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 6
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 5
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 4
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 3
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 2
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 1
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	Write pulse bit field:This register should be written once finishing Writing into the mailbox memory of processor 0

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2.3.144 MSS_CTRL_ICSSM_PRU1_MBOX_READ_REQ Registers

2.3.144.1 MSS_ICSSM_PRU1_MBOX_READ_REQ Register (Offset = 14014h) [reset = h]

Short Description: ICSSM_PRU1_MBOX_READ_REQ register

Long Description:

Return to Summary Table

Table 2-387. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 4014h

Access Types Legend

Table 2-388. ICSSM_PRU1_MBOX_READ_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	This is request from processor 7 to corresponding ICSSM_PRU. Mailbox Read Request.
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	This is request from processor 6 to corresponding ICSSM_PRU. Mailbox Read Request.
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	This is request from processor 5 to corresponding ICSSM_PRU. Mailbox Read Request.
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	This is request from processor 4 to corresponding ICSSM_PRU. Mailbox Read Request.
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	This is request from processor 3 to corresponding ICSSM_PRU. Mailbox Read Request.
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	This is request from processor 2 to corresponding ICSSM_PRU. Mailbox Read Request.
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	This is request from processor 1 to corresponding ICSSM_PRU. Mailbox Read Request.
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	This is request from processor 0 to corresponding ICSSM_PRU. Mailbox Read Request.

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2.3.145 MSS_CTRL_ICSSM_PRU1_MBOX_READ_DONE_ACK Registers

2.3.145.1 MSS_ICSSM_PRU1_MBOX_READ_DONE_ACK Register (Offset = 14018h) [reset = h]

Short Description: ICSSM_PRU1_MBOX_READ_DONE_ACK register

Long Description:

Return to Summary Table

Table 2-389. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 4018h

Access Types Legend

Table 2-390. ICSSM_PRU1_MBOX_READ_DONE_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	PROC	RW	0h	Write pulse bit field: For bits 0 to 7:Writing 1'b1 : Generates pulse interrupt to corresponding processors from ICSSM_PRU0. For bits 8 to 15:Writing 1'b1 : Generates pulse interrupt to corresponding processors from ICSSM_PRU1.

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2.3.146 MSS_CTRL_ICSSM_PRU1_MBOX_READ_DONE Registers

2.3.146.1 MSS_ICSSM_PRU1_MBOX_READ_DONE Register (Offset = 1401Ch) [reset = h]

Short Description: ICSSM_PRU1_MBOX_READ_DONE register

Long Description:

Return to Summary Table

Table 2-391. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 401Ch

Access Types Legend

Table 2-392. ICSSM_PRU1_MBOX_READ_DONE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28	PROC_7	RW	0h	This register should be written once read is complete from corresponding ICSSM_PRU's mailbox written by processors 7
	RESERVED	NONE		Reserved
24	PROC_6	RW	0h	This register should be written once read is complete from corresponding ICSSM_PRU's mailbox written by processors 6
	RESERVED	NONE		Reserved
20	PROC_5	RW	0h	This register should be written once read is complete from corresponding ICSSM_PRU's mailbox written by processors 5
	RESERVED	NONE		Reserved
16	PROC_4	RW	0h	This register should be written once read is complete from corresponding ICSSM_PRU's mailbox written by processors 4
	RESERVED	NONE		Reserved
12	PROC_3	RW	0h	This register should be written once read is complete from corresponding ICSSM_PRU's mailbox written by processors 3
	RESERVED	NONE		Reserved
8	PROC_2	RW	0h	This register should be written once read is complete from corresponding ICSSM_PRU's mailbox written by processors 2
	RESERVED	NONE		Reserved
4	PROC_1	RW	0h	This register should be written once read is complete from corresponding ICSSM_PRU's mailbox written by processors 1
	RESERVED	NONE		Reserved
0	PROC_0	RW	0h	This register should be written once read is complete from corresponding ICSSM_PRU's mailbox written by processors 0

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2.3.147 MSS_CTRL_TPCC0_ERRAGG_MASK Registers

2.3.147.1 MSS_TPCC0_ERRAGG_MASK Register (Offset = 18000h) [reset = h]

Short Description: TPCC0_ERRAGG_MASK register

Long Description:

Return to Summary Table

Table 2-393. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8000h

Access Types Legend

Table 2-394. TPCC0_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
26	TPTC_A1_READ_ACCESS_ERROR	RW	0h	Mask Error from MSS_TPTC_A1 to aggregated Error MSS_TPCC_A_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
25	TPTC_A0_READ_ACCESS_ERROR	RW	0h	Mask Error from MSS_TPTC_A0 to aggregated Error MSS_TPCC_A_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
24	TPCC_A_READ_ACCESS_ERROR	RW	0h	Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
	RESERVED	NONE		Reserved
18	TPTC_A1_WRITE_ACCESS_ERROR	RW	0h	Mask Error from MSS_TPTC_A1 to aggregated Error MSS_TPCC_A_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
17	TPTC_A0_WRITE_ACCESS_ERROR	RW	0h	Mask Error from MSS_TPTC_A0 to aggregated Error MSS_TPCC_A_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
16	TPCC_A_WRITE_ACCESS_ERROR	RW	0h	Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
	RESERVED	NONE		Reserved
4	TPCC_A_PAR_ERR	RW	0h	Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
3	TPTC_A1_ERR	RW	0h	Mask Error from MSS_TPTC_A1 to aggregated Error MSS_TPCC_A_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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Table 2-394. TPCC0_ERRAGG_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TPTC_A0_ERR	RW	0h	Mask Error from MSS_TPTC_A0 to aggregated Error MSS_TPCC_A_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
1	TPCC_A_MPINT	RW	0h	Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
0	TPCC_A_ERRINT	RW	0h	Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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2.3.148 MSS_CTRL_TPCC0_ERRAGG_STATUS Registers

2.3.148.1 MSS_TPCC0_ERRAGG_STATUS Register (Offset = 18004h) [reset = h]

Short Description: TPCC0_ERRAGG_STATUS register

Long Description:

Return to Summary Table

Table 2-395. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8004h

Access Types Legend

Table 2-396. TPCC0_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
26	TPTC_A1_READ_ACCESS_ERROR	RW	0h	Status of Error from MSS_TPTC_A1. Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK#br#Write 0x1 to clear this Error.
25	TPTC_A0_READ_ACCESS_ERROR	RW	0h	Status of Error from MSS_TPTC_A0. Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK. Write 0x1 to clear this Error.
24	TPCC_A_READ_ACCESS_ERROR	RW	0h	Status of Error from MSS_TPCC_A. Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK#. Write 0x1 to clear this Error.
	RESERVED	NONE		Reserved
18	TPTC_A1_WRITE_ACCESS_ERROR	RW	0h	Status of Error from MSS_TPTC_A1. Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK. Write 0x1 to clear this Error.
17	TPTC_A0_WRITE_ACCESS_ERROR	RW	0h	Status of Error from MSS_TPTC_A0. Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK. Write 0x1 to clear this Error.
16	TPCC_A_WRITE_ACCESS_ERROR	RW	0h	Status of Error from MSS_TPCC_A. Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK. Write 0x1 to clear this Error.
	RESERVED	NONE		Reserved
4	TPCC_A_PAR_ERR	RW	0h	Status of Error from MSS_TPCC_A. Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK. Write 0x1 to clear this Error.
3	TPTC_A1_ERR	RW	0h	Status of Error from MSS_TPTC_A1. Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK. Write 0x1 to clear this Error.
2	TPTC_A0_ERR	RW	0h	Status of Error from MSS_TPTC_A0. Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK. Write 0x1 to clear this Error.
1	TPCC_A_MPINT	RW	0h	Status of Error from MSS_TPCC_A. Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK. Write 0x1 to clear this Error.
0	TPCC_A_ERRINT	RW	0h	Status of Error from MSS_TPCC_A. Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK. Write 0x1 to clear this Error.

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2.3.149 MSS_CTRL_TPCC0_ERRAGG_STATUS_RAW Registers

2.3.149.1 MSS_TPCC0_ERRAGG_STATUS_RAW Register (Offset = 18008h) [reset = h]

Short Description: TPCC0_ERRAGG_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-397. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8008h

Access Types Legend

Table 2-398. TPCC0_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
26	TPTC_A1_READ_ACCESS_ERROR	RW	0h	Raw Status of Error from MSS_TPTC_A1. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK
25	TPTC_A0_READ_ACCESS_ERROR	RW	0h	Raw Status of Error from MSS_TPTC_A0. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK
24	TPCC_A_READ_ACCESS_ERROR	RW	0h	Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK
	RESERVED	NONE		Reserved
18	TPTC_A1_WRITE_ACCESS_ERROR	RW	0h	Raw Status of Error from MSS_TPTC_A1. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK
17	TPTC_A0_WRITE_ACCESS_ERROR	RW	0h	Raw Status of Error from MSS_TPTC_A0. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK
16	TPCC_A_WRITE_ACCESS_ERROR	RW	0h	Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK
	RESERVED	NONE		Reserved
4	TPCC_A_PAR_ERR	RW	0h	Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK
3	TPTC_A1_ERR	RW	0h	Raw Status of Error from MSS_TPTC_A1. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK
2	TPTC_A0_ERR	RW	0h	Raw Status of Error from MSS_TPTC_A0. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK
1	TPCC_A_MPINT	RW	0h	Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK
0	TPCC_A_ERRINT	RW	0h	Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK

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2.3.150 MSS_CTRL_MMR_ACCESS_ERRAGG_MASK0 Registers

2.3.150.1 MSS_MMR_ACCESS_ERRAGG_MASK0 Register (Offset = 18010h) [reset = h]

Short Description: MMR_ACCESS_ERRAGG_MASK0 register

Long Description:

Return to Summary Table

Table 2-399. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8010h

Access Types Legend

Table 2-400. MMR_ACCESS_ERRAGG_MASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11	HSM_CTRL_WR	RW	0h	Mask Interrupt from HSM_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
10	HSM_CTRL_RD	RW	0h	Mask Interrupt from HSM_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
9	HSM_SOC_CTRL_WR	RW	0h	Mask Interrupt from HSM_SOC_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
8	HSM_SOC_CTRL_RD	RW	0h	Mask Interrupt from HSM_SOC_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
7	TOP_RCM_WR	RW	0h	Mask Interrupt from TOP_RCM to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
6	TOP_RCM_RD	RW	0h	Mask Interrupt from TOP_RCM to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
5	TOP_CTRL_WR	RW	0h	Mask Interrupt from TOP_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
4	TOP_CTRL_RD	RW	0h	Mask Interrupt from TOP_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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Table 2-400. MMR_ACCESS_ERRAGG_MASK0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	MSS_RCM_WR	RW	0h	Mask Interrupt from MSS_RCM to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
2	MSS_RCM_RD	RW	0h	Mask Interrupt from MSS_RCM to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
1	MSS_CTRL_WR	RW	0h	Mask Interrupt from MSS_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG • 1: Error is Masked • 0: Error is Unmasked
0	MSS_CTRL_RD	RW	0h	Mask Interrupt from MSS_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG • 1: Error is Masked • 0: Error is Unmasked

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2.3.151 MSS_CTRL_MMR_ACCESS_ERRAGG_STATUS0 Registers

2.3.151.1 MSS_MMR_ACCESS_ERRAGG_STATUS0 Register (Offset = 18014h) [reset = h]

Short Description: MMR_ACCESS_ERRAGG_STATUS0 register

Long Description:

Return to Summary Table

Table 2-401. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8014h

Access Types Legend

Table 2-402. MMR_ACCESS_ERRAGG_STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11	HSM_CTRL_WR	RW	0h	Status of Interrupt from HSM_CTRLSet only if Interrupt is unmasked in MSS_PERIPH_ERRAGG_MASK0. Write 0x1 to clear this interrupt.
10	HSM_CTRL_RD	RW	0h	Status of Interrupt from HSM_CTRLSet only if Interrupt is unmasked in MSS_PERIPH_ERRAGG_MASK0. Write 0x1 to clear this interrupt.
9	HSM_SOC_CTRL_WR	RW	0h	Status of Interrupt from HSM_SOC_CTRLSet only if Interrupt is unmasked in MSS_PERIPH_ERRAGG_MASK0. Write 0x1 to clear this interrupt.
8	HSM_SOC_CTRL_RD	RW	0h	Status of Interrupt from HSM_SOC_CTRLSet only if Interrupt is unmasked in MSS_PERIPH_ERRAGG_MASK0. Write 0x1 to clear this interrupt.
7	TOP_RCM_WR	RW	0h	Status of Interrupt from TOP_RCMSet only if Interrupt is unmasked in MSS_PERIPH_ERRAGG_MASK0. Write 0x1 to clear this interrupt.
6	TOP_RCM_RD	RW	0h	Status of Interrupt from TOP_RCMSet only if Interrupt is unmasked in MSS_PERIPH_ERRAGG_MASK0. Write 0x1 to clear this interrupt.
5	TOP_CTRL_WR	RW	0h	Status of Interrupt from TOP_CTRLSet only if Interrupt is unmasked in MSS_PERIPH_ERRAGG_MASK0. Write 0x1 to clear this interrupt.
4	TOP_CTRL_RD	RW	0h	Status of Interrupt from TOP_CTRLSet only if Interrupt is unmasked in MSS_PERIPH_ERRAGG_MASK0. Write 0x1 to clear this interrupt.
3	MSS_RCM_WR	RW	0h	Status of Interrupt from MSS_RCMSet only if Interrupt is unmasked in MSS_PERIPH_ERRAGG_MASK0. Write 0x1 to clear this interrupt.
2	MSS_RCM_RD	RW	0h	Status of Interrupt from MSS_RCMSet only if Interrupt is unmasked in MSS_PERIPH_ERRAGG_MASK0. Write 0x1 to clear this interrupt.
1	MSS_CTRL_WR	RW	0h	Status of Interrupt from MSS_CTRLSet only if Interrupt is unmasked in MSS_PERIPH_ERRAGG_MASK0. Write 0x1 to clear this interrupt.
0	MSS_CTRL_RD	RW	0h	Status of Interrupt from MSS_CTRLSet only if Interrupt is unmasked in MSS_PERIPH_ERRAGG_MASK0. Write 0x1 to clear this interrupt.

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2.3.152 MSS_CTRL_MMR_ACCESS_ERRAGG_STATUS_RAW0 Registers

2.3.152.1 MSS_MMR_ACCESS_ERRAGG_STATUS_RAW0 Register (Offset = 18018h) [reset = h]

Short Description: MMR_ACCESS_ERRAGG_STATUS_RAW0 register

Long Description:

Return to Summary Table

Table 2-403. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8018h

Access Types Legend

Table 2-404. MMR_ACCESS_ERRAGG_STATUS_RAW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11	HSM_CTRL_WR	RW	0h	Raw Status of Interrupt from HSM_CTRL. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0
10	HSM_CTRL_RD	RW	0h	Raw Status of Interrupt from HSM_CTRL. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0
9	HSM_SOC_CTRL_WR	RW	0h	Raw Status of Interrupt from HSM_SOC_CTRL. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0
8	HSM_SOC_CTRL_RD	RW	0h	Raw Status of Interrupt from HSM_SOC_CTRL. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0
7	TOP_RCM_WR	RW	0h	Raw Status of Interrupt from TOP_RCM. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0
6	TOP_RCM_RD	RW	0h	Raw Status of Interrupt from TOP_RCM. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0
5	TOP_CTRL_WR	RW	0h	Raw Status of Interrupt from TOP_CTRL. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0
4	TOP_CTRL_RD	RW	0h	Raw Status of Interrupt from TOP_CTRL. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0
3	MSS_RCM_WR	RW	0h	Raw Status of Interrupt from MSS_RCM. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0
2	MSS_RCM_RD	RW	0h	Raw Status of Interrupt from MSS_RCM. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0
1	MSS_CTRL_WR	RW	0h	Raw Status of Interrupt from MSS_CTRL. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0
0	MSS_CTRL_RD	RW	0h	Raw Status of Interrupt from MSS_CTRL. Set irrespective if the Interupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0

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2.3.153 MSS_CTRL_R5SS0_CPU0_ECC_CORR_ERRAGG_MASK Registers

2.3.153.1 MSS_R5SS0_CPU0_ECC_CORR_ERRAGG_MASK Register (Offset = 18080h) [reset = h]

Short Description: R5SS0_CPU0_ECC_CORR_ERRAGG_MASK register

Long Description:

Return to Summary Table

Table 2-405. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8080h

Access Types Legend

Table 2-406. R5SS0_CPU0_ECC_CORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	R5SS0_CPU0_IDATA_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
5	R5SS0_CPU0_ITAG_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
4	R5SS0_CPU0_DDATA_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
3	R5SS0_CPU0_DTAG_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
2	R5SS0_CPU0_B0TCM_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
1	R5SS0_CPU0_B1TCM_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
0	R5SS0_CPU0_ATCM_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked

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2.3.154 MSS_CTRL_R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS Registers

2.3.154.1 MSS_R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS Register (Offset = 18084h) [reset = h]

Short Description: R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS register

Long Description:

Return to Summary Table

Table 2-407. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8084h

Access Types Legend

Table 2-408. R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	R5SS0_CPU0_IDATA_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
5	R5SS0_CPU0_ITAG_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
4	R5SS0_CPU0_DDATA_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
3	R5SS0_CPU0_DTAG_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
2	R5SS0_CPU0_B0TCM_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS0_CPU0_B1TCM_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS0_CPU0_ATCM_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.155 MSS_CTRL_R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW Registers

2.3.155.1 MSS_R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW Register (Offset = 18088h) [reset = h]

Short Description: R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-409. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8088h

Access Types Legend

Table 2-410. R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	R5SS0_CPU0_IDATA_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
5	R5SS0_CPU0_ITAG_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
4	R5SS0_CPU0_DDATA_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
3	R5SS0_CPU0_DTAG_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
2	R5SS0_CPU0_B0TCM_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS0_CPU0_B1TCM_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS0_CPU0_ATCM_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.156 MSS_CTRL_R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK Registers

2.3.156.1 MSS_R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK Register (Offset = 18090h) [reset = h]

Short Description: R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK register

Long Description:

Return to Summary Table

Table 2-411. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8090h

Access Types Legend

Table 2-412. R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4	R5SS0_CPU0_DDATA_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
3	R5SS0_CPU0_DTAG_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
2	R5SS0_CPU0_B0TCM_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
1	R5SS0_CPU0_B1TCM_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
0	R5SS0_CPU0_ATCM_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked

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2.3.157 MSS_CTRL_R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS Registers

2.3.157.1 MSS_R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS Register (Offset = 18094h) [reset = h]

Short Description: R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS register

Long Description:

Return to Summary Table

Table 2-413. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8094h

Access Types Legend

Table 2-414. R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4	R5SS0_CPU0_DDATA_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
3	R5SS0_CPU0_DTAG_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
2	R5SS0_CPU0_B0TCM_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS0_CPU0_B1TCM_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS0_CPU0_ATCM_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.158 MSS_CTRL_R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW Registers

2.3.158.1 MSS_R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW Register (Offset = 18098h) [reset = h]

Short Description: R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-415. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8098h

Access Types Legend

Table 2-416. R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4	R5SS0_CPU0_DDATA_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
3	R5SS0_CPU0_DTAG_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
2	R5SS0_CPU0_B0TCM_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS0_CPU0_B1TCM_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS0_CPU0_ATCM_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.159 MSS_CTRL_R5SS0_CPU1_ECC_CORR_ERRAGG_MASK Registers

2.3.159.1 MSS_R5SS0_CPU1_ECC_CORR_ERRAGG_MASK Register (Offset = 180A0h) [reset = h]

Short Description: R5SS0_CPU1_ECC_CORR_ERRAGG_MASK register

Long Description:

Return to Summary Table

Table 2-417. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80A0h

Access Types Legend

Table 2-418. R5SS0_CPU1_ECC_CORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	R5SS0_CPU1_IDATA_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
5	R5SS0_CPU1_ITAG_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
4	R5SS0_CPU1_DDATA_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
3	R5SS0_CPU1_DTAG_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
2	R5SS0_CPU1_B0TCM_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
1	R5SS0_CPU1_B1TCM_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
0	R5SS0_CPU1_ATCM_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked

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2.3.160 MSS_CTRL_R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS Registers

2.3.160.1 MSS_R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS Register (Offset = 180A4h) [reset = h]

Short Description: R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS register

Long Description:

Return to Summary Table

Table 2-419. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80A4h

Access Types Legend

Table 2-420. R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	R5SS0_CPU1_IDATA_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
5	R5SS0_CPU1_ITAG_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
4	R5SS0_CPU1_DDATA_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
3	R5SS0_CPU1_DTAG_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
2	R5SS0_CPU1_B0TCM_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS0_CPU1_B1TCM_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS0_CPU1_ATCM_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.161 MSS_CTRL_R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW Registers

2.3.161.1 MSS_R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW Register (Offset = 180A8h) [reset = h]

Short Description: R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-421. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80A8h

Access Types Legend

Table 2-422. R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	R5SS0_CPU1_IDATA_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
5	R5SS0_CPU1_ITAG_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU#br#Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
4	R5SS0_CPU1_DDATA_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU#br#Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
3	R5SS0_CPU1_DTAG_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
2	R5SS0_CPU1_B0TCM_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS0_CPU1_B1TCM_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS0_CPU1_ATCM_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.162 MSS_CTRL_R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK Registers

2.3.162.1 MSS_R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK Register (Offset = 180B0h) [reset = h]

Short Description: R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK register

Long Description:

Return to Summary Table

Table 2-423. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80B0h

Access Types Legend

Table 2-424. R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4	R5SS0_CPU1_DDATA_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
3	R5SS0_CPU1_DTAG_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
2	R5SS0_CPU1_B0TCM_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
1	R5SS0_CPU1_B1TCM_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
0	R5SS0_CPU1_ATCM_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked

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2.3.163 MSS_CTRL_R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS Registers

2.3.163.1 MSS_R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS Register (Offset = 180B4h) [reset = h]

Short Description: R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS register

Long Description:

Return to Summary Table

Table 2-425. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80B4h

Access Types Legend

Table 2-426. R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4	R5SS0_CPU1_DDATA_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
3	R5SS0_CPU1_DTAG_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
2	R5SS0_CPU1_B0TCM_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS0_CPU1_B1TCM_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS0_CPU1_ATCM_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.164 MSS_CTRL_R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW Registers

2.3.164.1 MSS_R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW Register (Offset = 180B8h) [reset = h]

Short Description: R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-427. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80B8h

Access Types Legend

Table 2-428. R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4	R5SS0_CPU1_DDATA_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
3	R5SS0_CPU1_DTAG_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
2	R5SS0_CPU1_B0TCM_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS0_CPU1_B1TCM_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS0_CPU1_ATCM_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.165 MSS_CTRL_R5SS1_CPU0_ECC_CORR_ERRAGG_MASK Registers

2.3.165.1 MSS_R5SS1_CPU0_ECC_CORR_ERRAGG_MASK Register (Offset = 180C0h) [reset = h]

Short Description: R5SS1_CPU0_ECC_CORR_ERRAGG_MASK register

Long Description:

Return to Summary Table

Table 2-429. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80C0h

Access Types Legend

Table 2-430. R5SS1_CPU0_ECC_CORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	R5SS1_CPU0_IDATA_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
5	R5SS1_CPU0_ITAG_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
4	R5SS1_CPU0_DDATA_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
3	R5SS1_CPU0_DTAG_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
2	R5SS1_CPU0_B0TCM_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
1	R5SS1_CPU0_B1TCM_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
0	R5SS1_CPU0_ATCM_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked

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2.3.166 MSS_CTRL_R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS Registers

2.3.166.1 MSS_R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS Register (Offset = 180C4h) [reset = h]

Short Description: R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS register

Long Description:

Return to Summary Table

Table 2-431. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80C4h

Access Types Legend

Table 2-432. R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	R5SS1_CPU0_IDATA_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
5	R5SS1_CPU0_ITAG_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
4	R5SS1_CPU0_DDATA_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
3	R5SS1_CPU0_DTAG_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
2	R5SS1_CPU0_B0TCM_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU#br#Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS1_CPU0_B1TCM_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS1_CPU0_ATCM_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.167 MSS_CTRL_R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW Registers

2.3.167.1 MSS_R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW Register (Offset = 180C8h) [reset = h]

Short Description: R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-433. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80C8h

Access Types Legend

Table 2-434. R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	R5SS1_CPU0_IDATA_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
5	R5SS1_CPU0_ITAG_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
4	R5SS1_CPU0_DDATA_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
3	R5SS1_CPU0_DTAG_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
2	R5SS1_CPU0_B0TCM_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS1_CPU0_B1TCM_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS1_CPU0_ATCM_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.168 MSS_CTRL_R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK Registers

2.3.168.1 MSS_R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK Register (Offset = 180D0h) [reset = h]

Short Description: R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK register

Long Description:

Return to Summary Table

Table 2-435. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80D0h

Access Types Legend

Table 2-436. R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4	R5SS1_CPU0_DDATA_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
3	R5SS1_CPU0_DTAG_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
2	R5SS1_CPU0_B0TCM_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
1	R5SS1_CPU0_B1TCM_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
0	R5SS1_CPU0_ATCM_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked

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2.3.169 MSS_CTRL_R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS Registers

2.3.169.1 MSS_R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS Register (Offset = 180D4h) [reset = h]

Short Description: R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS register

Long Description:

Return to Summary Table

Table 2-437. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80D4h

Access Types Legend

Table 2-438. R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4	R5SS1_CPU0_DDATA_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
3	R5SS1_CPU0_DTAG_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
2	R5SS1_CPU0_B0TCM_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS1_CPU0_B1TCM_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS1_CPU0_ATCM_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.170 MSS_CTRL_R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW Registers

2.3.170.1 MSS_R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW Register (Offset = 180D8h) [reset = h]

Short Description: R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-439. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80D8h

Access Types Legend

Table 2-440. R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4	R5SS1_CPU0_DDATA_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
3	R5SS1_CPU0_DTAG_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
2	R5SS1_CPU0_B0TCM_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS1_CPU0_B1TCM_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS1_CPU0_ATCM_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.171 MSS_CTRL_R5SS1_CPU1_ECC_CORR_ERRAGG_MASK Registers

2.3.171.1 MSS_R5SS1_CPU1_ECC_CORR_ERRAGG_MASK Register (Offset = 180E0h) [reset = h]

Short Description: R5SS1_CPU1_ECC_CORR_ERRAGG_MASK register

Long Description:

Return to Summary Table

Table 2-441. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80E0h

Access Types Legend

Table 2-442. R5SS1_CPU1_ECC_CORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	R5SS1_CPU1_IDATA_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
5	R5SS1_CPU1_ITAG_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
4	R5SS1_CPU1_DDATA_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
3	R5SS1_CPU1_DTAG_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
2	R5SS1_CPU1_B0TCM_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
1	R5SS1_CPU1_B1TCM_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
0	R5SS1_CPU1_ATCM_CORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked

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2.3.172 MSS_CTRL_R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS Registers

2.3.172.1 MSS_R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS Register (Offset = 180E4h) [reset = h]

Short Description: R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS register

Long Description:

Return to Summary Table

Table 2-443. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80E4h

Access Types Legend

Table 2-444. R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	R5SS1_CPU1_IDATA_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
5	R5SS1_CPU1_ITAG_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
4	R5SS1_CPU1_DDATA_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
3	R5SS1_CPU1_DTAG_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
2	R5SS1_CPU1_B0TCM_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS1_CPU1_B1TCM_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS1_CPU1_ATCM_CORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.173 MSS_CTRL_R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW Registers

2.3.173.1 MSS_R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW Register (Offset = 180E8h) [reset = h]

Short Description: R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-445. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80E8h

Access Types Legend

Table 2-446. R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	R5SS1_CPU1_IDATA_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
5	R5SS1_CPU1_ITAG_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
4	R5SS1_CPU1_DDATA_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
3	R5SS1_CPU1_DTAG_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
2	R5SS1_CPU1_B0TCM_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS1_CPU1_B1TCM_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS1_CPU1_ATCM_CORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.174 MSS_CTRL_R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK Registers

2.3.174.1 MSS_R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK Register (Offset = 180F0h) [reset = h]

Short Description: R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK register

Long Description:

Return to Summary Table

Table 2-447. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80F0h

Access Types Legend

Table 2-448. R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4	R5SS1_CPU1_DDATA_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
3	R5SS1_CPU1_DTAG_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
2	R5SS1_CPU1_B0TCM_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
1	R5SS1_CPU1_B1TCM_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
0	R5SS1_CPU1_ATCM_UNCORR_ERR	RW	0h	Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked

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2.3.175 MSS_CTRL_R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS Registers

2.3.175.1 MSS_R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS Register (Offset = 180F4h) [reset = h]

Short Description: R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS register

Long Description:

Return to Summary Table

Table 2-449. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80F4h

Access Types Legend

Table 2-450. R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4	R5SS1_CPU1_DDATA_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
3	R5SS1_CPU1_DTAG_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
2	R5SS1_CPU1_B0TCM_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS1_CPU1_B1TCM_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS1_CPU1_ATCM_UNCORR_ERR	RW	0h	Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.176 MSS_CTRL_R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW Registers

2.3.176.1 MSS_R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW Register (Offset = 180F8h) [reset = h]

Short Description: R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-451. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 80F8h

Access Types Legend

Table 2-452. R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4	R5SS1_CPU1_DDATA_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
3	R5SS1_CPU1_DTAG_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
2	R5SS1_CPU1_B0TCM_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS1_CPU1_B1TCM_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS1_CPU1_ATCM_UNCORR_ERR	RW	0h	Raw Status of Interrupt from correctable error of corresponding CPU. Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.177 MSS_CTRL_R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK Registers

2.3.177.1 MSS_R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK Register (Offset = 18100h) [reset = h]

Short Description: R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK register

Long Description:

Return to Summary Table

Table 2-453. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8100h

Access Types Legend

Table 2-454. R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2	R5SS0_CPU0_B1TCM0_PARITY_ERR	RW	0h	Mask Interrupt for address parity errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
1	R5SS0_CPU0_B0TCM0_PARITY_ERR	RW	0h	Mask Interrupt for address parity errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
0	R5SS0_CPU0_ATCM0_PARITY_ERR	RW	0h	Mask Interrupt for address parity errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked

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2.3.178 MSS_CTRL_R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS Registers

2.3.178.1 MSS_R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS Register (Offset = 18104h) [reset = h]

Short Description: R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS register

Long Description:

Return to Summary Table

Table 2-455. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8104h

Access Types Legend

Table 2-456. R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2	R5SS0_CPU0_B1TCM0_PARITY_ERR	RW	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS0_CPU0_B0TCM0_PARITY_ERR	RW	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS0_CPU0_ATCM0_PARITY_ERR	RW	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.179 MSS_CTRL_R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Registers

2.3.179.1 MSS_R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register (Offset = 18108h) [reset = h]

Short Description: R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-457. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8108h

Access Types Legend

Table 2-458. R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2	R5SS0_CPU0_B1TCM0_PARITY_ERR	RW	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS0_CPU0_B0TCM0_PARITY_ERR	RW	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS0_CPU0_ATCM0_PARITY_ERR	RW	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.180 MSS_CTRL_R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK Registers

2.3.180.1 MSS_R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK Register (Offset = 18110h) [reset = h]

Short Description: R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK register

Long Description:

Return to Summary Table

Table 2-459. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8110h

Access Types Legend

Table 2-460. R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2	R5SS0_CPU1_B1TCM1_PARITY_ERR	RW	0h	Mask Interrupt for address parity errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
1	R5SS0_CPU1_B1TCM0_PARITY_ERR	RW	0h	Mask Interrupt for address parity errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
0	R5SS0_CPU1_ATCM1_PARITY_ERR	RW	0h	Mask Interrupt for address parity errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked

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2.3.181 MSS_CTRL_R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS Registers

2.3.181.1 MSS_R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS Register (Offset = 18114h) [reset = h]

Short Description: R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS register

Long Description:

Return to Summary Table

Table 2-461. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8114h

Access Types Legend

Table 2-462. R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2	R5SS0_CPU1_B1TCM1_PARITY_ERR	RW	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS0_CPU1_B0TCM1_PARITY_ERR	RW	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS0_CPU1_ATCM1_PARITY_ERR	RW	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.182 MSS_CTRL_R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Registers

2.3.182.1 MSS_R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register (Offset = 18118h) [reset = h]

Short Description: R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-463. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8118h

Access Types Legend

Table 2-464. R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2	R5SS0_CPU1_B1TCM1_PARITY_ERR	RW	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS0_CPU1_B0TCM1_PARITY_ERR	RW	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS0_CPU1_ATCM1_PARITY_ERR	RW	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.183 MSS_CTRL_R5SS0_TCM_ADDRPARITY_CLR Registers

2.3.183.1 MSS_R5SS0_TCM_ADDRPARITY_CLR Register (Offset = 18120h) [reset = h]

Short Description: R5SS0_TCM_ADDRPARITY_CLR register

Long Description:

Return to Summary Table

Table 2-465. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8120h

Access Types Legend

Table 2-466. R5SS0_TCM_ADDRPARITY_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 20	B1TCM1_ERRADDR_CLR	RW	0h	Write pulse bit field : Writing 3'b111 clears the Address latched after parity error for B1TCM of CR5B
	RESERVED	NONE		Reserved
18 - 16	B1TCM0_ERRADDR_CLR	RW	0h	Write pulse bit field : Writing 3'b111 clears the Address latched after parity error for B1TCM of CR5A
	RESERVED	NONE		Reserved
14 - 12	B0CM1_ERRADDR_CLR	RW	0h	Write pulse bit field : Writing 3'b111 clears the Address latched after parity error for B0TCM of CR5B
	RESERVED	NONE		Reserved
10 - 8	B0TCM0_ERRADDR_CLR	RW	0h	Write pulse bit field : Writing 3'b111 clears the Address latched after parity error for B0TCM of CR5A
	RESERVED	NONE		Reserved
6 - 4	ATCM1_ERRADDR_CLR	RW	0h	Write pulse bit field : Writing 3'b111 clears the Address latched after parity error for ATCM of CR5B
	RESERVED	NONE		Reserved
2 - 0	ATCM0_ERRADDR_CLR	RW	0h	Pulse bit-field Writing 3'b111 clears the Address latched after parity error for ATCM of CR5A

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2.3.184 MSS_CTRL_R5SS0_CORE0_ADDRPARITY_ERR_ATCM Registers

2.3.184.1 MSS_R5SS0_CORE0_ADDRPARITY_ERR_ATCM Register (Offset = 18124h) [reset = h]

Short Description: R5SS0_CORE0_ADDRPARITY_ERR_ATCM register

Long Description:

Return to Summary Table

Table 2-467. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8124h

Access Types Legend

Table 2-468. R5SS0_CORE0_ADDRPARITY_ERR_ATCM Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	ADDR	RO	0h	Address latched when parity error is occurred for ATCM of CR5A

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2.3.185 MSS_CTRL_R5SS0_CORE1_ADDRPARITY_ERR_ATCM Registers

2.3.185.1 MSS_R5SS0_CORE1_ADDRPARITY_ERR_ATCM Register (Offset = 18128h) [reset = h]

Short Description: R5SS0_CORE1_ADDRPARITY_ERR_ATCM register

Long Description:

Return to Summary Table

Table 2-469. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8128h

Access Types Legend

Table 2-470. R5SS0_CORE1_ADDRPARITY_ERR_ATCM Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	ADDR	RO	0h	Address latched when parity error is occurred for ATCM of CR5B

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2.3.186 MSS_CTRL_R5SS0_CORE0_ERR_ADDRPARITY_B0TCM Registers

2.3.186.1 MSS_R5SS0_CORE0_ERR_ADDRPARITY_B0TCM Register (Offset = 1812Ch) [reset = h]

Short Description: R5SS0_CORE0_ERR_ADDRPARITY_B0TCM register

Long Description:

Return to Summary Table

Table 2-471. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 812Ch

Access Types Legend

Table 2-472. R5SS0_CORE0_ERR_ADDRPARITY_B0TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	ADDR	RO	0h	Address latched when parity error is occurred for B0TCM of CR5A

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2.3.187 MSS_CTRL_R5SS0_CORE1_ERR_ADDRPARITY_B0TCM Registers

2.3.187.1 MSS_R5SS0_CORE1_ERR_ADDRPARITY_B0TCM Register (Offset = 18130h) [reset = h]

Short Description: R5SS0_CORE1_ERR_ADDRPARITY_B0TCM register

Long Description:

Return to Summary Table

Table 2-473. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8130h

Access Types Legend

Table 2-474. R5SS0_CORE1_ERR_ADDRPARITY_B0TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	ADDR	RO	0h	Address latched when parity error is occurred for B0TCM of CR5B

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2.3.188 MSS_CTRL_R5SS0_CORE0_ERR_ADDRPARITY_B1TCM Registers

2.3.188.1 MSS_R5SS0_CORE0_ERR_ADDRPARITY_B1TCM Register (Offset = 18134h) [reset = h]

Short Description: R5SS0_CORE0_ERR_ADDRPARITY_B1TCM register

Long Description:

Return to Summary Table

Table 2-475. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8134h

Access Types Legend

Table 2-476. R5SS0_CORE0_ERR_ADDRPARITY_B1TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	ADDR	RO	0h	Address latched when parity error is occurred for B1TCM of CR5A

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2.3.189 MSS_CTRL_R5SS0_CORE1_ERR_ADDRPARITY_B1TCM Registers

2.3.189.1 MSS_R5SS0_CORE1_ERR_ADDRPARITY_B1TCM Register (Offset = 18138h) [reset = h]

Short Description: R5SS0_CORE1_ERR_ADDRPARITY_B1TCM register

Long Description:

Return to Summary Table

Table 2-477. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8138h

Access Types Legend

Table 2-478. R5SS0_CORE1_ERR_ADDRPARITY_B1TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	ADDR	RO	0h	Address latched when parity error is occurred for B1TCM of CR5B

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2.3.190 MSS_CTRL_R5SS0_TCM_ADDRPARITY_ERRFORCE Registers

2.3.190.1 MSS_R5SS0_TCM_ADDRPARITY_ERRFORCE Register (Offset = 1813Ch) [reset = h]

Short Description: R5SS0_TCM_ADDRPARITY_ERRFORCE register

Long Description:

Return to Summary Table

Table 2-479. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 813Ch

Access Types Legend

Table 2-480. R5SS0_TCM_ADDRPARITY_ERRFORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 20	B1TCM1	RW	0h	Write pulse bit field : Writing 3'b111 forces a parity error for B1TCM of CR5B
	RESERVED	NONE		Reserved
18 - 16	B1TCM0	RW	0h	Write pulse bit field : Writing 3'b111 forces a parity error for B1TCM of CR5A
	RESERVED	NONE		Reserved
14 - 12	B0TCM1	RW	0h	Write pulse bit field : Writing 3'b111 forces a parity error for B0TCM of CR5B
	RESERVED	NONE		Reserved
10 - 8	B0TCM0	RW	0h	Write pulse bit field : Writing 3'b111 forces a parity error for B0TCM of CR5A
	RESERVED	NONE		Reserved
6 - 4	ATCM1	RW	0h	Write pulse bit field : Writing 3'b111 forces a parity error for ATCM of CR5B
	RESERVED	NONE		Reserved
2 - 0	ATCM0	RW	0h	Write pulse bit field : Writing 3'b111 forces a parity error for ATCM of CR5A

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2.3.191 MSS_CTRL_R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK Registers

2.3.191.1 MSS_R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK Register (Offset = 18140h) [reset = h]

Short Description: R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK register

Long Description:

Return to Summary Table

Table 2-481. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8140h

Access Types Legend

Table 2-482. R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2	R5SS1_CPU0_B1TCM0_PARITY_ERR	RW	0h	Mask Interrupt for address parity errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
1	R5SS1_CPU0_B0TCM0_PARITY_ERR	RW	0h	Mask Interrupt for address parity errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
0	R5SS1_CPU0_ATCM0_PARITY_ERR	RW	0h	Mask Interrupt for address parity errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked

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2.3.192 MSS_CTRL_R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS Registers

2.3.192.1 MSS_R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS Register (Offset = 18144h) [reset = h]

Short Description: R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS register

Long Description:

Return to Summary Table

Table 2-483. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8144h

Access Types Legend

Table 2-484. R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2	R5SS1_CPU0_B1TCM0_PARITY_ERR	RW	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS1_CPU0_B0TCM0_PARITY_ERR	RW	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS1_CPU0_ATCM0_PARITY_ERR	RW	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.193 MSS_CTRL_R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Registers

2.3.193.1 MSS_R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register (Offset = 18148h) [reset = h]

Short Description: R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-485. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8148h

Access Types Legend

Table 2-486. R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2	R5SS1_CPU0_B1TCM0_PARITY_ERR	RW	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS1_CPU0_B0TCM0_PARITY_ERR	RW	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS1_CPU0_ATCM0_PARITY_ERR	RW	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.194 MSS_CTRL_R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK Registers

2.3.194.1 MSS_R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK Register (Offset = 18150h) [reset = h]

Short Description: R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK register

Long Description:

Return to Summary Table

Table 2-487. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8150h

Access Types Legend

Table 2-488. R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2	R5SS1_CPU1_B1TCM1_PARITY_ERR	RW	0h	Mask Interrupt for address parity errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
1	R5SS1_CPU1_B0TCM1_PARITY_ERR	RW	0h	Mask Interrupt for address parity errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked
0	R5SS1_CPU1_ATCM1_PARITY_ERR	RW	0h	Mask Interrupt for address parity errors to aggregated Interrupt of corresponding CPU • 1: Error is Masked • 0: Error is Unmasked

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2.3.195 MSS_CTRL_R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS Registers

2.3.195.1 MSS_R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS Register (Offset = 18154h) [reset = h]

Short Description: R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS register

Long Description:

Return to Summary Table

Table 2-489. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8154h

Access Types Legend

Table 2-490. R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2	R5SS1_CPU1_B1TCM1_PARITY_ERR	RW	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS1_CPU1_B0TCM1_PARITY_ERR	RW	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS1_CPU1_ATCM1_PARITY_ERR	RW	0h	Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.196 MSS_CTRL_R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Registers

2.3.196.1 MSS_R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register (Offset = 18158h) [reset = h]

Short Description: R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW register

Long Description:

Return to Summary Table

Table 2-491. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8158h

Access Types Legend

Table 2-492. R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2	R5SS1_CPU1_B1TCM1_PARITY_ERR	RW	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
1	R5SS1_CPU1_B0TCM1_PARITY_ERR	RW	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.
0	R5SS1_CPU1_ATCM1_PARITY_ERR	RW	0h	Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register. Write 0x1 to clear this interrupt.

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2.3.197 MSS_CTRL_R5SS1_TCM_ADDRPARITY_CLR Registers

2.3.197.1 MSS_R5SS1_TCM_ADDRPARITY_CLR Register (Offset = 18160h) [reset = h]

Short Description: R5SS1_TCM_ADDRPARITY_CLR register

Long Description:

Return to Summary Table

Table 2-493. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8160h

Access Types Legend

Table 2-494. R5SS1_TCM_ADDRPARITY_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 20	B1TCM1_ERRADDR_CLR	RW	0h	Write pulse bit field : Writing 3'b111 clears the Address latched after parity error for B1TCM of CR5B
	RESERVED	NONE		Reserved
18 - 16	B1TCM0_ERRADDR_CLR	RW	0h	Write pulse bit field : Writing 3'b111 clears the Address latched after parity error for B1TCM of CR5A
	RESERVED	NONE		Reserved
14 - 12	B0CM1_ERRADDR_CLR	RW	0h	Write pulse bit field : Writing 3'b111 clears the Address latched after parity error for B0TCM of CR5B
	RESERVED	NONE		Reserved
10 - 8	B0TCM0_ERRADDR_CLR	RW	0h	Write pulse bit field : Writing 3'b111 clears the Address latched after parity error for B0TCM of CR5A
	RESERVED	NONE		Reserved
6 - 4	ATCM1_ERRADDR_CLR	RW	0h	Write pulse bit field : Writing 3'b111 clears the Address latched after parity error for ATCM of CR5B
	RESERVED	NONE		Reserved
2 - 0	ATCM0_ERRADDR_CLR	RW	0h	Pulse bit-field Writing 3'b111 clears the Address latched after parity error for ATCM of CR5A

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2.3.198 MSS_CTRL_R5SS1_CORE0_ADDRPARITY_ERR_ATCM Registers

2.3.198.1 MSS_R5SS1_CORE0_ADDRPARITY_ERR_ATCM Register (Offset = 18164h) [reset = h]

Short Description: R5SS1_CORE0_ADDRPARITY_ERR_ATCM register

Long Description:

Return to Summary Table

Table 2-495. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8164h

Access Types Legend

Table 2-496. R5SS1_CORE0_ADDRPARITY_ERR_ATCM Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	ADDR	RO	0h	Address latched when parity error is occurred for ATCM of CR5A

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2.3.199 MSS_CTRL_R5SS1_CORE1_ADDRPARITY_ERR_ATCM Registers

2.3.199.1 MSS_R5SS1_CORE1_ADDRPARITY_ERR_ATCM Register (Offset = 18168h) [reset = h]

Short Description: R5SS1_CORE1_ADDRPARITY_ERR_ATCM register

Long Description:

Return to Summary Table

Table 2-497. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8168h

Access Types Legend

Table 2-498. R5SS1_CORE1_ADDRPARITY_ERR_ATCM Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	ADDR	RO	0h	Address latched when parity error is occurred for ATCM of CR5B

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2.3.200 MSS_CTRL_R5SS1_CORE0_ERR_ADDRPARITY_B0TCM Registers

2.3.200.1 MSS_R5SS1_CORE0_ERR_ADDRPARITY_B0TCM Register (Offset = 1816Ch) [reset = h]

Short Description: R5SS1_CORE0_ERR_ADDRPARITY_B0TCM register

Long Description:

Return to Summary Table

Table 2-499. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 816Ch

Access Types Legend

Table 2-500. R5SS1_CORE0_ERR_ADDRPARITY_B0TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	ADDR	RO	0h	Address latched when parity error is occurred for B0TCM of CR5A

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2.3.201 MSS_CTRL_R5SS1_CORE1_ERR_ADDRPARITY_B0TCM Registers

2.3.201.1 MSS_R5SS1_CORE1_ERR_ADDRPARITY_B0TCM Register (Offset = 18170h) [reset = h]

Short Description: R5SS1_CORE1_ERR_ADDRPARITY_B0TCM register

Long Description:

Return to Summary Table

Table 2-501. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8170h

Access Types Legend

Table 2-502. R5SS1_CORE1_ERR_ADDRPARITY_B0TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	ADDR	RO	0h	Address latched when parity error is occurred for B0TCM of CR5B

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2.3.202 MSS_CTRL_R5SS1_CORE0_ERR_ADDRPARITY_B1TCM Registers

2.3.202.1 MSS_R5SS1_CORE0_ERR_ADDRPARITY_B1TCM Register (Offset = 18174h) [reset = h]

Short Description: R5SS1_CORE0_ERR_ADDRPARITY_B1TCM register

Long Description:

Return to Summary Table

Table 2-503. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8174h

Access Types Legend

Table 2-504. R5SS1_CORE0_ERR_ADDRPARITY_B1TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	ADDR	RO	0h	Address latched when parity error is occurred for B1TCM of CR5A

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2.3.203 MSS_CTRL_R5SS1_CORE1_ERR_ADDRPARITY_B1TCM Registers

2.3.203.1 MSS_R5SS1_CORE1_ERR_ADDRPARITY_B1TCM Register (Offset = 18178h) [reset = h]

Short Description: R5SS1_CORE1_ERR_ADDRPARITY_B1TCM register

Long Description:

Return to Summary Table

Table 2-505. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8178h

Access Types Legend

Table 2-506. R5SS1_CORE1_ERR_ADDRPARITY_B1TCM Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	ADDR	RO	0h	Address latched when parity error is occurred for B1TCM of CR5B

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2.3.204 MSS_CTRL_R5SS1_TCM_ADDRPARITY_ERRFORCE Registers

2.3.204.1 MSS_R5SS1_TCM_ADDRPARITY_ERRFORCE Register (Offset = 1817Ch) [reset = h]

Short Description: R5SS1_TCM_ADDRPARITY_ERRFORCE register

Long Description:

Return to Summary Table

Table 2-507. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 817Ch

Access Types Legend

Table 2-508. R5SS1_TCM_ADDRPARITY_ERRFORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 20	B1TCM1	RW	0h	Write pulse bit field : Writing 3'b111 forces a parity error for B1TCM of CR5B
	RESERVED	NONE		Reserved
18 - 16	B1TCM0	RW	0h	Write pulse bit field : Writing 3'b111 forces a parity error for B1TCM of CR5A
	RESERVED	NONE		Reserved
14 - 12	B0TCM1	RW	0h	Write pulse bit field : Writing 3'b111 forces a parity error for B0TCM of CR5B
	RESERVED	NONE		Reserved
10 - 8	B0TCM0	RW	0h	Write pulse bit field : Writing 3'b111 forces a parity error for B0TCM of CR5A
	RESERVED	NONE		Reserved
6 - 4	ATCM1	RW	0h	Write pulse bit field : Writing 3'b111 forces a parity error for ATCM of CR5B
	RESERVED	NONE		Reserved
2 - 0	ATCM0	RW	0h	Write pulse bit field : Writing 3'b111 forces a parity error for ATCM of CR5A

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2.3.205 MSS_CTRL_TPCC0_PARITY_CTRL Registers

2.3.205.1 MSS_TPCC0_PARITY_CTRL Register (Offset = 18180h) [reset = h]

Short Description: TPCC0_PARITY_CTRL register

Long Description:

Return to Summary Table

Table 2-509. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8180h

Access Types Legend

Table 2-510. TPCC0_PARITY_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
16	TPCC_A_PARITY_ERR_CLR	RW	0h	Write pulse bit field: Parity clear bit. Writing 1'b1 will clear the tpcc_a_parity_addr
	RESERVED	NONE		Reserved
4	TPCC_A_PARITY_TESTEN	RW	0h	Parity Test Enable for TPCC_A. Writing 1'b1 enables parity test for TPCC_A
	RESERVED	NONE		Reserved
0	TPCC_A_PARITY_EN	RW	0h	Parity Enable for TPCC_A. Writing 1'b1 enables parity for TPCC_A

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2.3.206 MSS_CTRL_TPCC0_PARITY_STATUS Registers

2.3.206.1 MSS_TPCC0_PARITY_STATUS Register (Offset = 18184h) [reset = h]

Short Description: TPCC0_PARITY_STATUS register

Long Description:

Return to Summary Table

Table 2-511. Instance Table

Instance Name	Physical Address
MSS_CTRL	50D1 8184h

Access Types Legend

Table 2-512. TPCC0_PARITY_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
8 - 0	TPCC_A_PARITY_ADDR	RO	0h	TPCC_A Parity Error Address Location

2.3.207 Access Table

Table 2-513. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
WO	WO	Write

2.4 MSS_IOMUX Registers

Table 2-514. MSS_IOMUX Registers Base Address Table

Offset	Length	Acronym	Register Name	MSS_IOMUX Physical Address
0h	32	MSS_IOMUX_QSPI0_CSN0_CFG_REG	RW	5310 0000h
4h	32	MSS_IOMUX_QSPI0_CSN1_CFG_REG	RW	5310 0004h
8h	32	MSS_IOMUX_QSPI0_CLK_CFG_REG	RW	5310 0008h
Ch	32	MSS_IOMUX_QSPI0_D0_CFG_REG	RW	5310 000Ch
10h	32	MSS_IOMUX_QSPI0_D1_CFG_REG	RW	5310 0010h
14h	32	MSS_IOMUX_QSPI0_D2_CFG_REG	RW	5310 0014h
18h	32	MSS_IOMUX_QSPI0_D3_CFG_REG	RW	5310 0018h
1Ch	32	MSS_IOMUX_MCAN0_RX_CFG_REG	RW	5310 001Ch
20h	32	MSS_IOMUX_MCAN0_TX_CFG_REG	RW	5310 0020h
24h	32	MSS_IOMUX_MCAN1_RX_CFG_REG	RW	5310 0024h
28h	32	MSS_IOMUX_MCAN1_TX_CFG_REG	RW	5310 0028h
2Ch	32	MSS_IOMUX_SPI0_CS0_CFG_REG	RW	5310 002Ch
30h	32	MSS_IOMUX_SPI0_CLK_CFG_REG	RW	5310 0030h
34h	32	MSS_IOMUX_SPI0_D0_CFG_REG	RW	5310 0034h
38h	32	MSS_IOMUX_SPI0_D1_CFG_REG	RW	5310 0038h
3Ch	32	MSS_IOMUX_SPI1_CS0_CFG_REG	RW	5310 003Ch
40h	32	MSS_IOMUX_SPI1_CLK_CFG_REG	RW	5310 0040h
44h	32	MSS_IOMUX_SPI1_D0_CFG_REG	RW	5310 0044h
48h	32	MSS_IOMUX_SPI1_D1_CFG_REG	RW	5310 0048h
4Ch	32	MSS_IOMUX_LIN1_RXD_CFG_REG	RW	5310 004Ch
50h	32	MSS_IOMUX_LIN1_TXD_CFG_REG	RW	5310 0050h

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Table 2-514. MSS_IOMUX Registers Base Address Table (continued)

Offset	Length	Acronym	Register Name	MSS_IOMUX Physical Address
54h	32	MSS_IOMUX_LIN2_RXD_CFG_REG	RW	5310 0054h
58h	32	MSS_IOMUX_LIN2_TXD_CFG_REG	RW	5310 0058h
5Ch	32	MSS_IOMUX_I2C1_SCL_CFG_REG	RW	5310 005Ch
60h	32	MSS_IOMUX_I2C1_SDA_CFG_REG	RW	5310 0060h
64h	32	MSS_IOMUX_UART0_RTSN_CFG_REG	RW	5310 0064h
68h	32	MSS_IOMUX_UART0_CTSN_CFG_REG	RW	5310 0068h
6Ch	32	MSS_IOMUX_UART0_RXD_CFG_REG	RW	5310 006Ch
70h	32	MSS_IOMUX_UART0_TXD_CFG_REG	RW	5310 0070h
74h	32	MSS_IOMUX_RGMII1_RXC_CFG_REG	RW	5310 0074h
78h	32	MSS_IOMUX_RGMII1_RX_CTL_CFG_REG	RW	5310 0078h
7Ch	32	MSS_IOMUX_RGMII1_RD0_CFG_REG	RW	5310 007Ch
80h	32	MSS_IOMUX_RGMII1_RD1_CFG_REG	RW	5310 0080h
84h	32	MSS_IOMUX_RGMII1_RD2_CFG_REG	RW	5310 0084h
88h	32	MSS_IOMUX_RGMII1_RD3_CFG_REG	RW	5310 0088h
8Ch	32	MSS_IOMUX_RGMII1_TXC_CFG_REG	RW	5310 008Ch
90h	32	MSS_IOMUX_RGMII1_TX_CTL_CFG_REG	RW	5310 0090h
94h	32	MSS_IOMUX_RGMII1_TD0_CFG_REG	RW	5310 0094h
98h	32	MSS_IOMUX_RGMII1_TD1_CFG_REG	RW	5310 0098h
9Ch	32	MSS_IOMUX_RGMII1_TD2_CFG_REG	RW	5310 009Ch
A0h	32	MSS_IOMUX_RGMII1_TD3_CFG_REG	RW	5310 00A0h
A4h	32	MSS_IOMUX_MDIO0_MDIO_CFG_REG	RW	5310 00A4h
A8h	32	MSS_IOMUX_MDIO0_MDC_CFG_REG	RW	5310 00A8h
ACh	32	MSS_IOMUX_EPWM0_A_CFG_REG	RW	5310 00ACh
B0h	32	MSS_IOMUX_EPWM0_B_CFG_REG	RW	5310 00B0h
B4h	32	MSS_IOMUX_EPWM1_A_CFG_REG	RW	5310 00B4h
B8h	32	MSS_IOMUX_EPWM1_B_CFG_REG	RW	5310 00B8h
BCh	32	MSS_IOMUX_EPWM2_A_CFG_REG	RW	5310 00BCh
C0h	32	MSS_IOMUX_EPWM2_B_CFG_REG	RW	5310 00C0h
C4h	32	MSS_IOMUX_EPWM3_A_CFG_REG	RW	5310 00C4h
C8h	32	MSS_IOMUX_EPWM3_B_CFG_REG	RW	5310 00C8h
CCh	32	MSS_IOMUX_EPWM4_A_CFG_REG	RW	5310 00CCh
D0h	32	MSS_IOMUX_EPWM4_B_CFG_REG	RW	5310 00D0h
D4h	32	MSS_IOMUX_EPWM5_A_CFG_REG	RW	5310 00D4h
D8h	32	MSS_IOMUX_EPWM5_B_CFG_REG	RW	5310 00D8h
DCh	32	MSS_IOMUX_EPWM6_A_CFG_REG	RW	5310 00DCh
E0h	32	MSS_IOMUX_EPWM6_B_CFG_REG	RW	5310 00E0h
E4h	32	MSS_IOMUX_EPWM7_A_CFG_REG	RW	5310 00E4h
E8h	32	MSS_IOMUX_EPWM7_B_CFG_REG	RW	5310 00E8h
ECh	32	MSS_IOMUX_EPWM8_A_CFG_REG	RW	5310 00ECh
F0h	32	MSS_IOMUX_EPWM8_B_CFG_REG	RW	5310 00F0h
F4h	32	MSS_IOMUX_EPWM9_A_CFG_REG	RW	5310 00F4h
F8h	32	MSS_IOMUX_EPWM9_B_CFG_REG	RW	5310 00F8h
FCh	32	MSS_IOMUX_EPWM10_A_CFG_REG	RW	5310 00FCh
100h	32	MSS_IOMUX_EPWM10_B_CFG_REG	RW	5310 0100h
104h	32	MSS_IOMUX_EPWM11_A_CFG_REG	RW	5310 0104h
108h	32	MSS_IOMUX_EPWM11_B_CFG_REG	RW	5310 0108h
10Ch	32	MSS_IOMUX_EPWM12_A_CFG_REG	RW	5310 010Ch

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Table 2-514. MSS_IOMUX Registers Base Address Table (continued)

Offset	Length	Acronym	Register Name	MSS_IOMUX Physical Address
110h	32	MSS_IOMUX_EPWM12_B_CFG_REG	RW	5310 0110h
114h	32	MSS_IOMUX_EPWM13_A_CFG_REG	RW	5310 0114h
118h	32	MSS_IOMUX_EPWM13_B_CFG_REG	RW	5310 0118h
11Ch	32	MSS_IOMUX_EPWM14_A_CFG_REG	RW	5310 011Ch
120h	32	MSS_IOMUX_EPWM14_B_CFG_REG	RW	5310 0120h
124h	32	MSS_IOMUX_EPWM15_A_CFG_REG	RW	5310 0124h
128h	32	MSS_IOMUX_EPWM15_B_CFG_REG	RW	5310 0128h
12Ch	32	MSS_IOMUX_UART1_RXD_CFG_REG	RW	5310 012Ch
130h	32	MSS_IOMUX_UART1_TXD_CFG_REG	RW	5310 0130h
134h	32	MSS_IOMUX_MMC0_CLK_CFG_REG	RW	5310 0134h
138h	32	MSS_IOMUX_MMC0_CMD_CFG_REG	RW	5310 0138h
13Ch	32	MSS_IOMUX_MMC0_D0_CFG_REG	RW	5310 013Ch
140h	32	MSS_IOMUX_MMC0_D1_CFG_REG	RW	5310 0140h
144h	32	MSS_IOMUX_MMC0_D2_CFG_REG	RW	5310 0144h
148h	32	MSS_IOMUX_MMC0_D3_CFG_REG	RW	5310 0148h
14Ch	32	MSS_IOMUX_MMC0_WP_CFG_REG	RW	5310 014Ch
150h	32	MSS_IOMUX_MMC0_CD_CFG_REG	RW	5310 0150h
154h	32	MSS_IOMUX_PR0_MDIO0_MDIO_CFG_REG	RW	5310 0154h
158h	32	MSS_IOMUX_PR0_MDIO0_MDC_CFG_REG	RW	5310 0158h
15Ch	32	MSS_IOMUX_PR0_PRU0_GPO5_CFG_REG	RW	5310 015Ch
160h	32	MSS_IOMUX_PR0_PRU0_GPO9_CFG_REG	RW	5310 0160h
164h	32	MSS_IOMUX_PR0_PRU0_GPO10_CFG_REG	RW	5310 0164h
168h	32	MSS_IOMUX_PR0_PRU0_GPO8_CFG_REG	RW	5310 0168h
16Ch	32	MSS_IOMUX_PR0_PRU0_GPO6_CFG_REG	RW	5310 016Ch
170h	32	MSS_IOMUX_PR0_PRU0_GPO4_CFG_REG	RW	5310 0170h
174h	32	MSS_IOMUX_PR0_PRU0_GPO0_CFG_REG	RW	5310 0174h
178h	32	MSS_IOMUX_PR0_PRU0_GPO1_CFG_REG	RW	5310 0178h
17Ch	32	MSS_IOMUX_PR0_PRU0_GPO2_CFG_REG	RW	5310 017Ch
180h	32	MSS_IOMUX_PR0_PRU0_GPO3_CFG_REG	RW	5310 0180h
184h	32	MSS_IOMUX_PR0_PRU0_GPO16_CFG_REG	RW	5310 0184h
188h	32	MSS_IOMUX_PR0_PRU0_GPO15_CFG_REG	RW	5310 0188h
18Ch	32	MSS_IOMUX_PR0_PRU0_GPO11_CFG_REG	RW	5310 018Ch
190h	32	MSS_IOMUX_PR0_PRU0_GPO12_CFG_REG	RW	5310 0190h
194h	32	MSS_IOMUX_PR0_PRU0_GPO13_CFG_REG	RW	5310 0194h

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Table 2-514. MSS_IOMUX Registers Base Address Table (continued)

Offset	Length	Acronym	Register Name	MSS_IOMUX Physical Address
198h	32	MSS_IOMUX_PR0_PRU0_GPO14_CFG_REG	RW	5310 0198h
19Ch	32	MSS_IOMUX_PR0_PRU1_GPO5_CFG_REG	RW	5310 019Ch
1A0h	32	MSS_IOMUX_PR0_PRU1_GPO9_CFG_REG	RW	5310 01A0h
1A4h	32	MSS_IOMUX_PR0_PRU1_GPO10_CFG_REG	RW	5310 01A4h
1A8h	32	MSS_IOMUX_PR0_PRU1_GPO8_CFG_REG	RW	5310 01A8h
1ACh	32	MSS_IOMUX_PR0_PRU1_GPO6_CFG_REG	RW	5310 01ACh
1B0h	32	MSS_IOMUX_PR0_PRU1_GPO4_CFG_REG	RW	5310 01B0h
1B4h	32	MSS_IOMUX_PR0_PRU1_GPO0_CFG_REG	RW	5310 01B4h
1B8h	32	MSS_IOMUX_PR0_PRU1_GPO1_CFG_REG	RW	5310 01B8h
1BCh	32	MSS_IOMUX_PR0_PRU1_GPO2_CFG_REG	RW	5310 01BCh
1C0h	32	MSS_IOMUX_PR0_PRU1_GPO3_CFG_REG	RW	5310 01C0h
1C4h	32	MSS_IOMUX_PR0_PRU1_GPO16_CFG_REG	RW	5310 01C4h
1C8h	32	MSS_IOMUX_PR0_PRU1_GPO15_CFG_REG	RW	5310 01C8h
1CCh	32	MSS_IOMUX_PR0_PRU1_GPO11_CFG_REG	RW	5310 01CCh
1D0h	32	MSS_IOMUX_PR0_PRU1_GPO12_CFG_REG	RW	5310 01D0h
1D4h	32	MSS_IOMUX_PR0_PRU1_GPO13_CFG_REG	RW	5310 01D4h
1D8h	32	MSS_IOMUX_PR0_PRU1_GPO14_CFG_REG	RW	5310 01D8h
1DCh	32	MSS_IOMUX_PR0_PRU1_GPO19_CFG_REG	RW	5310 01DCh
1E0h	32	MSS_IOMUX_PR0_PRU1_GPO18_CFG_REG	RW	5310 01E0h
1E4h	32	MSS_IOMUX_EXT_REFCLK0_CFG_REG	RW	5310 01E4h
1E8h	32	MSS_IOMUX_SDFM0_CLK0_CFG_REG	RW	5310 01E8h
1ECh	32	MSS_IOMUX_SDFM0_D0_CFG_REG	RW	5310 01ECh
1F0h	32	MSS_IOMUX_SDFM0_CLK1_CFG_REG	RW	5310 01F0h
1F4h	32	MSS_IOMUX_SDFM0_D1_CFG_REG	RW	5310 01F4h
1F8h	32	MSS_IOMUX_SDFM0_CLK2_CFG_REG	RW	5310 01F8h
1FCh	32	MSS_IOMUX_SDFM0_D2_CFG_REG	RW	5310 01FCh
200h	32	MSS_IOMUX_SDFM0_CLK3_CFG_REG	RW	5310 0200h
204h	32	MSS_IOMUX_SDFM0_D3_CFG_REG	RW	5310 0204h
208h	32	MSS_IOMUX_EQEP0_A_CFG_REG	RW	5310 0208h
20Ch	32	MSS_IOMUX_EQEP0_B_CFG_REG	RW	5310 020Ch
210h	32	MSS_IOMUX_EQEP0_STROBE_CFG_REG	RW	5310 0210h
214h	32	MSS_IOMUX_EQEP0_INDEX_CFG_REG	RW	5310 0214h
218h	32	MSS_IOMUX_I2C0_SDA_CFG_REG	RW	5310 0218h

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Table 2-514. MSS_IOMUX Registers Base Address Table (continued)

Offset	Length	Acronym	Register Name	MSS_IOMUX Physical Address
21Ch	32	MSS_IOMUX_I2C0_SCL_CFG_REG	RW	5310 021Ch
220h	32	MSS_IOMUX_MCAN2_TX_CFG_REG	RW	5310 0220h
224h	32	MSS_IOMUX_MCAN2_RX_CFG_REG	RW	5310 0224h
228h	32	MSS_IOMUX_CLKOUT0_CFG_REG	RW	5310 0228h
22Ch	32	MSS_IOMUX_WARMRSTN_CFG_REG	RW	5310 022Ch
230h	32	MSS_IOMUX_SAFETY_ERRORN_CFG_REG	RW	5310 0230h
234h	32	MSS_IOMUX_TDI_CFG_REG	RW	5310 0234h
238h	32	MSS_IOMUX_TDO_CFG_REG	RW	5310 0238h
23Ch	32	MSS_IOMUX_TMS_CFG_REG	RW	5310 023Ch
240h	32	MSS_IOMUX_TCK_CFG_REG	RW	5310 0240h
244h	32	MSS_IOMUX_QSPI0_CLKLB_CFG_REG	RW	5310 0244h
248h	32	MSS_IOMUX_QUAL_GRP_0_CFG_REG	RW	5310 0248h
24Ch	32	MSS_IOMUX_QUAL_GRP_1_CFG_REG	RW	5310 024Ch
250h	32	MSS_IOMUX_QUAL_GRP_2_CFG_REG	RW	5310 0250h
254h	32	MSS_IOMUX_QUAL_GRP_3_CFG_REG	RW	5310 0254h
258h	32	MSS_IOMUX_QUAL_GRP_4_CFG_REG	RW	5310 0258h
25Ch	32	MSS_IOMUX_QUAL_GRP_5_CFG_REG	RW	5310 025Ch
260h	32	MSS_IOMUX_QUAL_GRP_6_CFG_REG	RW	5310 0260h
264h	32	MSS_IOMUX_QUAL_GRP_7_CFG_REG	RW	5310 0264h
268h	32	MSS_IOMUX_QUAL_GRP_8_CFG_REG	RW	5310 0268h
26Ch	32	MSS_IOMUX_QUAL_GRP_9_CFG_REG	RW	5310 026Ch
270h	32	MSS_IOMUX_QUAL_GRP_10_CFG_REG	RW	5310 0270h
274h	32	MSS_IOMUX_QUAL_GRP_11_CFG_REG	RW	5310 0274h
278h	32	MSS_IOMUX_QUAL_GRP_12_CFG_REG	RW	5310 0278h
27Ch	32	MSS_IOMUX_QUAL_GRP_13_CFG_REG	RW	5310 027Ch
280h	32	MSS_IOMUX_QUAL_GRP_14_CFG_REG	RW	5310 0280h
284h	32	MSS_IOMUX_QUAL_GRP_15_CFG_REG	RW	5310 0284h
288h	32	MSS_IOMUX_QUAL_GRP_16_CFG_REG	RW	5310 0288h
28Ch	32	MSS_IOMUX_QUAL_GRP_17_CFG_REG	RW	5310 028Ch
290h	32	MSS_IOMUX_USER_MODE_EN	RW	5310 0290h
294h	32	MSS_IOMUX_PADGLBL_CFG_REG	RW	5310 0294h
298h	32	MSS_IOMUX_IO_CFG_KICK0	RW	5310 0298h
29Ch	32	MSS_IOMUX_IO_CFG_KICK1	RW	5310 029Ch

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2.4.1 MSS_IOMUX_QSPI0_CSN0_CFG_REG Registers

2.4.1.1 IOMUX_CSN0_CFG_REG Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-515. Instance Table

Instance Name	Physical Address
IOMUX	5310 0000h

Access Types Legend

Table 2-516. QSPI0_CSN0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-516. QSPI0_CSN0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.2 MSS_IOMUX_QSPI0_CSN1_CFG_REG Registers

2.4.2.1 IOMUX_CSN1_CFG_REG Register (Offset = 4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-517. Instance Table

Instance Name	Physical Address
IOMUX	5310 0004h

Access Types Legend

Table 2-518. QSPI0_CSN1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-518. QSPI0_CSN1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.3 MSS_IOMUX_QSPI0_CLK_CFG_REG Registers

2.4.3.1 IOMUX_CLK_CFG_REG Register (Offset = 8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-519. Instance Table

Instance Name	Physical Address
IOMUX	5310 0008h

Access Types Legend

Table 2-520. QSPI0_CLK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Enable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-520. QSPI0_CLK_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.4 MSS_IOMUX_QSPI0_D0_CFG_REG Registers

2.4.4.1 IOMUX_D0_CFG_REG Register (Offset = Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-521. Instance Table

Instance Name	Physical Address
IOMUX	5310 000Ch

Access Types Legend

Table 2-522. QSPI0_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-522. QSPI0_D0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.5 MSS_IOMUX_QSPI0_D1_CFG_REG Registers

2.4.5.1 IOMUX_D1_CFG_REG Register (Offset = 10h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-523. Instance Table

Instance Name	Physical Address
IOMUX	5310 0010h

Access Types Legend

Table 2-524. QSPI0_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-524. QSPI0_D1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.6 MSS_IOMUX_QSPI0_D2_CFG_REG Registers

2.4.6.1 IOMUX_D2_CFG_REG Register (Offset = 14h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-525. Instance Table

Instance Name	Physical Address
IOMUX	5310 0014h

Access Types Legend

Table 2-526. QSPI0_D2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-526. QSPI0_D2_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.7 MSS_IOMUX_QSPI0_D3_CFG_REG Registers

2.4.7.1 IOMUX_D3_CFG_REG Register (Offset = 18h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-527. Instance Table

Instance Name	Physical Address
IOMUX	5310 0018h

Access Types Legend

Table 2-528. QSPI0_D3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-528. QSPI0_D3_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.8 MSS_IOMUX_MCAN0_RX_CFG_REG Registers

2.4.8.1 IOMUX_RX_CFG_REG Register (Offset = 1Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-529. Instance Table

Instance Name	Physical Address
IOMUX	5310 001Ch

Access Types Legend

Table 2-530. MCAN0_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-530. MCAN0_RX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.9 MSS_IOMUX_MCAN0_TX_CFG_REG Registers

2.4.9.1 IOMUX_TX_CFG_REG Register (Offset = 20h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-531. Instance Table

Instance Name	Physical Address
IOMUX	5310 0020h

Access Types Legend

Table 2-532. MCAN0_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-532. MCAN0_TX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.10 MSS_IOMUX_MCAN1_RX_CFG_REG Registers

2.4.10.1 IOMUX_RX_CFG_REG Register (Offset = 24h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-533. Instance Table

Instance Name	Physical Address
IOMUX	5310 0024h

Access Types Legend

Table 2-534. MCAN1_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-534. MCAN1_RX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.11 MSS_IOMUX_MCAN1_TX_CFG_REG Registers

2.4.11.1 IOMUX_TX_CFG_REG Register (Offset = 28h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-535. Instance Table

Instance Name	Physical Address
IOMUX	5310 0028h

Access Types Legend

Table 2-536. MCAN1_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-536. MCAN1_TX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.12 MSS_IOMUX_SPI0_CS0_CFG_REG Registers

2.4.12.1 IOMUX_CS0_CFG_REG Register (Offset = 2Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-537. Instance Table

Instance Name	Physical Address
IOMUX	5310 002Ch

Access Types Legend

Table 2-538. SPI0_CS0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-538. SPI0_CS0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.13 MSS_IOMUX_SPI0_CLK_CFG_REG Registers

2.4.13.1 IOMUX_CLK_CFG_REG Register (Offset = 30h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-539. Instance Table

Instance Name	Physical Address
IOMUX	5310 0030h

Access Types Legend

Table 2-540. SPI0_CLK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-540. SPI0_CLK_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.14 MSS_IOMUX_SPI0_D0_CFG_REG Registers

2.4.14.1 IOMUX_D0_CFG_REG Register (Offset = 34h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-541. Instance Table

Instance Name	Physical Address
IOMUX	5310 0034h

Access Types Legend

Table 2-542. SPI0_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-542. SPI0_D0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.15 MSS_IOMUX_SPI0_D1_CFG_REG Registers

2.4.15.1 IOMUX_D1_CFG_REG Register (Offset = 38h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-543. Instance Table

Instance Name	Physical Address
IOMUX	5310 0038h

Access Types Legend

Table 2-544. SPI0_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-544. SPI0_D1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.16 MSS_IOMUX_SPI1_CS0_CFG_REG Registers

2.4.16.1 IOMUX_CS0_CFG_REG Register (Offset = 3Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-545. Instance Table

Instance Name	Physical Address
IOMUX	5310 003Ch

Access Types Legend

Table 2-546. SPI1_CS0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-546. SPI1_CS0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.17 MSS_IOMUX_SPI1_CLK_CFG_REG Registers

2.4.17.1 IOMUX_CLK_CFG_REG Register (Offset = 40h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-547. Instance Table

Instance Name	Physical Address
IOMUX	5310 0040h

Access Types Legend

Table 2-548. SPI1_CLK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-548. SPI1_CLK_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.18 MSS_IOMUX_SPI1_D0_CFG_REG Registers

2.4.18.1 IOMUX_D0_CFG_REG Register (Offset = 44h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-549. Instance Table

Instance Name	Physical Address
IOMUX	5310 0044h

Access Types Legend

Table 2-550. SPI1_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-550. SPI1_D0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.19 MSS_IOMUX_SPI1_D1_CFG_REG Registers

2.4.19.1 IOMUX_D1_CFG_REG Register (Offset = 48h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-551. Instance Table

Instance Name	Physical Address
IOMUX	5310 0048h

Access Types Legend

Table 2-552. SPI1_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-552. SPI1_D1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.20 MSS_IOMUX_LIN1_RXD_CFG_REG Registers

2.4.20.1 IOMUX_RXD_CFG_REG Register (Offset = 4Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-553. Instance Table

Instance Name	Physical Address
IOMUX	5310 004Ch

Access Types Legend

Table 2-554. LIN1_RXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-554. LIN1_RXD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.21 IOMUX_MSS_IOMUX_LIN1_TXD_CFG_REG Registers

2.4.21.1 IOMUX_TXD_CFG_REG Register (Offset = 50h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-555. Instance Table

Instance Name	Physical Address
IOMUX	5310 0050h

Access Types Legend

Table 2-556. LIN1_TXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-556. LIN1_TXD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.22 IOMUX_MSS_IOMUX_LIN2_RXD_CFG_REG Registers

2.4.22.1 IOMUX_RXD_CFG_REG Register (Offset = 54h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-557. Instance Table

Instance Name	Physical Address
IOMUX	5310 0054h

Access Types Legend

Table 2-558. LIN2_RXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-558. LIN2_RXD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.23 IOMUX_MSS_IOMUX_LIN2_TXD_CFG_REG Registers

2.4.23.1 IOMUX_TXD_CFG_REG Register (Offset = 58h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-559. Instance Table

Instance Name	Physical Address
IOMUX	5310 0058h

Access Types Legend

Table 2-560. LIN2_TXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-560. LIN2_TXD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.24 IOMUX_MSS_IOMUX_I2C1_SCL_CFG_REG Registers

2.4.24.1 IOMUX_SCL_CFG_REG Register (Offset = 5Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-561. Instance Table

Instance Name	Physical Address
IOMUX	5310 005Ch

Access Types Legend

Table 2-562. I2C1_SCL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-562. I2C1_SCL_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.25 IOMUX_MSS_IOMUX_I2C1_SDA_CFG_REG Registers

2.4.25.1 IOMUX_SDA_CFG_REG Register (Offset = 60h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-563. Instance Table

Instance Name	Physical Address
IOMUX	5310 0060h

Access Types Legend

Table 2-564. I2C1_SDA_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-564. I2C1_SDA_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.26 IOMUX_MSS_IOMUX_UART0_RTSN_CFG_REG Registers

2.4.26.1 IOMUX_RTSN_CFG_REG Register (Offset = 64h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-565. Instance Table

Instance Name	Physical Address
IOMUX	5310 0064h

Access Types Legend

Table 2-566. UART0_RTSN_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-566. UART0_RTSN_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.27 IOMUX_MSS_IOMUX_UART0_CTSN_CFG_REG Registers

2.4.27.1 IOMUX_CTSN_CFG_REG Register (Offset = 68h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-567. Instance Table

Instance Name	Physical Address
IOMUX	5310 0068h

Access Types Legend

Table 2-568. UART0_CTSN_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-568. UART0_CTSN_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.28 IOMUX_MSS_IOMUX_UART0_RXD_CFG_REG Registers

2.4.28.1 IOMUX_RXD_CFG_REG Register (Offset = 6Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-569. Instance Table

Instance Name	Physical Address
IOMUX	5310 006Ch

Access Types Legend

Table 2-570. UART0_RXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-570. UART0_RXD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.29 IOMUX_MSS_IOMUX_UART0_TXD_CFG_REG Registers

2.4.29.1 IOMUX_TXD_CFG_REG Register (Offset = 70h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-571. Instance Table

Instance Name	Physical Address
IOMUX	5310 0070h

Access Types Legend

Table 2-572. UART0_TXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-572. UART0_TXD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.30 IOMUX_MSS_IOMUX_RGMII1_RXC_CFG_REG Registers

2.4.30.1 IOMUX_RXC_CFG_REG Register (Offset = 74h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-573. Instance Table

Instance Name	Physical Address
IOMUX	5310 0074h

Access Types Legend

Table 2-574. RGMII1_RXC_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-574. RGMII1_RXC_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.31 IOMUX_MSS_IOMUX_RGMII1_RX_CTL_CFG_REG Registers

2.4.31.1 IOMUX_RX_CTL_CFG_REG Register (Offset = 78h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-575. Instance Table

Instance Name	Physical Address
IOMUX	5310 0078h

Access Types Legend

Table 2-576. RGMII1_RX_CTL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Enable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-576. RGMII1_RX_CTL_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.32 IOMUX_MSS_IOMUX_RGMII1_RD0_CFG_REG Registers

2.4.32.1 IOMUX_RD0_CFG_REG Register (Offset = 7Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-577. Instance Table

Instance Name	Physical Address
IOMUX	5310 007Ch

Access Types Legend

Table 2-578. RGMII1_RD0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-578. RGMII1_RD0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.33 IOMUX_MSS_IOMUX_RGMII1_RD1_CFG_REG Registers

2.4.33.1 IOMUX_RD1_CFG_REG Register (Offset = 80h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-579. Instance Table

Instance Name	Physical Address
IOMUX	5310 0080h

Access Types Legend

Table 2-580. RGMII1_RD1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-580. RGMII1_RD1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.34 IOMUX_MSS_IOMUX_RGMII1_RD2_CFG_REG Registers

2.4.34.1 IOMUX_RD2_CFG_REG Register (Offset = 84h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-581. Instance Table

Instance Name	Physical Address
IOMUX	5310 0084h

Access Types Legend

Table 2-582. RGMII1_RD2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-582. RGMII1_RD2_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.35 IOMUX_MSS_IOMUX_RGMII1_RD3_CFG_REG Registers

2.4.35.1 IOMUX_RD3_CFG_REG Register (Offset = 88h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-583. Instance Table

Instance Name	Physical Address
IOMUX	5310 0088h

Access Types Legend

Table 2-584. RGMII1_RD3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-584. RGMII1_RD3_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.36 IOMUX_MSS_IOMUX_RGMII1_TXC_CFG_REG Registers

2.4.36.1 IOMUX_TXC_CFG_REG Register (Offset = 8Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-585. Instance Table

Instance Name	Physical Address
IOMUX	5310 008Ch

Access Types Legend

Table 2-586. RGMII1_TXC_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-586. RGMII1_TXC_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.37 IOMUX_MSS_IOMUX_RGMII1_TX_CTL_CFG_REG Registers

2.4.37.1 IOMUX_TX_CTL_CFG_REG Register (Offset = 90h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-587. Instance Table

Instance Name	Physical Address
IOMUX	5310 0090h

Access Types Legend

Table 2-588. RGMII1_TX_CTL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-588. RGMII1_TX_CTL_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.38 IOMUX_MSS_IOMUX_RGMII1_TD0_CFG_REG Registers

2.4.38.1 IOMUX_TD0_CFG_REG Register (Offset = 94h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-589. Instance Table

Instance Name	Physical Address
IOMUX	5310 0094h

Access Types Legend

Table 2-590. RGMII1_TD0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-590. RGMII1_TD0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.39 IOMUX_MSS_IOMUX_RGMII1_TD1_CFG_REG Registers

2.4.39.1 IOMUX_TD1_CFG_REG Register (Offset = 98h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-591. Instance Table

Instance Name	Physical Address
IOMUX	5310 0098h

Access Types Legend

Table 2-592. RGMII1_TD1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-592. RGMII1_TD1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.40 IOMUX_MSS_IOMUX_RGMII1_TD2_CFG_REG Registers

2.4.40.1 IOMUX_TD2_CFG_REG Register (Offset = 9Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-593. Instance Table

Instance Name	Physical Address
IOMUX	5310 009Ch

Access Types Legend

Table 2-594. RGMII1_TD2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-594. RGMII1_TD2_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.41 IOMUX_MSS_IOMUX_RGMII1_TD3_CFG_REG Registers

2.4.41.1 IOMUX_TD3_CFG_REG Register (Offset = A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-595. Instance Table

Instance Name	Physical Address
IOMUX	5310 00A0h

Access Types Legend

Table 2-596. RGMII1_TD3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-596. RGMII1_TD3_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.42 IOMUX_MSS_IOMUX_MDIO0_MDIO_CFG_REG Registers

2.4.42.1 IOMUX_MDIO_CFG_REG Register (Offset = A4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-597. Instance Table

Instance Name	Physical Address
IOMUX	5310 00A4h

Access Types Legend

Table 2-598. MDIO0_MDIO_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-598. MDIO0_MDIO_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.43 IOMUX_MSS_IOMUX_MDIO0_MDC_CFG_REG Registers

2.4.43.1 IOMUX_MDC_CFG_REG Register (Offset = A8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-599. Instance Table

Instance Name	Physical Address
IOMUX	5310 00A8h

Access Types Legend

Table 2-600. MDIO0_MDC_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-600. MDIO0_MDC_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.44 IOMUX_MSS_IOMUX_EPWM0_A_CFG_REG Registers

2.4.44.1 IOMUX_A_CFG_REG Register (Offset = ACh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-601. Instance Table

Instance Name	Physical Address
IOMUX	5310 00ACh

Access Types Legend

Table 2-602. EPWM0_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-602. EPWM0_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.45 IOMUX_MSS_IOMUX_EPWM0_B_CFG_REG Registers

2.4.45.1 IOMUX_B_CFG_REG Register (Offset = B0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-603. Instance Table

Instance Name	Physical Address
IOMUX	5310 00B0h

Access Types Legend

Table 2-604. EPWM0_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-604. EPWM0_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.46 IOMUX_MSS_IOMUX_EPWM1_A_CFG_REG Registers

2.4.46.1 IOMUX_A_CFG_REG Register (Offset = B4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-605. Instance Table

Instance Name	Physical Address
IOMUX	5310 00B4h

Access Types Legend

Table 2-606. EPWM1_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-606. EPWM1_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.47 IOMUX_MSS_IOMUX_EPWM1_B_CFG_REG Registers

2.4.47.1 IOMUX_B_CFG_REG Register (Offset = B8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-607. Instance Table

Instance Name	Physical Address
IOMUX	5310 00B8h

Access Types Legend

Table 2-608. EPWM1_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-608. EPWM1_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.48 IOMUX_MSS_IOMUX_EPWM2_A_CFG_REG Registers

2.4.48.1 IOMUX_A_CFG_REG Register (Offset = BCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-609. Instance Table

Instance Name	Physical Address
IOMUX	5310 00BCh

Access Types Legend

Table 2-610. EPWM2_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware

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Table 2-610. EPWM2_A_CFG_REG Register Field Descriptions (continued)

5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.49 IOMUX_MSS_IOMUX_EPWM2_B_CFG_REG Registers

2.4.49.1 IOMUX_B_CFG_REG Register (Offset = C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-611. Instance Table

Instance Name	Physical Address
IOMUX	5310 00C0h

Access Types Legend

Table 2-612. EPWM2_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-612. EPWM2_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.50 IOMUX_MSS_IOMUX_EPWM3_A_CFG_REG Registers

2.4.50.1 IOMUX_A_CFG_REG Register (Offset = C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-613. Instance Table

Instance Name	Physical Address
IOMUX	5310 00C4h

Access Types Legend

Table 2-614. EPWM3_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-614. EPWM3_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.51 IOMUX_MSS_IOMUX_EPWM3_B_CFG_REG Registers

2.4.51.1 IOMUX_B_CFG_REG Register (Offset = C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-615. Instance Table

Instance Name	Physical Address
IOMUX	5310 00C8h

Access Types Legend

Table 2-616. EPWM3_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-616. EPWM3_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.52 IOMUX_MSS_IOMUX_EPWM4_A_CFG_REG Registers

2.4.52.1 IOMUX_A_CFG_REG Register (Offset = CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-617. Instance Table

Instance Name	Physical Address
IOMUX	5310 00CCh

Access Types Legend

Table 2-618. EPWM4_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-618. EPWM4_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.53 IOMUX_MSS_IOMUX_EPWM4_B_CFG_REG Registers

2.4.53.1 IOMUX_B_CFG_REG Register (Offset = D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-619. Instance Table

Instance Name	Physical Address
IOMUX	5310 00D0h

Access Types Legend

Table 2-620. EPWM4_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-620. EPWM4_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.54 IOMUX_MSS_IOMUX_EPWM5_A_CFG_REG Registers

2.4.54.1 IOMUX_A_CFG_REG Register (Offset = D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-621. Instance Table

Instance Name	Physical Address
IOMUX	5310 00D4h

Access Types Legend

Table 2-622. EPWM5_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-622. EPWM5_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.55 IOMUX_MSS_IOMUX_EPWM5_B_CFG_REG Registers

2.4.55.1 IOMUX_B_CFG_REG Register (Offset = D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-623. Instance Table

Instance Name	Physical Address
IOMUX	5310 00D8h

Access Types Legend

Table 2-624. EPWM5_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-624. EPWM5_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.56 IOMUX_MSS_IOMUX_EPWM6_A_CFG_REG Registers

2.4.56.1 IOMUX_A_CFG_REG Register (Offset = DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-625. Instance Table

Instance Name	Physical Address
IOMUX	5310 00DCh

Access Types Legend

Table 2-626. EPWM6_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-626. EPWM6_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.57 IOMUX_MSS_IOMUX_EPWM6_B_CFG_REG Registers

2.4.57.1 IOMUX_B_CFG_REG Register (Offset = E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-627. Instance Table

Instance Name	Physical Address
IOMUX	5310 00E0h

Access Types Legend

Table 2-628. EPWM6_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-628. EPWM6_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.58 IOMUX_MSS_IOMUX_EPWM7_A_CFG_REG Registers

2.4.58.1 IOMUX_A_CFG_REG Register (Offset = E4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-629. Instance Table

Instance Name	Physical Address
IOMUX	5310 00E4h

Access Types Legend

Table 2-630. EPWM7_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-630. EPWM7_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.59 IOMUX_MSS_IOMUX_EPWM7_B_CFG_REG Registers

2.4.59.1 IOMUX_B_CFG_REG Register (Offset = E8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-631. Instance Table

Instance Name	Physical Address
IOMUX	5310 00E8h

Access Types Legend

Table 2-632. EPWM7_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-632. EPWM7_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.60 IOMUX_MSS_IOMUX_EPWM8_A_CFG_REG Registers

2.4.60.1 IOMUX_A_CFG_REG Register (Offset = ECh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-633. Instance Table

Instance Name	Physical Address
IOMUX	5310 00ECh

Access Types Legend

Table 2-634. EPWM8_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-634. EPWM8_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.61 IOMUX_MSS_IOMUX_EPWM8_B_CFG_REG Registers

2.4.61.1 IOMUX_B_CFG_REG Register (Offset = F0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-635. Instance Table

Instance Name	Physical Address
IOMUX	5310 00F0h

Access Types Legend

Table 2-636. EPWM8_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-636. EPWM8_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.62 IOMUX_MSS_IOMUX_EPWM9_A_CFG_REG Registers

2.4.62.1 IOMUX_A_CFG_REG Register (Offset = F4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-637. Instance Table

Instance Name	Physical Address
IOMUX	5310 00F4h

Access Types Legend

Table 2-638. EPWM9_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-638. EPWM9_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.63 IOMUX_MSS_IOMUX_EPWM9_B_CFG_REG Registers

2.4.63.1 IOMUX_B_CFG_REG Register (Offset = F8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-639. Instance Table

Instance Name	Physical Address
IOMUX	5310 00F8h

Access Types Legend

Table 2-640. EPWM9_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-640. EPWM9_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.64 IOMUX_MSS_IOMUX_EPWM10_A_CFG_REG Registers

2.4.64.1 IOMUX_A_CFG_REG Register (Offset = FCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-641. Instance Table

Instance Name	Physical Address
IOMUX	5310 00FCh

Access Types Legend

Table 2-642. EPWM10_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-642. EPWM10_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.65 IOMUX_MSS_IOMUX_EPWM10_B_CFG_REG Registers

2.4.65.1 IOMUX_B_CFG_REG Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-643. Instance Table

Instance Name	Physical Address
IOMUX	5310 0100h

Access Types Legend

Table 2-644. EPWM10_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-644. EPWM10_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.66 IOMUX_MSS_IOMUX_EPWM11_A_CFG_REG Registers

2.4.66.1 IOMUX_A_CFG_REG Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-645. Instance Table

Instance Name	Physical Address
IOMUX	5310 0104h

Access Types Legend

Table 2-646. EPWM11_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-646. EPWM11_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.67 IOMUX_MSS_IOMUX_EPWM11_B_CFG_REG Registers

2.4.67.1 IOMUX_B_CFG_REG Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-647. Instance Table

Instance Name	Physical Address
IOMUX	5310 0108h

Access Types Legend

Table 2-648. EPWM11_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-648. EPWM11_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.68 IOMUX_MSS_IOMUX_EPWM12_A_CFG_REG Registers

2.4.68.1 IOMUX_A_CFG_REG Register (Offset = 10Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-649. Instance Table

Instance Name	Physical Address
IOMUX	5310 010Ch

Access Types Legend

Table 2-650. EPWM12_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-650. EPWM12_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.69 IOMUX_MSS_IOMUX_EPWM12_B_CFG_REG Registers

2.4.69.1 IOMUX_B_CFG_REG Register (Offset = 110h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-651. Instance Table

Instance Name	Physical Address
IOMUX	5310 0110h

Access Types Legend

Table 2-652. EPWM12_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-652. EPWM12_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.70 IOMUX_MSS_IOMUX_EPWM13_A_CFG_REG Registers

2.4.70.1 IOMUX_A_CFG_REG Register (Offset = 114h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-653. Instance Table

Instance Name	Physical Address
IOMUX	5310 0114h

Access Types Legend

Table 2-654. EPWM13_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-654. EPWM13_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.71 IOMUX_MSS_IOMUX_EPWM13_B_CFG_REG Registers

2.4.71.1 IOMUX_B_CFG_REG Register (Offset = 118h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-655. Instance Table

Instance Name	Physical Address
IOMUX	5310 0118h

Access Types Legend

Table 2-656. EPWM13_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-656. EPWM13_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.72 IOMUX_MSS_IOMUX_EPWM14_A_CFG_REG Registers

2.4.72.1 IOMUX_A_CFG_REG Register (Offset = 11Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-657. Instance Table

Instance Name	Physical Address
IOMUX	5310 011Ch

Access Types Legend

Table 2-658. EPWM14_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-658. EPWM14_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.73 IOMUX_MSS_IOMUX_EPWM14_B_CFG_REG Registers

2.4.73.1 IOMUX_B_CFG_REG Register (Offset = 120h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-659. Instance Table

Instance Name	Physical Address
IOMUX	5310 0120h

Access Types Legend

Table 2-660. EPWM14_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-660. EPWM14_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.74 IOMUX_MSS_IOMUX_EPWM15_A_CFG_REG Registers

2.4.74.1 IOMUX_A_CFG_REG Register (Offset = 124h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-661. Instance Table

Instance Name	Physical Address
IOMUX	5310 0124h

Access Types Legend

Table 2-662. EPWM15_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-662. EPWM15_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.75 IOMUX_MSS_IOMUX_EPWM15_B_CFG_REG Registers

2.4.75.1 IOMUX_B_CFG_REG Register (Offset = 128h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-663. Instance Table

Instance Name	Physical Address
IOMUX	5310 0128h

Access Types Legend

Table 2-664. EPWM15_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-664. EPWM15_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.76 IOMUX_MSS_IOMUX_UART1_RXD_CFG_REG Registers

2.4.76.1 IOMUX_RXD_CFG_REG Register (Offset = 12Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-665. Instance Table

Instance Name	Physical Address
IOMUX	5310 012Ch

Access Types Legend

Table 2-666. UART1_RXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-666. UART1_RXD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.77 IOMUX_MSS_IOMUX_UART1_TXD_CFG_REG Registers

2.4.77.1 IOMUX_TXD_CFG_REG Register (Offset = 130h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-667. Instance Table

Instance Name	Physical Address
IOMUX	5310 0130h

Access Types Legend

Table 2-668. UART1_TXD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-668. UART1_TXD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.78 IOMUX_MSS_IOMUX_MMC0_CLK_CFG_REG Registers

2.4.78.1 IOMUX_CLK_CFG_REG Register (Offset = 134h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-669. Instance Table

Instance Name	Physical Address
IOMUX	5310 0134h

Access Types Legend

Table 2-670. MMC0_CLK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-670. MMC0_CLK_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.79 IOMUX_MSS_IOMUX_MMC0_CMD_CFG_REG Registers

2.4.79.1 IOMUX_CMD_CFG_REG Register (Offset = 138h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-671. Instance Table

Instance Name	Physical Address
IOMUX	5310 0138h

Access Types Legend

Table 2-672. MMC0_CMD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-672. MMC0_CMD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.80 IOMUX_MSS_IOMUX_MMC0_D0_CFG_REG Registers

2.4.80.1 IOMUX_D0_CFG_REG Register (Offset = 13Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-673. Instance Table

Instance Name	Physical Address
IOMUX	5310 013Ch

Access Types Legend

Table 2-674. MMC0_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-674. MMC0_D0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.81 IOMUX_MSS_IOMUX_MMC0_D1_CFG_REG Registers

2.4.81.1 IOMUX_D1_CFG_REG Register (Offset = 140h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-675. Instance Table

Instance Name	Physical Address
IOMUX	5310 0140h

Access Types Legend

Table 2-676. MMC0_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-676. MMC0_D1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.82 IOMUX_MSS_IOMUX_MMC0_D2_CFG_REG Registers

2.4.82.1 IOMUX_D2_CFG_REG Register (Offset = 144h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-677. Instance Table

Instance Name	Physical Address
IOMUX	5310 0144h

Access Types Legend

Table 2-678. MMC0_D2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-678. MMC0_D2_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.83 IOMUX_MSS_IOMUX_MMC0_D3_CFG_REG Registers

2.4.83.1 IOMUX_D3_CFG_REG Register (Offset = 148h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-679. Instance Table

Instance Name	Physical Address
IOMUX	5310 0148h

Access Types Legend

Table 2-680. MMC0_D3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-680. MMC0_D3_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.84 IOMUX_MSS_IOMUX_MMC0_WP_CFG_REG Registers

2.4.84.1 IOMUX_WP_CFG_REG Register (Offset = 14Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-681. Instance Table

Instance Name	Physical Address
IOMUX	5310 014Ch

Access Types Legend

Table 2-682. MMC0_WP_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-682. MMC0_WP_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.85 IOMUX_MSS_IOMUX_MMC0_CD_CFG_REG Registers

2.4.85.1 IOMUX_CD_CFG_REG Register (Offset = 150h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-683. Instance Table

Instance Name	Physical Address
IOMUX	5310 0150h

Access Types Legend

Table 2-684. MMC0_CD_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-684. MMC0_CD_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.86 IOMUX_MSS_IOMUX_PR0_MDIO0_MDIO_CFG_REG Registers

2.4.86.1 IOMUX_MDIO0_MDIO_CFG_REG Register (Offset = 154h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-685. Instance Table

Instance Name	Physical Address
IOMUX	5310 0154h

Access Types Legend

Table 2-686. PR0_MDIO0_MDIO_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-686. PR0_MDIO0_MDIO_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.87 IOMUX_MSS_IOMUX_PR0_MDIO0_MDC_CFG_REG Registers

2.4.87.1 IOMUX_MDIO0_MDC_CFG_REG Register (Offset = 158h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-687. Instance Table

Instance Name	Physical Address
IOMUX	5310 0158h

Access Types Legend

Table 2-688. PR0_MDIO0_MDC_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-688. PR0_MDIO0_MDC_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.88 IOMUX_MSS_IOMUX_PR0_PRU0_GPO5_CFG_REG Registers

2.4.88.1 IOMUX_PRU0_GPO5_CFG_REG Register (Offset = 15Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-689. Instance Table

Instance Name	Physical Address
IOMUX	5310 015Ch

Access Types Legend

Table 2-690. PR0_PRU0_GPO5_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-690. PR0_PRU0_GPO5_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.89 IOMUX_MSS_IOMUX_PR0_PRU0_GPO9_CFG_REG Registers

2.4.89.1 IOMUX_PRU0_GPO9_CFG_REG Register (Offset = 160h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-691. Instance Table

Instance Name	Physical Address
IOMUX	5310 0160h

Access Types Legend

Table 2-692. PR0_PRU0_GPO9_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-692. PR0_PRU0_GPO9_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.90 IOMUX_MSS_IOMUX_PR0_PRU0_GPO10_CFG_REG Registers

2.4.90.1 IOMUX_PRU0_GPO10_CFG_REG Register (Offset = 164h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-693. Instance Table

Instance Name	Physical Address
IOMUX	5310 0164h

Access Types Legend

Table 2-694. PR0_PRU0_GPO10_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-694. PR0_PRU0_GPO10_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.91 IOMUX_MSS_IOMUX_PR0_PRU0_GPO8_CFG_REG Registers

2.4.91.1 IOMUX_PRU0_GPO8_CFG_REG Register (Offset = 168h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-695. Instance Table

Instance Name	Physical Address
IOMUX	5310 0168h

Access Types Legend

Table 2-696. PR0_PRU0_GPO8_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-696. PR0_PRU0_GPO8_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.92 IOMUX_MSS_IOMUX_PR0_PRU0_GPO6_CFG_REG Registers

2.4.92.1 IOMUX_PRU0_GPO6_CFG_REG Register (Offset = 16Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-697. Instance Table

Instance Name	Physical Address
IOMUX	5310 016Ch

Access Types Legend

Table 2-698. PR0_PRU0_GPO6_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-698. PR0_PRU0_GPO6_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.93 IOMUX_MSS_IOMUX_PR0_PRU0_GPO4_CFG_REG Registers

2.4.93.1 IOMUX_PRU0_GPO4_CFG_REG Register (Offset = 170h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-699. Instance Table

Instance Name	Physical Address
IOMUX	5310 0170h

Access Types Legend

Table 2-700. PR0_PRU0_GPO4_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-700. PR0_PRU0_GPO4_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.94 IOMUX_MSS_IOMUX_PR0_PRU0_GPO0_CFG_REG Registers

2.4.94.1 IOMUX_PRU0_GPO0_CFG_REG Register (Offset = 174h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-701. Instance Table

Instance Name	Physical Address
IOMUX	5310 0174h

Access Types Legend

Table 2-702. PR0_PRU0_GPO0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-702. PR0_PRU0_GPO0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.95 IOMUX_MSS_IOMUX_PR0_PRU0_GPO1_CFG_REG Registers

2.4.95.1 IOMUX_PRU0_GPO1_CFG_REG Register (Offset = 178h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-703. Instance Table

Instance Name	Physical Address
IOMUX	5310 0178h

Access Types Legend

Table 2-704. PR0_PRU0_GPO1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-704. PR0_PRU0_GPO1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.96 IOMUX_MSS_IOMUX_PR0_PRU0_GPO2_CFG_REG Registers

2.4.96.1 IOMUX_PRU0_GPO2_CFG_REG Register (Offset = 17Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-705. Instance Table

Instance Name	Physical Address
IOMUX	5310 017Ch

Access Types Legend

Table 2-706. PR0_PRU0_GPO2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-706. PR0_PRU0_GPO2_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.97 IOMUX_MSS_IOMUX_PR0_PRU0_GPO3_CFG_REG Registers

2.4.97.1 IOMUX_PRU0_GPO3_CFG_REG Register (Offset = 180h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-707. Instance Table

Instance Name	Physical Address
IOMUX	5310 0180h

Access Types Legend

Table 2-708. PR0_PRU0_GPO3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-708. PR0_PRU0_GPO3_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.98 IOMUX_MSS_IOMUX_PR0_PRU0_GPO16_CFG_REG Registers

2.4.98.1 IOMUX_PRU0_GPO16_CFG_REG Register (Offset = 184h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-709. Instance Table

Instance Name	Physical Address
IOMUX	5310 0184h

Access Types Legend

Table 2-710. PR0_PRU0_GPO16_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-710. PR0_PRU0_GPO16_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.99 IOMUX_MSS_IOMUX_PR0_PRU0_GPO15_CFG_REG Registers

2.4.99.1 IOMUX_PRU0_GPO15_CFG_REG Register (Offset = 188h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-711. Instance Table

Instance Name	Physical Address
IOMUX	5310 0188h

Access Types Legend

Table 2-712. PR0_PRU0_GPO15_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-712. PR0_PRU0_GPO15_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.100 IOMUX_MSS_IOMUX_PR0_PRU0_GPO11_CFG_REG Registers

2.4.100.1 IOMUX_PRU0_GPO11_CFG_REG Register (Offset = 18Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-713. Instance Table

Instance Name	Physical Address
IOMUX	5310 018Ch

Access Types Legend

Table 2-714. PR0_PRU0_GPO11_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-714. PR0_PRU0_GPO11_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.101 IOMUX_MSS_IOMUX_PR0_PRU0_GPO12_CFG_REG Registers

2.4.101.1 IOMUX_PRU0_GPO12_CFG_REG Register (Offset = 190h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-715. Instance Table

Instance Name	Physical Address
IOMUX	5310 0190h

Access Types Legend

Table 2-716. PR0_PRU0_GPO12_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-716. PR0_PRU0_GPO12_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.102 IOMUX_MSS_IOMUX_PR0_PRU0_GPO13_CFG_REG Registers

2.4.102.1 IOMUX_PRU0_GPO13_CFG_REG Register (Offset = 194h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-717. Instance Table

Instance Name	Physical Address
IOMUX	5310 0194h

Access Types Legend

Table 2-718. PR0_PRU0_GPO13_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-718. PR0_PRU0_GPO13_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.103 IOMUX_MSS_IOMUX_PR0_PRU0_GPO14_CFG_REG Registers

2.4.103.1 IOMUX_PRU0_GPO14_CFG_REG Register (Offset = 198h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-719. Instance Table

Instance Name	Physical Address
IOMUX	5310 0198h

Access Types Legend

Table 2-720. PR0_PRU0_GPO14_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-720. PR0_PRU0_GPO14_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.104 IOMUX_MSS_IOMUX_PR0_PRU1_GPO5_CFG_REG Registers

2.4.104.1 IOMUX_PRU1_GPO5_CFG_REG Register (Offset = 19Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-721. Instance Table

Instance Name	Physical Address
IOMUX	5310 019Ch

Access Types Legend

Table 2-722. PR0_PRU1_GPO5_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-722. PR0_PRU1_GPO5_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.105 IOMUX_MSS_IOMUX_PR0_PRU1_GPO9_CFG_REG Registers

2.4.105.1 IOMUX_PRU1_GPO9_CFG_REG Register (Offset = 1A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-723. Instance Table

Instance Name	Physical Address
IOMUX	5310 01A0h

Access Types Legend

Table 2-724. PR0_PRU1_GPO9_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-724. PR0_PRU1_GPO9_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.106 IOMUX_MSS_IOMUX_PR0_PRU1_GPO10_CFG_REG Registers

2.4.106.1 IOMUX_PRU1_GPO10_CFG_REG Register (Offset = 1A4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-725. Instance Table

Instance Name	Physical Address
IOMUX	5310 01A4h

Access Types Legend

Table 2-726. PR0_PRU1_GPO10_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-726. PR0_PRU1_GPO10_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.107 IOMUX_MSS_IOMUX_PR0_PRU1_GPO8_CFG_REG Registers

2.4.107.1 IOMUX_PRU1_GPO8_CFG_REG Register (Offset = 1A8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-727. Instance Table

Instance Name	Physical Address
IOMUX	5310 01A8h

Access Types Legend

Table 2-728. PR0_PRU1_GPO8_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-728. PR0_PRU1_GPO8_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.108 IOMUX_MSS_IOMUX_PR0_PRU1_GPO6_CFG_REG Registers

2.4.108.1 IOMUX_PRU1_GPO6_CFG_REG Register (Offset = 1ACh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-729. Instance Table

Instance Name	Physical Address
IOMUX	5310 01ACh

Access Types Legend

Table 2-730. PR0_PRU1_GPO6_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-730. PR0_PRU1_GPO6_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.109 IOMUX_MSS_IOMUX_PR0_PRU1_GPO4_CFG_REG Registers

2.4.109.1 IOMUX_PRU1_GPO4_CFG_REG Register (Offset = 1B0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-731. Instance Table

Instance Name	Physical Address
IOMUX	5310 01B0h

Access Types Legend

Table 2-732. PR0_PRU1_GPO4_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-732. PR0_PRU1_GPO4_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.110 IOMUX_MSS_IOMUX_PR0_PRU1_GPO0_CFG_REG Registers

2.4.110.1 IOMUX_PRU1_GPO0_CFG_REG Register (Offset = 1B4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-733. Instance Table

Instance Name	Physical Address
IOMUX	5310 01B4h

Access Types Legend

Table 2-734. PR0_PRU1_GPO0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-734. PR0_PRU1_GPO0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.111 IOMUX_MSS_IOMUX_PR0_PRU1_GPO1_CFG_REG Registers

2.4.111.1 IOMUX_PRU1_GPO1_CFG_REG Register (Offset = 1B8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-735. Instance Table

Instance Name	Physical Address
IOMUX	5310 01B8h

Access Types Legend

Table 2-736. PR0_PRU1_GPO1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-736. PR0_PRU1_GPO1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.112 IOMUX_MSS_IOMUX_PR0_PRU1_GPO2_CFG_REG Registers

2.4.112.1 IOMUX_PRU1_GPO2_CFG_REG Register (Offset = 1BCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-737. Instance Table

Instance Name	Physical Address
IOMUX	5310 01BCh

Access Types Legend

Table 2-738. PR0_PRU1_GPO2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-738. PR0_PRU1_GPO2_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.113 IOMUX_MSS_IOMUX_PR0_PRU1_GPO3_CFG_REG Registers

2.4.113.1 IOMUX_PRU1_GPO3_CFG_REG Register (Offset = 1C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-739. Instance Table

Instance Name	Physical Address
IOMUX	5310 01C0h

Access Types Legend

Table 2-740. PR0_PRU1_GPO3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-740. PR0_PRU1_GPO3_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.114 IOMUX_MSS_IOMUX_PR0_PRU1_GPO16_CFG_REG Registers

2.4.114.1 IOMUX_PRU1_GPO16_CFG_REG Register (Offset = 1C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-741. Instance Table

Instance Name	Physical Address
IOMUX	5310 01C4h

Access Types Legend

Table 2-742. PR0_PRU1_GPO16_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-742. PR0_PRU1_GPO16_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.115 IOMUX_MSS_IOMUX_PR0_PRU1_GPO15_CFG_REG Registers

2.4.115.1 IOMUX_PRU1_GPO15_CFG_REG Register (Offset = 1C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-743. Instance Table

Instance Name	Physical Address
IOMUX	5310 01C8h

Access Types Legend

Table 2-744. PR0_PRU1_GPO15_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-744. PR0_PRU1_GPO15_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.116 IOMUX_MSS_IOMUX_PR0_PRU1_GPO11_CFG_REG Registers

2.4.116.1 IOMUX_PRU1_GPO11_CFG_REG Register (Offset = 1CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-745. Instance Table

Instance Name	Physical Address
IOMUX	5310 01CCh

Access Types Legend

Table 2-746. PR0_PRU1_GPO11_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-746. PR0_PRU1_GPO11_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.117 IOMUX_MSS_IOMUX_PR0_PRU1_GPO12_CFG_REG Registers

2.4.117.1 IOMUX_PRU1_GPO12_CFG_REG Register (Offset = 1D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-747. Instance Table

Instance Name	Physical Address
IOMUX	5310 01D0h

Access Types Legend

Table 2-748. PR0_PRU1_GPO12_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-748. PR0_PRU1_GPO12_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.118 IOMUX_MSS_IOMUX_PR0_PRU1_GPO13_CFG_REG Registers

2.4.118.1 IOMUX_PRU1_GPO13_CFG_REG Register (Offset = 1D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-749. Instance Table

Instance Name	Physical Address
IOMUX	5310 01D4h

Access Types Legend

Table 2-750. PR0_PRU1_GPO13_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-750. PR0_PRU1_GPO13_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.119 IOMUX_MSS_IOMUX_PR0_PRU1_GPO14_CFG_REG Registers

2.4.119.1 IOMUX_PRU1_GPO14_CFG_REG Register (Offset = 1D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-751. Instance Table

Instance Name	Physical Address
IOMUX	5310 01D8h

Access Types Legend

Table 2-752. PR0_PRU1_GPO14_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-752. PR0_PRU1_GPO14_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.120 IOMUX_MSS_IOMUX_PR0_PRU1_GPO19_CFG_REG Registers

2.4.120.1 IOMUX_PRU1_GPO19_CFG_REG Register (Offset = 1DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-753. Instance Table

Instance Name	Physical Address
IOMUX	5310 01DCh

Access Types Legend

Table 2-754. PR0_PRU1_GPO19_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-754. PR0_PRU1_GPO19_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.121 IOMUX_MSS_IOMUX_PR0_PRU1_GPO18_CFG_REG Registers

2.4.121.1 IOMUX_PRU1_GPO18_CFG_REG Register (Offset = 1E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-755. Instance Table

Instance Name	Physical Address
IOMUX	5310 01E0h

Access Types Legend

Table 2-756. PR0_PRU1_GPO18_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-756. PR0_PRU1_GPO18_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.122 IOMUX_MSS_IOMUX_EXT_REFCLK0_CFG_REG Registers

2.4.122.1 IOMUX_REFCLK0_CFG_REG Register (Offset = 1E4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-757. Instance Table

Instance Name	Physical Address
IOMUX	5310 01E4h

Access Types Legend

Table 2-758. EXT_REFCLK0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-758. EXT_REFCLK0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.123 IOMUX_MSS_IOMUX_SDFM0_CLK0_CFG_REG Registers

2.4.123.1 IOMUX_CLK0_CFG_REG Register (Offset = 1E8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-759. Instance Table

Instance Name	Physical Address
IOMUX	5310 01E8h

Access Types Legend

Table 2-760. SDFM0_CLK0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip. 0: Non Inverted. 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	6Fh	Mux Mode Function Select

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2.4.124 IOMUX_MSS_IOMUX_SDFM0_D0_CFG_REG Registers

2.4.124.1 IOMUX_D0_CFG_REG Register (Offset = 1ECh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-761. Instance Table

Instance Name	Physical Address
IOMUX	5310 01ECh

Access Types Legend

Table 2-762. SDFM0_D0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-762. SDFM0_D0_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.125 IOMUX_MSS_IOMUX_SDFM0_CLK1_CFG_REG Registers

2.4.125.1 IOMUX_CLK1_CFG_REG Register (Offset = 1F0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-763. Instance Table

Instance Name	Physical Address
IOMUX	5310 01F0h

Access Types Legend

Table 2-764. SDFM0_CLK1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-764. SDFM0_CLK1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.126 IOMUX_MSS_IOMUX_SDFM0_D1_CFG_REG Registers

2.4.126.1 IOMUX_D1_CFG_REG Register (Offset = 1F4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-765. Instance Table

Instance Name	Physical Address
IOMUX	5310 01F4h

Access Types Legend

Table 2-766. SDFM0_D1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-766. SDFM0_D1_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.127 IOMUX_MSS_IOMUX_SDFM0_CLK2_CFG_REG Registers

2.4.127.1 IOMUX_CLK2_CFG_REG Register (Offset = 1F8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-767. Instance Table

Instance Name	Physical Address
IOMUX	5310 01F8h

Access Types Legend

Table 2-768. SDFM0_CLK2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-768. SDFM0_CLK2_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.128 IOMUX_MSS_IOMUX_SDFM0_D2_CFG_REG Registers

2.4.128.1 IOMUX_D2_CFG_REG Register (Offset = 1FCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-769. Instance Table

Instance Name	Physical Address
IOMUX	5310 01FCh

Access Types Legend

Table 2-770. SDFM0_D2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-770. SDFM0_D2_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.129 IOMUX_MSS_IOMUX_SDFM0_CLK3_CFG_REG Registers

2.4.129.1 IOMUX_CLK3_CFG_REG Register (Offset = 200h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-771. Instance Table

Instance Name	Physical Address
IOMUX	5310 0200h

Access Types Legend

Table 2-772. SDFM0_CLK3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-772. SDFM0_CLK3_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.130 IOMUX_MSS_IOMUX_SDFM0_D3_CFG_REG Registers

2.4.130.1 IOMUX_D3_CFG_REG Register (Offset = 204h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-773. Instance Table

Instance Name	Physical Address
IOMUX	5310 0204h

Access Types Legend

Table 2-774. SDFM0_D3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-774. SDFM0_D3_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.131 IOMUX_MSS_IOMUX_EQEP0_A_CFG_REG Registers

2.4.131.1 IOMUX_A_CFG_REG Register (Offset = 208h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-775. Instance Table

Instance Name	Physical Address
IOMUX	5310 0208h

Access Types Legend

Table 2-776. EQEP0_A_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-776. EQEP0_A_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.132 IOMUX_MSS_IOMUX_EQEP0_B_CFG_REG Registers

2.4.132.1 IOMUX_B_CFG_REG Register (Offset = 20Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-777. Instance Table

Instance Name	Physical Address
IOMUX	5310 020Ch

Access Types Legend

Table 2-778. EQEP0_B_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-778. EQEP0_B_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.133 IOMUX_MSS_IOMUX_EQEP0_STROBE_CFG_REG Registers

2.4.133.1 IOMUX_STROBE_CFG_REG Register (Offset = 210h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-779. Instance Table

Instance Name	Physical Address
IOMUX	5310 0210h

Access Types Legend

Table 2-780. EQEP0_STROBE_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-780. EQEP0_STROBE_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.134 IOMUX_MSS_IOMUX_EQEP0_INDEX_CFG_REG Registers

2.4.134.1 IOMUX_INDEX_CFG_REG Register (Offset = 214h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-781. Instance Table

Instance Name	Physical Address
IOMUX	5310 0214h

Access Types Legend

Table 2-782. EQEP0_INDEX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-782. EQEP0_INDEX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.135 IOMUX_MSS_IOMUX_I2C0_SDA_CFG_REG Registers

2.4.135.1 IOMUX_SDA_CFG_REG Register (Offset = 218h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-783. Instance Table

Instance Name	Physical Address
IOMUX	5310 0218h

Access Types Legend

Table 2-784. I2C0_SDA_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-784. I2C0_SDA_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.136 IOMUX_MSS_IOMUX_I2C0_SCL_CFG_REG Registers

2.4.136.1 IOMUX_SCL_CFG_REG Register (Offset = 21Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-785. Instance Table

Instance Name	Physical Address
IOMUX	5310 021Ch

Access Types Legend

Table 2-786. I2C0_SCL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-786. I2C0_SCL_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.137 IOMUX_MSS_IOMUX_MCAN2_TX_CFG_REG Registers

2.4.137.1 IOMUX_TX_CFG_REG Register (Offset = 220h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-787. Instance Table

Instance Name	Physical Address
IOMUX	5310 0220h

Access Types Legend

Table 2-788. MCAN2_TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-788. MCAN2_TX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.138 IOMUX_MSS_IOMUX_MCAN2_RX_CFG_REG Registers

2.4.138.1 IOMUX_RX_CFG_REG Register (Offset = 224h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-789. Instance Table

Instance Name	Physical Address
IOMUX	5310 0224h

Access Types Legend

Table 2-790. MCAN2_RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for choosing inverted version of PAD input for chip: • 0: Non Inverted • 1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for choosing input qualifier type for PAD. • 00: Sync • 01: 3 Samples • 10: 6 Samples • 11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO. • 0: GPO0 • 1: GPO1 • 2: GPO2 • 3: GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware

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Table 2-790. MCAN2_RX_CFG_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	FUNC_SEL	RW	7h	Mux Mode Function Select

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2.4.139 IOMUX_MSS_IOMUX_CLKOUT0_CFG_REG Registers

2.4.139.1 IOMUX_CFG_REG Register (Offset = 228h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-791. Instance Table

Instance Name	Physical Address
IOMUX	5310 0228h

Access Types Legend

Table 2-792. CLKOUT0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HSMASTER	RW	0h	MMR bits for HSMASTER pin incase of true I2C pads
30	HSMODE	RW	0h	MMR bits for HSMODE pin incase of true I2C pads
	RESERVED	NONE		Reserved
20	INP_INV_SEL	RW	0h	Select value for chosing inverted version of PAD input for chip:#br#0: Non Inverted#br#1: Inverted
19 - 18	QUAL_SEL	RW	0h	Select value for chosing input qualifer type for PAD.#br#00: Sync#br#01: 3 Samples#br#10: 6 Samples#br#11: Async
17 - 16	GPIO_SEL	RW	0h	R5F CPU ownership select for GPIO.#br#0:GPO0#br1:GPO1#br#2:GPO2#br#3:GPO3
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control:#br#0 : Higher slew rate#br#1: Lower slew rate
9	PUPDSEL	RW	0h	Pullup/PullDown Selection#br#0: Pull Down#br#1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable#br#0 -- Enable 1- Disable
7	OE_OVERRIDE	RW	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
3 - 0	FUNC_SEL	RW	0h	Mux Mode Function Select

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2.4.140 IOMUX_MSS_IOMUX_WARMRSTN_CFG_REG Registers

2.4.140.1 IOMUX_CFG_REG Register (Offset = 22Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-793. Instance Table

Instance Name	Physical Address
IOMUX	5310 022Ch

Access Types Legend

Table 2-794. WARMRSTN_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
	RESERVED	NONE		Reserved

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2.4.141 IOMUX_MSS_IOMUX_SAFETY_ERRORN_CFG_REG Registers

2.4.141.1 IOMUX_ERRORN_CFG_REG Register (Offset = 230h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-795. Instance Table

Instance Name	Physical Address
IOMUX	5310 0230h

Access Types Legend

Table 2-796. SAFETY_ERRORN_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control. 0: Higher slew rate. 1: Lower slew rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection. 0: Pull Down. 1: Pull Up
8	PI	RW	0h	Internal Pull Resistor Disable. 0: Enable 1:Disable
7	OE_OVERRIDE	RW	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	0h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
	RESERVED	NONE		Reserved

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2.4.142 IOMUX_MSS_IOMUX_TDI_CFG_REG Registers

2.4.142.1 IOMUX_CFG_REG Register (Offset = 234h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-797. Instance Table

Instance Name	Physical Address
IOMUX	5310 0234h

Access Types Legend

Table 2-798. TDI_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control. 0: Higher slew rate. 1: Lower slew rate
9	PUPDSEL	RW	1h	Pull Up/Pull Down Selection. 0: Pull Down. 1: Pull Up
8	PI	RW	0h	Internal Pull Resistor Disable. 0: Enable. 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
	RESERVED	NONE		Reserved

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2.4.143 IOMUX_MSS_IOMUX_TDO_CFG_REG Registers

2.4.143.1 IOMUX_CFG_REG Register (Offset = 238h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-799. Instance Table

Instance Name	Physical Address
IOMUX	5310 0238h

Access Types Legend

Table 2-800. TDO_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
	RESERVED	NONE		Reserved

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2.4.144 IOMUX_MSS_IOMUX_TMS_CFG_REG Registers

2.4.144.1 IOMUX_CFG_REG Register (Offset = 23Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-801. Instance Table

Instance Name	Physical Address
IOMUX	5310 023Ch

Access Types Legend

Table 2-802. TMS_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: • 0: Higher Slew Rate • 1: Lower Slew Rate
9	PUPDSEL	RW	0h	Pull Up/Pull Down Selection • 0: Pull Down • 1: Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable • 0: Enable • 1: Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control. Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
	RESERVED	NONE		Reserved

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2.4.145 IOMUX_MSS_IOMUX_TCK_CFG_REG Registers

2.4.145.1 IOMUX_CFG_REG Register (Offset = 240h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-803. Instance Table

Instance Name	Physical Address
IOMUX	5310 0240h

Access Types Legend

Table 2-804. TCK_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
10	SC1	RW	0h	IO Slew rate control. 0: Higher slew rate. 1: Lower slew rate
9	PUPDSEL	RW	1h	Pull Up/Pull Down Selection. 0: Pull Down. 1: Pull Up
8	PI	RW	0h	Internal Pull Resistor Disable. 0: Enable. 1: Disable
7	OE_OVERRIDE	RW	0h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	0h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	0h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
	RESERVED	NONE		Reserved

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2.4.146 IOMUX_MSS_IOMUX_QSPI0_CLKLB_CFG_REG Registers

2.4.146.1 IOMUX_CLKLB_CFG_REG Register (Offset = 244h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-805. Instance Table

Instance Name	Physical Address
IOMUX	5310 0244h

Access Types Legend

Table 2-806. QSPI0_CLKLB_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
10	SC1	RW	1h	IO Slew rate control: 0 = Higher slew rate; 1 = Lower slew rate
9	PUPDSEL	RW	0h	Pullup/PullDown Selection: 0: =Pull Down; 1 = Pull Up
8	PI	RW	1h	Internal Pull Resistor Disable: 0 = Enable; 1 = Disable
7	OE_OVERRIDE	RW	1h	Active Low Output Override
6	OE_OVERRIDE_CTRL	RW	1h	Active Low Output Override Control : Write 1 to select Active low Output Override value to control IOs OE_N/GZ instead of the control from hardware
5	IE_OVERRIDE	RW	1h	Active Low Input Override
4	IE_OVERRIDE_CTRL	RW	1h	Active Low Input Override Control : Write 1 to select Active low Input Override value to control IOs IE_N/RXACTIVE_N instead of the control from hardware
	RESERVED	NONE		Reserved

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2.4.147 IOMUX_MSS_IOMUX_QUAL_GRP_0_CFG_REG Registers

2.4.147.1 IOMUX_GRP_0_CFG_REG Register (Offset = 248h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-807. Instance Table

Instance Name	Physical Address
IOMUX	5310 0248h

Access Types Legend

Table 2-808. QUAL_GRP_0_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.148 IOMUX_MSS_IOMUX_QUAL_GRP_1_CFG_REG Registers

2.4.148.1 IOMUX_GRP_1_CFG_REG Register (Offset = 24Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-809. Instance Table

Instance Name	Physical Address
IOMUX	5310 024Ch

Access Types Legend

Table 2-810. QUAL_GRP_1_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.149 IOMUX_MSS_IOMUX_QUAL_GRP_2_CFG_REG Registers

2.4.149.1 IOMUX_GRP_2_CFG_REG Register (Offset = 250h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-811. Instance Table

Instance Name	Physical Address
IOMUX	5310 0250h

Access Types Legend

Table 2-812. QUAL_GRP_2_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.150 IOMUX_MSS_IOMUX_QUAL_GRP_3_CFG_REG Registers

2.4.150.1 IOMUX_GRP_3_CFG_REG Register (Offset = 254h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-813. Instance Table

Instance Name	Physical Address
IOMUX	5310 0254h

Access Types Legend

Table 2-814. QUAL_GRP_3_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.151 IOMUX_MSS_IOMUX_QUAL_GRP_4_CFG_REG Registers

2.4.151.1 IOMUX_GRP_4_CFG_REG Register (Offset = 258h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-815. Instance Table

Instance Name	Physical Address
IOMUX	5310 0258h

Access Types Legend

Table 2-816. QUAL_GRP_4_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.152 IOMUX_MSS_IOMUX_QUAL_GRP_5_CFG_REG Registers

2.4.152.1 IOMUX_GRP_5_CFG_REG Register (Offset = 25Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-817. Instance Table

Instance Name	Physical Address
IOMUX	5310 025Ch

Access Types Legend

Table 2-818. QUAL_GRP_5_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.153 IOMUX_MSS_IOMUX_QUAL_GRP_6_CFG_REG Registers

2.4.153.1 IOMUX_GRP_6_CFG_REG Register (Offset = 260h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-819. Instance Table

Instance Name	Physical Address
IOMUX	5310 0260h

Access Types Legend

Table 2-820. QUAL_GRP_6_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.154 IOMUX_MSS_IOMUX_QUAL_GRP_7_CFG_REG Registers

2.4.154.1 IOMUX_GRP_7_CFG_REG Register (Offset = 264h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-821. Instance Table

Instance Name	Physical Address
IOMUX	5310 0264h

Access Types Legend

Table 2-822. QUAL_GRP_7_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.155 IOMUX_MSS_IOMUX_QUAL_GRP_8_CFG_REG Registers

2.4.155.1 IOMUX_GRP_8_CFG_REG Register (Offset = 268h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-823. Instance Table

Instance Name	Physical Address
IOMUX	5310 0268h

Access Types Legend

Table 2-824. QUAL_GRP_8_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.156 IOMUX_MSS_IOMUX_QUAL_GRP_9_CFG_REG Registers

2.4.156.1 IOMUX_GRP_9_CFG_REG Register (Offset = 26Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-825. Instance Table

Instance Name	Physical Address
IOMUX	5310 026Ch

Access Types Legend

Table 2-826. QUAL_GRP_9_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.157 IOMUX_MSS_IOMUX_QUAL_GRP_10_CFG_REG Registers

2.4.157.1 IOMUX_GRP_10_CFG_REG Register (Offset = 270h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-827. Instance Table

Instance Name	Physical Address
IOMUX	5310 0270h

Access Types Legend

Table 2-828. QUAL_GRP_10_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.158 IOMUX_MSS_IOMUX_QUAL_GRP_11_CFG_REG Registers

2.4.158.1 IOMUX_GRP_11_CFG_REG Register (Offset = 274h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-829. Instance Table

Instance Name	Physical Address
IOMUX	5310 0274h

Access Types Legend

Table 2-830. QUAL_GRP_11_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.159 IOMUX_MSS_IOMUX_QUAL_GRP_12_CFG_REG Registers

2.4.159.1 IOMUX_GRP_12_CFG_REG Register (Offset = 278h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-831. Instance Table

Instance Name	Physical Address
IOMUX	5310 0278h

Access Types Legend

Table 2-832. QUAL_GRP_12_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.160 IOMUX_MSS_IOMUX_QUAL_GRP_13_CFG_REG Registers

2.4.160.1 IOMUX_GRP_13_CFG_REG Register (Offset = 27Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-833. Instance Table

Instance Name	Physical Address
IOMUX	5310 027Ch

Access Types Legend

Table 2-834. QUAL_GRP_13_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.161 IOMUX_MSS_IOMUX_QUAL_GRP_14_CFG_REG Registers

2.4.161.1 IOMUX_GRP_14_CFG_REG Register (Offset = 280h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-835. Instance Table

Instance Name	Physical Address
IOMUX	5310 0280h

Access Types Legend

Table 2-836. QUAL_GRP_14_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.162 IOMUX_MSS_IOMUX_QUAL_GRP_15_CFG_REG Registers

2.4.162.1 IOMUX_GRP_15_CFG_REG Register (Offset = 284h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-837. Instance Table

Instance Name	Physical Address
IOMUX	5310 0284h

Access Types Legend

Table 2-838. QUAL_GRP_15_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.163 IOMUX_MSS_IOMUX_QUAL_GRP_16_CFG_REG Registers

2.4.163.1 IOMUX_GRP_16_CFG_REG Register (Offset = 288h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-839. Instance Table

Instance Name	Physical Address
IOMUX	5310 0288h

Access Types Legend

Table 2-840. QUAL_GRP_16_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.164 IOMUX_MSS_IOMUX_QUAL_GRP_17_CFG_REG Registers

2.4.164.1 IOMUX_GRP_17_CFG_REG Register (Offset = 28Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-841. Instance Table

Instance Name	Physical Address
IOMUX	5310 028Ch

Access Types Legend

Table 2-842. QUAL_GRP_17_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	RO		Reserved
	RESERVED	NONE		Reserved
7 - 0	QUAL_PERIOD_PER_SAMPLE	RW	0h	MMR bits for programming the qualifier clock count per sample

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2.4.165 IOMUX_MSS_IOMUX_USER_MODE_EN Registers

2.4.165.1 IOMUX_MODE_EN Register (Offset = 290h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-843. Instance Table

Instance Name	Physical Address
IOMUX	5310 0290h

Access Types Legend

Table 2-844. USER_MODE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	USER_MODE_EN	RW	0h	Write 0XADADADAD to enable user mode write access to IO CFG space

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2.4.166 IOMUX_MSS_IOMUX_PADGLBL_CFG_REG Registers

2.4.166.1 IOMUX_CFG_REG Register (Offset = 294h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-845. Instance Table

Instance Name	Physical Address
IOMUX	5310 0294h

Access Types Legend

Table 2-846. PADGLBL_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PADGLBL_CFG_REG	RW	0h	2:0 : global_ie_n_ctl - Write 3'b111 to pass global_ie_n_val to IE_N/RXACTIVE_N pin of all the IOs.3 : global_ie_n_val - Active low10:8 : global_oe_n_ctl - Write 3'b111 to pass global_oe_n_val to OE_N/GZ pin of all the IOs.11 : global_oe_n_val - Active low18:16 : global_pi_ctl - Write 3'b111 to pass global_pi_val and global_pu_val to all the IOs19 : global_pi_val20 : global_pu_val

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2.4.167 IOMUX_MSS_IOMUX_IO_CFG_KICK0 Registers

2.4.167.1 IOMUX_CFG_KICK0 Register (Offset = 298h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-847. Instance Table

Instance Name	Physical Address
IOMUX	5310 0298h

Access Types Legend

Table 2-848. IO_CFG_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	IO_CFG_KICK0	RW	0h	Kicker 0 Register. The value 83E7 0B13h must be written to KICK0 as part of the process to unlock the CPU.write access to the above PIN MUX registers (including IOCFGKICK1)

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2.4.168 IOMUX_MSS_IOMUX_IO_CFG_KICK1 Registers

2.4.168.1 IOMUX_CFG_KICK1 Register (Offset = 29Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-849. Instance Table

Instance Name	Physical Address
IOMUX	5310 029Ch

Access Types Legend

Table 2-850. IO_CFG_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	IO_CFG_KICK1	RW	A7D8C1h	Kicker 1 Register. The value 95A4 F1E0h must be written to the KICK1 as part of the process to unlock the CPU write access to above PINMUX registers (excluding IOCFGKICK0). IOCFGKICK0 has to be written with 83E70B13h to enable access to IOCFGKICK1.

2.4.169 Access Table

Table 2-851. Access Type Codes

Access Type	Code	Description
RW	RW	Read / Write
RO	RO	Read

2.5 MSS_TOPRCM Registers

Table 2-852. MSS_TOP_RCM Registers Base Address Table

Offset	Length	Acronym	Register Name	MSS_TOP_RCM Physical Address
0h	32	MSS_TOPRCM_PID	PID register	5320 0000h
4h	32	MSS_TOPRCM_WARM_RESET_CONFIG	RW	5320 0004h
8h	8	MSS_TOPRCM_WARM_RESET_REQ	RW	5320 0008h
Ch	16	MSS_TOPRCM_WARM_RST_CAUSE	RO	5320 000Ch
10h	8	MSS_TOPRCM_WARM_RST_CAUSE_CLR	RW	5320 0010h
14h	8	MSS_TOPRCM_RCOSC32K_CTRL	RW	5320 0014h
18h	16	MSS_TOPRCM_LIMP_MODE_EN	RW	5320 0018h
1Ch	8	MSS_TOPRCM_PLL_REF_CLK_SRC_SEL	RW	5320 001Ch
20h	8	MSS_TOPRCM_PAD_XTAL_CTRL	RW	5320 0020h
24h	32	MSS_TOPRCM_SOP_MODE_VALUE	RO	5320 0024h
28h	8	MSS_TOPRCM_CLK_LOSS_STATUS	RO	5320 0028h
30h	16	MSS_TOPRCM_WARM_RSTTIME1	RW	5320 0030h
34h	16	MSS_TOPRCM_WARM_RSTTIME2	RW	5320 0034h
38h	16	MSS_TOPRCM_WARM_RSTTIME3	RW	5320 0038h
400h	8	MSS_TOPRCM_PLL_CORE_PWRCTRL	RW	5320 0400h
404h	32	MSS_TOPRCM_PLL_CORE_CLKCTRL	RW	5320 0404h
408h	0	MSS_TOPRCM_PLL_CORE_TENABLE	RW	5320 0408h
40Ch	0	MSS_TOPRCM_PLL_CORE_TENABLEDIV	RW	5320 040Ch
410h	24	MSS_TOPRCM_PLL_CORE_M2NDIV	RW	5320 0410h
414h	24	MSS_TOPRCM_PLL_CORE_MN2DIV	RW	5320 0414h

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Table 2-852. MSS_TOP_RCM Registers Base Address Table (continued)

Offset	Length	Acronym	Register Name	MSS_TOP_RCM Physical Address
418h	32	MSS_TOPRCM_PLL_CORE_FRACDIV	RW	5320 0418h
41Ch	8	MSS_TOPRCM_PLL_CORE_BWCTRL	RW	5320 041Ch
420h	32	MSS_TOPRCM_PLL_CORE_FRACCTRL	RW	5320 0420h
424h	32	MSS_TOPRCM_PLL_CORE_STATUS	RO	5320 0424h
428h	24	MSS_TOPRCM_PLL_CORE_HSDIVIDER	RW	5320 0428h
42Ch	16	MSS_TOPRCM_PLL_CORE_HSDIVIDER_CLKOUT0	RW	5320 042Ch
430h	16	MSS_TOPRCM_PLL_CORE_HSDIVIDER_CLKOUT1	RW	5320 0430h
434h	16	MSS_TOPRCM_PLL_CORE_HSDIVIDER_CLKOUT2	RW	5320 0434h
43Ch	8	MSS_TOPRCM_PLL_CORE_RSTCTRL	RW	5320 043Ch
440h	8	MSS_TOPRCM_PLL_CORE_HSDIVIDER_RSTCTRL	RW	5320 0440h
500h	16	MSS_TOPRCM_R5SS_CLK_SRC_SEL	RW	5320 0500h
504h	8	MSS_TOPRCM_R5SS_CLK_STATUS	RO	5320 0504h
510h	8	MSS_TOPRCM_R5SS0_CLK_DIV_SEL	RW	5320 0510h
514h	8	MSS_TOPRCM_R5SS1_CLK_DIV_SEL	RW	5320 0514h
518h	8	MSS_TOPRCM_R5SS0_CLK_GATE	RW	5320 0518h
51Ch	8	MSS_TOPRCM_R5SS1_CLK_GATE	RW	5320 051Ch
520h	16	MSS_TOPRCM_SYS_CLK_DIV_VAL	RW	5320 0520h
524h	8	MSS_TOPRCM_SYS_CLK_GATE	RW	5320 0524h
528h	16	MSS_TOPRCM_SYS_CLK_STATUS	RO	5320 0528h
800h	8	MSS_TOPRCM_PLL_PER_PWRCTRL	RW	5320 0800h
804h	32	MSS_TOPRCM_PLL_PER_CLKCTRL	RW	5320 0804h
808h	0	MSS_TOPRCM_PLL_PER_TENABLE	RW	5320 0808h
80Ch	0	MSS_TOPRCM_PLL_PER_TENABLEDIV	RW	5320 080Ch
810h	24	MSS_TOPRCM_PLL_PER_M2NDIV	RW	5320 0810h
814h	24	MSS_TOPRCM_PLL_PER_MN2DIV	RW	5320 0814h
818h	32	MSS_TOPRCM_PLL_PER_FRACDIV	RW	5320 0818h
81Ch	8	MSS_TOPRCM_PLL_PER_BWCTRL	RW	5320 081Ch
820h	32	MSS_TOPRCM_PLL_PER_FRACCTRL	RW	5320 0820h
824h	32	MSS_TOPRCM_PLL_PER_STATUS	RO	5320 0824h
828h	24	MSS_TOPRCM_PLL_PER_HSDIVIDER	RW	5320 0828h
82Ch	16	MSS_TOPRCM_PLL_PER_HSDIVIDER_CLKOUT0	RW	5320 082Ch
830h	16	MSS_TOPRCM_PLL_PER_HSDIVIDER_CLKOUT1	RW	5320 0830h
83Ch	8	MSS_TOPRCM_PLL_PER_RSTCTRL	RW	5320 083Ch
840h	8	MSS_TOPRCM_PLL_PER_HSDIVIDER_RSTCTRL	RW	5320 0840h
C00h	16	MSS_TOPRCM_CLKOUT0_CLK_SRC_SEL	RW	5320 0C00h
C04h	16	MSS_TOPRCM_CLKOUT1_CLK_SRC_SEL	RW	5320 0C04h
C08h	16	MSS_TOPRCM_CLKOUT0_DIV_VAL	RW	5320 0C08h
C0Ch	16	MSS_TOPRCM_CLKOUT1_DIV_VAL	RW	5320 0C0Ch
C10h	8	MSS_TOPRCM_CLKOUT0_CLK_GATE	RW	5320 0C10h
C14h	8	MSS_TOPRCM_CLKOUT1_CLK_GATE	RW	5320 0C14h
C18h	16	MSS_TOPRCM_CLKOUT0_CLK_STATUS	RO	5320 0C18h

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Table 2-852. MSS_TOP_RCM Registers Base Address Table (continued)

Offset	Length	Acronym	Register Name	MSS_TOP_RCM Physical Address
C1Ch	16	MSS_TOPRCM_CLKOUT1_CLK_STATUS	RO	5320 0C1Ch
C20h	16	MSS_TOPRCM_TRCCLKOUT_CLK_SRC_SEL	RW	5320 0C20h
C24h	16	MSS_TOPRCM_TRCCLKOUT_DIV_VAL	RW	5320 0C24h
C28h	8	MSS_TOPRCM_TRCCLKOUT_CLK_GATE	RW	5320 0C28h
C2Ch	16	MSS_TOPRCM_TRCCLKOUT_CLK_STATUS	RO	5320 0C2Ch
D00h	32	MSS_TOPRCM_DFT_DMLED_EXEC	RW	5320 0D00h
D04h	32	MSS_TOPRCM_DFT_DMLED_STATUS	RW	5320 0D04h
E00h	32	MSS_TOPRCM_HW_REG0	RW	5320 0E00h
E04h	32	MSS_TOPRCM_HW_REG1	RW	5320 0E04h
E08h	32	MSS_TOPRCM_HW_REG2	RW	5320 0E08h
E0Ch	32	MSS_TOPRCM_HW_REG3	RW	5320 0E0Ch
FD0h	32	MSS_TOPRCM_HW_SPARE_RW0	RW	5320 0FD0h
FD4h	32	MSS_TOPRCM_HW_SPARE_RW1	RW	5320 0FD4h
FD8h	32	MSS_TOPRCM_HW_SPARE_RW2	RW	5320 0FD8h
FDCh	32	MSS_TOPRCM_HW_SPARE_RW3	RW	5320 0FDCh
FE0h	32	MSS_TOPRCM_HW_SPARE_RO0	RO	5320 0FE0h
FE4h	32	MSS_TOPRCM_HW_SPARE_RO1	RO	5320 0FE4h
FE8h	32	MSS_TOPRCM_HW_SPARE_RO2	RO	5320 0FE8h
FECh	32	MSS_TOPRCM_HW_SPARE_RO3	RO	5320 0FECh
FF0h	32	MSS_TOPRCM_HW_SPARE_WPH	RW	5320 0FF0h
FF4h	32	MSS_TOPRCM_HW_SPARE_REC	RW	5320 0FF4h
1008h	32	MSS_TOPRCM_LOCK0_KICK0	- KICK0 component	5320 1008h
100Ch	32	MSS_TOPRCM_LOCK0_KICK1	- KICK1 component	5320 100Ch
1010h	8	MSS_TOPRCM_INTR_RAW_STATUS	Interrupt Raw Status/Set Register	5320 1010h
1014h	8	MSS_TOPRCM_INTR_ENABLED_STATUS_CLEAR	Interrupt Enabled Status/Clear register	5320 1014h
1018h	8	MSS_TOPRCM_INTR_ENABLE	Interrupt Enable register	5320 1018h
101Ch	8	MSS_TOPRCM_INTR_ENABLE_CLEAR	Interrupt Enable Clear register	5320 101Ch
1020h	8	MSS_TOPRCM_EOI	EOI register	5320 1020h
1024h	32	MSS_TOPRCM_FAULT_ADDRESS	Fault Address register	5320 1024h
1028h	8	MSS_TOPRCM_FAULT_TYPE_STATUS	Fault Type Status register	5320 1028h
102Ch	32	MSS_TOPRCM_FAULT_ATTR_STATUS	Fault Attribute Status register	5320 102Ch
1030h	0	MSS_TOPRCM_FAULT_CLEAR	Fault Clear register	5320 1030h

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2.5.1 TOP_RCM_MSS_TOPRCM_PID Registers

2.5.1.1 TOP_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

Return to Summary Table

Table 2-853. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0000h

Access Types Legend

Table 2-854. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	640B657B5780h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	Ah	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	2774h	Not Defined

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2.5.2 TOP_RCM_MSS_TOPRCM_WARM_RESET_CONFIG Registers

2.5.2.1 TOP_WARM_RESET_CONFIG Register (Offset = 4h) [reset = h]

Short Description: Warm Reset Configuration Register

Long Description: Register allows user to configure warm reset options.

Return to Summary Table

Table 2-855. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0004h

Access Types Legend

Table 2-856. WARM_RESET_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
30 - 28	WDOG3_RST_EN	RW	7h	Data should be loaded as multibit. Write 3'b000 to disable corresponding Watchdog control on Warm reset Write 3'b111 enable corresponding Watchdog to control Warm reset
	RESERVED	NONE		Reserved
26 - 24	WDOG2_RST_EN	RW	7h	Data should be loaded as multibit. Write 3'b000 to disable corresponding Watchdog control on Warm reset Write 3'b111 enable corresponding Watchdog to control Warm reset
	RESERVED	NONE		Reserved
22 - 20	WDOG1_RST_EN	RW	7h	Data should be loaded as multibit. Write 3'b000 to disable corresponding Watchdog control on Warm reset Write 3'b111 enable corresponding Watchdog to control Warm reset
	RESERVED	NONE		Reserved
18 - 16	WDOG0_RST_EN	RW	7h	Data should be loaded as multibit. Write 3'b000 to disable corresponding Watchdog control on Warm reset Write 3'b111 enable corresponding Watchdog to control Warm reset
	RESERVED	NONE		Reserved
6 - 4	DEBUGSS_RST_EN	RW	7h	Data should be loaded as multibit. Write 3'b000 to disable debugger control on Warm reset Write 3'b111 enable debugger to control Warm reset
	RESERVED	NONE		Reserved
2 - 0	PAD_BYPASS	RW	7h	Bypass the Warm Reset from Pad Input Data should be loaded as multibit. Write 3'b000 : Warm Reset pin has control over warm reset Write 3'b111 : Warm Reset pin has no control on warm reset

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2.5.3 TOP_RCM_MSS_TOPRCM_WARM_RESET_REQ Registers

2.5.3.1 TOP_WARM_RESET_REQ Register (Offset = 8h) [reset = h]

Short Description: Software Warm Reset Request Register

Long Description: This register allows the application software to request a warm reset.

Return to Summary Table

Table 2-857. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0008h

Access Types Legend

Table 2-858. WARM_RESET_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SW_RST	RW	7h	Data should be loaded as multibit. Write 3'b000 to assert warm reset from SW Write 3'b111 to deassert warm reset from SW (if this is the only source of warm reset)

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2.5.4 MSS_TOPRCM_WARM_RST_CAUSE Registers

2.5.4.1 TOPRCM_WARM_RST_CAUSE Register (Offset = Ch) [reset = h]

Short Description: Warm Reset Source Register

Long Description: Captures Reason for Warm and Power-On Resets

Return to Summary Table

Table 2-859. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 000Ch

Access Types Legend

Table 2-860. WARM_RST_CAUSE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CAUSE	RO	F4241h	System Reset Cause register: 12'b 0000_0100_0001 - POR reset (PORz) 12'b 0000_0100_0010 - Warm reset caused by MSS_WDT0 12'b 0000_0100_0100 - Warm reset caused by MSS_WDT1 12'b 0000_0100_1000 - Warm reset caused by MSS_WDT2 12'b 0000_0101_0000 - Warm reset caused by MSS_WDT3 12'b 0000_0110_0000 - Warm reset caused by TOP_RMC:WARM_RESET_REQ 12'b 0000_0100_0000 - External Warm Reset Request (RESETn) 12'b 0000_1100_0000 - Warm reset caused by HSM_WDT 12'b 0001_0100_0000 - Warm Reset caused by DEBUGSS

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2.5.5 TOP_RCM_MSS_TOPRCM_WARM_RST_CAUSE_CLR Registers

2.5.5.1 TOP_WARM_RST_CAUSE_CLR Register (Offset = 10h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-861. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0010h

Access Types Legend

Table 2-862. WARM_RST_CAUSE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLEAR	RW	0h	Write pulse bit field: Data should be loaded as multibit. 3'b111: System Reset Cause Register Clear

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2.5.6 TOP_RCM_MSS_TOPRCM_RCOSC32K_CTRL Registers

2.5.6.1 TOP_RCOSC32K_CTRL Register (Offset = 14h) [reset = h]

Short Description: 32 KHz RC Oscillator Control Register

Long Description: This register allows the user to configure the on-chip 32 KHz RC Oscillator.

Return to Summary Table

Table 2-863. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0014h

Access Types Legend

Table 2-864. RCOSC32K_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	STOPOSC	RW	0h	32 KHz RCOSC Clock Stop Bit 3'b111: Stop 32 KHz RCOSC clock

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2.5.7 TOP_RCM_MSS_TOPRCM_LIMP_MODE_EN Registers

2.5.7.1 TOP_LIMP_MODE_EN Register (Offset = 18h) [reset = h]

Short Description: Limp Mode Enable Register

Long Description: This register allows the user to configure the clock loss triggers for enabling Limp Mode operation.

Return to Summary Table

Table 2-865. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0018h

Access Types Legend

Table 2-866. LIMP_MODE_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 8	COREPLL_LOSS_EN	RW	0h	Enable for core pll phase lock loss to generate Limp mode 3'b111: PLL Lock loss will generate Limp mode (multibit 111) 3'b000: PLL Lock loss will **not** generate Limp mode (multibit 000)
	RESERVED	NONE		Reserved
6 - 4	XTALCLK_LOSS_EN	RW	0h	Enable for crystal_clock_loss to generate Limp mode 3'b111: XTAL clock loss will generate Limp mode (multibit 111) 3'b000: XTAL clock loss will **not** generate Limp mode (multibit 000)
	RESERVED	NONE		Reserved
2 - 0	DCC0_ERROR_EN	RW	0h	Enable DCC0 Error to generate Limp mode 3'b111: DCC0 Error will generate Limp mode (multibit 111) 3'b000: DCC0 Error will **not** generate Limp mode (multibit 000)

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2.5.8 TOP_RCM_MSS_TOPRCM_PLL_REF_CLK_SRC_SEL Registers

2.5.8.1 TOP_PLL_REF_CLK_SRC_SEL Register (Offset = 1Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-867. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 001Ch

Access Types Legend

Table 2-868. PLL_REF_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6 - 4	PLL_PERI_REF_CLK_SRC_SEL	RW	0h	Mux selct for PERI PLL REF clockWrite 3'b111 : to select external reference clock as PLL reference clockWrite 3'b000 : to select on-die clock as PLL reference clock
	RESERVED	NONE		Reserved
2 - 0	PLL_CORE_REF_CLK_SRC_SEL	RW	0h	Mux selct for CORE PLL REF clockWrite 3'b111 : to select external reference clock as PLL reference clockWrite 3'b000 : to select on-die clock as PLL reference clock

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2.5.9 TOP_RCM_MSS_TOPRCM_PAD_XTAL_CTRL Registers

2.5.9.1 TOP_PAD_XTAL_CTRL Register (Offset = 20h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-869. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0020h

Access Types Legend

Table 2-870. PAD_XTAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	XTAL_XI_OE_N	RW	0h	When gz is low, the padxo output is enabled, padxi to padxo is a single stage inverter, and the oscillator can oscillate with an external crystal plus capacitors/resistor. When gz is high, padxo is in high impedance mode, padxi and Y are driven low, and the oscillator is disabled. With gz high, the internal bias resistor between padxi and padxo is disconnected regardless of the state of resselect.
2	XTAL_XO_RESSELECT	RW	0h	When resselect is low, an internal 1Meg Ohm resistor is connected between padxi and padxo for oscillator bias. When resselect is asserted (high), the internal resistor is disconnected. For oscillation with a crystal while resselect is high, an external resistor must be connected between padxi and padxo to provide bias.
1	XTAL_XO_SW2	RW	0h	XTAL pad control bit frequency selection pin SW2 Based on table belowsw2 sw1 Freq of operation0 0 5 20 MHz0 1 15 35 MHz1 0 30 40 MHz1 1 40 55 MHz
0	XTAL_XO_SW1	RW	1h	XTAL pad control bit frequency selection pin SW1 Based on table belowsw2 sw1 Freq of operation0 0 5 20 MHz0 1 15 35 MHz1 0 30 40 MHz1 1 40 55 MHz

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2.5.10 TOP_RCM_MSS_TOPRCM_SOP_MODE_VALUE Registers

2.5.10.1 TOP_SOP_MODE_VALUE Register (Offset = 24h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-871. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0024h

Access Types Legend

Table 2-872. SOP_MODE_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RO	0h	0000: QSPI Functional mode(4S) 0001 UART Functional mode 0010 QSPI Functional mode(1S) 0100: QSPI Functional mode(4S) (UART Backup) 0101: QSPI Functional mode(1S) (UART Backup) 1011: DevBoot mode All other values unsupported. Reset value of MMR is 0 but will latch the SOP pin values after PORz is released. When CPU reads the MMR it will show the latched SOP mode value.

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2.5.11 TOP_RCM_MSS_TOPRCM_CLK_LOSS_STATUS Registers

2.5.11.1 TOP_CLK_LOSS_STATUS Register (Offset = 28h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-873. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0028h

Access Types Legend

Table 2-874. CLK_LOSS_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
8	RC_GOOD_BOOT	RO	1h	Clock status of RC clock at boot. Reset value will reflect the actual status1 --> clock present at boot0 --> clock not present at boot
	RESERVED	NONE		Reserved
4	RC_CLOCK_LOSS	RO	0h	Coarse detection clock loss status for RC clock. Reset value will reflect the actual status1 --> clock lost0 --> clock good
	RESERVED	NONE		Reserved
0	CRYSTAL_CLOCK_LOSS	RO	0h	Coarse detection clock loss status for Crystal clock. Reset value will reflect the actual status1 --> clock lost0 --> clock good

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2.5.12 TOP_RCM_MSS_TOPRCM_WARM_RSTTIME1 Registers

2.5.12.1 TOP_WARM_RSTTIME1 Register (Offset = 30h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-875. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0030h

Access Types Legend

Table 2-876. WARM_RSTTIME1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	DELAY	RW	888h	programing Output delay Data should be loaded as multibit. For example: if value of 0x5 should be selected then 0x555 should be configured to the register.

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2.5.13 TOP_RCM_MSS_TOPRCM_WARM_RSTTIME2 Registers

2.5.13.1 TOP_WARM_RSTTIME2 Register (Offset = 34h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-877. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0034h

Access Types Legend

Table 2-878. WARM_RSTTIME2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	DELAY	RW	888h	programing input Rise delay Data should be loaded as multibit. For example: if value of 0x5 should be selected then 0x555 should be configured to the register.

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2.5.14 TOP_RCM_MSS_TOPRCM_WARM_RSTTIME3 Registers

2.5.14.1 TOP_WARM_RSTTIME3 Register (Offset = 38h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-879. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0038h

Access Types Legend

Table 2-880. WARM_RSTTIME3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	DELAY	RW	111h	programing Input Fall delay Data should be loaded as multibit. For example: if value of 0x5 should be selected then 0x555 should be configured to the register.

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2.5.15 TOP_RCM_MSS_TOPRCM_PLL_CORE_PWRCTRL Registers

2.5.15.1 TOP_PLL_CORE_PWRCTRL Register (Offset = 400h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-881. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0400h

Access Types Legend

Table 2-882. PLL_CORE_PWRCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
5	PONIN	RW	1h	ON/OFF control of the weak power switch digital. For functionalmode it should be 1
4	PGOODIN	RW	1h	ON/OFF control of the strong power switch digital. For functional mode it should be 1
3	RET	RW	0h	Save/Restore control for Retention mode. For functional mode itshould be 0
2	ISORET	RW	0h	Save/Restore control for Isolation of output pins For functional modeit should be 0
1	ISOSCAN	RW	0h	Save/Restore control for Isolation of the Scanout pins. For functionalmode it should be 0
0	OFFMODE	RW	0h	Used to switch OFF the logic on VDDA. For functional mode itshould be 0

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2.5.16 TOP_RCM_MSS_TOPRCM_PLL_CORE_CLKCTRL Registers

2.5.16.1 TOP_PLL_CORE_CLKCTRL Register (Offset = 404h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-883. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0404h

Access Types Legend

Table 2-884. PLL_CORE_CLKCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CYCLESLIPEN	RW	0h	FailSafe enable to trigger re-calibration in case CycleSlip occurs between REFCLK and FBCLK.
30	ENSSC	RW	0h	Controls Clock Spreading. SSC is not supported. Should be set to 0x0 to disable clock spreading.
29	CLKDCOLDOEN	RW	0h	Synchronously enables/disables CLKDCOLDO0x0 : synchronously disables CLKDCOLDO0x1 : synchronously enables CLKDCOLDO
	RESERVED	NONE		Reserved
23	IDLE	RW	1h	Sets PLL to Idle mode0x0 : When SYSRESET = 0 and TINITZ = 1 IDLE = 0 PLL will go toActive and Locked0x1 : When SYSRESET = 0 and TINITZ = 1 IDLE = 1 PLL will go toIdle Bypass low powe
22	BYPASSACKZ	RW	0h	BYPASSACKZ is a special purpose input to the module. In generalthis input is expected to be tied to static low. For the output clocks ofthe module that do not have an internal bypass mux viz.CLKDCOLDO and CLKOUTLDO, a bypass mux could beimplemented external to the module.
21	STBYRET	RW	0h	Standby retention control0x0 : prepares ADPLLLJ for relock when out of retention byremoving the gating on all internal clocks.0x1 : prepares ADPLLLJ for retention by gating all the internalclocks.
20	CLKOUTEN	RW	0h	CLKOUT enable or disable0x0 : synchronously disables CLKOUT0x1 : synchronously enables CLKOUT
19	CLKOUTLDOEN	RW	1h	Synchronously enables/disables CLKOUTLDO 0x0 : synchronously disables CLKOUTLDO 0x1 : synchronously enables CLKOUTLDO
18	ULOWCLKEN	RW	0h	Select CLKOUT source in bypass0x0: When ADPLLLJ in bypass mode, CLKOUT = CLKINP/(N2+1)0x1: When ADPLLLJ in bypass mode, CLKOUT = CLKINPULOW.
17	CLKDCOLDOPWDNZ	RW	0h	0 Asynchronous power down for CLKDCOLDO o/p.
16	M2PWDNZ	RW	1h	M2 divider power down mode0x0: Asynchronous power down for M2 divider0x1 : M2 divider is functional
	RESERVED	NONE		Reserved
14	STOPMODE	RW	1h	When in Lossclk/Stbyret 0x0 : Limp mode 0x1 : Stopmode
	RESERVED	NONE		Reserved
12 - 10	SELFREQDCO	RW	64h	DCO Clock (DCOCLK = CLKINP * [M/(N+1)]) frequency rangeselector.0x0: Reserved0x2: HS2 : DCOCLK range is from 500 MHz to 1000 MHz0x3: Reserved0x4: HS1: DCOCLK range is from 1000 MHz to 2000 MHz0x5: Reserved
	RESERVED	NONE		Reserved
8	RELAXED_LOCK	RW	0h	Decides when FREQLOCK asserted0x0: FREQLOCK asserted when DC frequency error less than 1%0x1: FREQLOCK asserted when DC frequency error less than 2%
	RESERVED	NONE		Reserved
1	SSCTYPE	RW	0h	SSC Type

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Table 2-884. PLL_CORE_CLKCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TINTZ	RW	0h	PLL core soft reset

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2.5.17 TOP_RCM_MSS_TOPRCM_PLL_CORE_TENABLE Registers

2.5.17.1 TOP_PLL_CORE_TENABLE Register (Offset = 408h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-885. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0408h

Access Types Legend

Table 2-886. PLL_CORE_TENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
0	TENABLE	RW	0h	M, N. SD and SELFREQDCO latch (active rise edge)

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2.5.18 TOP_RCM_MSS_TOPRCM_PLL_CORE_TENABLEDIV Registers

2.5.18.1 TOP_PLL_CORE_TENABLEDIV Register (Offset = 40Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-887. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 040Ch

Access Types Legend

Table 2-888. PLL_CORE_TENABLEDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
0	TENABLEDIV	RW	0h	M2 and N2 latch (active rise edge)

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2.5.19 TOP_RCM_MSS_TOPRCM_PLL_CORE_M2NDIV Registers

2.5.19.1 TOP_PLL_CORE_M2NDIV Register (Offset = 410h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-889. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0410h

Access Types Legend

Table 2-890. PLL_CORE_M2NDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 16	M2	RW	640h	Post-divider is REGM2
	RESERVED	NONE		Reserved
7 - 0	N	RW	13h	Pre-divider is REGN+1

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2.5.20 TOP_RCM_MSS_TOPRCM_PLL_CORE_MN2DIV Registers

2.5.20.1 TOP_PLL_CORE_MN2DIV Register (Offset = 414h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-891. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0414h

Access Types Legend

Table 2-892. PLL_CORE_MN2DIV Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 16	N2	RW	0h	Bypass divider is REGN2+1
	RESERVED	NONE		Reserved
11 - 0	M	RW	28FB5F040h	Feedback Multiplier is REGM

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2.5.21 TOP_RCM_MSS_TOPRCM_PLL_CORE_FRACDIV Registers

2.5.21.1 TOP_PLL_CORE_FRACDIV Register (Offset = 418h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-893. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0418h

Access Types Legend

Table 2-894. PLL_CORE_FRACDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	REGSD	RW	3E8h	Sigma-Delta DividerShould be set by s/w to provide optimum jitter performance.DPLL_SD_DIV = CEILING ([DPLL_MULT/ (DPLL_DIV+1)] * CLKINP/ 250), where CLKINP is the input clock of the DPLL in MHz
	RESERVED	NONE		Reserved
17 - 0	FRACTIONALM	RW	0h	Fractional part of the M divider.

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2.5.22 TOP_RCM_MSS_TOPRCM_PLL_CORE_BWCTRL Registers

2.5.22.1 TOP_PLL_CORE_BWCTRL Register (Offset = 41Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-895. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 041Ch

Access Types Legend

Table 2-896. PLL_CORE_BWCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 1	BWCONTROL	RW	0h	Change Loop Bandwidth
0	BW_INCR_DECRZ	RW	0h	Direction of Loop Bandwidth0x0 : decrease BW0x1 : increase BW

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2.5.23 TOP_RCM_MSS_TOPRCM_PLL_CORE_FRACCTRL Registers

2.5.23.1 TOP_PLL_CORE_FRACCTRL Register (Offset = 420h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-897. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0420h

Access Types Legend

Table 2-898. PLL_CORE_FRACCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DOWNSPREAD	RW	0h	Controls frequency spread0x0 : enables both side frequency spread about the programmed frequency.0x1 : enables low frequency spread only
30 - 28	MODFREQDIVIDEREXPONENT	RW	0h	Exponent of the REFCLK divider to define the modulation frequency.
27 - 21	MODFREQDIVIDERMANTISSA	RW	0h	Mantissa of the REFCLK divider to define the modulation frequency
20 - 18	DELTAMSTEPINTEGER	RW	0h	Integer part of Frequency Spread control
17 - 0	DELTAMSTEPFRACTION	RW	0h	The fraction part of Frequency Spread control

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2.5.24 TOP_RCM_MSS_TOPRCM_PLL_CORE_STATUS Registers

2.5.24.1 TOP_PLL_CORE_STATUS Register (Offset = 424h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-899. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0424h

Access Types Legend

Table 2-900. PLL_CORE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PONOUT	RO	1h	Status of the weak power-switch0x0 : indicates the/OFF status of the weak power-switch in digital toSOC.0x1 : ndicates the ON status of the weak power-switch in digital toSOC.
30	PGOODOUT	RO	1h	Status of the strong power-switch0x0 : indicates the/OFF status of the strong power-switch in digital toSOC.0x1 : ndicates the ON status of the strong power-switch in digital toSOC.
29	LDOPWDN	RO	1h	1 indicates ADPLLLJ internal LDO is power down. VDDLDOOUT willbe un-defined in this condition
28	RECAL_BSTATUS3	RO	0h	Recalibration status flag. 1 ADPLLLJ requires recalibration
27	RECAL_OPPIN	RO	0h	Recalibration status flag. 1 ADPLLLJ requires recalibration
	RESERVED	NONE		Reserved
12	CLKOUTLDOENACK	RO	1h	Indicates the enable/disable condition of CLKOUTLDOEN0x0 = CLKOUTLDO gating completed0x1 = CLKOUTLDO enabling completed
11	CLKDCOLDOACK	RO	0h	Indicates the enable/disable condition of CLKDCOLDOEN0x0 = CLKDCOLDO gating completed0x1 = CLKDCOLOD enabling completed
10	PHASELOCK	RO	0h	Status on PHASELOCK output pin
9	FREQLOCK	RO	0h	Status on FREQLOCK output pin
8	BYPASSACK	RO	1h	Status of BYPASSACK output pin
7	STBYRETACK	RO	0h	Standby and retention status0x0: indicates to SOC that all internal clocks in ADPLLLJ are activeand it is starting the relock process.0x1: indicates to SOC that all internal clocks in ADPLLLJ are gatedand it is ready for retention.
6	LOSSREF	RO	1h	Reference input loss
5	CLKOUTENACK	RO	0h	Indicates the enable/disable condition of CLKOUTEN0x0 = CLKOUT gating completed0x1 = CLKOUT enabling completed
4	LOCK2	RO	0h	ADPLL internal loop lock status
3	M2CHANGEACK	RO	0h	Acknowledge for change to M2 divider. Toggles from 1-0 or 0-1(depending on current value) once CLKOUT frequency change hascompleted.
2	SSCACK	RO	0h	Spread Spectrum status0x0 : Spread-spectrum Clocking is disabled on output clocks0x1 : Spread-spectrum Clocking is enabled on output clocks
1	HIGHJITTER	RO	0h	1 indicates jitter. After PHASELOCK is asserted high, theHIGHJITTER flag is asserted high if phase error between REFCLKand FBCLK greater than 24%.
0	BYPASS	RO	1h	Bypass status signal. 1 CLKOUT in bypass

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2.5.25 TOP_RCM_MSS_TOPRCM_PLL_CORE_HSDIVIDER Registers

2.5.25.1 TOP_PLL_CORE_HSDIVIDER Register (Offset = 428h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-901. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0428h

Access Types Legend

Table 2-902. PLL_CORE_HSDIVIDER Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	LDOPWDNACK	RO	0h	LDO Power Down Ack
16	BYPASSACKZ	RO	0h	HSDIVIDER Bypass Ack
	RESERVED	NONE		Reserved
2	TENABLEDIV	RW	0h	Tenable Div
1	LDOPWDN	RW	0h	LDO Power Down
0	BYPASS	RW	0h	HSDIVIDER Bypass

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2.5.26 TOP_RCM_MSS_TOPRCM_PLL_CORE_HSDIVIDER_CLKOUT0 Registers

2.5.26.1 TOP_PLL_CORE_HSDIVIDER_CLKOUT0 Register (Offset = 42Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-903. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 042Ch

Access Types Legend

Table 2-904. PLL_CORE_HSDIVIDER_CLKOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
12	PWDN	RW	0h	Power down for HSDIVIDER M4 divider and hence CLKOUT0 output0h (R/W) = CLKOUT0 divider active1h (R/W) = CLKOUT0 divider is powered down
	RESERVED	NONE		Reserved
9	STATUS	RO	0h	HSDIVIDER CLKOUT0 status0h (R) = The clock output is gated1h (R) = The clock output is enabled
8	GATE_CTRL	RW	0h	Control gating of HSDIVIDER CLKOUT00h (R/W) = Automatically gate this clock when there is nodependency for it1h (R/W) = Force this clock to stay enabled even if there is norequest
	RESERVED	NONE		Reserved
5	DIVCHACK	RO	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT0_DIVindicates that the change in divider value has taken effect
4 - 0	DIV	RW	4h	DPLL post-divider factor, M4, for internal clock generation.Divide values from 1 to 31.0h (R/W) = Reserved

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2.5.27 TOP_RCM_MSS_TOPRCM_PLL_CORE_HSDIVIDER_CLKOUT1 Registers

2.5.27.1 TOP_PLL_CORE_HSDIVIDER_CLKOUT1 Register (Offset = 430h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-905. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0430h

Access Types Legend

Table 2-906. PLL_CORE_HSDIVIDER_CLKOUT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
12	PWDN	RW	0h	Power down for HSDIVIDER M5 divider and hence CLKOUT1 output0h (R/W) = CLKOUT1 divider active1h (R/W) = CLKOUT1 divider is powered down
	RESERVED	NONE		Reserved
9	STATUS	RO	0h	HSDIVIDER CLKOUT1 status0h (R) = The clock output is gated1h (R) = The clock output is enabled
8	GATE_CTRL	RW	0h	Control gating of HSDIVIDER CLKOUT10h (R/W) = Automatically gate this clock when there is nodependency for it1h (R/W) = Force this clock to stay enabled even if there is norequest
	RESERVED	NONE		Reserved
5	DIVCHACK	RO	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIVindicates that the change in divider value has taken effect
4 - 0	DIV	RW	3h	DPLL post-divider factor, M5, for internal clock generation.Divide values from 1 to 31.0h (R/W) = Reserved

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2.5.28 TOP_RCM_MSS_TOPRCM_PLL_CORE_HSDIVIDER_CLKOUT2 Registers

2.5.28.1 TOP_PLL_CORE_HSDIVIDER_CLKOUT2 Register (Offset = 434h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-907. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0434h

Access Types Legend

Table 2-908. PLL_CORE_HSDIVIDER_CLKOUT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
12	PWDN	RW	0h	Power down for HSDIVIDER M6 divider and hence CLKOUT2 output0h (R/W) = CLKOUT2 divider active1h (R/W) = CLKOUT2 divider is powered down
	RESERVED	NONE		Reserved
9	STATUS	RO	0h	HSDIVIDER CLKOUT2 status0h (R) = The clock output is gated1h (R) = The clock output is enabled
8	GATE_CTRL	RW	0h	Control gating of HSDIVIDER CLKOUT20h (R/W) = Automatically gate this clock when there is nodependency for it1h (R/W) = Force this clock to stay enabled even if there is norequest
	RESERVED	NONE		Reserved
5	DIVCHACK	RO	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT2_DIVindicates that the change in divider value has taken effect
4 - 0	DIV	RW	4h	DPLL post-divider factor, M6, for internal clock generation.Divide values from 1 to 31.0h (R/W) = Reserved

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2.5.29 TOP_RCM_MSS_TOPRCM_PLL_CORE_RSTCTRL Registers

2.5.29.1 TOP_PLL_CORE_RSTCTRL Register (Offset = 43Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-909. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 043Ch

Access Types Legend

Table 2-910. PLL_CORE_RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	SW Reset override for the PLLWrite 3'b111 : Override is enabled and Reset is asserted

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2.5.30 TOP_RCM_MSS_TOPRCM_PLL_CORE_HSDIVIDER_RSTCTRL Registers

2.5.30.1 TOP_PLL_CORE_HSDIVIDER_RSTCTRL Register (Offset = 440h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-911. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0440h

Access Types Legend

Table 2-912. PLL_CORE_HSDIVIDER_RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	SW Reset override for the HSDIVIDERWrite 3'b111 : Override is enabled and Reset is asserted

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2.5.31 TOP_RCM_MSS_TOPRCM_R5SS_CLK_SRC_SEL Registers

2.5.31.1 TOP_R5SS_CLK_SRC_SEL Register (Offset = 500h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-913. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0500h

Access Types Legend

Table 2-914. R5SS_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for MSS Coretex R5 and System bus Clock.Data should be loaded as multibit. For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register.Refer to AM602 clock spec for source clock reference

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2.5.32 TOP_RCM_MSS_TOPRCM_R5SS_CLK_STATUS Registers

2.5.32.1 TOP_R5SS_CLK_STATUS Register (Offset = 504h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-915. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0504h

Access Types Legend

Table 2-916. R5SS_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Root clock for CortexR5 and Sysclk

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2.5.33 TOP_RCM_MSS_TOPRCM_R5SS0_CLK_DIV_SEL Registers

2.5.33.1 TOP_R5SS0_CLK_DIV_SEL Register (Offset = 510h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-917. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0510h

Access Types Legend

Table 2-918. R5SS0_CLK_DIV_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLKDIVSEL	RW	0h	writing 3'b000 Sets R5 clock = R5SS Root clockWriting 3'b111 Sets R5 Clock = SYSCLK

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2.5.34 TOP_RCM_MSS_TOPRCM_R5SS1_CLK_DIV_SEL Registers

2.5.34.1 TOP_R5SS1_CLK_DIV_SEL Register (Offset = 514h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-919. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0514h

Access Types Legend

Table 2-920. R5SS1_CLK_DIV_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLKDIVSEL	RW	0h	writing 3'b000 Sets R5 clock = R5SS Root clockWriting 3'b111 Sets R5 Clock = SYSCLK

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2.5.35 TOP_RCM_MSS_TOPRCM_R5SS0_CLK_GATE Registers

2.5.35.1 TOP_R5SS0_CLK_GATE Register (Offset = 518h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-921. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0518h

Access Types Legend

Table 2-922. R5SS0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Only for debug- Functionality not guaranteed Clock gating config for MSS Coretex R5.Data should be loaded as multibit. Write 3'b000 : Clock is ungated (multibit 000)Write 3'b111 : Clock is gated (multibit 111)

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2.5.36 TOP_RCM_MSS_TOPRCM_R5SS1_CLK_GATE Registers

2.5.36.1 TOP_R5SS1_CLK_GATE Register (Offset = 51Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-923. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 051Ch

Access Types Legend

Table 2-924. R5SS1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Only for debug- Functionality not guaranteed Clock gating config for MSS Coretex R5.Data should be loaded as multibit. Write 3'b000 : Clock is ungated (multibit 000)Write 3'b111 : Clock is gated (multibit 111)

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2.5.37 TOP_RCM_MSS_TOPRCM_SYS_CLK_DIV_VAL Registers

2.5.37.1 TOP_SYS_CLK_DIV_VAL Register (Offset = 520h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-925. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0520h

Access Types Legend

Table 2-926. SYS_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIV	RW	0h	Divider value for System Clock selected clock.Data should be loaded as multibit. For example: if divider value of 0x5 should be selected then 0x555 should be configured to the register.

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2.5.38 TOP_RCM_MSS_TOPRCM_SYS_CLK_GATE Registers

2.5.38.1 TOP_SYS_CLK_GATE Register (Offset = 524h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-927. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0524h

Access Types Legend

Table 2-928. SYS_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Only for debug- Functionality not guaranteed Clock gating config for System ClockData should be loaded as multibit. Write 3'b000 : Clock is ungated (multibit 000)Write 3'b111 : Clock is gated (multibit 111)

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2.5.39 TOP_RCM_MSS_TOPRCM_SYS_CLK_STATUS Registers

2.5.39.1 TOP_SYS_CLK_STATUS Register (Offset = 528h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-929. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0528h

Access Types Legend

Table 2-930. SYS_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Sys Clock
	RESERVED	NONE		Reserved

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2.5.40 TOP_RCM_MSS_TOPRCM_PLL_PER_PWRCTRL Registers

2.5.40.1 TOP_PLL_PER_PWRCTRL Register (Offset = 800h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-931. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0800h

Access Types Legend

Table 2-932. PLL_PER_PWRCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
5	PONIN	RW	1h	ON/OFF control of the weak power switch digital. For functionalmode it should be 1
4	PGOODIN	RW	1h	ON/OFF control of the strong power switch digital. For functional mode it should be 1
3	RET	RW	0h	Save/Restore control for Retention mode. For functional mode itshould be 0
2	ISORET	RW	0h	Save/Restore control for Isolation of output pins For functional modeit should be 0
1	ISOSCAN	RW	0h	Save/Restore control for Isolation of the Scanout pins. For functionalmode it should be 0
0	OFFMODE	RW	0h	Used to switch OFF the logic on VDDA. For functional mode itshould be 0

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2.5.41 TOP_RCM_MSS_TOPRCM_PLL_PER_CLKCTRL Registers

2.5.41.1 TOP_PLL_PER_CLKCTRL Register (Offset = 804h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-933. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0804h

Access Types Legend

Table 2-934. PLL_PER_CLKCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CYCLESLIPEN	RW	0h	FailSafe enable to trigger re-calibration in case CycleSlip occurs between REFCLK and FBCLK.
30	ENSSC	RW	0h	Controls Clock Spreading. SSC is not supported. Should be set to 0x0 to disable clock spreading.
29	CLKDCOLDOEN	RW	0h	Synchronously enables/disables CLKDCOLDO0x0 : synchronously disables CLKDCOLDO0x1 : synchronously enables CLKDCOLDO
	RESERVED	NONE		Reserved
23	IDLE	RW	1h	Sets PLL to Idle mode0x0 : When SYSRESET = 0 and TINITZ = 1 IDLE = 0 PLL will go toActive and Locked0x1 : When SYSRESET = 0 and TINITZ = 1 IDLE = 1 PLL will go toIdle Bypass low powe
22	BYPASSACKZ	RW	0h	BYPASSACKZ is a special purpose input to the module. In generalthis input is expected to be tied to static low. For the output clocks ofthe module that do not have an internal bypass mux viz.CLKDCOLDO and CLKOUTLDO, a bypass mux could beimplemented external to the module.
21	STBYRET	RW	0h	Standby retention control0x0 : prepares ADPLLLJ for relock when out of retention byremoving the gating on all internal clocks.0x1 : prepares ADPLLLJ for retention by gating all the internalclocks.
20	CLKOUTEN	RW	0h	CLKOUT enable or disable0x0 : synchronously disables CLKOUT0x1 : synchronously enables CLKOUT
19	CLKOUTLDOEN	RW	1h	Synchronously enables/disables CLKOUTLDO 0x0 : synchronously disables CLKOUTLDO 0x1 : synchronously enables CLKOUTLDO
18	ULOWCLKEN	RW	0h	Select CLKOUT source in bypass0x0: When ADPLLLJ in bypass mode, CLKOUT = CLKINP/(N2+1)0x1: When ADPLLLJ in bypass mode, CLKOUT = CLKINPULOW.
17	CLKDCOLDOPWDNZ	RW	0h	0 Asynchronous power down for CLKDCOLDO o/p.
16	M2PWDNZ	RW	1h	M2 divider power down mode0x0: Asynchronous power down for M2 divider0x1 : M2 divider is functional
	RESERVED	NONE		Reserved
14	STOPMODE	RW	1h	When in Lossclk/Stbyret 0x0 : Limp mode 0x1 : Stopmode
	RESERVED	NONE		Reserved
12 - 10	SELFREQDCO	RW	64h	DCO Clock (DCOCLK = CLKINP * [M/(N+1)]) frequency rangeselector.0x0: Reserved0x2: HS2 : DCOCLK range is from 500 MHz to 1000 MHz0x3: Reserved0x4: HS1: DCOCLK range is from 1000 MHz to 2000 MHz0x5: Reserved
	RESERVED	NONE		Reserved
8	RELAXED_LOCK	RW	0h	Decides when FREQLOCK asserted0x0: FREQLOCK asserted when DC frequency error less than 1%0x1: FREQLOCK asserted when DC frequency error less than 2%
	RESERVED	NONE		Reserved
1	SSCTYPE	RW	0h	SSC Type

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Table 2-934. PLL_PER_CLKCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TINTZ	RW	0h	PLL core soft reset

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2.5.42 TOP_RCM_MSS_TOPRCM_PLL_PER_TENABLE Registers

2.5.42.1 TOP_PLL_PER_TENABLE Register (Offset = 808h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-935. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0808h

Access Types Legend

Table 2-936. PLL_PER_TENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
0	TENABLE	RW	0h	M, N. SD and SELFREQDCO latch (active rise edge)

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2.5.43 TOP_RCM_MSS_TOPRCM_PLL_PER_TENABLEDIV Registers

2.5.43.1 TOP_PLL_PER_TENABLEDIV Register (Offset = 80Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-937. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 080Ch

Access Types Legend

Table 2-938. PLL_PER_TENABLEDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
0	TENABLEDIV	RW	0h	M2 and N2 latch (active rise edge)

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2.5.44 TOP_RCM_MSS_TOPRCM_PLL_PER_M2NDIV Registers

2.5.44.1 TOP_PLL_PER_M2NDIV Register (Offset = 810h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-939. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0810h

Access Types Legend

Table 2-940. PLL_PER_M2NDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 16	M2	RW	0h	Post-divider is REGM2
	RESERVED	NONE		Reserved
7 - 0	N	RW	13h	Pre-divider is REGN+1

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2.5.45 TOP_RCM_MSS_TOPRCM_PLL_PER_MN2DIV Registers

2.5.45.1 TOP_PLL_PER_MN2DIV Register (Offset = 814h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-941. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0814h

Access Types Legend

Table 2-942. PLL_PER_MN2DIV Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 16	N2	RW	0h	Bypass divider is REGN2+1
	RESERVED	NONE		Reserved
11 - 0	M	RW	28FA6AE00h	Feedback Multiplier is REGM

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2.5.46 TOP_RCM_MSS_TOPRCM_PLL_PER_FRACDIV Registers

2.5.46.1 TOP_PLL_PER_FRACDIV Register (Offset = 818h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-943. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0818h

Access Types Legend

Table 2-944. PLL_PER_FRACDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	REGSD	RW	3E8h	Sigma-Delta DividerShould be set by s/w to provide optimum jitter performance.DPLL_SD_DIV = CEILING ([DPLL_MULT/ (DPLL_DIV+1)] * CLKINP/ 250), where CLKINP is the input clock of the DPLL in MHz
	RESERVED	NONE		Reserved
17 - 0	FRACTIONALM	RW	0h	Fractional part of the M divider.

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2.5.47 TOP_RCM_MSS_TOPRCM_PLL_PER_BWCTRL Registers

2.5.47.1 TOP_PLL_PER_BWCTRL Register (Offset = 81Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-945. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 081Ch

Access Types Legend

Table 2-946. PLL_PER_BWCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 1	BWCONTROL	RW	0h	Change Loop Bandwidth
0	BW_INCR_DECRZ	RW	0h	Direction of Loop Bandwidth0x0 : decrease BW0x1 : increase BW

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2.5.48 TOP_RCM_MSS_TOPRCM_PLL_PER_FRACCTRL Registers

2.5.48.1 TOP_PLL_PER_FRACCTRL Register (Offset = 820h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-947. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0820h

Access Types Legend

Table 2-948. PLL_PER_FRACCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DOWNSPREAD	RW	0h	Controls frequency spread0x0 : enables both side frequency spread about the programmed frequency.0x1 : enables low frequency spread only
30 - 28	MODFREQDIVIDEREXPONENT	RW	0h	Exponent of the REFCLK divider to define the modulation frequency.
27 - 21	MODFREQDIVIDERMANTISSA	RW	0h	Mantissa of the REFCLK divider to define the modulation frequency
20 - 18	DELTAMSTEPINTEGER	RW	0h	Integer part of Frequency Spread control
17 - 0	DELTAMSTEPFRACTION	RW	0h	The fraction part of Frequency Spread control

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2.5.49 TOP_RCM_MSS_TOPRCM_PLL_PER_STATUS Registers

2.5.49.1 TOP_PLL_PER_STATUS Register (Offset = 824h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-949. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0824h

Access Types Legend

Table 2-950. PLL_PER_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PONOUT	RO	1h	Status of the weak power-switch0x0 : indicates the/OFF status of the weak power-switch in digital toSOC.0x1 : ndicates the ON status of the weak power-switch in digital toSOC.
30	PGOODOUT	RO	1h	Status of the strong power-switch0x0 : indicates the/OFF status of the strong power-switch in digital toSOC.0x1 : ndicates the ON status of the strong power-switch in digital toSOC.
29	LDOPWDN	RO	1h	1 indicates ADPLLLJ internal LDO is power down. VDDLDOOUT willbe un-defined in this condition
28	RECAL_BSTATUS3	RO	0h	Recalibration status flag. 1 ADPLLLJ requires recalibration
27	RECAL_OPPIN	RO	0h	Recalibration status flag. 1 ADPLLLJ requires recalibration
	RESERVED	NONE		Reserved
12	CLKOUTLDOENACK	RO	1h	Indicates the enable/disable condition of CLKOUTLDOEN0x0 = CLKOUTLDO gating completed0x1 = CLKOUTLDO enabling completed
11	CLKDCOLDOACK	RO	0h	Indicates the enable/disable condition of CLKDCOLDOEN0x0 = CLKDCOLDO gating completed0x1 = CLKDCOLDO enabling completed
10	PHASELOCK	RO	0h	Status on PHASELOCK output pin
9	FREQLOCK	RO	0h	Status on FREQLOCK output pin
8	BYPASSACK	RO	1h	Status of BYPASSACK output pin
7	STBYRETACK	RO	0h	Standby and retention status0x0: indicates to SOC that all internal clocks in ADPLLLJ are activeand it is starting the relock process.0x1: indicates to SOC that all internal clocks in ADPLLLJ are gatedand it is ready for retention.
6	LOSSREF	RO	1h	Reference input loss
5	CLKOUTENACK	RO	0h	Indicates the enable/disable condition of CLKOUTEN0x0 = CLKOUT gating completed0x1 = CLKOUT enabling completed
4	LOCK2	RO	0h	ADPLL internal loop lock status
3	M2CHANGEACK	RO	0h	Acknowledge for change to M2 divider. Toggles from 1-0 or 0-1(depending on current value) once CLKOUT frequency change hascompleted.
2	SSCACK	RO	0h	Spread Spectrum status0x0 : Spread-spectrum Clocking is disabled on output clocks0x1 : Spread-spectrum Clocking is enabled on output clocks
1	HIGHJITTER	RO	0h	1 indicates jitter. After PHASELOCK is asserted high, theHIGHJITTER flag is asserted high if phase error between REFCLKand FBCLK greater than 24%.
0	BYPASS	RO	1h	Bypass status signal. 1 CLKOUT in bypass

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2.5.50 TOP_RCM_MSS_TOPRCM_PLL_PER_HSDIVIDER Registers

2.5.50.1 TOP_PLL_PER_HSDIVIDER Register (Offset = 828h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-951. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0828h

Access Types Legend

Table 2-952. PLL_PER_HSDIVIDER Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	LDOPWDNACK	RO	0h	LDO Power Down Ack
16	BYPASSACKZ	RO	0h	HSDIVIDER Bypass Ack
	RESERVED	NONE		Reserved
2	TENABLEDIV	RW	0h	Tenable Div
1	LDOPWDN	RW	0h	LDO Power Down
0	BYPASS	RW	0h	HSDIVIDER Bypass

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2.5.51 TOP_RCM_MSS_TOPRCM_PLL_PER_HSDIVIDER_CLKOUT0 Registers

2.5.51.1 TOP_PLL_PER_HSDIVIDER_CLKOUT0 Register (Offset = 82Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-953. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 082Ch

Access Types Legend

Table 2-954. PLL_PER_HSDIVIDER_CLKOUT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
12	PWDN	RW	0h	Power down for HSDIVIDER M4 divider and hence CLKOUT0 output0h (R/W) = CLKOUT0 divider active1h (R/W) = CLKOUT0 divider is powered down
	RESERVED	NONE		Reserved
9	STATUS	RO	0h	HSDIVIDER CLKOUT0 status0h (R) = The clock output is gated1h (R) = The clock output is enabled
8	GATE_CTRL	RW	0h	Control gating of HSDIVIDER CLKOUT00h (R/W) = Automatically gate this clock when there is nodependency for it1h (R/W) = Force this clock to stay enabled even if there is norequest
	RESERVED	NONE		Reserved
5	DIVCHACK	RO	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT0_DIVindicates that the change in divider value has taken effect
4 - 0	DIV	RW	Bh	DPLL post-divider factor, M4, for internal clock generation.Divide values from 1 to 31.0h (R/W) = Reserved

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2.5.52 TOP_RCM_MSS_TOPRCM_PLL_PER_HSDIVIDER_CLKOUT1 Registers

2.5.52.1 TOP_PLL_PER_HSDIVIDER_CLKOUT1 Register (Offset = 830h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-955. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0830h

Access Types Legend

Table 2-956. PLL_PER_HSDIVIDER_CLKOUT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
12	PWDN	RW	0h	Power down for HSDIVIDER M5 divider and hence CLKOUT1 output0h (R/W) = CLKOUT1 divider active1h (R/W) = CLKOUT1 divider is powered down
	RESERVED	NONE		Reserved
9	STATUS	RO	0h	HSDIVIDER CLKOUT1 status0h (R) = The clock output is gated1h (R) = The clock output is enabled
8	GATE_CTRL	RW	0h	Control gating of HSDIVIDER CLKOUT10h (R/W) = Automatically gate this clock when there is nodependency for it1h (R/W) = Force this clock to stay enabled even if there is norequest
	RESERVED	NONE		Reserved
5	DIVCHACK	RO	0h	Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIVindicates that the change in divider value has taken effect
4 - 0	DIV	RW	9h	DPLL post-divider factor, M5, for internal clock generation.Divide values from 1 to 31.0h (R/W) = Reserved

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2.5.53 TOP_RCM_MSS_TOPRCM_PLL_PER_RSTCTRL Registers

2.5.53.1 TOP_PLL_PER_RSTCTRL Register (Offset = 83Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-957. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 083Ch

Access Types Legend

Table 2-958. PLL_PER_RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	SW Reset override for the PLLWrite 3'b111 : Override is enabled and Reset is asserted

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2.5.54 TOP_RCM_MSS_TOPRCM_PLL_PER_HSDIVIDER_RSTCTRL Registers

2.5.54.1 TOP_PLL_PER_HSDIVIDER_RSTCTRL Register (Offset = 840h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-959. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0840h

Access Types Legend

Table 2-960. PLL_PER_HSDIVIDER_RSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	SW Reset override for the HSDIVIDERWrite 3'b111 : Override is enabled and Reset is asserted

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2.5.55 TOP_RCM_MSS_TOPRCM_CLKOUT0_CLK_SRC_SEL Registers

2.5.55.1 TOP_CLKOUT0_CLK_SRC_SEL Register (Offset = C00h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-961. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C00h

Access Types Legend

Table 2-962. CLKOUT0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for MSS CLKOUT .Data should be loaded as multibit. For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register.Refer to AM602 clock spec for source clock reference

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2.5.56 TOP_RCM_MSS_TOPRCM_CLKOUT1_CLK_SRC_SEL Registers

2.5.56.1 TOP_CLKOUT1_CLK_SRC_SEL Register (Offset = C04h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-963. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C04h

Access Types Legend

Table 2-964. CLKOUT1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for MSS CLKOUT .Data should be loaded as multibit. For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register.Refer to AM602 clock spec for source clock reference

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2.5.57 TOP_RCM_MSS_TOPRCM_CLKOUT0_DIV_VAL Registers

2.5.57.1 TOP_CLKOUT0_DIV_VAL Register (Offset = C08h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-965. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C08h

Access Types Legend

Table 2-966. CLKOUT0_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIV	RW	0h	Divider value for CLKOUT selected clock.Data should be loaded as multibit. For example: if divider value of 0x5 should be selected then 0x555 should be configured to the register.

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2.5.58 TOP_RCM_MSS_TOPRCM_CLKOUT1_DIV_VAL Registers

2.5.58.1 TOP_CLKOUT1_DIV_VAL Register (Offset = C0Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-967. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C0Ch

Access Types Legend

Table 2-968. CLKOUT1_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIV	RW	0h	Divider value for CLKOUT selected clock.Data should be loaded as multibit. For example: if divider value of 0x5 should be selected then 0x555 should be configured to the register.

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2.5.59 TOP_RCM_MSS_TOPRCM_CLKOUT0_CLK_GATE Registers

2.5.59.1 TOP_CLKOUT0_CLK_GATE Register (Offset = C10h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-969. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C10h

Access Types Legend

Table 2-970. CLKOUT0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Only for debug- Functionality not guaranteed Clock gating config for MSS CLKOUTData should be loaded as multibit. Write 3'b000 : Clock is ungated (multibit 000)Write 3'b111 : Clock is gated (multibit 111)

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2.5.60 TOP_RCM_MSS_TOPRCM_CLKOUT1_CLK_GATE Registers

2.5.60.1 TOP_CLKOUT1_CLK_GATE Register (Offset = C14h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-971. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C14h

Access Types Legend

Table 2-972. CLKOUT1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Only for debug- Functionality not guaranteed Clock gating config for MSS CLKOUTData should be loaded as multibit. Write 3'b000 : Clock is ungated (multibit 000)Write 3'b111 : Clock is gated (multibit 111)

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2.5.61 TOP_RCM_MSS_TOPRCM_CLKOUT0_CLK_STATUS Registers

2.5.61.1 TOP_CLKOUT0_CLK_STATUS Register (Offset = C18h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-973. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C18h

Access Types Legend

Table 2-974. CLKOUT0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for CLKOUT Clock
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for CLKOUT Clock

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2.5.62 TOP_RCM_MSS_TOPRCM_CLKOUT1_CLK_STATUS Registers

2.5.62.1 TOP_CLKOUT1_CLK_STATUS Register (Offset = C1Ch) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-975. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C1Ch

Access Types Legend

Table 2-976. CLKOUT1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for CLKOUT Clock
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for CLKOUT Clock

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2.5.63 TOP_RCM_MSS_TOPRCM_TRCCLKOUT_CLK_SRC_SEL Registers

2.5.63.1 TOP_TRCCLKOUT_CLK_SRC_SEL Register (Offset = C20h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-977. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C20h

Access Types Legend

Table 2-978. TRCCLKOUT_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for TRC ClkoutData should be loaded as multibit. For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register.Refer to AM602 clock spec for source clock reference

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2.5.64 TOP_RCM_MSS_TOPRCM_TRCCLKOUT_DIV_VAL Registers

2.5.64.1 TOP_TRCCLKOUT_DIV_VAL Register (Offset = C24h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-979. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C24h

Access Types Legend

Table 2-980. TRCCLKOUT_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIV	RW	0h	Divider value for TRC Clkout selected clock.Data should be loaded as multibit. For example: if divider value of 0x5 should be selected then 0x555 should be configured to the register.

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2.5.65 TOP_RCM_MSS_TOPRCM_TRCCLKOUT_CLK_GATE Registers

2.5.65.1 TOP_TRCCLKOUT_CLK_GATE Register (Offset = C28h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-981. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C28h

Access Types Legend

Table 2-982. TRCCLKOUT_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Clock gatring config for TRC ClkoutData should be loaded as multibit. Write 3'b000 : Clock is ungated (multibit 000)Write 3'b111 : Clock is gated (multibit 111)

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2.5.66 TOP_RCM_MSS_TOPRCM_TRCCLKOUT_CLK_STATUS Registers

2.5.66.1 TOP_TRCCLKOUT_CLK_STATUS Register (Offset = C2Ch) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-983. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 0C2Ch

Access Types Legend

Table 2-984. TRCCLKOUT_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for PMIC Clkout Clock
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for PMIC Clkout Clock

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2.5.67 TOP_RCM_MSS_TOPRCM_LOCK0_KICK0 Registers

2.5.67.1 TOP_LOCK0_KICK0 Register (Offset = 1008h) [reset = h]

Short Description: - KICK0 component

Long Description:

Return to Summary Table

Table 2-985. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1008h

Access Types Legend

Table 2-986. LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	LOCK0_KICK0	RW	0h	- KICK0 component

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2.5.68 TOP_RCM_MSS_TOPRCM_LOCK0_KICK1 Registers

2.5.68.1 TOP_LOCK0_KICK1 Register (Offset = 100Ch) [reset = h]

Short Description: - KICK1 component

Long Description:

Return to Summary Table

Table 2-987. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 100Ch

Access Types Legend

Table 2-988. LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	LOCK0_KICK1	RW	0h	- KICK1 component

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2.5.69 TOP_RCM_MSS_TOPRCM_INTR_RAW_STATUS Registers

2.5.69.1 TOP_INTR_RAW_STATUS Register (Offset = 1010h) [reset = h]

Short Description: Interrupt Raw Status/Set Register

Long Description:

Return to Summary Table

Table 2-989. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1010h

Access Types Legend

Table 2-990. INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR	RW	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
2	KICK_ERR	RW	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
1	ADDR_ERR	RW	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
0	PROT_ERR	RW	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.

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2.5.70 TOP_RCM_MSS_TOPRCM_INTR_ENABLED_STATUS_CLEAR Registers

2.5.70.1 TOP_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = h]

Short Description: Interrupt Enabled Status/Clear register

Long Description:

Return to Summary Table

Table 2-991. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1014h

Access Types Legend

Table 2-992. INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	ENABLED_PROXY_ERR	RW	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
2	ENABLED_KICK_ERR	RW	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
1	ENABLED_ADDR_ERR	RW	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
0	ENABLED_PROT_ERR	RW	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.

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2.5.71 TOP_RCM_MSS_TOPRCM_INTR_ENABLE Registers

2.5.71.1 TOP_INTR_ENABLE Register (Offset = 1018h) [reset = h]

Short Description: Interrupt Enable register

Long Description:

Return to Summary Table

Table 2-993. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1018h

Access Types Legend

Table 2-994. INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR_EN	RW	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
2	KICK_ERR_EN	RW	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN	RW	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
0	PROT_ERR_EN	RW	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.

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2.5.72 TOP_RCM_MSS_TOPRCM_INTR_ENABLE_CLEAR Registers

2.5.72.1 TOP_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = h]

Short Description: Interrupt Enable Clear register

Long Description:

Return to Summary Table

Table 2-995. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 101Ch

Access Types Legend

Table 2-996. INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR_EN_CLR	RW	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
2	KICK_ERR_EN_CLR	RW	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN_CLR	RW	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
0	PROT_ERR_EN_CLR	RW	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.

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2.5.73 TOP_RCM_MSS_TOPRCM_EOI Registers

2.5.73.1 TOP_EOI Register (Offset = 1020h) [reset = h]

Short Description: EOI register

Long Description:

Return to Summary Table

Table 2-997. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1020h

Access Types Legend

Table 2-998. EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	EOI_VECTOR	RW	0h	EOI vector value. Write this with interrupt distribution value in the chip.

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2.5.74 TOP_RCM_MSS_TOPRCM_FAULT_ADDRESS Registers

2.5.74.1 TOP_FAULT_ADDRESS Register (Offset = 1024h) [reset = h]

Short Description: Fault Address register

Long Description:

Return to Summary Table

Table 2-999. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1024h

Access Types Legend

Table 2-1000. FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FAULT_ADDR	RO	0h	Fault Address.

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2.5.75 TOP_RCM_MSS_TOPRCM_FAULT_TYPE_STATUS Registers

2.5.75.1 TOP_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = h]

Short Description: Fault Type Status register

Long Description:

Return to Summary Table

Table 2-1001. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1028h

Access Types Legend

Table 2-1002. FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	FAULT_NS	RO	0h	Non-secure access.
5 - 0	FAULT_TYPE	RO	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype ! = 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault

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2.5.76 TOP_RCM_MSS_TOPRCM_FAULT_ATTR_STATUS Registers

2.5.76.1 TOP_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = h]

Short Description: Fault Attribute Status register

Long Description:

Return to Summary Table

Table 2-1003. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 102Ch

Access Types Legend

Table 2-1004. FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	FAULT_XID	RO	0h	XID.
19 - 8	FAULT_ROUTEID	RO	0h	Route ID.
7 - 0	FAULT_PRIVID	RO	0h	Privilege ID.

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2.5.77 TOP_RCM_MSS_TOPRCM_FAULT_CLEAR Registers

2.5.77.1 TOP_FAULT_CLEAR Register (Offset = 1030h) [reset = h]

Short Description: Fault Clear register

Long Description:

Return to Summary Table

Table 2-1005. Instance Table

Instance Name	Physical Address
TOP_RCM	5320 1030h

Access Types Legend

Table 2-1006. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
0	FAULT_CLR	WO	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect.

2.5.78 Access Table

Table 2-1007. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
WO	WO	Write

2.6 MSS_RCM Registers

Table 2-1008. MSS_RCM Registers Base Address Table

Offset	Length	Acronym	Register Name	MSS_RCM Physical Address
0h	32	MSS_RCM_PID	PID register	5320 8000h
10h	16	MSS_RCM_R5SS0_RST_STATUS	R5SS0_RST_STATUS register	5320 8010h
14h	8	MSS_RCM_R5SS0_RST_CAUSE_CLR	R5SS0_RST_CAUSE_CLR register	5320 8014h
18h	24	MSS_RCM_R5SS0_DBG_RST_EN	R5SS0_DBG_RST_EN register	5320 8018h
1Ch	8	MSS_RCM_R5SS0_RST_ASSERDLY	R5SS0_RST_ASSERDLY register	5320 801Ch
20h	32	MSS_RCM_R5SS0_RST2ASSERTDLY	R5SS0_RST2ASSERTDLY register	5320 8020h
24h	32	MSS_RCM_R5SS0_RST_WFICHECK	R5SS0_RST_WFICHECK register	5320 8024h
30h	16	MSS_RCM_R5SS1_RST_STATUS	R5SS1_RST_STATUS register	5320 8030h
34h	8	MSS_RCM_R5SS1_RST_CAUSE_CLR	R5SS1_RST_CAUSE_CLR register	5320 8034h
38h	24	MSS_RCM_R5SS1_DBG_RST_EN	R5SS1_DBG_RST_EN register	5320 8038h
3Ch	8	MSS_RCM_R5SS1_RST_ASSERDLY	R5SS1_RST_ASSERDLY register	5320 803Ch
40h	32	MSS_RCM_R5SS1_RST2ASSERTDLY	R5SS1_RST2ASSERTDLY register	5320 8040h
44h	32	MSS_RCM_R5SS1_RST_WFICHECK	R5SS1_RST_WFICHECK register	5320 8044h
100h	16	MSS_RCM_MCAN0_CLK_SRC_SEL	MCAN0_CLK_SRC_SEL register	5320 8100h
104h	16	MSS_RCM_MCAN1_CLK_SRC_SEL	MCAN1_CLK_SRC_SEL register	5320 8104h

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Table 2-1008. MSS_RCM Registers Base Address Table (continued)

Offset	Length	Acronym	Register Name	MSS_RCM Physical Address
108h	16	MSS_RCM_MCAN2_CLK_SRC_SEL	MCAN2_CLK_SRC_SEL register	5320 8108h
10Ch	16	MSS_RCM_MCAN3_CLK_SRC_SEL	MCAN3_CLK_SRC_SEL register	5320 810Ch
110h	16	MSS_RCM_QSPI0_CLK_SRC_SEL	QSPI0_CLK_SRC_SEL register	5320 8110h
114h	16	MSS_RCM_RTI0_CLK_SRC_SEL	RTI0_CLK_SRC_SEL register	5320 8114h
118h	16	MSS_RCM_RTI1_CLK_SRC_SEL	RTI1_CLK_SRC_SEL register	5320 8118h
11Ch	16	MSS_RCM_RTI2_CLK_SRC_SEL	RTI2_CLK_SRC_SEL register	5320 811Ch
120h	16	MSS_RCM_RTI3_CLK_SRC_SEL	RTI3_CLK_SRC_SEL register	5320 8120h
128h	16	MSS_RCM_WDT0_CLK_SRC_SEL	WDT0_CLK_SRC_SEL register	5320 8128h
12Ch	16	MSS_RCM_WDT1_CLK_SRC_SEL	WDT1_CLK_SRC_SEL register	5320 812Ch
130h	16	MSS_RCM_WDT2_CLK_SRC_SEL	WDT2_CLK_SRC_SEL register	5320 8130h
134h	16	MSS_RCM_WDT3_CLK_SRC_SEL	WDT3_CLK_SRC_SEL register	5320 8134h
13Ch	16	MSS_RCM_MCSPI0_CLK_SRC_SEL	MCSPI0_CLK_SRC_SEL register	5320 813Ch
140h	16	MSS_RCM_MCSPI1_CLK_SRC_SEL	MCSPI1_CLK_SRC_SEL register	5320 8140h
144h	16	MSS_RCM_MCSPI2_CLK_SRC_SEL	MCSPI2_CLK_SRC_SEL register	5320 8144h
148h	16	MSS_RCM_MCSPI3_CLK_SRC_SEL	MCSPI3_CLK_SRC_SEL register	5320 8148h
14Ch	16	MSS_RCM_MCSPI4_CLK_SRC_SEL	MCSPI4_CLK_SRC_SEL register	5320 814Ch
150h	16	MSS_RCM_MMC0_CLK_SRC_SEL	MMC0_CLK_SRC_SEL register	5320 8150h
154h	16	MSS_RCM_ICSSM0_UART0_CLK_SRC_SEL	ICSSM0_UART0_CLK_SRC_SEL register	5320 8154h
158h	16	MSS_RCM_CPTS_CLK_SRC_SEL	CPTS_CLK_SRC_SEL register	5320 8158h
15Ch	16	MSS_RCM_GPMC_CLK_SRC_SEL	GPMC_CLK_SRC_SEL register	5320 815Ch
160h	16	MSS_RCM_CONTROLSS_PLL_CLK_SRC_SEL	CONTROLSS_PLL_CLK_SRC_SEL register	5320 8160h
164h	16	MSS_RCM_I2C_CLK_SRC_SEL	I2C_CLK_SRC_SEL register	5320 8164h
174h	16	MSS_RCM_LIN0_UART0_CLK_SRC_SEL	LIN0_UART0_CLK_SRC_SEL register	5320 8174h
178h	16	MSS_RCM_LIN1_UART1_CLK_SRC_SEL	LIN1_UART1_CLK_SRC_SEL register	5320 8178h
17Ch	16	MSS_RCM_LIN2_UART2_CLK_SRC_SEL	LIN2_UART2_CLK_SRC_SEL register	5320 817Ch
180h	16	MSS_RCM_LIN3_UART3_CLK_SRC_SEL	LIN3_UART3_CLK_SRC_SEL register	5320 8180h
184h	16	MSS_RCM_LIN4_UART4_CLK_SRC_SEL	LIN4_UART4_CLK_SRC_SEL register	5320 8184h
188h	16	MSS_RCM_LIN5_UART5_CLK_SRC_SEL	LIN5_UART5_CLK_SRC_SEL register	5320 8188h
200h	16	MSS_RCM_MCAN0_CLK_DIV_VAL	MCAN0_CLK_DIV_VAL register	5320 8200h
204h	16	MSS_RCM_MCAN1_CLK_DIV_VAL	MCAN1_CLK_DIV_VAL register	5320 8204h
208h	16	MSS_RCM_MCAN2_CLK_DIV_VAL	MCAN2_CLK_DIV_VAL register	5320 8208h
20Ch	16	MSS_RCM_MCAN3_CLK_DIV_VAL	MCAN3_CLK_DIV_VAL register	5320 820Ch
210h	16	MSS_RCM_QSPI0_CLK_DIV_VAL	QSPI0_CLK_DIV_VAL register	5320 8210h
214h	16	MSS_RCM_RTI0_CLK_DIV_VAL	RTI0_CLK_DIV_VAL register	5320 8214h
218h	16	MSS_RCM_RTI1_CLK_DIV_VAL	RTI1_CLK_DIV_VAL register	5320 8218h
21Ch	16	MSS_RCM_RTI2_CLK_DIV_VAL	RTI2_CLK_DIV_VAL register	5320 821Ch
220h	16	MSS_RCM_RTI3_CLK_DIV_VAL	RTI3_CLK_DIV_VAL register	5320 8220h
228h	16	MSS_RCM_WDT0_CLK_DIV_VAL	WDT0_CLK_DIV_VAL register	5320 8228h
22Ch	16	MSS_RCM_WDT1_CLK_DIV_VAL	WDT1_CLK_DIV_VAL register	5320 822Ch
230h	16	MSS_RCM_WDT2_CLK_DIV_VAL	WDT2_CLK_DIV_VAL register	5320 8230h
234h	16	MSS_RCM_WDT3_CLK_DIV_VAL	WDT3_CLK_DIV_VAL register	5320 8234h

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Table 2-1008. MSS_RCM Registers Base Address Table (continued)

Offset	Length	Acronym	Register Name	MSS_RCM Physical Address
23Ch	16	MSS_RCM_MCSPI0_CLK_DIV_VAL	MCSPI0_CLK_DIV_VAL register	5320 823Ch
240h	16	MSS_RCM_MCSPI1_CLK_DIV_VAL	MCSPI1_CLK_DIV_VAL register	5320 8240h
244h	16	MSS_RCM_MCSPI2_CLK_DIV_VAL	MCSPI2_CLK_DIV_VAL register	5320 8244h
248h	16	MSS_RCM_MCSPI3_CLK_DIV_VAL	MCSPI3_CLK_DIV_VAL register	5320 8248h
24Ch	16	MSS_RCM_MCSPI4_CLK_DIV_VAL	MCSPI4_CLK_DIV_VAL register	5320 824Ch
250h	16	MSS_RCM_MMC0_CLK_DIV_VAL	MMC0_CLK_DIV_VAL register	5320 8250h
254h	16	MSS_RCM_ICSSM0_UART_CLK_DIV_VAL	ICSSM0_UART_CLK_DIV_VAL register	5320 8254h
258h	16	MSS_RCM_CPTS_CLK_DIV_VAL	CPTS_CLK_DIV_VAL register	5320 8258h
25Ch	16	MSS_RCM_GPMC_CLK_DIV_VAL	GPMC_CLK_DIV_VAL register	5320 825Ch
260h	16	MSS_RCM_CONTROLSS_PLL_CLK_DIV_VAL	CONTROLSS_PLL_CLK_DIV_VAL register	5320 8260h
264h	16	MSS_RCM_I2C_CLK_DIV_VAL	I2C_CLK_DIV_VAL register	5320 8264h
274h	16	MSS_RCM_LIN0_UART0_CLK_DIV_VAL	LIN0_UART0_CLK_DIV_VAL register	5320 8274h
278h	16	MSS_RCM_LIN1_UART1_CLK_DIV_VAL	LIN1_UART1_CLK_DIV_VAL register	5320 8278h
27Ch	16	MSS_RCM_LIN2_UART2_CLK_DIV_VAL	LIN2_UART2_CLK_DIV_VAL register	5320 827Ch
280h	16	MSS_RCM_LIN3_UART3_CLK_DIV_VAL	LIN3_UART3_CLK_DIV_VAL register	5320 8280h
284h	16	MSS_RCM_LIN4_UART4_CLK_DIV_VAL	LIN4_UART4_CLK_DIV_VAL register	5320 8284h
288h	16	MSS_RCM_LIN5_UART5_CLK_DIV_VAL	LIN5_UART5_CLK_DIV_VAL register	5320 8288h
28Ch	16	MSS_RCM_RGMII_250_CLK_DIV_VAL	RGMII_250_CLK_DIV_VAL register	5320 828Ch
290h	16	MSS_RCM_RGMII_50_CLK_DIV_VAL	RGMII_50_CLK_DIV_VAL register	5320 8290h
294h	24	MSS_RCM_RGMII_5_CLK_DIV_VAL	RGMII_5_CLK_DIV_VAL register	5320 8294h
298h	32	MSS_RCM_XTAL_MMC_32K_CLK_DIV_VAL	XTAL_MMC_32K_CLK_DIV_VAL register	5320 8298h
29Ch	32	MSS_RCM_XTAL_TEMPSENSE_32K_CLK_DIV_VAL	XTAL_TEMPSENSE_32K_CLK_DIV_VAL register	5320 829Ch
2A0h	16	MSS_RCM_ELM_CLK_DIV_VAL	ELM_CLK_DIV_VAL register	5320 82A0h
300h	8	MSS_RCM_MCAN0_CLK_GATE	MCAN0_CLK_GATE register	5320 8300h
304h	8	MSS_RCM_MCAN1_CLK_GATE	MCAN1_CLK_GATE register	5320 8304h
308h	8	MSS_RCM_MCAN2_CLK_GATE	MCAN2_CLK_GATE register	5320 8308h
30Ch	8	MSS_RCM_MCAN3_CLK_GATE	MCAN3_CLK_GATE register	5320 830Ch
310h	8	MSS_RCM_QSPI0_CLK_GATE	QSPI0_CLK_GATE register	5320 8310h
314h	8	MSS_RCM_RTI0_CLK_GATE	RTI0_CLK_GATE register	5320 8314h
318h	8	MSS_RCM_RTI1_CLK_GATE	RTI1_CLK_GATE register	5320 8318h
31Ch	8	MSS_RCM_RTI2_CLK_GATE	RTI2_CLK_GATE register	5320 831Ch
320h	8	MSS_RCM_RTI3_CLK_GATE	RTI3_CLK_GATE register	5320 8320h
328h	8	MSS_RCM_WDT0_CLK_GATE	WDT0_CLK_GATE register	5320 8328h
32Ch	8	MSS_RCM_WDT1_CLK_GATE	WDT1_CLK_GATE register	5320 832Ch
330h	8	MSS_RCM_WDT2_CLK_GATE	WDT2_CLK_GATE register	5320 8330h
334h	8	MSS_RCM_WDT3_CLK_GATE	WDT3_CLK_GATE register	5320 8334h
33Ch	8	MSS_RCM_MCSPI0_CLK_GATE	MCSPI0_CLK_GATE register	5320 833Ch
340h	8	MSS_RCM_MCSPI1_CLK_GATE	MCSPI1_CLK_GATE register	5320 8340h

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Table 2-1008. MSS_RCM Registers Base Address Table (continued)

Offset	Length	Acronym	Register Name	MSS_RCM Physical Address
344h	8	MSS_RCM_MCSPI2_CLK_GATE	MCSPI2_CLK_GATE register	5320 8344h
348h	8	MSS_RCM_MCSPI3_CLK_GATE	MCSPI3_CLK_GATE register	5320 8348h
34Ch	8	MSS_RCM_MCSPI4_CLK_GATE	MCSPI4_CLK_GATE register	5320 834Ch
350h	8	MSS_RCM_MMC0_CLK_GATE	MMC0_CLK_GATE register	5320 8350h
354h	8	MSS_RCM_ICSSM0_UART_CLK_GATE	ICSSM0_UART_CLK_GATE register	5320 8354h
358h	8	MSS_RCM_CPTS_CLK_GATE	CPTS_CLK_GATE register	5320 8358h
35Ch	8	MSS_RCM_GPMC_CLK_GATE	GPMC_CLK_GATE register	5320 835Ch
360h	8	MSS_RCM_CONTROLSS_PLL_CLK_GATE	CONTROLSS_PLL_CLK_GATE register	5320 8360h
364h	8	MSS_RCM_I2C0_CLK_GATE	I2C0_CLK_GATE register	5320 8364h
368h	8	MSS_RCM_I2C1_CLK_GATE	I2C1_CLK_GATE register	5320 8368h
36Ch	8	MSS_RCM_I2C2_CLK_GATE	I2C2_CLK_GATE register	5320 836Ch
370h	8	MSS_RCM_I2C3_CLK_GATE	I2C3_CLK_GATE register	5320 8370h
374h	8	MSS_RCM_LIN0_CLK_GATE	LIN0_CLK_GATE register	5320 8374h
378h	8	MSS_RCM_LIN1_CLK_GATE	LIN1_CLK_GATE register	5320 8378h
37Ch	8	MSS_RCM_LIN2_CLK_GATE	LIN2_CLK_GATE register	5320 837Ch
380h	8	MSS_RCM_LIN3_CLK_GATE	LIN3_CLK_GATE register	5320 8380h
384h	8	MSS_RCM_LIN4_CLK_GATE	LIN4_CLK_GATE register	5320 8384h
38Ch	8	MSS_RCM_UART0_CLK_GATE	UART0_CLK_GATE register	5320 838Ch
390h	8	MSS_RCM_UART1_CLK_GATE	UART1_CLK_GATE register	5320 8390h
394h	8	MSS_RCM_UART2_CLK_GATE	UART2_CLK_GATE register	5320 8394h
398h	8	MSS_RCM_UART3_CLK_GATE	UART3_CLK_GATE register	5320 8398h
39Ch	8	MSS_RCM_UART4_CLK_GATE	UART4_CLK_GATE register	5320 839Ch
3A0h	8	MSS_RCM_UART5_CLK_GATE	UART5_CLK_GATE register	5320 83A0h
3A4h	8	MSS_RCM_RGMII_250_CLK_GATE	RGMII_250_CLK_GATE register	5320 83A4h
3A8h	8	MSS_RCM_RGMII_50_CLK_GATE	RGMII_50_CLK_GATE register	5320 83A8h
3ACh	8	MSS_RCM_RGMII_5_CLK_GATE	RGMII_5_CLK_GATE register	5320 83ACh
3B0h	8	MSS_RCM_MMC0_32K_CLK_GATE	MMC0_32K_CLK_GATE register	5320 83B0h
3B4h	8	MSS_RCM_TEMPSENSE_32K_CLK_GATE	TEMPSENSE_32K_CLK_GATE register	5320 83B4h
3B8h	8	MSS_RCM_CPSW_CLK_GATE	CPSW_CLK_GATE register	5320 83B8h
3BCh	8	MSS_RCM_ICSSM0_IEP_CLK_GATE	ICSSM0_IEP_CLK_GATE register	5320 83BCh
3C0h	8	MSS_RCM_ICSSM0_CORE_CLK_GATE	ICSSM0_CORE_CLK_GATE register	5320 83C0h
3C4h	8	MSS_RCM_ICSSM_SYS_CLK_GATE	ICSSM_SYS_CLK_GATE register	5320 83C4h
3C8h	8	MSS_RCM_ELM_CLK_GATE	ELM_CLK_GATE register	5320 83C8h
3CCh	8	MSS_RCM_R5SS0_CORE0_GATE	R5SS0_CORE0_GATE register	5320 83CCh
3D0h	8	MSS_RCM_R5SS1_CORE0_GATE	R5SS1_CORE0_GATE register	5320 83D0h
3D4h	8	MSS_RCM_R5SS0_CORE1_GATE	R5SS0_CORE1_GATE register	5320 83D4h
3D8h	8	MSS_RCM_R5SS1_CORE1_GATE	R5SS1_CORE1_GATE register	5320 83D8h
400h	16	MSS_RCM_MCAN0_CLK_STATUS	MCAN0_CLK_STATUS register	5320 8400h
404h	16	MSS_RCM_MCAN1_CLK_STATUS	MCAN1_CLK_STATUS register	5320 8404h
408h	16	MSS_RCM_MCAN2_CLK_STATUS	MCAN2_CLK_STATUS register	5320 8408h
40Ch	16	MSS_RCM_MCAN3_CLK_STATUS	MCAN3_CLK_STATUS register	5320 840Ch
410h	16	MSS_RCM_QSPI0_CLK_STATUS	QSPI0_CLK_STATUS register	5320 8410h
414h	16	MSS_RCM_RTI0_CLK_STATUS	RTI0_CLK_STATUS register	5320 8414h

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Table 2-1008. MSS_RCM Registers Base Address Table (continued)

Offset	Length	Acronym	Register Name	MSS_RCM Physical Address
418h	16	MSS_RCM_RTI1_CLK_STATUS	RTI1_CLK_STATUS register	5320 8418h
41Ch	16	MSS_RCM_RTI2_CLK_STATUS	RTI2_CLK_STATUS register	5320 841Ch
420h	16	MSS_RCM_RTI3_CLK_STATUS	RTI3_CLK_STATUS register	5320 8420h
428h	16	MSS_RCM_WDT0_CLK_STATUS	WDT0_CLK_STATUS register	5320 8428h
42Ch	16	MSS_RCM_WDT1_CLK_STATUS	WDT1_CLK_STATUS register	5320 842Ch
430h	16	MSS_RCM_WDT2_CLK_STATUS	WDT2_CLK_STATUS register	5320 8430h
434h	16	MSS_RCM_WDT3_CLK_STATUS	WDT3_CLK_STATUS register	5320 8434h
43Ch	16	MSS_RCM_MCSPI0_CLK_STATUS	MCSPI0_CLK_STATUS register	5320 843Ch
440h	16	MSS_RCM_MCSPI1_CLK_STATUS	MCSPI1_CLK_STATUS register	5320 8440h
444h	16	MSS_RCM_MCSPI2_CLK_STATUS	MCSPI2_CLK_STATUS register	5320 8444h
448h	16	MSS_RCM_MCSPI3_CLK_STATUS	MCSPI3_CLK_STATUS register	5320 8448h
44Ch	16	MSS_RCM_MCSPI4_CLK_STATUS	MCSPI4_CLK_STATUS register	5320 844Ch
450h	16	MSS_RCM_MMC0_CLK_STATUS	MMC0_CLK_STATUS register	5320 8450h
454h	16	MSS_RCM_ICSSM0_UART_CLK_STATUS	ICSSM0_UART_CLK_STATUS register	5320 8454h
458h	16	MSS_RCM_CPTS_CLK_STATUS	CPTS_CLK_STATUS register	5320 8458h
45Ch	16	MSS_RCM_GPMC_CLK_STATUS	GPMC_CLK_STATUS register	5320 845Ch
460h	16	MSS_RCM_CONTROLSS_PLL_CLK_STATUS	CONTROLSS_PLL_CLK_STATUS register	5320 8460h
464h	16	MSS_RCM_I2C_CLK_STATUS	I2C_CLK_STATUS register	5320 8464h
474h	16	MSS_RCM_LIN0_UART0_CLK_STATUS	LIN0_UART0_CLK_STATUS register	5320 8474h
478h	16	MSS_RCM_LIN1_UART1_CLK_STATUS	LIN1_UART1_CLK_STATUS register	5320 8478h
47Ch	16	MSS_RCM_LIN2_UART2_CLK_STATUS	LIN2_UART2_CLK_STATUS register	5320 847Ch
480h	16	MSS_RCM_LIN3_UART3_CLK_STATUS	LIN3_UART3_CLK_STATUS register	5320 8480h
484h	16	MSS_RCM_LIN4_UART4_CLK_STATUS	LIN4_UART4_CLK_STATUS register	5320 8484h
488h	16	MSS_RCM_LIN5_UART5_CLK_STATUS	LIN5_UART5_CLK_STATUS register	5320 8488h
48Ch	16	MSS_RCM_RGMII_250_CLK_STATUS	RGMII_250_CLK_STATUS register	5320 848Ch
490h	16	MSS_RCM_RGMII_50_CLK_STATUS	RGMII_50_CLK_STATUS register	5320 8490h
494h	16	MSS_RCM_RGMII_5_CLK_STATUS	RGMII_5_CLK_STATUS register	5320 8494h
49Ch	24	MSS_RCM_MMC0_32K_CLK_STATUS	MMC0_32K_CLK_STATUS register	5320 849Ch
4A0h	24	MSS_RCM_TEMPSENSE_32K_CLK_STATUS	TEMPSENSE_32K_CLK_STATUS register	5320 84A0h
4A4h	16	MSS_RCM_ELM_CLK_STATUS	ELM_CLK_STATUS register	5320 84A4h
500h	8	MSS_RCM_R5SS0_POR_RST_CTRL	R5SS0_POR_RST_CTRL register	5320 8500h
504h	8	MSS_RCM_R5SS1_POR_RST_CTRL	R5SS1_POR_RST_CTRL register	5320 8504h
508h	8	MSS_RCM_R5SS0_CORE0_GRST_CTRL	R5SS0_CORE0_GRST_CTRL register	5320 8508h
50Ch	8	MSS_RCM_R5SS1_CORE0_GRST_CTRL	R5SS1_CORE0_GRST_CTRL register	5320 850Ch
510h	8	MSS_RCM_R5SS0_CORE1_GRST_CTRL	R5SS0_CORE1_GRST_CTRL register	5320 8510h

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Table 2-1008. MSS_RCM Registers Base Address Table (continued)

Offset	Length	Acronym	Register Name	MSS_RCM Physical Address
514h	8	MSS_RCM_R5SS1_CORE1_GRST_CTRL	R5SS1_CORE1_GRST_CTRL register	5320 8514h
518h	8	MSS_RCM_R5SS0_CORE0_LRST_CTRL	R5SS0_CORE0_LRST_CTRL register	5320 8518h
51Ch	8	MSS_RCM_R5SS1_CORE0_LRST_CTRL	R5SS1_CORE0_LRST_CTRL register	5320 851Ch
520h	8	MSS_RCM_R5SS0_CORE1_LRST_CTRL	R5SS0_CORE1_LRST_CTRL register	5320 8520h
524h	8	MSS_RCM_R5SS1_CORE1_LRST_CTRL	R5SS1_CORE1_LRST_CTRL register	5320 8524h
528h	8	MSS_RCM_R5SS0_VIM0_RST_CTRL	R5SS0_VIM0_RST_CTRL register	5320 8528h
52Ch	8	MSS_RCM_R5SS1_VIM0_RST_CTRL	R5SS1_VIM0_RST_CTRL register	5320 852Ch
530h	8	MSS_RCM_R5SS0_VIM1_RST_CTRL	R5SS0_VIM1_RST_CTRL register	5320 8530h
534h	8	MSS_RCM_R5SS1_VIM1_RST_CTRL	R5SS1_VIM1_RST_CTRL register	5320 8534h
538h	8	MSS_RCM_MCRC0_RST_CTRL	MCRC0_RST_CTRL register	5320 8538h
53Ch	8	MSS_RCM_RTI0_RST_CTRL	RTI0_RST_CTRL register	5320 853Ch
540h	8	MSS_RCM_RTI1_RST_CTRL	RTI1_RST_CTRL register	5320 8540h
544h	8	MSS_RCM_RTI2_RST_CTRL	RTI2_RST_CTRL register	5320 8544h
548h	8	MSS_RCM_RTI3_RST_CTRL	RTI3_RST_CTRL register	5320 8548h
54Ch	8	MSS_RCM_WDT0_RST_CTRL	WDT0_RST_CTRL register	5320 854Ch
550h	8	MSS_RCM_WDT1_RST_CTRL	WDT1_RST_CTRL register	5320 8550h
554h	8	MSS_RCM_WDT2_RST_CTRL	WDT2_RST_CTRL register	5320 8554h
558h	8	MSS_RCM_WDT3_RST_CTRL	WDT3_RST_CTRL register	5320 8558h
55Ch	8	MSS_RCM_TOP_ESM_RST_CTRL	TOP_ESM_RST_CTRL register	5320 855Ch
560h	8	MSS_RCM_DCC0_RST_CTRL	DCC0_RST_CTRL register	5320 8560h
564h	8	MSS_RCM_DCC1_RST_CTRL	DCC1_RST_CTRL register	5320 8564h
568h	8	MSS_RCM_DCC2_RST_CTRL	DCC2_RST_CTRL register	5320 8568h
56Ch	8	MSS_RCM_DCC3_RST_CTRL	DCC3_RST_CTRL register	5320 856Ch
570h	8	MSS_RCM_MCSPI0_RST_CTRL	MCSPI0_RST_CTRL register	5320 8570h
574h	8	MSS_RCM_MCSPI1_RST_CTRL	MCSPI1_RST_CTRL register	5320 8574h
578h	8	MSS_RCM_MCSPI2_RST_CTRL	MCSPI2_RST_CTRL register	5320 8578h
57Ch	8	MSS_RCM_MCSPI3_RST_CTRL	MCSPI3_RST_CTRL register	5320 857Ch
580h	8	MSS_RCM_MCSPI4_RST_CTRL	MCSPI4_RST_CTRL register	5320 8580h
584h	8	MSS_RCM_QSPI0_RST_CTRL	QSPI0_RST_CTRL register	5320 8584h
588h	8	MSS_RCM_MCAN0_RST_CTRL	MCAN0_RST_CTRL register	5320 8588h
58Ch	8	MSS_RCM_MCAN1_RST_CTRL	MCAN1_RST_CTRL register	5320 858Ch
590h	8	MSS_RCM_MCAN2_RST_CTRL	MCAN2_RST_CTRL register	5320 8590h
594h	8	MSS_RCM_MCAN3_RST_CTRL	MCAN3_RST_CTRL register	5320 8594h
598h	8	MSS_RCM_I2C0_RST_CTRL	I2C0_RST_CTRL register	5320 8598h
59Ch	8	MSS_RCM_I2C1_RST_CTRL	I2C1_RST_CTRL register	5320 859Ch
5A0h	8	MSS_RCM_I2C2_RST_CTRL	I2C2_RST_CTRL register	5320 85A0h
5A4h	8	MSS_RCM_I2C3_RST_CTRL	I2C3_RST_CTRL register	5320 85A4h
5A8h	8	MSS_RCM_UART0_RST_CTRL	UART0_RST_CTRL register	5320 85A8h
5ACh	8	MSS_RCM_UART1_RST_CTRL	UART1_RST_CTRL register	5320 85ACh
5B0h	8	MSS_RCM_UART2_RST_CTRL	UART2_RST_CTRL register	5320 85B0h

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Table 2-1008. MSS_RCM Registers Base Address Table (continued)

Offset	Length	Acronym	Register Name	MSS_RCM Physical Address
5B4h	8	MSS_RCM_UART3_RST_CTRL	UART3_RST_CTRL register	5320 85B4h
5B8h	8	MSS_RCM_UART4_RST_CTRL	UART4_RST_CTRL register	5320 85B8h
5BCh	8	MSS_RCM_UART5_RST_CTRL	UART5_RST_CTRL register	5320 85BCh
5C0h	8	MSS_RCM_LIN0_RST_CTRL	LIN0_RST_CTRL register	5320 85C0h
5C4h	8	MSS_RCM_LIN1_RST_CTRL	LIN1_RST_CTRL register	5320 85C4h
5C8h	8	MSS_RCM_LIN2_RST_CTRL	LIN2_RST_CTRL register	5320 85C8h
5CCh	8	MSS_RCM_LIN3_RST_CTRL	LIN3_RST_CTRL register	5320 85CCh
5D0h	8	MSS_RCM_LIN4_RST_CTRL	LIN4_RST_CTRL register	5320 85D0h
5D8h	16	MSS_RCM_EDMA_RST_CTRL	EDMA_RST_CTRL register	5320 85D8h
5DCh	8	MSS_RCM_INFRA_RST_CTRL	INFRA_RST_CTRL register	5320 85DCh
5E0h	8	MSS_RCM_CPSW_RST_CTRL	CPSW_RST_CTRL register	5320 85E0h
5E4h	8	MSS_RCM_ICSSM0_RST_CTRL	ICSSM0_RST_CTRL register	5320 85E4h
5E8h	8	MSS_RCM_MMC0_RST_CTRL	MMC0_RST_CTRL register	5320 85E8h
5ECh	8	MSS_RCM_GPIO0_RST_CTRL	GPIO0_RST_CTRL register	5320 85ECh
5F0h	8	MSS_RCM_GPIO1_RST_CTRL	GPIO1_RST_CTRL register	5320 85F0h
5F4h	8	MSS_RCM_GPIO2_RST_CTRL	GPIO2_RST_CTRL register	5320 85F4h
5F8h	8	MSS_RCM_GPIO3_RST_CTRL	GPIO3_RST_CTRL register	5320 85F8h
5FCh	8	MSS_RCM_SPINLOCK0_RST_CTRL	SPINLOCK0_RST_CTRL register	5320 85FCh
600h	8	MSS_RCM_GPMC_RST_CTRL	GPMC_RST_CTRL register	5320 8600h
604h	8	MSS_RCM_TEMPSENSE_32K_RST_CTRL	TEMPSENSE_32K_RST_CTRL register	5320 8604h
608h	8	MSS_RCM_ELM_RST_CTRL	ELM_RST_CTRL register	5320 8608h
700h	16	MSS_RCM_L2OCRAM_BANK0_PD_CTRL	L2OCRAM_BANK0_PD_CTRL register	5320 8700h
704h	16	MSS_RCM_L2OCRAM_BANK1_PD_CTRL	L2OCRAM_BANK1_PD_CTRL register	5320 8704h
708h	16	MSS_RCM_L2OCRAM_BANK2_PD_CTRL	L2OCRAM_BANK2_PD_CTRL register	5320 8708h
70Ch	16	MSS_RCM_L2OCRAM_BANK3_PD_CTRL	L2OCRAM_BANK3_PD_CTRL register	5320 870Ch
710h	8	MSS_RCM_L2OCRAM_BANK0_PD_STATUS	L2OCRAM_BANK0_PD_STATUS register	5320 8710h
714h	8	MSS_RCM_L2OCRAM_BANK1_PD_STATUS	L2OCRAM_BANK1_PD_STATUS register	5320 8714h
718h	8	MSS_RCM_L2OCRAM_BANK2_PD_STATUS	L2OCRAM_BANK2_PD_STATUS register	5320 8718h
71Ch	8	MSS_RCM_L2OCRAM_BANK3_PD_STATUS	L2OCRAM_BANK3_PD_STATUS register	5320 871Ch
800h	16	MSS_RCM_HSM_RTIA_CLK_SRC_SEL	HSM_RTIA_CLK_SRC_SEL register	5320 8800h
804h	16	MSS_RCM_HSM_WDT_CLK_SRC_SEL	HSM_WDT_CLK_SRC_SEL register	5320 8804h
808h	16	MSS_RCM_HSM_RTC_CLK_SRC_SEL	HSM_RTC_CLK_SRC_SEL register	5320 8808h
80Ch	16	MSS_RCM_HSM_DMTA_CLK_SRC_SEL	HSM_DMTA_CLK_SRC_SEL register	5320 880Ch
810h	16	MSS_RCM_HSM_DMTB_CLK_SRC_SEL	HSM_DMTB_CLK_SRC_SEL register	5320 8810h
814h	16	MSS_RCM_HSM_RTI_CLK_DIV_VAL	HSM_RTI_CLK_DIV_VAL register	5320 8814h
818h	16	MSS_RCM_HSM_WDT_CLK_DIV_VAL	HSM_WDT_CLK_DIV_VAL register	5320 8818h

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Table 2-1008. MSS_RCM Registers Base Address Table (continued)

Offset	Length	Acronym	Register Name	MSS_RCM Physical Address
81Ch	16	MSS_RCM_HSM_RTC_CLK_DIV_VAL	HSM_RTC_CLK_DIV_VAL register	5320 881Ch
820h	16	MSS_RCM_HSM_DMTA_CLK_DIV_VAL	HSM_DMTA_CLK_DIV_VAL register	5320 8820h
824h	16	MSS_RCM_HSM_DMTB_CLK_DIV_VAL	HSM_DMTB_CLK_DIV_VAL register	5320 8824h
828h	8	MSS_RCM_HSM_RTI_CLK_GATE	HSM_RTI_CLK_GATE register	5320 8828h
82Ch	8	MSS_RCM_HSM_WDT_CLK_GATE	HSM_WDT_CLK_GATE register	5320 882Ch
830h	8	MSS_RCM_HSM_RTC_CLK_GATE	HSM_RTC_CLK_GATE register	5320 8830h
834h	8	MSS_RCM_HSM_DMTA_CLK_GATE	HSM_DMTA_CLK_GATE register	5320 8834h
838h	8	MSS_RCM_HSM_DMTB_CLK_GATE	HSM_DMTB_CLK_GATE register	5320 8838h
83Ch	16	MSS_RCM_HSM_RTI_CLK_STATUS	HSM_RTI_CLK_STATUS register	5320 883Ch
840h	16	MSS_RCM_HSM_WDT_CLK_STATUS	HSM_WDT_CLK_STATUS register	5320 8840h
844h	16	MSS_RCM_HSM_RTC_CLK_STATUS	HSM_RTC_CLK_STATUS register	5320 8844h
848h	16	MSS_RCM_HSM_DMTA_CLK_STATUS	HSM_DMTA_CLK_STATUS register	5320 8848h
84Ch	16	MSS_RCM_HSM_DMTB_CLK_STATUS	HSM_DMTB_CLK_STATUS register	5320 884Ch
1008h	32	MSS_RCM_LOCK0_KICK0	- KICK0 component	5320 9008h
100Ch	32	MSS_RCM_LOCK0_KICK1	- KICK1 component	5320 900Ch
1010h	8	MSS_RCM_INTR_RAW_STATUS	Interrupt Raw Status/Set Register	5320 9010h
1014h	8	MSS_RCM_INTR_ENABLED_STATUS_CLEAR	Interrupt Enabled Status/Clear register	5320 9014h
1018h	8	MSS_RCM_INTR_ENABLE	Interrupt Enable register	5320 9018h
101Ch	8	MSS_RCM_INTR_ENABLE_CLEAR	Interrupt Enable Clear register	5320 901Ch
1020h	8	MSS_RCM_EOI	EOI register	5320 9020h
1024h	32	MSS_RCM_FAULT_ADDRESS	Fault Address register	5320 9024h
1028h	8	MSS_RCM_FAULT_TYPE_STATUS	Fault Type Status register	5320 9028h
102Ch	32	MSS_RCM_FAULT_ATTR_STATUS	Fault Attribute Status register	5320 902Ch
1030h	0	MSS_RCM_FAULT_CLEAR	Fault Clear register	5320 9030h

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2.6.1 MSS_RCM_MSS_RCM_PID Registers

2.6.1.1 MSS_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

Return to Summary Table

Table 2-1009. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8000h

Access Types Legend

Table 2-1010. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	640B657B5780h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	Ah	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	2774h	Not Defined

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2.6.2 MSS_RCM_MSS_RCM_R5SS0_RST_STATUS Registers

2.6.2.1 MSS_R5SS0_RST_STATUS Register (Offset = 10h) [reset = h]

Short Description: R5SS0_RST_STATUS register

Long Description:

Return to Summary Table

Table 2-1011. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8010h

Access Types Legend

Table 2-1012. R5SS0_RST_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 0	CAUSE	RO	Bh	Reset Cause Status#br#Bit0: POR Reset#br#Bit1: Warm Reset (Also set during POR Reset)#br#Bit2: CR5SS0 STC Reset#br#Bit3: Reset for CORE0 and MSS_CORE00_VIM using MSS_RCM::MSS_CR5SSA0_RST_CTRL#br#Bit4: Reset for CORE1 and MSS_CORE10_VIM using MSS_RCM::MSS_CR5SSB0_RST_CTRL#br#Bit5: Reset for CORE0 only using MSS_RCM::MSS_CORE00_RST_CTRL#br#Bit6: Reset for CORE1 only using using MSS_RCM::MSS_CORE10_RST_CTRL#br#Bit7: Reset for CORE0 and MSS_CORE0_VIM caused because of reset request by debugger in CORE0#br#Bit8: Reset for CORE10 and MSS_CORE10_VIM caused because of reset request by debugger in CORE10#br#Bit9: Reset for CR5SS0 by the RESET FSM using MSS_CTRL::R5SS0_CONTROL_RESET_FSM_TRIGGER#br#Bit 10 : MSS_RCM.MSS_CR5SS_POR_RST_CTRL0

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2.6.3 MSS_RCM_MSS_RCM_R5SS0_RST_CAUSE_CLR Registers

2.6.3.1 MSS_R5SS0_RST_CAUSE_CLR Register (Offset = 14h) [reset = h]

Short Description: R5SS0_RST_CAUSE_CLR register

Long Description:

Return to Summary Table

Table 2-1013. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8014h

Access Types Legend

Table 2-1014. R5SS0_RST_CAUSE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLR	RW	0h	Write pulse bit field:Clear bit for rst cause register (Writing 3'b111 will clear the rst cause register)

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2.6.4 MSS_RCM_MSS_RCM_R5SS0_DBG_RST_EN Registers

2.6.4.1 MSS_R5SS0_DBG_RST_EN Register (Offset = 18h) [reset = h]

Short Description: R5SS0_DBG_RST_EN register

Long Description:

Return to Summary Table

Table 2-1015. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8018h

Access Types Legend

Table 2-1016. R5SS0_DBG_RST_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
18 - 16	EN_CORE1	RW	0h	Writing 3'b111 will block debug reset request from CORE1 toggling reset for CORE1 of respective R5SS
	RESERVED	NONE		Reserved
2 - 0	EN_CORE0	RW	0h	Writing 3'b111 will block debug reset request from CORE0 toggling reset for CORE0 of respective R5SS

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2.6.5 MSS_RCM_MSS_RCM_R5SS0_RST_ASSERDLY Registers

2.6.5.1 MSS_R5SS0_RST_ASSERDLY Register (Offset = 1Ch) [reset = h]

Short Description: R5SS0_RST_ASSERDLY register

Long Description:

Return to Summary Table

Table 2-1017. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 801Ch

Access Types Legend

Table 2-1018. R5SS0_RST_ASSERDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	COUNT	RW	457h	Value decides number of cycles reset should be kept asserted for CR5SS related resets. Programming a value of 0xFF will keep the reset asserted untill a new value other than 0xFF is written to this registerThe actual duration is count + 2 cycles. S/W Recommended value for this is 0x0FThe COUNT is applicable to both CPU cores

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2.6.6 MSS_RCM_MSS_RCM_R5SS0_RST2ASSERTDLY Registers

2.6.6.1 MSS_R5SS0_RST2ASSERTDLY Register (Offset = 20h) [reset = h]

Short Description: R5SS0_RST2ASSERTDLY register

Long Description:

Return to Summary Table

Table 2-1019. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8020h

Access Types Legend

Table 2-1020. R5SS0_RST2ASSERTDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	R5_CORE1_COUNT	RW	0h	Value decides number of cycles to wait before asserting reset for local reset for CORE1
23 - 16	R5_CORE0_COUNT	RW	0h	Value decides number of cycles to wait before asserting reset for local reset for CORE0.
15 - 8	R5SS_CORE1_COUNT	RW	0h	Value decides number of cycles to wait before asserting reset for global reset for CORE1
7 - 0	R5SS_CORE0_COUNT	RW	0h	Value decides number of cycles to wait before asserting reset for global reset for CORE0.

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2.6.7 MSS_RCM_MSS_RCM_R5SS0_RST_WFICHECK Registers

2.6.7.1 MSS_R5SS0_RST_WFICHECK Register (Offset = 24h) [reset = h]

Short Description: R5SS0_RST_WFICHECK register

Long Description:

Return to Summary Table

Table 2-1021. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8024h

Access Types Legend

Table 2-1022. R5SS0_RST_WFICHECK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
26 - 24	EN_R5_CORE1	RW	6Fh	Writing 3'b000 will disable check for WFI before local reset assertion of CORE0
	RESERVED	NONE		Reserved
18 - 16	EN_R5_CORE0	RW	6Fh	Writing 3'b000 will disable check for WFI before local reset assertion of CORE0
	RESERVED	NONE		Reserved
10 - 8	EN_R5SS_CORE1	RW	6Fh	Writing 3'b000 will disable check for WFI before global reset assertion of CORE1
	RESERVED	NONE		Reserved
2 - 0	EN_R5SS_CORE0	RW	6Fh	Writing 3'b000 will disable check for WFI before global reset assertion of CORE0

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2.6.8 MSS_RCM_MSS_RCM_R5SS1_RST_STATUS Registers

2.6.8.1 MSS_R5SS1_RST_STATUS Register (Offset = 30h) [reset = h]

Short Description: R5SS1_RST_STATUS register

Long Description:

Return to Summary Table

Table 2-1023. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8030h

Access Types Legend

Table 2-1024. R5SS1_RST_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 0	CAUSE	RO	Bh	Has the status because of which reset has happened. Bit0: POR ResetBit1: Warm Reset (ALso set during POR Reset)Bit2: CR5SS1 STC ResetBit3 Reset for CORE0 and MSS_CORE00_VIM using MSS_RCM::MSS_CR5SSA0_RST_CTRLBit4: Reset for CORE1 and MSS_CORE10_VIM using MSS_RCM::MSS_CR5SSB0_RST_CTRLBit5: Reset for CORE0 only using MSS_RCM::MSS_CORE00_RST_CTRLBit6: Reset for CORE1 only using using MSS_RCM::MSS_CORE10_RST_CTRLBit7: Reset for CORE0 and MSS_CORE00_VIM caused because of reset request by debugger in CORE00 Bit8: Reset for CORE10 and MSS_CORE10_VIM caused because of reset request by debugger in CORE10Bit9: Reset for CR5SS0 by the RESET FSM using MSS_CTRL::R5SS0_CONTROL_RESET_FSM_TRIGGER Bit 10 : MSS_RCM.MSS_CR5SS_POR_RST_CTRL0

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2.6.9 MSS_RCM_MSS_RCM_R5SS1_RST_CAUSE_CLR Registers

2.6.9.1 MSS_R5SS1_RST_CAUSE_CLR Register (Offset = 34h) [reset = h]

Short Description: R5SS1_RST_CAUSE_CLR register

Long Description:

Return to Summary Table

Table 2-1025. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8034h

Access Types Legend

Table 2-1026. R5SS1_RST_CAUSE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLR	RW	0h	Write pulse bit field:Clear bit for rst cause register (Writing 3'b111 will clear the rst cause register)

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2.6.10 MSS_RCM_MSS_RCM_R5SS1_DBG_RST_EN Registers

2.6.10.1 MSS_R5SS1_DBG_RST_EN Register (Offset = 38h) [reset = h]

Short Description: R5SS1_DBG_RST_EN register

Long Description:

Return to Summary Table

Table 2-1027. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8038h

Access Types Legend

Table 2-1028. R5SS1_DBG_RST_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
18 - 16	EN_CORE1	RW	0h	Writing 3'b111 will block debug reset request from CORE1 toggling reset for CORE1 of respective R5SS
	RESERVED	NONE		Reserved
2 - 0	EN_CORE0	RW	0h	Writing 3'b111 will block debug reset request from CORE0 toggling reset for CORE0 of respective R5SS

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2.6.11 MSS_RCM_MSS_RCM_R5SS1_RST_ASSERDLY Registers

2.6.11.1 MSS_R5SS1_RST_ASSERDLY Register (Offset = 3Ch) [reset = h]

Short Description: R5SS1_RST_ASSERDLY register

Long Description:

Return to Summary Table

Table 2-1029. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 803Ch

Access Types Legend

Table 2-1030. R5SS1_RST_ASSERDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	COUNT	RW	457h	Value decides number of cycles reset should be kept asserted for CR5SS related resets. Programming a value of 0xFF will keep the reset asserted untill a new value other than 0xFF is written to this registerThe actual duration is count + 2 cycles. S/W Recommended value for this is 0x0FThe COUNT is applicable to both CPU cores

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2.6.12 MSS_RCM_MSS_RCM_R5SS1_RST2ASSERTDLY Registers

2.6.12.1 MSS_R5SS1_RST2ASSERTDLY Register (Offset = 40h) [reset = h]

Short Description: R5SS1_RST2ASSERTDLY register

Long Description:

Return to Summary Table

Table 2-1031. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8040h

Access Types Legend

Table 2-1032. R5SS1_RST2ASSERTDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	R5_CORE1_COUNT	RW	0h	Value decides number of cycles to wait before asserting reset for local reset for CORE1
23 - 16	R5_CORE0_COUNT	RW	0h	Value decides number of cycles to wait before asserting reset for local reset for CORE0.
15 - 8	R5SS_CORE1_COUNT	RW	0h	Value decides number of cycles to wait before asserting reset for global reset for CORE1
7 - 0	R5SS_CORE0_COUNT	RW	0h	Value decides number of cycles to wait before asserting reset for global reset for CORE0.

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2.6.13 MSS_RCM_MSS_RCM_R5SS1_RST_WFICHECK Registers

2.6.13.1 MSS_R5SS1_RST_WFICHECK Register (Offset = 44h) [reset = h]

Short Description: R5SS1_RST_WFICHECK register

Long Description:

Return to Summary Table

Table 2-1033. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8044h

Access Types Legend

Table 2-1034. R5SS1_RST_WFICHECK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
26 - 24	EN_R5_CORE1	RW	6Fh	Writing 3'b000 will disable check for WFI before local reset assertion of CORE0
	RESERVED	NONE		Reserved
18 - 16	EN_R5_CORE0	RW	6Fh	Writing 3'b000 will disable check for WFI before local reset assertion of CORE0
	RESERVED	NONE		Reserved
10 - 8	EN_R5SS_CORE1	RW	6Fh	Writing 3'b000 will disable check for WFI before global reset assertion of CORE1
	RESERVED	NONE		Reserved
2 - 0	EN_R5SS_CORE0	RW	6Fh	Writing 3'b000 will disable check for WFI before global reset assertion of CORE0

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2.6.14 MSS_RCM_MSS_RCM_MCAN0_CLK_SRC_SEL Registers

2.6.14.1 MSS_MCAN0_CLK_SRC_SEL Register (Offset = 100h) [reset = h]

Short Description: MCAN0_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1035. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8100h

Access Types Legend

Table 2-1036. MCAN0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.15 MSS_RCM_MSS_RCM_MCAN1_CLK_SRC_SEL Registers

2.6.15.1 MSS_MCAN1_CLK_SRC_SEL Register (Offset = 104h) [reset = h]

Short Description: MCAN1_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1037. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8104h

Access Types Legend

Table 2-1038. MCAN1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.16 MSS_RCM_MSS_RCM_MCAN2_CLK_SRC_SEL Registers

2.6.16.1 MSS_MCAN2_CLK_SRC_SEL Register (Offset = 108h) [reset = h]

Short Description: MCAN2_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1039. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8108h

Access Types Legend

Table 2-1040. MCAN2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.17 MSS_RCM_MSS_RCM_MCAN3_CLK_SRC_SEL Registers

2.6.17.1 MSS_MCAN3_CLK_SRC_SEL Register (Offset = 10Ch) [reset = h]

Short Description: MCAN3_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1041. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 810Ch

Access Types Legend

Table 2-1042. MCAN3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding MCAN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.18 MSS_RCM_MSS_RCM_QSPI0_CLK_SRC_SEL Registers

2.6.18.1 MSS_QSPI0_CLK_SRC_SEL Register (Offset = 110h) [reset = h]

Short Description: QSPI0_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1043. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8110h

Access Types Legend

Table 2-1044. QSPI0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for QSPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.19 MSS_RCM_MSS_RCM_RTI0_CLK_SRC_SEL Registers

2.6.19.1 MSS_RTI0_CLK_SRC_SEL Register (Offset = 114h) [reset = h]

Short Description: RTI0_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1045. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8114h

Access Types Legend

Table 2-1046. RTI0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.20 MSS_RCM_MSS_RCM_RTI1_CLK_SRC_SEL Registers

2.6.20.1 MSS_RTI1_CLK_SRC_SEL Register (Offset = 118h) [reset = h]

Short Description: RTI1_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1047. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8118h

Access Types Legend

Table 2-1048. RTI1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.21 MSS_RCM_MSS_RCM_RTI2_CLK_SRC_SEL Registers

2.6.21.1 MSS_RTI2_CLK_SRC_SEL Register (Offset = 11Ch) [reset = h]

Short Description: RTI2_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1049. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 811Ch

Access Types Legend

Table 2-1050. RTI2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.22 MSS_RCM_MSS_RCM_RTI3_CLK_SRC_SEL Registers

2.6.22.1 MSS_RTI3_CLK_SRC_SEL Register (Offset = 120h) [reset = h]

Short Description: RTI3_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1051. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8120h

Access Types Legend

Table 2-1052. RTI3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.23 MSS_RCM_MSS_RCM_WDT0_CLK_SRC_SEL Registers

2.6.23.1 MSS_WDT0_CLK_SRC_SEL Register (Offset = 128h) [reset = h]

Short Description: WDT0_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1053. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8128h

Access Types Legend

Table 2-1054. WDT0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for WDT.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.24 MSS_RCM_MSS_RCM_WDT1_CLK_SRC_SEL Registers

2.6.24.1 MSS_WDT1_CLK_SRC_SEL Register (Offset = 12Ch) [reset = h]

Short Description: WDT1_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1055. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 812Ch

Access Types Legend

Table 2-1056. WDT1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for WDT.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.25 MSS_RCM_MSS_RCM_WDT2_CLK_SRC_SEL Registers

2.6.25.1 MSS_WDT2_CLK_SRC_SEL Register (Offset = 130h) [reset = h]

Short Description: WDT2_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1057. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8130h

Access Types Legend

Table 2-1058. WDT2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for WDT.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.26 MSS_RCM_MSS_RCM_WDT3_CLK_SRC_SEL Registers

2.6.26.1 MSS_WDT3_CLK_SRC_SEL Register (Offset = 134h) [reset = h]

Short Description: WDT3_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1059. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8134h

Access Types Legend

Table 2-1060. WDT3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for WDT.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.27 MSS_RCM_MSS_RCM_MCSPI0_CLK_SRC_SEL Registers

2.6.27.1 MSS_MCSPI0_CLK_SRC_SEL Register (Offset = 13Ch) [reset = h]

Short Description: MCSPI0_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1061. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 813Ch

Access Types Legend

Table 2-1062. MCSPI0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.28 MSS_RCM_MSS_RCM_MCSPI1_CLK_SRC_SEL Registers

2.6.28.1 MSS_MCSPI1_CLK_SRC_SEL Register (Offset = 140h) [reset = h]

Short Description: MCSPI1_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1063. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8140h

Access Types Legend

Table 2-1064. MCSPI1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.29 MSS_RCM_MSS_RCM_MCSPI2_CLK_SRC_SEL Registers

2.6.29.1 MSS_MCSPI2_CLK_SRC_SEL Register (Offset = 144h) [reset = h]

Short Description: MCSPI2_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1065. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8144h

Access Types Legend

Table 2-1066. MCSPI2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.30 MSS_RCM_MSS_RCM_MCSPI3_CLK_SRC_SEL Registers

2.6.30.1 MSS_MCSPI3_CLK_SRC_SEL Register (Offset = 148h) [reset = h]

Short Description: MCSPI3_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1067. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8148h

Access Types Legend

Table 2-1068. MCSPI3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.31 MSS_RCM_MSS_RCM_MCSPI4_CLK_SRC_SEL Registers

2.6.31.1 MSS_MCSPI4_CLK_SRC_SEL Register (Offset = 14Ch) [reset = h]

Short Description: MCSPI4_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1069. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 814Ch

Access Types Legend

Table 2-1070. MCSPI4_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for Corresponding SPI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.32 MSS_RCM_MSS_RCM_MMC0_CLK_SRC_SEL Registers

2.6.32.1 MSS_MMC0_CLK_SRC_SEL Register (Offset = 150h) [reset = h]

Short Description: MMC0_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1071. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8150h

Access Types Legend

Table 2-1072. MMC0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for MMCSD.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.33 MSS_RCM_MSS_RCM_ICSSM0_UART0_CLK_SRC_SEL Registers

2.6.33.1 MSS_ICSSM0_UART0_CLK_SRC_SEL Register (Offset = 154h) [reset = h]

Short Description: ICSSM0_UART0_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1073. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8154h

Access Types Legend

Table 2-1074. ICSSM0_UART0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for ICSSM_UCLK.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.34 MSS_RCM_MSS_RCM_CPTS_CLK_SRC_SEL Registers

2.6.34.1 MSS_CPTS_CLK_SRC_SEL Register (Offset = 158h) [reset = h]

Short Description: CPTS_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1075. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8158h

Access Types Legend

Table 2-1076. CPTS_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for CPTS.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.35 MSS_RCM_MSS_RCM_GPMC_CLK_SRC_SEL Registers

2.6.35.1 MSS_GPMC_CLK_SRC_SEL Register (Offset = 15Ch) [reset = h]

Short Description: GPMC_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1077. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 815Ch

Access Types Legend

Table 2-1078. GPMC_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	GPMC_CLK_SRC_SEL	RW	0h	Select line for selecting source clock for GPMC. Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.36 MSS_RCM_MSS_RCM_CONTROLSS_PLL_CLK_SRC_SEL Registers

2.6.36.1 MSS_CONTROLSS_PLL_CLK_SRC_SEL Register (Offset = 160h) [reset = h]

Short Description: CONTROLSS_PLL_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1079. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8160h

Access Types Legend

Table 2-1080. CONTROLSS_PLL_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for CONTROLSS_PLL.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.37 MSS_RCM_MSS_RCM_I2C_CLK_SRC_SEL Registers

2.6.37.1 MSS_I2C_CLK_SRC_SEL Register (Offset = 164h) [reset = h]

Short Description: I2C_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1081. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8164h

Access Types Legend

Table 2-1082. I2C_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for I2C.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.38 MSS_RCM_MSS_RCM_LIN0_UART0_CLK_SRC_SEL Registers

2.6.38.1 MSS_LIN0_UART0_CLK_SRC_SEL Register (Offset = 174h) [reset = h]

Short Description: LIN0_UART0_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1083. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8174h

Access Types Legend

Table 2-1084. LIN0_UART0_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.39 MSS_RCM_MSS_RCM_LIN1_UART1_CLK_SRC_SEL Registers

2.6.39.1 MSS_LIN1_UART1_CLK_SRC_SEL Register (Offset = 178h) [reset = h]

Short Description: LIN1_UART1_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1085. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8178h

Access Types Legend

Table 2-1086. LIN1_UART1_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.40 MSS_RCM_MSS_RCM_LIN2_UART2_CLK_SRC_SEL Registers

2.6.40.1 MSS_LIN2_UART2_CLK_SRC_SEL Register (Offset = 17Ch) [reset = h]

Short Description: LIN2_UART2_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1087. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 817Ch

Access Types Legend

Table 2-1088. LIN2_UART2_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.41 MSS_RCM_MSS_RCM_LIN3_UART3_CLK_SRC_SEL Registers

2.6.41.1 MSS_LIN3_UART3_CLK_SRC_SEL Register (Offset = 180h) [reset = h]

Short Description: LIN3_UART3_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1089. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8180h

Access Types Legend

Table 2-1090. LIN3_UART3_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.42 MSS_RCM_MSS_RCM_LIN4_UART4_CLK_SRC_SEL Registers

2.6.42.1 MSS_LIN4_UART4_CLK_SRC_SEL Register (Offset = 184h) [reset = h]

Short Description: LIN4_UART4_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1091. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8184h

Access Types Legend

Table 2-1092. LIN4_UART4_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.43 MSS_RCM_MSS_RCM_LIN5_UART5_CLK_SRC_SEL Registers

2.6.43.1 MSS_LIN5_UART5_CLK_SRC_SEL Register (Offset = 188h) [reset = h]

Short Description: LIN5_UART5_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1093. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8188h

Access Types Legend

Table 2-1094. LIN5_UART5_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKSRCSEL	RW	0h	Select line for selecting source clock for corresponding UART and LIN.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.44 MSS_RCM_MSS_RCM_MCAN0_CLK_DIV_VAL Registers

2.6.44.1 MSS_MCAN0_CLK_DIV_VAL Register (Offset = 200h) [reset = h]

Short Description: MCAN0_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1095. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8200h

Access Types Legend

Table 2-1096. MCAN0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value corresponding MCAN selected clock.Data should be loaded as multibit. For example: if divider value of 8(1000) should be selected then '100010001000' should be configured to the register.

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2.6.45 MSS_RCM_MSS_RCM_MCAN1_CLK_DIV_VAL Registers

2.6.45.1 MSS_MCAN1_CLK_DIV_VAL Register (Offset = 204h) [reset = h]

Short Description: MCAN1_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1097. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8204h

Access Types Legend

Table 2-1098. MCAN1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value corresponding MCAN selected clock.Data should be loaded as multibit. For example: if divider value of 8(1000) should be selected then '100010001000' should be configured to the register.

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2.6.46 MSS_RCM_MSS_RCM_MCAN2_CLK_DIV_VAL Registers

2.6.46.1 MSS_MCAN2_CLK_DIV_VAL Register (Offset = 208h) [reset = h]

Short Description: MCAN2_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1099. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8208h

Access Types Legend

Table 2-1100. MCAN2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value corresponding MCAN selected clock.Data should be loaded as multibit. For example: if divider value of 8(1000) should be selected then '100010001000' should be configured to the register.

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2.6.47 MSS_RCM_MSS_RCM_MCAN3_CLK_DIV_VAL Registers

2.6.47.1 MSS_MCAN3_CLK_DIV_VAL Register (Offset = 20Ch) [reset = h]

Short Description: MCAN3_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1101. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 820Ch

Access Types Legend

Table 2-1102. MCAN3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value corresponding MCAN selected clock.Data should be loaded as multibit. For example: if divider value of 8(1000) should be selected then '100010001000' should be configured to the register.

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2.6.48 MSS_RCM_MSS_RCM_QSPI0_CLK_DIV_VAL Registers

2.6.48.1 MSS_QSPI0_CLK_DIV_VAL Register (Offset = 210h) [reset = h]

Short Description: QSPI0_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1103. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8210h

Access Types Legend

Table 2-1104. QSPI0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value QSPI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.49 MSS_RCM_MSS_RCM_RTI0_CLK_DIV_VAL Registers

2.6.49.1 MSS_RTI0_CLK_DIV_VAL Register (Offset = 214h) [reset = h]

Short Description: RTI0_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1105. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8214h

Access Types Legend

Table 2-1106. RTI0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding RTI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.50 MSS_RCM_MSS_RCM_RTI1_CLK_DIV_VAL Registers

2.6.50.1 MSS_RTI1_CLK_DIV_VAL Register (Offset = 218h) [reset = h]

Short Description: RTI1_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1107. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8218h

Access Types Legend

Table 2-1108. RTI1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding RTI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.51 MSS_RCM_MSS_RCM_RTI2_CLK_DIV_VAL Registers

2.6.51.1 MSS_RTI2_CLK_DIV_VAL Register (Offset = 21Ch) [reset = h]

Short Description: RTI2_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1109. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 821Ch

Access Types Legend

Table 2-1110. RTI2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding RTI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.52 MSS_RCM_MSS_RCM_RTI3_CLK_DIV_VAL Registers

2.6.52.1 MSS_RTI3_CLK_DIV_VAL Register (Offset = 220h) [reset = h]

Short Description: RTI3_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1111. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8220h

Access Types Legend

Table 2-1112. RTI3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding RTI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.53 MSS_RCM_MSS_RCM_WDT0_CLK_DIV_VAL Registers

2.6.53.1 MSS_WDT0_CLK_DIV_VAL Register (Offset = 228h) [reset = h]

Short Description: WDT0_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1113. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8228h

Access Types Legend

Table 2-1114. WDT0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value WDT selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.54 MSS_RCM_MSS_RCM_WDT1_CLK_DIV_VAL Registers

2.6.54.1 MSS_WDT1_CLK_DIV_VAL Register (Offset = 22Ch) [reset = h]

Short Description: WDT1_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1115. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 822Ch

Access Types Legend

Table 2-1116. WDT1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value WDT selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.55 MSS_RCM_MSS_RCM_WDT2_CLK_DIV_VAL Registers

2.6.55.1 MSS_WDT2_CLK_DIV_VAL Register (Offset = 230h) [reset = h]

Short Description: WDT2_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1117. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8230h

Access Types Legend

Table 2-1118. WDT2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value WDT selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.56 MSS_RCM_MSS_RCM_WDT3_CLK_DIV_VAL Registers

2.6.56.1 MSS_WDT3_CLK_DIV_VAL Register (Offset = 234h) [reset = h]

Short Description: WDT3_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1119. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8234h

Access Types Legend

Table 2-1120. WDT3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value WDT selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.57 MSS_RCM_MSS_RCM_MCSPI0_CLK_DIV_VAL Registers

2.6.57.1 MSS_MCSPI0_CLK_DIV_VAL Register (Offset = 23Ch) [reset = h]

Short Description: MCSPI0_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1121. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 823Ch

Access Types Legend

Table 2-1122. MCSPI0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding SPI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.58 MSS_RCM_MSS_RCM_MCSPI1_CLK_DIV_VAL Registers

2.6.58.1 MSS_MCSPI1_CLK_DIV_VAL Register (Offset = 240h) [reset = h]

Short Description: MCSPI1_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1123. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8240h

Access Types Legend

Table 2-1124. MCSPI1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding SPI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.59 MSS_RCM_MSS_RCM_MCSPI2_CLK_DIV_VAL Registers

2.6.59.1 MSS_MCSPI2_CLK_DIV_VAL Register (Offset = 244h) [reset = h]

Short Description: MCSPI2_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1125. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8244h

Access Types Legend

Table 2-1126. MCSPI2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding SPI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.60 MSS_RCM_MSS_RCM_MCSPI3_CLK_DIV_VAL Registers

2.6.60.1 MSS_MCSPI3_CLK_DIV_VAL Register (Offset = 248h) [reset = h]

Short Description: MCSPI3_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1127. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8248h

Access Types Legend

Table 2-1128. MCSPI3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding SPI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.61 MSS_RCM_MSS_RCM_MCSPI4_CLK_DIV_VAL Registers

2.6.61.1 MSS_MCSPI4_CLK_DIV_VAL Register (Offset = 24Ch) [reset = h]

Short Description: MCSPI4_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1129. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 824Ch

Access Types Legend

Table 2-1130. MCSPI4_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value Corresponding SPI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.62 MSS_RCM_MSS_RCM_MMC0_CLK_DIV_VAL Registers

2.6.62.1 MSS_MMC0_CLK_DIV_VAL Register (Offset = 250h) [reset = h]

Short Description: MMC0_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1131. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8250h

Access Types Legend

Table 2-1132. MMC0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value MMCSD selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.63 MSS_RCM_MSS_RCM_ICSSM0_UART_CLK_DIV_VAL Registers

2.6.63.1 MSS_ICSSM0_UART_CLK_DIV_VAL Register (Offset = 254h) [reset = h]

Short Description: ICSSM0_UART_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1133. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8254h

Access Types Legend

Table 2-1134. ICSSM0_UART_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value ICSSM_UCLK selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.64 MSS_RCM_MSS_RCM_CPTS_CLK_DIV_VAL Registers

2.6.64.1 MSS_CPTS_CLK_DIV_VAL Register (Offset = 258h) [reset = h]

Short Description: CPTS_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1135. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8258h

Access Types Legend

Table 2-1136. CPTS_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value CPTS selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.65 MSS_RCM_MSS_RCM_GPMC_CLK_DIV_VAL Registers

2.6.65.1 MSS_GPMC_CLK_DIV_VAL Register (Offset = 25Ch) [reset = h]

Short Description: GPMC_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1137. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 825Ch

Access Types Legend

Table 2-1138. GPMC_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value GPMC selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.66 MSS_RCM_MSS_RCM_CONTROLSS_PLL_CLK_DIV_VAL Registers

2.6.66.1 MSS_CONTROLSS_PLL_CLK_DIV_VAL Register (Offset = 260h) [reset = h]

Short Description: CONTROLSS_PLL_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1139. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8260h

Access Types Legend

Table 2-1140. CONTROLSS_PLL_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value CONTROLSS_PLL selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.67 MSS_RCM_MSS_RCM_I2C_CLK_DIV_VAL Registers

2.6.67.1 MSS_I2C_CLK_DIV_VAL Register (Offset = 264h) [reset = h]

Short Description: I2C_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1141. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8264h

Access Types Legend

Table 2-1142. I2C_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value I2C selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.68 MSS_RCM_MSS_RCM_LIN0_UART0_CLK_DIV_VAL Registers

2.6.68.1 MSS_LIN0_UART0_CLK_DIV_VAL Register (Offset = 274h) [reset = h]

Short Description: LIN0_UART0_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1143. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8274h

Access Types Legend

Table 2-1144. LIN0_UART0_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.69 MSS_RCM_MSS_RCM_LIN1_UART1_CLK_DIV_VAL Registers

2.6.69.1 MSS_LIN1_UART1_CLK_DIV_VAL Register (Offset = 278h) [reset = h]

Short Description: LIN1_UART1_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1145. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8278h

Access Types Legend

Table 2-1146. LIN1_UART1_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.70 MSS_RCM_MSS_RCM_LIN2_UART2_CLK_DIV_VAL Registers

2.6.70.1 MSS_LIN2_UART2_CLK_DIV_VAL Register (Offset = 27Ch) [reset = h]

Short Description: LIN2_UART2_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1147. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 827Ch

Access Types Legend

Table 2-1148. LIN2_UART2_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.71 MSS_RCM_MSS_RCM_LIN3_UART3_CLK_DIV_VAL Registers

2.6.71.1 MSS_LIN3_UART3_CLK_DIV_VAL Register (Offset = 280h) [reset = h]

Short Description: LIN3_UART3_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1149. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8280h

Access Types Legend

Table 2-1150. LIN3_UART3_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.72 MSS_RCM_MSS_RCM_LIN4_UART4_CLK_DIV_VAL Registers

2.6.72.1 MSS_LIN4_UART4_CLK_DIV_VAL Register (Offset = 284h) [reset = h]

Short Description: LIN4_UART4_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1151. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8284h

Access Types Legend

Table 2-1152. LIN4_UART4_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.73 MSS_RCM_MSS_RCM_LIN5_UART5_CLK_DIV_VAL Registers

2.6.73.1 MSS_LIN5_UART5_CLK_DIV_VAL Register (Offset = 288h) [reset = h]

Short Description: LIN5_UART5_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1153. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8288h

Access Types Legend

Table 2-1154. LIN5_UART5_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value for corresponding UART and LIN selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.74 MSS_RCM_MSS_RCM_RGMII_250_CLK_DIV_VAL Registers

2.6.74.1 MSS_RGMII_250_CLK_DIV_VAL Register (Offset = 28Ch) [reset = h]

Short Description: RGMII_250_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1155. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 828Ch

Access Types Legend

Table 2-1156. RGMII_250_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	5F60811h	Divider value RGMII selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.75 MSS_RCM_MSS_RCM_RGMII_50_CLK_DIV_VAL Registers

2.6.75.1 MSS_RGMII_50_CLK_DIV_VAL Register (Offset = 290h) [reset = h]

Short Description: RGMII_50_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1157. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8290h

Access Types Legend

Table 2-1158. RGMII_50_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	174F058A79h	Divider value MII100 selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.76 MSS_RCM_MSS_RCM_RGMII_5_CLK_DIV_VAL Registers

2.6.76.1 MSS_RGMII_5_CLK_DIV_VAL Register (Offset = 294h) [reset = h]

Short Description: RGMII_5_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1159. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8294h

Access Types Legend

Table 2-1160. RGMII_5_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	CLKDIVR	RW	2545131A7F6FEB953EBh	Divider value MII10 selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.77 MSS_RCM_MSS_RCM_XTAL_MMC_32K_CLK_DIV_VAL Registers

2.6.77.1 MSS_XTAL_MMC_32K_CLK_DIV_VAL Register (Offset = 298h) [reset = h]

Short Description: XTAL_MMC_32K_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1161. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8298h

Access Types Legend

Table 2-1162. XTAL_MMC_32K_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 0	CLKDIVR	RW	1636DF558 60E7A8EAE EB45F4Ch	Divider value for XTAL_32K clock.Data should be loaded as multibit. For example: if divider value of '0x30C' is required then '0x30CC330C' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.78 MSS_RCM_MSS_RCM_XTAL_TEMPSENSE_32K_CLK_DIV_VAL Registers

2.6.78.1 MSS_XTAL_TEMPSENSE_32K_CLK_DIV_VAL Register (Offset = 29Ch) [reset = h]

Short Description: XTAL_TEMPSENSE_32K_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1163. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 829Ch

Access Types Legend

Table 2-1164. XTAL_TEMPSENSE_32K_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 0	CLKDIVR	RW	1636DF558 60E7A8EAE EB45F4Ch	Divider value for XTAL_32K clock.Data should be loaded as multibit. For example: if divider value of '0x30C' is required then '0x30CC330C' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.79 MSS_RCM_MSS_RCM_MSS_ELM_CLK_DIV_VAL Registers

2.6.79.1 MSS_MSS_ELM_CLK_DIV_VAL Register (Offset = 2A0h) [reset = h]

Short Description: MSS_ELM_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1165. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 82A0h

Access Types Legend

Table 2-1166. MSS_ELM_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	419258BBh	Divider value ELM clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.80 MSS_RCM_MSS_RCM_MCAN0_CLK_GATE Registers

2.6.80.1 MSS_MCAN0_CLK_GATE Register (Offset = 300h) [reset = h]

Short Description: MCAN0_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1167. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8300h

Access Types Legend

Table 2-1168. MCAN0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for corresponding MCAN

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2.6.81 MSS_RCM_MSS_RCM_MCAN1_CLK_GATE Registers

2.6.81.1 MSS_MCAN1_CLK_GATE Register (Offset = 304h) [reset = h]

Short Description: MCAN1_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1169. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8304h

Access Types Legend

Table 2-1170. MCAN1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for corresponding MCAN

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2.6.82 MSS_RCM_MSS_RCM_MCAN2_CLK_GATE Registers

2.6.82.1 MSS_MCAN2_CLK_GATE Register (Offset = 308h) [reset = h]

Short Description: MCAN2_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1171. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8308h

Access Types Legend

Table 2-1172. MCAN2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for corresponding MCAN

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2.6.83 MSS_RCM_MSS_RCM_MCAN3_CLK_GATE Registers

2.6.83.1 MSS_MCAN3_CLK_GATE Register (Offset = 30Ch) [reset = h]

Short Description: MCAN3_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1173. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 830Ch

Access Types Legend

Table 2-1174. MCAN3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for corresponding MCAN

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2.6.84 MSS_RCM_MSS_RCM_QSPI0_CLK_GATE Registers

2.6.84.1 MSS_QSPI0_CLK_GATE Register (Offset = 310h) [reset = h]

Short Description: QSPI0_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1175. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8310h

Access Types Legend

Table 2-1176. QSPI0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for QSPI

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2.6.85 MSS_RCM_MSS_RCM_RTI0_CLK_GATE Registers

2.6.85.1 MSS_RTI0_CLK_GATE Register (Offset = 314h) [reset = h]

Short Description: RTI0_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1177. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8314h

Access Types Legend

Table 2-1178. RTI0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for Corresponding RTI

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2.6.86 MSS_RCM_MSS_RCM_RTI1_CLK_GATE Registers

2.6.86.1 MSS_RTI1_CLK_GATE Register (Offset = 318h) [reset = h]

Short Description: RTI1_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1179. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8318h

Access Types Legend

Table 2-1180. RTI1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for Corresponding RTI

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2.6.87 MSS_RCM_MSS_RCM_RTI2_CLK_GATE Registers

2.6.87.1 MSS_RTI2_CLK_GATE Register (Offset = 31Ch) [reset = h]

Short Description: RTI2_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1181. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 831Ch

Access Types Legend

Table 2-1182. RTI2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for Corresponding RTI

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2.6.88 MSS_RCM_MSS_RCM_RTI3_CLK_GATE Registers

2.6.88.1 MSS_RTI3_CLK_GATE Register (Offset = 320h) [reset = h]

Short Description: RTI3_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1183. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8320h

Access Types Legend

Table 2-1184. RTI3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for Corresponding RTI

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2.6.89 MSS_RCM_MSS_RCM_WDT0_CLK_GATE Registers

2.6.89.1 MSS_WDT0_CLK_GATE Register (Offset = 328h) [reset = h]

Short Description: WDT0_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1185. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8328h

Access Types Legend

Table 2-1186. WDT0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for WDT

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2.6.90 MSS_RCM_MSS_RCM_WDT1_CLK_GATE Registers

2.6.90.1 MSS_WDT1_CLK_GATE Register (Offset = 32Ch) [reset = h]

Short Description: WDT1_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1187. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 832Ch

Access Types Legend

Table 2-1188. WDT1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for WDT

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2.6.91 MSS_RCM_MSS_RCM_WDT2_CLK_GATE Registers

2.6.91.1 MSS_WDT2_CLK_GATE Register (Offset = 330h) [reset = h]

Short Description: WDT2_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1189. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8330h

Access Types Legend

Table 2-1190. WDT2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for WDT

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2.6.92 MSS_RCM_MSS_RCM_WDT3_CLK_GATE Registers

2.6.92.1 MSS_WDT3_CLK_GATE Register (Offset = 334h) [reset = h]

Short Description: WDT3_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1191. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8334h

Access Types Legend

Table 2-1192. WDT3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for WDT

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2.6.93 MSS_RCM_MSS_RCM_MCSPI0_CLK_GATE Registers

2.6.93.1 MSS_MCSPI0_CLK_GATE Register (Offset = 33Ch) [reset = h]

Short Description: MCSPI0_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1193. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 833Ch

Access Types Legend

Table 2-1194. MCSPI0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for Corresponding SPI

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2.6.94 MSS_RCM_MSS_RCM_MCSPI1_CLK_GATE Registers

2.6.94.1 MSS_MCSPI1_CLK_GATE Register (Offset = 340h) [reset = h]

Short Description: MCSPI1_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1195. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8340h

Access Types Legend

Table 2-1196. MCSPI1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for Corresponding SPI

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2.6.95 MSS_RCM_MSS_RCM_MCSPI2_CLK_GATE Registers

2.6.95.1 MSS_MCSPI2_CLK_GATE Register (Offset = 344h) [reset = h]

Short Description: MCSPI2_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1197. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8344h

Access Types Legend

Table 2-1198. MCSPI2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for Corresponding SPI

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2.6.96 MSS_RCM_MSS_RCM_MCSPI3_CLK_GATE Registers

2.6.96.1 MSS_MCSPI3_CLK_GATE Register (Offset = 348h) [reset = h]

Short Description: MCSPI3_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1199. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8348h

Access Types Legend

Table 2-1200. MCSPI3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for Corresponding SPI

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2.6.97 MSS_RCM_MSS_RCM_MCSPI4_CLK_GATE Registers

2.6.97.1 MSS_MCSPI4_CLK_GATE Register (Offset = 34Ch) [reset = h]

Short Description: MCSPI4_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1201. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 834Ch

Access Types Legend

Table 2-1202. MCSPI4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for Corresponding SPI

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2.6.98 MSS_RCM_MSS_RCM_MMC0_CLK_GATE Registers

2.6.98.1 MSS_MMC0_CLK_GATE Register (Offset = 350h) [reset = h]

Short Description: MMC0_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1203. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8350h

Access Types Legend

Table 2-1204. MMC0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for MMCSD

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2.6.99 MSS_RCM_MSS_RCM_ICSSM0_UART_CLK_GATE Registers

2.6.99.1 MSS_ICSSM0_UART_CLK_GATE Register (Offset = 354h) [reset = h]

Short Description: ICSSM0_UART_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1205. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8354h

Access Types Legend

Table 2-1206. ICSSM0_UART_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for ICSSM_UCLK

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2.6.100 MSS_RCM_MSS_RCM_CPTS_CLK_GATE Registers

2.6.100.1 MSS_CPTS_CLK_GATE Register (Offset = 358h) [reset = h]

Short Description: CPTS_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1207. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8358h

Access Types Legend

Table 2-1208. CPTS_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for CPTS

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2.6.101 MSS_RCM_MSS_RCM_GPMC_CLK_GATE Registers

2.6.101.1 MSS_GPMC_CLK_GATE Register (Offset = 35Ch) [reset = h]

Short Description: GPMC_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1209. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 835Ch

Access Types Legend

Table 2-1210. GPMC_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for GPMC

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2.6.102 MSS_RCM_MSS_RCM_CONTROLSS_PLL_CLK_GATE Registers

2.6.102.1 MSS_CONTROLSS_PLL_CLK_GATE Register (Offset = 360h) [reset = h]

Short Description: CONTROLSS_PLL_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1211. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8360h

Access Types Legend

Table 2-1212. CONTROLSS_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for CONTROLSS_PLL

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2.6.103 MSS_RCM_MSS_RCM_I2C0_CLK_GATE Registers

2.6.103.1 MSS_I2C0_CLK_GATE Register (Offset = 364h) [reset = h]

Short Description: I2C0_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1213. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8364h

Access Types Legend

Table 2-1214. I2C0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for I2C

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2.6.104 MSS_RCM_MSS_RCM_I2C1_CLK_GATE Registers

2.6.104.1 MSS_I2C1_CLK_GATE Register (Offset = 368h) [reset = h]

Short Description: I2C1_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1215. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8368h

Access Types Legend

Table 2-1216. I2C1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for I2C

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2.6.105 MSS_RCM_MSS_RCM_I2C2_CLK_GATE Registers

2.6.105.1 MSS_I2C2_CLK_GATE Register (Offset = 36Ch) [reset = h]

Short Description: I2C2_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1217. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 836Ch

Access Types Legend

Table 2-1218. I2C2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for I2C

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2.6.106 MSS_RCM_MSS_RCM_I2C3_CLK_GATE Registers

2.6.106.1 MSS_I2C3_CLK_GATE Register (Offset = 370h) [reset = h]

Short Description: I2C3_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1219. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8370h

Access Types Legend

Table 2-1220. I2C3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for I2C

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2.6.107 MSS_RCM_MSS_RCM_LIN0_CLK_GATE Registers

2.6.107.1 MSS_LIN0_CLK_GATE Register (Offset = 374h) [reset = h]

Short Description: LIN0_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1221. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8374h

Access Types Legend

Table 2-1222. LIN0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for SPIB

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2.6.108 MSS_RCM_MSS_RCM_LIN1_CLK_GATE Registers

2.6.108.1 MSS_LIN1_CLK_GATE Register (Offset = 378h) [reset = h]

Short Description: LIN1_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1223. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8378h

Access Types Legend

Table 2-1224. LIN1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for SPIB

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2.6.109 MSS_RCM_MSS_RCM_LIN2_CLK_GATE Registers

2.6.109.1 MSS_LIN2_CLK_GATE Register (Offset = 37Ch) [reset = h]

Short Description: LIN2_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1225. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 837Ch

Access Types Legend

Table 2-1226. LIN2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for SPIB

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2.6.110 MSS_RCM_MSS_RCM_LIN3_CLK_GATE Registers

2.6.110.1 MSS_LIN3_CLK_GATE Register (Offset = 380h) [reset = h]

Short Description: LIN3_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1227. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8380h

Access Types Legend

Table 2-1228. LIN3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for SPIB

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2.6.111 MSS_RCM_MSS_RCM_LIN4_CLK_GATE Registers

2.6.111.1 MSS_LIN4_CLK_GATE Register (Offset = 384h) [reset = h]

Short Description: LIN4_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1229. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8384h

Access Types Legend

Table 2-1230. LIN4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for SPIB

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2.6.112 MSS_RCM_MSS_RCM_UART0_CLK_GATE Registers

2.6.112.1 MSS_UART0_CLK_GATE Register (Offset = 38Ch) [reset = h]

Short Description: UART0_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1231. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 838Ch

Access Types Legend

Table 2-1232. UART0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for corresponding UART

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2.6.113 MSS_RCM_MSS_RCM_UART1_CLK_GATE Registers

2.6.113.1 MSS_UART1_CLK_GATE Register (Offset = 390h) [reset = h]

Short Description: UART1_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1233. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8390h

Access Types Legend

Table 2-1234. UART1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for corresponding UART

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2.6.114 MSS_RCM_MSS_RCM_UART2_CLK_GATE Registers

2.6.114.1 MSS_UART2_CLK_GATE Register (Offset = 394h) [reset = h]

Short Description: UART2_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1235. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8394h

Access Types Legend

Table 2-1236. UART2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for corresponding UART

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2.6.115 MSS_RCM_MSS_RCM_UART3_CLK_GATE Registers

2.6.115.1 MSS_UART3_CLK_GATE Register (Offset = 398h) [reset = h]

Short Description: UART3_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1237. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8398h

Access Types Legend

Table 2-1238. UART3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for corresponding UART

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2.6.116 MSS_RCM_MSS_RCM_UART4_CLK_GATE Registers

2.6.116.1 MSS_UART4_CLK_GATE Register (Offset = 39Ch) [reset = h]

Short Description: UART4_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1239. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 839Ch

Access Types Legend

Table 2-1240. UART4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for corresponding UART

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2.6.117 MSS_RCM_MSS_RCM_UART5_CLK_GATE Registers

2.6.117.1 MSS_UART5_CLK_GATE Register (Offset = 3A0h) [reset = h]

Short Description: UART5_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1241. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83A0h

Access Types Legend

Table 2-1242. UART5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for corresponding UART

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2.6.118 MSS_RCM_MSS_RCM_RGMII_250_CLK_GATE Registers

2.6.118.1 MSS_RGMII_250_CLK_GATE Register (Offset = 3A4h) [reset = h]

Short Description: RGMII_250_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1243. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83A4h

Access Types Legend

Table 2-1244. RGMII_250_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for RGMII

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2.6.119 MSS_RCM_MSS_RCM_RGMII_50_CLK_GATE Registers

2.6.119.1 MSS_RGMII_50_CLK_GATE Register (Offset = 3A8h) [reset = h]

Short Description: RGMII_50_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1245. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83A8h

Access Types Legend

Table 2-1246. RGMII_50_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for MII100

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2.6.120 MSS_RCM_MSS_RCM_RGMII_5_CLK_GATE Registers

2.6.120.1 MSS_RGMII_5_CLK_GATE Register (Offset = 3ACh) [reset = h]

Short Description: RGMII_5_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1247. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83ACh

Access Types Legend

Table 2-1248. RGMII_5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for MII10

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2.6.121 MSS_RCM_MSS_RCM_MMC0_32K_CLK_GATE Registers

2.6.121.1 MSS_MMC0_32K_CLK_GATE Register (Offset = 3B0h) [reset = h]

Short Description: MMC0_32K_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1249. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83B0h

Access Types Legend

Table 2-1250. MMC0_32K_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for MMCSD_32K

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2.6.122 MSS_RCM_MSS_RCM_TEMPSENSE_32K_CLK_GATE Registers

2.6.122.1 MSS_TEMPSENSE_32K_CLK_GATE Register (Offset = 3B4h) [reset = h]

Short Description: TEMPSENSE_32K_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1251. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83B4h

Access Types Legend

Table 2-1252. TEMPSENSE_32K_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for TEMPSENSE_32K

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2.6.123 MSS_RCM_MSS_RCM_CPSW_CLK_GATE Registers

2.6.123.1 MSS_CPSW_CLK_GATE Register (Offset = 3B8h) [reset = h]

Short Description: CPSW_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1253. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83B8h

Access Types Legend

Table 2-1254. CPSW_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for CPSW CPPI

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2.6.124 MSS_RCM_MSS_RCM_ICSSM0_IEP_CLK_GATE Registers

2.6.124.1 MSS_ICSSM0_IEP_CLK_GATE Register (Offset = 3BCh) [reset = h]

Short Description: ICSSM0_IEP_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1255. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83BCh

Access Types Legend

Table 2-1256. ICSSM0_IEP_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for ICSSM_IEP

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2.6.125 MSS_RCM_MSS_RCM_ICSSM0_CORE_CLK_GATE Registers

2.6.125.1 MSS_ICSSM0_CORE_CLK_GATE Register (Offset = 3C0h) [reset = h]

Short Description: ICSSM0_CORE_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1257. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83C0h

Access Types Legend

Table 2-1258. ICSSM0_CORE_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for ICSSM_CORE

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2.6.126 MSS_RCM_MSS_RCM_MSS_ICSSM_SYS_CLK_GATE Registers

2.6.126.1 MSS_MSS_ICSSM_SYS_CLK_GATE Register (Offset = 3C4h) [reset = h]

Short Description: MSS_ICSSM_SYS_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1259. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83C4h

Access Types Legend

Table 2-1260. MSS_ICSSM_SYS_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for ICSSM_SYS

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2.6.127 MSS_RCM_MSS_RCM_MSS_ELM_CLK_GATE Registers

2.6.127.1 MSS_MSS_ELM_CLK_GATE Register (Offset = 3C8h) [reset = h]

Short Description: MSS_ELM_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1261. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83C8h

Access Types Legend

Table 2-1262. MSS_ELM_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for ELM

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2.6.128 MSS_RCM_MSS_RCM_R5SS0_CORE0_GATE Registers

2.6.128.1 MSS_R5SS0_CORE0_GATE Register (Offset = 3CCh) [reset = h]

Short Description: R5SS0_CORE0_GATE register

Long Description:

Return to Summary Table

Table 2-1263. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83CCh

Access Types Legend

Table 2-1264. R5SS0_CORE0_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLKGATE	RW	0h	Writing 3'b111 will gate clock to CORE0 related peripherals inside Cortexr5ss

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2.6.129 MSS_RCM_MSS_RCM_R5SS1_CORE0_GATE Registers

2.6.129.1 MSS_R5SS1_CORE0_GATE Register (Offset = 3D0h) [reset = h]

Short Description: R5SS1_CORE0_GATE register

Long Description:

Return to Summary Table

Table 2-1265. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83D0h

Access Types Legend

Table 2-1266. R5SS1_CORE0_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLKGATE	RW	0h	Writing 3'b111 will gate clock to CORE0 related peripherals inside Cortexr5ss

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2.6.130 MSS_RCM_MSS_RCM_R5SS0_CORE1_GATE Registers

2.6.130.1 MSS_R5SS0_CORE1_GATE Register (Offset = 3D4h) [reset = h]

Short Description: R5SS0_CORE1_GATE register

Long Description:

Return to Summary Table

Table 2-1267. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83D4h

Access Types Legend

Table 2-1268. R5SS0_CORE1_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLKGATE	RW	0h	Writing 3'b111 will gate clock to CORE1 related peripherals inside Cortexr5ss

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2.6.131 MSS_RCM_MSS_RCM_R5SS1_CORE1_GATE Registers

2.6.131.1 MSS_R5SS1_CORE1_GATE Register (Offset = 3D8h) [reset = h]

Short Description: R5SS1_CORE1_GATE register

Long Description:

Return to Summary Table

Table 2-1269. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 83D8h

Access Types Legend

Table 2-1270. R5SS1_CORE1_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLKGATE	RW	0h	Writing 3'b111 will gate clock to CORE1 related peripherals inside Cortexr5ss

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2.6.132 MSS_RCM_MSS_RCM_MCAN0_CLK_STATUS Registers

2.6.132.1 MSS_MCAN0_CLK_STATUS Register (Offset = 400h) [reset = h]

Short Description: MCAN0_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1271. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8400h

Access Types Legend

Table 2-1272. MCAN0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding MCAN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding MCAN

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2.6.133 MSS_RCM_MSS_RCM_MCAN1_CLK_STATUS Registers

2.6.133.1 MSS_MCAN1_CLK_STATUS Register (Offset = 404h) [reset = h]

Short Description: MCAN1_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1273. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8404h

Access Types Legend

Table 2-1274. MCAN1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding MCAN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding MCAN

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2.6.134 MSS_RCM_MSS_RCM_MCAN2_CLK_STATUS Registers

2.6.134.1 MSS_MCAN2_CLK_STATUS Register (Offset = 408h) [reset = h]

Short Description: MCAN2_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1275. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8408h

Access Types Legend

Table 2-1276. MCAN2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding MCAN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding MCAN

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2.6.135 MSS_RCM_MSS_RCM_MCAN3_CLK_STATUS Registers

2.6.135.1 MSS_MCAN3_CLK_STATUS Register (Offset = 40Ch) [reset = h]

Short Description: MCAN3_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1277. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 840Ch

Access Types Legend

Table 2-1278. MCAN3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding MCAN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding MCAN

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2.6.136 MSS_RCM_MSS_RCM_QSPI0_CLK_STATUS Registers

2.6.136.1 MSS_QSPI0_CLK_STATUS Register (Offset = 410h) [reset = h]

Short Description: QSPI0_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1279. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8410h

Access Types Legend

Table 2-1280. QSPI0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for QSPI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for QSPI

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2.6.137 MSS_RCM_MSS_RCM_RTI0_CLK_STATUS Registers

2.6.137.1 MSS_RTI0_CLK_STATUS Register (Offset = 414h) [reset = h]

Short Description: RTI0_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1281. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8414h

Access Types Legend

Table 2-1282. RTI0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding RTI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding RTI

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2.6.138 MSS_RCM_MSS_RCM_RTI1_CLK_STATUS Registers

2.6.138.1 MSS_RTI1_CLK_STATUS Register (Offset = 418h) [reset = h]

Short Description: RTI1_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1283. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8418h

Access Types Legend

Table 2-1284. RTI1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding RTI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding RTI

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2.6.139 MSS_RCM_MSS_RCM_RTI2_CLK_STATUS Registers

2.6.139.1 MSS_RTI2_CLK_STATUS Register (Offset = 41Ch) [reset = h]

Short Description: RTI2_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1285. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 841Ch

Access Types Legend

Table 2-1286. RTI2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding RTI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding RTI

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2.6.140 MSS_RCM_MSS_RCM_RTI3_CLK_STATUS Registers

2.6.140.1 MSS_RTI3_CLK_STATUS Register (Offset = 420h) [reset = h]

Short Description: RTI3_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1287. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8420h

Access Types Legend

Table 2-1288. RTI3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding RTI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding RTI

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2.6.141 MSS_RCM_MSS_RCM_WDT0_CLK_STATUS Registers

2.6.141.1 MSS_WDT0_CLK_STATUS Register (Offset = 428h) [reset = h]

Short Description: WDT0_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1289. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8428h

Access Types Legend

Table 2-1290. WDT0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for WDT
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for WDT

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2.6.142 MSS_RCM_MSS_RCM_WDT1_CLK_STATUS Registers

2.6.142.1 MSS_WDT1_CLK_STATUS Register (Offset = 42Ch) [reset = h]

Short Description: WDT1_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1291. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 842Ch

Access Types Legend

Table 2-1292. WDT1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for WDT
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for WDT

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2.6.143 MSS_RCM_MSS_RCM_WDT2_CLK_STATUS Registers

2.6.143.1 MSS_WDT2_CLK_STATUS Register (Offset = 430h) [reset = h]

Short Description: WDT2_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1293. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8430h

Access Types Legend

Table 2-1294. WDT2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for WDT
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for WDT

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2.6.144 MSS_RCM_MSS_RCM_WDT3_CLK_STATUS Registers

2.6.144.1 MSS_WDT3_CLK_STATUS Register (Offset = 434h) [reset = h]

Short Description: WDT3_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1295. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8434h

Access Types Legend

Table 2-1296. WDT3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for WDT
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for WDT

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2.6.145 MSS_RCM_MSS_RCM_MCSPI0_CLK_STATUS Registers

2.6.145.1 MSS_MCSPI0_CLK_STATUS Register (Offset = 43Ch) [reset = h]

Short Description: MCSPI0_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1297. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 843Ch

Access Types Legend

Table 2-1298. MCSPI0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding SPI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding SPI

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2.6.146 MSS_RCM_MSS_RCM_MCSPI1_CLK_STATUS Registers

2.6.146.1 MSS_MCSPI1_CLK_STATUS Register (Offset = 440h) [reset = h]

Short Description: MCSPI1_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1299. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8440h

Access Types Legend

Table 2-1300. MCSPI1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding SPI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding SPI

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2.6.147 MSS_RCM_MSS_RCM_MCSPI2_CLK_STATUS Registers

2.6.147.1 MSS_MCSPI2_CLK_STATUS Register (Offset = 444h) [reset = h]

Short Description: MCSPI2_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1301. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8444h

Access Types Legend

Table 2-1302. MCSPI2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding SPI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding SPI

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2.6.148 MSS_RCM_MSS_RCM_MCSPI3_CLK_STATUS Registers

2.6.148.1 MSS_MCSPI3_CLK_STATUS Register (Offset = 448h) [reset = h]

Short Description: MCSPI3_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1303. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8448h

Access Types Legend

Table 2-1304. MCSPI3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding SPI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding SPI

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2.6.149 MSS_RCM_MSS_RCM_MCSPI4_CLK_STATUS Registers

2.6.149.1 MSS_MCSPI4_CLK_STATUS Register (Offset = 44Ch) [reset = h]

Short Description: MCSPI4_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1305. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 844Ch

Access Types Legend

Table 2-1306. MCSPI4_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for Corresponding SPI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for Corresponding SPI

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2.6.150 MSS_RCM_MSS_RCM_MMC0_CLK_STATUS Registers

2.6.150.1 MSS_MMC0_CLK_STATUS Register (Offset = 450h) [reset = h]

Short Description: MMC0_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1307. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8450h

Access Types Legend

Table 2-1308. MMC0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for MMCSD
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for MMCSD

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2.6.151 MSS_RCM_MSS_RCM_ICSSM0_UART_CLK_STATUS Registers

2.6.151.1 MSS_ICSSM0_UART_CLK_STATUS Register (Offset = 454h) [reset = h]

Short Description: ICSSM0_UART_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1309. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8454h

Access Types Legend

Table 2-1310. ICSSM0_UART_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for ICSSM_UCLK
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for ICSSM_UCLK

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2.6.152 MSS_RCM_MSS_RCM_CPTS_CLK_STATUS Registers

2.6.152.1 MSS_CPTS_CLK_STATUS Register (Offset = 458h) [reset = h]

Short Description: CPTS_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1311. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8458h

Access Types Legend

Table 2-1312. CPTS_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for CPTS
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for CPTS

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2.6.153 MSS_RCM_MSS_RCM_GPMC_CLK_STATUS Registers

2.6.153.1 MSS_GPMC_CLK_STATUS Register (Offset = 45Ch) [reset = h]

Short Description: GPMC_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1313. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 845Ch

Access Types Legend

Table 2-1314. GPMC_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for GPMC
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for GPMC

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2.6.154 MSS_RCM_MSS_RCM_CONTROLSS_PLL_CLK_STATUS Registers

2.6.154.1 MSS_CONTROLSS_PLL_CLK_STATUS Register (Offset = 460h) [reset = h]

Short Description: CONTROLSS_PLL_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1315. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8460h

Access Types Legend

Table 2-1316. CONTROLSS_PLL_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for CONTROLSS_PLL
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for CONTROLSS_PLL

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2.6.155 MSS_RCM_MSS_RCM_I2C_CLK_STATUS Registers

2.6.155.1 MSS_I2C_CLK_STATUS Register (Offset = 464h) [reset = h]

Short Description: I2C_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1317. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8464h

Access Types Legend

Table 2-1318. I2C_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for I2C
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for I2C

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2.6.156 MSS_RCM_MSS_RCM_LIN0_UART0_CLK_STATUS Registers

2.6.156.1 MSS_LIN0_UART0_CLK_STATUS Register (Offset = 474h) [reset = h]

Short Description: LIN0_UART0_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1319. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8474h

Access Types Legend

Table 2-1320. LIN0_UART0_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding UART and LIN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding UART and LIN

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2.6.157 MSS_RCM_MSS_RCM_LIN1_UART1_CLK_STATUS Registers

2.6.157.1 MSS_LIN1_UART1_CLK_STATUS Register (Offset = 478h) [reset = h]

Short Description: LIN1_UART1_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1321. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8478h

Access Types Legend

Table 2-1322. LIN1_UART1_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding UART and LIN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding UART and LIN

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2.6.158 MSS_RCM_MSS_RCM_LIN2_UART2_CLK_STATUS Registers

2.6.158.1 MSS_LIN2_UART2_CLK_STATUS Register (Offset = 47Ch) [reset = h]

Short Description: LIN2_UART2_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1323. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 847Ch

Access Types Legend

Table 2-1324. LIN2_UART2_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding UART and LIN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding UART and LIN

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2.6.159 MSS_RCM_MSS_RCM_LIN3_UART3_CLK_STATUS Registers

2.6.159.1 MSS_LIN3_UART3_CLK_STATUS Register (Offset = 480h) [reset = h]

Short Description: LIN3_UART3_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1325. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8480h

Access Types Legend

Table 2-1326. LIN3_UART3_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding UART and LIN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding UART and LIN

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2.6.160 MSS_RCM_MSS_RCM_LIN4_UART4_CLK_STATUS Registers

2.6.160.1 MSS_LIN4_UART4_CLK_STATUS Register (Offset = 484h) [reset = h]

Short Description: LIN4_UART4_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1327. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8484h

Access Types Legend

Table 2-1328. LIN4_UART4_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding UART and LIN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding UART and LIN

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2.6.161 MSS_RCM_MSS_RCM_LIN5_UART5_CLK_STATUS Registers

2.6.161.1 MSS_LIN5_UART5_CLK_STATUS Register (Offset = 488h) [reset = h]

Short Description: LIN5_UART5_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1329. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8488h

Access Types Legend

Table 2-1330. LIN5_UART5_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for corresponding UART and LIN
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for corresponding UART and LIN

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2.6.162 MSS_RCM_MSS_RCM_RGMII_250_CLK_STATUS Registers

2.6.162.1 MSS_RGMII_250_CLK_STATUS Register (Offset = 48Ch) [reset = h]

Short Description: RGMII_250_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1331. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 848Ch

Access Types Legend

Table 2-1332. RGMII_250_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	1h	Status shows the current divider value choosen for RGMII
	RESERVED	NONE		Reserved

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2.6.163 MSS_RCM_MSS_RCM_RGMII_50_CLK_STATUS Registers

2.6.163.1 MSS_RGMII_50_CLK_STATUS Register (Offset = 490h) [reset = h]

Short Description: RGMII_50_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1333. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8490h

Access Types Legend

Table 2-1334. RGMII_50_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	3E9h	Status shows the current divider value choosen for MII100
	RESERVED	NONE		Reserved

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2.6.164 MSS_RCM_MSS_RCM_RGMII_5_CLK_STATUS Registers

2.6.164.1 MSS_RGMII_5_CLK_STATUS Register (Offset = 494h) [reset = h]

Short Description: RGMII_5_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1335. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8494h

Access Types Legend

Table 2-1336. RGMII_5_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	10C8EBh	Status shows the current divider value choosen for MII10
	RESERVED	NONE		Reserved

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2.6.165 MSS_RCM_MSS_RCM_MMC0_32K_CLK_STATUS Registers

2.6.165.1 MSS_MMC0_32K_CLK_STATUS Register (Offset = 49Ch) [reset = h]

Short Description: MMC0_32K_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1337. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 849Ch

Access Types Legend

Table 2-1338. MMC0_32K_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17 - 8	CURRDIVIDER	RO	4190AF4Ch	Status shows the current divider value choosen for XTAL_32K
	RESERVED	NONE		Reserved

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2.6.166 MSS_RCM_MSS_RCM_TEMPSENSE_32K_CLK_STATUS Registers

2.6.166.1 MSS_TEMPSENSE_32K_CLK_STATUS Register (Offset = 4A0h) [reset = h]

Short Description: TEMPSENSE_32K_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1339. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 84A0h

Access Types Legend

Table 2-1340. TEMPSENSE_32K_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17 - 8	CURRDIVIDER	RO	4190AF4Ch	Status shows the current divider value choosen for XTAL_32K
	RESERVED	NONE		Reserved

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2.6.167 MSS_RCM_MSS_RCM_MSS_ELM_CLK_STATUS Registers

2.6.167.1 MSS_MSS_ELM_CLK_STATUS Register (Offset = 4A4h) [reset = h]

Short Description: MSS_ELM_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1341. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 84A4h

Access Types Legend

Table 2-1342. MSS_ELM_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	Bh	Status shows the current divider value choosen for ELM
	RESERVED	NONE		Reserved

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2.6.168 MSS_RCM_MSS_RCM_R5SS0_POR_RST_CTRL Registers

2.6.168.1 MSS_R5SS0_POR_RST_CTRL Register (Offset = 500h) [reset = h]

Short Description: R5SS0_POR_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1343. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8500h

Access Types Legend

Table 2-1344. R5SS0_POR_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:Writing 3'b111 will assert por reset to R5SS Read is always 000

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2.6.169 MSS_RCM_MSS_RCM_R5SS1_POR_RST_CTRL Registers

2.6.169.1 MSS_R5SS1_POR_RST_CTRL Register (Offset = 504h) [reset = h]

Short Description: R5SS1_POR_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1345. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8504h

Access Types Legend

Table 2-1346. R5SS1_POR_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:Writing 3'b111 will assert por reset to R5SS Read is always 000

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2.6.170 MSS_RCM_MSS_RCM_R5SS0_CORE0_GRST_CTRL Registers

2.6.170.1 MSS_R5SS0_CORE0_GRST_CTRL Register (Offset = 508h) [reset = h]

Short Description: R5SS0_CORE0_GRST_CTRL register

Long Description:

Return to Summary Table

Table 2-1347. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8508h

Access Types Legend

Table 2-1348. R5SS0_CORE0_GRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:Writing 3'b111 will reset CORE0 and MSS_CORE0_VIM

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2.6.171 MSS_RCM_MSS_RCM_R5SS1_CORE0_GRST_CTRL Registers

2.6.171.1 MSS_R5SS1_CORE0_GRST_CTRL Register (Offset = 50Ch) [reset = h]

Short Description: R5SS1_CORE0_GRST_CTRL register

Long Description:

Return to Summary Table

Table 2-1349. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 850Ch

Access Types Legend

Table 2-1350. R5SS1_CORE0_GRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:Writing 3'b111 will reset CORE0 and MSS_CORE0_VIM

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2.6.172 MSS_RCM_MSS_RCM_R5SS0_CORE1_GRST_CTRL Registers

2.6.172.1 MSS_R5SS0_CORE1_GRST_CTRL Register (Offset = 510h) [reset = h]

Short Description: R5SS0_CORE1_GRST_CTRL register

Long Description:

Return to Summary Table

Table 2-1351. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8510h

Access Types Legend

Table 2-1352. R5SS0_CORE1_GRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:Writing 3'b111 will reset CORE1 and MSS_CORE1_VIM

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2.6.173 MSS_RCM_MSS_RCM_R5SS1_CORE1_GRST_CTRL Registers

2.6.173.1 MSS_R5SS1_CORE1_GRST_CTRL Register (Offset = 514h) [reset = h]

Short Description: R5SS1_CORE1_GRST_CTRL register

Long Description:

Return to Summary Table

Table 2-1353. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8514h

Access Types Legend

Table 2-1354. R5SS1_CORE1_GRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:Writing 3'b111 will reset CORE1 and MSS_CORE1_VIM

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2.6.174 MSS_RCM_MSS_RCM_R5SS0_CORE0_LRST_CTRL Registers

2.6.174.1 MSS_R5SS0_CORE0_LRST_CTRL Register (Offset = 518h) [reset = h]

Short Description: R5SS0_CORE0_LRST_CTRL register

Long Description:

Return to Summary Table

Table 2-1355. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8518h

Access Types Legend

Table 2-1356. R5SS0_CORE0_LRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:Writing 3'b111 will reset CORE0 only

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2.6.175 MSS_RCM_MSS_RCM_R5SS1_CORE0_LRST_CTRL Registers

2.6.175.1 MSS_R5SS1_CORE0_LRST_CTRL Register (Offset = 51Ch) [reset = h]

Short Description: R5SS1_CORE0_LRST_CTRL register

Long Description:

Return to Summary Table

Table 2-1357. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 851Ch

Access Types Legend

Table 2-1358. R5SS1_CORE0_LRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:Writing 3'b111 will reset CORE0 only

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2.6.176 MSS_RCM_MSS_RCM_R5SS0_CORE1_LRST_CTRL Registers

2.6.176.1 MSS_R5SS0_CORE1_LRST_CTRL Register (Offset = 520h) [reset = h]

Short Description: R5SS0_CORE1_LRST_CTRL register

Long Description:

Return to Summary Table

Table 2-1359. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8520h

Access Types Legend

Table 2-1360. R5SS0_CORE1_LRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:Writing 3'b111 will reset CORE1 only

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2.6.177 MSS_RCM_MSS_RCM_R5SS1_CORE1_LRST_CTRL Registers

2.6.177.1 MSS_R5SS1_CORE1_LRST_CTRL Register (Offset = 524h) [reset = h]

Short Description: R5SS1_CORE1_LRST_CTRL register

Long Description:

Return to Summary Table

Table 2-1361. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8524h

Access Types Legend

Table 2-1362. R5SS1_CORE1_LRST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.write pulse bit field:Writing 3'b111 will reset CORE1 only

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2.6.178 MSS_RCM_MSS_RCM_R5SS0_VIM0_RST_CTRL Registers

2.6.178.1 MSS_R5SS0_VIM0_RST_CTRL Register (Offset = 528h) [reset = h]

Short Description: R5SS0_VIM0_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1363. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8528h

Access Types Legend

Table 2-1364. R5SS0_VIM0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_CORE0_VIM Writing 000 will deassert the reset

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2.6.179 MSS_RCM_MSS_RCM_R5SS1_VIM0_RST_CTRL Registers

2.6.179.1 MSS_R5SS1_VIM0_RST_CTRL Register (Offset = 52Ch) [reset = h]

Short Description: R5SS1_VIM0_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1365. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 852Ch

Access Types Legend

Table 2-1366. R5SS1_VIM0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_CORE0_VIM Writing 000 will deassert the reset

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2.6.180 MSS_RCM_MSS_RCM_R5SS0_VIM1_RST_CTRL Registers

2.6.180.1 MSS_R5SS0_VIM1_RST_CTRL Register (Offset = 530h) [reset = h]

Short Description: R5SS0_VIM1_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1367. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8530h

Access Types Legend

Table 2-1368. R5SS0_VIM1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_CORE1_VIM

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2.6.181 MSS_RCM_MSS_RCM_R5SS1_VIM1_RST_CTRL Registers

2.6.181.1 MSS_R5SS1_VIM1_RST_CTRL Register (Offset = 534h) [reset = h]

Short Description: R5SS1_VIM1_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1369. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8534h

Access Types Legend

Table 2-1370. R5SS1_VIM1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_CORE1_VIM

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2.6.182 MSS_RCM_MSS_RCM_MCRC0_RST_CTRL Registers

2.6.182.1 MSS_MCRC0_RST_CTRL Register (Offset = 538h) [reset = h]

Short Description: MCRC0_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1371. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8538h

Access Types Legend

Table 2-1372. MCRC0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MCRC

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2.6.183 MSS_RCM_MSS_RCM_RTI0_RST_CTRL Registers

2.6.183.1 MSS_RTI0_RST_CTRL Register (Offset = 53Ch) [reset = h]

Short Description: RTI0_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1373. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 853Ch

Access Types Legend

Table 2-1374. RTI0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding RTI

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2.6.184 MSS_RCM_MSS_RCM_RTI1_RST_CTRL Registers

2.6.184.1 MSS_RTI1_RST_CTRL Register (Offset = 540h) [reset = h]

Short Description: RTI1_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1375. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8540h

Access Types Legend

Table 2-1376. RTI1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding RTI

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2.6.185 MSS_RCM_MSS_RCM_RTI2_RST_CTRL Registers

2.6.185.1 MSS_RTI2_RST_CTRL Register (Offset = 544h) [reset = h]

Short Description: RTI2_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1377. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8544h

Access Types Legend

Table 2-1378. RTI2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding RTI

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2.6.186 MSS_RCM_MSS_RCM_RTI3_RST_CTRL Registers

2.6.186.1 MSS_RTI3_RST_CTRL Register (Offset = 548h) [reset = h]

Short Description: RTI3_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1379. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8548h

Access Types Legend

Table 2-1380. RTI3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding RTI

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2.6.187 MSS_RCM_MSS_RCM_WDT0_RST_CTRL Registers

2.6.187.1 MSS_WDT0_RST_CTRL Register (Offset = 54Ch) [reset = h]

Short Description: WDT0_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1381. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 854Ch

Access Types Legend

Table 2-1382. WDT0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset WDT

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2.6.188 MSS_RCM_MSS_RCM_WDT1_RST_CTRL Registers

2.6.188.1 MSS_WDT1_RST_CTRL Register (Offset = 550h) [reset = h]

Short Description: WDT1_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1383. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8550h

Access Types Legend

Table 2-1384. WDT1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset WDT

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2.6.189 MSS_RCM_MSS_RCM_WDT2_RST_CTRL Registers

2.6.189.1 MSS_WDT2_RST_CTRL Register (Offset = 554h) [reset = h]

Short Description: WDT2_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1385. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8554h

Access Types Legend

Table 2-1386. WDT2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset WDT

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2.6.190 MSS_RCM_MSS_RCM_WDT3_RST_CTRL Registers

2.6.190.1 MSS_WDT3_RST_CTRL Register (Offset = 558h) [reset = h]

Short Description: WDT3_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1387. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8558h

Access Types Legend

Table 2-1388. WDT3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset WDT

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2.6.191 MSS_RCM_MSS_RCM_TOP_ESM_RST_CTRL Registers

2.6.191.1 MSS_TOP_ESM_RST_CTRL Register (Offset = 55Ch) [reset = h]

Short Description: TOP_ESM_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1389. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 855Ch

Access Types Legend

Table 2-1390. TOP_ESM_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset ESM

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2.6.192 MSS_RCM_MSS_RCM_DCC0_RST_CTRL Registers

2.6.192.1 MSS_DCC0_RST_CTRL Register (Offset = 560h) [reset = h]

Short Description: DCC0_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1391. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8560h

Access Types Legend

Table 2-1392. DCC0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset DCCA

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2.6.193 MSS_RCM_MSS_RCM_DCC1_RST_CTRL Registers

2.6.193.1 MSS_DCC1_RST_CTRL Register (Offset = 564h) [reset = h]

Short Description: DCC1_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1393. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8564h

Access Types Legend

Table 2-1394. DCC1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset DCCB

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2.6.194 MSS_RCM_MSS_RCM_DCC2_RST_CTRL Registers

2.6.194.1 MSS_DCC2_RST_CTRL Register (Offset = 568h) [reset = h]

Short Description: DCC2_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1395. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8568h

Access Types Legend

Table 2-1396. DCC2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset DCCC

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2.6.195 MSS_RCM_MSS_RCM_DCC3_RST_CTRL Registers

2.6.195.1 MSS_DCC3_RST_CTRL Register (Offset = 56Ch) [reset = h]

Short Description: DCC3_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1397. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 856Ch

Access Types Legend

Table 2-1398. DCC3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset DCCD

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2.6.196 MSS_RCM_MSS_RCM_MCSPI0_RST_CTRL Registers

2.6.196.1 MSS_MCSPI0_RST_CTRL Register (Offset = 570h) [reset = h]

Short Description: MCSPI0_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1399. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8570h

Access Types Legend

Table 2-1400. MCSPI0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI

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2.6.197 MSS_RCM_MSS_RCM_MCSPI1_RST_CTRL Registers

2.6.197.1 MSS_MCSPI1_RST_CTRL Register (Offset = 574h) [reset = h]

Short Description: MCSPI1_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1401. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8574h

Access Types Legend

Table 2-1402. MCSPI1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI

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2.6.198 MSS_RCM_MSS_RCM_MCSPI2_RST_CTRL Registers

2.6.198.1 MSS_MCSPI2_RST_CTRL Register (Offset = 578h) [reset = h]

Short Description: MCSPI2_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1403. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8578h

Access Types Legend

Table 2-1404. MCSPI2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI

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2.6.199 MSS_RCM_MSS_RCM_MCSPI3_RST_CTRL Registers

2.6.199.1 MSS_MCSPI3_RST_CTRL Register (Offset = 57Ch) [reset = h]

Short Description: MCSPI3_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1405. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 857Ch

Access Types Legend

Table 2-1406. MCSPI3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI

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2.6.200 MSS_RCM_MSS_RCM_MCSPI4_RST_CTRL Registers

2.6.200.1 MSS_MCSPI4_RST_CTRL Register (Offset = 580h) [reset = h]

Short Description: MCSPI4_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1407. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8580h

Access Types Legend

Table 2-1408. MCSPI4_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI

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2.6.201 MSS_RCM_MSS_RCM_QSPI0_RST_CTRL Registers

2.6.201.1 MSS_QSPI0_RST_CTRL Register (Offset = 584h) [reset = h]

Short Description: QSPI0_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1409. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8584h

Access Types Legend

Table 2-1410. QSPI0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset QSPI

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2.6.202 MSS_RCM_MSS_RCM_MCAN0_RST_CTRL Registers

2.6.202.1 MSS_MCAN0_RST_CTRL Register (Offset = 588h) [reset = h]

Short Description: MCAN0_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1411. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8588h

Access Types Legend

Table 2-1412. MCAN0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding MCAN

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2.6.203 MSS_RCM_MSS_RCM_MCAN1_RST_CTRL Registers

2.6.203.1 MSS_MCAN1_RST_CTRL Register (Offset = 58Ch) [reset = h]

Short Description: MCAN1_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1413. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 858Ch

Access Types Legend

Table 2-1414. MCAN1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding MCAN

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2.6.204 MSS_RCM_MSS_RCM_MCAN2_RST_CTRL Registers

2.6.204.1 MSS_MCAN2_RST_CTRL Register (Offset = 590h) [reset = h]

Short Description: MCAN2_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1415. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8590h

Access Types Legend

Table 2-1416. MCAN2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding MCAN

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2.6.205 MSS_RCM_MSS_RCM_MCAN3_RST_CTRL Registers

2.6.205.1 MSS_MCAN3_RST_CTRL Register (Offset = 594h) [reset = h]

Short Description: MCAN3_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1417. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8594h

Access Types Legend

Table 2-1418. MCAN3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding MCAN

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2.6.206 MSS_RCM_MSS_RCM_I2C0_RST_CTRL Registers

2.6.206.1 MSS_I2C0_RST_CTRL Register (Offset = 598h) [reset = h]

Short Description: I2C0_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1419. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8598h

Access Types Legend

Table 2-1420. I2C0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding I2C

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2.6.207 MSS_RCM_MSS_RCM_I2C1_RST_CTRL Registers

2.6.207.1 MSS_I2C1_RST_CTRL Register (Offset = 59Ch) [reset = h]

Short Description: I2C1_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1421. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 859Ch

Access Types Legend

Table 2-1422. I2C1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding I2C

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2.6.208 MSS_RCM_MSS_RCM_I2C2_RST_CTRL Registers

2.6.208.1 MSS_I2C2_RST_CTRL Register (Offset = 5A0h) [reset = h]

Short Description: I2C2_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1423. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85A0h

Access Types Legend

Table 2-1424. I2C2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding I2C

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2.6.209 MSS_RCM_MSS_RCM_I2C3_RST_CTRL Registers

2.6.209.1 MSS_I2C3_RST_CTRL Register (Offset = 5A4h) [reset = h]

Short Description: I2C3_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1425. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85A4h

Access Types Legend

Table 2-1426. I2C3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding I2C

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2.6.210 MSS_RCM_MSS_RCM_UART0_RST_CTRL Registers

2.6.210.1 MSS_UART0_RST_CTRL Register (Offset = 5A8h) [reset = h]

Short Description: UART0_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1427. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85A8h

Access Types Legend

Table 2-1428. UART0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance

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2.6.211 MSS_RCM_MSS_RCM_UART1_RST_CTRL Registers

2.6.211.1 MSS_UART1_RST_CTRL Register (Offset = 5ACh) [reset = h]

Short Description: UART1_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1429. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85ACh

Access Types Legend

Table 2-1430. UART1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance

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2.6.212 MSS_RCM_MSS_RCM_UART2_RST_CTRL Registers

2.6.212.1 MSS_UART2_RST_CTRL Register (Offset = 5B0h) [reset = h]

Short Description: UART2_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1431. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85B0h

Access Types Legend

Table 2-1432. UART2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance

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2.6.213 MSS_RCM_MSS_RCM_UART3_RST_CTRL Registers

2.6.213.1 MSS_UART3_RST_CTRL Register (Offset = 5B4h) [reset = h]

Short Description: UART3_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1433. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85B4h

Access Types Legend

Table 2-1434. UART3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance

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2.6.214 MSS_RCM_MSS_RCM_UART4_RST_CTRL Registers

2.6.214.1 MSS_UART4_RST_CTRL Register (Offset = 5B8h) [reset = h]

Short Description: UART4_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1435. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85B8h

Access Types Legend

Table 2-1436. UART4_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance

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2.6.215 MSS_RCM_MSS_RCM_UART5_RST_CTRL Registers

2.6.215.1 MSS_UART5_RST_CTRL Register (Offset = 5BCh) [reset = h]

Short Description: UART5_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1437. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85BCh

Access Types Legend

Table 2-1438. UART5_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance

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2.6.216 MSS_RCM_MSS_RCM_LIN0_RST_CTRL Registers

2.6.216.1 MSS_LIN0_RST_CTRL Register (Offset = 5C0h) [reset = h]

Short Description: LIN0_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1439. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85C0h

Access Types Legend

Table 2-1440. LIN0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset LIN

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2.6.217 MSS_RCM_MSS_RCM_LIN1_RST_CTRL Registers

2.6.217.1 MSS_LIN1_RST_CTRL Register (Offset = 5C4h) [reset = h]

Short Description: LIN1_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1441. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85C4h

Access Types Legend

Table 2-1442. LIN1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset LIN

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2.6.218 MSS_RCM_MSS_RCM_LIN2_RST_CTRL Registers

2.6.218.1 MSS_LIN2_RST_CTRL Register (Offset = 5C8h) [reset = h]

Short Description: LIN2_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1443. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85C8h

Access Types Legend

Table 2-1444. LIN2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset LIN

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2.6.219 MSS_RCM_MSS_RCM_LIN3_RST_CTRL Registers

2.6.219.1 MSS_LIN3_RST_CTRL Register (Offset = 5CCh) [reset = h]

Short Description: LIN3_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1445. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85CCh

Access Types Legend

Table 2-1446. LIN3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset LIN

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2.6.220 MSS_RCM_MSS_RCM_LIN4_RST_CTRL Registers

2.6.220.1 MSS_LIN4_RST_CTRL Register (Offset = 5D0h) [reset = h]

Short Description: LIN4_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1447. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85D0h

Access Types Legend

Table 2-1448. LIN4_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset LIN

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2.6.221 MSS_RCM_MSS_RCM_EDMA_RST_CTRL Registers

2.6.221.1 MSS_EDMA_RST_CTRL Register (Offset = 5D8h) [reset = h]

Short Description: EDMA_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1449. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85D8h

Access Types Legend

Table 2-1450. EDMA_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
14 - 12	TPTCA1_ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_TPTCA1
	RESERVED	NONE		Reserved
10 - 8	TPTCA0_ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_TPTCA0
	RESERVED	NONE		Reserved
6 - 4	TPCCA_ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_TPCCA
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset EDMA

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2.6.222 MSS_RCM_MSS_RCM_INFRA_RST_CTRL Registers

2.6.222.1 MSS_INFRA_RST_CTRL Register (Offset = 5DCh) [reset = h]

Short Description: INFRA_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1451. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85DCh

Access Types Legend

Table 2-1452. INFRA_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS INFRA

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2.6.223 MSS_RCM_MSS_RCM_CPSW_RST_CTRL Registers

2.6.223.1 MSS_CPSW_RST_CTRL Register (Offset = 5E0h) [reset = h]

Short Description: CPSW_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1453. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85E0h

Access Types Legend

Table 2-1454. CPSW_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS CPSW

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2.6.224 MSS_RCM_MSS_RCM_ICSSM0_RST_CTRL Registers

2.6.224.1 MSS_ICSSM0_RST_CTRL Register (Offset = 5E4h) [reset = h]

Short Description: ICSSM0_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1455. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85E4h

Access Types Legend

Table 2-1456. ICSSM0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS ICSSM

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2.6.225 MSS_RCM_MSS_RCM_MMC0_RST_CTRL Registers

2.6.225.1 MSS_MMC0_RST_CTRL Register (Offset = 5E8h) [reset = h]

Short Description: MMC0_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1457. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85E8h

Access Types Legend

Table 2-1458. MMC0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MMCSD

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2.6.226 MSS_RCM_MSS_RCM_GPIO0_RST_CTRL Registers

2.6.226.1 MSS_GPIO0_RST_CTRL Register (Offset = 5ECh) [reset = h]

Short Description: GPIO0_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1459. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85ECh

Access Types Legend

Table 2-1460. GPIO0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding GPIO

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2.6.227 MSS_RCM_MSS_RCM_GPIO1_RST_CTRL Registers

2.6.227.1 MSS_GPIO1_RST_CTRL Register (Offset = 5F0h) [reset = h]

Short Description: GPIO1_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1461. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85F0h

Access Types Legend

Table 2-1462. GPIO1_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding GPIO

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2.6.228 MSS_RCM_MSS_RCM_GPIO2_RST_CTRL Registers

2.6.228.1 MSS_GPIO2_RST_CTRL Register (Offset = 5F4h) [reset = h]

Short Description: GPIO2_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1463. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85F4h

Access Types Legend

Table 2-1464. GPIO2_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding GPIO

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2.6.229 MSS_RCM_MSS_RCM_GPIO3_RST_CTRL Registers

2.6.229.1 MSS_GPIO3_RST_CTRL Register (Offset = 5F8h) [reset = h]

Short Description: GPIO3_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1465. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85F8h

Access Types Legend

Table 2-1466. GPIO3_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding GPIO

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2.6.230 MSS_RCM_MSS_RCM_SPINLOCK0_RST_CTRL Registers

2.6.230.1 MSS_SPINLOCK0_RST_CTRL Register (Offset = 5FCh) [reset = h]

Short Description: SPINLOCK0_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1467. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 85FCh

Access Types Legend

Table 2-1468. SPINLOCK0_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset SPINLOCK

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2.6.231 MSS_RCM_MSS_RCM_GPMC_RST_CTRL Registers

2.6.231.1 MSS_GPMC_RST_CTRL Register (Offset = 600h) [reset = h]

Short Description: GPMC_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1469. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8600h

Access Types Legend

Table 2-1470. GPMC_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset GPMC

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2.6.232 MSS_RCM_MSS_RCM_TEMPSENSE_32K_RST_CTRL Registers

2.6.232.1 MSS_TEMPSENSE_32K_RST_CTRL Register (Offset = 604h) [reset = h]

Short Description: TEMPSENSE_32K_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1471. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8604h

Access Types Legend

Table 2-1472. TEMPSENSE_32K_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset TEMPSENSE

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2.6.233 MSS_RCM_MSS_RCM_MSS_ELM_RST_CTRL Registers

2.6.233.1 MSS_MSS_ELM_RST_CTRL Register (Offset = 608h) [reset = h]

Short Description: MSS_ELM_RST_CTRL register

Long Description:

Return to Summary Table

Table 2-1473. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8608h

Access Types Legend

Table 2-1474. MSS_ELM_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ASSERT	RW	0h	This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset ELM

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2.6.234 MSS_RCM_MSS_RCM_L2OCRAM_BANK0_PD_CTRL Registers

2.6.234.1 MSS_L2OCRAM_BANK0_PD_CTRL Register (Offset = 700h) [reset = h]

Short Description: L2OCRAM_BANK0_PD_CTRL register

Long Description:

Return to Summary Table

Table 2-1475. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8700h

Access Types Legend

Table 2-1476. L2OCRAM_BANK0_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 8	AGOODIN	RW	6Fh	SW control for power signal 'AGOODIN' for MSS_L2_BANKA
	RESERVED	NONE		Reserved
6 - 4	AONIN	RW	6Fh	SW control for power signal 'AONIN' for MSS_L2_BANKA
	RESERVED	NONE		Reserved
2 - 0	ISO	RW	0h	SW control for power signal 'ISO' for MSS_L2_BANKA

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2.6.235 MSS_RCM_MSS_RCM_L2OCRAM_BANK1_PD_CTRL Registers

2.6.235.1 MSS_L2OCRAM_BANK1_PD_CTRL Register (Offset = 704h) [reset = h]

Short Description: L2OCRAM_BANK1_PD_CTRL register

Long Description:

Return to Summary Table

Table 2-1477. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8704h

Access Types Legend

Table 2-1478. L2OCRAM_BANK1_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 8	AGOODIN	RW	6Fh	SW control for power signal 'AGOODIN' for MSS_L2_BANKB
	RESERVED	NONE		Reserved
6 - 4	AONIN	RW	6Fh	SW control for power signal 'AONIN' for MSS_L2_BANKB
	RESERVED	NONE		Reserved
2 - 0	ISO	RW	0h	SW control for power signal 'ISO' for MSS_L2_BANKB

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2.6.236 MSS_RCM_MSS_RCM_L2OCRAM_BANK2_PD_CTRL Registers

2.6.236.1 MSS_L2OCRAM_BANK2_PD_CTRL Register (Offset = 708h) [reset = h]

Short Description: L2OCRAM_BANK2_PD_CTRL register

Long Description:

Return to Summary Table

Table 2-1479. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8708h

Access Types Legend

Table 2-1480. L2OCRAM_BANK2_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 8	AGOODIN	RW	6Fh	SW control for power signal 'AGOODIN' for MSS_L2_BANKC
	RESERVED	NONE		Reserved
6 - 4	AONIN	RW	6Fh	SW control for power signal 'AONIN' for MSS_L2_BANKC
	RESERVED	NONE		Reserved
2 - 0	ISO	RW	0h	SW control for power signal 'ISO' for MSS_L2_BANKC

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2.6.237 MSS_RCM_MSS_RCM_L2OCRAM_BANK3_PD_CTRL Registers

2.6.237.1 MSS_L2OCRAM_BANK3_PD_CTRL Register (Offset = 70Ch) [reset = h]

Short Description: L2OCRAM_BANK3_PD_CTRL register

Long Description:

Return to Summary Table

Table 2-1481. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 870Ch

Access Types Legend

Table 2-1482. L2OCRAM_BANK3_PD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 8	AGOODIN	RW	6Fh	SW control for power signal 'AGOODIN' for MSS_L2_BANKD
	RESERVED	NONE		Reserved
6 - 4	AONIN	RW	6Fh	SW control for power signal 'AONIN' for MSS_L2_BANKD
	RESERVED	NONE		Reserved
2 - 0	ISO	RW	0h	SW control for power signal 'ISO' for MSS_L2_BANKD

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2.6.238 MSS_RCM_MSS_RCM_L2OCRAM_BANK0_PD_STATUS Registers

2.6.238.1 MSS_L2OCRAM_BANK0_PD_STATUS Register (Offset = 710h) [reset = h]

Short Description: L2OCRAM_BANK0_PD_STATUS register

Long Description:

Return to Summary Table

Table 2-1483. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8710h

Access Types Legend

Table 2-1484. L2OCRAM_BANK0_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	AGOODOUT	RO	1h	SW status indicating the 'pgoodin' of MSS_L2_BANKA
0	AONOUT	RO	1h	SW status indicating the 'ponin' of MSS_L2_BANKA

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2.6.239 MSS_RCM_MSS_RCM_L2OCRAM_BANK1_PD_STATUS Registers

2.6.239.1 MSS_L2OCRAM_BANK1_PD_STATUS Register (Offset = 714h) [reset = h]

Short Description: L2OCRAM_BANK1_PD_STATUS register

Long Description:

Return to Summary Table

Table 2-1485. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8714h

Access Types Legend

Table 2-1486. L2OCRAM_BANK1_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	AGOODOUT	RO	1h	SW status indicating the 'pgoodin' of MSS_L2_BANKB
0	AONOUT	RO	1h	SW status indicating the 'ponin' of MSS_L2_BANKB

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2.6.240 MSS_RCM_MSS_RCM_L2OCRAM_BANK2_PD_STATUS Registers

2.6.240.1 MSS_L2OCRAM_BANK2_PD_STATUS Register (Offset = 718h) [reset = h]

Short Description: L2OCRAM_BANK2_PD_STATUS register

Long Description:

Return to Summary Table

Table 2-1487. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8718h

Access Types Legend

Table 2-1488. L2OCRAM_BANK2_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	AGOODOUT	RO	1h	SW status indicating the 'pgoodin' of MSS_L2_BANKC
0	AONOUT	RO	1h	SW status indicating the 'ponin' of MSS_L2_BANKC

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2.6.241 MSS_RCM_MSS_RCM_L2OCRAM_BANK3_PD_STATUS Registers

2.6.241.1 MSS_L2OCRAM_BANK3_PD_STATUS Register (Offset = 71Ch) [reset = h]

Short Description: L2OCRAM_BANK3_PD_STATUS register

Long Description:

Return to Summary Table

Table 2-1489. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 871Ch

Access Types Legend

Table 2-1490. L2OCRAM_BANK3_PD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	AGOODOUT	RO	1h	SW status indicating the 'pgoodin' of MSS_L2_BANKD
0	AONOUT	RO	1h	SW status indicating the 'ponin' of MSS_L2_BANKD

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2.6.242 MSS_RCM_MSS_RCM_HW_REG0 Registers

2.6.242.1 MSS_HW_REG0 Register (Offset = 720h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1491. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8720h

Figure 2-1. MSS_RCM_HW_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HWREG															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HWREG															
RW															
0															

Access Types Legend

Table 2-1492. HW_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HWREG	RW	0h	HW Reserved regiser

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2.6.243 MSS_RCM_MSS_RCM_HW_REG1 Registers

2.6.243.1 MSS_HW_REG1 Register (Offset = 724h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1493. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8724h

Figure 2-2. MSS_RCM_HW_REG1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HWREG															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HWREG															
RW															
0															

Access Types Legend

Table 2-1494. HW_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HWREG	RW	0h	HW Reserved regiser

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2.6.244 MSS_RCM_MSS_RCM_HW_REG2 Registers

2.6.244.1 MSS_HW_REG2 Register (Offset = 728h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1495. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8728h

Figure 2-3. MSS_RCM_HW_REG2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HWREG															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HWREG															
RW															
0															

Access Types Legend

Table 2-1496. HW_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HWREG	RW	0h	HW Reserved regiser

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2.6.245 MSS_RCM_MSS_RCM_HW_REG3 Registers

2.6.245.1 MSS_HW_REG3 Register (Offset = 72Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1497. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 872Ch

Figure 2-4. MSS_RCM_HW_REG3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HWREG															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HWREG															
RW															
0															

Access Types Legend

Table 2-1498. HW_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HWREG	RW	0h	HW Reserved regiser

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2.6.246 MSS_RCM_MSS_RCM_HSM_RTIA_CLK_SRC_SEL Registers

2.6.246.1 MSS_HSM_RTIA_CLK_SRC_SEL Register (Offset = 800h) [reset = h]

Short Description: HSM_RTIA_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1499. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8800h

Access Types Legend

Table 2-1500. HSM_RTIA_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	HSM_RTI0_CLK_SRC_SEL	RW	0h	Select line for selecting source clock for HSM_Corresponding RTI.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.247 MSS_RCM_MSS_RCM_HSM_WDT_CLK_SRC_SEL Registers

2.6.247.1 MSS_HSM_WDT_CLK_SRC_SEL Register (Offset = 804h) [reset = h]

Short Description: HSM_WDT_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1501. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8804h

Access Types Legend

Table 2-1502. HSM_WDT_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	HSM_WDT0_CLK_SRC_SEL	RW	0h	Select line for selecting source clock for HSM_WDT.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.248 MSS_RCM_MSS_RCM_HSM_RTC_CLK_SRC_SEL Registers

2.6.248.1 MSS_HSM_RTC_CLK_SRC_SEL Register (Offset = 808h) [reset = h]

Short Description: HSM_RTC_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1503. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8808h

Access Types Legend

Table 2-1504. HSM_RTC_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	HSM_RTC0_CLK_SRC_SEL	RW	295AD7F5Fh	Select line for selecting source clock for HSM_RTC.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.249 MSS_RCM_MSS_RCM_HSM_DMTA_CLK_SRC_SEL Registers

2.6.249.1 MSS_HSM_DMTA_CLK_SRC_SEL Register (Offset = 80Ch) [reset = h]

Short Description: HSM_DMTA_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1505. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 880Ch

Access Types Legend

Table 2-1506. HSM_DMTA_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	HSM_DTM0_CLK_SRC_SEL	RW	0h	Select line for selecting source clock for HSM_DMTA.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.250 MSS_RCM_MSS_RCM_HSM_DMTB_CLK_SRC_SEL Registers

2.6.250.1 MSS_HSM_DMTB_CLK_SRC_SEL Register (Offset = 810h) [reset = h]

Short Description: HSM_DMTB_CLK_SRC_SEL register

Long Description:

Return to Summary Table

Table 2-1507. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8810h

Access Types Legend

Table 2-1508. HSM_DMTB_CLK_SRC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	HSM_DTM1_CLK_SRC_SEL	RW	0h	Select line for selecting source clock for HSM_DMTB.Data should be loaded as multibit. For example: if '0x5' should be selected then '0x555' should be configured to the register.

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2.6.251 MSS_RCM_MSS_RCM_HSM_RTI_CLK_DIV_VAL Registers

2.6.251.1 MSS_HSM_RTI_CLK_DIV_VAL Register (Offset = 814h) [reset = h]

Short Description: HSM_RTI_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1509. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8814h

Access Types Legend

Table 2-1510. HSM_RTI_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value HSM RTI selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.252 MSS_RCM_MSS_RCM_HSM_WDT_CLK_DIV_VAL Registers

2.6.252.1 MSS_HSM_WDT_CLK_DIV_VAL Register (Offset = 818h) [reset = h]

Short Description: HSM_WDT_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1511. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8818h

Access Types Legend

Table 2-1512. HSM_WDT_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value HSM WDT selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.253 MSS_RCM_MSS_RCM_HSM_RTC_CLK_DIV_VAL Registers

2.6.253.1 MSS_HSM_RTC_CLK_DIV_VAL Register (Offset = 81Ch) [reset = h]

Short Description: HSM_RTC_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1513. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 881Ch

Access Types Legend

Table 2-1514. HSM_RTC_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value HSM RTC selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.254 MSS_RCM_MSS_RCM_HSM_DMTA_CLK_DIV_VAL Registers

2.6.254.1 MSS_HSM_DMTA_CLK_DIV_VAL Register (Offset = 820h) [reset = h]

Short Description: HSM_DMTA_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1515. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8820h

Access Types Legend

Table 2-1516. HSM_DMTA_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value HSM DMTA selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.255 MSS_RCM_MSS_RCM_HSM_DMTB_CLK_DIV_VAL Registers

2.6.255.1 MSS_HSM_DMTB_CLK_DIV_VAL Register (Offset = 824h) [reset = h]

Short Description: HSM_DMTB_CLK_DIV_VAL register

Long Description:

Return to Summary Table

Table 2-1517. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8824h

Access Types Legend

Table 2-1518. HSM_DMTB_CLK_DIV_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	CLKDIVR	RW	0h	Divider value HSM DMTB selected clock.Data should be loaded as multibit. For example: if divider value of '0x8' should be selected then '0x888' should be configured to the register.Refer to AM602 clock spec for clock reference

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2.6.256 MSS_RCM_MSS_RCM_HSM_RTI_CLK_GATE Registers

2.6.256.1 MSS_HSM_RTI_CLK_GATE Register (Offset = 828h) [reset = h]

Short Description: HSM_RTI_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1519. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8828h

Access Types Legend

Table 2-1520. HSM_RTI_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for HSM RTI

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2.6.257 MSS_RCM_MSS_RCM_HSM_WDT_CLK_GATE Registers

2.6.257.1 MSS_HSM_WDT_CLK_GATE Register (Offset = 82Ch) [reset = h]

Short Description: HSM_WDT_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1521. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 882Ch

Access Types Legend

Table 2-1522. HSM_WDT_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for HSM WDT

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2.6.258 MSS_RCM_MSS_RCM_HSM_RTC_CLK_GATE Registers

2.6.258.1 MSS_HSM_RTC_CLK_GATE Register (Offset = 830h) [reset = h]

Short Description: HSM_RTC_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1523. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8830h

Access Types Legend

Table 2-1524. HSM_RTC_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for HSM RTC

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2.6.259 MSS_RCM_MSS_RCM_HSM_DMTA_CLK_GATE Registers

2.6.259.1 MSS_HSM_DMTA_CLK_GATE Register (Offset = 834h) [reset = h]

Short Description: HSM_DMTA_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1525. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8834h

Access Types Legend

Table 2-1526. HSM_DMTA_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for HSM DMTA

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2.6.260 MSS_RCM_MSS_RCM_HSM_DMTB_CLK_GATE Registers

2.6.260.1 MSS_HSM_DMTB_CLK_GATE Register (Offset = 838h) [reset = h]

Short Description: HSM_DMTB_CLK_GATE register

Long Description:

Return to Summary Table

Table 2-1527. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8838h

Access Types Legend

Table 2-1528. HSM_DMTB_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GATED	RW	0h	Writing 3'b111 will gate clock for HSM DMTB

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2.6.261 MSS_RCM_MSS_RCM_HSM_RTI_CLK_STATUS Registers

2.6.261.1 MSS_HSM_RTI_CLK_STATUS Register (Offset = 83Ch) [reset = h]

Short Description: HSM_RTI_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1529. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 883Ch

Access Types Legend

Table 2-1530. HSM_RTI_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for HSM_RTI
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for HSM_RTI

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2.6.262 MSS_RCM_MSS_RCM_HSM_WDT_CLK_STATUS Registers

2.6.262.1 MSS_HSM_WDT_CLK_STATUS Register (Offset = 840h) [reset = h]

Short Description: HSM_WDT_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1531. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8840h

Access Types Legend

Table 2-1532. HSM_WDT_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for HSM_WDT
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for HSM_WDT

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2.6.263 MSS_RCM_MSS_RCM_HSM_RTC_CLK_STATUS Registers

2.6.263.1 MSS_HSM_RTC_CLK_STATUS Register (Offset = 844h) [reset = h]

Short Description: HSM_RTC_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1533. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8844h

Access Types Legend

Table 2-1534. HSM_RTC_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for HSM_RTC
7 - 0	CLKINUSE	RO	989680h	Status shows the source clock slected for HSM_RTC

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2.6.264 MSS_RCM_MSS_RCM_HSM_DMTA_CLK_STATUS Registers

2.6.264.1 MSS_HSM_DMTA_CLK_STATUS Register (Offset = 848h) [reset = h]

Short Description: HSM_DMTA_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1535. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8848h

Access Types Legend

Table 2-1536. HSM_DMTA_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for HSM_DMTA
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for HSM_DMTA

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2.6.265 MSS_RCM_MSS_RCM_HSM_DMTB_CLK_STATUS Registers

2.6.265.1 MSS_HSM_DMTB_CLK_STATUS Register (Offset = 84Ch) [reset = h]

Short Description: HSM_DMTB_CLK_STATUS register

Long Description:

Return to Summary Table

Table 2-1537. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 884Ch

Access Types Legend

Table 2-1538. HSM_DMTB_CLK_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CURRDIVIDER	RO	0h	Status shows the current divider value choosen for HSM_DMTB
7 - 0	CLKINUSE	RO	1h	Status shows the source clock slected for HSM_DMTB

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2.6.266 MSS_RCM_MSS_RCM_HW_SPARE_RW0 Registers

2.6.266.1 MSS_HW_SPARE_RW0 Register (Offset = FD0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1539. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FD0h

Figure 2-5. MSS_RCM_HW_SPARE_RW0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW0															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW0															
RW															
0															

Access Types Legend

Table 2-1540. HW_SPARE_RW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RW0	RW	0h	Reserved for HW R&D

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2.6.267 MSS_RCM_MSS_RCM_HW_SPARE_RW1 Registers

2.6.267.1 MSS_HW_SPARE_RW1 Register (Offset = FD4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1541. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FD4h

Figure 2-6. MSS_RCM_HW_SPARE_RW1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW1															
RW															
0															

Access Types Legend

Table 2-1542. HW_SPARE_RW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RW1	RW	0h	Reserved for HW R&D

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2.6.268 MSS_RCM_MSS_RCM_HW_SPARE_RW2 Registers

2.6.268.1 MSS_HW_SPARE_RW2 Register (Offset = FD8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1543. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FD8h

Figure 2-7. MSS_RCM_HW_SPARE_RW2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW2															
RW															
0															

Access Types Legend

Table 2-1544. HW_SPARE_RW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RW2	RW	0h	Reserved for HW R&D

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2.6.269 MSS_RCM_MSS_RCM_HW_SPARE_RW3 Registers

2.6.269.1 MSS_HW_SPARE_RW3 Register (Offset = FDCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1545. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FDCh

Figure 2-8. MSS_RCM_HW_SPARE_RW3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RW3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RW3															
RW															
0															

Access Types Legend

Table 2-1546. HW_SPARE_RW3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RW3	RW	0h	Reserved for HW R&D

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2.6.270 MSS_RCM_MSS_RCM_HW_SPARE_RO0 Registers

2.6.270.1 MSS_HW_SPARE_RO0 Register (Offset = FE0h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-1547. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FE0h

Figure 2-9. MSS_RCM_HW_SPARE_RO0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO0															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO0															
RO															
0															

Access Types Legend

Table 2-1548. HW_SPARE_RO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RO0	RO	0h	Reserved for HW R&D

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2.6.271 MSS_RCM_MSS_RCM_HW_SPARE_RO1 Registers

2.6.271.1 MSS_HW_SPARE_RO1 Register (Offset = FE4h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-1549. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FE4h

Figure 2-10. MSS_RCM_HW_SPARE_RO1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO1															
RO															
0															

Access Types Legend

Table 2-1550. HW_SPARE_RO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RO1	RO	0h	Reserved for HW R&D

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2.6.272 MSS_RCM_MSS_RCM_HW_SPARE_RO2 Registers

2.6.272.1 MSS_HW_SPARE_RO2 Register (Offset = FE8h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-1551. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FE8h

Figure 2-11. MSS_RCM_HW_SPARE_RO2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO2															
RO															
0															

Access Types Legend

Table 2-1552. HW_SPARE_RO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RO2	RO	0h	Reserved for HW R&D

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2.6.273 MSS_RCM_MSS_RCM_HW_SPARE_RO3 Registers

2.6.273.1 MSS_HW_SPARE_RO3 Register (Offset = FECh) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 2-1553. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FECh

Figure 2-12. MSS_RCM_HW_SPARE_RO3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_RO3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_RO3															
RO															
0															

Access Types Legend

Table 2-1554. HW_SPARE_RO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_RO3	RO	0h	Reserved for HW R&D

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2.6.274 MSS_RCM_MSS_RCM_HW_SPARE_WPH Registers

2.6.274.1 MSS_HW_SPARE_WPH Register (Offset = FF0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1555. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FF0h

Figure 2-13. MSS_RCM_HW_SPARE_WPH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_WPH															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_WPH															
RW															
0															

Access Types Legend

Table 2-1556. HW_SPARE_WPH Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	HW_SPARE_WPH	RW	0h	Reserved for HW R&D

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2.6.275 MSS_RCM_MSS_RCM_HW_SPARE_REC Registers

2.6.275.1 MSS_HW_SPARE_REC Register (Offset = FF4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 2-1557. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 8FF4h

Figure 2-14. MSS_RCM_HW_SPARE_REC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_SPARE_REC31	HW_SPARE_REC30	HW_SPARE_REC29	HW_SPARE_REC28	HW_SPARE_REC27	HW_SPARE_REC26	HW_SPARE_REC25	HW_SPARE_REC24	HW_SPARE_REC23	HW_SPARE_REC22	HW_SPARE_REC21	HW_SPARE_REC20	HW_SPARE_REC19	HW_SPARE_REC18	HW_SPARE_REC17	HW_SPARE_REC16
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_SPARE_REC15	HW_SPARE_REC14	HW_SPARE_REC13	HW_SPARE_REC12	HW_SPARE_REC11	HW_SPARE_REC10	HW_SPARE_REC9	HW_SPARE_REC8	HW_SPARE_REC7	HW_SPARE_REC6	HW_SPARE_REC5	HW_SPARE_REC4	HW_SPARE_REC3	HW_SPARE_REC2	HW_SPARE_REC1	HW_SPARE_REC0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 2-1558. HW_SPARE_REC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HW_SPARE_REC31	RW	0h	Reserved for HW R&D
30	HW_SPARE_REC30	RW	0h	Reserved for HW R&D
29	HW_SPARE_REC29	RW	0h	Reserved for HW R&D
28	HW_SPARE_REC28	RW	0h	Reserved for HW R&D
27	HW_SPARE_REC27	RW	0h	Reserved for HW R&D
26	HW_SPARE_REC26	RW	0h	Reserved for HW R&D
25	HW_SPARE_REC25	RW	0h	Reserved for HW R&D
24	HW_SPARE_REC24	RW	0h	Reserved for HW R&D
23	HW_SPARE_REC23	RW	0h	Reserved for HW R&D
22	HW_SPARE_REC22	RW	0h	Reserved for HW R&D
21	HW_SPARE_REC21	RW	0h	Reserved for HW R&D
20	HW_SPARE_REC20	RW	0h	Reserved for HW R&D
19	HW_SPARE_REC19	RW	0h	Reserved for HW R&D
18	HW_SPARE_REC18	RW	0h	Reserved for HW R&D
17	HW_SPARE_REC17	RW	0h	Reserved for HW R&D
16	HW_SPARE_REC16	RW	0h	Reserved for HW R&D
15	HW_SPARE_REC15	RW	0h	Reserved for HW R&D
14	HW_SPARE_REC14	RW	0h	Reserved for HW R&D
13	HW_SPARE_REC13	RW	0h	Reserved for HW R&D
12	HW_SPARE_REC12	RW	0h	Reserved for HW R&D
11	HW_SPARE_REC11	RW	0h	Reserved for HW R&D
10	HW_SPARE_REC10	RW	0h	Reserved for HW R&D

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Table 2-1558. HW_SPARE_REC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	HW_SPARE_REC9	RW	0h	Reserved for HW R&D
8	HW_SPARE_REC8	RW	0h	Reserved for HW R&D
7	HW_SPARE_REC7	RW	0h	Reserved for HW R&D
6	HW_SPARE_REC6	RW	0h	Reserved for HW R&D
5	HW_SPARE_REC5	RW	0h	Reserved for HW R&D
4	HW_SPARE_REC4	RW	0h	Reserved for HW R&D
3	HW_SPARE_REC3	RW	0h	Reserved for HW R&D
2	HW_SPARE_REC2	RW	0h	Reserved for HW R&D
1	HW_SPARE_REC1	RW	0h	Reserved for HW R&D
0	HW_SPARE_REC0	RW	0h	Reserved for HW R&D

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2.6.276 MSS_RCM_MSS_RCM_LOCK0_KICK0 Registers

2.6.276.1 MSS_LOCK0_KICK0 Register (Offset = 1008h) [reset = h]

Short Description: - KICK0 component

Long Description:

Return to Summary Table

Table 2-1559. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9008h

Access Types Legend

Table 2-1560. LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	LOCK0_KICK0	RW	0h	- KICK0 component

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2.6.277 MSS_RCM_MSS_RCM_LOCK0_KICK1 Registers

2.6.277.1 MSS_LOCK0_KICK1 Register (Offset = 100Ch) [reset = h]

Short Description: - KICK1 component

Long Description:

Return to Summary Table

Table 2-1561. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 900Ch

Access Types Legend

Table 2-1562. LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	LOCK0_KICK1	RW	0h	- KICK1 component

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2.6.278 MSS_RCM_MSS_RCM_INTR_RAW_STATUS Registers

2.6.278.1 MSS_INTR_RAW_STATUS Register (Offset = 1010h) [reset = h]

Short Description: Interrupt Raw Status/Set Register

Long Description:

Return to Summary Table

Table 2-1563. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9010h

Access Types Legend

Table 2-1564. INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR	RW	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
2	KICK_ERR	RW	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
1	ADDR_ERR	RW	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
0	PROT_ERR	RW	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.

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2.6.279 MSS_RCM_MSS_RCM_INTR_ENABLED_STATUS_CLEAR Registers

2.6.279.1 MSS_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = h]

Short Description: Interrupt Enabled Status/Clear register

Long Description:

Return to Summary Table

Table 2-1565. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9014h

Access Types Legend

Table 2-1566. INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	ENABLED_PROXY_ERR	RW	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
2	ENABLED_KICK_ERR	RW	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
1	ENABLED_ADDR_ERR	RW	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
0	ENABLED_PROT_ERR	RW	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.

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2.6.280 MSS_RCM_MSS_RCM_INTR_ENABLE Registers

2.6.280.1 MSS_INTR_ENABLE Register (Offset = 1018h) [reset = h]

Short Description: Interrupt Enable register

Long Description:

Return to Summary Table

Table 2-1567. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9018h

Access Types Legend

Table 2-1568. INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR_EN	RW	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
2	KICK_ERR_EN	RW	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN	RW	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
0	PROT_ERR_EN	RW	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.

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2.6.281 MSS_RCM_MSS_RCM_INTR_ENABLE_CLEAR Registers

2.6.281.1 MSS_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = h]

Short Description: Interrupt Enable Clear register

Long Description:

Return to Summary Table

Table 2-1569. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 901Ch

Access Types Legend

Table 2-1570. INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR_EN_CLR	RW	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
2	KICK_ERR_EN_CLR	RW	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN_CLR	RW	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
0	PROT_ERR_EN_CLR	RW	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.

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2.6.282 MSS_RCM_MSS_RCM_EOI Registers

2.6.282.1 MSS_EOI Register (Offset = 1020h) [reset = h]

Short Description: EOI register

Long Description:

Return to Summary Table

Table 2-1571. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9020h

Access Types Legend

Table 2-1572. EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	EOI_VECTOR	RW	0h	EOI vector value. Write this with interrupt distribution value in the chip.

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2.6.283 MSS_RCM_MSS_RCM_FAULT_ADDRESS Registers

2.6.283.1 MSS_FAULT_ADDRESS Register (Offset = 1024h) [reset = h]

Short Description: Fault Address register

Long Description:

Return to Summary Table

Table 2-1573. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9024h

Access Types Legend

Table 2-1574. FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FAULT_ADDR	RO	0h	Fault Address.

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2.6.284 MSS_RCM_MSS_RCM_FAULT_TYPE_STATUS Registers

2.6.284.1 MSS_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = h]

Short Description: Fault Type Status register

Long Description:

Return to Summary Table

Table 2-1575. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9028h

Access Types Legend

Table 2-1576. FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	FAULT_NS	RO	0h	Non-secure access.
5 - 0	FAULT_TYPE	RO	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype ! = 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault

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2.6.285 MSS_RCM_MSS_RCM_FAULT_ATTR_STATUS Registers

2.6.285.1 MSS_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = h]

Short Description: Fault Attribute Status register

Long Description:

Return to Summary Table

Table 2-1577. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 902Ch

Access Types Legend

Table 2-1578. FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	FAULT_XID	RO	0h	XID.
19 - 8	FAULT_ROUTEID	RO	0h	Route ID.
7 - 0	FAULT_PRIVID	RO	0h	Privilege ID.

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2.6.286 MSS_RCM_MSS_RCM_FAULT_CLEAR Registers

2.6.286.1 MSS_FAULT_CLEAR Register (Offset = 1030h) [reset = h]

Short Description: Fault Clear register

Long Description:

Return to Summary Table

Table 2-1579. Instance Table

Instance Name	Physical Address
MSS_RCM	5320 9030h

Access Types Legend

Table 2-1580. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
0	FAULT_CLR	WO	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect.

2.6.287 Access Table

Table 2-1581. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
WO	WO	Write

2.7 CTRLMMR CONTROLSS_GLOBAL_CTRL Registers

These registers are documented in the respective CONTROLSS chapter.

Please refer to .

3 Real-time Control Subsystem (CONTROLSS) Registers

The Real-time Control Subsystem (CONTROLSS) registers are described in the following sections.

3.1 CONTROLSS 16-bit Register Access Note

Note

8-bit wide register access is **not allowed** for ADC, EPWM, DAC, CMPSS, EQEP, SDFM, and FSI MMR regions. 16-bit access must be used instead.

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3.2 ADC_CFG Registers

Table 3-1. CONTROLSS_ADC[0:2]_CFG Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_ADC0_CFG Physical Address	CONTROLSS_ADC1_CFG Physical Address	CONTROLSS_ADC2_CFG Physical Address
0h	16	ADC_CFG_ADCCTL1	502C 0000h	502C 1000h	502C 2000h
2h	16	ADC_CFG_ADCCTL2	502C 0002h	502C 1002h	502C 2002h
4h	16	ADC_CFG_ADCBURSTCTL	502C 0004h	502C 1004h	502C 2004h
6h	16	ADC_CFG_ADCINTFLG	502C 0006h	502C 1006h	502C 2006h
8h	16	ADC_CFG_ADCINTFLGCLR	502C 0008h	502C 1008h	502C 2008h
Ah	16	ADC_CFG_ADCINTOVF	502C 000Ah	502C 100Ah	502C 200Ah
Ch	16	ADC_CFG_ADCINTOVFCLR	502C 000Ch	502C 100Ch	502C 200Ch
Eh	16	ADC_CFG_ADCINTSEL1N2	502C 000Eh	502C 100Eh	502C 200Eh
10h	16	ADC_CFG_ADCINTSEL3N4	502C 0010h	502C 1010h	502C 2010h
12h	16	ADC_CFG_ADCSOCPRICTL	502C 0012h	502C 1012h	502C 2012h
14h	16	ADC_CFG_ADCINTSOCSEL1	502C 0014h	502C 1014h	502C 2014h
16h	16	ADC_CFG_ADCINTSOCSEL2	502C 0016h	502C 1016h	502C 2016h
18h	16	ADC_CFG_ADCSOCFLG1	502C 0018h	502C 1018h	502C 2018h
1Ah	16	ADC_CFG_ADCSOCFRC1	502C 001Ah	502C 101Ah	502C 201Ah
1Ch	16	ADC_CFG_ADCSOCOVF1	502C 001Ch	502C 101Ch	502C 201Ch
1Eh	16	ADC_CFG_ADCSOCOVFCLR1	502C 001Eh	502C 101Eh	502C 201Eh
20h	32	ADC_CFG_ADCSOC0CTL	502C 0020h	502C 1020h	502C 2020h
24h	32	ADC_CFG_ADCSOC1CTL	502C 0024h	502C 1024h	502C 2024h
28h	32	ADC_CFG_ADCSOC2CTL	502C 0028h	502C 1028h	502C 2028h
2Ch	32	ADC_CFG_ADCSOC3CTL	502C 002Ch	502C 102Ch	502C 202Ch
30h	32	ADC_CFG_ADCSOC4CTL	502C 0030h	502C 1030h	502C 2030h
34h	32	ADC_CFG_ADCSOC5CTL	502C 0034h	502C 1034h	502C 2034h
38h	32	ADC_CFG_ADCSOC6CTL	502C 0038h	502C 1038h	502C 2038h
3Ch	32	ADC_CFG_ADCSOC7CTL	502C 003Ch	502C 103Ch	502C 203Ch
40h	32	ADC_CFG_ADCSOC8CTL	502C 0040h	502C 1040h	502C 2040h
44h	32	ADC_CFG_ADCSOC9CTL	502C 0044h	502C 1044h	502C 2044h
48h	32	ADC_CFG_ADCSOC10CTL	502C 0048h	502C 1048h	502C 2048h
4Ch	32	ADC_CFG_ADCSOC11CTL	502C 004Ch	502C 104Ch	502C 204Ch
50h	32	ADC_CFG_ADCSOC12CTL	502C 0050h	502C 1050h	502C 2050h
54h	32	ADC_CFG_ADCSOC13CTL	502C 0054h	502C 1054h	502C 2054h
58h	32	ADC_CFG_ADCSOC14CTL	502C 0058h	502C 1058h	502C 2058h
5Ch	32	ADC_CFG_ADCSOC15CTL	502C 005Ch	502C 105Ch	502C 205Ch
60h	16	ADC_CFG_ADCEVTSTAT	502C 0060h	502C 1060h	502C 2060h
64h	16	ADC_CFG_ADCEVTCLR	502C 0064h	502C 1064h	502C 2064h
68h	16	ADC_CFG_ADCEVTSEL	502C 0068h	502C 1068h	502C 2068h
6Ch	16	ADC_CFG_ADCEVTINTSEL	502C 006Ch	502C 106Ch	502C 206Ch
70h	16	ADC_CFG_ADCOSDETECT	502C 0070h	502C 1070h	502C 2070h
72h	16	ADC_CFG_ADCCOUNTER	502C 0072h	502C 1072h	502C 2072h
74h	16	ADC_CFG_ADCREV	502C 0074h	502C 1074h	502C 2074h
76h	16	ADC_CFG_ADCOFFTRIM	502C 0076h	502C 1076h	502C 2076h
7Ch	32	ADC_CFG_ADCCONFIG	502C 007Ch	502C 107Ch	502C 207Ch
80h	16	ADC_CFG_ADCPPB1CONFIG	502C 0080h	502C 1080h	502C 2080h
82h	16	ADC_CFG_ADCPPB1STAMP	502C 0082h	502C 1082h	502C 2082h
84h	16	ADC_CFG_ADCPPB1OFFCAL	502C 0084h	502C 1084h	502C 2084h

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Table 3-1. CONTROLSS_ADC[0:2]_CFG Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_ADC0_CFG Physical Address	CONTROLSS_ADC1_CFG Physical Address	CONTROLSS_ADC2_CFG Physical Address
86h	16	ADC_CFG_ADCPPB1OFFREF	502C 0086h	502C 1086h	502C 2086h
88h	32	ADC_CFG_ADCPPB1TRIPHI	502C 0088h	502C 1088h	502C 2088h
8Ch	32	ADC_CFG_ADCPPB1TRIPLO	502C 008Ch	502C 108Ch	502C 208Ch
90h	16	ADC_CFG_ADCPPB2CONFIG	502C 0090h	502C 1090h	502C 2090h
92h	16	ADC_CFG_ADCPPB2STAMP	502C 0092h	502C 1092h	502C 2092h
94h	16	ADC_CFG_ADCPPB2OFFCAL	502C 0094h	502C 1094h	502C 2094h
96h	16	ADC_CFG_ADCPPB2OFFREF	502C 0096h	502C 1096h	502C 2096h
98h	32	ADC_CFG_ADCPPB2TRIPHI	502C 0098h	502C 1098h	502C 2098h
9Ch	32	ADC_CFG_ADCPPB2TRIPLO	502C 009Ch	502C 109Ch	502C 209Ch
A0h	16	ADC_CFG_ADCPPB3CONFIG	502C 00A0h	502C 10A0h	502C 20A0h
A2h	16	ADC_CFG_ADCPPB3STAMP	502C 00A2h	502C 10A2h	502C 20A2h
A4h	16	ADC_CFG_ADCPPB3OFFCAL	502C 00A4h	502C 10A4h	502C 20A4h
A6h	16	ADC_CFG_ADCPPB3OFFREF	502C 00A6h	502C 10A6h	502C 20A6h
A8h	32	ADC_CFG_ADCPPB3TRIPHI	502C 00A8h	502C 10A8h	502C 20A8h
ACh	32	ADC_CFG_ADCPPB3TRIPLO	502C 00ACh	502C 10ACh	502C 20ACh
B0h	16	ADC_CFG_ADCPPB4CONFIG	502C 00B0h	502C 10B0h	502C 20B0h
B2h	16	ADC_CFG_ADCPPB4STAMP	502C 00B2h	502C 10B2h	502C 20B2h
B4h	16	ADC_CFG_ADCPPB4OFFCAL	502C 00B4h	502C 10B4h	502C 20B4h
B6h	16	ADC_CFG_ADCPPB4OFFREF	502C 00B6h	502C 10B6h	502C 20B6h
B8h	32	ADC_CFG_ADCPPB4TRIPHI	502C 00B8h	502C 10B8h	502C 20B8h
BCh	32	ADC_CFG_ADCPPB4TRIPLO	502C 00BCh	502C 10BCh	502C 20BCh
DEh	16	ADC_CFG_ADCINTCYCLE	502C 00DEh	502C 10DEh	502C 20DEh
E0h	32	ADC_CFG_ADCINLTRIM1	502C 00E0h	502C 10E0h	502C 20E0h
E4h	32	ADC_CFG_ADCINLTRIM2	502C 00E4h	502C 10E4h	502C 20E4h
E8h	32	ADC_CFG_ADCINLTRIM3	502C 00E8h	502C 10E8h	502C 20E8h
ECh	32	ADC_CFG_ADCINLTRIM4	502C 00ECh	502C 10ECh	502C 20ECh
F0h	32	ADC_CFG_ADCINLTRIM5	502C 00F0h	502C 10F0h	502C 20F0h
F4h	32	ADC_CFG_ADCINLTRIM6	502C 00F4h	502C 10F4h	502C 20F4h
FCh	32	ADC_CFG_ADCINLTRIMCTL	502C 00FCh	502C 10FCh	502C 20FCh

Table 3-2. CONTROLSS_ADC[3:4]_CFG Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_ADC3_CFG Physical Address	CONTROLSS_ADC4_CFG Physical Address
0h	16	ADC_CFG_ADCCTL1	502C 3000h	502C 4000h
2h	16	ADC_CFG_ADCCTL2	502C 3002h	502C 4002h
4h	16	ADC_CFG_ADCBURSTCTL	502C 3004h	502C 4004h
6h	16	ADC_CFG_ADCINTFLG	502C 3006h	502C 4006h
8h	16	ADC_CFG_ADCINTFLGCLR	502C 3008h	502C 4008h
Ah	16	ADC_CFG_ADCINTOVF	502C 300Ah	502C 400Ah
Ch	16	ADC_CFG_ADCINTOVFCLR	502C 300Ch	502C 400Ch
Eh	16	ADC_CFG_ADCINTSEL1N2	502C 300Eh	502C 400Eh
10h	16	ADC_CFG_ADCINTSEL3N4	502C 3010h	502C 4010h
12h	16	ADC_CFG_ADCSOCPRICTL	502C 3012h	502C 4012h
14h	16	ADC_CFG_ADCINTSOCSEL1	502C 3014h	502C 4014h
16h	16	ADC_CFG_ADCINTSOCSEL2	502C 3016h	502C 4016h
18h	16	ADC_CFG_ADCSOCFLG1	502C 3018h	502C 4018h

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Table 3-2. CONTROLSS_ADC[3:4]_CFG Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_ADC3_CFG Physical Address	CONTROLSS_ADC4_CFG Physical Address
1Ah	16	ADC_CFG_ADCSOCFRC1	502C 301Ah	502C 401Ah
1Ch	16	ADC_CFG_ADCSOCOVF1	502C 301Ch	502C 401Ch
1Eh	16	ADC_CFG_ADCSOCOVFCLR1	502C 301Eh	502C 401Eh
20h	32	ADC_CFG_ADCSOC0CTL	502C 3020h	502C 4020h
24h	32	ADC_CFG_ADCSOC1CTL	502C 3024h	502C 4024h
28h	32	ADC_CFG_ADCSOC2CTL	502C 3028h	502C 4028h
2Ch	32	ADC_CFG_ADCSOC3CTL	502C 302Ch	502C 402Ch
30h	32	ADC_CFG_ADCSOC4CTL	502C 3030h	502C 4030h
34h	32	ADC_CFG_ADCSOC5CTL	502C 3034h	502C 4034h
38h	32	ADC_CFG_ADCSOC6CTL	502C 3038h	502C 4038h
3Ch	32	ADC_CFG_ADCSOC7CTL	502C 303Ch	502C 403Ch
40h	32	ADC_CFG_ADCSOC8CTL	502C 3040h	502C 4040h
44h	32	ADC_CFG_ADCSOC9CTL	502C 3044h	502C 4044h
48h	32	ADC_CFG_ADCSOC10CTL	502C 3048h	502C 4048h
4Ch	32	ADC_CFG_ADCSOC11CTL	502C 304Ch	502C 404Ch
50h	32	ADC_CFG_ADCSOC12CTL	502C 3050h	502C 4050h
54h	32	ADC_CFG_ADCSOC13CTL	502C 3054h	502C 4054h
58h	32	ADC_CFG_ADCSOC14CTL	502C 3058h	502C 4058h
5Ch	32	ADC_CFG_ADCSOC15CTL	502C 305Ch	502C 405Ch
60h	16	ADC_CFG_ADCEVTSTAT	502C 3060h	502C 4060h
64h	16	ADC_CFG_ADCEVTCLR	502C 3064h	502C 4064h
68h	16	ADC_CFG_ADCEVTSEL	502C 3068h	502C 4068h
6Ch	16	ADC_CFG_ADCEVTINTSEL	502C 306Ch	502C 406Ch
70h	16	ADC_CFG_ADCOSDETECT	502C 3070h	502C 4070h
72h	16	ADC_CFG_ADCCOUNTER	502C 3072h	502C 4072h
74h	16	ADC_CFG_ADCREV	502C 3074h	502C 4074h
76h	16	ADC_CFG_ADCOFFTRIM	502C 3076h	502C 4076h
7Ch	32	ADC_CFG_ADCCONFIG	502C 307Ch	502C 407Ch
80h	16	ADC_CFG_ADCPPB1CONFIG	502C 3080h	502C 4080h
82h	16	ADC_CFG_ADCPPB1STAMP	502C 3082h	502C 4082h
84h	16	ADC_CFG_ADCPPB1OFFCAL	502C 3084h	502C 4084h
86h	16	ADC_CFG_ADCPPB1OFFREF	502C 3086h	502C 4086h
88h	32	ADC_CFG_ADCPPB1TRIPHI	502C 3088h	502C 4088h
8Ch	32	ADC_CFG_ADCPPB1TRIPLO	502C 308Ch	502C 408Ch
90h	16	ADC_CFG_ADCPPB2CONFIG	502C 3090h	502C 4090h
92h	16	ADC_CFG_ADCPPB2STAMP	502C 3092h	502C 4092h
94h	16	ADC_CFG_ADCPPB2OFFCAL	502C 3094h	502C 4094h
96h	16	ADC_CFG_ADCPPB2OFFREF	502C 3096h	502C 4096h
98h	32	ADC_CFG_ADCPPB2TRIPHI	502C 3098h	502C 4098h
9Ch	32	ADC_CFG_ADCPPB2TRIPLO	502C 309Ch	502C 409Ch
A0h	16	ADC_CFG_ADCPPB3CONFIG	502C 30A0h	502C 40A0h
A2h	16	ADC_CFG_ADCPPB3STAMP	502C 30A2h	502C 40A2h
A4h	16	ADC_CFG_ADCPPB3OFFCAL	502C 30A4h	502C 40A4h
A6h	16	ADC_CFG_ADCPPB3OFFREF	502C 30A6h	502C 40A6h
A8h	32	ADC_CFG_ADCPPB3TRIPHI	502C 30A8h	502C 40A8h
ACh	32	ADC_CFG_ADCPPB3TRIPLO	502C 30ACh	502C 40ACh

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Table 3-2. CONTROLSS_ADC[3:4]_CFG Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_ADC3_CFG Physical Address	CONTROLSS_ADC4_CFG Physical Address
B0h	16	ADC_CFG_ADCPPB4CONFIG	502C 30B0h	502C 40B0h
B2h	16	ADC_CFG_ADCPPB4STAMP	502C 30B2h	502C 40B2h
B4h	16	ADC_CFG_ADCPPB4OFFCAL	502C 30B4h	502C 40B4h
B6h	16	ADC_CFG_ADCPPB4OFFREF	502C 30B6h	502C 40B6h
B8h	32	ADC_CFG_ADCPPB4TRIPHI	502C 30B8h	502C 40B8h
BCh	32	ADC_CFG_ADCPPB4TRIPLO	502C 30BCh	502C 40BCh
DEh	16	ADC_CFG_ADCINTCYCLE	502C 30DEh	502C 40DEh
E0h	32	ADC_CFG_ADCINLTRIM1	502C 30E0h	502C 40E0h
E4h	32	ADC_CFG_ADCINLTRIM2	502C 30E4h	502C 40E4h
E8h	32	ADC_CFG_ADCINLTRIM3	502C 30E8h	502C 40E8h
ECh	32	ADC_CFG_ADCINLTRIM4	502C 30ECh	502C 40ECh
F0h	32	ADC_CFG_ADCINLTRIM5	502C 30F0h	502C 40F0h
F4h	32	ADC_CFG_ADCINLTRIM6	502C 30F4h	502C 40F4h
FCh	32	ADC_CFG_ADCINLTRIMCTL	502C 30FCh	502C 40FCh

3.2.1 ADC_CFG Instance Count Note

Note

n = 0 to 4 for the ADC_CFG registers defined below.

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3.2.2 CONTROLSS_ADCn_CFG_ADCCTL1 Registers

3.2.2.1 ADCn_CFG_ADCCTL1 Register (Offset = 0h) [reset = h]

Short Description: ADC Control 1 Register

Long Description:

Return to Summary Table

Table 3-3. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0000h
CONTROLSS_ADC1_CFG	502C 1000h
CONTROLSS_ADC2_CFG	502C 2000h
CONTROLSS_ADC3_CFG	502C 3000h
CONTROLSS_ADC4_CFG	502C 4000h

Figure 3-1. ADCCTL1 Name Register

15	14	13	12	11	10	9	8
RESERVED		ADCBSY	RESERVED	ADCBSYCHN			
R		R	R	R			
0		0	0	0			
7	6	5	4	3	2	1	0
ADCPWDNZ	RESERVED				INTPULSEPOS	RESERVED	
R/W	R				R/W	R	
0	0				0	0	

Access Types Legend

Table 3-4. ADCCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	RESERVED	R		Reserved
13	ADCBSY	R	0h	ADC Busy. Set when ADC SOC is generated, cleared by hardware four ADC clocks after negative edge of S/H pulse. Used by the ADC state machine to determine if ADC is available to sample. 0 ADC is available to sample next channel 1 ADC is busy and cannot sample another channel
12	RESERVED	R		Reserved
11 - 8	ADCBSYCHN	R	0h	ADC Busy Channel. Set when an ADC Start of Conversion (SOC) is generated. When ADCBSY=0: holds the value of the last converted SOC When ADCBSY=1: reflects the SOC currently being processed 0h SOC0 is currently processing or was last SOC converted 1h SOC1 is currently processing or was last SOC converted 2h SOC2 is currently processing or was last SOC converted 3h SOC3 is currently processing or was last SOC converted 4h SOC4 is currently processing or was last SOC converted 5h SOC5 is currently processing or was last SOC converted 6h SOC6 is currently processing or was last SOC converted 7h SOC7 is currently processing or was last SOC converted 8h SOC8 is currently processing or was last SOC converted 9h SOC9 is currently processing or was last SOC converted Ah SOC10 is currently processing or was last SOC converted Bh SOC11 is currently processing or was last SOC converted Ch SOC12 is currently processing or was last SOC converted Dh SOC13 is currently processing or was last SOC converted Eh SOC14 is currently processing or was last SOC converted Fh SOC15 is currently processing or was last SOC converted

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Table 3-4. ADCCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	ADCPWDNZ	R/W	0h	ADC Power Down (active low). This bit controls the power up and power down of all the analog circuitry inside the analog core. 0 All analog circuitry inside the core is powered down 1 All analog circuitry inside the core is powered up
6 - 3	RESERVED	R		Reserved
2	INTPULSEPOS	R/W	0h	ADC Interrupt Pulse Position. 0 Interrupt pulse generation occurs when ADC begins conversion (at the end of the acquisition window) plus a number of SYSCLK cycles as specified in the ADCINTCYCLE.OFFSET register. 1 Interrupt pulse generation occurs at the end of the conversion, 1 cycle prior to the ADC result latching into its result register
1 - 0	RESERVED	R		Reserved

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3.2.3 CONTROLSS_ADCn_CFG_ADCCTL2 Registers

3.2.3.1 ADCn_CFG_ADCCTL2 Register (Offset = 2h) [reset = h]

Short Description: ADC Control 2 Register

Long Description:

Return to Summary Table

Table 3-5. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0002h
CONTROLSS_ADC1_CFG	502C 1002h
CONTROLSS_ADC2_CFG	502C 2002h
CONTROLSS_ADC3_CFG	502C 3002h
CONTROLSS_ADC4_CFG	502C 4002h

Figure 3-2. ADCCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED				RESERVED			
R				R			
0				0			
7	6	5	4	3	2	1	0
SIGNALMODE	RESOLUTION	RESERVED		PRESCALE			
R/W	R/W	R		R/W			
0	0	0		0			

Access Types Legend

Table 3-6. ADCCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	R		Reserved
12 - 8	RESERVED	R		Reserved
7	SIGNALMODE	R/W	0h	SOC Signaling Mode. Selects the input mode of the converter. Use the AdcSetMode function to change the signal mode. 0 Single-ended 1 Differential
6	RESOLUTION	R/W	0h	SOC Conversion Resolution. Selects the resolution of the converter. Use the AdcSetMode function to change the resolution. 0 12-bit resolution 1 16-bit resolution
5 - 4	RESERVED	R		Reserved
3 - 0	PRESCALE	R/W	0h	ADC Clock Prescaler. 0000 ADCCLK = Input Clock / 1.0 0001 Invalid 0010 ADCCLK = Input Clock / 2.0 0011 ADCCLK = Input Clock / 2.5 0100 ADCCLK = Input Clock / 3.0 0101 ADCCLK = Input Clock / 3.5 0110 ADCCLK = Input Clock / 4.0 0111 ADCCLK = Input Clock / 4.5 1000 ADCCLK = Input Clock / 5.0 1001 ADCCLK = Input Clock / 5.5 1010 ADCCLK = Input Clock / 6.0 1011 ADCCLK = Input Clock / 6.5 1100 ADCCLK = Input Clock / 7.0 1101 ADCCLK = Input Clock / 7.5 1110 ADCCLK = Input Clock / 8.0 1111 ADCCLK = Input Clock / 8.5

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3.2.4 CONTROLSS_ADCn_CFG_ADCINTFLG Registers

3.2.4.1 ADCn_CFG_ADCINTFLG Register (Offset = 6h) [reset = h]

Short Description: ADC Interrupt Flag Register

Long Description:

Return to Summary Table

Table 3-7. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0006h
CONTROLSS_ADC1_CFG	502C 1006h
CONTROLSS_ADC2_CFG	502C 2006h
CONTROLSS_ADC3_CFG	502C 3006h
CONTROLSS_ADC4_CFG	502C 4006h

Figure 3-3. ADCINTFLG Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R				R	R	R	R
0				0	0	0	0

Access Types Legend

Table 3-8. ADCINTFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	R		Reserved
3	ADCINT4	R	0h	ADC Interrupt 4 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode (INTSELxNy register) then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.
2	ADCINT3	R	0h	ADC Interrupt 3 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode (INTSELxNy register) then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.

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Table 3-8. ADCINTFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ADCINT2	R	0h	ADC Interrupt 2 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode (INTSELxNy register) then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.
0	ADCINT1	R	0h	ADC Interrupt 1 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear. 0 No ADC interrupt pulse generated 1 ADC interrupt pulse generated If the ADC interrupt is placed in continue to interrupt mode (INTSELxNy register) then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.

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3.2.5 CONTROLSS_ADCn_CFG_ADCBURSTCTL Registers

3.2.5.1 ADCn_CFG_ADCBURSTCTL Register (Offset = 4h) [reset = h]

Short Description: ADC Burst Control Register

Long Description:

Return to Summary Table

Table 3-9. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0004h
CONTROLSS_ADC1_CFG	502C 1004h
CONTROLSS_ADC2_CFG	502C 2004h
CONTROLSS_ADC3_CFG	502C 3004h
CONTROLSS_ADC4_CFG	502C 4004h

Figure 3-4. ADCBURSTCTL Name Register

15	14	13	12	11	10	9	8
BURSTEN	RESERVED			BURSTSIZE			
R/W	R			R/W			
0	0			0			
7	6	5	4	3	2	1	0
RESERVED	BURSTTRIGSEL						
R	R/W						
0	0						

Access Types Legend

Table 3-10. ADCBURSTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BURSTEN	R/W	0h	SOC Burst Mode Enable. This bit enables the SOC Burst Mode of operation. 0 Burst mode is disabled. 1 Burst mode is enabled.
14 - 12	RESERVED	R		Reserved
11 - 8	BURSTSIZE	R/W	0h	SOC Burst Size Select. This bit field determines how many SOCs are converted when a burst conversion sequence is started. The first SOC converted is defined by the round robin pointer, which is advanced as each SOC is converted. 0h 1 SOC converted 1h 2 SOCs converted 2h 3 SOCs converted 3h 4 SOCs converted 4h 5 SOCs converted 5h 6 SOCs converted 6h 7 SOCs converted 7h 8 SOCs converted 8h 9 SOCs converted 9h 10 SOCs converted Ah 11 SOCs converted Bh 12 SOCs converted Ch 13 SOCs converted Dh 14 SOCs converted Eh 15 SOCs converted Fh 16 SOCs converted
7	RESERVED	R		Reserved
6 - 0	BURSTTRIGSEL	R/W	0h	SOC Burst Trigger Source Select. Configures which trigger will start a burst conversion sequence. 00h - 7Fh: See AM602 spec. for trigger defintion

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3.2.6 CONTROLSS_ADCn_CFG_ADCINTFLGCLR Registers

3.2.6.1 ADCn_CFG_ADCINTFLGCLR Register (Offset = 8h) [reset = h]

Short Description: ADC Interrupt Flag Clear Register

Long Description:

Return to Summary Table

Table 3-11. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0008h
CONTROLSS_ADC1_CFG	502C 1008h
CONTROLSS_ADC2_CFG	502C 2008h
CONTROLSS_ADC3_CFG	502C 3008h
CONTROLSS_ADC4_CFG	502C 4008h

Figure 3-5. ADCINTFLGCLR Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R				R-0/W	R-0/W	R-0/W	R-0/W
0				0	0	0	0

Access Types Legend

Table 3-12. ADCINTFLGCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	R		Reserved
3	ADCINT4	R-0/W	0h	ADC Interrupt 4 Flag Clear. Reads return 0. 0 No action 1 Clears ADCINT4 and ADCINT4RESULT flags in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
2	ADCINT3	R-0/W	0h	ADC Interrupt 3 Flag Clear. Reads return 0. 0 No action 1 Clears ADCINT3 and ADCINT3RESULT flags in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
1	ADCINT2	R-0/W	0h	ADC Interrupt 2 Flag Clear. Reads return 0. 0 No action 1 Clears ADCINT2 and ADCINT2RESULT flags in the ADCINTFLG register. . If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set
0	ADCINT1	R-0/W	0h	ADC Interrupt 1 Flag Clear. Reads return 0. 0 No action 1 Clears ADCINT1 and ADCINT1RESULT flags in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set

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3.2.7 CONTROLSS_ADCn_CFG_ADCINTOVF Registers

3.2.7.1 ADCn_CFG_ADCINTOVF Register (Offset = Ah) [reset = h]

Short Description: ADC Interrupt Overflow Register

Long Description:

Return to Summary Table

Table 3-13. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 000Ah
CONTROLSS_ADC1_CFG	502C 100Ah
CONTROLSS_ADC2_CFG	502C 200Ah
CONTROLSS_ADC3_CFG	502C 300Ah
CONTROLSS_ADC4_CFG	502C 400Ah

Figure 3-6. ADCINTOVF Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R				R	R	R	R
0				0	0	0	0

Access Types Legend

Table 3-14. ADCINTOVF Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	R		Reserved
3	ADCINT4	R	0h	ADC Interrupt 4 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.
2	ADCINT3	R	0h	ADC Interrupt 3 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.
1	ADCINT2	R	0h	ADC Interrupt 2 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.

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Table 3-14. ADCINTOVF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ADCINT1	R	0h	ADC Interrupt 1 Overflow Flags Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs. 0 No ADC interrupt overflow event detected. 1 ADC Interrupt overflow event detected. The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.

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3.2.8 CONTROLSS_ADCn_CFG_ADCINTOVFCLR Registers

3.2.8.1 ADCn_CFG_ADCINTOVFCLR Register (Offset = Ch) [reset = h]

Short Description: ADC Interrupt Overflow Clear Register

Long Description:

Return to Summary Table

Table 3-15. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 000Ch
CONTROLSS_ADC1_CFG	502C 100Ch
CONTROLSS_ADC2_CFG	502C 200Ch
CONTROLSS_ADC3_CFG	502C 300Ch
CONTROLSS_ADC4_CFG	502C 400Ch

Figure 3-7. ADCINTOVFCLR Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED				ADCINT4	ADCINT3	ADCINT2	ADCINT1
R				R-0/W	R-0/W	R-0/W	R-0/W
0				0	0	0	0

Access Types Legend

Table 3-16. ADCINTOVFCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	R		Reserved
3	ADCINT4	R-0/W	0h	ADC Interrupt 4 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
2	ADCINT3	R-0/W	0h	ADC Interrupt 3 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
1	ADCINT2	R-0/W	0h	ADC Interrupt 2 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.
0	ADCINT1	R-0/W	0h	ADC Interrupt 1 Overflow Clear Bits 0 No action. 1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set.

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3.2.9 CONTROLSS_ADCn_CFG_ADCINTSEL1N2 Registers

3.2.9.1 ADCn_CFG_ADCINTSEL1N2 Register (Offset = Eh) [reset = h]

Short Description: ADC Interrupt 1 and 2 Selection Register

Long Description:

Return to Summary Table

Table 3-17. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 000Eh
CONTROLSS_ADC1_CFG	502C 100Eh
CONTROLSS_ADC2_CFG	502C 200Eh
CONTROLSS_ADC3_CFG	502C 300Eh
CONTROLSS_ADC4_CFG	502C 400Eh

Figure 3-8. ADCINTSEL1N2 Name Register

15	14	13	12	11	10	9	8
RESERVED	INT2CONT	INT2E	RESERVED	INT2SEL			
R	R/W	R/W	R	R/W			
0	0	0	0	0			
7	6	5	4	3	2	1	0
RESERVED	INT1CONT	INT1E	RESERVED	INT1SEL			
R	R/W	R/W	R	R/W			
0	0	0	0	0			

Access Types Legend

Table 3-18. ADCINTSEL1N2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	INT2CONT	R/W	0h	ADCINT2 Continue to Interrupt Mode 0 No further ADCINT2 pulses are generated until ADCINT2 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT2 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
13	INT2E	R/W	0h	ADCINT2 Interrupt Enable 0 ADCINT2 is disabled 1 ADCINT2 is enabled
12	RESERVED	R		Reserved
11 - 8	INT2SEL	R/W	0h	ADCINT2 EOC Source Select 0h EOC0 is trigger for ADCINT2 1h EOC1 is trigger for ADCINT2 2h EOC2 is trigger for ADCINT2 3h EOC3 is trigger for ADCINT2 4h EOC4 is trigger for ADCINT2 5h EOC5 is trigger for ADCINT2 6h EOC6 is trigger for ADCINT2 7h EOC7 is trigger for ADCINT2 8h EOC8 is trigger for ADCINT2 9h EOC9 is trigger for ADCINT2 Ah EOC10 is trigger for ADCINT2 Bh EOC11 is trigger for ADCINT2 Ch EOC12 is trigger for ADCINT2 Dh EOC13 is trigger for ADCINT2 Eh EOC14 is trigger for ADCINT2 Fh EOC15 is trigger for ADCINT2
7	RESERVED	R		Reserved
6	INT1CONT	R/W	0h	ADCINT1 Continue to Interrupt Mode 0 No further ADCINT1 pulses are generated until ADCINT1 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT1 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
5	INT1E	R/W	0h	ADCINT1 Interrupt Enable 0 ADCINT1 is disabled 1 ADCINT1 is enabled
4	RESERVED	R		Reserved

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Table 3-18. ADCINTSEL1N2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	INT1SEL	R/W	0h	ADCINT1 EOC Source Select 0h EOC0 is trigger for ADCINT1 1h EOC1 is trigger for ADCINT1 2h EOC2 is trigger for ADCINT1 3h EOC3 is trigger for ADCINT1 4h EOC4 is trigger for ADCINT1 5h EOC5 is trigger for ADCINT1 6h EOC6 is trigger for ADCINT1 7h EOC7 is trigger for ADCINT1 8h EOC8 is trigger for ADCINT1 9h EOC9 is trigger for ADCINT1 Ah EOC10 is trigger for ADCINT1 Bh EOC11 is trigger for ADCINT1 Ch EOC12 is trigger for ADCINT1 Dh EOC13 is trigger for ADCINT1 Eh EOC14 is trigger for ADCINT1 Fh EOC15 is trigger for ADCINT1

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3.2.10 CONTROLSS_ADCn_CFG_ADCINTSEL3N4 Registers

3.2.10.1 ADCn_CFG_ADCINTSEL3N4 Register (Offset = 10h) [reset = h]

Short Description: ADC Interrupt 3 and 4 Selection Register

Long Description:

Return to Summary Table

Table 3-19. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0010h
CONTROLSS_ADC1_CFG	502C 1010h
CONTROLSS_ADC2_CFG	502C 2010h
CONTROLSS_ADC3_CFG	502C 3010h
CONTROLSS_ADC4_CFG	502C 4010h

Figure 3-9. ADCINTSEL3N4 Name Register

15	14	13	12	11	10	9	8
RESERVED	INT4CONT	INT4E	RESERVED	INT4SEL			
R	R/W	R/W	R	R/W			
0	0	0	0	0			
7	6	5	4	3	2	1	0
RESERVED	INT3CONT	INT3E	RESERVED	INT3SEL			
R	R/W	R/W	R	R/W			
0	0	0	0	0			

Access Types Legend

Table 3-20. ADCINTSEL3N4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	INT4CONT	R/W	0h	ADCINT4 Continue to Interrupt Mode 0 No further ADCINT4 pulses are generated until ADCINT4 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT4 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
13	INT4E	R/W	0h	ADCINT4 Interrupt Enable 0 ADCINT4 is disabled 1 ADCINT4 is enabled
12	RESERVED	R		Reserved
11 - 8	INT4SEL	R/W	0h	ADCINT4 EOC Source Select 0h EOC0 is trigger for ADCINT4 1h EOC1 is trigger for ADCINT4 2h EOC2 is trigger for ADCINT4 3h EOC3 is trigger for ADCINT4 4h EOC4 is trigger for ADCINT4 5h EOC5 is trigger for ADCINT4 6h EOC6 is trigger for ADCINT4 7h EOC7 is trigger for ADCINT4 8h EOC8 is trigger for ADCINT4 9h EOC9 is trigger for ADCINT4 Ah EOC10 is trigger for ADCINT4 Bh EOC11 is trigger for ADCINT4 Ch EOC12 is trigger for ADCINT4 Dh EOC13 is trigger for ADCINT4 Eh EOC14 is trigger for ADCINT4 Fh EOC15 is trigger for ADCINT4
7	RESERVED	R		Reserved
6	INT3CONT	R/W	0h	ADCINT3 Continue to Interrupt Mode 0 No further ADCINT3 pulses are generated until ADCINT3 flag (in ADCINTFLG register) is cleared by user. 1 ADCINT3 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.
5	INT3E	R/W	0h	ADCINT3 Interrupt Enable 0 ADCINT3 is disabled 1 ADCINT3 is enabled
4	RESERVED	R		Reserved

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Table 3-20. ADCINTSEL3N4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	INT3SEL	R/W	0h	ADCINT3 EOC Source Select 0h EOC0 is trigger for ADCINT3 1h EOC1 is trigger for ADCINT3 2h EOC2 is trigger for ADCINT3 3h EOC3 is trigger for ADCINT3 4h EOC4 is trigger for ADCINT3 5h EOC5 is trigger for ADCINT3 6h EOC6 is trigger for ADCINT3 7h EOC7 is trigger for ADCINT3 8h EOC8 is trigger for ADCINT3 9h EOC9 is trigger for ADCINT3 Ah EOC10 is trigger for ADCINT3 Bh EOC11 is trigger for ADCINT3 Ch EOC12 is trigger for ADCINT3 Dh EOC13 is trigger for ADCINT3 Eh EOC14 is trigger for ADCINT3 Fh EOC15 is trigger for ADCINT3

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3.2.11 CONTROLSS_ADCn_CFG_ADCSOCPRICTL Registers

3.2.11.1 ADCn_CFG_ADCSOCPRICTL Register (Offset = 12h) [reset = h]

Short Description: ADC SOC Priority Control Register

Long Description:

Return to Summary Table

Table 3-21. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0012h
CONTROLSS_ADC1_CFG	502C 1012h
CONTROLSS_ADC2_CFG	502C 2012h
CONTROLSS_ADC3_CFG	502C 3012h
CONTROLSS_ADC4_CFG	502C 4012h

Figure 3-10. ADCSOCPRICTL Name Register

15	14	13	12	11	10	9	8
RESERVED						RRPOINTER	
R						R	
0						10000	
7	6	5	4	3	2	1	0
RRPOINTER			SOCPRIORITY				
R			R/W				
10000			0				

Access Types Legend

Table 3-22. ADCSOCPRICTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	R		Reserved

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Table 3-22. ADCSOCPRICTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9 - 5	RRPOINTER	R	10h	Round Robin Pointer. Holds the value of the last converted round robin SOCx to be used by the round robin scheme to determine order of conversions. 00h SOC0 was last round robin SOC to convert, SOC1 is highest round robin priority. 01h SOC1 was last round robin SOC to convert, SOC2 is highest round robin priority. 02h SOC2 was last round robin SOC to convert, SOC3 is highest round robin priority. 03h SOC3 was last round robin SOC to convert, SOC4 is highest round robin priority. 04h SOC4 was last round robin SOC to convert, SOC5 is highest round robin priority. 05h SOC5 was last round robin SOC to convert, SOC6 is highest round robin priority. 06h SOC6 was last round robin SOC to convert, SOC7 is highest round robin priority. 07h SOC7 was last round robin SOC to convert, SOC8 is highest round robin priority. 08h SOC8 was last round robin SOC to convert, SOC9 is highest round robin priority. 09h SOC9 was last round robin SOC to convert, SOC10 is highest round robin priority. 0Ah SOC10 was last round robin SOC to convert, SOC11 is highest round robin priority. 0Bh SOC11 was last round robin SOC to convert, SOC12 is highest round robin priority. 0Ch SOC12 was last round robin SOC to convert, SOC13 is highest round robin priority. 0Dh SOC13 was last round robin SOC to convert, SOC14 is highest round robin priority. 0Eh SOC14 was last round robin SOC to convert, SOC15 is highest round robin priority. 0Fh SOC15 was last round robin SOC to convert, SOC0 is highest round robin priority. 10h Reset value to indicate no SOC has been converted. SOC0 is highest round robin priority. Set to this value when the device is reset, when the ADCCTL1.RESET bit is set, or when the ADCSOCPRICTL register is written. In the latter case, if a conversion is currently in progress, it will complete and then the new priority will take effect. Others Invalid value.
4 - 0	SOCPRIORITY	R/W	0h	SOC Priority Determines the cutoff point for priority mode and round robin arbitration for SOCx 00h SOC priority is handled in round robin mode for all channels. 01h SOC0 is high priority, rest of channels are in round robin mode. 02h SOC0-SOC1 are high priority, SOC2-SOC15 are in round robin mode. 03h SOC0-SOC2 are high priority, SOC3-SOC15 are in round robin mode. 04h SOC0-SOC3 are high priority, SOC4-SOC15 are in round robin mode. 05h SOC0-SOC4 are high priority, SOC5-SOC15 are in round robin mode. 06h SOC0-SOC5 are high priority, SOC6-SOC15 are in round robin mode. 07h SOC0-SOC6 are high priority, SOC7-SOC15 are in round robin mode. 08h SOC0-SOC7 are high priority, SOC8-SOC15 are in round robin mode. 09h SOC0-SOC8 are high priority, SOC9-SOC15 are in round robin mode. 0Ah SOC0-SOC9 are high priority, SOC10-SOC15 are in round robin mode. 0Bh SOC0-SOC10 are high priority, SOC11-SOC15 are in round robin mode. 0Ch SOC0-SOC11 are high priority, SOC12-SOC15 are in round robin mode. 0Dh SOC0-SOC12 are high priority, SOC13-SOC15 are in round robin mode. 0Eh SOC0-SOC13 are high priority, SOC14-SOC15 are in round robin mode. 0Fh SOC0-SOC14 are high priority, SOC15 is in round robin mode. 10h All SOCs are in high priority mode, arbitrated by SOC number. Others Invalid selection.

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3.2.12 CONTROLSS_ADCn_CFG_ADCINTSOCSEL1 Registers

3.2.12.1 ADCn_CFG_ADCINTSOCSEL1 Register (Offset = 14h) [reset = h]

Short Description: ADC Interrupt SOC Selection 1 Register

Long Description:

Return to Summary Table

Table 3-23. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0014h
CONTROLSS_ADC1_CFG	502C 1014h
CONTROLSS_ADC2_CFG	502C 2014h
CONTROLSS_ADC3_CFG	502C 3014h
CONTROLSS_ADC4_CFG	502C 4014h

Figure 3-11. ADCINTSOCSEL1 Name Register

15	14	13	12	11	10	9	8
SOC7		SOC6		SOC5		SOC4	
R/W		R/W		R/W		R/W	
0		0		0		0	
7	6	5	4	3	2	1	0
SOC3		SOC2		SOC1		SOC0	
R/W		R/W		R/W		R/W	
0		0		0		0	

Access Types Legend

Table 3-24. ADCINTSOCSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	SOC7	R/W	0h	SOC7 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC7. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC7. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC7. 10 ADCINT2 will trigger SOC7. 11 Invalid selection.
13 - 12	SOC6	R/W	0h	SOC6 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC6. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC6. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC6. 10 ADCINT2 will trigger SOC6. 11 Invalid selection.
11 - 10	SOC5	R/W	0h	SOC5 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC5. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC5. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC5. 10 ADCINT2 will trigger SOC5. 11 Invalid selection.
9 - 8	SOC4	R/W	0h	SOC4 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC4. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC4. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC4. 10 ADCINT2 will trigger SOC4. 11 Invalid selection.

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Table 3-24. ADCINTSOCSEL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7 - 6	SOC3	R/W	0h	SOC3 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC3. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC3. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC3. 10 ADCINT2 will trigger SOC3. 11 Invalid selection.
5 - 4	SOC2	R/W	0h	SOC2 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC2. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC2. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC2. 10 ADCINT2 will trigger SOC2. 11 Invalid selection.
3 - 2	SOC1	R/W	0h	SOC1 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC1. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC1. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC1. 10 ADCINT2 will trigger SOC1. 11 Invalid selection.
1 - 0	SOC0	R/W	0h	SOC0 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC0. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC0. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC0. 10 ADCINT2 will trigger SOC0. 11 Invalid selection.

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3.2.13 CONTROLSS_ADCn_CFG_ADCINTSOCSEL2 Registers

3.2.13.1 ADCn_CFG_ADCINTSOCSEL2 Register (Offset = 16h) [reset = h]

Short Description: ADC Interrupt SOC Selection 2 Register

Long Description:

Return to Summary Table

Table 3-25. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0016h
CONTROLSS_ADC1_CFG	502C 1016h
CONTROLSS_ADC2_CFG	502C 2016h
CONTROLSS_ADC3_CFG	502C 3016h
CONTROLSS_ADC4_CFG	502C 4016h

Figure 3-12. ADCINTSOCSEL2 Name Register

15	14	13	12	11	10	9	8
SOC15		SOC14		SOC13		SOC12	
R/W		R/W		R/W		R/W	
0		0		0		0	
7	6	5	4	3	2	1	0
SOC11		SOC10		SOC9		SOC8	
R/W		R/W		R/W		R/W	
0		0		0		0	

Access Types Legend

Table 3-26. ADCINTSOCSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	SOC15	R/W	0h	SOC15 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC15. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC15. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC15. 10 ADCINT2 will trigger SOC15. 11 Invalid selection.
13 - 12	SOC14	R/W	0h	SOC14 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC14. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC14. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC14. 10 ADCINT2 will trigger SOC14. 11 Invalid selection.
11 - 10	SOC13	R/W	0h	SOC13 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC13. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC13. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC13. 10 ADCINT2 will trigger SOC13. 11 Invalid selection.
9 - 8	SOC12	R/W	0h	SOC12 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC12. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC12. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC12. 10 ADCINT2 will trigger SOC12. 11 Invalid selection.

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Table 3-26. ADCINTSOCSEL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7 - 6	SOC11	R/W	0h	SOC11 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC11. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC11. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC11. 10 ADCINT2 will trigger SOC11. 11 Invalid selection.
5 - 4	SOC10	R/W	0h	SOC10 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC10. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC10. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC10. 10 ADCINT2 will trigger SOC10. 11 Invalid selection.
3 - 2	SOC9	R/W	0h	SOC9 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC9. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC9. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC9. 10 ADCINT2 will trigger SOC9. 11 Invalid selection.
1 - 0	SOC8	R/W	0h	SOC8 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC8. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register. 00 No ADCINT will trigger SOC8. TRIGSEL field alone determines SOC0 trigger. 01 ADCINT1 will trigger SOC8. 10 ADCINT2 will trigger SOC8. 11 Invalid selection.

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3.2.14 CONTROLSS_ADCn_CFG_ADCSOCFLG1 Registers

3.2.14.1 ADCn_CFG_ADCSOCFLG1 Register (Offset = 18h) [reset = h]

Short Description: ADC SOC Flag 1 Register

Long Description:

Return to Summary Table

Table 3-27. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0018h
CONTROLSS_ADC1_CFG	502C 1018h
CONTROLSS_ADC2_CFG	502C 2018h
CONTROLSS_ADC3_CFG	502C 3018h
CONTROLSS_ADC4_CFG	502C 4018h

Figure 3-13. ADCSOCFLG1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-28. ADCSOCFLG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R	0h	SOC15 Start of Conversion Flag. Indicates the state of SOC15 conversions. 0 No sample pending for SOC15. 1 Trigger has been received and sample is pending for SOC15. This bit will be automatically cleared when the SOC15 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
14	SOC14	R	0h	SOC14 Start of Conversion Flag. Indicates the state of SOC14 conversions. 0 No sample pending for SOC14. 1 Trigger has been received and sample is pending for SOC14. This bit will be automatically cleared when the SOC14 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
13	SOC13	R	0h	SOC13 Start of Conversion Flag. Indicates the state of SOC13 conversions. 0 No sample pending for SOC13. 1 Trigger has been received and sample is pending for SOC13. This bit will be automatically cleared when the SOC13 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

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Table 3-28. ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	SOC12	R	0h	SOC12 Start of Conversion Flag. Indicates the state of SOC12 conversions. 0 No sample pending for SOC12. 1 Trigger has been received and sample is pending for SOC12. This bit will be automatically cleared when the SOC12 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
11	SOC11	R	0h	SOC11 Start of Conversion Flag. Indicates the state of SOC11 conversions. 0 No sample pending for SOC11. 1 Trigger has been received and sample is pending for SOC11. This bit will be automatically cleared when the SOC11 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
10	SOC10	R	0h	SOC10 Start of Conversion Flag. Indicates the state of SOC10 conversions. 0 No sample pending for SOC10. 1 Trigger has been received and sample is pending for SOC10. This bit will be automatically cleared when the SOC10 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
9	SOC9	R	0h	SOC9 Start of Conversion Flag. Indicates the state of SOC9 conversions. 0 No sample pending for SOC9. 1 Trigger has been received and sample is pending for SOC9. This bit will be automatically cleared when the SOC9 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
8	SOC8	R	0h	SOC8 Start of Conversion Flag. Indicates the state of SOC8 conversions. 0 No sample pending for SOC8. 1 Trigger has been received and sample is pending for SOC8. This bit will be automatically cleared when the SOC8 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
7	SOC7	R	0h	SOC7 Start of Conversion Flag. Indicates the state of SOC7 conversions. 0 No sample pending for SOC7. 1 Trigger has been received and sample is pending for SOC7. This bit will be automatically cleared when the SOC7 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
6	SOC6	R	0h	SOC6 Start of Conversion Flag. Indicates the state of SOC6 conversions. 0 No sample pending for SOC6. 1 Trigger has been received and sample is pending for SOC6. This bit will be automatically cleared when the SOC6 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

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Table 3-28. ADCSOCFLG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SOC5	R	0h	SOC5 Start of Conversion Flag. Indicates the state of SOC5 conversions. 0 No sample pending for SOC5. 1 Trigger has been received and sample is pending for SOC5. This bit will be automatically cleared when the SOC5 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
4	SOC4	R	0h	SOC4 Start of Conversion Flag. Indicates the state of SOC4 conversions. 0 No sample pending for SOC4. 1 Trigger has been received and sample is pending for SOC4. This bit will be automatically cleared when the SOC4 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
3	SOC3	R	0h	SOC3 Start of Conversion Flag. Indicates the state of SOC3 conversions. 0 No sample pending for SOC3. 1 Trigger has been received and sample is pending for SOC3. This bit will be automatically cleared when the SOC3 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
2	SOC2	R	0h	SOC2 Start of Conversion Flag. Indicates the state of SOC2 conversions. 0 No sample pending for SOC2. 1 Trigger has been received and sample is pending for SOC2. This bit will be automatically cleared when the SOC2 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
1	SOC1	R	0h	SOC1 Start of Conversion Flag. Indicates the state of SOC1 conversions. 0 No sample pending for SOC1. 1 Trigger has been received and sample is pending for SOC1. This bit will be automatically cleared when the SOC1 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.
0	SOC0	R	0h	SOC0 Start of Conversion Flag. Indicates the state of SOC0 conversions. 0 No sample pending for SOC0. 1 Trigger has been received and sample is pending for SOC0. This bit will be automatically cleared when the SOC0 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.

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3.2.15 CONTROLSS_ADCn_CFG_ADCSOCFRC1 Registers

3.2.15.1 ADCn_CFG_ADCSOCFRC1 Register (Offset = 1Ah) [reset = h]

Short Description: ADC SOC Force 1 Register

Long Description:

Return to Summary Table

Table 3-29. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 001Ah
CONTROLSS_ADC1_CFG	502C 101Ah
CONTROLSS_ADC2_CFG	502C 201Ah
CONTROLSS_ADC3_CFG	502C 301Ah
CONTROLSS_ADC4_CFG	502C 401Ah

Figure 3-14. ADCSOCFRC1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-30. ADCSOCFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R-0/W	0h	SOC15 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC15 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC15 flag bit to 1. This will cause a conversion to start once priority is given to SOC15. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC15 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
14	SOC14	R-0/W	0h	SOC14 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC14 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC14 flag bit to 1. This will cause a conversion to start once priority is given to SOC14. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC14 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

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Table 3-30. ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	SOC13	R-0/W	0h	SOC13 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC13 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC13 flag bit to 1. This will cause a conversion to start once priority is given to SOC13. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC13 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
12	SOC12	R-0/W	0h	SOC12 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC12 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC12 flag bit to 1. This will cause a conversion to start once priority is given to SOC12. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC12 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
11	SOC11	R-0/W	0h	SOC11 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC11 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC11 flag bit to 1. This will cause a conversion to start once priority is given to SOC11. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC11 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
10	SOC10	R-0/W	0h	SOC10 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC10 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC10 flag bit to 1. This will cause a conversion to start once priority is given to SOC10. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC10 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
9	SOC9	R-0/W	0h	SOC9 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC9 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC9 flag bit to 1. This will cause a conversion to start once priority is given to SOC9. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC9 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

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Table 3-30. ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SOC8	R-0/W	0h	SOC8 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC8 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC8 flag bit to 1. This will cause a conversion to start once priority is given to SOC8. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC8 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
7	SOC7	R-0/W	0h	SOC7 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC7 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC7 flag bit to 1. This will cause a conversion to start once priority is given to SOC7. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC7 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
6	SOC6	R-0/W	0h	SOC6 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC6 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC6 flag bit to 1. This will cause a conversion to start once priority is given to SOC6. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC6 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
5	SOC5	R-0/W	0h	SOC5 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC5 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC5 flag bit to 1. This will cause a conversion to start once priority is given to SOC5. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC5 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
4	SOC4	R-0/W	0h	SOC4 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC4 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC4 flag bit to 1. This will cause a conversion to start once priority is given to SOC4. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC4 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

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Table 3-30. ADCSOCFRC1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SOC3	R-0/W	0h	SOC3 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC3 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC3 flag bit to 1. This will cause a conversion to start once priority is given to SOC3. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC3 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
2	SOC2	R-0/W	0h	SOC2 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC2 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC2 flag bit to 1. This will cause a conversion to start once priority is given to SOC2. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC2 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
1	SOC1	R-0/W	0h	SOC1 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC1 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC1 flag bit to 1. This will cause a conversion to start once priority is given to SOC1. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC1 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.
0	SOC0	R-0/W	0h	SOC0 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC0 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0. 0 No action. 1 Force SOC0 flag bit to 1. This will cause a conversion to start once priority is given to SOC0. If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC0 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.

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3.2.16 CONTROLSS_ADCn_CFG_ADCSOCOVF1 Registers

3.2.16.1 ADCn_CFG_ADCSOCOVF1 Register (Offset = 1Ch) [reset = h]

Short Description: ADC SOC Overflow 1 Register

Long Description:

Return to Summary Table

Table 3-31. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 001Ch
CONTROLSS_ADC1_CFG	502C 101Ch
CONTROLSS_ADC2_CFG	502C 201Ch
CONTROLSS_ADC3_CFG	502C 301Ch
CONTROLSS_ADC4_CFG	502C 401Ch

Figure 3-15. ADCSOCOVF1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-32. ADCSOCOVF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R	0h	SOC15 Start of Conversion Overflow Flag. Indicates an SOC15 event was generated in hardware while an existing SOC15 event was already pending. 0 No SOC15 event overflow. 1 SOC15 event overflow. An overflow condition does not stop SOC15 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
14	SOC14	R	0h	SOC14 Start of Conversion Overflow Flag. Indicates an SOC14 event was generated in hardware while an existing SOC14 event was already pending. 0 No SOC14 event overflow. 1 SOC14 event overflow. An overflow condition does not stop SOC14 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
13	SOC13	R	0h	SOC13 Start of Conversion Overflow Flag. Indicates an SOC13 event was generated in hardware while an existing SOC13 event was already pending. 0 No SOC13 event overflow. 1 SOC13 event overflow. An overflow condition does not stop SOC13 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
12	SOC12	R	0h	SOC12 Start of Conversion Overflow Flag. Indicates an SOC12 event was generated in hardware while an existing SOC12 event was already pending. 0 No SOC12 event overflow. 1 SOC12 event overflow. An overflow condition does not stop SOC12 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.

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Table 3-32. ADCSOCOVF1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	SOC11	R	0h	SOC11 Start of Conversion Overflow Flag. Indicates an SOC11 event was generated in hardware while an existing SOC11 event was already pending. 0 No SOC11 event overflow. 1 SOC11 event overflow. An overflow condition does not stop SOC11 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
10	SOC10	R	0h	SOC10 Start of Conversion Overflow Flag. Indicates an SOC10 event was generated in hardware while an existing SOC10 event was already pending. 0 No SOC10 event overflow. 1 SOC10 event overflow. An overflow condition does not stop SOC10 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
9	SOC9	R	0h	SOC9 Start of Conversion Overflow Flag. Indicates an SOC9 event was generated in hardware while an existing SOC9 event was already pending. 0 No SOC9 event overflow. 1 SOC9 event overflow. An overflow condition does not stop SOC9 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
8	SOC8	R	0h	SOC8 Start of Conversion Overflow Flag. Indicates an SOC8 event was generated in hardware while an existing SOC8 event was already pending. 0 No SOC8 event overflow. 1 SOC8 event overflow. An overflow condition does not stop SOC8 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
7	SOC7	R	0h	SOC7 Start of Conversion Overflow Flag. Indicates an SOC7 event was generated in hardware while an existing SOC7 event was already pending. 0 No SOC7 event overflow. 1 SOC7 event overflow. An overflow condition does not stop SOC7 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
6	SOC6	R	0h	SOC6 Start of Conversion Overflow Flag. Indicates an SOC6 event was generated in hardware while an existing SOC6 event was already pending. 0 No SOC6 event overflow. 1 SOC6 event overflow. An overflow condition does not stop SOC6 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
5	SOC5	R	0h	SOC5 Start of Conversion Overflow Flag. Indicates an SOC5 event was generated in hardware while an existing SOC5 event was already pending. 0 No SOC5 event overflow. 1 SOC5 event overflow. An overflow condition does not stop SOC5 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
4	SOC4	R	0h	SOC4 Start of Conversion Overflow Flag. Indicates an SOC4 event was generated in hardware while an existing SOC4 event was already pending. 0 No SOC4 event overflow. 1 SOC4 event overflow. An overflow condition does not stop SOC4 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
3	SOC3	R	0h	SOC3 Start of Conversion Overflow Flag. Indicates an SOC3 event was generated in hardware while an existing SOC3 event was already pending. 0 No SOC3 event overflow. 1 SOC3 event overflow. An overflow condition does not stop SOC3 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
2	SOC2	R	0h	SOC2 Start of Conversion Overflow Flag. Indicates an SOC2 event was generated in hardware while an existing SOC2 event was already pending. 0 No SOC2 event overflow. 1 SOC2 event overflow. An overflow condition does not stop SOC2 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.

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Table 3-32. ADCSOCOVF1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SOC1	R	0h	SOC1 Start of Conversion Overflow Flag. Indicates an SOC1 event was generated in hardware while an existing SOC1 event was already pending. 0 No SOC1 event overflow. 1 SOC1 event overflow. An overflow condition does not stop SOC1 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.
0	SOC0	R	0h	SOC0 Start of Conversion Overflow Flag. Indicates an SOC0 event was generated in hardware while an existing SOC0 event was already pending. 0 No SOC0 event overflow. 1 SOC0 event overflow. An overflow condition does not stop SOC0 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not affect this bit.

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3.2.17 CONTROLSS_ADCn_CFG_ADCSOCOVFCLR1 Registers

3.2.17.1 ADCn_CFG_ADCSOCOVFCLR1 Register (Offset = 1Eh) [reset = h]

Short Description: ADC SOC Overflow Clear 1 Register

Long Description:

Return to Summary Table

Table 3-33. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 001Eh
CONTROLSS_ADC1_CFG	502C 101Eh
CONTROLSS_ADC2_CFG	502C 201Eh
CONTROLSS_ADC3_CFG	502C 301Eh
CONTROLSS_ADC4_CFG	502C 401Eh

Figure 3-16. ADCSOCOVFCLR1 Name Register

15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0
R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-34. ADCSOCOVFCLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOC15	R-0/W	0h	SOC15 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC15 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC15 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
14	SOC14	R-0/W	0h	SOC14 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC14 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC14 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
13	SOC13	R-0/W	0h	SOC13 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC13 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC13 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
12	SOC12	R-0/W	0h	SOC12 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC12 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC12 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..

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Table 3-34. ADCSOCOVFCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	SOC11	R-0/W	0h	SOC11 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC11 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC11 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
10	SOC10	R-0/W	0h	SOC10 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC10 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC10 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
9	SOC9	R-0/W	0h	SOC9 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC9 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC9 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
8	SOC8	R-0/W	0h	SOC8 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC8 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC8 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
7	SOC7	R-0/W	0h	SOC7 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC7 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC7 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
6	SOC6	R-0/W	0h	SOC6 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC6 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC6 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
5	SOC5	R-0/W	0h	SOC5 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC5 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC5 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
4	SOC4	R-0/W	0h	SOC4 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC4 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC4 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
3	SOC3	R-0/W	0h	SOC3 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC3 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC3 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..

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Table 3-34. ADCSOCOVFCLR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SOC2	R-0/W	0h	SOC2 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC2 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC2 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
1	SOC1	R-0/W	0h	SOC1 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC1 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC1 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..
0	SOC0	R-0/W	0h	SOC0 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC0 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0. 0 No action. 1 Clear SOC0 overflow flag. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..

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3.2.18 CONTROLSS_ADCn_CFG_ADCSOC0CTL Registers

3.2.18.1 ADCn_CFG_ADCSOC0CTL Register (Offset = 20h) [reset = h]

Short Description: ADC SOC0 Control Register

Long Description:

Return to Summary Table

Table 3-35. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0020h
CONTROLSS_ADC1_CFG	502C 1020h
CONTROLSS_ADC2_CFG	502C 2020h
CONTROLSS_ADC3_CFG	502C 3020h
CONTROLSS_ADC4_CFG	502C 4020h

Figure 3-17. ADCSOC0CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-36. ADCSOC0CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC0 Trigger Source Select. Along with the SOC0 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC0 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC0 Channel Select. Selects the channel to be converted when SOC0 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC0 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

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3.2.19 CONTROLSS_ADCn_CFG_ADCSOC1CTL Registers

3.2.19.1 ADCn_CFG_ADCSOC1CTL Register (Offset = 24h) [reset = h]

Short Description: ADC SOC1 Control Register

Long Description:

Return to Summary Table

Table 3-37. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0024h
CONTROLSS_ADC1_CFG	502C 1024h
CONTROLSS_ADC2_CFG	502C 2024h
CONTROLSS_ADC3_CFG	502C 3024h
CONTROLSS_ADC4_CFG	502C 4024h

Figure 3-18. ADCSOC1CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-38. ADCSOC1CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC1 Trigger Source Select. Along with the SOC1 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC1 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC1 Channel Select. Selects the channel to be converted when SOC1 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC1 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

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3.2.20 CONTROLSS_ADCn_CFG_ADCSOC2CTL Registers

3.2.20.1 ADCn_CFG_ADCSOC2CTL Register (Offset = 28h) [reset = h]

Short Description: ADC SOC2 Control Register

Long Description:

Return to Summary Table

Table 3-39. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0028h
CONTROLSS_ADC1_CFG	502C 1028h
CONTROLSS_ADC2_CFG	502C 2028h
CONTROLSS_ADC3_CFG	502C 3028h
CONTROLSS_ADC4_CFG	502C 4028h

Figure 3-19. ADCSOC2CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-40. ADCSOC2CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC2 Trigger Source Select. Along with the SOC2 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC2 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC2 Channel Select. Selects the channel to be converted when SOC2 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC2 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

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3.2.21 CONTROLSS_ADCn_CFG_ADCSOC3CTL Registers

3.2.21.1 ADCn_CFG_ADCSOC3CTL Register (Offset = 2Ch) [reset = h]

Short Description: ADC SOC3 Control Register

Long Description:

Return to Summary Table

Table 3-41. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 002Ch
CONTROLSS_ADC1_CFG	502C 102Ch
CONTROLSS_ADC2_CFG	502C 202Ch
CONTROLSS_ADC3_CFG	502C 302Ch
CONTROLSS_ADC4_CFG	502C 402Ch

Figure 3-20. ADCSOC3CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-42. ADCSOC3CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC3 Trigger Source Select. Along with the SOC3 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC3 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC3 Channel Select. Selects the channel to be converted when SOC3 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC3 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

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3.2.22 CONTROLSS_ADCn_CFG_ADCSOC4CTL Registers

3.2.22.1 ADCn_CFG_ADCSOC4CTL Register (Offset = 30h) [reset = h]

Short Description: ADC SOC4 Control Register

Long Description:

Return to Summary Table

Table 3-43. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0030h
CONTROLSS_ADC1_CFG	502C 1030h
CONTROLSS_ADC2_CFG	502C 2030h
CONTROLSS_ADC3_CFG	502C 3030h
CONTROLSS_ADC4_CFG	502C 4030h

Figure 3-21. ADCSOC4CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-44. ADCSOC4CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC4 Trigger Source Select. Along with the SOC4 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC4 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC4 Channel Select. Selects the channel to be converted when SOC4 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC4 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

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3.2.23 CONTROLSS_ADCn_CFG_ADCSOC5CTL Registers

3.2.23.1 ADCn_CFG_ADCSOC5CTL Register (Offset = 34h) [reset = h]

Short Description: ADC SOC5 Control Register

Long Description:

Return to Summary Table

Table 3-45. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0034h
CONTROLSS_ADC1_CFG	502C 1034h
CONTROLSS_ADC2_CFG	502C 2034h
CONTROLSS_ADC3_CFG	502C 3034h
CONTROLSS_ADC4_CFG	502C 4034h

Figure 3-22. ADCSOC5CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-46. ADCSOC5CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC5 Trigger Source Select. Along with the SOC5 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC5 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC5 Channel Select. Selects the channel to be converted when SOC5 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC5 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

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3.2.24 CONTROLSS_ADCn_CFG_ADCSOC6CTL Registers

3.2.24.1 ADCn_CFG_ADCSOC6CTL Register (Offset = 38h) [reset = h]

Short Description: ADC SOC6 Control Register

Long Description:

Return to Summary Table

Table 3-47. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0038h
CONTROLSS_ADC1_CFG	502C 1038h
CONTROLSS_ADC2_CFG	502C 2038h
CONTROLSS_ADC3_CFG	502C 3038h
CONTROLSS_ADC4_CFG	502C 4038h

Figure 3-23. ADCSOC6CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-48. ADCSOC6CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC6 Trigger Source Select. Along with the SOC6 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC6 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC6 Channel Select. Selects the channel to be converted when SOC6 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC6 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

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3.2.25 CONTROLSS_ADCn_CFG_ADCSOC7CTL Registers

3.2.25.1 ADCn_CFG_ADCSOC7CTL Register (Offset = 3Ch) [reset = h]

Short Description: ADC SOC7 Control Register

Long Description:

Return to Summary Table

Table 3-49. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 003Ch
CONTROLSS_ADC1_CFG	502C 103Ch
CONTROLSS_ADC2_CFG	502C 203Ch
CONTROLSS_ADC3_CFG	502C 303Ch
CONTROLSS_ADC4_CFG	502C 403Ch

Figure 3-24. ADCSOC7CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-50. ADCSOC7CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC7 Trigger Source Select. Along with the SOC7 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC7 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC7 Channel Select. Selects the channel to be converted when SOC7 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC7 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

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3.2.26 CONTROLSS_ADCn_CFG_ADCSOC8CTL Registers

3.2.26.1 ADCn_CFG_ADCSOC8CTL Register (Offset = 40h) [reset = h]

Short Description: ADC SOC8 Control Register

Long Description:

Return to Summary Table

Table 3-51. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0040h
CONTROLSS_ADC1_CFG	502C 1040h
CONTROLSS_ADC2_CFG	502C 2040h
CONTROLSS_ADC3_CFG	502C 3040h
CONTROLSS_ADC4_CFG	502C 4040h

Figure 3-25. ADCSOC8CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-52. ADCSOC8CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC8 Trigger Source Select. Along with the SOC8 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC8 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC8 Channel Select. Selects the channel to be converted when SOC8 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC8 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device data sheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

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3.2.27 CONTROLSS_ADCn_CFG_ADCSOC9CTL Registers

3.2.27.1 ADCn_CFG_ADCSOC9CTL Register (Offset = 44h) [reset = h]

Short Description: ADC SOC9 Control Register

Long Description:

Return to Summary Table

Table 3-53. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0044h
CONTROLSS_ADC1_CFG	502C 1044h
CONTROLSS_ADC2_CFG	502C 2044h
CONTROLSS_ADC3_CFG	502C 3044h
CONTROLSS_ADC4_CFG	502C 4044h

Figure 3-26. ADCSOC9CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-54. ADCSOC9CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC9 Trigger Source Select. Along with the SOC9 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC9 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC9 Channel Select. Selects the channel to be converted when SOC9 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC9 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

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3.2.28 CONTROLSS_ADCn_CFG_ADCSOC10CTL Registers

3.2.28.1 ADCn_CFG_ADCSOC10CTL Register (Offset = 48h) [reset = h]

Short Description: ADC SOC10 Control Register

Long Description:

Return to Summary Table

Table 3-55. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0048h
CONTROLSS_ADC1_CFG	502C 1048h
CONTROLSS_ADC2_CFG	502C 2048h
CONTROLSS_ADC3_CFG	502C 3048h
CONTROLSS_ADC4_CFG	502C 4048h

Figure 3-27. ADCSOC10CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-56. ADCSOC10CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC10 Trigger Source Select. Along with the SOC10 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC10 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC10 Channel Select. Selects the channel to be converted when SOC10 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC10 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

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3.2.29 CONTROLSS_ADCn_CFG_ADCSOC11CTL Registers

3.2.29.1 ADCn_CFG_ADCSOC11CTL Register (Offset = 4Ch) [reset = h]

Short Description: ADC SOC11 Control Register

Long Description:

Return to Summary Table

Table 3-57. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 004Ch
CONTROLSS_ADC1_CFG	502C 104Ch
CONTROLSS_ADC2_CFG	502C 204Ch
CONTROLSS_ADC3_CFG	502C 304Ch
CONTROLSS_ADC4_CFG	502C 404Ch

Figure 3-28. ADCSOC11CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-58. ADCSOC11CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC11 Trigger Source Select. Along with the SOC11 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC11 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC11 Channel Select. Selects the channel to be converted when SOC11 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC11 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

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3.2.30 CONTROLSS_ADCn_CFG_ADCSOC12CTL Registers

3.2.30.1 ADCn_CFG_ADCSOC12CTL Register (Offset = 50h) [reset = h]

Short Description: ADC SOC12 Control Register

Long Description:

Return to Summary Table

Table 3-59. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0050h
CONTROLSS_ADC1_CFG	502C 1050h
CONTROLSS_ADC2_CFG	502C 2050h
CONTROLSS_ADC3_CFG	502C 3050h
CONTROLSS_ADC4_CFG	502C 4050h

Figure 3-29. ADCSOC12CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-60. ADCSOC12CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC12 Trigger Source Select. Along with the SOC12 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC12 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC12 Channel Select. Selects the channel to be converted when SOC12 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC12 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

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3.2.31 CONTROLSS_ADCn_CFG_ADCSOC13CTL Registers

3.2.31.1 ADCn_CFG_ADCSOC13CTL Register (Offset = 54h) [reset = h]

Short Description: ADC SOC13 Control Register

Long Description:

Return to Summary Table

Table 3-61. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0054h
CONTROLSS_ADC1_CFG	502C 1054h
CONTROLSS_ADC2_CFG	502C 2054h
CONTROLSS_ADC3_CFG	502C 3054h
CONTROLSS_ADC4_CFG	502C 4054h

Figure 3-30. ADCSOC13CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-62. ADCSOC13CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC13 Trigger Source Select. Along with the SOC13 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC13 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC13 Channel Select. Selects the channel to be converted when SOC13 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC13 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

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3.2.32 CONTROLSS_ADCn_CFG_ADCSOC14CTL Registers

3.2.32.1 ADCn_CFG_ADCSOC14CTL Register (Offset = 58h) [reset = h]

Short Description: ADC SOC14 Control Register

Long Description:

Return to Summary Table

Table 3-63. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0058h
CONTROLSS_ADC1_CFG	502C 1058h
CONTROLSS_ADC2_CFG	502C 2058h
CONTROLSS_ADC3_CFG	502C 3058h
CONTROLSS_ADC4_CFG	502C 4058h

Figure 3-31. ADCSOC14CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-64. ADCSOC14CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC14 Trigger Source Select. Along with the SOC14 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC14 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC14 Channel Select. Selects the channel to be converted when SOC14 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC14 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device datasheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

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3.2.33 CONTROLSS_ADCn_CFG_ADCSOC15CTL Registers

3.2.33.1 ADCn_CFG_ADCSOC15CTL Register (Offset = 5Ch) [reset = h]

Short Description: ADC SOC15 Control Register

Long Description:

Return to Summary Table

Table 3-65. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 005Ch
CONTROLSS_ADC1_CFG	502C 105Ch
CONTROLSS_ADC2_CFG	502C 205Ch
CONTROLSS_ADC3_CFG	502C 305Ch
CONTROLSS_ADC4_CFG	502C 405Ch

Figure 3-32. ADCSOC15CTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					TRIGSEL							CHSEL			
R					R/W							R/W			
0					0							0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHSEL	RESERVED							ACQPS							
R/W	R							R/W							
0	0							0							

Access Types Legend

Table 3-66. ADCSOC15CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	RESERVED	R		Reserved
26 - 20	TRIGSEL	R/W	0h	SOC15 Trigger Source Select. Along with the SOC15 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC15 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it. 00h - 7Fh: See AM602 Spec. for trigger defintion
19 - 15	CHSEL	R/W	0h	SOC15 Channel Select. Selects the channel to be converted when SOC15 is received by the ADC. 00h ADCIN0 01h ADCIN1 02h ADCIN2 03h ADCIN3 ... 1Dh ADCIN29 1Eh ADCIN30 1Fh ADCIN31
14 - 9	RESERVED	R		Reserved
8 - 0	ACQPS	R/W	0h	SOC15 Acquisition Prescale. Controls the sample and hold window for this SOC. The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The device data sheet will also specify a minimum sample and hold window duration. 000h Sample window is 1 system clock cycle wide 001h Sample window is 2 system clock cycles wide 002h Sample window is 3 system clock cycles wide ... 1FFh Sample window is 512 system clock cycles wide

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3.2.34 CONTROLSS_ADCn_CFG_ADCEVTSTAT Registers

3.2.34.1 ADCn_CFG_ADCEVTSTAT Register (Offset = 60h) [reset = h]

Short Description: ADC Event Status Register

Long Description:

Return to Summary Table

Table 3-67. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0060h
CONTROLSS_ADC1_CFG	502C 1060h
CONTROLSS_ADC2_CFG	502C 2060h
CONTROLSS_ADC3_CFG	502C 3060h
CONTROLSS_ADC4_CFG	502C 4060h

Figure 3-33. ADCEVTSTAT Name Register

15	14	13	12	11	10	9	8
RESERVED	PPB4ZER	PPB4TRIPLO	PPB4TRIPHI	RESERVED	PPB3ZER	PPB3TRIPLO	PPB3TRIPHI
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RESERVED	PPB2ZER	PPB2TRIPLO	PPB2TRIPHI	RESERVED	PPB1ZER	PPB1TRIPLO	PPB1TRIPHI
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-68. ADCEVTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	PPB4ZER	R	0h	Post Processing Block 4 Zero Crossing Flag. When set indicates the ADCPPB4RESULT register has changed sign. This bit is gated by EOC signal.
13	PPB4TRIPLO	R	0h	Post Processing Block 4 Trip Low Flag. When set indicates a digital compare trip low event has occurred.
12	PPB4TRIPHI	R	0h	Post Processing Block 4 Trip High Flag. When set indicates a digital compare trip high event has occurred.
11	RESERVED	R		Reserved
10	PPB3ZER	R	0h	Post Processing Block 3 Zero Crossing Flag. When set indicates the ADCPPB3RESULT register has changed sign. This bit is gated by EOC signal.
9	PPB3TRIPLO	R	0h	Post Processing Block 3 Trip Low Flag. When set indicates a digital compare trip low event has occurred.
8	PPB3TRIPHI	R	0h	Post Processing Block 3 Trip High Flag. When set indicates a digital compare trip high event has occurred.
7	RESERVED	R		Reserved
6	PPB2ZER	R	0h	Post Processing Block 2 Zero Crossing Flag. When set indicates the ADCPPB2RESULT register has changed sign. This bit is gated by EOC signal.
5	PPB2TRIPLO	R	0h	Post Processing Block 2 Trip Low Flag. When set indicates a digital compare trip low event has occurred.
4	PPB2TRIPHI	R	0h	Post Processing Block 2 Trip High Flag. When set indicates a digital compare trip high event has occurred.

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Table 3-68. ADCEVTSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R		Reserved
2	PPB1ZER	R	0h	Post Processing Block 1 Zero Crossing Flag. When set indicates the ADCPPB1RESULT register has changed sign. This bit is gated by EOC signal.
1	PPB1TRIPLO	R	0h	Post Processing Block 1 Trip Low Flag. When set indicates a digital compare trip low event has occurred.
0	PPB1TRIPHI	R	0h	Post Processing Block 1 Trip High Flag. When set indicates a digital compare trip high event has occurred.

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3.2.35 CONTROLSS_ADCn_CFG_ADCEVTCLR Registers

3.2.35.1 ADCn_CFG_ADCEVTCLR Register (Offset = 64h) [reset = h]

Short Description: ADC Event Clear Register

Long Description:

Return to Summary Table

Table 3-69. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0064h
CONTROLSS_ADC1_CFG	502C 1064h
CONTROLSS_ADC2_CFG	502C 2064h
CONTROLSS_ADC3_CFG	502C 3064h
CONTROLSS_ADC4_CFG	502C 4064h

Figure 3-34. ADCEVTCLR Name Register

15	14	13	12	11	10	9	8
RESERVED	PPB4ZER	PPB4TRIPLO	PPB4TRIPHI	RESERVED	PPB3ZER	PPB3TRIPLO	PPB3TRIPHI
R	R-0/W	R-0/W	R-0/W	R	R-0/W	R-0/W	R-0/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RESERVED	PPB2ZER	PPB2TRIPLO	PPB2TRIPHI	RESERVED	PPB1ZER	PPB1TRIPLO	PPB1TRIPHI
R	R-0/W	R-0/W	R-0/W	R	R-0/W	R-0/W	R-0/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-70. ADCEVTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	PPB4ZER	R-0/W	0h	Post Processing Block 4 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.
13	PPB4TRIPLO	R-0/W	0h	Post Processing Block 4 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.
12	PPB4TRIPHI	R-0/W	0h	Post Processing Block 4 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.
11	RESERVED	R		Reserved
10	PPB3ZER	R-0/W	0h	Post Processing Block 3 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.
9	PPB3TRIPLO	R-0/W	0h	Post Processing Block 3 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.
8	PPB3TRIPHI	R-0/W	0h	Post Processing Block 3 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.
7	RESERVED	R		Reserved
6	PPB2ZER	R-0/W	0h	Post Processing Block 2 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.
5	PPB2TRIPLO	R-0/W	0h	Post Processing Block 2 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.
4	PPB2TRIPHI	R-0/W	0h	Post Processing Block 2 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.
3	RESERVED	R		Reserved
2	PPB1ZER	R-0/W	0h	Post Processing Block 1 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.

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Table 3-70. ADCEVTCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PPB1TRIPLO	R-0/W	0h	Post Processing Block 1 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.
0	PPB1TRIPHI	R-0/W	0h	Post Processing Block 1 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.

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3.2.36 CONTROLSS_ADCn_CFG_ADCEVTSEL Registers

3.2.36.1 ADCn_CFG_ADCEVTSEL Register (Offset = 68h) [reset = h]

Short Description: ADC Event Selection Register

Long Description:

Return to Summary Table

Table 3-71. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0068h
CONTROLSS_ADC1_CFG	502C 1068h
CONTROLSS_ADC2_CFG	502C 2068h
CONTROLSS_ADC3_CFG	502C 3068h
CONTROLSS_ADC4_CFG	502C 4068h

Figure 3-35. ADCEVTSEL Name Register

15	14	13	12	11	10	9	8
RESERVED	PPB4ZER	PPB4TRIPLO	PPB4TRIPHI	RESERVED	PPB3ZER	PPB3TRIPLO	PPB3TRIPHI
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RESERVED	PPB2ZER	PPB2TRIPLO	PPB2TRIPHI	RESERVED	PPB1ZER	PPB1TRIPLO	PPB1TRIPHI
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-72. ADCEVTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	PPB4ZER	R/W	0h	Post Processing Block 4 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
13	PPB4TRIPLO	R/W	0h	Post Processing Block 4 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
12	PPB4TRIPHI	R/W	0h	Post Processing Block 4 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
11	RESERVED	R		Reserved
10	PPB3ZER	R/W	0h	Post Processing Block 3 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
9	PPB3TRIPLO	R/W	0h	Post Processing Block 3 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
8	PPB3TRIPHI	R/W	0h	Post Processing Block 3 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.

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Table 3-72. ADCEVTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	R		Reserved
6	PPB2ZER	R/W	0h	Post Processing Block 2 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
5	PPB2TRIPLO	R/W	0h	Post Processing Block 2 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
4	PPB2TRIPHI	R/W	0h	Post Processing Block 2 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
3	RESERVED	R		Reserved
2	PPB1ZER	R/W	0h	Post Processing Block 1 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
1	PPB1TRIPLO	R/W	0h	Post Processing Block 1 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.
0	PPB1TRIPHI	R/W	0h	Post Processing Block 1 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.

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3.2.37 CONTROLSS_ADCn_CFG_ADCEVTINTSEL Registers

3.2.37.1 ADCn_CFG_ADCEVTINTSEL Register (Offset = 6Ch) [reset = h]

Short Description: ADC Event Interrupt Selection Register

Long Description:

Return to Summary Table

Table 3-73. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 006Ch
CONTROLSS_ADC1_CFG	502C 106Ch
CONTROLSS_ADC2_CFG	502C 206Ch
CONTROLSS_ADC3_CFG	502C 306Ch
CONTROLSS_ADC4_CFG	502C 406Ch

Figure 3-36. ADCEVTINTSEL Name Register

15	14	13	12	11	10	9	8
RESERVED	PPB4ZER	PPB4TRIPLO	PPB4TRIPHI	RESERVED	PPB3ZER	PPB3TRIPLO	PPB3TRIPHI
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
RESERVED	PPB2ZER	PPB2TRIPLO	PPB2TRIPHI	RESERVED	PPB1ZER	PPB1TRIPLO	PPB1TRIPHI
R	R/W	R/W	R/W	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-74. ADCEVTINTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	PPB4ZER	R/W	0h	Post Processing Block 4 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
13	PPB4TRIPLO	R/W	0h	Post Processing Block 4 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
12	PPB4TRIPHI	R/W	0h	Post Processing Block 4 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
11	RESERVED	R		Reserved
10	PPB3ZER	R/W	0h	Post Processing Block 3 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
9	PPB3TRIPLO	R/W	0h	Post Processing Block 3 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
8	PPB3TRIPHI	R/W	0h	Post Processing Block 3 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.

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Table 3-74. ADCEVTINTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	R		Reserved
6	PPB2ZER	R/W	0h	Post Processing Block 2 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
5	PPB2TRIPLO	R/W	0h	Post Processing Block 2 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
4	PPB2TRIPHI	R/W	0h	Post Processing Block 2 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
3	RESERVED	R		Reserved
2	PPB1ZER	R/W	0h	Post Processing Block 1 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
1	PPB1TRIPLO	R/W	0h	Post Processing Block 1 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.
0	PPB1TRIPHI	R/W	0h	Post Processing Block 1 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.

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3.2.38 CONTROLSS_ADCn_CFG_ADCOSDETECT Registers

3.2.38.1 ADCn_CFG_ADCOSDETECT Register (Offset = 70h) [reset = h]

Short Description: ADC Open and Shorts Detect Register

Long Description:

Return to Summary Table

Table 3-75. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0070h
CONTROLSS_ADC1_CFG	502C 1070h
CONTROLSS_ADC2_CFG	502C 2070h
CONTROLSS_ADC3_CFG	502C 3070h
CONTROLSS_ADC4_CFG	502C 4070h

Figure 3-37. ADCOSDETECT Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED					DETECTCFG		
R					R/W		
0					0		

Access Types Legend

Table 3-76. ADCOSDETECT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 3	RESERVED	R		Reserved
2 - 0	DETECTCFG	R/W	0h	ADC Opens and Shorts Detect Configuration. This bit field defines the open/shorts detection circuit state. 0h Open/Shorts detection circuit is disabled. 1h Open/Shorts detection circuit is enabled at zero scale. 2h Open/Shorts detection circuit is enabled at full scale. 3h Open/Shorts detection circuit is enabled at (nominal) 5/12 scale. 4h Open/Shorts detection circuit is enabled at (nominal) 7/12 scale. 5h Open/Shorts detection circuit is enabled with a (nominal) 5K pulldown to VSSA. 6h Open/Shorts detection circuit is enabled with a (nominal) 5K pullup to VDDA. 7h Open/Shorts detection circuit is enabled with a (nominal) 7K pulldown to VSSA.

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3.2.39 CONTROLSS_ADCn_CFG_ADCCOUNTER Registers

3.2.39.1 ADCn_CFG_ADCCOUNTER Register (Offset = 72h) [reset = h]

Short Description: ADC Counter Register

Long Description:

Return to Summary Table

Table 3-77. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0072h
CONTROLSS_ADC1_CFG	502C 1072h
CONTROLSS_ADC2_CFG	502C 2072h
CONTROLSS_ADC3_CFG	502C 3072h
CONTROLSS_ADC4_CFG	502C 4072h

Figure 3-38. ADCCOUNTER Name Register

15	14	13	12	11	10	9	8
RESERVED				FREECOUNT			
R				R			
0				0			
7	6	5	4	3	2	1	0
FREECOUNT							
R							
0							

Access Types Legend

Table 3-78. ADCCOUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R		Reserved
11 - 0	FREECOUNT	R	0h	ADC Free Running Counter Value. This bit field reflects the status of the free running ADC counter.

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3.2.40 CONTROLSS_ADCn_CFG_ADCREV Registers

3.2.40.1 ADCn_CFG_ADCREV Register (Offset = 74h) [reset = h]

Short Description: ADC Revision Register

Long Description:

Return to Summary Table

Table 3-79. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0074h
CONTROLSS_ADC1_CFG	502C 1074h
CONTROLSS_ADC2_CFG	502C 2074h
CONTROLSS_ADC3_CFG	502C 3074h
CONTROLSS_ADC4_CFG	502C 4074h

Figure 3-39. ADCREV Name Register

15	14	13	12	11	10	9	8
REV							
R							
1							
7	6	5	4	3	2	1	0
TYPE							
R							
101							

Access Types Legend

Table 3-80. ADCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	REV	R	1h	ADC Revision. To allow documentation of differences between revisions. First version is labeled as 00h.
7 - 0	TYPE	R	5h	ADC Type. Always set to 5 for this ADC.

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3.2.41 CONTROLSS_ADCn_CFG_ADCOFFTRIM Registers

3.2.41.1 ADCn_CFG_ADCOFFTRIM Register (Offset = 76h) [reset = h]

Short Description: ADC Offset Trim Register

Long Description:

Return to Summary Table

Table 3-81. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0076h
CONTROLSS_ADC1_CFG	502C 1076h
CONTROLSS_ADC2_CFG	502C 2076h
CONTROLSS_ADC3_CFG	502C 3076h
CONTROLSS_ADC4_CFG	502C 4076h

Figure 3-40. ADCOFFTRIM Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
OFFTRIM							
R/W							
0							

Access Types Legend

Table 3-82. ADCOFFTRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R		Reserved
7 - 0	OFFTRIM	R/W	0h	ADC Offset Trim Adjusts the conversion results of the converter up or down to account for offset error in the ADC. A factory trim setting will be loaded during device boot. Offset can be corrected in the range of +7 to -8 LSBs. Value is 16*Offset in 8-bit 2's complement: 7 LSB (16*7) = 112 6 LSB (16*6) = 96 5 LSB (16*5) = 80 4 LSB (16*4) = 64 3 LSB (16*3) = 48 2 LSB (16*2) = 32 1 LSB (16*1) = 16 0 LSB (16*0) = 0 -1 LSB (16*(-1)) = 240 : : -7LSB(16*(-7)) = 144

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3.2.42 CONTROLSS_ADCn_CFG_ADCCONFIG Registers

3.2.42.1 ADCn_CFG_ADCCONFIG Register (Offset = 7Ch) [reset = h]

Short Description: ADC Config Register

Long Description:

Return to Summary Table

Table 3-83. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 007Ch
CONTROLSS_ADC1_CFG	502C 107Ch
CONTROLSS_ADC2_CFG	502C 207Ch
CONTROLSS_ADC3_CFG	502C 307Ch
CONTROLSS_ADC4_CFG	502C 407Ch

Figure 3-41. ADCCONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CONFIG															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONFIG															
R/W															
0															

Access Types Legend

Table 3-84. ADCCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CONFIG	R/W	0h	ADC Configuration. This bit field is used for TI internal testing/ debugging.

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3.2.43 CONTROLSS_ADCn_CFG_ADCPPB1CONFIG Registers

3.2.43.1 ADCn_CFG_ADCPPB1CONFIG Register (Offset = 80h) [reset = h]

Short Description: ADC PPB1 Config Register

Long Description:

Return to Summary Table

Table 3-85. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0080h
CONTROLSS_ADC1_CFG	502C 1080h
CONTROLSS_ADC2_CFG	502C 2080h
CONTROLSS_ADC3_CFG	502C 3080h
CONTROLSS_ADC4_CFG	502C 4080h

Figure 3-42. ADCPPB1CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED		CBCEN	TWOSCOMPEN	CONFIG			
R		R/W	R/W	R/W			
0		0	0	0			

Access Types Legend

Table 3-86. ADCPPB1CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 6	RESERVED	R		Reserved
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block 1 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB1RESULT register. 0 ADCPPB1RESULT = ADCRESULTx - ADCPPB1OFFREF 1 ADCPPB1RESULT = ADCPPB1OFFREF - ADCRESULTx

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Table 3-86. ADCPPB1CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	CONFIG	R/W	0h	ADC Post Processing Block 1 Configuration. This bit field defines which SOC/EOC/RESULT is assocatied with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 1 0001 SOC1/EOC1/RESULT1 is associated with post processing block 1 0010 SOC2/EOC2/RESULT2 is associated with post processing block 1 0011 SOC3/EOC3/RESULT3 is associated with post processing block 1 0100 SOC4/EOC4/RESULT4 is associated with post processing block 1 0101 SOC5/EOC5/RESULT5 is associated with post processing block 1 0110 SOC6/EOC6/RESULT6 is associated with post processing block 1 0111 SOC7/EOC7/RESULT7 is associated with post processing block 1 1000 SOC8/EOC8/RESULT8 is associated with post processing block 1 1001 SOC9/EOC9/RESULT9 is associated with post processing block 1 1010 SOC10/EOC10/RESULT10 is associated with post processing block 1 1011 SOC11/EOC11/RESULT11 is associated with post processing block 1 1100 SOC12/EOC12/RESULT12 is associated with post processing block 1 1101 SOC13/EOC13/RESULT13 is associated with post processing block 1 1110 SOC14/EOC14/RESULT14 is associated with post processing block 1 1111 SOC15/EOC15/RESULT15 is associated with post processing block 1

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3.2.44 CONTROLSS_ADCn_CFG_ADCPPB1STAMP Registers

3.2.44.1 ADCn_CFG_ADCPPB1STAMP Register (Offset = 82h) [reset = h]

Short Description: ADC PPB1 Sample Delay Time Stamp Register

Long Description:

Return to Summary Table

Table 3-87. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0082h
CONTROLSS_ADC1_CFG	502C 1082h
CONTROLSS_ADC2_CFG	502C 2082h
CONTROLSS_ADC3_CFG	502C 3082h
CONTROLSS_ADC4_CFG	502C 4082h

Figure 3-43. ADCPPB1STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED				DLYSTAMP			
R				R			
0				0			
7	6	5	4	3	2	1	0
DLYSTAMP							
R							
0							

Access Types Legend

Table 3-88. ADCPPB1STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R		Reserved
11 - 0	DLYSTAMP	R	0h	ADC Post Processing Block 1 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

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3.2.45 CONTROLSS_ADCn_CFG_ADCPPB1OFFCAL Registers

3.2.45.1 ADCn_CFG_ADCPPB1OFFCAL Register (Offset = 84h) [reset = h]

Short Description: ADC PPB1 Offset Calibration Register

Long Description:

Return to Summary Table

Table 3-89. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0084h
CONTROLSS_ADC1_CFG	502C 1084h
CONTROLSS_ADC2_CFG	502C 2084h
CONTROLSS_ADC3_CFG	502C 3084h
CONTROLSS_ADC4_CFG	502C 4084h

Figure 3-44. ADCPPB1OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED						OFFCAL	
R						R/W	
0						0	
7	6	5	4	3	2	1	0
OFFCAL							
R/W							
0							

Access Types Legend

Table 3-90. ADCPPB1OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	R		Reserved
9 - 0	OFFCAL	R/W	0h	ADC Post Processing Block 1 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000h and 0FFFh before being stored into the ADCRESULT register.

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3.2.46 CONTROLSS_ADCn_CFG_ADCPPB1OFFREF Registers

3.2.46.1 ADCn_CFG_ADCPPB1OFFREF Register (Offset = 86h) [reset = h]

Short Description: ADC PPB1 Offset Reference Register

Long Description:

Return to Summary Table

Table 3-91. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0086h
CONTROLSS_ADC1_CFG	502C 1086h
CONTROLSS_ADC2_CFG	502C 2086h
CONTROLSS_ADC3_CFG	502C 3086h
CONTROLSS_ADC4_CFG	502C 4086h

Figure 3-45. ADCPPB1OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
R/W							
0							
7	6	5	4	3	2	1	0
OFFREF							
R/W							
0							

Access Types Legend

Table 3-92. ADCPPB1OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	OFFREF	R/W	0h	ADC Post Processing Block 1 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB1RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

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3.2.47 CONTROLSS_ADCn_CFG_ADCPPB1TRIPHI Registers

3.2.47.1 ADCn_CFG_ADCPPB1TRIPHI Register (Offset = 88h) [reset = h]

Short Description: ADC PPB1 Trip High Register

Long Description:

Return to Summary Table

Table 3-93. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0088h
CONTROLSS_ADC1_CFG	502C 1088h
CONTROLSS_ADC2_CFG	502C 2088h
CONTROLSS_ADC3_CFG	502C 3088h
CONTROLSS_ADC4_CFG	502C 4088h

Figure 3-46. ADCPPB1TRIPHI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															HSIGN
R															R/W
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITHI															
R/W															
0															

Access Types Legend

Table 3-94. ADCPPB1TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RESERVED	R		Reserved
16	HSIGN	R/W	0h	High Limit Sign Bit. This is the sign bit (17th bit) to the LIMITHI bit field when in 16-bit ADC mode.
15 - 0	LIMITHI	R/W	0h	ADC Post Processing Block 1 Trip High Limit. This value sets the digital comparator trip high limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB1RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRESULT bit field of the ADCPPB1RESULT register.

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3.2.48 CONTROLSS_ADCn_CFG_ADCPPB1TRIPLO Registers

3.2.48.1 ADCn_CFG_ADCPPB1TRIPLO Register (Offset = 8Ch) [reset = h]

Short Description: ADC PPB1 Trip Low/Trigger Time Stamp Register

Long Description:

Return to Summary Table

Table 3-95. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 008Ch
CONTROLSS_ADC1_CFG	502C 108Ch
CONTROLSS_ADC2_CFG	502C 208Ch
CONTROLSS_ADC3_CFG	502C 308Ch
CONTROLSS_ADC4_CFG	502C 408Ch

Figure 3-47. ADCPPB1TRIPLO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REQSTAMP												RESERVED			LSIGN
R												R			R/W
0												0			0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITLO															
R/W															
0															

Access Types Legend

Table 3-96. ADCPPB1TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	REQSTAMP	R	0h	ADC Post Processing Block 1 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19 - 17	RESERVED	R		Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit (17th bit) to the LIMITLO bit field when in 16-bit ADC mode.
15 - 0	LIMITLO	R/W	0h	ADC Post Processing Block 1 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB1RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB1RESULT register.

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3.2.49 CONTROLSS_ADCn_CFG_ADCPPB2CONFIG Registers

3.2.49.1 ADCn_CFG_ADCPPB2CONFIG Register (Offset = 90h) [reset = h]

Short Description: ADC PPB2 Config Register

Long Description:

Return to Summary Table

Table 3-97. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0090h
CONTROLSS_ADC1_CFG	502C 1090h
CONTROLSS_ADC2_CFG	502C 2090h
CONTROLSS_ADC3_CFG	502C 3090h
CONTROLSS_ADC4_CFG	502C 4090h

Figure 3-48. ADCPPB2CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED		CBCEN	TWOSCOMPEN	CONFIG			
R		R/W	R/W	R/W			
0		0	0	0			

Access Types Legend

Table 3-98. ADCPPB2CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 6	RESERVED	R		Reserved
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block 2 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB2RESULT register. 0 ADCPPB2RESULT = ADCRESULTx - ADCPPB2OFFREF 1 ADCPPB2RESULT = ADCPPB2OFFREF - ADCRESULTx

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Table 3-98. ADCPPB2CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	CONFIG	R/W	0h	ADC Post Processing Block 2 Configuration. This bit field defines which SOC/EOC/RESULT is assocatied with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 2 0001 SOC1/EOC1/RESULT1 is associated with post processing block 2 0010 SOC2/EOC2/RESULT2 is associated with post processing block 2 0011 SOC3/EOC3/RESULT3 is associated with post processing block 2 0100 SOC4/EOC4/RESULT4 is associated with post processing block 2 0101 SOC5/EOC5/RESULT5 is associated with post processing block 2 0110 SOC6/EOC6/RESULT6 is associated with post processing block 2 0111 SOC7/EOC7/RESULT7 is associated with post processing block 2 1000 SOC8/EOC8/RESULT8 is associated with post processing block 2 1001 SOC9/EOC9/RESULT9 is associated with post processing block 2 1010 SOC10/EOC10/RESULT10 is associated with post processing block 2 1011 SOC11/EOC11/RESULT11 is associated with post processing block 2 1100 SOC12/EOC12/RESULT12 is associated with post processing block 2 1101 SOC13/EOC13/RESULT13 is associated with post processing block 2 1110 SOC14/EOC14/RESULT14 is associated with post processing block 2 1111 SOC15/EOC15/RESULT15 is associated with post processing block 2

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3.2.50 CONTROLSS_ADCn_CFG_ADCPPB2STAMP Registers

3.2.50.1 ADCn_CFG_ADCPPB2STAMP Register (Offset = 92h) [reset = h]

Short Description: ADC PPB2 Sample Delay Time Stamp Register

Long Description:

Return to Summary Table

Table 3-99. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0092h
CONTROLSS_ADC1_CFG	502C 1092h
CONTROLSS_ADC2_CFG	502C 2092h
CONTROLSS_ADC3_CFG	502C 3092h
CONTROLSS_ADC4_CFG	502C 4092h

Figure 3-49. ADCPPB2STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED				DLYSTAMP			
R				R			
0				0			
7	6	5	4	3	2	1	0
DLYSTAMP							
R							
0							

Access Types Legend

Table 3-100. ADCPPB2STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R		Reserved
11 - 0	DLYSTAMP	R	0h	ADC Post Processing Block 2 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

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3.2.51 CONTROLSS_ADCn_CFG_ADCPPB2OFFCAL Registers

3.2.51.1 ADCn_CFG_ADCPPB2OFFCAL Register (Offset = 94h) [reset = h]

Short Description: ADC PPB2 Offset Calibration Register

Long Description:

Return to Summary Table

Table 3-101. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0094h
CONTROLSS_ADC1_CFG	502C 1094h
CONTROLSS_ADC2_CFG	502C 2094h
CONTROLSS_ADC3_CFG	502C 3094h
CONTROLSS_ADC4_CFG	502C 4094h

Figure 3-50. ADCPPB2OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED						OFFCAL	
R						R/W	
0						0	
7	6	5	4	3	2	1	0
OFFCAL							
R/W							
0							

Access Types Legend

Table 3-102. ADCPPB2OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	R		Reserved
9 - 0	OFFCAL	R/W	0h	ADC Post Processing Block 2 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000h and 0FFFh before being stored into the ADCRESULT register.

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3.2.52 CONTROLSS_ADCn_CFG_ADCPPB2OFFREF Registers

3.2.52.1 ADCn_CFG_ADCPPB2OFFREF Register (Offset = 96h) [reset = h]

Short Description: ADC PPB2 Offset Reference Register

Long Description:

Return to Summary Table

Table 3-103. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0096h
CONTROLSS_ADC1_CFG	502C 1096h
CONTROLSS_ADC2_CFG	502C 2096h
CONTROLSS_ADC3_CFG	502C 3096h
CONTROLSS_ADC4_CFG	502C 4096h

Figure 3-51. ADCPPB2OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
R/W							
0							
7	6	5	4	3	2	1	0
OFFREF							
R/W							
0							

Access Types Legend

Table 3-104. ADCPPB2OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	OFFREF	R/W	0h	ADC Post Processing Block 2 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB2RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

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3.2.53 CONTROLSS_ADCn_CFG_ADCPPB2TRIPHI Registers

3.2.53.1 ADCn_CFG_ADCPPB2TRIPHI Register (Offset = 98h) [reset = h]

Short Description: ADC PPB2 Trip High Register

Long Description:

Return to Summary Table

Table 3-105. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 0098h
CONTROLSS_ADC1_CFG	502C 1098h
CONTROLSS_ADC2_CFG	502C 2098h
CONTROLSS_ADC3_CFG	502C 3098h
CONTROLSS_ADC4_CFG	502C 4098h

Figure 3-52. ADCPPB2TRIPHI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															HSIGN
R															R/W
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITHI															
R/W															
0															

Access Types Legend

Table 3-106. ADCPPB2TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RESERVED	R		Reserved
16	HSIGN	R/W	0h	High Limit Sign Bit. This is the sign bit (17th bit) to the LIMITHI bit field when in 16-bit ADC mode.
15 - 0	LIMITHI	R/W	0h	ADC Post Processing Block 2 Trip High Limit. This value sets the digital comparator trip high limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB2RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRESULT bit field of the ADCPPB2RESULT register.

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3.2.54 CONTROLSS_ADCn_CFG_ADCPPB2TRIPLO Registers

3.2.54.1 ADCn_CFG_ADCPPB2TRIPLO Register (Offset = 9Ch) [reset = h]

Short Description: ADC PPB2 Trip Low/Trigger Time Stamp Register

Long Description:

Return to Summary Table

Table 3-107. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 009Ch
CONTROLSS_ADC1_CFG	502C 109Ch
CONTROLSS_ADC2_CFG	502C 209Ch
CONTROLSS_ADC3_CFG	502C 309Ch
CONTROLSS_ADC4_CFG	502C 409Ch

Figure 3-53. ADCPPB2TRIPLO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REQSTAMP												RESERVED			LSIGN
R												R			R/W
0												0			0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITLO															
R/W															
0															

Access Types Legend

Table 3-108. ADCPPB2TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	REQSTAMP	R	0h	ADC Post Processing Block 2 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19 - 17	RESERVED	R		Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit (17th bit) to the LIMITLO bit field when in 16-bit ADC mode.
15 - 0	LIMITLO	R/W	0h	ADC Post Processing Block 2 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB2RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB2RESULT register.

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3.2.55 CONTROLSS_ADCn_CFG_ADCPPB3CONFIG Registers

3.2.55.1 ADCn_CFG_ADCPPB3CONFIG Register (Offset = A0h) [reset = h]

Short Description: ADC PPB3 Config Register

Long Description:

Return to Summary Table

Table 3-109. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00A0h
CONTROLSS_ADC1_CFG	502C 10A0h
CONTROLSS_ADC2_CFG	502C 20A0h
CONTROLSS_ADC3_CFG	502C 30A0h
CONTROLSS_ADC4_CFG	502C 40A0h

Figure 3-54. ADCPPB3CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED		CBCEN	TWOSCOMPEN	CONFIG			
R		R/W	R/W	R/W			
0		0	0	0			

Access Types Legend

Table 3-110. ADCPPB3CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 6	RESERVED	R		Reserved
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block 3 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB3RESULT register. 0 ADCPPB3RESULT = ADCRESULTx - ADCPPB3OFFREF 1 ADCPPB3RESULT = ADCPPB3OFFREF - ADCRESULTx

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Table 3-110. ADCPPB3CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	CONFIG	R/W	0h	ADC Post Processing Block 3 Configuration. This bit field defines which SOC/EOC/RESULT is assocatied with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 3 0001 SOC1/EOC1/RESULT1 is associated with post processing block 3 0010 SOC2/EOC2/RESULT2 is associated with post processing block 3 0011 SOC3/EOC3/RESULT3 is associated with post processing block 3 0100 SOC4/EOC4/RESULT4 is associated with post processing block 3 0101 SOC5/EOC5/RESULT5 is associated with post processing block 3 0110 SOC6/EOC6/RESULT6 is associated with post processing block 3 0111 SOC7/EOC7/RESULT7 is associated with post processing block 3 1000 SOC8/EOC8/RESULT8 is associated with post processing block 3 1001 SOC9/EOC9/RESULT9 is associated with post processing block 3 1010 SOC10/EOC10/RESULT10 is associated with post processing block 3 1011 SOC11/EOC11/RESULT11 is associated with post processing block 3 1100 SOC12/EOC12/RESULT12 is associated with post processing block 3 1101 SOC13/EOC13/RESULT13 is associated with post processing block 3 1110 SOC14/EOC14/RESULT14 is associated with post processing block 3 1111 SOC15/EOC15/RESULT15 is associated with post processing block 3

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3.2.56 CONTROLSS_ADCn_CFG_ADCPPB3STAMP Registers

3.2.56.1 ADCn_CFG_ADCPPB3STAMP Register (Offset = A2h) [reset = h]

Short Description: ADC PPB3 Sample Delay Time Stamp Register

Long Description:

Return to Summary Table

Table 3-111. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00A2h
CONTROLSS_ADC1_CFG	502C 10A2h
CONTROLSS_ADC2_CFG	502C 20A2h
CONTROLSS_ADC3_CFG	502C 30A2h
CONTROLSS_ADC4_CFG	502C 40A2h

Figure 3-55. ADCPPB3STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED				DLYSTAMP			
R				R			
0				0			
7	6	5	4	3	2	1	0
DLYSTAMP							
R							
0							

Access Types Legend

Table 3-112. ADCPPB3STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R		Reserved
11 - 0	DLYSTAMP	R	0h	ADC Post Processing Block 3 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

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3.2.57 CONTROLSS_ADCn_CFG_ADCPPB3OFFCAL Registers

3.2.57.1 ADCn_CFG_ADCPPB3OFFCAL Register (Offset = A4h) [reset = h]

Short Description: ADC PPB3 Offset Calibration Register

Long Description:

Return to Summary Table

Table 3-113. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00A4h
CONTROLSS_ADC1_CFG	502C 10A4h
CONTROLSS_ADC2_CFG	502C 20A4h
CONTROLSS_ADC3_CFG	502C 30A4h
CONTROLSS_ADC4_CFG	502C 40A4h

Figure 3-56. ADCPPB3OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED						OFFCAL	
R						R/W	
0						0	
7	6	5	4	3	2	1	0
OFFCAL							
R/W							
0							

Access Types Legend

Table 3-114. ADCPPB3OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	R		Reserved
9 - 0	OFFCAL	R/W	0h	ADC Post Processing Block 3 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000h and 0FFFh before being stored into the ADCRESULT register.

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3.2.58 CONTROLSS_ADCn_CFG_ADCPPB3OFFREF Registers

3.2.58.1 ADCn_CFG_ADCPPB3OFFREF Register (Offset = A6h) [reset = h]

Short Description: ADC PPB3 Offset Reference Register

Long Description:

Return to Summary Table

Table 3-115. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00A6h
CONTROLSS_ADC1_CFG	502C 10A6h
CONTROLSS_ADC2_CFG	502C 20A6h
CONTROLSS_ADC3_CFG	502C 30A6h
CONTROLSS_ADC4_CFG	502C 40A6h

Figure 3-57. ADCPPB3OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
R/W							
0							
7	6	5	4	3	2	1	0
OFFREF							
R/W							
0							

Access Types Legend

Table 3-116. ADCPPB3OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	OFFREF	R/W	0h	ADC Post Processing Block 3 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB3RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

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3.2.59 CONTROLSS_ADCn_CFG_ADCPPB3TRIPHI Registers

3.2.59.1 ADCn_CFG_ADCPPB3TRIPHI Register (Offset = A8h) [reset = h]

Short Description: ADC PPB3 Trip High Register

Long Description:

Return to Summary Table

Table 3-117. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00A8h
CONTROLSS_ADC1_CFG	502C 10A8h
CONTROLSS_ADC2_CFG	502C 20A8h
CONTROLSS_ADC3_CFG	502C 30A8h
CONTROLSS_ADC4_CFG	502C 40A8h

Figure 3-58. ADCPPB3TRIPHI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															HSIGN
R															R/W
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITHI															
R/W															
0															

Access Types Legend

Table 3-118. ADCPPB3TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RESERVED	R		Reserved
16	HSIGN	R/W	0h	High Limit Sign Bit. This is the sign bit (17th bit) to the LIMITHI bit field when in 16-bit ADC mode.
15 - 0	LIMITHI	R/W	0h	ADC Post Processing Block 3 Trip High Limit. This value sets the digital comparator trip high limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB3RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRESULT bit field of the ADCPPB3RESULT register.

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3.2.60 CONTROLSS_ADCn_CFG_ADCPPB3TRIPLO Registers

3.2.60.1 ADCn_CFG_ADCPPB3TRIPLO Register (Offset = ACh) [reset = h]

Short Description: ADC PPB3 Trip Low/Trigger Time Stamp Register

Long Description:

Return to Summary Table

Table 3-119. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00ACh
CONTROLSS_ADC1_CFG	502C 10ACh
CONTROLSS_ADC2_CFG	502C 20ACh
CONTROLSS_ADC3_CFG	502C 30ACh
CONTROLSS_ADC4_CFG	502C 40ACh

Figure 3-59. ADCPPB3TRIPLO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REQSTAMP												RESERVED			LSIGN
R												R			R/W
0												0			0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITLO															
R/W															
0															

Access Types Legend

Table 3-120. ADCPPB3TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	REQSTAMP	R	0h	ADC Post Processing Block 3 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19 - 17	RESERVED	R		Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit (17th bit) to the LIMITLO bit field when in 16-bit ADC mode.
15 - 0	LIMITLO	R/W	0h	ADC Post Processing Block 3 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB3RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB3RESULT register.

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3.2.61 CONTROLSS_ADCn_CFG_ADCPPB4CONFIG Registers

3.2.61.1 ADCn_CFG_ADCPPB4CONFIG Register (Offset = B0h) [reset = h]

Short Description: ADC PPB4 Config Register

Long Description:

Return to Summary Table

Table 3-121. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00B0h
CONTROLSS_ADC1_CFG	502C 10B0h
CONTROLSS_ADC2_CFG	502C 20B0h
CONTROLSS_ADC3_CFG	502C 30B0h
CONTROLSS_ADC4_CFG	502C 40B0h

Figure 3-60. ADCPPB4CONFIG Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED		CBCEN	TWOSCOMPEN	CONFIG			
R		R/W	R/W	R/W			
0		0	0	0			

Access Types Legend

Table 3-122. ADCPPB4CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 6	RESERVED	R		Reserved
5	CBCEN	R/W	0h	ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.
4	TWOSCOMPEN	R/W	0h	ADC Post Processing Block 4 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB4RESULT register. 0 ADCPPB4RESULT = ADCRESULTx - ADCPPB4OFFREF 1 ADCPPB4RESULT = ADCPPB4OFFREF - ADCRESULTx

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Table 3-122. ADCPPB4CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 0	CONFIG	R/W	0h	ADC Post Processing Block 4 Configuration. This bit field defines which SOC/EOC/RESULT is assocatied with this post processing block. 0000 SOC0/EOC0/RESULT0 is associated with post processing block 4 0001 SOC1/EOC1/RESULT1 is associated with post processing block 4 0010 SOC2/EOC2/RESULT2 is associated with post processing block 4 0011 SOC3/EOC3/RESULT3 is associated with post processing block 4 0100 SOC4/EOC4/RESULT4 is associated with post processing block 4 0101 SOC5/EOC5/RESULT5 is associated with post processing block 4 0110 SOC6/EOC6/RESULT6 is associated with post processing block 4 0111 SOC7/EOC7/RESULT7 is associated with post processing block 4 1000 SOC8/EOC8/RESULT8 is associated with post processing block 4 1001 SOC9/EOC9/RESULT9 is associated with post processing block 4 1010 SOC10/EOC10/RESULT10 is associated with post processing block 4 1011 SOC11/EOC11/RESULT11 is associated with post processing block 4 1100 SOC12/EOC12/RESULT12 is associated with post processing block 4 1101 SOC13/EOC13/RESULT13 is associated with post processing block 4 1110 SOC14/EOC14/RESULT14 is associated with post processing block 4 1111 SOC15/EOC15/RESULT15 is associated with post processing block 4

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3.2.62 CONTROLSS_ADCn_CFG_ADCPPB4STAMP Registers

3.2.62.1 ADCn_CFG_ADCPPB4STAMP Register (Offset = B2h) [reset = h]

Short Description: ADC PPB4 Sample Delay Time Stamp Register

Long Description:

Return to Summary Table

Table 3-123. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00B2h
CONTROLSS_ADC1_CFG	502C 10B2h
CONTROLSS_ADC2_CFG	502C 20B2h
CONTROLSS_ADC3_CFG	502C 30B2h
CONTROLSS_ADC4_CFG	502C 40B2h

Figure 3-61. ADCPPB4STAMP Name Register

15	14	13	12	11	10	9	8
RESERVED				DLYSTAMP			
R				R			
0				0			
7	6	5	4	3	2	1	0
DLYSTAMP							
R							
0							

Access Types Legend

Table 3-124. ADCPPB4STAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R		Reserved
11 - 0	DLYSTAMP	R	0h	ADC Post Processing Block 4 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample.

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3.2.63 CONTROLSS_ADCn_CFG_ADCPPB4OFFCAL Registers

3.2.63.1 ADCn_CFG_ADCPPB4OFFCAL Register (Offset = B4h) [reset = h]

Short Description: ADC PPB4 Offset Calibration Register

Long Description:

Return to Summary Table

Table 3-125. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00B4h
CONTROLSS_ADC1_CFG	502C 10B4h
CONTROLSS_ADC2_CFG	502C 20B4h
CONTROLSS_ADC3_CFG	502C 30B4h
CONTROLSS_ADC4_CFG	502C 40B4h

Figure 3-62. ADCPPB4OFFCAL Name Register

15	14	13	12	11	10	9	8
RESERVED						OFFCAL	
R						R/W	
0						0	
7	6	5	4	3	2	1	0
OFFCAL							
R/W							
0							

Access Types Legend

Table 3-126. ADCPPB4OFFCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	R		Reserved
9 - 0	OFFCAL	R/W	0h	ADC Post Processing Block 4 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register. 000h No change. The ADC output is stored directly into ADCRESULT. 001h ADC output - 1 is stored into ADCRESULT. 002h ADC output - 2 is stored into ADCRESULT. ... 200h ADC output + 512 is stored into ADCRESULT. ... 3FFh ADC output + 1 is stored into ADCRESULT. NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register. In 12-bit mode, the subtraction will saturate at 0000h and 0FFFh before being stored into the ADCRESULT register.

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3.2.64 CONTROLSS_ADCn_CFG_ADCPPB4OFFREF Registers

3.2.64.1 ADCn_CFG_ADCPPB4OFFREF Register (Offset = B6h) [reset = h]

Short Description: ADC PPB4 Offset Reference Register

Long Description:

Return to Summary Table

Table 3-127. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00B6h
CONTROLSS_ADC1_CFG	502C 10B6h
CONTROLSS_ADC2_CFG	502C 20B6h
CONTROLSS_ADC3_CFG	502C 30B6h
CONTROLSS_ADC4_CFG	502C 40B6h

Figure 3-63. ADCPPB4OFFREF Name Register

15	14	13	12	11	10	9	8
OFFREF							
R/W							
0							
7	6	5	4	3	2	1	0
OFFREF							
R/W							
0							

Access Types Legend

Table 3-128. ADCPPB4OFFREF Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	OFFREF	R/W	0h	ADC Post Processing Block 4 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB4RESULT register. This subtraction is not saturated. 0000h No change. The ADCRESULT value is passed on. 0001h ADCRESULT - 1 is passed on. 0002h ADCRESULT - 2 is passed on. ... 8000h ADCRESULT - 32,768 is passed on. ... FFFFh ADCRESULT - 65,535 is passed on. NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.

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3.2.65 CONTROLSS_ADCn_CFG_ADCPPB4TRIPHI Registers

3.2.65.1 ADCn_CFG_ADCPPB4TRIPHI Register (Offset = B8h) [reset = h]

Short Description: ADC PPB4 Trip High Register

Long Description:

Return to Summary Table

Table 3-129. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00B8h
CONTROLSS_ADC1_CFG	502C 10B8h
CONTROLSS_ADC2_CFG	502C 20B8h
CONTROLSS_ADC3_CFG	502C 30B8h
CONTROLSS_ADC4_CFG	502C 40B8h

Figure 3-64. ADCPPB4TRIPHI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															HSIGN
R															R/W
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITHI															
R/W															
0															

Access Types Legend

Table 3-130. ADCPPB4TRIPHI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RESERVED	R		Reserved
16	HSIGN	R/W	0h	High Limit Sign Bit. This is the sign bit (17th bit) to the LIMITHI bit field when in 16-bit ADC mode.
15 - 0	LIMITHI	R/W	0h	ADC Post Processing Block 4 Trip High Limit. This value sets the digital comparator trip high limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB4RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRESULT bit field of the ADCPPB4RESULT register.

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3.2.66 CONTROLSS_ADCn_CFG_ADCPPB4TRIPLO Registers

3.2.66.1 ADCn_CFG_ADCPPB4TRIPLO Register (Offset = BCh) [reset = h]

Short Description: ADC PPB4 Trip Low/Trigger Time Stamp Register

Long Description:

Return to Summary Table

Table 3-131. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00BCh
CONTROLSS_ADC1_CFG	502C 10BCh
CONTROLSS_ADC2_CFG	502C 20BCh
CONTROLSS_ADC3_CFG	502C 30BCh
CONTROLSS_ADC4_CFG	502C 40BCh

Figure 3-65. ADCPPB4TRIPLO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REQSTAMP												RESERVED			LSIGN
R												R			R/W
0												0			0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIMITLO															
R/W															
0															

Access Types Legend

Table 3-132. ADCPPB4TRIPLO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	REQSTAMP	R	0h	ADC Post Processing Block 4 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.
19 - 17	RESERVED	R		Reserved
16	LSIGN	R/W	0h	Low Limit Sign Bit. This is the sign bit (17th bit) to the LIMITLO bit field when in 16-bit ADC mode.
15 - 0	LIMITLO	R/W	0h	ADC Post Processing Block 4 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB4RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB4RESULT register.

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3.2.67 CONTROLSS_ADCn_CFG_ADCINTCYCLE Registers

3.2.67.1 ADCn_CFG_ADCINTCYCLE Register (Offset = DEh) [reset = h]

Short Description: ADC Early Interrupt Generation Cycle

Long Description:

Return to Summary Table

Table 3-133. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00DEh
CONTROLSS_ADC1_CFG	502C 10DEh
CONTROLSS_ADC2_CFG	502C 20DEh
CONTROLSS_ADC3_CFG	502C 30DEh
CONTROLSS_ADC4_CFG	502C 40DEh

Figure 3-66. ADCINTCYCLE Name Register

15	14	13	12	11	10	9	8
DELAY							
R/W							
0							
7	6	5	4	3	2	1	0
DELAY							
R/W							
0							

Access Types Legend

Table 3-134. ADCINTCYCLE Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	DELAY	R/W	0h	ADC Early Interrupt Generation Cycle Delay: Defines the delay from the fall edge of ADCSOC in terms of system clock cycles, for the interrupt to be generated.

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3.2.68 CONTROLSS_ADCn_CFG_ADCINLTRIM1 Registers

3.2.68.1 ADCn_CFG_ADCINLTRIM1 Register (Offset = E0h) [reset = h]

Short Description: ADC Linearity Trim 1 Register

Long Description:

Return to Summary Table

Table 3-135. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00E0h
CONTROLSS_ADC1_CFG	502C 10E0h
CONTROLSS_ADC2_CFG	502C 20E0h
CONTROLSS_ADC3_CFG	502C 30E0h
CONTROLSS_ADC4_CFG	502C 40E0h

Figure 3-67. ADCINLTRIM1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM31TO0															
R/W															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM31TO0															
R/W															
11000000111111111101110															

Access Types Legend

Table 3-136. ADCINLTRIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM31TO0	R/W	C0FFEEh	ADC Linearity Trim Bits 31-0. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of data sheet specifications.

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3.2.69 CONTROLSS_ADCn_CFG_ADCINLTRIM2 Registers

3.2.69.1 ADCn_CFG_ADCINLTRIM2 Register (Offset = E4h) [reset = h]

Short Description: ADC Linearity Trim 2 Register

Long Description:

Return to Summary Table

Table 3-137. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00E4h
CONTROLSS_ADC1_CFG	502C 10E4h
CONTROLSS_ADC2_CFG	502C 20E4h
CONTROLSS_ADC3_CFG	502C 30E4h
CONTROLSS_ADC4_CFG	502C 40E4h

Figure 3-68. ADCINLTRIM2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM63TO32															
R/W															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM63TO32															
R/W															
11000000111111111101110															

Access Types Legend

Table 3-138. ADCINLTRIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM63TO32	R/W	C0FFEEh	ADC Linearity Trim Bits 63-32. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of datasheet specifications.

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3.2.70 CONTROLSS_ADCn_CFG_ADCINLTRIM3 Registers

3.2.70.1 ADCn_CFG_ADCINLTRIM3 Register (Offset = E8h) [reset = h]

Short Description: ADC Linearity Trim 3 Register

Long Description:

Return to Summary Table

Table 3-139. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00E8h
CONTROLSS_ADC1_CFG	502C 10E8h
CONTROLSS_ADC2_CFG	502C 20E8h
CONTROLSS_ADC3_CFG	502C 30E8h
CONTROLSS_ADC4_CFG	502C 40E8h

Figure 3-69. ADCINLTRIM3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM95TO64															
R/W															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM95TO64															
R/W															
11000000111111111101110															

Access Types Legend

Table 3-140. ADCINLTRIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM95TO64	R/W	C0FFEEh	ADC Linearity Trim Bits 95-64. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of data sheet specifications.

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3.2.71 CONTROLSS_ADCn_CFG_ADCINLTRIM4 Registers

3.2.71.1 ADCn_CFG_ADCINLTRIM4 Register (Offset = ECh) [reset = h]

Short Description: ADC Linearity Trim 4 Register

Long Description:

Return to Summary Table

Table 3-141. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00ECh
CONTROLSS_ADC1_CFG	502C 10ECh
CONTROLSS_ADC2_CFG	502C 20ECh
CONTROLSS_ADC3_CFG	502C 30ECh
CONTROLSS_ADC4_CFG	502C 40ECh

Figure 3-70. ADCINLTRIM4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM127TO96															
R/W															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM127TO96															
R/W															
11000000111111111101110															

Access Types Legend

Table 3-142. ADCINLTRIM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM127TO96	R/W	C0FFEEh	ADC Linearity Trim Bits 127-96. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of data sheet specifications.

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3.2.72 CONTROLSS_ADCn_CFG_ADCINLTRIM5 Registers

3.2.72.1 ADCn_CFG_ADCINLTRIM5 Register (Offset = F0h) [reset = h]

Short Description: ADC Linearity Trim 5 Register

Long Description:

Return to Summary Table

Table 3-143. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00F0h
CONTROLSS_ADC1_CFG	502C 10F0h
CONTROLSS_ADC2_CFG	502C 20F0h
CONTROLSS_ADC3_CFG	502C 30F0h
CONTROLSS_ADC4_CFG	502C 40F0h

Figure 3-71. ADCINLTRIM5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM159TO128															
R/W															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM159TO128															
R/W															
11000000111111111101110															

Access Types Legend

Table 3-144. ADCINLTRIM5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM159TO128	R/W	C0FFEEh	ADC Linearity Trim Bits 159-128. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of data sheet specifications.

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3.2.73 CONTROLSS_ADCn_CFG_ADCINLTRIM6 Registers

3.2.73.1 ADCn_CFG_ADCINLTRIM6 Register (Offset = F4h) [reset = h]

Short Description: ADC Linearity Trim 6 Register

Long Description:

Return to Summary Table

Table 3-145. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00F4h
CONTROLSS_ADC1_CFG	502C 10F4h
CONTROLSS_ADC2_CFG	502C 20F4h
CONTROLSS_ADC3_CFG	502C 30F4h
CONTROLSS_ADC4_CFG	502C 40F4h

Figure 3-72. ADCINLTRIM6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INLTRIM191TO160															
R/W															
11000000111111111101110															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INLTRIM191TO160															
R/W															
11000000111111111101110															

Access Types Legend

Table 3-146. ADCINLTRIM6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INLTRIM191TO160	R/W	C0FFEEh	ADC Linearity Trim Bits 191-160. This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of data sheet specifications.

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3.2.74 CONTROLSS_ADCn_CFG_ADCINLTRIMCTL Registers

3.2.74.1 ADCn_CFG_ADCINLTRIMCTL Register (Offset = FCh) [reset = h]

Short Description: ADC Linearity Trim Control Register

Long Description:

Return to Summary Table

Table 3-147. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_CFG	502C 00FCh
CONTROLSS_ADC1_CFG	502C 10FCh
CONTROLSS_ADC2_CFG	502C 20FCh
CONTROLSS_ADC3_CFG	502C 30FCh
CONTROLSS_ADC4_CFG	502C 40FCh

Figure 3-73. ADCINLTRIMCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
KEY															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										CALIBSTEP					CALIB MODE
R										R/W					R/W
0										0					0

Access Types Legend

Table 3-148. ADCINLTRIMCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	KEY	R/W	0h	ADC Linearity Trim Control Write Key. Any write to this register must contain the value 0xA5A5 in these bit locations. If a write request attempts to load any other value into these bits, the write for the entire register is ignored. These bits always read back a zero.
15 - 6	RESERVED	R		Reserved
5 - 1	CALIBSTEP	R/W	0h	ADC Linearity Calibration Step. Defines which of the 24 steps of calibration is to be executed. Never set this bit field while the ADC SELFTRIM is in progress. The R-M-W operation could unintentionally set the CALIBMODE bit again.
0	CALIBMODE	R/W	0h	ADC Linearity Calibration Mode.

3.2.75 Access Table

Table 3-149. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
R-0/W	R-0/W	Read returns 0s/Write

3.3 ADC_RESULT_REGS Registers

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Table 3-150. CONTROLSS_ADC[0:2]_RESULT Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_ADC0_RESULT Physical Address	CONTROLSS_ADC1_RESULT Physical Address	CONTROLSS_ADC2_RESULT Physical Address
0h	16	ADC_RESULT_REGS_ADCRESULT0	5010 0000h	5010 1000h	5010 2000h
2h	16	ADC_RESULT_REGS_ADCRESULT1	5010 0002h	5010 1002h	5010 2002h
4h	16	ADC_RESULT_REGS_ADCRESULT2	5010 0004h	5010 1004h	5010 2004h
6h	16	ADC_RESULT_REGS_ADCRESULT3	5010 0006h	5010 1006h	5010 2006h
8h	16	ADC_RESULT_REGS_ADCRESULT4	5010 0008h	5010 1008h	5010 2008h
Ah	16	ADC_RESULT_REGS_ADCRESULT5	5010 000Ah	5010 100Ah	5010 200Ah
Ch	16	ADC_RESULT_REGS_ADCRESULT6	5010 000Ch	5010 100Ch	5010 200Ch
Eh	16	ADC_RESULT_REGS_ADCRESULT7	5010 000Eh	5010 100Eh	5010 200Eh
10h	16	ADC_RESULT_REGS_ADCRESULT8	5010 0010h	5010 1010h	5010 2010h
12h	16	ADC_RESULT_REGS_ADCRESULT9	5010 0012h	5010 1012h	5010 2012h
14h	16	ADC_RESULT_REGS_ADCRESULT10	5010 0014h	5010 1014h	5010 2014h
16h	16	ADC_RESULT_REGS_ADCRESULT11	5010 0016h	5010 1016h	5010 2016h
18h	16	ADC_RESULT_REGS_ADCRESULT12	5010 0018h	5010 1018h	5010 2018h
1Ah	16	ADC_RESULT_REGS_ADCRESULT13	5010 001Ah	5010 101Ah	5010 201Ah
1Ch	16	ADC_RESULT_REGS_ADCRESULT14	5010 001Ch	5010 101Ch	5010 201Ch
1Eh	16	ADC_RESULT_REGS_ADCRESULT15	5010 001Eh	5010 101Eh	5010 201Eh
20h	32	ADC_RESULT_REGS_ADCPPB1RESULT	5010 0020h	5010 1020h	5010 2020h
24h	32	ADC_RESULT_REGS_ADCPPB2RESULT	5010 0024h	5010 1024h	5010 2024h
28h	32	ADC_RESULT_REGS_ADCPPB3RESULT	5010 0028h	5010 1028h	5010 2028h
2Ch	32	ADC_RESULT_REGS_ADCPPB4RESULT	5010 002Ch	5010 102Ch	5010 202Ch

Table 3-151. CONTROLSS_ADC[3:4]_RESULT Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_ADC3_RESULT Physical Address	CONTROLSS_ADC4_RESULT Physical Address
0h	16	ADC_RESULT_REGS_ADCRESULT0	5010 3000h	5010 4000h
2h	16	ADC_RESULT_REGS_ADCRESULT1	5010 3002h	5010 4002h
4h	16	ADC_RESULT_REGS_ADCRESULT2	5010 3004h	5010 4004h
6h	16	ADC_RESULT_REGS_ADCRESULT3	5010 3006h	5010 4006h
8h	16	ADC_RESULT_REGS_ADCRESULT4	5010 3008h	5010 4008h
Ah	16	ADC_RESULT_REGS_ADCRESULT5	5010 300Ah	5010 400Ah
Ch	16	ADC_RESULT_REGS_ADCRESULT6	5010 300Ch	5010 400Ch
Eh	16	ADC_RESULT_REGS_ADCRESULT7	5010 300Eh	5010 400Eh

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Table 3-151. CONTROLSS_ADC[3:4]_RESULT Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_ADC3_RESULT Physical Address	CONTROLSS_ADC4_RESULT Physical Address
10h	16	ADC_RESULT_REGS_ADCRESULT8	5010 3010h	5010 4010h
12h	16	ADC_RESULT_REGS_ADCRESULT9	5010 3012h	5010 4012h
14h	16	ADC_RESULT_REGS_ADCRESULT10	5010 3014h	5010 4014h
16h	16	ADC_RESULT_REGS_ADCRESULT11	5010 3016h	5010 4016h
18h	16	ADC_RESULT_REGS_ADCRESULT12	5010 3018h	5010 4018h
1Ah	16	ADC_RESULT_REGS_ADCRESULT13	5010 301Ah	5010 401Ah
1Ch	16	ADC_RESULT_REGS_ADCRESULT14	5010 301Ch	5010 401Ch
1Eh	16	ADC_RESULT_REGS_ADCRESULT15	5010 301Eh	5010 401Eh
20h	32	ADC_RESULT_REGS_ADCPPB1RESULT	5010 3020h	5010 4020h
24h	32	ADC_RESULT_REGS_ADCPPB2RESULT	5010 3024h	5010 4024h
28h	32	ADC_RESULT_REGS_ADCPPB3RESULT	5010 3028h	5010 4028h
2Ch	32	ADC_RESULT_REGS_ADCPPB4RESULT	5010 302Ch	5010 402Ch

3.3.1 ADC_RESULT_REGS Instance Count Note

Note

n = 0 to 4 for the ADC_RESULT_REGS registers defined below.

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3.3.2 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT0 Registers

3.3.2.1 ADCn_RESULT_REGS_ADCRESULT0 Register (Offset = 0h)

Short Description: ADC Result 0 Register

Long Description:

Return to Summary Table

Table 3-152. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0000h
CONTROLSS_ADC1_RESULT	5010 1000h
CONTROLSS_ADC2_RESULT	5010 2000h
CONTROLSS_ADC3_RESULT	5010 3000h
CONTROLSS_ADC4_RESULT	5010 4000h

Access Types Legend

Table 3-153. ADCRESULT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 0 - 16-bit ADC result. After the ADC completes a conversion of SOC0, the digital result is placed in this bit field.

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3.3.3 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT1 Registers

3.3.3.1 ADCn_RESULT_REGS_ADCRESULT1 Register (Offset = 2h)

Short Description: ADC Result 1 Register

Long Description:

Return to Summary Table

Table 3-154. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0002h
CONTROLSS_ADC1_RESULT	5010 1002h
CONTROLSS_ADC2_RESULT	5010 2002h
CONTROLSS_ADC3_RESULT	5010 3002h
CONTROLSS_ADC4_RESULT	5010 4002h

Access Types Legend

Table 3-155. ADCRESULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 1 - 16-bit ADC result. After the ADC completes a conversion of SOC1, the digital result is placed in this bit field.

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3.3.4 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT2 Registers

3.3.4.1 ADCn_RESULT_REGS_ADCRESULT2 Register (Offset = 4h)

Short Description: ADC Result 2 Register

Long Description:

Return to Summary Table

Table 3-156. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0004h
CONTROLSS_ADC1_RESULT	5010 1004h
CONTROLSS_ADC2_RESULT	5010 2004h
CONTROLSS_ADC3_RESULT	5010 3004h
CONTROLSS_ADC4_RESULT	5010 4004h

Access Types Legend

Table 3-157. ADCRESULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 2 - 16-bit ADC result. After the ADC completes a conversion of SOC2, the digital result is placed in this bit field.

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3.3.5 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT3 Registers

3.3.5.1 ADCn_RESULT_REGS_ADCRESULT3 Register (Offset = 6h)

Short Description: ADC Result 3 Register

Long Description:

Return to Summary Table

Table 3-158. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0006h
CONTROLSS_ADC1_RESULT	5010 1006h
CONTROLSS_ADC2_RESULT	5010 2006h
CONTROLSS_ADC3_RESULT	5010 3006h
CONTROLSS_ADC4_RESULT	5010 4006h

Access Types Legend

Table 3-159. ADCRESULT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 3 - 16-bit ADC result. After the ADC completes a conversion of SOC3, the digital result is placed in this bit field.

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3.3.6 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT4 Registers

3.3.6.1 ADCn_RESULT_REGS_ADCRESULT4 Register (Offset = 8h)

Short Description: ADC Result 4 Register

Long Description:

Return to Summary Table

Table 3-160. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0008h
CONTROLSS_ADC1_RESULT	5010 1008h
CONTROLSS_ADC2_RESULT	5010 2008h
CONTROLSS_ADC3_RESULT	5010 3008h
CONTROLSS_ADC4_RESULT	5010 4008h

Access Types Legend

Table 3-161. ADCRESULT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 4 - 16-bit ADC result. After the ADC completes a conversion of SOC4, the digital result is placed in this bit field.

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3.3.7 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT5 Registers

3.3.7.1 ADCn_RESULT_REGS_ADCRESULT5 Register (Offset = Ah)

Short Description: ADC Result 5 Register

Long Description:

Return to Summary Table

Table 3-162. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 000Ah
CONTROLSS_ADC1_RESULT	5010 100Ah
CONTROLSS_ADC2_RESULT	5010 200Ah
CONTROLSS_ADC3_RESULT	5010 300Ah
CONTROLSS_ADC4_RESULT	5010 400Ah

Access Types Legend

Table 3-163. ADCRESULT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 5 - 16-bit ADC result. After the ADC completes a conversion of SOC5, the digital result is placed in this bit field.

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3.3.8 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT6 Registers

3.3.8.1 ADCn_RESULT_REGS_ADCRESULT6 Register (Offset = Ch)

Short Description: ADC Result 6 Register

Long Description:

Return to Summary Table

Table 3-164. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 000Ch
CONTROLSS_ADC1_RESULT	5010 100Ch
CONTROLSS_ADC2_RESULT	5010 200Ch
CONTROLSS_ADC3_RESULT	5010 300Ch
CONTROLSS_ADC4_RESULT	5010 400Ch

Access Types Legend

Table 3-165. ADCRESULT6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 6 - 16-bit ADC result. After the ADC completes a conversion of SOC6, the digital result is placed in this bit field.

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3.3.9 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT7 Registers

3.3.9.1 ADCn_RESULT_REGS_ADCRESULT7 Register (Offset = Eh)

Short Description: ADC Result 7 Register

Long Description:

Return to Summary Table

Table 3-166. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 000Eh
CONTROLSS_ADC1_RESULT	5010 100Eh
CONTROLSS_ADC2_RESULT	5010 200Eh
CONTROLSS_ADC3_RESULT	5010 300Eh
CONTROLSS_ADC4_RESULT	5010 400Eh

Access Types Legend

Table 3-167. ADCRESULT7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 7 - 16-bit ADC result. After the ADC completes a conversion of SOC7, the digital result is placed in this bit field.

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3.3.10 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT8 Registers

3.3.10.1 ADCn_RESULT_REGS_ADCRESULT8 Register (Offset = 10h)

Short Description: ADC Result 8 Register

Long Description:

Return to Summary Table

Table 3-168. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0010h
CONTROLSS_ADC1_RESULT	5010 1010h
CONTROLSS_ADC2_RESULT	5010 2010h
CONTROLSS_ADC3_RESULT	5010 3010h
CONTROLSS_ADC4_RESULT	5010 4010h

Access Types Legend

Table 3-169. ADCRESULT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 8 - 16-bit ADC result. After the ADC completes a conversion of SOC8, the digital result is placed in this bit field.

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3.3.11 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT9 Registers

3.3.11.1 ADCn_RESULT_REGS_ADCRESULT9 Register (Offset = 12h)

Short Description: ADC Result 9 Register

Long Description:

Return to Summary Table

Table 3-170. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0012h
CONTROLSS_ADC1_RESULT	5010 1012h
CONTROLSS_ADC2_RESULT	5010 2012h
CONTROLSS_ADC3_RESULT	5010 3012h
CONTROLSS_ADC4_RESULT	5010 4012h

Access Types Legend

Table 3-171. ADCRESULT9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 9 - 16-bit ADC result. After the ADC completes a conversion of SOC9, the digital result is placed in this bit field.

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3.3.12 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT10 Registers

3.3.12.1 ADCn_RESULT_REGS_ADCRESULT10 Register (Offset = 14h)

Short Description: ADC Result 10 Register

Long Description:

Return to Summary Table

Table 3-172. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0014h
CONTROLSS_ADC1_RESULT	5010 1014h
CONTROLSS_ADC2_RESULT	5010 2014h
CONTROLSS_ADC3_RESULT	5010 3014h
CONTROLSS_ADC4_RESULT	5010 4014h

Access Types Legend

Table 3-173. ADCRESULT10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 10 - 16-bit ADC result. After the ADC completes a conversion of SOC10, the digital result is placed in this bit field.

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3.3.13 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT11 Registers

3.3.13.1 ADCn_RESULT_REGS_ADCRESULT11 Register (Offset = 16h)

Short Description: ADC Result 11 Register

Long Description:

Return to Summary Table

Table 3-174. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0016h
CONTROLSS_ADC1_RESULT	5010 1016h
CONTROLSS_ADC2_RESULT	5010 2016h
CONTROLSS_ADC3_RESULT	5010 3016h
CONTROLSS_ADC4_RESULT	5010 4016h

Access Types Legend

Table 3-175. ADCRESULT11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 11 - 16-bit ADC result. After the ADC completes a conversion of SOC11, the digital result is placed in this bit field.

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3.3.14 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT12 Registers

3.3.14.1 ADCn_RESULT_REGS_ADCRESULT12 Register (Offset = 18h)

Short Description: ADC Result 12 Register

Long Description:

Return to Summary Table

Table 3-176. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0018h
CONTROLSS_ADC1_RESULT	5010 1018h
CONTROLSS_ADC2_RESULT	5010 2018h
CONTROLSS_ADC3_RESULT	5010 3018h
CONTROLSS_ADC4_RESULT	5010 4018h

Access Types Legend

Table 3-177. ADCRESULT12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 12 - 16-bit ADC result. After the ADC completes a conversion of SOC12, the digital result is placed in this bit field.

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3.3.15 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT13 Registers

3.3.15.1 ADCn_RESULT_REGS_ADCRESULT13 Register (Offset = 1Ah)

Short Description: ADC Result 13 Register

Long Description:

Return to Summary Table

Table 3-178. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 001Ah
CONTROLSS_ADC1_RESULT	5010 101Ah
CONTROLSS_ADC2_RESULT	5010 201Ah
CONTROLSS_ADC3_RESULT	5010 301Ah
CONTROLSS_ADC4_RESULT	5010 401Ah

Access Types Legend

Table 3-179. ADCRESULT13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 13 - 16-bit ADC result. After the ADC completes a conversion of SOC13, the digital result is placed in this bit field.

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3.3.16 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT14 Registers

3.3.16.1 ADCn_RESULT_REGS_ADCRESULT14 Register (Offset = 1Ch)

Short Description: ADC Result 14 Register

Long Description:

Return to Summary Table

Table 3-180. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 001Ch
CONTROLSS_ADC1_RESULT	5010 101Ch
CONTROLSS_ADC2_RESULT	5010 201Ch
CONTROLSS_ADC3_RESULT	5010 301Ch
CONTROLSS_ADC4_RESULT	5010 401Ch

Access Types Legend

Table 3-181. ADCRESULT14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 14 - 16-bit ADC result. After the ADC completes a conversion of SOC14, the digital result is placed in this bit field.

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3.3.17 CONTROLSS_ADCn_RESULT_REGS_ADCRESULT15 Registers

3.3.17.1 ADCn_RESULT_REGS_ADCRESULT15 Register (Offset = 1Eh)

Short Description: ADC Result 15 Register

Long Description:

Return to Summary Table

Table 3-182. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 001Eh
CONTROLSS_ADC1_RESULT	5010 101Eh
CONTROLSS_ADC2_RESULT	5010 201Eh
CONTROLSS_ADC3_RESULT	5010 301Eh
CONTROLSS_ADC4_RESULT	5010 401Eh

Access Types Legend

Table 3-183. ADCRESULT15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RESULT	R	0h	ADC Result 15 - 16-bit ADC result. After the ADC completes a conversion of SOC15, the digital result is placed in this bit field.

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3.3.18 CONTROLSS_ADCn_RESULT_REGS_ADCPPB1RESULT Registers

3.3.18.1 ADCn_RESULT_REGS_ADCPPB1RESULT Register (Offset = 20h)

Short Description: ADC Post Processing Block 1 Result Register

Long Description:

Return to Summary Table

Table 3-184. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0020h
CONTROLSS_ADC1_RESULT	5010 1020h
CONTROLSS_ADC2_RESULT	5010 2020h
CONTROLSS_ADC3_RESULT	5010 3020h
CONTROLSS_ADC4_RESULT	5010 4020h

Access Types Legend

Table 3-185. ADCPPB1RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. - NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	R	0h	ADC Post Processing Block Result 1 - The result of the offset/ reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to verify that post conversion processing is populated in this register. - NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

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3.3.19 CONTROLSS_ADCn_RESULT_REGS_ADCPPB2RESULT Registers

3.3.19.1 ADCn_RESULT_REGS_ADCPPB2RESULT Register (Offset = 24h)

Short Description: ADC Post Processing Block 2 Result Register

Long Description:

Return to Summary Table

Table 3-186. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0024h
CONTROLSS_ADC1_RESULT	5010 1024h
CONTROLSS_ADC2_RESULT	5010 2024h
CONTROLSS_ADC3_RESULT	5010 3024h
CONTROLSS_ADC4_RESULT	5010 4024h

Access Types Legend

Table 3-187. ADCPPB2RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. - NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	R	0h	ADC Post Processing Block Result 2 - The result of the offset/ reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to verify that post conversion processing is populated in this register. - NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

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3.3.20 CONTROLSS_ADCn_RESULT_REGS_ADCPPB3RESULT Registers

3.3.20.1 ADCn_RESULT_REGS_ADCPPB3RESULT Register (Offset = 28h)

Short Description: ADC Post Processing Block 3 Result Register

Long Description:

Return to Summary Table

Table 3-188. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 0028h
CONTROLSS_ADC1_RESULT	5010 1028h
CONTROLSS_ADC2_RESULT	5010 2028h
CONTROLSS_ADC3_RESULT	5010 3028h
CONTROLSS_ADC4_RESULT	5010 4028h

Access Types Legend

Table 3-189. ADCPPB3RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. - NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	R	0h	ADC Post Processing Block Result 3 - The result of the offset/ reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to verify that post conversion processing is populated in this register. - NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

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3.3.21 CONTROLSS_ADCn_RESULT_REGS_ADCPPB4RESULT Registers

3.3.21.1 ADCn_RESULT_REGS_ADCPPB4RESULT Register (Offset = 2Ch)

Short Description: ADC Post Processing Block 4 Result Register

Long Description:

Return to Summary Table

Table 3-190. Instance Table

Instance Name	Physical Address
CONTROLSS_ADC0_RESULT	5010 002Ch
CONTROLSS_ADC1_RESULT	5010 102Ch
CONTROLSS_ADC2_RESULT	5010 202Ch
CONTROLSS_ADC3_RESULT	5010 302Ch
CONTROLSS_ADC4_RESULT	5010 402Ch

Access Types Legend

Table 3-191. ADCPPB4RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SIGN	R	0h	Sign Extended Bits. These bits reflect the same value as bit 16. - NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12.
15 - 0	PPBRESULT	R	0h	ADC Post Processing Block Result 4 - The result of the offset/ reference subtraction post conversion processing is stored in this register. If ADCINTFLG is polled in reading PPBRESULT, user needs to add a NOP instruction to verify that post conversion processing is populated in this register. - NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.

3.3.22 Access Table

Table 3-192. Access Type Codes

Access Type	Code	Description
R	R	Read

3.4 CMPSSA Registers

Table 3-193. CONTROLSS_CMPSSA[0:2] Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_CMPSSA0 Physical Address	CONTROLSS_CMPSSA1 Physical Address	CONTROLSS_CMPSSA2 Physical Address
0h	16	CMPSSA_COMPCTL	5020 0000h	5020 1000h	5020 2000h
4h	16	CMPSSA_COMPSTS	5020 0004h	5020 1004h	5020 2004h
6h	16	CMPSSA_COMPSTSCLR	5020 0006h	5020 1006h	5020 2006h
8h	16	CMPSSA_COMPDACCTL	5020 0008h	5020 1008h	5020 2008h
Ah	16	CMPSSA_COMPDACCTL2	5020 000Ah	5020 100Ah	5020 200Ah
Ch	16	CMPSSA_DACHVALS	5020 000Ch	5020 100Ch	5020 200Ch
Eh	16	CMPSSA_DACHVALA	5020 000Eh	5020 100Eh	5020 200Eh
10h	16	CMPSSA_RAMPMAXREFA	5020 0010h	5020 1010h	5020 2010h
14h	16	CMPSSA_RAMPMAXREFS	5020 0014h	5020 1014h	5020 2014h
18h	16	CMPSSA_RAMPDECVALA	5020 0018h	5020 1018h	5020 2018h
1Ch	16	CMPSSA_RAMPDECVALS	5020 001Ch	5020 101Ch	5020 201Ch
20h	16	CMPSSA_RAMPSTS	5020 0020h	5020 1020h	5020 2020h

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Table 3-193. CONTROLSS_CMPSSA[0:2] Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_CMPSSA0 Physical Address	CONTROLSS_CMPSSA1 Physical Address	CONTROLSS_CMPSSA2 Physical Address
24h	16	CMPSSA_DACLVALS	5020 0024h	5020 1024h	5020 2024h
26h	16	CMPSSA_DACLVALA	5020 0026h	5020 1026h	5020 2026h
28h	16	CMPSSA_RAMPDLYA	5020 0028h	5020 1028h	5020 2028h
2Ah	16	CMPSSA_RAMPDLYS	5020 002Ah	5020 102Ah	5020 202Ah
2Ch	16	CMPSSA_CTRIPLFILCTL	5020 002Ch	5020 102Ch	5020 202Ch
2Eh	16	CMPSSA_CTRIPLFILCLKCTL	5020 002Eh	5020 102Eh	5020 202Eh
30h	16	CMPSSA_CTRIPHFILCTL	5020 0030h	5020 1030h	5020 2030h
32h	16	CMPSSA_CTRIPHFILCLKCTL	5020 0032h	5020 1032h	5020 2032h
34h	16	CMPSSA_COMPLOCK	5020 0034h	5020 1034h	5020 2034h
38h	16	CMPSSA_DACHVALS2	5020 0038h	5020 1038h	5020 2038h
3Ah	16	CMPSSA_DACLVALS2	5020 003Ah	5020 103Ah	5020 203Ah
3Ch	16	CMPSSA_CONFIG1	5020 003Ch	5020 103Ch	5020 203Ch

Table 3-194. CONTROLSS_CMPSSA[3:5] Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_CMPSSA3 Physical Address	CONTROLSS_CMPSSA4 Physical Address	CONTROLSS_CMPSSA5 Physical Address
0h	16	CMPSSA_COMPCTL	5020 3000h	5020 4000h	5020 5000h
4h	16	CMPSSA_COMPSTS	5020 3004h	5020 4004h	5020 5004h
6h	16	CMPSSA_COMPSTSCLR	5020 3006h	5020 4006h	5020 5006h
8h	16	CMPSSA_COMPDACCTL	5020 3008h	5020 4008h	5020 5008h
Ah	16	CMPSSA_COMPDACCTL2	5020 300Ah	5020 400Ah	5020 500Ah
Ch	16	CMPSSA_DACHVALS	5020 300Ch	5020 400Ch	5020 500Ch
Eh	16	CMPSSA_DACHVALA	5020 300Eh	5020 400Eh	5020 500Eh
10h	16	CMPSSA_RAMPMAXREFA	5020 3010h	5020 4010h	5020 5010h
14h	16	CMPSSA_RAMPMAXREFS	5020 3014h	5020 4014h	5020 5014h
18h	16	CMPSSA_RAMPDECVALA	5020 3018h	5020 4018h	5020 5018h
1Ch	16	CMPSSA_RAMPDECVALS	5020 301Ch	5020 401Ch	5020 501Ch
20h	16	CMPSSA_RAMPSTS	5020 3020h	5020 4020h	5020 5020h
24h	16	CMPSSA_DACLVALS	5020 3024h	5020 4024h	5020 5024h
26h	16	CMPSSA_DACLVALA	5020 3026h	5020 4026h	5020 5026h
28h	16	CMPSSA_RAMPDLYA	5020 3028h	5020 4028h	5020 5028h
2Ah	16	CMPSSA_RAMPDLYS	5020 302Ah	5020 402Ah	5020 502Ah
2Ch	16	CMPSSA_CTRIPLFILCTL	5020 302Ch	5020 402Ch	5020 502Ch
2Eh	16	CMPSSA_CTRIPLFILCLKCTL	5020 302Eh	5020 402Eh	5020 502Eh
30h	16	CMPSSA_CTRIPHFILCTL	5020 3030h	5020 4030h	5020 5030h
32h	16	CMPSSA_CTRIPHFILCLKCTL	5020 3032h	5020 4032h	5020 5032h
34h	16	CMPSSA_COMPLOCK	5020 3034h	5020 4034h	5020 5034h
38h	16	CMPSSA_DACHVALS2	5020 3038h	5020 4038h	5020 5038h
3Ah	16	CMPSSA_DACLVALS2	5020 303Ah	5020 403Ah	5020 503Ah
3Ch	16	CMPSSA_CONFIG1	5020 303Ch	5020 403Ch	5020 503Ch

Table 3-195. CONTROLSS_CMPSSA[6:8] Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_CMPSSA6 Physical Address	CONTROLSS_CMPSSA7 Physical Address	CONTROLSS_CMPSSA8 Physical Address
0h	16	CMPSSA_COMPCTL	5020 6000h	5020 7000h	5020 8000h
4h	16	CMPSSA_COMPSTS	5020 6004h	5020 7004h	5020 8004h

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Table 3-195. CONTROLSS_CMPSSA[6:8] Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_CMPSSA6 Physical Address	CONTROLSS_CMPSSA7 Physical Address	CONTROLSS_CMPSSA8 Physical Address
6h	16	CMPSSA_COMPSTSCLR	5020 6006h	5020 7006h	5020 8006h
8h	16	CMPSSA_COMPDACCTL	5020 6008h	5020 7008h	5020 8008h
Ah	16	CMPSSA_COMPDACCTL2	5020 600Ah	5020 700Ah	5020 800Ah
Ch	16	CMPSSA_DACHVALS	5020 600Ch	5020 700Ch	5020 800Ch
Eh	16	CMPSSA_DACHVALA	5020 600Eh	5020 700Eh	5020 800Eh
10h	16	CMPSSA_RAMPMAXREFA	5020 6010h	5020 7010h	5020 8010h
14h	16	CMPSSA_RAMPMAXREFS	5020 6014h	5020 7014h	5020 8014h
18h	16	CMPSSA_RAMPDECVALA	5020 6018h	5020 7018h	5020 8018h
1Ch	16	CMPSSA_RAMPDECVALS	5020 601Ch	5020 701Ch	5020 801Ch
20h	16	CMPSSA_RAMPSTS	5020 6020h	5020 7020h	5020 8020h
24h	16	CMPSSA_DACLVALS	5020 6024h	5020 7024h	5020 8024h
26h	16	CMPSSA_DACLVALA	5020 6026h	5020 7026h	5020 8026h
28h	16	CMPSSA_RAMPDLYA	5020 6028h	5020 7028h	5020 8028h
2Ah	16	CMPSSA_RAMPDLYS	5020 602Ah	5020 702Ah	5020 802Ah
2Ch	16	CMPSSA_CTRIPLFILCTL	5020 602Ch	5020 702Ch	5020 802Ch
2Eh	16	CMPSSA_CTRIPLFILCLKCTL	5020 602Eh	5020 702Eh	5020 802Eh
30h	16	CMPSSA_CTRIPHFILCTL	5020 6030h	5020 7030h	5020 8030h
32h	16	CMPSSA_CTRIPHFILCLKCTL	5020 6032h	5020 7032h	5020 8032h
34h	16	CMPSSA_COMPLOCK	5020 6034h	5020 7034h	5020 8034h
38h	16	CMPSSA_DACHVALS2	5020 6038h	5020 7038h	5020 8038h
3Ah	16	CMPSSA_DACLVALS2	5020 603Ah	5020 703Ah	5020 803Ah
3Ch	16	CMPSSA_CONFIG1	5020 603Ch	5020 703Ch	5020 803Ch

Table 3-196. CONTROLSS_CMPSSA9 Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_CMPSSA9 Physical Address
0h	16	CMPSSA_COMPCTL	5020 9000h
4h	16	CMPSSA_COMPSTS	5020 9004h
6h	16	CMPSSA_COMPSTSCLR	5020 9006h
8h	16	CMPSSA_COMPDACCTL	5020 9008h
Ah	16	CMPSSA_COMPDACCTL2	5020 900Ah
Ch	16	CMPSSA_DACHVALS	5020 900Ch
Eh	16	CMPSSA_DACHVALA	5020 900Eh
10h	16	CMPSSA_RAMPMAXREFA	5020 9010h
14h	16	CMPSSA_RAMPMAXREFS	5020 9014h
18h	16	CMPSSA_RAMPDECVALA	5020 9018h
1Ch	16	CMPSSA_RAMPDECVALS	5020 901Ch
20h	16	CMPSSA_RAMPSTS	5020 9020h
24h	16	CMPSSA_DACLVALS	5020 9024h
26h	16	CMPSSA_DACLVALA	5020 9026h
28h	16	CMPSSA_RAMPDLYA	5020 9028h
2Ah	16	CMPSSA_RAMPDLYS	5020 902Ah
2Ch	16	CMPSSA_CTRIPLFILCTL	5020 902Ch
2Eh	16	CMPSSA_CTRIPLFILCLKCTL	5020 902Eh
30h	16	CMPSSA_CTRIPHFILCTL	5020 9030h
32h	16	CMPSSA_CTRIPHFILCLKCTL	5020 9032h
34h	16	CMPSSA_COMPLOCK	5020 9034h

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Table 3-196. CONTROLSS_CMPSSA9 Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_CMPSSA9 Physical Address
38h	16	CMPSSA_DACHVALS2	5020 9038h
3Ah	16	CMPSSA_DACLVALS2	5020 903Ah
3Ch	16	CMPSSA_CONFIG1	5020 903Ch

3.4.1 CMPSSA Instance Count Note

Note

n = 0 to 9 for the CMPSSA registers defined below.

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3.4.2 CONTROLSS_CMPSSAn_COMPCTL Registers

3.4.2.1 CMPSSAn_COMPCTL Register (Offset = 0h) [reset = h]

Short Description: CMPSS Comparator Control Register

Long Description:

Return to Summary Table

Table 3-197. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0000h
CONTROLSS_CMPSSA1	5020 1000h
CONTROLSS_CMPSSA2	5020 2000h
CONTROLSS_CMPSSA3	5020 3000h
CONTROLSS_CMPSSA4	5020 4000h
CONTROLSS_CMPSSA5	5020 5000h
CONTROLSS_CMPSSA6	5020 6000h
CONTROLSS_CMPSSA7	5020 7000h
CONTROLSS_CMPSSA8	5020 8000h
CONTROLSS_CMPSSA9	5020 9000h

Access Types Legend

Table 3-198. COMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	COMPDACE	RW	0h	Comparator/DAC enable. 0 Comparator/DAC disabled 1 Comparator/DAC enabled
14	ASYNCLEN	RW	0h	Low comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPLSEL=3 or CTRIPOUTLSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output
13 - 12	CTRIPOUTLSEL	RW	0h	Low comparator CTRIPOUTL source select. 0 Asynchronous comparator output drives CTRIPOUTL 1 Synchronous comparator output drives CTRIPOUTL 2 Output of digital filter drives CTRIPOUTL 3 Latched output of digital filter drives CTRIPOUTL
11 - 10	CTRIPLSEL	RW	0h	Low comparator CTRIPL source select. 0 Asynchronous comparator output drives CTRIPL 1 Synchronous comparator output drives CTRIPL 2 Output of digital filter drives CTRIPL 3 Latched output of digital filter drives CTRIPL
9	COMPLINV	RW	0h	Low comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted
8	COMPLSOURCE	RW	0h	CompL Pos Mux Select0 positive mux selects INL_3p3v voltage (default)1 postive mux selects INH_3p3v
7	RESERVED	RO		Reserved
6	ASYNCHEN	RW	0h	High comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPHSEL=3 or CTRIPOUTHSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output
5 - 4	CTRIPOUTHSEL	RW	0h	High comparator CTRIPOUTH source select. 0 Asynchronous comparator output drives CTRIPOUTH 1 Synchronous comparator output drives CTRIPOUTH 2 Output of digital filter drives CTRIPOUTH 3 Latched output of digital filter drives CTRIPOUTH

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Table 3-198. COMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 2	CTRIPHSEL	RW	0h	High comparator CTRIPH source select. 0 Asynchronous comparator output drives CTRIPH 1 Synchronous comparator output drives CTRIPH 2 Output of digital filter drives CTRIPH 3 Latched output of digital filter drives CTRIPH
1	COMPHINV	RW	0h	High comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted
0	COMPHSOURCE	RW	0h	CompH neg Mux slect0 negative mux selects DAC voltage (default)1 negative mux selects INL_3p3v

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3.4.3 CONTROLSS_CMPSSAn_COMPSTS Registers

3.4.3.1 CMPSSAn_COMPSTS Register (Offset = 4h) [reset = h]

Short Description: CMPSS Comparator Status Register

Long Description:

Return to Summary Table

Table 3-199. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0004h
CONTROLSS_CMPSSA1	5020 1004h
CONTROLSS_CMPSSA2	5020 2004h
CONTROLSS_CMPSSA3	5020 3004h
CONTROLSS_CMPSSA4	5020 4004h
CONTROLSS_CMPSSA5	5020 5004h
CONTROLSS_CMPSSA6	5020 6004h
CONTROLSS_CMPSSA7	5020 7004h
CONTROLSS_CMPSSA8	5020 8004h
CONTROLSS_CMPSSA9	5020 9004h

Access Types Legend

Table 3-200. COMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9	COMPLLATCH	RO	0h	Latched value of low comparator digital filter output
8	COMPLSTS	RO	0h	Low comparator digital filter output
7 - 2	RESERVED	RO		Reserved
1	COMPHLATCH	RO	0h	Latched value of high comparator digital filter output
0	COMPHSTS	RO	0h	High comparator digital filter output

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3.4.4 CONTROLSS_CMPSSAn_COMPSTSCLR Registers

3.4.4.1 CMPSSAn_COMPSTSCLR Register (Offset = 6h) [reset = h]

Short Description: CMPSS Comparator Status Clear Register

Long Description:

Return to Summary Table

Table 3-201. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0006h
CONTROLSS_CMPSSA1	5020 1006h
CONTROLSS_CMPSSA2	5020 2006h
CONTROLSS_CMPSSA3	5020 3006h
CONTROLSS_CMPSSA4	5020 4006h
CONTROLSS_CMPSSA5	5020 5006h
CONTROLSS_CMPSSA6	5020 6006h
CONTROLSS_CMPSSA7	5020 7006h
CONTROLSS_CMPSSA8	5020 8006h
CONTROLSS_CMPSSA9	5020 9006h

Access Types Legend

Table 3-202. COMPSTSCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO		Reserved
10	LSYNCCLREN	RW	0h	Low comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. 0 EPWMSYNCPER will not reset latch 1 EPWMSYNCPER will reset latch
9	LLATCHCLR	RW RRETURNS 0S	0h	Low comparator latch software clear. Perform software reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPLLATCH]
8 - 3	RESERVED	RO		Reserved
2	HSYNCCLREN	RW	0h	High comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. 0 EPWMSYNCPER will not reset latch 1 EPWMSYNCPER will reset latch
1	HLATCHCLR	RW RRETURNS 0S	0h	High comparator latch software clear. Perform software reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPHLATCH]
0	RESERVED	RO		Reserved

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3.4.5 CONTROLSS_CMPSSAn_COMPDACCTL Registers

3.4.5.1 CMPSSAn_COMPDACCTL Register (Offset = 8h) [reset = h]

Short Description: CMPSS DAC Control Register

Long Description:

Return to Summary Table

Table 3-203. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0008h
CONTROLSS_CMPSSA1	5020 1008h
CONTROLSS_CMPSSA2	5020 2008h
CONTROLSS_CMPSSA3	5020 3008h
CONTROLSS_CMPSSA4	5020 4008h
CONTROLSS_CMPSSA5	5020 5008h
CONTROLSS_CMPSSA6	5020 6008h
CONTROLSS_CMPSSA7	5020 7008h
CONTROLSS_CMPSSA8	5020 8008h
CONTROLSS_CMPSSA9	5020 9008h

Access Types Legend

Table 3-204. COMPDACCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	FREESOFT	RW	0h	Free-run or software-run emulation behavior. Behavior of the ramp generator during emulation suspend. 00b Ramp generator stops immediately during emulation suspend 01b Ramp generator completes current ramp and stops at next EPWMSYNCPER during emulation suspend 1Xb Ramp generator runs freely
13	RESERVED	RO		Reserved
12	BLANKEN	RW	0h	EPWMBLANK enable. This bit enables the EPWMBLANK signal. 0 EPWMBLANK signal is disabled. 1 EPWMBLANK signal is enabled.
11 - 8	BLANKSOURCE	RW	0h	EPWMBLANK source select. This bit field determines which EPWMnBLANK is passed on as the EPWMBLANK signal. Where n represents the maximum number of EPWMBLANK signals available on the device: 0 EPWM1BLANK 1 EPWM2BLANK 2 EPWM3BLANK ... n-1 EPWMnBLANK
7	SWLOADSEL	RW	0h	Software load select. Determines whether DACxVALA is updated from DACxVALS on SYSCLK or EPWMSYNCPER. 0 DACxVALA is updated from DACxVALS on SYSCLK 1 DACxVALA is updated from DACxVALS on EPWMSYNCPER
6	RAMPLOADSEL	RW	0h	Ramp load select. Determines whether RAMPSTS is updated from RAMPMAXREFA or RAMPMAXREFS when COMPSTS[COMPHSTS] is triggered. 0 RAMPSTS is loaded from RAMPMAXREFA 1 RAMPSTS is loaded from RAMPMAXREFS
5	SELREF	RW	0h	CMPSS reference select0 vref_1p8v as reference voltage (default)1 vdd_1p8v as reference voltage
4 - 1	RAMPSOURCE	RW	0h	EPWMSYNCPER source select. Determines which EPWMnSYNCPER signal is used within the CMPSS module. Where n represents the maximum number of EPWMSYNCPER signals available on the device: 0 EPWM1SYNCPER 1 EPWM2SYNCPER 2 EPWM3SYNCPER ... n-1 EPWMnSYNCPER
0	DACSOURCE	RW	0h	DAC source select. Determines whether DACHVALA is updated from DACHVALS or from the ramp generator. 0 DACHVALA is updated from DACHVALS 1 DACHVALA is updated from the ramp generator

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3.4.6 CONTROLSS_CMPSSAn_COMPDACCTL2 Registers

3.4.6.1 CMPSSAn_COMPDACCTL2 Register (Offset = Ah) [reset = h]

Short Description: CMPSS DAC Control Register 2

Long Description:

Return to Summary Table

Table 3-205. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 000Ah
CONTROLSS_CMPSSA1	5020 100Ah
CONTROLSS_CMPSSA2	5020 200Ah
CONTROLSS_CMPSSA3	5020 300Ah
CONTROLSS_CMPSSA4	5020 400Ah
CONTROLSS_CMPSSA5	5020 500Ah
CONTROLSS_CMPSSA6	5020 600Ah
CONTROLSS_CMPSSA7	5020 700Ah
CONTROLSS_CMPSSA8	5020 800Ah
CONTROLSS_CMPSSA9	5020 900Ah

Access Types Legend

Table 3-206. COMPDACCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO		Reserved
10	RAMPSOURCEUSEL	RW	0h	0: Selects EPWM0 to 15 as RAMP source 1: Selects EPWM16 to 31 as RAMP source
9	RESERVED	RO		Reserved
8	BLANKSOURCEUSEL	RW	0h	0: Selects EPWM0 to 15 as blank source 1: Selects EPWM16 to 31 as blank source
7 - 6	RESERVED	RO		Reserved
5 - 1	DEACTIVESEL	RW	0h	DEACTIVE source select: 0x0 : EPWM1.DEACTIVE 0x1 : EPWM2.DEACTIVE 0x2 : EPWM3.DEACTIVE 0x3 : EPWM4.DEACTIVE . . 0x31 : EPWM32.DEACTIVE
0	DEENABLE	RW	0h	DE mode enable. 0 DE mode features disabled. 1 DE mode features enabled.

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3.4.7 CONTROLSS_CMPSSAn_DACHVALS Registers

3.4.7.1 CMPSSAn_DACHVALS Register (Offset = Ch) [reset = h]

Short Description: CMPSS High DAC Value Shadow Register

Long Description:

Return to Summary Table

Table 3-207. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 000Ch
CONTROLSS_CMPSSA1	5020 100Ch
CONTROLSS_CMPSSA2	5020 200Ch
CONTROLSS_CMPSSA3	5020 300Ch
CONTROLSS_CMPSSA4	5020 400Ch
CONTROLSS_CMPSSA5	5020 500Ch
CONTROLSS_CMPSSA6	5020 600Ch
CONTROLSS_CMPSSA7	5020 700Ch
CONTROLSS_CMPSSA8	5020 800Ch
CONTROLSS_CMPSSA9	5020 900Ch

Access Types Legend

Table 3-208. DACHVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RW	0h	High DAC shadow value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS is loaded into DACHVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL].

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3.4.8 CONTROLSS_CMPSSAn_DACHVALA Registers

3.4.8.1 CMPSSAn_DACHVALA Register (Offset = Eh) [reset = h]

Short Description: CMPSS High DAC Value Active Register

Long Description:

Return to Summary Table

Table 3-209. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 000Eh
CONTROLSS_CMPSSA1	5020 100Eh
CONTROLSS_CMPSSA2	5020 200Eh
CONTROLSS_CMPSSA3	5020 300Eh
CONTROLSS_CMPSSA4	5020 400Eh
CONTROLSS_CMPSSA5	5020 500Eh
CONTROLSS_CMPSSA6	5020 600Eh
CONTROLSS_CMPSSA7	5020 700Eh
CONTROLSS_CMPSSA8	5020 800Eh
CONTROLSS_CMPSSA9	5020 900Eh

Access Types Legend

Table 3-210. DACHVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RO	0h	High DAC active value. Value that is actively driven by the high DAC.

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3.4.9 CONTROLSS_CMPSSAn_RAMPMAXREFA Registers

3.4.9.1 CMPSSAn_RAMPMAXREFA Register (Offset = 10h) [reset = h]

Short Description: CMPSS Ramp Max Reference Active Register

Long Description:

Return to Summary Table

Table 3-211. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0010h
CONTROLSS_CMPSSA1	5020 1010h
CONTROLSS_CMPSSA2	5020 2010h
CONTROLSS_CMPSSA3	5020 3010h
CONTROLSS_CMPSSA4	5020 4010h
CONTROLSS_CMPSSA5	5020 5010h
CONTROLSS_CMPSSA6	5020 6010h
CONTROLSS_CMPSSA7	5020 7010h
CONTROLSS_CMPSSA8	5020 8010h
CONTROLSS_CMPSSA9	5020 9010h

Access Types Legend

Table 3-212. RAMPMAXREFA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPMAXREF	RO	0h	Ramp maximum reference active value. Latched value to be loaded into ramp generator RAMPSTS.

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3.4.10 CONTROLSS_CMPSSAn_RAMPMAXREFS Registers

3.4.10.1 CMPSSAn_RAMPMAXREFS Register (Offset = 14h) [reset = h]

Short Description: CMPSS Ramp Max Reference Shadow Register

Long Description:

Return to Summary Table

Table 3-213. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0014h
CONTROLSS_CMPSSA1	5020 1014h
CONTROLSS_CMPSSA2	5020 2014h
CONTROLSS_CMPSSA3	5020 3014h
CONTROLSS_CMPSSA4	5020 4014h
CONTROLSS_CMPSSA5	5020 5014h
CONTROLSS_CMPSSA6	5020 6014h
CONTROLSS_CMPSSA7	5020 7014h
CONTROLSS_CMPSSA8	5020 8014h
CONTROLSS_CMPSSA9	5020 9014h

Access Types Legend

Table 3-214. RAMPMAXREFS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPMAXREF	RW	0h	Ramp maximum reference shadow. Unlatched value to be loaded into ramp generator RAMPSTS.

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3.4.11 CONTROLSS_CMPSSAn_RAMPDECVALA Registers

3.4.11.1 CMPSSAn_RAMPDECVALA Register (Offset = 18h) [reset = h]

Short Description: CMPSS Ramp Decrement Value Active Register

Long Description:

Return to Summary Table

Table 3-215. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0018h
CONTROLSS_CMPSSA1	5020 1018h
CONTROLSS_CMPSSA2	5020 2018h
CONTROLSS_CMPSSA3	5020 3018h
CONTROLSS_CMPSSA4	5020 4018h
CONTROLSS_CMPSSA5	5020 5018h
CONTROLSS_CMPSSA6	5020 6018h
CONTROLSS_CMPSSA7	5020 7018h
CONTROLSS_CMPSSA8	5020 8018h
CONTROLSS_CMPSSA9	5020 9018h

Access Types Legend

Table 3-216. RAMPDECVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPDECVAL	RO	0h	Ramp decrement value active. Latched value that will be subtracted from RAMPSTS.

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3.4.12 CONTROLSS_CMPSSAn_RAMPDECVALS Registers

3.4.12.1 CMPSSAn_RAMPDECVALS Register (Offset = 1Ch) [reset = h]

Short Description: CMPSS Ramp Decrement Value Shadow Register

Long Description:

Return to Summary Table

Table 3-217. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 001Ch
CONTROLSS_CMPSSA1	5020 101Ch
CONTROLSS_CMPSSA2	5020 201Ch
CONTROLSS_CMPSSA3	5020 301Ch
CONTROLSS_CMPSSA4	5020 401Ch
CONTROLSS_CMPSSA5	5020 501Ch
CONTROLSS_CMPSSA6	5020 601Ch
CONTROLSS_CMPSSA7	5020 701Ch
CONTROLSS_CMPSSA8	5020 801Ch
CONTROLSS_CMPSSA9	5020 901Ch

Access Types Legend

Table 3-218. RAMPDECVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPDECVAL	RW	0h	Ramp decrement value shadow. Unlatched value to be loaded into RAMPDECVALA.

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3.4.13 CONTROLSS_CMPSSAn_RAMPSTS Registers

3.4.13.1 CMPSSAn_RAMPSTS Register (Offset = 20h) [reset = h]

Short Description: CMPSS Ramp Status Register

Long Description:

Return to Summary Table

Table 3-219. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0020h
CONTROLSS_CMPSSA1	5020 1020h
CONTROLSS_CMPSSA2	5020 2020h
CONTROLSS_CMPSSA3	5020 3020h
CONTROLSS_CMPSSA4	5020 4020h
CONTROLSS_CMPSSA5	5020 5020h
CONTROLSS_CMPSSA6	5020 6020h
CONTROLSS_CMPSSA7	5020 7020h
CONTROLSS_CMPSSA8	5020 8020h
CONTROLSS_CMPSSA9	5020 9020h

Access Types Legend

Table 3-220. RAMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPVALUE	RO	0h	Ramp value. Present value of ramp generator.

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3.4.14 CONTROLSS_CMPSSAn_DACLVALS Registers

3.4.14.1 CMPSSAn_DACLVALS Register (Offset = 24h) [reset = h]

Short Description: CMPSS Low DAC Value Shadow Register

Long Description:

Return to Summary Table

Table 3-221. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0024h
CONTROLSS_CMPSSA1	5020 1024h
CONTROLSS_CMPSSA2	5020 2024h
CONTROLSS_CMPSSA3	5020 3024h
CONTROLSS_CMPSSA4	5020 4024h
CONTROLSS_CMPSSA5	5020 5024h
CONTROLSS_CMPSSA6	5020 6024h
CONTROLSS_CMPSSA7	5020 7024h
CONTROLSS_CMPSSA8	5020 8024h
CONTROLSS_CMPSSA9	5020 9024h

Access Types Legend

Table 3-222. DACLVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RW	0h	Low DAC shadow value. value to be loaded into DACLVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL].

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3.4.15 CONTROLSS_CMPSSAn_DACLVALA Registers

3.4.15.1 CMPSSAn_DACLVALA Register (Offset = 26h) [reset = h]

Short Description: CMPSS Low DAC Value Active Register

Long Description:

Return to Summary Table

Table 3-223. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0026h
CONTROLSS_CMPSSA1	5020 1026h
CONTROLSS_CMPSSA2	5020 2026h
CONTROLSS_CMPSSA3	5020 3026h
CONTROLSS_CMPSSA4	5020 4026h
CONTROLSS_CMPSSA5	5020 5026h
CONTROLSS_CMPSSA6	5020 6026h
CONTROLSS_CMPSSA7	5020 7026h
CONTROLSS_CMPSSA8	5020 8026h
CONTROLSS_CMPSSA9	5020 9026h

Access Types Legend

Table 3-224. DACLVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RO	0h	Low DAC active value. Value that is actively driven by the low DAC.

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3.4.16 CONTROLSS_CMPSSAn_RAMPDLYA Registers

3.4.16.1 CMPSSAn_RAMPDLYA Register (Offset = 28h) [reset = h]

Short Description: CMPSS Ramp Delay Active Register

Long Description:

Return to Summary Table

Table 3-225. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0028h
CONTROLSS_CMPSSA1	5020 1028h
CONTROLSS_CMPSSA2	5020 2028h
CONTROLSS_CMPSSA3	5020 3028h
CONTROLSS_CMPSSA4	5020 4028h
CONTROLSS_CMPSSA5	5020 5028h
CONTROLSS_CMPSSA6	5020 6028h
CONTROLSS_CMPSSA7	5020 7028h
CONTROLSS_CMPSSA8	5020 8028h
CONTROLSS_CMPSSA9	5020 9028h

Access Types Legend

Table 3-226. RAMPDLYA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12 - 0	DELAY	RO	0h	Ramp delay active value. Latched value of the number of cycles to delay the start of the ramp generator decrementer after a EPWMSYNCPER is received.

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3.4.17 CONTROLSS_CMPSSAn_RAMPDLYS Registers

3.4.17.1 CMPSSAn_RAMPDLYS Register (Offset = 2Ah) [reset = h]

Short Description: CMPSS Ramp Delay Shadow Register

Long Description:

Return to Summary Table

Table 3-227. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 002Ah
CONTROLSS_CMPSSA1	5020 102Ah
CONTROLSS_CMPSSA2	5020 202Ah
CONTROLSS_CMPSSA3	5020 302Ah
CONTROLSS_CMPSSA4	5020 402Ah
CONTROLSS_CMPSSA5	5020 502Ah
CONTROLSS_CMPSSA6	5020 602Ah
CONTROLSS_CMPSSA7	5020 702Ah
CONTROLSS_CMPSSA8	5020 802Ah
CONTROLSS_CMPSSA9	5020 902Ah

Access Types Legend

Table 3-228. RAMPDLYS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12 - 0	DELAY	RW	0h	Ramp delay shadow value. Unlatched value to be loaded into RAMPDLYA.

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3.4.18 CONTROLSS_CMPSSAn_CTRIPLFILCTL Registers

3.4.18.1 CMPSSAn_CTRIPLFILCTL Register (Offset = 2Ch) [reset = h]

Short Description: CTRIPL Filter Control Register

Long Description:

Return to Summary Table

Table 3-229. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 002Ch
CONTROLSS_CMPSSA1	5020 102Ch
CONTROLSS_CMPSSA2	5020 202Ch
CONTROLSS_CMPSSA3	5020 302Ch
CONTROLSS_CMPSSA4	5020 402Ch
CONTROLSS_CMPSSA5	5020 502Ch
CONTROLSS_CMPSSA6	5020 602Ch
CONTROLSS_CMPSSA7	5020 702Ch
CONTROLSS_CMPSSA8	5020 802Ch
CONTROLSS_CMPSSA9	5020 902Ch

Access Types Legend

Table 3-230. CTRIPLFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1.
8 - 4	SAMPWIN	RW	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

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3.4.19 CONTROLSS_CMPSSAn_CTRIPLFILCLKCTL Registers

3.4.19.1 CMPSSAn_CTRIPLFILCLKCTL Register (Offset = 2Eh) [reset = h]

Short Description: CTRIPL Filter Clock Control Register

Long Description:

Return to Summary Table

Table 3-231. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 002Eh
CONTROLSS_CMPSSA1	5020 102Eh
CONTROLSS_CMPSSA2	5020 202Eh
CONTROLSS_CMPSSA3	5020 302Eh
CONTROLSS_CMPSSA4	5020 402Eh
CONTROLSS_CMPSSA5	5020 502Eh
CONTROLSS_CMPSSA6	5020 602Eh
CONTROLSS_CMPSSA7	5020 702Eh
CONTROLSS_CMPSSA8	5020 802Eh
CONTROLSS_CMPSSA9	5020 902Eh

Access Types Legend

Table 3-232. CTRIPLFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	CLKPRESCALE	RW	0h	Low filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1.

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3.4.20 CONTROLSS_CMPSSAn_CTRIPHFILCTL Registers

3.4.20.1 CMPSSAn_CTRIPHFILCTL Register (Offset = 30h) [reset = h]

Short Description: CTRIPH Filter Control Register

Long Description:

Return to Summary Table

Table 3-233. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0030h
CONTROLSS_CMPSSA1	5020 1030h
CONTROLSS_CMPSSA2	5020 2030h
CONTROLSS_CMPSSA3	5020 3030h
CONTROLSS_CMPSSA4	5020 4030h
CONTROLSS_CMPSSA5	5020 5030h
CONTROLSS_CMPSSA6	5020 6030h
CONTROLSS_CMPSSA7	5020 7030h
CONTROLSS_CMPSSA8	5020 8030h
CONTROLSS_CMPSSA9	5020 9030h

Access Types Legend

Table 3-234. CTRIPHFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1.
8 - 4	SAMPWIN	RW	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

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3.4.21 CONTROLSS_CMPSSAn_CTRIPHFILCLKCTL Registers

3.4.21.1 CMPSSAn_CTRIPHFILCLKCTL Register (Offset = 32h) [reset = h]

Short Description: CTRIPH Filter Clock Control Register

Long Description:

Return to Summary Table

Table 3-235. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0032h
CONTROLSS_CMPSSA1	5020 1032h
CONTROLSS_CMPSSA2	5020 2032h
CONTROLSS_CMPSSA3	5020 3032h
CONTROLSS_CMPSSA4	5020 4032h
CONTROLSS_CMPSSA5	5020 5032h
CONTROLSS_CMPSSA6	5020 6032h
CONTROLSS_CMPSSA7	5020 7032h
CONTROLSS_CMPSSA8	5020 8032h
CONTROLSS_CMPSSA9	5020 9032h

Access Types Legend

Table 3-236. CTRIPHFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	CLKPRESCALE	RW	0h	High filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1.

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3.4.22 CONTROLSS_CMPSSAn_COMPLOCK Registers

3.4.22.1 CMPSSAn_COMPLOCK Register (Offset = 34h) [reset = h]

Short Description: CMPSS Lock Register

Long Description:

Return to Summary Table

Table 3-237. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0034h
CONTROLSS_CMPSSA1	5020 1034h
CONTROLSS_CMPSSA2	5020 2034h
CONTROLSS_CMPSSA3	5020 3034h
CONTROLSS_CMPSSA4	5020 4034h
CONTROLSS_CMPSSA5	5020 5034h
CONTROLSS_CMPSSA6	5020 6034h
CONTROLSS_CMPSSA7	5020 7034h
CONTROLSS_CMPSSA8	5020 8034h
CONTROLSS_CMPSSA9	5020 9034h

Access Types Legend

Table 3-238. COMPLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 5	RESERVED	RO		Reserved
4	TEST	RW SONCE	0h	TEST Lock. This bit, when set, will prevent any further writes to the any undocumented registers that may affect the performance/ behavior of this block. Once set this bit can only be cleared by a reset.
3	CTRIP	RW SONCE	0h	Lock write-access to the CTRIPxFILTCTL and CTRIPxFILCLKCTL registers. 0 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are locked. Only a system reset can clear this bit.
2	DACCTL	RW SONCE	0h	Lock write-access to the DACCTL register. 0 DACCTL register is not locked. Write 0 to this bit has no effect. 1 DACCTL register is locked. Only a system reset can clear this bit.
1	COMPHYSCTL	RW SONCE	0h	Lock write-access to the COMPHYSCTL register. 0 COMPHYSCTL register is not locked. Write 0 to this bit has no effect. 1 COMPHYSCTL register is locked. Only a system reset can clear this bit.
0	COMPCTL	RW SONCE	0h	Lock write-access to the COMPCTL register. 0 COMPCTL register is not locked. Write 0 to this bit has no effect. 1 COMPCTL register is locked. Only a system reset can clear this bit.

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3.4.23 CONTROLSS_CMPSSAn_DACHVALS2 Registers

3.4.23.1 CMPSSAn_DACHVALS2 Register (Offset = 38h) [reset = h]

Short Description: CMPSS High DAC Value Shadow Register 2

Long Description:

Return to Summary Table

Table 3-239. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 0038h
CONTROLSS_CMPSSA1	5020 1038h
CONTROLSS_CMPSSA2	5020 2038h
CONTROLSS_CMPSSA3	5020 3038h
CONTROLSS_CMPSSA4	5020 4038h
CONTROLSS_CMPSSA5	5020 5038h
CONTROLSS_CMPSSA6	5020 6038h
CONTROLSS_CMPSSA7	5020 7038h
CONTROLSS_CMPSSA8	5020 8038h
CONTROLSS_CMPSSA9	5020 9038h

Access Types Legend

Table 3-240. DACHVALS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RW	0h	High DAC shadow register2 value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted.

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3.4.24 CONTROLSS_CMPSSAn_DACLVALS2 Registers

3.4.24.1 CMPSSAn_DACLVALS2 Register (Offset = 3Ah) [reset = h]

Short Description: CMPSS Low DAC Value Shadow Register 2

Long Description:

Return to Summary Table

Table 3-241. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 003Ah
CONTROLSS_CMPSSA1	5020 103Ah
CONTROLSS_CMPSSA2	5020 203Ah
CONTROLSS_CMPSSA3	5020 303Ah
CONTROLSS_CMPSSA4	5020 403Ah
CONTROLSS_CMPSSA5	5020 503Ah
CONTROLSS_CMPSSA6	5020 603Ah
CONTROLSS_CMPSSA7	5020 703Ah
CONTROLSS_CMPSSA8	5020 803Ah
CONTROLSS_CMPSSA9	5020 903Ah

Access Types Legend

Table 3-242. DACLVALS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RW	0h	Low DAC shadow register2 value. Value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted.

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3.4.25 CONTROLSS_CMPSSAn_CONFIG1 Registers

3.4.25.1 CMPSSAn_CONFIG1 Register (Offset = 3Ch) [reset = h]

Short Description: CMPSS Config1 Register

Long Description:

Return to Summary Table

Table 3-243. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSA0	5020 003Ch
CONTROLSS_CMPSSA1	5020 103Ch
CONTROLSS_CMPSSA2	5020 203Ch
CONTROLSS_CMPSSA3	5020 303Ch
CONTROLSS_CMPSSA4	5020 403Ch
CONTROLSS_CMPSSA5	5020 503Ch
CONTROLSS_CMPSSA6	5020 603Ch
CONTROLSS_CMPSSA7	5020 703Ch
CONTROLSS_CMPSSA8	5020 803Ch
CONTROLSS_CMPSSA9	5020 903Ch

Access Types Legend

Table 3-244. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	SPARE	RW	0h	SPARE
7 - 4	COMPLHYS	RW	0h	compL Hysterisishystl_1p1v[3] = reservedhystl_1p1v[2] = control which comparator output value the hysteresis is applied tohystl_1p1v[1:0] = hysteresis value00 0 LSB01 17.5 LSB10 35 LSB11 52.5 LSB
3 - 0	COMPHHYS	RW	0h	CompH Hysteresishysth_1p1v[3] = reservedhysth_1p1v[2] 0 comparator hysteresis is applied when the comparator output is 1'b11 comparator hysteresis is applied when the comparator output is 1'b0hysth_1p1v[1:0] = hysteresis value00 0 LSB01 17.5 LSB10 35 LSB11 52.5 LSB

3.4.26 Access Table

Table 3-245. Access Type Codes

Access Type	Code	Description
RW	RW	Read / Write
RO	RO	Read
RW RRETURNS0S	RW RRETURNS0S	Read returns 0s/Write
RW SONCE	RW SONCE	Read/Write (Set Once)

3.5 CMPSSB Registers

Table 3-246. CONTROLSS_CMPSSB[0:2] Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_CMPSSB0 Physical Address	CONTROLSS_CMPSSB1 Physical Address	CONTROLSS_CMPSSB2 Physical Address
0h	16	CMPSSB_COMPCTL	5022 0000h	5022 1000h	5022 2000h
4h	16	CMPSSB_COMPSTS	5022 0004h	5022 1004h	5022 2004h
6h	16	CMPSSB_COMPSTSCLR	5022 0006h	5022 1006h	5022 2006h

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Table 3-246. CONTROLSS_CMPSSB[0:2] Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_CMPSSB0 Physical Address	CONTROLSS_CMPSSB1 Physical Address	CONTROLSS_CMPSSB2 Physical Address
8h	16	CMPSSB_COMPDACCTL	5022 0008h	5022 1008h	5022 2008h
Ah	16	CMPSSB_COMPDACCTL2	5022 000Ah	5022 100Ah	5022 200Ah
Ch	16	CMPSSB_DACHVALS	5022 000Ch	5022 100Ch	5022 200Ch
Eh	16	CMPSSB_DACHVALA	5022 000Eh	5022 100Eh	5022 200Eh
10h	16	CMPSSB_RAMPMAXREFA	5022 0010h	5022 1010h	5022 2010h
14h	16	CMPSSB_RAMPMAXREFS	5022 0014h	5022 1014h	5022 2014h
18h	16	CMPSSB_RAMPDECVALA	5022 0018h	5022 1018h	5022 2018h
1Ch	16	CMPSSB_RAMPDECVALS	5022 001Ch	5022 101Ch	5022 201Ch
20h	16	CMPSSB_RAMPSTS	5022 0020h	5022 1020h	5022 2020h
24h	16	CMPSSB_DACLVALS	5022 0024h	5022 1024h	5022 2024h
26h	16	CMPSSB_DACLVALA	5022 0026h	5022 1026h	5022 2026h
28h	16	CMPSSB_RAMPDLYA	5022 0028h	5022 1028h	5022 2028h
2Ah	16	CMPSSB_RAMPDLYS	5022 002Ah	5022 102Ah	5022 202Ah
2Ch	16	CMPSSB_CTRIPLFILCTL	5022 002Ch	5022 102Ch	5022 202Ch
2Eh	16	CMPSSB_CTRIPLFILCLKCTL	5022 002Eh	5022 102Eh	5022 202Eh
30h	16	CMPSSB_CTRIPHFILCTL	5022 0030h	5022 1030h	5022 2030h
32h	16	CMPSSB_CTRIPHFILCLKCTL	5022 0032h	5022 1032h	5022 2032h
34h	16	CMPSSB_COMPLOCK	5022 0034h	5022 1034h	5022 2034h
38h	16	CMPSSB_DACHVALS2	5022 0038h	5022 1038h	5022 2038h
3Ah	16	CMPSSB_DACLVALS2	5022 003Ah	5022 103Ah	5022 203Ah
3Ch	16	CMPSSB_CONFIG1	5022 003Ch	5022 103Ch	5022 203Ch

Table 3-247. CONTROLSS_CMPSSB[3:5] Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_CMPSSB3 Physical Address	CONTROLSS_CMPSSB4 Physical Address	CONTROLSS_CMPSSB5 Physical Address
0h	16	CMPSSB_COMPCTL	5022 3000h	5022 4000h	5022 5000h
4h	16	CMPSSB_COMPSTS	5022 3004h	5022 4004h	5022 5004h
6h	16	CMPSSB_COMPSTSCLR	5022 3006h	5022 4006h	5022 5006h
8h	16	CMPSSB_COMPDACCTL	5022 3008h	5022 4008h	5022 5008h
Ah	16	CMPSSB_COMPDACCTL2	5022 300Ah	5022 400Ah	5022 500Ah
Ch	16	CMPSSB_DACHVALS	5022 300Ch	5022 400Ch	5022 500Ch
Eh	16	CMPSSB_DACHVALA	5022 300Eh	5022 400Eh	5022 500Eh
10h	16	CMPSSB_RAMPMAXREFA	5022 3010h	5022 4010h	5022 5010h
14h	16	CMPSSB_RAMPMAXREFS	5022 3014h	5022 4014h	5022 5014h
18h	16	CMPSSB_RAMPDECVALA	5022 3018h	5022 4018h	5022 5018h
1Ch	16	CMPSSB_RAMPDECVALS	5022 301Ch	5022 401Ch	5022 501Ch
20h	16	CMPSSB_RAMPSTS	5022 3020h	5022 4020h	5022 5020h
24h	16	CMPSSB_DACLVALS	5022 3024h	5022 4024h	5022 5024h
26h	16	CMPSSB_DACLVALA	5022 3026h	5022 4026h	5022 5026h
28h	16	CMPSSB_RAMPDLYA	5022 3028h	5022 4028h	5022 5028h
2Ah	16	CMPSSB_RAMPDLYS	5022 302Ah	5022 402Ah	5022 502Ah
2Ch	16	CMPSSB_CTRIPLFILCTL	5022 302Ch	5022 402Ch	5022 502Ch
2Eh	16	CMPSSB_CTRIPLFILCLKCTL	5022 302Eh	5022 402Eh	5022 502Eh
30h	16	CMPSSB_CTRIPHFILCTL	5022 3030h	5022 4030h	5022 5030h
32h	16	CMPSSB_CTRIPHFILCLKCTL	5022 3032h	5022 4032h	5022 5032h
34h	16	CMPSSB_COMPLOCK	5022 3034h	5022 4034h	5022 5034h

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Table 3-247. CONTROLSS_CMPSSB[3:5] Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_CMPSSB3 Physical Address	CONTROLSS_CMPSSB4 Physical Address	CONTROLSS_CMPSSB5 Physical Address
38h	16	CMPSSB_DACHVALS2	5022 3038h	5022 4038h	5022 5038h
3Ah	16	CMPSSB_DACLVALS2	5022 303Ah	5022 403Ah	5022 503Ah
3Ch	16	CMPSSB_CONFIG1	5022 303Ch	5022 403Ch	5022 503Ch

Table 3-248. CONTROLSS_CMPSSB[6:8] Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_CMPSSB6 Physical Address	CONTROLSS_CMPSSB7 Physical Address	CONTROLSS_CMPSSB8 Physical Address
0h	16	CMPSSB_COMPCTL	5022 6000h	5022 7000h	5022 8000h
4h	16	CMPSSB_COMPSTS	5022 6004h	5022 7004h	5022 8004h
6h	16	CMPSSB_COMPSTSCLR	5022 6006h	5022 7006h	5022 8006h
8h	16	CMPSSB_COMPDACCTL	5022 6008h	5022 7008h	5022 8008h
Ah	16	CMPSSB_COMPDACCTL2	5022 600Ah	5022 700Ah	5022 800Ah
Ch	16	CMPSSB_DACHVALS	5022 600Ch	5022 700Ch	5022 800Ch
Eh	16	CMPSSB_DACHVALA	5022 600Eh	5022 700Eh	5022 800Eh
10h	16	CMPSSB_RAMPMAXREFA	5022 6010h	5022 7010h	5022 8010h
14h	16	CMPSSB_RAMPMAXREFS	5022 6014h	5022 7014h	5022 8014h
18h	16	CMPSSB_RAMPDECVALA	5022 6018h	5022 7018h	5022 8018h
1Ch	16	CMPSSB_RAMPDECVALS	5022 601Ch	5022 701Ch	5022 801Ch
20h	16	CMPSSB_RAMPSTS	5022 6020h	5022 7020h	5022 8020h
24h	16	CMPSSB_DACLVALS	5022 6024h	5022 7024h	5022 8024h
26h	16	CMPSSB_DACLVALA	5022 6026h	5022 7026h	5022 8026h
28h	16	CMPSSB_RAMPDLYA	5022 6028h	5022 7028h	5022 8028h
2Ah	16	CMPSSB_RAMPDLYS	5022 602Ah	5022 702Ah	5022 802Ah
2Ch	16	CMPSSB_CTRIPLFILCTL	5022 602Ch	5022 702Ch	5022 802Ch
2Eh	16	CMPSSB_CTRIPLFILCLKCTL	5022 602Eh	5022 702Eh	5022 802Eh
30h	16	CMPSSB_CTRIPHFILCTL	5022 6030h	5022 7030h	5022 8030h
32h	16	CMPSSB_CTRIPHFILCLKCTL	5022 6032h	5022 7032h	5022 8032h
34h	16	CMPSSB_COMPLOCK	5022 6034h	5022 7034h	5022 8034h
38h	16	CMPSSB_DACHVALS2	5022 6038h	5022 7038h	5022 8038h
3Ah	16	CMPSSB_DACLVALS2	5022 603Ah	5022 703Ah	5022 803Ah
3Ch	16	CMPSSB_CONFIG1	5022 603Ch	5022 703Ch	5022 803Ch

Table 3-249. CONTROLSS_CMPSSB9 Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_CMPSSB9 Physical Address
0h	16	CMPSSB_COMPCTL	5022 9000h
4h	16	CMPSSB_COMPSTS	5022 9004h
6h	16	CMPSSB_COMPSTSCLR	5022 9006h
8h	16	CMPSSB_COMPDACCTL	5022 9008h
Ah	16	CMPSSB_COMPDACCTL2	5022 900Ah
Ch	16	CMPSSB_DACHVALS	5022 900Ch
Eh	16	CMPSSB_DACHVALA	5022 900Eh
10h	16	CMPSSB_RAMPMAXREFA	5022 9010h
14h	16	CMPSSB_RAMPMAXREFS	5022 9014h
18h	16	CMPSSB_RAMPDECVALA	5022 9018h
1Ch	16	CMPSSB_RAMPDECVALS	5022 901Ch
20h	16	CMPSSB_RAMPSTS	5022 9020h

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Table 3-249. CONTROLSS_CMPSSB9 Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_CMPSSB9 Physical Address
24h	16	CMPSSB_DACLVALS	5022 9024h
26h	16	CMPSSB_DACLVALA	5022 9026h
28h	16	CMPSSB_RAMPDLYA	5022 9028h
2Ah	16	CMPSSB_RAMPDLYS	5022 902Ah
2Ch	16	CMPSSB_CTRIPLFILCTL	5022 902Ch
2Eh	16	CMPSSB_CTRIPLFILCLKCTL	5022 902Eh
30h	16	CMPSSB_CTRIPHFILCTL	5022 9030h
32h	16	CMPSSB_CTRIPHFILCLKCTL	5022 9032h
34h	16	CMPSSB_COMPLOCK	5022 9034h
38h	16	CMPSSB_DACHVALS2	5022 9038h
3Ah	16	CMPSSB_DACLVALS2	5022 903Ah
3Ch	16	CMPSSB_CONFIG1	5022 903Ch

3.5.1 CMPSSB Instance Count Note

Note

n = 0 to 9 for the CMPSSB registers defined below.

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3.5.2 CONTROLSS_CMPSSBn_COMPCTL Registers

3.5.2.1 CMPSSBn_COMPCTL Register (Offset = 0h) [reset = h]

Short Description: CMPSS Comparator Control Register

Long Description:

Return to Summary Table

Table 3-250. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0000h
CONTROLSS_CMPSSB1	5022 1000h
CONTROLSS_CMPSSB2	5022 2000h
CONTROLSS_CMPSSB3	5022 3000h
CONTROLSS_CMPSSB4	5022 4000h
CONTROLSS_CMPSSB5	5022 5000h
CONTROLSS_CMPSSB6	5022 6000h
CONTROLSS_CMPSSB7	5022 7000h
CONTROLSS_CMPSSB8	5022 8000h
CONTROLSS_CMPSSB9	5022 9000h

Access Types Legend

Table 3-251. COMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	COMPDACE	RW	0h	Comparator/DAC enable. 0 Comparator/DAC disabled 1 Comparator/DAC enabled
14	ASYNCLEN	RW	0h	Low comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPLSEL=3 or CTRIPOUTLSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output
13 - 12	CTRIPOUTLSEL	RW	0h	Low comparator CTRIPOUTL source select. 0 Asynchronous comparator output drives CTRIPOUTL 1 Synchronous comparator output drives CTRIPOUTL 2 Output of digital filter drives CTRIPOUTL 3 Latched output of digital filter drives CTRIPOUTL
11 - 10	CTRIPLSEL	RW	0h	Low comparator CTRIPL source select. 0 Asynchronous comparator output drives CTRIPL 1 Synchronous comparator output drives CTRIPL 2 Output of digital filter drives CTRIPL 3 Latched output of digital filter drives CTRIPL
9	COMPLINV	RW	0h	Low comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted
8	RESERVED_3	RW	0h	Reserved for CMPSSB
7	RESERVED	RO		Reserved
6	ASYNCHEN	RW	0h	High comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPHSEL=3 or CTRIPOUTHSEL=3. 0 Asynchronous comparator output does not feed into OR gate with latched digital filter output 1 Asynchronous comparator output feeds into OR gate with latched digital filter output
5 - 4	CTRIPOUTHSEL	RW	0h	High comparator CTRIPOUTH source select. 0 Asynchronous comparator output drives CTRIPOUTH 1 Synchronous comparator output drives CTRIPOUTH 2 Output of digital filter drives CTRIPOUTH 3 Latched output of digital filter drives CTRIPOUTH

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Table 3-251. COMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 2	CTRIPHSEL	RW	0h	High comparator CTRIPH source select. 0 Asynchronous comparator output drives CTRIPH 1 Synchronous comparator output drives CTRIPH 2 Output of digital filter drives CTRIPH 3 Latched output of digital filter drives CTRIPH
1	COMPHINV	RW	0h	High comparator output invert. 0 Output of comparator is not inverted 1 Output of comparator is inverted
0	RESERVED_1	RW	0h	Reserved for CMPSSB

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3.5.3 CONTROLSS_CMPSSBn_COMPSTS Registers

3.5.3.1 CMPSSBn_COMPSTS Register (Offset = 4h) [reset = h]

Short Description: CMPSS Comparator Status Register

Long Description:

Return to Summary Table

Table 3-252. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0004h
CONTROLSS_CMPSSB1	5022 1004h
CONTROLSS_CMPSSB2	5022 2004h
CONTROLSS_CMPSSB3	5022 3004h
CONTROLSS_CMPSSB4	5022 4004h
CONTROLSS_CMPSSB5	5022 5004h
CONTROLSS_CMPSSB6	5022 6004h
CONTROLSS_CMPSSB7	5022 7004h
CONTROLSS_CMPSSB8	5022 8004h
CONTROLSS_CMPSSB9	5022 9004h

Access Types Legend

Table 3-253. COMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9	COMPLLATCH	RO	0h	Latched value of low comparator digital filter output
8	COMPLSTS	RO	0h	Low comparator digital filter output
7 - 2	RESERVED	RO		Reserved
1	COMPHLATCH	RO	0h	Latched value of high comparator digital filter output
0	COMPHSTS	RO	0h	High comparator digital filter output

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3.5.4 CONTROLSS_CMPSSBn_COMPSTSCLR Registers

3.5.4.1 CMPSSBn_COMPSTSCLR Register (Offset = 6h) [reset = h]

Short Description: CMPSS Comparator Status Clear Register

Long Description:

Return to Summary Table

Table 3-254. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0006h
CONTROLSS_CMPSSB1	5022 1006h
CONTROLSS_CMPSSB2	5022 2006h
CONTROLSS_CMPSSB3	5022 3006h
CONTROLSS_CMPSSB4	5022 4006h
CONTROLSS_CMPSSB5	5022 5006h
CONTROLSS_CMPSSB6	5022 6006h
CONTROLSS_CMPSSB7	5022 7006h
CONTROLSS_CMPSSB8	5022 8006h
CONTROLSS_CMPSSB9	5022 9006h

Access Types Legend

Table 3-255. COMPSTSCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO		Reserved
10	LSYNCCLREN	RW	0h	Low comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. 0 EPWMSYNCPER will not reset latch 1 EPWMSYNCPER will reset latch
9	LLATCHCLR	RW RRETURNS 0S	0h	Low comparator latch software clear. Perform software reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPLLATCH]
8 - 3	RESERVED	RO		Reserved
2	HSYNCCLREN	RW	0h	High comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. 0 EPWMSYNCPER will not reset latch 1 EPWMSYNCPER will reset latch
1	HLATCHCLR	RW RRETURNS 0S	0h	High comparator latch software clear. Perform software reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. Reads always return 0. 0 No effect 1 Generate a single pulse of latch reset signal for COMPSTS[COMPHLATCH]
0	RESERVED	RO		Reserved

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3.5.5 CONTROLSS_CMPSSBn_COMPDACCTL Registers

3.5.5.1 CMPSSBn_COMPDACCTL Register (Offset = 8h) [reset = h]

Short Description: CMPSS DAC Control Register

Long Description:

Return to Summary Table

Table 3-256. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0008h
CONTROLSS_CMPSSB1	5022 1008h
CONTROLSS_CMPSSB2	5022 2008h
CONTROLSS_CMPSSB3	5022 3008h
CONTROLSS_CMPSSB4	5022 4008h
CONTROLSS_CMPSSB5	5022 5008h
CONTROLSS_CMPSSB6	5022 6008h
CONTROLSS_CMPSSB7	5022 7008h
CONTROLSS_CMPSSB8	5022 8008h
CONTROLSS_CMPSSB9	5022 9008h

Access Types Legend

Table 3-257. COMPDACCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	FREESOFT	RW	0h	Free-run or software-run emulation behavior. Behavior of the ramp generator during emulation suspend. 00b Ramp generator stops immediately during emulation suspend 01b Ramp generator completes current ramp and stops at next EPWMSYNCPER during emulation suspend 1Xb Ramp generator runs freely
13	RESERVED	RO		Reserved
12	BLANKEN	RW	0h	EPWMBLANK enable. This bit enables the EPWMBLANK signal. 0 EPWMBLANK signal is disabled. 1 EPWMBLANK signal is enabled.
11 - 8	BLANKSOURCE	RW	0h	EPWMBLANK source select. This bit field determines which EPWMnBLANK is passed on as the EPWMBLANK signal. Where n represents the maximum number of EPWMBLANK signals available on the device: 0 EPWM1BLANK 1 EPWM2BLANK 2 EPWM3BLANK ... n-1 EPWMnBLANK
7	SWLOADSEL	RW	0h	Software load select. Determines whether DACxVALA is updated from DACxVALS on SYSCLK or EPWMSYNCPER. 0 DACxVALA is updated from DACxVALS on SYSCLK 1 DACxVALA is updated from DACxVALS on EPWMSYNCPER
6	RAMPLOADSEL	RW	0h	Ramp load select. Determines whether RAMPSTS is updated from RAMPMAXREFA or RAMPMAXREFS when COMPSTS[COMPHSTS] is triggered. 0 RAMPSTS is loaded from RAMPMAXREFA 1 RAMPSTS is loaded from RAMPMAXREFS
5	SELREF	RW	0h	CMPSS reference select0 vref_1p8v as reference voltage (default)1 vdd_1p8v as reference voltage
4 - 1	RAMPSOURCE	RW	0h	EPWMSYNCPER source select. Determines which EPWMnSYNCPER signal is used within the CMPSS module. Where n represents the maximum number of EPWMSYNCPER signals available on the device: 0 EPWM1SYNCPER 1 EPWM2SYNCPER 2 EPWM3SYNCPER ... n-1 EPWMnSYNCPER
0	DACSOURCE	RW	0h	DAC source select. Determines whether DACHVALA is updated from DACHVALS or from the ramp generator. 0 DACHVALA is updated from DACHVALS 1 DACHVALA is updated from the ramp generator

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3.5.6 CONTROLSS_CMPSSBn_COMPDACCTL2 Registers

3.5.6.1 CMPSSBn_COMPDACCTL2 Register (Offset = Ah) [reset = h]

Short Description: CMPSS DAC Control Register 2

Long Description:

Return to Summary Table

Table 3-258. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 000Ah
CONTROLSS_CMPSSB1	5022 100Ah
CONTROLSS_CMPSSB2	5022 200Ah
CONTROLSS_CMPSSB3	5022 300Ah
CONTROLSS_CMPSSB4	5022 400Ah
CONTROLSS_CMPSSB5	5022 500Ah
CONTROLSS_CMPSSB6	5022 600Ah
CONTROLSS_CMPSSB7	5022 700Ah
CONTROLSS_CMPSSB8	5022 800Ah
CONTROLSS_CMPSSB9	5022 900Ah

Access Types Legend

Table 3-259. COMPDACCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO		Reserved
10	RAMPSOURCEUSEL	RW	0h	0: Selects EPWM0 to 15 as RAMP source 1: Selects EPWM16 to 31 as RAMP source
9	RESERVED	RO		Reserved
8	BLANKSOURCEUSEL	RW	0h	0: Selects EPWM0 to 15 as blank source 1: Selects EPWM16 to 31 as blank source
7 - 6	RESERVED	RO		Reserved
5 - 1	DEACTIVESEL	RW	0h	DEACTIVE source select: 0x0 : EPWM1.DEACTIVE 0x1 : EPWM2.DEACTIVE 0x2 : EPWM3.DEACTIVE 0x3 : EPWM4.DEACTIVE . . 0x31 : EPWM32.DEACTIVE
0	DEENABLE	RW	0h	DE mode enable. 0 DE mode features disabled. 1 DE mode features enabled.

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3.5.7 CONTROLSS_CMPSSBn_DACHVALS Registers

3.5.7.1 CMPSSBn_DACHVALS Register (Offset = Ch) [reset = h]

Short Description: CMPSS High DAC Value Shadow Register

Long Description:

Return to Summary Table

Table 3-260. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 000Ch
CONTROLSS_CMPSSB1	5022 100Ch
CONTROLSS_CMPSSB2	5022 200Ch
CONTROLSS_CMPSSB3	5022 300Ch
CONTROLSS_CMPSSB4	5022 400Ch
CONTROLSS_CMPSSB5	5022 500Ch
CONTROLSS_CMPSSB6	5022 600Ch
CONTROLSS_CMPSSB7	5022 700Ch
CONTROLSS_CMPSSB8	5022 800Ch
CONTROLSS_CMPSSB9	5022 900Ch

Access Types Legend

Table 3-261. DACHVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RW	0h	High DAC shadow value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS is loaded into DACHVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL].

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3.5.8 CONTROLSS_CMPSSBn_DACHVALA Registers

3.5.8.1 CMPSSBn_DACHVALA Register (Offset = Eh) [reset = h]

Short Description: CMPSS High DAC Value Active Register

Long Description:

Return to Summary Table

Table 3-262. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 000Eh
CONTROLSS_CMPSSB1	5022 100Eh
CONTROLSS_CMPSSB2	5022 200Eh
CONTROLSS_CMPSSB3	5022 300Eh
CONTROLSS_CMPSSB4	5022 400Eh
CONTROLSS_CMPSSB5	5022 500Eh
CONTROLSS_CMPSSB6	5022 600Eh
CONTROLSS_CMPSSB7	5022 700Eh
CONTROLSS_CMPSSB8	5022 800Eh
CONTROLSS_CMPSSB9	5022 900Eh

Access Types Legend

Table 3-263. DACHVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RO	0h	High DAC active value. Value that is actively driven by the high DAC.

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3.5.9 CONTROLSS_CMPSSBn_RAMPMAXREFA Registers

3.5.9.1 CMPSSBn_RAMPMAXREFA Register (Offset = 10h) [reset = h]

Short Description: CMPSS Ramp Max Reference Active Register

Long Description:

Return to Summary Table

Table 3-264. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0010h
CONTROLSS_CMPSSB1	5022 1010h
CONTROLSS_CMPSSB2	5022 2010h
CONTROLSS_CMPSSB3	5022 3010h
CONTROLSS_CMPSSB4	5022 4010h
CONTROLSS_CMPSSB5	5022 5010h
CONTROLSS_CMPSSB6	5022 6010h
CONTROLSS_CMPSSB7	5022 7010h
CONTROLSS_CMPSSB8	5022 8010h
CONTROLSS_CMPSSB9	5022 9010h

Access Types Legend

Table 3-265. RAMPMAXREFA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPMAXREF	RO	0h	Ramp maximum reference active value. Latched value to be loaded into ramp generator RAMPSTS.

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3.5.10 CONTROLSS_CMPSSBn_RAMPMAXREFS Registers

3.5.10.1 CMPSSBn_RAMPMAXREFS Register (Offset = 14h) [reset = h]

Short Description: CMPSS Ramp Max Reference Shadow Register

Long Description:

Return to Summary Table

Table 3-266. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0014h
CONTROLSS_CMPSSB1	5022 1014h
CONTROLSS_CMPSSB2	5022 2014h
CONTROLSS_CMPSSB3	5022 3014h
CONTROLSS_CMPSSB4	5022 4014h
CONTROLSS_CMPSSB5	5022 5014h
CONTROLSS_CMPSSB6	5022 6014h
CONTROLSS_CMPSSB7	5022 7014h
CONTROLSS_CMPSSB8	5022 8014h
CONTROLSS_CMPSSB9	5022 9014h

Access Types Legend

Table 3-267. RAMPMAXREFS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPMAXREF	RW	0h	Ramp maximum reference shadow. Unlatched value to be loaded into ramp generator RAMPSTS.

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3.5.11 CONTROLSS_CMPSSBn_RAMPDECVALA Registers

3.5.11.1 CMPSSBn_RAMPDECVALA Register (Offset = 18h) [reset = h]

Short Description: CMPSS Ramp Decrement Value Active Register

Long Description:

Return to Summary Table

Table 3-268. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0018h
CONTROLSS_CMPSSB1	5022 1018h
CONTROLSS_CMPSSB2	5022 2018h
CONTROLSS_CMPSSB3	5022 3018h
CONTROLSS_CMPSSB4	5022 4018h
CONTROLSS_CMPSSB5	5022 5018h
CONTROLSS_CMPSSB6	5022 6018h
CONTROLSS_CMPSSB7	5022 7018h
CONTROLSS_CMPSSB8	5022 8018h
CONTROLSS_CMPSSB9	5022 9018h

Access Types Legend

Table 3-269. RAMPDECVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPDECVAL	RO	0h	Ramp decrement value active. Latched value that will be subtracted from RAMPSTS.

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3.5.12 CONTROLSS_CMPSSBn_RAMPDECVALS Registers

3.5.12.1 CMPSSBn_RAMPDECVALS Register (Offset = 1Ch) [reset = h]

Short Description: CMPSS Ramp Decrement Value Shadow Register

Long Description:

Return to Summary Table

Table 3-270. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 001Ch
CONTROLSS_CMPSSB1	5022 101Ch
CONTROLSS_CMPSSB2	5022 201Ch
CONTROLSS_CMPSSB3	5022 301Ch
CONTROLSS_CMPSSB4	5022 401Ch
CONTROLSS_CMPSSB5	5022 501Ch
CONTROLSS_CMPSSB6	5022 601Ch
CONTROLSS_CMPSSB7	5022 701Ch
CONTROLSS_CMPSSB8	5022 801Ch
CONTROLSS_CMPSSB9	5022 901Ch

Access Types Legend

Table 3-271. RAMPDECVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPDECVAL	RW	0h	Ramp decrement value shadow. Unlatched value to be loaded into RAMPDECVALA.

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3.5.13 CONTROLSS_CMPSSBn_RAMPSTS Registers

3.5.13.1 CMPSSBn_RAMPSTS Register (Offset = 20h) [reset = h]

Short Description: CMPSS Ramp Status Register

Long Description:

Return to Summary Table

Table 3-272. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0020h
CONTROLSS_CMPSSB1	5022 1020h
CONTROLSS_CMPSSB2	5022 2020h
CONTROLSS_CMPSSB3	5022 3020h
CONTROLSS_CMPSSB4	5022 4020h
CONTROLSS_CMPSSB5	5022 5020h
CONTROLSS_CMPSSB6	5022 6020h
CONTROLSS_CMPSSB7	5022 7020h
CONTROLSS_CMPSSB8	5022 8020h
CONTROLSS_CMPSSB9	5022 9020h

Access Types Legend

Table 3-273. RAMPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	RAMPVALUE	RO	0h	Ramp value. Present value of ramp generator.

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3.5.14 CONTROLSS_CMPSSBn_DACLVALS Registers

3.5.14.1 CMPSSBn_DACLVALS Register (Offset = 24h) [reset = h]

Short Description: CMPSS Low DAC Value Shadow Register

Long Description:

Return to Summary Table

Table 3-274. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0024h
CONTROLSS_CMPSSB1	5022 1024h
CONTROLSS_CMPSSB2	5022 2024h
CONTROLSS_CMPSSB3	5022 3024h
CONTROLSS_CMPSSB4	5022 4024h
CONTROLSS_CMPSSB5	5022 5024h
CONTROLSS_CMPSSB6	5022 6024h
CONTROLSS_CMPSSB7	5022 7024h
CONTROLSS_CMPSSB8	5022 8024h
CONTROLSS_CMPSSB9	5022 9024h

Access Types Legend

Table 3-275. DACLVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RW	0h	Low DAC shadow value. value to be loaded into DACLVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL].

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3.5.15 CONTROLSS_CMPSSBn_DACLVALA Registers

3.5.15.1 CMPSSBn_DACLVALA Register (Offset = 26h) [reset = h]

Short Description: CMPSS Low DAC Value Active Register

Long Description:

Return to Summary Table

Table 3-276. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0026h
CONTROLSS_CMPSSB1	5022 1026h
CONTROLSS_CMPSSB2	5022 2026h
CONTROLSS_CMPSSB3	5022 3026h
CONTROLSS_CMPSSB4	5022 4026h
CONTROLSS_CMPSSB5	5022 5026h
CONTROLSS_CMPSSB6	5022 6026h
CONTROLSS_CMPSSB7	5022 7026h
CONTROLSS_CMPSSB8	5022 8026h
CONTROLSS_CMPSSB9	5022 9026h

Access Types Legend

Table 3-277. DACLVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RO	0h	Low DAC active value. Value that is actively driven by the low DAC.

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3.5.16 CONTROLSS_CMPSSBn_RAMPDLYA Registers

3.5.16.1 CMPSSBn_RAMPDLYA Register (Offset = 28h) [reset = h]

Short Description: CMPSS Ramp Delay Active Register

Long Description:

Return to Summary Table

Table 3-278. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0028h
CONTROLSS_CMPSSB1	5022 1028h
CONTROLSS_CMPSSB2	5022 2028h
CONTROLSS_CMPSSB3	5022 3028h
CONTROLSS_CMPSSB4	5022 4028h
CONTROLSS_CMPSSB5	5022 5028h
CONTROLSS_CMPSSB6	5022 6028h
CONTROLSS_CMPSSB7	5022 7028h
CONTROLSS_CMPSSB8	5022 8028h
CONTROLSS_CMPSSB9	5022 9028h

Access Types Legend

Table 3-279. RAMPDLYA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12 - 0	DELAY	RO	0h	Ramp delay active value. Latched value of the number of cycles to delay the start of the ramp generator decrementer after a EPWMSYNCPER is received.

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3.5.17 CONTROLSS_CMPSSBn_RAMPDLYS Registers

3.5.17.1 CMPSSBn_RAMPDLYS Register (Offset = 2Ah) [reset = h]

Short Description: CMPSS Ramp Delay Shadow Register

Long Description:

Return to Summary Table

Table 3-280. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 002Ah
CONTROLSS_CMPSSB1	5022 102Ah
CONTROLSS_CMPSSB2	5022 202Ah
CONTROLSS_CMPSSB3	5022 302Ah
CONTROLSS_CMPSSB4	5022 402Ah
CONTROLSS_CMPSSB5	5022 502Ah
CONTROLSS_CMPSSB6	5022 602Ah
CONTROLSS_CMPSSB7	5022 702Ah
CONTROLSS_CMPSSB8	5022 802Ah
CONTROLSS_CMPSSB9	5022 902Ah

Access Types Legend

Table 3-281. RAMPDLYS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12 - 0	DELAY	RW	0h	Ramp delay shadow value. Unlatched value to be loaded into RAMPDLYA.

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3.5.18 CONTROLSS_CMPSSBn_CTRIPLFILCTL Registers

3.5.18.1 CMPSSBn_CTRIPLFILCTL Register (Offset = 2Ch) [reset = h]

Short Description: CTRIPL Filter Control Register

Long Description:

Return to Summary Table

Table 3-282. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 002Ch
CONTROLSS_CMPSSB1	5022 102Ch
CONTROLSS_CMPSSB2	5022 202Ch
CONTROLSS_CMPSSB3	5022 302Ch
CONTROLSS_CMPSSB4	5022 402Ch
CONTROLSS_CMPSSB5	5022 502Ch
CONTROLSS_CMPSSB6	5022 602Ch
CONTROLSS_CMPSSB7	5022 702Ch
CONTROLSS_CMPSSB8	5022 802Ch
CONTROLSS_CMPSSB9	5022 902Ch

Access Types Legend

Table 3-283. CTRIPLFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1.
8 - 4	SAMPWIN	RW	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

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3.5.19 CONTROLSS_CMPSSBn_CTRIPLFILCLKCTL Registers

3.5.19.1 CMPSSBn_CTRIPLFILCLKCTL Register (Offset = 2Eh) [reset = h]

Short Description: CTRIPL Filter Clock Control Register

Long Description:

Return to Summary Table

Table 3-284. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 002Eh
CONTROLSS_CMPSSB1	5022 102Eh
CONTROLSS_CMPSSB2	5022 202Eh
CONTROLSS_CMPSSB3	5022 302Eh
CONTROLSS_CMPSSB4	5022 402Eh
CONTROLSS_CMPSSB5	5022 502Eh
CONTROLSS_CMPSSB6	5022 602Eh
CONTROLSS_CMPSSB7	5022 702Eh
CONTROLSS_CMPSSB8	5022 802Eh
CONTROLSS_CMPSSB9	5022 902Eh

Access Types Legend

Table 3-285. CTRIPLFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	CLKPRESCALE	RW	0h	Low filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1.

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3.5.20 CONTROLSS_CMPSSBn_CTRIPHFILCTL Registers

3.5.20.1 CMPSSBn_CTRIPHFILCTL Register (Offset = 30h) [reset = h]

Short Description: CTRIPH Filter Control Register

Long Description:

Return to Summary Table

Table 3-286. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0030h
CONTROLSS_CMPSSB1	5022 1030h
CONTROLSS_CMPSSB2	5022 2030h
CONTROLSS_CMPSSB3	5022 3030h
CONTROLSS_CMPSSB4	5022 4030h
CONTROLSS_CMPSSB5	5022 5030h
CONTROLSS_CMPSSB6	5022 6030h
CONTROLSS_CMPSSB7	5022 7030h
CONTROLSS_CMPSSB8	5022 8030h
CONTROLSS_CMPSSB9	5022 9030h

Access Types Legend

Table 3-287. CTRIPHFILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1.
8 - 4	SAMPWIN	RW	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

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3.5.21 CONTROLSS_CMPSSBn_CTRIPHFILCLKCTL Registers

3.5.21.1 CMPSSBn_CTRIPHFILCLKCTL Register (Offset = 32h) [reset = h]

Short Description: CTRIPH Filter Clock Control Register

Long Description:

Return to Summary Table

Table 3-288. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0032h
CONTROLSS_CMPSSB1	5022 1032h
CONTROLSS_CMPSSB2	5022 2032h
CONTROLSS_CMPSSB3	5022 3032h
CONTROLSS_CMPSSB4	5022 4032h
CONTROLSS_CMPSSB5	5022 5032h
CONTROLSS_CMPSSB6	5022 6032h
CONTROLSS_CMPSSB7	5022 7032h
CONTROLSS_CMPSSB8	5022 8032h
CONTROLSS_CMPSSB9	5022 9032h

Access Types Legend

Table 3-289. CTRIPHFILCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	CLKPRESCALE	RW	0h	High filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1.

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3.5.22 CONTROLSS_CMPSSBn_COMPLOCK Registers

3.5.22.1 CMPSSBn_COMPLOCK Register (Offset = 34h) [reset = h]

Short Description: CMPSS Lock Register

Long Description:

Return to Summary Table

Table 3-290. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0034h
CONTROLSS_CMPSSB1	5022 1034h
CONTROLSS_CMPSSB2	5022 2034h
CONTROLSS_CMPSSB3	5022 3034h
CONTROLSS_CMPSSB4	5022 4034h
CONTROLSS_CMPSSB5	5022 5034h
CONTROLSS_CMPSSB6	5022 6034h
CONTROLSS_CMPSSB7	5022 7034h
CONTROLSS_CMPSSB8	5022 8034h
CONTROLSS_CMPSSB9	5022 9034h

Access Types Legend

Table 3-291. COMPLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 5	RESERVED	RO		Reserved
4	TEST	RW SONCE	0h	TEST Lock. This bit, when set, will prevent any further writes to the any undocumented registers that may affect the performance/ behavior of this block. Once set this bit can only be cleared by a reset.
3	CTRIP	RW SONCE	0h	Lock write-access to the CTRIPxFILTCTL and CTRIPxFILCLKCTL registers. 0 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 CTRIPxFILCTL and CTRIPxFILCLKCTL registers are locked. Only a system reset can clear this bit.
2	DACCTL	RW SONCE	0h	Lock write-access to the DACCTL register. 0 DACCTL register is not locked. Write 0 to this bit has no effect. 1 DACCTL register is locked. Only a system reset can clear this bit.
1	COMPHYSCTL	RW SONCE	0h	Lock write-access to the COMPHYSCTL register. 0 COMPHYSCTL register is not locked. Write 0 to this bit has no effect. 1 COMPHYSCTL register is locked. Only a system reset can clear this bit.
0	COMPCTL	RW SONCE	0h	Lock write-access to the COMPCTL register. 0 COMPCTL register is not locked. Write 0 to this bit has no effect. 1 COMPCTL register is locked. Only a system reset can clear this bit.

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3.5.23 CONTROLSS_CMPSSBn_DACHVALS2 Registers

3.5.23.1 CMPSSBn_DACHVALS2 Register (Offset = 38h) [reset = h]

Short Description: CMPSS High DAC Value Shadow Register 2

Long Description:

Return to Summary Table

Table 3-292. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 0038h
CONTROLSS_CMPSSB1	5022 1038h
CONTROLSS_CMPSSB2	5022 2038h
CONTROLSS_CMPSSB3	5022 3038h
CONTROLSS_CMPSSB4	5022 4038h
CONTROLSS_CMPSSB5	5022 5038h
CONTROLSS_CMPSSB6	5022 6038h
CONTROLSS_CMPSSB7	5022 7038h
CONTROLSS_CMPSSB8	5022 8038h
CONTROLSS_CMPSSB9	5022 9038h

Access Types Legend

Table 3-293. DACHVALS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RW	0h	High DAC shadow register2 value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted.

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3.5.24 CONTROLSS_CMPSSBn_DACLVALS2 Registers

3.5.24.1 CMPSSBn_DACLVALS2 Register (Offset = 3Ah) [reset = h]

Short Description: CMPSS Low DAC Value Shadow Register 2

Long Description:

Return to Summary Table

Table 3-294. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 003Ah
CONTROLSS_CMPSSB1	5022 103Ah
CONTROLSS_CMPSSB2	5022 203Ah
CONTROLSS_CMPSSB3	5022 303Ah
CONTROLSS_CMPSSB4	5022 403Ah
CONTROLSS_CMPSSB5	5022 503Ah
CONTROLSS_CMPSSB6	5022 603Ah
CONTROLSS_CMPSSB7	5022 703Ah
CONTROLSS_CMPSSB8	5022 803Ah
CONTROLSS_CMPSSB9	5022 903Ah

Access Types Legend

Table 3-295. DACLVALS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVAL	RW	0h	Low DAC shadow register2 value. Value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted.

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3.5.25 CONTROLSS_CMPSSBn_CONFIG1 Registers

3.5.25.1 CMPSSBn_CONFIG1 Register (Offset = 3Ch) [reset = h]

Short Description: CMPSS Config1 Register

Long Description:

Return to Summary Table

Table 3-296. Instance Table

Instance Name	Physical Address
CONTROLSS_CMPSSB0	5022 003Ch
CONTROLSS_CMPSSB1	5022 103Ch
CONTROLSS_CMPSSB2	5022 203Ch
CONTROLSS_CMPSSB3	5022 303Ch
CONTROLSS_CMPSSB4	5022 403Ch
CONTROLSS_CMPSSB5	5022 503Ch
CONTROLSS_CMPSSB6	5022 603Ch
CONTROLSS_CMPSSB7	5022 703Ch
CONTROLSS_CMPSSB8	5022 803Ch
CONTROLSS_CMPSSB9	5022 903Ch

Access Types Legend

Table 3-297. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	SPARE	RW	0h	SPARE
7 - 4	COMPLHYS	RW	0h	compL Hysterisishystl_1p1v[3] = reservedhystl_1p1v[2] = control which comparator output value the hysteresis is applied tohystl_1p1v[1:0] = hysteresis value00 0 LSB01 17.5 LSB10 35 LSB11 52.5 LSB
3 - 0	COMPHHYS	RW	0h	CompH Hysteresishysth_1p1v[3] = reservedhysth_1p1v[2] 0 comparator hysteresis is applied when the comparator output is 1'b11 comparator hysteresis is applied when the comparator output is 1'b0hysth_1p1v[1:0] = hysteresis value00 0 LSB01 17.5 LSB10 35 LSB11 52.5 LSB

3.5.26 Access Table

Table 3-298. Access Type Codes

Access Type	Code	Description
RW	RW	Read / Write
RO	RO	Read
RW RRETURNS0S	RW RRETURNS0S	Read returns 0s/Write
RW SONCE	RW SONCE	Read/Write (Set Once)

3.6 DAC Registers

Table 3-299. CONTROLSS_DAC0 Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_DAC0 Physical Address
0h	16	DAC_DACREV	5026 0000h
2h	16	DAC_DACCTL_ALT2_	5026 0002h
4h	16	DAC_DACVALA	5026 0004h
6h	16	DAC_DACVALS	5026 0006h

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Table 3-299. CONTROLSS_DAC0 Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_DAC0 Physical Address
8h	16	DAC_DACOUTEN	5026 0008h
Ah	16	DAC_DACLOCK	5026 000Ah
Ch	16	DAC_DACTRIM	5026 000Ch

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3.6.1 CONTROLSS_DAC0_DACREV Registers

3.6.1.1 DAC0_DACREV Register (Offset = 0h) [reset = h]

Short Description: DAC Revision Register

Long Description:

Return to Summary Table

Table 3-300. Instance Table

Instance Name	Physical Address
CONTROLSS_DAC0	5026 0000h

Access Types Legend

Table 3-301. DACREV Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO		Reserved
7 - 0	REV	RO	0h	DAC Revision

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3.6.2 CONTROLSS_DAC0_DACCTL_ALT2_ Registers

3.6.2.1 DAC0_DACCTL_ALT2_ Register (Offset = 2h) [reset = h]

Short Description: DAC Control Register

Long Description:

Return to Summary Table

Table 3-302. Instance Table

Instance Name	Physical Address
CONTROLSS_DAC0	5026 0002h

Access Types Legend

Table 3-303. DACCTL_ALT2_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9	RESERVED	RO		Reserved
8 - 4	SYNCSEL	RW	0h	DAC EPWMSYNCPER select. Determines which EPWMSYNCPER signal will update the DACVALA register.[[br]] [[br]]Where n represents the maximum number of EPWMSYNCPER signals available on the device:[[br]] [[br]] 0 EPWM1SYNCPER[[br]] 1 EPWM2SYNCPER[[br]] 2 EPWM3SYNCPER[[br]] ...[[br]] n-1 EPWMnSYNCPER
3	RESERVED	RO		Reserved
2	LOADMODE	RW	0h	DACVALA load mode. Determines when the DACVALA register is updated with the value from DACVALS.[[br]] [[br]] 0 Load on next SYSCLK[[br]] 1 Load on next EPWMSYNCPER specified by SYNCSEL
1	MODE	RW	0h	DAC gain mode select. Selects the gain mode for the buffered output. The MODE value is only used when DACREFSEL=1 and internal ADC reference mode is selected.[[br]] [[br]] 0 Gain is 1[[br]] 1 Gain is 2
0	DACREFSEL	RW	0h	DAC reference select. Selects which voltage references are used by the DAC.[[br]] [[br]] 0 VDAC/VSSA are the reference voltages[[br]] 1 ADC VREFHI/VSSA are the reference voltages

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3.6.3 CONTROLSS_DAC0_DACVALA Registers

3.6.3.1 DAC0_DACVALA Register (Offset = 4h) [reset = h]

Short Description: DAC Value Register - Active

Long Description:

Return to Summary Table

Table 3-304. Instance Table

Instance Name	Physical Address
CONTROLSS_DAC0	5026 0004h

Access Types Legend

Table 3-305. DACVALA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVALA	RO	0h	Active output code currently driven by the DAC

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3.6.4 CONTROLSS_DAC0_DACVALS Registers

3.6.4.1 DAC0_DACVALS Register (Offset = 6h) [reset = h]

Short Description: DAC Value Register - Shadow

Long Description:

Return to Summary Table

Table 3-306. Instance Table

Instance Name	Physical Address
CONTROLSS_DAC0	5026 0006h

Access Types Legend

Table 3-307. DACVALS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 0	DACVALS	RW	0h	Shadow output code to be loaded into DACVALA

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3.6.5 CONTROLSS_DAC0_DACOUTEN Registers

3.6.5.1 DAC0_DACOUTEN Register (Offset = 8h) [reset = h]

Short Description: DAC Output Enable Register

Long Description:

Return to Summary Table

Table 3-308. Instance Table

Instance Name	Physical Address
CONTROLSS_DAC0	5026 0008h

Access Types Legend

Table 3-309. DACOUTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 1	RESERVED	RO		Reserved
0	DACOUTEN	RW	0h	DAC output enable[[br]] [[br]] 0 DAC output is disabled[[br]] 1 DAC output is enabled

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3.6.6 CONTROLSS_DAC0_DACLOCK Registers

3.6.6.1 DAC0_DACLOCK Register (Offset = Ah) [reset = h]

Short Description: DAC Lock Register

Long Description:

Return to Summary Table

Table 3-310. Instance Table

Instance Name	Physical Address
CONTROLSS_DAC0	5026 000Ah

Access Types Legend

Table 3-311. DACLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	KEY	RW RRETURNS 0S	0h	Writes to this register succeed only if this field is written with a value of 0xA.[[br]] [[br]]Only 16-bit writes will succeed (provided the KEY matches). Read-modify-writes to individual bits in this register will be ignored.
11 - 3	RESERVED	RO		Reserved
2	DACOUTEN	RW SONCE	0h	Lock write-access to the DACOUTEN register.[[br]] [[br]] 0 DACOUTEN register is not locked. Write 0 to this bit has no effect. [[br]] 1 DACOUTEN register is locked. Only a system reset can clear this bit.
1	DACVAL	RW SONCE	0h	Lock write-access to the DACVALS register.[[br]] [[br]] 0 DACVALS register is not locked. Write 0 to this bit has no effect.[[br]] 1 DACVALS register is locked. Only a system reset can clear this bit.
0	DACCTL	RW SONCE	0h	Lock write-access to the DACCTL register.[[br]] [[br]] 0 DACCTL register is not locked. Write 0 to this bit has no effect.[[br]] 1 DACCTL register is locked. Only a system reset can clear this bit.

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3.6.7 CONTROLSS_DAC0_DACTRIM Registers

3.6.7.1 DAC0_DACTRIM Register (Offset = Ch) [reset = h]

Short Description: DAC Trim Register

Long Description:

Return to Summary Table

Table 3-312. Instance Table

Instance Name	Physical Address
CONTROLSS_DAC0	5026 000Ch

Access Types Legend

Table 3-313. DACTRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11 - 8	RESERVED	RW		DAC Gain Trim. This signed (two's complement) bit field is used to adjust the gain of the DAC. This register will be written with a factory set value during the device boot procedure.[[br]] [[br]] 1000 Gain is increased by the equivalent of 0.8%[[br]] ...[[br]] 1110 Gain is increased by the equivalent of 0.2% LSB[[br]] 1111 Gain is increased by the equivalent of 0.1% LSB[[br]] 0000 Gain is not adjusted[[br]] 0001 Gain is decreased by the equivalent of 0.1% LSB[[br]] 0010 Gain is decreased by the equivalent of 0.2% LSB[[br]] ...[[br]] 0111 Gain is decreased by the equivalent of 0.7% LSB
7 - 0	OFFSET_TRIM	RW	0h	DAC Offset Trim.[[br]] [[br]]This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of datasheet specifications.

3.6.8 Access Table

Table 3-314. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
RW RRETURNS0S	RW RRETURNS0S	Read returns 0s/Write
RW SONCE	RW SONCE	Read/Write (Set Once)

3.7 DMAXBAR Registers

Table 3-315. CONTROLSS_DMAXBAR Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_DMAXBAR Physical Address
0h	32	DMAXBAR_PID	502D 6000h
100h	8	DMAXBAR_DMAXBAR0_GSEL	502D 6100h
104h	8	DMAXBAR_DMAXBAR0_G0	502D 6104h
108h	8	DMAXBAR_DMAXBAR0_G1	502D 6108h
10Ch	8	DMAXBAR_DMAXBAR0_G2	502D 610Ch
110h	8	DMAXBAR_DMAXBAR0_G3	502D 6110h
114h	8	DMAXBAR_DMAXBAR0_G4	502D 6114h
118h	8	DMAXBAR_DMAXBAR0_G5	502D 6118h
140h	8	DMAXBAR_DMAXBAR1_GSEL	502D 6140h
144h	8	DMAXBAR_DMAXBAR1_G0	502D 6144h

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Table 3-315. CONTROLSS_DMAXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_DMAXBAR Physical Address
148h	8	DMAXBAR_DMAXBAR1_G1	502D 6148h
14Ch	8	DMAXBAR_DMAXBAR1_G2	502D 614Ch
150h	8	DMAXBAR_DMAXBAR1_G3	502D 6150h
154h	8	DMAXBAR_DMAXBAR1_G4	502D 6154h
158h	8	DMAXBAR_DMAXBAR1_G5	502D 6158h
180h	8	DMAXBAR_DMAXBAR2_GSEL	502D 6180h
184h	8	DMAXBAR_DMAXBAR2_G0	502D 6184h
188h	8	DMAXBAR_DMAXBAR2_G1	502D 6188h
18Ch	8	DMAXBAR_DMAXBAR2_G2	502D 618Ch
190h	8	DMAXBAR_DMAXBAR2_G3	502D 6190h
194h	8	DMAXBAR_DMAXBAR2_G4	502D 6194h
198h	8	DMAXBAR_DMAXBAR2_G5	502D 6198h
1C0h	8	DMAXBAR_DMAXBAR3_GSEL	502D 61C0h
1C4h	8	DMAXBAR_DMAXBAR3_G0	502D 61C4h
1C8h	8	DMAXBAR_DMAXBAR3_G1	502D 61C8h
1CCh	8	DMAXBAR_DMAXBAR3_G2	502D 61CCh
1D0h	8	DMAXBAR_DMAXBAR3_G3	502D 61D0h
1D4h	8	DMAXBAR_DMAXBAR3_G4	502D 61D4h
1D8h	8	DMAXBAR_DMAXBAR3_G5	502D 61D8h
200h	8	DMAXBAR_DMAXBAR4_GSEL	502D 6200h
204h	8	DMAXBAR_DMAXBAR4_G0	502D 6204h
208h	8	DMAXBAR_DMAXBAR4_G1	502D 6208h
20Ch	8	DMAXBAR_DMAXBAR4_G2	502D 620Ch
210h	8	DMAXBAR_DMAXBAR4_G3	502D 6210h
214h	8	DMAXBAR_DMAXBAR4_G4	502D 6214h
218h	8	DMAXBAR_DMAXBAR4_G5	502D 6218h
240h	8	DMAXBAR_DMAXBAR5_GSEL	502D 6240h
244h	8	DMAXBAR_DMAXBAR5_G0	502D 6244h
248h	8	DMAXBAR_DMAXBAR5_G1	502D 6248h
24Ch	8	DMAXBAR_DMAXBAR5_G2	502D 624Ch
250h	8	DMAXBAR_DMAXBAR5_G3	502D 6250h
254h	8	DMAXBAR_DMAXBAR5_G4	502D 6254h
258h	8	DMAXBAR_DMAXBAR5_G5	502D 6258h
280h	8	DMAXBAR_DMAXBAR6_GSEL	502D 6280h
284h	8	DMAXBAR_DMAXBAR6_G0	502D 6284h
288h	8	DMAXBAR_DMAXBAR6_G1	502D 6288h
28Ch	8	DMAXBAR_DMAXBAR6_G2	502D 628Ch
290h	8	DMAXBAR_DMAXBAR6_G3	502D 6290h
294h	8	DMAXBAR_DMAXBAR6_G4	502D 6294h
298h	8	DMAXBAR_DMAXBAR6_G5	502D 6298h
2C0h	8	DMAXBAR_DMAXBAR7_GSEL	502D 62C0h
2C4h	8	DMAXBAR_DMAXBAR7_G0	502D 62C4h
2C8h	8	DMAXBAR_DMAXBAR7_G1	502D 62C8h
2CCh	8	DMAXBAR_DMAXBAR7_G2	502D 62CCh
2D0h	8	DMAXBAR_DMAXBAR7_G3	502D 62D0h
2D4h	8	DMAXBAR_DMAXBAR7_G4	502D 62D4h

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Table 3-315. CONTROLSS_DMAXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_DMAXBAR Physical Address
2D8h	8	DMAXBAR_DMAXBAR7_G5	502D 62D8h
300h	8	DMAXBAR_DMAXBAR8_GSEL	502D 6300h
304h	8	DMAXBAR_DMAXBAR8_G0	502D 6304h
308h	8	DMAXBAR_DMAXBAR8_G1	502D 6308h
30Ch	8	DMAXBAR_DMAXBAR8_G2	502D 630Ch
310h	8	DMAXBAR_DMAXBAR8_G3	502D 6310h
314h	8	DMAXBAR_DMAXBAR8_G4	502D 6314h
318h	8	DMAXBAR_DMAXBAR8_G5	502D 6318h
340h	8	DMAXBAR_DMAXBAR9_GSEL	502D 6340h
344h	8	DMAXBAR_DMAXBAR9_G0	502D 6344h
348h	8	DMAXBAR_DMAXBAR9_G1	502D 6348h
34Ch	8	DMAXBAR_DMAXBAR9_G2	502D 634Ch
350h	8	DMAXBAR_DMAXBAR9_G3	502D 6350h
354h	8	DMAXBAR_DMAXBAR9_G4	502D 6354h
358h	8	DMAXBAR_DMAXBAR9_G5	502D 6358h
380h	8	DMAXBAR_DMAXBAR10_GSEL	502D 6380h
384h	8	DMAXBAR_DMAXBAR10_G0	502D 6384h
388h	8	DMAXBAR_DMAXBAR10_G1	502D 6388h
38Ch	8	DMAXBAR_DMAXBAR10_G2	502D 638Ch
390h	8	DMAXBAR_DMAXBAR10_G3	502D 6390h
394h	8	DMAXBAR_DMAXBAR10_G4	502D 6394h
398h	8	DMAXBAR_DMAXBAR10_G5	502D 6398h
3C0h	8	DMAXBAR_DMAXBAR11_GSEL	502D 63C0h
3C4h	8	DMAXBAR_DMAXBAR11_G0	502D 63C4h
3C8h	8	DMAXBAR_DMAXBAR11_G1	502D 63C8h
3CCh	8	DMAXBAR_DMAXBAR11_G2	502D 63CCh
3D0h	8	DMAXBAR_DMAXBAR11_G3	502D 63D0h
3D4h	8	DMAXBAR_DMAXBAR11_G4	502D 63D4h
3D8h	8	DMAXBAR_DMAXBAR11_G5	502D 63D8h
400h	8	DMAXBAR_DMAXBAR12_GSEL	502D 6400h
404h	8	DMAXBAR_DMAXBAR12_G0	502D 6404h
408h	8	DMAXBAR_DMAXBAR12_G1	502D 6408h
40Ch	8	DMAXBAR_DMAXBAR12_G2	502D 640Ch
410h	8	DMAXBAR_DMAXBAR12_G3	502D 6410h
414h	8	DMAXBAR_DMAXBAR12_G4	502D 6414h
418h	8	DMAXBAR_DMAXBAR12_G5	502D 6418h
440h	8	DMAXBAR_DMAXBAR13_GSEL	502D 6440h
444h	8	DMAXBAR_DMAXBAR13_G0	502D 6444h
448h	8	DMAXBAR_DMAXBAR13_G1	502D 6448h
44Ch	8	DMAXBAR_DMAXBAR13_G2	502D 644Ch
450h	8	DMAXBAR_DMAXBAR13_G3	502D 6450h
454h	8	DMAXBAR_DMAXBAR13_G4	502D 6454h
458h	8	DMAXBAR_DMAXBAR13_G5	502D 6458h
480h	8	DMAXBAR_DMAXBAR14_GSEL	502D 6480h
484h	8	DMAXBAR_DMAXBAR14_G0	502D 6484h
488h	8	DMAXBAR_DMAXBAR14_G1	502D 6488h

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Table 3-315. CONTROLSS_DMAXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_DMAXBAR Physical Address
48Ch	8	DMAXBAR_DMAXBAR14_G2	502D 648Ch
490h	8	DMAXBAR_DMAXBAR14_G3	502D 6490h
494h	8	DMAXBAR_DMAXBAR14_G4	502D 6494h
498h	8	DMAXBAR_DMAXBAR14_G5	502D 6498h
4C0h	8	DMAXBAR_DMAXBAR15_GSEL	502D 64C0h
4C4h	8	DMAXBAR_DMAXBAR15_G0	502D 64C4h
4C8h	8	DMAXBAR_DMAXBAR15_G1	502D 64C8h
4CCh	8	DMAXBAR_DMAXBAR15_G2	502D 64CCh
4D0h	8	DMAXBAR_DMAXBAR15_G3	502D 64D0h
4D4h	8	DMAXBAR_DMAXBAR15_G4	502D 64D4h
4D8h	8	DMAXBAR_DMAXBAR15_G5	502D 64D8h

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3.7.1 CONTROLSS_DMAXBAR_PID Registers

3.7.1.1 DMAXBAR_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

Return to Summary Table

Table 3-316. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6000h

Access Types Legend

Table 3-317. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	6180h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	2h	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	14h	Not Defined

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3.7.2 CONTROLSS_DMAXBARn_GSEL Registers

3.7.2.1 DMAXBARn_GSEL Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x100+0x40*n* where *n* goes from 0-15 (1)

Table 3-318. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6**N**h

Access Types Legend

Table 3-319. GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	GSEL	RW	0h	Select input source:0: G0 selected..5: G5 selected

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3.7.3 CONTROLSS_DMAXBARn_G0 Registers

3.7.3.1 DMAXBARn_G0 Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x104+0x40*n* where *n* goes from 0-15 (2)

Table 3-320. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6**N**h

Access Types Legend

Table 3-321. G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCA to corresponding xbar1: PWMx.SOCA is selected0: PWMx.SOCA is de-selected

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3.7.4 CONTROLSS_DMAXBARn_G1 Registers

3.7.4.1 DMAXBARn_G1 Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x108+0x40*n* where *n* goes from 0-15 (3)

Table 3-322. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6**N**h

Access Types Legend

Table 3-323. G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ETPWM SOCB to corresponding xbar1: PWMx.SOCB is selected0: PWMx.SOCB is de-selected

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3.7.5 CONTROLSS_DMAXBARn_G2 Registers

3.7.5.1 DMAXBARn_G2 Register (Offset = 10Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x10C+0x40*n* where *n* goes from 0-15 (4)

Table 3-324. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6**N**h

Access Types Legend

Table 3-325. G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	ADC DMA requests to corresponding xbar0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

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3.7.6 CONTROLSS_DMAXBARn_G3 Registers

3.7.6.1 DMAXBARn_G3 Register (Offset = 110h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x110+0x40*n* where *n* goes from 0-15 (5)

Table 3-326. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6**N**h

Access Types Legend

Table 3-327. G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	FSI DMA requests to corresponding xbar0: FSIRX0.RX_DMA_EVT1; FSIRX0_DMATRIG12: FSIRX0_DMATRIG23: FSIRX1.RX_DMA_EVT4; FSIRX1_DMATRIG15: FSIRX1_DMATRIG26: FSIRX2.RX_DMA_EVT7; FSIRX2_DMATRIG18: FSIRX2_DMATRIG29: FSIRX3.RX_DMA_EVT10; FSIRX3_DMATRIG111: FSIRX3_DMATRIG212: FSITX0.TX_DMA_EVT13: FSITX1.TX_DMA_EVT14: FSITX2.TX_DMA_EVT15: FSITX3.TX_DMA_EVT

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3.7.7 CONTROLSS_DMAXBARn_G4 Registers

3.7.7.1 DMAXBARn_G4 Register (Offset = 114h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x114+0x40*n* where *n* goes from 0-15 (6)

Table 3-328. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6**N**h

Access Types Legend

Table 3-329. G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	SDFM DMA requests to corresponding xbar0: SD0.FILT1.DRINT1: SD0.FILT2.DRINT2: SD0.FILT3.DRINT3: SD0.FILT4.DRINT4: SD1.FILT1.DRINT5: SD1.FILT2.DRINT6: SD1.FILT3.DRINT7: SD1.FILT4.DRINT

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3.7.8 CONTROLSS_DMAXBARn_G5 Registers

3.7.8.1 DMAXBARn_G5 Register (Offset = 118h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x118+0x40*n* where *n* goes from 0-15 (7)

Table 3-330. Instance Table

Instance Name	Physical Address
CONTROLSS_DMAXBAR	502D 6**N**h

Access Types Legend

Table 3-331. G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	SEL	RW	0h	ECAP DMA requests to corresponding xbar0: ECAP0.DMA_INT1: ECAP1.DMA_INT2: ECAP2.DMA_INT3: ECAP3.DMA_INT4: ECAP4.DMA_INT5: ECAP5.DMA_INT6: ECAP6.DMA_INT7: ECAP7.DMA_INT8: ECAP8.DMA_INT9: ECAP9.DMA_INT

3.7.9 Access Table

Table 3-332. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

3.8 ECAP Registers

Table 3-333. CONTROLSS_ECAP[0:2] Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_ECAP0 Physical Address	CONTROLSS_ECAP1 Physical Address	CONTROLSS_ECAP2 Physical Address
0h	32	ECAP_TSCTR	5024 0000h	5024 1000h	5024 2000h
4h	32	ECAP_CTRPHS	5024 0004h	5024 1004h	5024 2004h
8h	32	ECAP_CAP1	5024 0008h	5024 1008h	5024 2008h
Ch	32	ECAP_CAP2	5024 000Ch	5024 100Ch	5024 200Ch
10h	32	ECAP_CAP3	5024 0010h	5024 1010h	5024 2010h
14h	32	ECAP_CAP4	5024 0014h	5024 1014h	5024 2014h
24h	32	ECAP_ECCTL0	5024 0024h	5024 1024h	5024 2024h
28h	16	ECAP_ECCTL1	5024 0028h	5024 1028h	5024 2028h
2Ah	16	ECAP_ECCTL2	5024 002Ah	5024 102Ah	5024 202Ah
2Ch	16	ECAP_ECEINT	5024 002Ch	5024 102Ch	5024 202Ch
2Eh	16	ECAP_ECFLG	5024 002Eh	5024 102Eh	5024 202Eh
30h	16	ECAP_ECCLR	5024 0030h	5024 1030h	5024 2030h
32h	16	ECAP_ECFRC	5024 0032h	5024 1032h	5024 2032h
3Ch	32	ECAP_ECAPSYNCINSEL	5024 003Ch	5024 103Ch	5024 203Ch
80h	32	ECAP_MUNIT_COMMON_CTL	5024 0080h	5024 1080h	5024 2080h
C0h	32	ECAP_MUNIT_1_CTL	5024 00C0h	5024 10C0h	5024 20C0h

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Table 3-333. CONTROLSS_ECAP[0:2] Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_ECAP0 Physical Address	CONTROLSS_ECAP1 Physical Address	CONTROLSS_ECAP2 Physical Address
C4h	32	ECAP_MUNIT_1_SHADOW_CTL	5024 00C4h	5024 10C4h	5024 20C4h
D0h	32	ECAP_MUNIT_1_MIN	5024 00D0h	5024 10D0h	5024 20D0h
D4h	32	ECAP_MUNIT_1_MAX	5024 00D4h	5024 10D4h	5024 20D4h
D8h	32	ECAP_MUNIT_1_MIN_SHADOW	5024 00D8h	5024 10D8h	5024 20D8h
DCh	32	ECAP_MUNIT_1_MAX_SHADOW	5024 00DCh	5024 10DCh	5024 20DCh
E0h	32	ECAP_MUNIT_1_DEBUG_RANGE_MIN	5024 00E0h	5024 10E0h	5024 20E0h
E4h	32	ECAP_MUNIT_1_DEBUG_RANGE_MAX	5024 00E4h	5024 10E4h	5024 20E4h
100h	32	ECAP_MUNIT_2_CTL	5024 0100h	5024 1100h	5024 2100h
104h	32	ECAP_MUNIT_2_SHADOW_CTL	5024 0104h	5024 1104h	5024 2104h
110h	32	ECAP_MUNIT_2_MIN	5024 0110h	5024 1110h	5024 2110h
114h	32	ECAP_MUNIT_2_MAX	5024 0114h	5024 1114h	5024 2114h
118h	32	ECAP_MUNIT_2_MIN_SHADOW	5024 0118h	5024 1118h	5024 2118h
11Ch	32	ECAP_MUNIT_2_MAX_SHADOW	5024 011Ch	5024 111Ch	5024 211Ch
120h	32	ECAP_MUNIT_2_DEBUG_RANGE_MIN	5024 0120h	5024 1120h	5024 2120h
124h	32	ECAP_MUNIT_2_DEBUG_RANGE_MAX	5024 0124h	5024 1124h	5024 2124h

Table 3-334. CONTROLSS_ECAP[3:5] Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_ECAP3 Physical Address	CONTROLSS_ECAP4 Physical Address	CONTROLSS_ECAP5 Physical Address
0h	32	ECAP_TSCTR	5024 3000h	5024 4000h	5024 5000h
4h	32	ECAP_CTRPHS	5024 3004h	5024 4004h	5024 5004h
8h	32	ECAP_CAP1	5024 3008h	5024 4008h	5024 5008h
Ch	32	ECAP_CAP2	5024 300Ch	5024 400Ch	5024 500Ch
10h	32	ECAP_CAP3	5024 3010h	5024 4010h	5024 5010h
14h	32	ECAP_CAP4	5024 3014h	5024 4014h	5024 5014h
24h	32	ECAP_ECCTL0	5024 3024h	5024 4024h	5024 5024h
28h	16	ECAP_ECCTL1	5024 3028h	5024 4028h	5024 5028h
2Ah	16	ECAP_ECCTL2	5024 302Ah	5024 402Ah	5024 502Ah
2Ch	16	ECAP_ECEINT	5024 302Ch	5024 402Ch	5024 502Ch
2Eh	16	ECAP_ECFLG	5024 302Eh	5024 402Eh	5024 502Eh
30h	16	ECAP_ECCLR	5024 3030h	5024 4030h	5024 5030h
32h	16	ECAP_ECFRC	5024 3032h	5024 4032h	5024 5032h
3Ch	32	ECAP_ECAPSYNCINSEL	5024 303Ch	5024 403Ch	5024 503Ch
80h	32	ECAP_MUNIT_COMMON_CTL	5024 3080h	5024 4080h	5024 5080h
C0h	32	ECAP_MUNIT_1_CTL	5024 30C0h	5024 40C0h	5024 50C0h
C4h	32	ECAP_MUNIT_1_SHADOW_CTL	5024 30C4h	5024 40C4h	5024 50C4h
D0h	32	ECAP_MUNIT_1_MIN	5024 30D0h	5024 40D0h	5024 50D0h
D4h	32	ECAP_MUNIT_1_MAX	5024 30D4h	5024 40D4h	5024 50D4h
D8h	32	ECAP_MUNIT_1_MIN_SHADOW	5024 30D8h	5024 40D8h	5024 50D8h
DCh	32	ECAP_MUNIT_1_MAX_SHADOW	5024 30DCh	5024 40DCh	5024 50DCh
E0h	32	ECAP_MUNIT_1_DEBUG_RANGE_MIN	5024 30E0h	5024 40E0h	5024 50E0h
E4h	32	ECAP_MUNIT_1_DEBUG_RANGE_MAX	5024 30E4h	5024 40E4h	5024 50E4h

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Table 3-334. CONTROLSS_ECAP[3:5] Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_ECAP3 Physical Address	CONTROLSS_ECAP4 Physical Address	CONTROLSS_ECAP5 Physical Address
100h	32	ECAP_MUNIT_2_CTL	5024 3100h	5024 4100h	5024 5100h
104h	32	ECAP_MUNIT_2_SHADOW_CTL	5024 3104h	5024 4104h	5024 5104h
110h	32	ECAP_MUNIT_2_MIN	5024 3110h	5024 4110h	5024 5110h
114h	32	ECAP_MUNIT_2_MAX	5024 3114h	5024 4114h	5024 5114h
118h	32	ECAP_MUNIT_2_MIN_SHADOW	5024 3118h	5024 4118h	5024 5118h
11Ch	32	ECAP_MUNIT_2_MAX_SHADOW	5024 311Ch	5024 411Ch	5024 511Ch
120h	32	ECAP_MUNIT_2_DEBUG_RANGE_MIN	5024 3120h	5024 4120h	5024 5120h
124h	32	ECAP_MUNIT_2_DEBUG_RANGE_MAX	5024 3124h	5024 4124h	5024 5124h

Table 3-335. CONTROLSS_ECAP[6:8] Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_ECAP6 Physical Address	CONTROLSS_ECAP7 Physical Address	CONTROLSS_ECAP8 Physical Address
0h	32	ECAP_TSCTR	5024 6000h	5024 7000h	5024 8000h
4h	32	ECAP_CTRPHS	5024 6004h	5024 7004h	5024 8004h
8h	32	ECAP_CAP1	5024 6008h	5024 7008h	5024 8008h
Ch	32	ECAP_CAP2	5024 600Ch	5024 700Ch	5024 800Ch
10h	32	ECAP_CAP3	5024 6010h	5024 7010h	5024 8010h
14h	32	ECAP_CAP4	5024 6014h	5024 7014h	5024 8014h
24h	32	ECAP_ECCTL0	5024 6024h	5024 7024h	5024 8024h
28h	16	ECAP_ECCTL1	5024 6028h	5024 7028h	5024 8028h
2Ah	16	ECAP_ECCTL2	5024 602Ah	5024 702Ah	5024 802Ah
2Ch	16	ECAP_ECEINT	5024 602Ch	5024 702Ch	5024 802Ch
2Eh	16	ECAP_ECFLG	5024 602Eh	5024 702Eh	5024 802Eh
30h	16	ECAP_ECCLR	5024 6030h	5024 7030h	5024 8030h
32h	16	ECAP_ECFRC	5024 6032h	5024 7032h	5024 8032h
3Ch	32	ECAP_ECAPSYNCINSEL	5024 603Ch	5024 703Ch	5024 803Ch
80h	32	ECAP_MUNIT_COMMON_CTL	5024 6080h	5024 7080h	5024 8080h
C0h	32	ECAP_MUNIT_1_CTL	5024 60C0h	5024 70C0h	5024 80C0h
C4h	32	ECAP_MUNIT_1_SHADOW_CTL	5024 60C4h	5024 70C4h	5024 80C4h
D0h	32	ECAP_MUNIT_1_MIN	5024 60D0h	5024 70D0h	5024 80D0h
D4h	32	ECAP_MUNIT_1_MAX	5024 60D4h	5024 70D4h	5024 80D4h
D8h	32	ECAP_MUNIT_1_MIN_SHADOW	5024 60D8h	5024 70D8h	5024 80D8h
DCh	32	ECAP_MUNIT_1_MAX_SHADOW	5024 60DCh	5024 70DCh	5024 80DCh
E0h	32	ECAP_MUNIT_1_DEBUG_RANGE_MIN	5024 60E0h	5024 70E0h	5024 80E0h
E4h	32	ECAP_MUNIT_1_DEBUG_RANGE_MAX	5024 60E4h	5024 70E4h	5024 80E4h
100h	32	ECAP_MUNIT_2_CTL	5024 6100h	5024 7100h	5024 8100h
104h	32	ECAP_MUNIT_2_SHADOW_CTL	5024 6104h	5024 7104h	5024 8104h
110h	32	ECAP_MUNIT_2_MIN	5024 6110h	5024 7110h	5024 8110h
114h	32	ECAP_MUNIT_2_MAX	5024 6114h	5024 7114h	5024 8114h
118h	32	ECAP_MUNIT_2_MIN_SHADOW	5024 6118h	5024 7118h	5024 8118h
11Ch	32	ECAP_MUNIT_2_MAX_SHADOW	5024 611Ch	5024 711Ch	5024 811Ch
120h	32	ECAP_MUNIT_2_DEBUG_RANGE_MIN	5024 6120h	5024 7120h	5024 8120h

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Table 3-335. CONTROLSS_ECAP[6:8] Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_ECAP6 Physical Address	CONTROLSS_ECAP7 Physical Address	CONTROLSS_ECAP8 Physical Address
124h	32	ECAP_MUNIT_2_DEBUG_RANGE_MAX	5024 6124h	5024 7124h	5024 8124h

Table 3-336. CONTROLSS_ECAP9 Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_ECAP9 Physical Address
0h	32	ECAP_TSCTR	5024 9000h
4h	32	ECAP_CTRPHS	5024 9004h
8h	32	ECAP_CAP1	5024 9008h
Ch	32	ECAP_CAP2	5024 900Ch
10h	32	ECAP_CAP3	5024 9010h
14h	32	ECAP_CAP4	5024 9014h
24h	32	ECAP_ECCTL0	5024 9024h
28h	16	ECAP_ECCTL1	5024 9028h
2Ah	16	ECAP_ECCTL2	5024 902Ah
2Ch	16	ECAP_ECEINT	5024 902Ch
2Eh	16	ECAP_ECFLG	5024 902Eh
30h	16	ECAP_ECCLR	5024 9030h
32h	16	ECAP_ECFRC	5024 9032h
3Ch	32	ECAP_ECAPSYNCINSEL	5024 903Ch
80h	32	ECAP_MUNIT_COMMON_CTL	5024 9080h
C0h	32	ECAP_MUNIT_1_CTL	5024 90C0h
C4h	32	ECAP_MUNIT_1_SHADOW_CTL	5024 90C4h
D0h	32	ECAP_MUNIT_1_MIN	5024 90D0h
D4h	32	ECAP_MUNIT_1_MAX	5024 90D4h
D8h	32	ECAP_MUNIT_1_MIN_SHADOW	5024 90D8h
DCh	32	ECAP_MUNIT_1_MAX_SHADOW	5024 90DCh
E0h	32	ECAP_MUNIT_1_DEBUG_RANGE_MIN	5024 90E0h
E4h	32	ECAP_MUNIT_1_DEBUG_RANGE_MAX	5024 90E4h
100h	32	ECAP_MUNIT_2_CTL	5024 9100h
104h	32	ECAP_MUNIT_2_SHADOW_CTL	5024 9104h
110h	32	ECAP_MUNIT_2_MIN	5024 9110h
114h	32	ECAP_MUNIT_2_MAX	5024 9114h
118h	32	ECAP_MUNIT_2_MIN_SHADOW	5024 9118h
11Ch	32	ECAP_MUNIT_2_MAX_SHADOW	5024 911Ch
120h	32	ECAP_MUNIT_2_DEBUG_RANGE_MIN	5024 9120h
124h	32	ECAP_MUNIT_2_DEBUG_RANGE_MAX	5024 9124h

3.8.1 ECAP Instance Count Note

Note

n = 0 to 9 for the ECAP registers defined below.

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3.8.2 CONTROLSS_ECAPn_TSCTR Registers

3.8.2.1 ECAPn_TSCTR Register (Offset = 0h) [reset = h]

Short Description: Time-Stamp Counter

Long Description:

Return to Summary Table

Table 3-337. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0000h
CONTROLSS_ECAP1	5024 1000h
CONTROLSS_ECAP2	5024 2000h
CONTROLSS_ECAP3	5024 3000h
CONTROLSS_ECAP4	5024 4000h
CONTROLSS_ECAP5	5024 5000h
CONTROLSS_ECAP6	5024 6000h
CONTROLSS_ECAP7	5024 7000h
CONTROLSS_ECAP8	5024 8000h
CONTROLSS_ECAP9	5024 9000h

Access Types Legend

Table 3-338. TSCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TSCTR	RW	0h	Active 32-bit counter register that is used as the capture time-base HR mode : 1) This register reads HRCOUNTER value and is not writable 2) can be reset using CTRFILTRESET 3) Its not synchronized to SYSCLK domain so reads may not be accurate

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3.8.3 CONTROLSS_ECAPn_CTRPHS Registers

3.8.3.1 ECAPn_CTRPHS Register (Offset = 4h) [reset = h]

Short Description: Counter Phase Offset Value Register

Long Description:

Return to Summary Table

Table 3-339. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0004h
CONTROLSS_ECAP1	5024 1004h
CONTROLSS_ECAP2	5024 2004h
CONTROLSS_ECAP3	5024 3004h
CONTROLSS_ECAP4	5024 4004h
CONTROLSS_ECAP5	5024 5004h
CONTROLSS_ECAP6	5024 6004h
CONTROLSS_ECAP7	5024 7004h
CONTROLSS_ECAP8	5024 8004h
CONTROLSS_ECAP9	5024 9004h

Access Types Legend

Table 3-340. CTRPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CTRPHS	RW	0h	Counter phase value register that can be programmed for phase lag/lead. This register CTRPHS is loaded into TSCTR upon either a SYNCI event or S/W force via a control bit. Used to achieve phase control synchronization with respect to other eCAP and EPWM time-bases. This register is not applicable in HR mode.

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3.8.4 CONTROLSS_ECAPn_CAP1 Registers

3.8.4.1 ECAPn_CAP1 Register (Offset = 8h) [reset = h]

Short Description: Capture 1 Register

Long Description:

Return to Summary Table

Table 3-341. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0008h
CONTROLSS_ECAP1	5024 1008h
CONTROLSS_ECAP2	5024 2008h
CONTROLSS_ECAP3	5024 3008h
CONTROLSS_ECAP4	5024 4008h
CONTROLSS_ECAP5	5024 5008h
CONTROLSS_ECAP6	5024 6008h
CONTROLSS_ECAP7	5024 7008h
CONTROLSS_ECAP8	5024 8008h
CONTROLSS_ECAP9	5024 9008h

Access Types Legend

Table 3-342. CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAP1	RW	0h	This register can be loaded (written) by: - Time-Stamp counter value (TSCTR) during a capture event - Software - may be useful for test purposes or initialization - ARPD shadow register (CAP3) when used in APWM mode

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3.8.5 CONTROLSS_ECAPn_CAP2 Registers

3.8.5.1 ECAPn_CAP2 Register (Offset = Ch) [reset = h]

Short Description: Capture 2 Register

Long Description:

Return to Summary Table

Table 3-343. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 000Ch
CONTROLSS_ECAP1	5024 100Ch
CONTROLSS_ECAP2	5024 200Ch
CONTROLSS_ECAP3	5024 300Ch
CONTROLSS_ECAP4	5024 400Ch
CONTROLSS_ECAP5	5024 500Ch
CONTROLSS_ECAP6	5024 600Ch
CONTROLSS_ECAP7	5024 700Ch
CONTROLSS_ECAP8	5024 800Ch
CONTROLSS_ECAP9	5024 900Ch

Access Types Legend

Table 3-344. CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAP2	RW	0h	This register can be loaded (written) by: - Time-Stamp (counter value) during a capture event - Software - may be useful for test purposes - ACMP shadow register (CAP4) when used in APWM mode

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3.8.6 CONTROLSS_ECAPn_CAP3 Registers

3.8.6.1 ECAPn_CAP3 Register (Offset = 10h) [reset = h]

Short Description: Capture 3 Register

Long Description:

Return to Summary Table

Table 3-345. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0010h
CONTROLSS_ECAP1	5024 1010h
CONTROLSS_ECAP2	5024 2010h
CONTROLSS_ECAP3	5024 3010h
CONTROLSS_ECAP4	5024 4010h
CONTROLSS_ECAP5	5024 5010h
CONTROLSS_ECAP6	5024 6010h
CONTROLSS_ECAP7	5024 7010h
CONTROLSS_ECAP8	5024 8010h
CONTROLSS_ECAP9	5024 9010h

Access Types Legend

Table 3-346. CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAP3	RW	0h	In CMP mode, this is a time-stamp capture register. In APWM mode, this is the period shadow (APRD) register. You can update the PWM period value through this register. CAP3 (APRD) shadows CAP1 in this mode.

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3.8.7 CONTROLSS_ECAPn_CAP4 Registers

3.8.7.1 ECAPn_CAP4 Register (Offset = 14h) [reset = h]

Short Description: Capture 4 Register

Long Description:

Return to Summary Table

Table 3-347. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0014h
CONTROLSS_ECAP1	5024 1014h
CONTROLSS_ECAP2	5024 2014h
CONTROLSS_ECAP3	5024 3014h
CONTROLSS_ECAP4	5024 4014h
CONTROLSS_ECAP5	5024 5014h
CONTROLSS_ECAP6	5024 6014h
CONTROLSS_ECAP7	5024 7014h
CONTROLSS_ECAP8	5024 8014h
CONTROLSS_ECAP9	5024 9014h

Access Types Legend

Table 3-348. CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAP4	RW	0h	In CMP mode, this is a time-stamp capture register. In APWM mode, this is the compare shadow (ACMP) register. You can update the PWM compare value via this register. CAP4 (ACMP) shadows CAP2 in this mode.

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3.8.8 CONTROLSS_ECAPn_ECCTL0 Registers

3.8.8.1 ECAPn_ECCTL0 Register (Offset = 24h) [reset = h]

Short Description: Capture Control Register 0

Long Description:

Return to Summary Table

Table 3-349. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0024h
CONTROLSS_ECAP1	5024 1024h
CONTROLSS_ECAP2	5024 2024h
CONTROLSS_ECAP3	5024 3024h
CONTROLSS_ECAP4	5024 4024h
CONTROLSS_ECAP5	5024 5024h
CONTROLSS_ECAP6	5024 6024h
CONTROLSS_ECAP7	5024 7024h
CONTROLSS_ECAP8	5024 8024h
CONTROLSS_ECAP9	5024 9024h

Access Types Legend

Table 3-350. ECCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 18	RESERVED	RO RRETURNS 0S		Reserved
17 - 16	SOCEVTSEL	RW	0h	ADC SOC event select Capture Mode: 00b (R/W) = SOC trigger source is CEVT1 01b (R/W) = SOC trigger source is CEVT2 10b (R/W) = SOC trigger source is CEVT3 11b (R/W) = SOC trigger source is CEVT4 APWM Mode: 00b (R/W) = SOC trigger interrupt source is period match 01b (R/W) = SOC trigger interrupt source is compare match 10b (R/W) = SOC trigger interrupt source is period match or compare match 11b (R/W) = Disabled
15 - 12	QUALPRD	RW	0h	Qual period to filter out noise on input signals being monitored, Not applicable for HR mode. 0x0 : Bypass 0x1 : pulses of with 1 cycle or less will be filtered out 0x2 : pulses of with 2 cycles or less will be filtered out .... 0xF : pulses of with 15 cycles or less will be filtered out
11 - 8	RESERVED	RO RRETURNS 0S		Reserved
7 - 0	INPUTSEL	RW	FFh	Capture input source select bits 0x0 capture input is ECAPxINPUT[0] 0x1 capture input is ECAPxINPUT[1] 0x2 capture input is ECAPxINPUT[2] ... 0xFF capture input is ECAPxINPUT[256]

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3.8.9 CONTROLSS_ECAPn_ECCTL1 Registers

3.8.9.1 ECAPn_ECCTL1 Register (Offset = 28h) [reset = h]

Short Description: Capture Control Register 1

Long Description:

Return to Summary Table

Table 3-351. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0028h
CONTROLSS_ECAP1	5024 1028h
CONTROLSS_ECAP2	5024 2028h
CONTROLSS_ECAP3	5024 3028h
CONTROLSS_ECAP4	5024 4028h
CONTROLSS_ECAP5	5024 5028h
CONTROLSS_ECAP6	5024 6028h
CONTROLSS_ECAP7	5024 7028h
CONTROLSS_ECAP8	5024 8028h
CONTROLSS_ECAP9	5024 9028h

Access Types Legend

Table 3-352. ECCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	FREE_SOFT	RW	0h	Emulation Control 0x0 | ECAP_STOP_EMUTSCTR counter stops immediately on emulation suspend 0x1 | ECAP_RUNS_UNTILTSCTR counter runs until = 0 0x2 | ECAP_UNAF_EMU_SUSTSCTR counter is unaffected by emulation suspend (Run Free) 0x3 | ECAP_UNAF_EMU_SUS2TSCTR counter is unaffected by emulation suspend (Run Free)
13 - 9	PRESCALE	RW	0h	Event Filter prescale select 0x00 | ECAP_DIV1Divide by 1 (i.e,. no prescale, by-pass the prescaler) 0x01 | ECAP_DIV2Divide by 2 0x02 | ECAP_DIV4Divide by 4 0x03 | ECAP_DIV6Divide by 6 0x04 | ECAP_DIV8Divide by 8 0x05 | ECAP_DIV10Divide by 10 0x1E | ECAP_DIV60Divide by 60 0x1F | ECAP_DIV62Divide by 62
8	CAPLDEN	RW	0h	Enable Loading of CAP1-4 registers on a capture event. Note that this bit does not disable CEVTn events from being generated. 0 | ECAP_DISABLEDisable CAP1-4 register loads at capture event time. 1 | ECAP_ENABLEEnable CAP1-4 register loads at capture event time.
7	CTRRST4	RW	0h	Counter Reset on Capture Event 4 0 | ECAP_DO_NOT_RESET_EVENT4Do not reset counter on Capture Event 4 (absolute time stamp operation) 1 | ECAP_RESET_EVENT4Reset counter after Capture Event 4 time-stamp has been captured (used in difference mode operation)
6	CAP4POL	RW	0h	Capture Event 4 Polarity select 0 | ECAP_CAP_EVENT4_RISECapture Event 4 triggered on a rising edge (RE) 1 | ECAP_CAP_EVENT4_FALLCapture Event 4 triggered on a falling edge (FE)
5	CTRRST3	RW	0h	Counter Reset on Capture Event 3 0 | ECAP_DO_NOT_RESET_EVENT3Do not reset counter on Capture Event 3 (absolute time stamp) 1 | ECAP_RESET_EVENT3Reset counter after Event 3 time-stamp has been captured (used in difference mode operation)

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Table 3-352. ECCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CAP3POL	RW	0h	Capture Event 3 Polarity select 0 | ECAP_CAP_EVENT3_RISECapture Event 3 triggered on a rising edge (RE) 1 | ECAP_CAP_EVENT3_FALLCapture Event 3 triggered on a falling edge (FE)
3	CTRRST2	RW	0h	Counter Reset on Capture Event 2 0 | ECAP_DO_NOT_RESET_EVENT2Do not reset counter on Capture Event 2 (absolute time stamp) 1 | ECAP_RESET_EVENT2Reset counter after Event 2 time-stamp has been captured (used in difference mode operation)
2	CAP2POL	RW	0h	Capture Event 2 Polarity select 0 | ECAP_CAP_EVENT2_RISECapture Event 2 triggered on a rising edge (RE) 1 | ECAP_CAP_EVENT2_FALLCapture Event 2 triggered on a falling edge (FE)
1	CTRRST1	RW	0h	Counter Reset on Capture Event 1 0 | ECAP_DO_NOT_RESET_EVENT1Do not reset counter on Capture Event 1 (absolute time stamp) 1 | ECAP_RESET_EVENT1Reset counter after Event 1 time-stamp has been captured (used in difference mode operation)
0	CAP1POL	RW	0h	Capture Event 1 Polarity select 0 | ECAP_CAP_EVENT1_RISECapture Event 1 triggered on a rising edge (RE) 1 | ECAP_CAP_EVENT1_FALLCapture Event 1 triggered on a falling edge (FE)

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3.8.10 CONTROLSS_ECAPn_ECCTL2 Registers

3.8.10.1 ECAPn_ECCTL2 Register (Offset = 2Ah) [reset = h]

Short Description: Capture Control Register 2

Long Description:

Return to Summary Table

Table 3-353. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 002Ah
CONTROLSS_ECAP1	5024 102Ah
CONTROLSS_ECAP2	5024 202Ah
CONTROLSS_ECAP3	5024 302Ah
CONTROLSS_ECAP4	5024 402Ah
CONTROLSS_ECAP5	5024 502Ah
CONTROLSS_ECAP6	5024 602Ah
CONTROLSS_ECAP7	5024 702Ah
CONTROLSS_ECAP8	5024 802Ah
CONTROLSS_ECAP9	5024 902Ah

Access Types Legend

Table 3-354. ECCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	MODCNTRSTS	RW	0h	This bit field reads current status on modulo counter 00b (R) = CAP1 register gets loaded on next capture event. 01b (R) = CAP2 register gets loaded on next capture event. 10b (R) = CAP3 register gets loaded on next capture event. 11b (R) = CAP4 register gets loaded on next capture event.
13 - 12	DMAEVTSEL	RW	0h	DMA event select Capture Mode: 00b (R/W) = DMA interrupt source is CEVT1 01b (R/W) = DMA interrupt source is CEVT2 10b (R/W) = DMA interrupt source is CEVT3 11b (R/W) = DMA interrupt source is CEVT4 APWM Mode: 00b (R/W) = DMA interrupt source is period match 01b (R/W) = DMA interrupt source is compare match 10b (R/W) = DMA interrupt source is period match or compare match 11b (R/W) = Disabled
11	CTRFILTRESET	RW RRETURNS 0S	0h	Reset Bit 0h (R) = No effect 1h (W) = Resets event filter, counter, modulo counter and CEVT[1,2,3,4] and CNTOVF , HRERROR flags Note: This provides an ability start capture module from known state in case spurious inputs are captured while ECAP is configured.
10	APWMPOL	RW	0h	APWM output polarity select. This is applicable only in APWM operating mode. 0 | ECAP_OUTPUT_ACTIVE_HIGHOutput is active high (Compare value defines high time) 1 | ECAP_OUTPUT_ACTIVE_LOWOutput is active low (Compare value defines low time)
9	CAP_APWM	RW	0h	CAP/APWM operating mode select 0 | ECAP_MODULEECAP module operates in capture mode. This mode forces the following configuration: - Inhibits TSCTR resets via CTR = PRD event - Inhibits shadow loads on CAP1 and 2 registers - Permits user to enable CAP1-4 register load - CAPx/APWMx pin operates as a capture input 1 | ECAP_MODULE_APWMECAP module operates in APWM mode. This mode forces the following configuration: - Resets TSCTR on CTR = PRD event (period boundary - Permits shadow loading on CAP1 and 2 registers - Disables loading of time-stamps into CAP1-4 registers - CAPx/APWMx pin operates as a APWM output

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Table 3-354. ECCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SWSYNC	RW RRETURNS 0S	0h	Software-forced Counter (TSCTR) Synchronizer. This provides the user a method to generate a synchronization pulse through software. In APWM mode, the synchronization pulse can also be sourced from the CTR = PRD event. 0 | ECAP_ZERO_NOEFFECTWriting a zero has no effect. Reading always returns a zero 1 | ECAP_WRITE_TSCTRWriting a one forces a TSCTR shadow load of current ECAP module and any ECAP modules down-stream providing the SYNCO_SEL bits are 0,0. After writing a 1, this bit returns to a zero. Note: Selection CTR = PRD is meaningful only in APWM mode; however, you can choose it in CAP mode if you find doing so useful.
7 - 6	SYNCO_SEL	RW	0h	Sync-Out Select 0x0 | SWSYNCsync out signal is SWSYNC 0x1 | ECAP_CTR_PRD_TO_SYNCOUTSelect CTR = PRD event to be the sync-out signal 0x2 | ECAP_DISABLE_SYNC_OUTDisable sync out signal 0x3 | ECAP_DISABLE_SYNC_OUTDisable sync out signal
5	SYNCI_EN	RW	0h	Counter (TSCTR) Sync-In select mode 0 | ECAP_DISABLE_SYNC_INDisable sync-in option 1 | ECAP_ENABLE_COUNTER_REGISTEREnable counter (TSCTR) to be loaded from CTRPHS register upon either a SYNCI signal or a S/W force event.
4	TSCTRSTOP	RW	0h	Time Stamp (TSCTR) Counter Stop (freeze) Control 0 | ECAP_TSCTR_STOPPEDTSCTR stopped 1 | ECAP_TSCTR_FREE_RUNNINGTSCTR free-running
3	REARM	RW RRETURNS 0S	0h	Re-Arming Control. Note: The re-arm function is valid in one shot or continuous mode 0 | ECAP_NO_EFFECT_RETURNS_0Has no effect (reading always returns a 0) 1 | ECAP_ARMS_ONESHOTArms the one-shot sequence as follows: 1) Resets the Mod4 counter to zero 2) Unfreezes the Mod4 counter 3) Enables capture register loads
2 - 1	STOP_WRAP	RW	Bh	Stop value for one-shot mode. This is the number (between 1-4) of captures allowed to occur before the CAP(1-4) registers are frozen, that is, capture sequence is stopped. Wrap value for continuous mode. This is the number (between 1-4) of the capture register in which the circular buffer wraps around and starts again. Notes: STOP_WRAP is compared to Mod4 counter and, when equal, 2 actions occur: - Mod4 counter is stopped (frozen) - Capture register loads are inhibited In one-shot mode, further interrupt events are blocked until re-armed. 0x0 | ECAP_STOPEVENT1_WRAPEVENT2Stop after Capture Event 1 in one-shot mode Wrap after Capture Event 1 in continuous mode. 0x1 | ECAP_STOPEVENT2_WRAPEVENT2Stop after Capture Event 2 in one-shot mode Wrap after Capture Event 2 in continuous mode. 0x2 | ECAP_STOPEVENT3_WRAPEVENT2Stop after Capture Event 3 in one-shot mode Wrap after Capture Event 3 in continuous mode. 0x3 | ECAP_STOPEVENT4_WRAPEVENT2Stop after Capture Event 4 in one-shot mode Wrap after Capture Event 4 in continuous mode.
0	CONT_ONESHT	RW	0h	Continuous or one-shot mode control (applicable only in capture mode) 0 | ECAP_OPP_CONTOperate in continuous mode 1 | ECAP_OPP_ONEOperate in one-Shot mode

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3.8.11 CONTROLSS_ECAPn_ECEINT Registers

3.8.11.1 ECAPn_ECEINT Register (Offset = 2Ch) [reset = h]

Short Description: The interrupt enable bits (CEVT1, ...) block any of the selected events from generating an interrupt. Events will still be latched into the flag bit (ECFLG register) and can be forced/cleared via the ECFRC/ECCLR registers. The proper procedure for configuring peripheral modes and interrupts is as follows: - Disable global interrupts - Stop eCAP counter - Disable eCAP interrupts - Configure peripheral registers - Clear spurious eCAP interrupt flags - Enable eCAP interrupts - Start eCAP counter - Enable global interrupts

Long Description:

Return to Summary Table

Table 3-355. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 002Ch
CONTROLSS_ECAP1	5024 102Ch
CONTROLSS_ECAP2	5024 202Ch
CONTROLSS_ECAP3	5024 302Ch
CONTROLSS_ECAP4	5024 402Ch
CONTROLSS_ECAP5	5024 502Ch
CONTROLSS_ECAP6	5024 602Ch
CONTROLSS_ECAP7	5024 702Ch
CONTROLSS_ECAP8	5024 802Ch
CONTROLSS_ECAP9	5024 902Ch

Access Types Legend

Table 3-356. ECEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	MUNIT_2_ERROR_EVT2	RW	0h	Monitoring unit 2 error event 2 interrupt enable 0 : Disable Monitoring unit 2 error event 2 interrupt 1 : Enable Monitoring unit 2 error event 2 interrupt
11	MUNIT_2_ERROR_EVT1	RW	0h	Monitoring unit 2 error event 2 interrupt enable 0 : Disable Monitoring unit 2 error event 1 interrupt 1 : Enable Monitoring unit 2 error event 1 interrupt
10	MUNIT_1_ERROR_EVT2	RW	0h	Monitoring unit 1 error event 1 interrupt enable 0 : Disable Monitoring unit 1 error event 2 interrupt 1 : Enable Monitoring unit 1 error event 2 interrupt
9	MUNIT_1_ERROR_EVT1	RW	0h	Monitoring unit 1 error event 1 interrupt enable 0 : Disable Monitoring unit 1 error event 1 interrupt 1 : Enable Monitoring unit 1 error event 1 interrupt
8	HRERROR	RW	0h	High resolution error interrupt enable 0 | ECAP_DISAB_HRERROR_INTERRUPTDisable High Resolution Error as an Interrupt source 1 | ECAP_ENAB_HRERROR_INTERRUPTEnable High Resolution Error as an Interrupt source
7	CTR_EQ_CMP	RW	0h	Counter Equal Compare Interrupt Enable 0 | ECAP_DISAB_CE_INTERRUPTDisable Compare Equal as an Interrupt source 1 | ECAP_ENAB_CE_INTERRUPTEnable Compare Equal as an Interrupt source
6	CTR_EQ_PRD	RW	0h	Counter Equal Period Interrupt Enable 0 | ECAP_DISAB_PE_INTERRUPTDisable Period Equal as an Interrupt source 1 | ECAP_ENAB_PE_INTERRUPTEnable Period Equal as an Interrupt source

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Table 3-356. ECEINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CTROVF	RW	0h	Counter Overflow Interrupt Enable 0 | ECAP_DISAB_CO_INTERRUPTDisabled counter Overflow as an Interrupt source 1 | ECAP_ENAB_CO_INTERRUPTEnable counter Overflow as an Interrupt source
4	CEVT4	RW	0h	Capture Event 4 Interrupt Enable 0 | ECAP_DISAB_CAP4_INTERRUPTDisable Capture Event 4 as an Interrupt source 1 | ECAP_ENAB_CAP4_INTERRUPTCapture Event 4 Interrupt Enable
3	CEVT3	RW	0h	Capture Event 3 Interrupt Enable 0 | ECAP_DISAB_CAP3_INTERRUPTDisable Capture Event 3 as an Interrupt source 1 | ECAP_ENAB_CAP3_INTERRUPTEnable Capture Event 3 as an Interrupt source
2	CEVT2	RW	0h	Capture Event 2 Interrupt Enable 0 | ECAP_DISAB_CAP2_INTERRUPTDisable Capture Event 2 as an Interrupt source 1 | ECAP_ENAB_CAP2_INTERRUPTEnable Capture Event 2 as an Interrupt source
1	CEVT1	RW	0h	Capture Event 1 Interrupt Enable 0 | ECAP_DISAB_CAP1_INTERRUPTDisable Capture Event 1 as an Interrupt source 1 | ECAP_ENAB_CAP1_INTERRUPTEnable Capture Event 1 as an Interrupt source
0	RESERVED	RO		Reserved

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3.8.12 CONTROLSS_ECAPn_ECFLG Registers

3.8.12.1 ECAPn_ECFLG Register (Offset = 2Eh) [reset = h]

Short Description: Capture Interrupt Flag Register

Long Description:

Return to Summary Table

Table 3-357. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 002Eh
CONTROLSS_ECAP1	5024 102Eh
CONTROLSS_ECAP2	5024 202Eh
CONTROLSS_ECAP3	5024 302Eh
CONTROLSS_ECAP4	5024 402Eh
CONTROLSS_ECAP5	5024 502Eh
CONTROLSS_ECAP6	5024 602Eh
CONTROLSS_ECAP7	5024 702Eh
CONTROLSS_ECAP8	5024 802Eh
CONTROLSS_ECAP9	5024 902Eh

Access Types Legend

Table 3-358. ECFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	MUNIT_2_ERROR_EVT2	RO	0h	Error event 2 Interrupt Flag from monitoring unit 2
11	MUNIT_2_ERROR_EVT1	RO	0h	Error event 2 Interrupt Flag from monitoring unit 2
10	MUNIT_1_ERROR_EVT2	RO	0h	Error event 2 Interrupt Flag from monitoring unit 1
9	MUNIT_1_ERROR_EVT1	RO	0h	Error event 2 Interrupt Flag from monitoring unit 1
8	HRERROR	RO	0h	High resolution error status flag Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_HIGH_RESOLUTION_ERRORIndicates the High resolution Error occurred
7	CTR_CMP	RO	0h	Compare Equal Compare Status Flag. This flag is active only in APWM mode. Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_COUNTER_COMPARE_REGIndicates the counter (TSCTR) reached the compare register value (ACMP)
6	CTR_PRD	RO	0h	Counter Equal Period Status Flag. This flag is only active in APWM mode. Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_PERIOD_VALUE_RESETIndicates the counter (TSCTR) reached the period register value (APRD) and was reset.
5	CTROVF	RO	0h	Counter Overflow Status Flag. This flag is active in CAP and APWM mode. Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_COUNTER_TRANSIndicates the counter (TSCTR) has made the transition from FFFFFFFF to 00000000
4	CEVT4	RO	0h	Capture Event 4 Status Flag This flag is only active in CAP mode. Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_4TH_EVENT_ECAPXIndicates the fourth event occurred at ECAPx pin
3	CEVT3	RO	0h	Capture Event 3 Status Flag. This flag is active only in CAP mode. Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_3RD_EVENT_ECAPXIndicates the third event occurred at ECAPx pin.

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Table 3-358. ECFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CEVT2	RO	0h	Capture Event 2 Status Flag. This flag is only active in CAP mode. Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_2ND_EVENT_ECAPXIndicates the second event occurred at ECAPx pin.
1	CEVT1	RO	0h	Capture Event 1 Status Flag. This flag is only active in CAP mode. Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_1ST_EVENT_ECAPXIndicates the first event occurred at ECAPx pin.
0	INT	RO	0h	Global Interrupt Status Flag Read0 | ECAP_INDICATE_NO_EVENTIndicates no event occurred Read1 | ECAP_INDICATE_INTERRUPTIndicates that an interrupt was generated.

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3.8.13 CONTROLSS_ECAPn_ECCLR Registers

3.8.13.1 ECAPn_ECCLR Register (Offset = 30h) [reset = h]

Short Description: Capture Interrupt Clear Register

Long Description:

Return to Summary Table

Table 3-359. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0030h
CONTROLSS_ECAP1	5024 1030h
CONTROLSS_ECAP2	5024 2030h
CONTROLSS_ECAP3	5024 3030h
CONTROLSS_ECAP4	5024 4030h
CONTROLSS_ECAP5	5024 5030h
CONTROLSS_ECAP6	5024 6030h
CONTROLSS_ECAP7	5024 7030h
CONTROLSS_ECAP8	5024 8030h
CONTROLSS_ECAP9	5024 9030h

Access Types Legend

Table 3-360. ECCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	MUNIT_2_ERROR_EVT2	RW RRETURNS 0S	0h	Writing '1' clears MUNIT_2_ERROR_EVT2 interrupt flag
11	MUNIT_2_ERROR_EVT1	RW RRETURNS 0S	0h	Writing '1' clears MUNIT_2_ERROR_EVT1 interrupt flag
10	MUNIT_1_ERROR_EVT2	RW RRETURNS 0S	0h	Writing '1' clears MUNIT_1_ERROR_EVT2 interrupt flag
9	MUNIT_1_ERROR_EVT1	RW RRETURNS 0S	0h	Writing '1' clears MUNIT_1_ERROR_EVT1 interrupt flag
8	HRERROR	RW RRETURNS 0S	0h	High resolution error status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_HRERRORWriting a 1 clears the HRERROR flag.
7	CTR_CMP	RW RRETURNS 0S	0h	Counter Equal Compare Status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_CTR_CMPWriting a 1 clears the CTR=CMP flag.
6	CTR_PRD	RW RRETURNS 0S	0h	Counter Equal Period Status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_CTR_PRDWriting a 1 clears the CTR=PRD flag.
5	CTROVF	RW RRETURNS 0S	0h	Counter Overflow Status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_CTROVFWriting a 1 clears the CTROVF flag.
4	CEVT4	RW RRETURNS 0S	0h	Capture Event 4 Status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_CEVT4Writing a 1 clears the CEVT4 flag.

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Table 3-360. ECCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CEVT3	RW RRETURNS 0S	0h	Capture Event 3 Status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_CEVT3Writing a 1 clears the CEVT3 flag.
2	CEVT2	RW RRETURNS 0S	0h	Capture Event 2 Status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_CEVT2Writing a 1 clears the CEVT2 flag.
1	CEVT1	RW RRETURNS 0S	0h	Capture Event 1 Status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_CEVT1Writing a 1 clears the CEVT1 flag.
0	INT	RW RRETURNS 0S	0h	ECAP Global Interrupt Status Clear 0 | ECAP_0_NO_EFFECTWriting a 0 has no effect. Always reads back a 0 1 | ECAP_1_CLEARS_INTWriting a 1 clears the INT flag and enable further interrupts to be generated if any of the event flags are set to 1

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3.8.14 CONTROLSS_ECAPn_ECFRC Registers

3.8.14.1 ECAPn_ECFRC Register (Offset = 32h) [reset = h]

Short Description: Capture Interrupt Force Register

Long Description:

Return to Summary Table

Table 3-361. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0032h
CONTROLSS_ECAP1	5024 1032h
CONTROLSS_ECAP2	5024 2032h
CONTROLSS_ECAP3	5024 3032h
CONTROLSS_ECAP4	5024 4032h
CONTROLSS_ECAP5	5024 5032h
CONTROLSS_ECAP6	5024 6032h
CONTROLSS_ECAP7	5024 7032h
CONTROLSS_ECAP8	5024 8032h
CONTROLSS_ECAP9	5024 9032h

Access Types Legend

Table 3-362. ECFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	MUNIT_2_ERROR_EVT2	RW RRETURNS 0S	0h	Writing '1' sets MUNIT_2_ERROR_EVT2 interrupt flag
11	MUNIT_2_ERROR_EVT1	RW RRETURNS 0S	0h	Writing '1' sets MUNIT_2_ERROR_EVT1 interrupt flag
10	MUNIT_1_ERROR_EVT2	RW RRETURNS 0S	0h	Writing '1' sets MUNIT_1_ERROR_EVT2 interrupt flag
9	MUNIT_1_ERROR_EVT1	RW RRETURNS 0S	0h	Writing '1' sets MUNIT_1_ERROR_EVT1 interrupt flag
8	HRERROR	RW RRETURNS 0S	0h	High resolution error Force interrupt 0 | ECAP_NO_EFFECT_0No effect. Always reads back a 0. 1 | ECAP_1_SETS_CTR_CMPWriting a 1 sets the CTR_CMP flag.
7	CTR_CMP	RW RRETURNS 0S	0h	Force Counter Equal Compare Interrupt. This event is only active in APWM mode. 0 | ECAP_NO_EFFECT_0No effect. Always reads back a 0. 1 | ECAP_1_SETS_CTR_CMPWriting a 1 sets the CTR_CMP flag.
6	CTR_PRD	RW RRETURNS 0S	0h	Force Counter Equal Period Interrupt. This event is only active in APWM mode. 0 | ECAP_NO_EFFECT_0No effect. Always reads back a 0. 1 | ECAP_1_CLEARS_CTR_PRDWriting a 1 sets the CTR_PRD flag.
5	CTROVF	RW RRETURNS 0S	0h	Force Counter Overflow 0 | ECAP_NO_EFFECT_0No effect. Always reads back a 0. 1 | ECAP_1_SETS_CTROVFWriting a 1 to this bit sets the CTROVF flag.
4	CEVT4	RW RRETURNS 0S	0h	Force Capture Event 4. This event is only active in CAP mode. 0 | ECAP_NO_EFFECT_0No effect. Always reads back a 0. 1 | ECAP_1_SETS_CEVT4Writing a 1 sets the CEVT4 flag.

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Table 3-362. ECFRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CEVT3	RW RRETURNS 0S	0h	Force Capture Event 3. This event is only active in CAP mode. 0 | ECAP_NO_EFFECT_0No effect. Always reads back a 0. 1 | ECAP_1_SETS_CEVT3Writing a 1 sets the CEVT3 flag.
2	CEVT2	RW RRETURNS 0S	0h	Force Capture Event 2. This event is only active in CAP mode. 0 | ECAP_NO_EFFECT_0No effect. Always reads back a 0. 1 | ECAP_1_SETS_CEVT2Writing a 1 sets the CEVT2 flag.
1	CEVT1	RW RRETURNS 0S	0h	Force Capture Event 1. This event is only active in CAP mode. 0 | ECAP_NO_EFFECT_0No effect. Always reads back a 0. 1 | ECAP_1_SETS_CEVT1Sets the CEVT1 flag.
0	RESERVED	RO		Reserved

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3.8.15 CONTROLSS_ECAPn_ECAPSYNCINSEL Registers

3.8.15.1 ECAPn_ECAPSYNCINSEL Register (Offset = 3Ch) [reset = h]

Short Description: SYNC source select register

Long Description:

Return to Summary Table

Table 3-363. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 003Ch
CONTROLSS_ECAP1	5024 103Ch
CONTROLSS_ECAP2	5024 203Ch
CONTROLSS_ECAP3	5024 303Ch
CONTROLSS_ECAP4	5024 403Ch
CONTROLSS_ECAP5	5024 503Ch
CONTROLSS_ECAP6	5024 603Ch
CONTROLSS_ECAP7	5024 703Ch
CONTROLSS_ECAP8	5024 803Ch
CONTROLSS_ECAP9	5024 903Ch

Access Types Legend

Table 3-364. ECAPSYNCINSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RESERVED	RO		Reserved
6 - 0	SEL	RW	1h	These bits determines the source of SYNCIN signal. 0x0 : Disabled using SOC tieoff. 0x7F : Refer to SOC spec for details.

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3.8.16 CONTROLSS_ECAPn_MUNIT_COMMON_CTL Registers

3.8.16.1 ECAPn_MUNIT_COMMON_CTL Register (Offset = 80h) [reset = h]

Short Description: Control registers for monitoring unit {#}

Long Description:

Return to Summary Table

Table 3-365. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0080h
CONTROLSS_ECAP1	5024 1080h
CONTROLSS_ECAP2	5024 2080h
CONTROLSS_ECAP3	5024 3080h
CONTROLSS_ECAP4	5024 4080h
CONTROLSS_ECAP5	5024 5080h
CONTROLSS_ECAP6	5024 6080h
CONTROLSS_ECAP7	5024 7080h
CONTROLSS_ECAP8	5024 8080h
CONTROLSS_ECAP9	5024 9080h

Access Types Legend

Table 3-366. MUNIT_COMMON_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO RRETURNS 0S		Reserved
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 8	GLDSTRBSEL	RW	0h	Global load strobe select to enable shadow to active loading 0x0 : Disabled with SOC level tieoff. 0x1 to 0x7F : Global load strobe from SOC level including ETPWM global load strobes.
7	RESERVED	RO RRETURNS 0S		Reserved
6 - 0	TRIPSEL	RW	0h	Trip signal select to disable and enable signal monitoring automatically 0x0 : Disabled, Trip signals does not affect signal monitoring, achieved with SOC level tieoff. 0x1 to 0x7F : Signal monioring is disabled when selected signal is high and enabled when it is low

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3.8.17 CONTROLSS_ECAPn_MUNIT_1_CTL Registers

3.8.17.1 ECAPn_MUNIT_1_CTL Register (Offset = C0h) [reset = h]

Short Description: Control registers for monitoring unit 1

Long Description:

Return to Summary Table

Table 3-367. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 00C0h
CONTROLSS_ECAP1	5024 10C0h
CONTROLSS_ECAP2	5024 20C0h
CONTROLSS_ECAP3	5024 30C0h
CONTROLSS_ECAP4	5024 40C0h
CONTROLSS_ECAP5	5024 50C0h
CONTROLSS_ECAP6	5024 60C0h
CONTROLSS_ECAP7	5024 70C0h
CONTROLSS_ECAP8	5024 80C0h
CONTROLSS_ECAP9	5024 90C0h

Access Types Legend

Table 3-368. MUNIT_1_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO RRETURNS 0S		Reserved
15 - 12	RESERVED	RO RRETURNS 0S		Reserved
11 - 8	MON_SEL	RW	0h	Type of monitoring 0 : High Pulse width 1 : Low Pulse width 2 : Period width from Rise to Rise 3 : Period width from fall to fall 4 : Monitor rise edge 5 : Monitor fall edge 6-15 : Reserved (High Pulse width)
7 - 2	RESERVED	RO RRETURNS 0S		Reserved
1	DEBUG_RANGE_EN	RW	0h	Debug mode enable. 0 : Debug mode is disabled. 1 : Debug mode of monitoring unit 1 is enabled to obtain the variation seen in the system for debug purpose. Range is captured in MUNIT_1_DEBUG_RANGE_MIN and MUNIT_1_DEBUG_RANGE_MAX registers Toggle DEBUG_RANGE_EN to restart this process, this will initialize MUNIT_1_DEBUG_RANGE_MIN and MUNIT_1_DEBUG_RANGE_MAX registers.
0	EN	RW	0h	0 : Monitoring unit 1 is disabled 1 : Monitoring unit 1 is enabled

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3.8.18 CONTROLSS_ECAPn_MUNIT_1_SHADOW_CTL Registers

3.8.18.1 ECAPn_MUNIT_1_SHADOW_CTL Register (Offset = C4h) [reset = h]

Short Description: Shadow control registers for monitoring unit 1

Long Description:

Return to Summary Table

Table 3-369. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 00C4h
CONTROLSS_ECAP1	5024 10C4h
CONTROLSS_ECAP2	5024 20C4h
CONTROLSS_ECAP3	5024 30C4h
CONTROLSS_ECAP4	5024 40C4h
CONTROLSS_ECAP5	5024 50C4h
CONTROLSS_ECAP6	5024 60C4h
CONTROLSS_ECAP7	5024 70C4h
CONTROLSS_ECAP8	5024 80C4h
CONTROLSS_ECAP9	5024 90C4h

Access Types Legend

Table 3-370. MUNIT_1_SHADOW_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	RESERVED	RO RRETURNS 0S		Reserved
2	LOADMODE	RW	0h	Load mode 0 : Active registers are loaded with shadow on next sync event 1 : Active registers are loaded with shadow on EPWMx.GLDLCSTRB event
1	SWSYNC	RW RRETURNS 0S	0h	Copies Min and Max values from shadow to active registers immediately if MUNIT_1_SHADOW_CTL.SYNCI_EN is set.
0	SYNCI_EN	RW	0h	Shadow Enable 0 : Disabled 1 : Enabled

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3.8.19 CONTROLSS_ECAPn_MUNIT_1_MIN Registers

3.8.19.1 ECAPn_MUNIT_1_MIN Register (Offset = D0h) [reset = h]

Short Description: Min value for monitoring unit 1

Long Description:

Return to Summary Table

Table 3-371. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 00D0h
CONTROLSS_ECAP1	5024 10D0h
CONTROLSS_ECAP2	5024 20D0h
CONTROLSS_ECAP3	5024 30D0h
CONTROLSS_ECAP4	5024 40D0h
CONTROLSS_ECAP5	5024 50D0h
CONTROLSS_ECAP6	5024 60D0h
CONTROLSS_ECAP7	5024 70D0h
CONTROLSS_ECAP8	5024 80D0h
CONTROLSS_ECAP9	5024 90D0h

Access Types Legend

Table 3-372. MUNIT_1_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MIN_VALUE	RW	0h	Minimum value for monitoring

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3.8.20 CONTROLSS_ECAPn_MUNIT_1_MAX Registers

3.8.20.1 ECAPn_MUNIT_1_MAX Register (Offset = D4h) [reset = h]

Short Description: Max value for monitoring unit 1

Long Description:

Return to Summary Table

Table 3-373. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 00D4h
CONTROLSS_ECAP1	5024 10D4h
CONTROLSS_ECAP2	5024 20D4h
CONTROLSS_ECAP3	5024 30D4h
CONTROLSS_ECAP4	5024 40D4h
CONTROLSS_ECAP5	5024 50D4h
CONTROLSS_ECAP6	5024 60D4h
CONTROLSS_ECAP7	5024 70D4h
CONTROLSS_ECAP8	5024 80D4h
CONTROLSS_ECAP9	5024 90D4h

Access Types Legend

Table 3-374. MUNIT_1_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MAX_VALUE	RW	0h	Maximum value for monitoring

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3.8.21 CONTROLSS_ECAPn_MUNIT_1_MIN_SHADOW Registers

3.8.21.1 ECAPn_MUNIT_1_MIN_SHADOW Register (Offset = D8h) [reset = h]

Short Description: Shadow register for Min value of monitoring unit 1

Long Description:

Return to Summary Table

Table 3-375. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 00D8h
CONTROLSS_ECAP1	5024 10D8h
CONTROLSS_ECAP2	5024 20D8h
CONTROLSS_ECAP3	5024 30D8h
CONTROLSS_ECAP4	5024 40D8h
CONTROLSS_ECAP5	5024 50D8h
CONTROLSS_ECAP6	5024 60D8h
CONTROLSS_ECAP7	5024 70D8h
CONTROLSS_ECAP8	5024 80D8h
CONTROLSS_ECAP9	5024 90D8h

Access Types Legend

Table 3-376. MUNIT_1_MIN_SHADOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MIN_VALUE_SHADOW	RW	0h	Shadow minimum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe.

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3.8.22 CONTROLSS_ECAPn_MUNIT_1_MAX_SHADOW Registers

3.8.22.1 ECAPn_MUNIT_1_MAX_SHADOW Register (Offset = DCh) [reset = h]

Short Description: Shadow register for Max value of monitoring unit 1

Long Description:

Return to Summary Table

Table 3-377. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 00DCh
CONTROLSS_ECAP1	5024 10DCh
CONTROLSS_ECAP2	5024 20DCh
CONTROLSS_ECAP3	5024 30DCh
CONTROLSS_ECAP4	5024 40DCh
CONTROLSS_ECAP5	5024 50DCh
CONTROLSS_ECAP6	5024 60DCh
CONTROLSS_ECAP7	5024 70DCh
CONTROLSS_ECAP8	5024 80DCh
CONTROLSS_ECAP9	5024 90DCh

Access Types Legend

Table 3-378. MUNIT_1_MAX_SHADOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MAX_VALUE_SHADOW	RW	0h	Shadow maximum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe.

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3.8.23 CONTROLSS_ECAPn_MUNIT_1_DEBUG_RANGE_MIN Registers

3.8.23.1 ECAPn_MUNIT_1_DEBUG_RANGE_MIN Register (Offset = E0h) [reset = h]

Short Description: Observed Min value of check being enabled on minotoring unit 1

Long Description:

Return to Summary Table

Table 3-379. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 00E0h
CONTROLSS_ECAP1	5024 10E0h
CONTROLSS_ECAP2	5024 20E0h
CONTROLSS_ECAP3	5024 30E0h
CONTROLSS_ECAP4	5024 40E0h
CONTROLSS_ECAP5	5024 50E0h
CONTROLSS_ECAP6	5024 60E0h
CONTROLSS_ECAP7	5024 70E0h
CONTROLSS_ECAP8	5024 80E0h
CONTROLSS_ECAP9	5024 90E0h

Access Types Legend

Table 3-380. MUNIT_1_DEBUG_RANGE_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MIN_VALUE	RO	FFFFFFFFh	Observed Min value of check being enabled on minotoring unit 1. Is updated when MUNIT_1_CTL.DEBUG_RANGE_EN is set to '1'

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3.8.24 CONTROLSS_ECAPn_MUNIT_1_DEBUG_RANGE_MAX Registers

3.8.24.1 ECAPn_MUNIT_1_DEBUG_RANGE_MAX Register (Offset = E4h) [reset = h]

Short Description: Observed Max value of check being enabled on minotoring unit 1

Long Description:

Return to Summary Table

Table 3-381. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 00E4h
CONTROLSS_ECAP1	5024 10E4h
CONTROLSS_ECAP2	5024 20E4h
CONTROLSS_ECAP3	5024 30E4h
CONTROLSS_ECAP4	5024 40E4h
CONTROLSS_ECAP5	5024 50E4h
CONTROLSS_ECAP6	5024 60E4h
CONTROLSS_ECAP7	5024 70E4h
CONTROLSS_ECAP8	5024 80E4h
CONTROLSS_ECAP9	5024 90E4h

Access Types Legend

Table 3-382. MUNIT_1_DEBUG_RANGE_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MAX_VALUE	RO	0h	Observed Min value of check being enabled on minotoring unit 1. Is updated when MUNIT_1_CTL.DEBUG_RANGE_EN is set to '1'

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3.8.25 CONTROLSS_ECAPn_MUNIT_2_CTL Registers

3.8.25.1 ECAPn_MUNIT_2_CTL Register (Offset = 100h) [reset = h]

Short Description: Control registers for monitoring unit 2

Long Description:

Return to Summary Table

Table 3-383. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0100h
CONTROLSS_ECAP1	5024 1100h
CONTROLSS_ECAP2	5024 2100h
CONTROLSS_ECAP3	5024 3100h
CONTROLSS_ECAP4	5024 4100h
CONTROLSS_ECAP5	5024 5100h
CONTROLSS_ECAP6	5024 6100h
CONTROLSS_ECAP7	5024 7100h
CONTROLSS_ECAP8	5024 8100h
CONTROLSS_ECAP9	5024 9100h

Access Types Legend

Table 3-384. MUNIT_2_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO RRETURNS 0S		Reserved
15 - 12	RESERVED	RO RRETURNS 0S		Reserved
11 - 8	MON_SEL	RW	0h	Type of monitoring 0 : High Pulse width 1 : Low Pulse width 2 : Period width from Rise to Rise 3 : Period width from fall to fall 4 : Monitor rise edge 5 : Monitor fall edge 6-15 : Reserved (High Pulse width)
7 - 2	RESERVED	RO RRETURNS 0S		Reserved
1	DEBUG_RANGE_EN	RW	0h	Debug mode enable. 0 : Debug mode is disabled. 1 : Debug mode of monitoring unit 2 is enabled to obtain the variation seen in the system for debug purpose. Range is captured in MUNIT_2_DEBUG_RANGE_MIN and MUNIT_2_DEBUG_RANGE_MAX registers Toggle DEBUG_RANGE_EN to restart this process, this will initialize MUNIT_2_DEBUG_RANGE_MIN and MUNIT_2_DEBUG_RANGE_MAX registers.
0	EN	RW	0h	0 : Monitoring unit 2 is disabled 1 : Monitoring unit 2 is enabled

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3.8.26 CONTROLSS_ECAPn_MUNIT_2_SHADOW_CTL Registers

3.8.26.1 ECAPn_MUNIT_2_SHADOW_CTL Register (Offset = 104h) [reset = h]

Short Description: Shadow control registers for monitoring unit 2

Long Description:

Return to Summary Table

Table 3-385. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0104h
CONTROLSS_ECAP1	5024 1104h
CONTROLSS_ECAP2	5024 2104h
CONTROLSS_ECAP3	5024 3104h
CONTROLSS_ECAP4	5024 4104h
CONTROLSS_ECAP5	5024 5104h
CONTROLSS_ECAP6	5024 6104h
CONTROLSS_ECAP7	5024 7104h
CONTROLSS_ECAP8	5024 8104h
CONTROLSS_ECAP9	5024 9104h

Access Types Legend

Table 3-386. MUNIT_2_SHADOW_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	RESERVED	RO RRETURNS 0S		Reserved
2	LOADMODE	RW	0h	Load mode 0 : Active registers are loaded with shadow on next sync event 1 : Active registers are loaded with shadow on EPWMx.GLDLCSTRB event
1	SWSYNC	RW RRETURNS 0S	0h	Copies Min and Max values from shadow to active registers immediately if MUNIT_2_SHADOW_CTL.SYNCI_EN is set.
0	SYNCI_EN	RW	0h	Shadow Enable 0 : Disabled 1 : Enabled

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3.8.27 CONTROLSS_ECAPn_MUNIT_2_MIN Registers

3.8.27.1 ECAPn_MUNIT_2_MIN Register (Offset = 110h) [reset = h]

Short Description: Min value for monitoring unit 2

Long Description:

Return to Summary Table

Table 3-387. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0110h
CONTROLSS_ECAP1	5024 1110h
CONTROLSS_ECAP2	5024 2110h
CONTROLSS_ECAP3	5024 3110h
CONTROLSS_ECAP4	5024 4110h
CONTROLSS_ECAP5	5024 5110h
CONTROLSS_ECAP6	5024 6110h
CONTROLSS_ECAP7	5024 7110h
CONTROLSS_ECAP8	5024 8110h
CONTROLSS_ECAP9	5024 9110h

Access Types Legend

Table 3-388. MUNIT_2_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MIN_VALUE	RW	0h	Minimum value for monitoring

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3.8.28 CONTROLSS_ECAPn_MUNIT_2_MAX Registers

3.8.28.1 ECAPn_MUNIT_2_MAX Register (Offset = 114h) [reset = h]

Short Description: Max value for monitoring unit 2

Long Description:

Return to Summary Table

Table 3-389. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0114h
CONTROLSS_ECAP1	5024 1114h
CONTROLSS_ECAP2	5024 2114h
CONTROLSS_ECAP3	5024 3114h
CONTROLSS_ECAP4	5024 4114h
CONTROLSS_ECAP5	5024 5114h
CONTROLSS_ECAP6	5024 6114h
CONTROLSS_ECAP7	5024 7114h
CONTROLSS_ECAP8	5024 8114h
CONTROLSS_ECAP9	5024 9114h

Access Types Legend

Table 3-390. MUNIT_2_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MAX_VALUE	RW	0h	Maximum value for monitoring

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3.8.29 CONTROLSS_ECAPn_MUNIT_2_MIN_SHADOW Registers

3.8.29.1 ECAPn_MUNIT_2_MIN_SHADOW Register (Offset = 118h) [reset = h]

Short Description: Shadow register for Min value of monitoring unit 2

Long Description:

Return to Summary Table

Table 3-391. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0118h
CONTROLSS_ECAP1	5024 1118h
CONTROLSS_ECAP2	5024 2118h
CONTROLSS_ECAP3	5024 3118h
CONTROLSS_ECAP4	5024 4118h
CONTROLSS_ECAP5	5024 5118h
CONTROLSS_ECAP6	5024 6118h
CONTROLSS_ECAP7	5024 7118h
CONTROLSS_ECAP8	5024 8118h
CONTROLSS_ECAP9	5024 9118h

Access Types Legend

Table 3-392. MUNIT_2_MIN_SHADOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MIN_VALUE_SHADOW	RW	0h	Shadow minimum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe.

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3.8.30 CONTROLSS_ECAPn_MUNIT_2_MAX_SHADOW Registers

3.8.30.1 ECAPn_MUNIT_2_MAX_SHADOW Register (Offset = 11Ch) [reset = h]

Short Description: Shadow register for Max value of monitoring unit 2

Long Description:

Return to Summary Table

Table 3-393. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 011Ch
CONTROLSS_ECAP1	5024 111Ch
CONTROLSS_ECAP2	5024 211Ch
CONTROLSS_ECAP3	5024 311Ch
CONTROLSS_ECAP4	5024 411Ch
CONTROLSS_ECAP5	5024 511Ch
CONTROLSS_ECAP6	5024 611Ch
CONTROLSS_ECAP7	5024 711Ch
CONTROLSS_ECAP8	5024 811Ch
CONTROLSS_ECAP9	5024 911Ch

Access Types Legend

Table 3-394. MUNIT_2_MAX_SHADOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MAX_VALUE_SHADOW	RW	0h	Shadow maximum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe.

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3.8.31 CONTROLSS_ECAPn_MUNIT_2_DEBUG_RANGE_MIN Registers

3.8.31.1 ECAPn_MUNIT_2_DEBUG_RANGE_MIN Register (Offset = 120h) [reset = h]

Short Description: Observed Min value of check being enabled on minotoring unit 2

Long Description:

Return to Summary Table

Table 3-395. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0120h
CONTROLSS_ECAP1	5024 1120h
CONTROLSS_ECAP2	5024 2120h
CONTROLSS_ECAP3	5024 3120h
CONTROLSS_ECAP4	5024 4120h
CONTROLSS_ECAP5	5024 5120h
CONTROLSS_ECAP6	5024 6120h
CONTROLSS_ECAP7	5024 7120h
CONTROLSS_ECAP8	5024 8120h
CONTROLSS_ECAP9	5024 9120h

Access Types Legend

Table 3-396. MUNIT_2_DEBUG_RANGE_MIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MIN_VALUE	RO	FFFFFFFFh	Observed Min value of check being enabled on minotoring unit 2. Is updated when MUNIT_2_CTL.DEBUG_RANGE_EN is set to '1'

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3.8.32 CONTROLSS_ECAPn_MUNIT_2_DEBUG_RANGE_MAX Registers

3.8.32.1 ECAPn_MUNIT_2_DEBUG_RANGE_MAX Register (Offset = 124h) [reset = h]

Short Description: Observed Max value of check being enabled on minotoring unit 2

Long Description:

Return to Summary Table

Table 3-397. Instance Table

Instance Name	Physical Address
CONTROLSS_ECAP0	5024 0124h
CONTROLSS_ECAP1	5024 1124h
CONTROLSS_ECAP2	5024 2124h
CONTROLSS_ECAP3	5024 3124h
CONTROLSS_ECAP4	5024 4124h
CONTROLSS_ECAP5	5024 5124h
CONTROLSS_ECAP6	5024 6124h
CONTROLSS_ECAP7	5024 7124h
CONTROLSS_ECAP8	5024 8124h
CONTROLSS_ECAP9	5024 9124h

Access Types Legend

Table 3-398. MUNIT_2_DEBUG_RANGE_MAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MAX_VALUE	RO	0h	Observed Min value of check being enabled on minotoring unit 2. Is updated when MUNIT_2_CTL.DEBUG_RANGE_EN is set to '1'

3.8.33 Access Table

Table 3-399. Access Type Codes

Access Type	Code	Description
RW	RW	Read / Write
RO RRETURNS0S	RO RRETURNS0S	Read returns 0s
RW RRETURNS0S	RW RRETURNS0S	Read returns 0s/Write
RO	RO	Read

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3.9 EPWM Registers

EPWM Instance Count Note

Note

N = [(m * 0x4 0000h) + (n * 0x1000h) + (Offset)] where
m = [0:3] and
n = [0:31]
for the EPWM registers defined below.

Table 3-400. CONTROLSS_Gm_EPWMn Registers Base Address Table

Offset	Length	Register Name	CONTROLSS_Gm_EPWMn Physical Address
0h	16	EPWM_TBCTL	500**N**h
2h	16	EPWM_TBCTL2	500**N**h
4h	16	EPWM_RESERVED_1	500**N**h
6h	16	EPWM_EPWMSYNCINSEL	500**N**h
8h	16	EPWM_TBCTR	500**N**h
Ah	16	EPWM_TBSTS	500**N**h
Ch	16	EPWM_EPWMSYNCOUTEN	500**N**h
Eh	16	EPWM_TBCTL3	500**N**h
10h	16	EPWM_CMPCTL	500**N**h
12h	16	EPWM_CMPCTL2	500**N**h
14h	16	EPWM_RESERVED_2	500**N**h
18h	16	EPWM_DBCTL	500**N**h
1Ah	16	EPWM_DBCTL2	500**N**h
1Ch	16	EPWM_RESERVED_3	500**N**h
20h	16	EPWM_AQCTL	500**N**h
22h	16	EPWM_AQTSRCSEL	500**N**h
24h	16	EPWM_RESERVED_4	500**N**h
28h	16	EPWM_PCCTL	500**N**h
2Ah	16	EPWM_RESERVED_5	500**N**h
30h	16	EPWM_VCAPCTL	500**N**h
32h	16	EPWM_VCNTCFG	500**N**h
34h	16	EPWM_RESERVED_6	500**N**h
40h	16	EPWM_HRCNFG	500**N**h
42h	16	EPWM_RESERVED_7	500**N**h
44h	16	EPWM_RESERVED_8	500**N**h
46h	16	EPWM_RESERVED_9	500**N**h
48h	16	EPWM_RESERVED_10	500**N**h
4Ah	16	EPWM_RESERVED_11	500**N**h
4Ch	16	EPWM_RESERVED_12	500**N**h
4Eh	16	EPWM_HRCNFG2	500**N**h
50h	16	EPWM_RESERVED_13	500**N**h
5Ah	16	EPWM_HRPCTL	500**N**h
5Ch	16	EPWM_TRREM	500**N**h
5Eh	16	EPWM_RESERVED_14	500**N**h
68h	16	EPWM_GLDCTL	500**N**h
6Ah	16	EPWM_GLDCFG	500**N**h

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Table 3-400. CONTROLSS_Gm_EPWMn Registers Base Address Table (continued)

Offset	Length	Register Name	CONTROLSS_Gm_EPWMn Physical Address
6Ch	16	EPWM_RESERVED_15	500**N**h
70h	32	EPWM_EPWMXLINK	500**N**h
74h	32	EPWM_EPWMXLINK2	500**N**h
78h	16	EPWM_RESERVED_16	500**N**h
7Ah	16	EPWM_ETEST	500**N**h
7Ch	16	EPWM_EPWMREV	500**N**h
7Eh	16	EPWM_HRPWMREV	500**N**h
80h	16	EPWM_AQCTLA	500**N**h
82h	16	EPWM_AQCTLA2	500**N**h
84h	16	EPWM_AQCTLB	500**N**h
86h	16	EPWM_AQCTLB2	500**N**h
88h	16	EPWM_RESERVED_17	500**N**h
8Eh	16	EPWM_AQSFRC	500**N**h
90h	16	EPWM_RESERVED_18	500**N**h
92h	16	EPWM_AQCSFRC	500**N**h
94h	16	EPWM_RESERVED_19	500**N**h
A0h	16	EPWM_DBREDHR	500**N**h
A2h	16	EPWM_DBRED	500**N**h
A4h	16	EPWM_DBFEDHR	500**N**h
A6h	16	EPWM_DBFED	500**N**h
A8h	16	EPWM_RESERVED_20	500**N**h
C0h	32	EPWM_TBPHS	500**N**h
C4h	16	EPWM_TBPRDHR	500**N**h
C6h	16	EPWM_TBPRD	500**N**h
C8h	16	EPWM_TBPRDHRB	500**N**h
CAh	16	EPWM_RESERVED_21	500**N**h
D4h	32	EPWM_CMPA	500**N**h
D8h	32	EPWM_CMPB	500**N**h
DCh	16	EPWM_RESERVED_22	500**N**h
DEh	16	EPWM_CMPC	500**N**h
E0h	16	EPWM_RESERVED_23	500**N**h
E2h	16	EPWM_CMPD	500**N**h
E4h	16	EPWM_RESERVED_24	500**N**h
E8h	16	EPWM_GLDCTL2	500**N**h
EAh	16	EPWM_RESERVED_25	500**N**h
EEh	16	EPWM_SWVDELVAL	500**N**h
F0h	16	EPWM_RESERVED_26	500**N**h
100h	16	EPWM_TZSEL	500**N**h
102h	16	EPWM_TZSEL2	500**N**h
104h	16	EPWM_TZDCSEL	500**N**h
106h	16	EPWM_RESERVED_27	500**N**h
108h	16	EPWM_TZCTL	500**N**h
10Ah	16	EPWM_TZCTL2	500**N**h
10Ch	16	EPWM_TZCTLDCA	500**N**h
10Eh	16	EPWM_TZCTLDCB	500**N**h
110h	16	EPWM_RESERVED_28	500**N**h

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Table 3-400. CONTROLSS_Gm_EPWMn Registers Base Address Table (continued)

Offset	Length	Register Name	CONTROLSS_Gm_EPWMn Physical Address
11Ah	16	EPWM_TZEINT	500**N**h
11Ch	16	EPWM_RESERVED_29	500**N**h
126h	16	EPWM_TZFLG	500**N**h
128h	16	EPWM_TZCBCFLG	500**N**h
12Ah	16	EPWM_TZOSTFLG	500**N**h
12Ch	16	EPWM_RESERVED_30	500**N**h
12Eh	16	EPWM_TZCLR	500**N**h
130h	16	EPWM_TZCBCCLR	500**N**h
132h	16	EPWM_TZOSTCLR	500**N**h
134h	16	EPWM_RESERVED_31	500**N**h
136h	16	EPWM_TZFRC	500**N**h
138h	16	EPWM_RESERVED_32	500**N**h
13Ah	16	EPWM_TZTRIPOUTSEL	500**N**h
13Ch	16	EPWM_RESERVED_33	500**N**h
148h	16	EPWM_ETSEL	500**N**h
14Ah	16	EPWM_RESERVED_34	500**N**h
14Ch	16	EPWM_ETPS	500**N**h
14Eh	16	EPWM_RESERVED_35	500**N**h
150h	16	EPWM_ETFLG	500**N**h
152h	16	EPWM_RESERVED_36	500**N**h
154h	16	EPWM_ETCLR	500**N**h
156h	16	EPWM_RESERVED_37	500**N**h
158h	16	EPWM_ETFRC	500**N**h
15Ah	16	EPWM_RESERVED_38	500**N**h
15Ch	16	EPWM_ETINTPS	500**N**h
15Eh	16	EPWM_RESERVED_39	500**N**h
160h	16	EPWM_ETSOCPS	500**N**h
162h	16	EPWM_RESERVED_40	500**N**h
164h	16	EPWM_ETCNTINITCTL	500**N**h
166h	16	EPWM_RESERVED_41	500**N**h
168h	16	EPWM_ETCNTINIT	500**N**h
16Ah	16	EPWM_RESERVED_42	500**N**h
16Ch	16	EPWM_ETINTMIXEN	500**N**h
16Eh	16	EPWM_RESERVED_43	500**N**h
170h	16	EPWM_ETSOCAMIXEN	500**N**h
172h	16	EPWM_RESERVED_44	500**N**h
174h	16	EPWM_ETSOCBMIXEN	500**N**h
176h	16	EPWM_RESERVED_45	500**N**h
180h	16	EPWM_DCTRIPSEL	500**N**h
182h	16	EPWM_RESERVED_46	500**N**h
186h	16	EPWM_DCACTL	500**N**h
188h	16	EPWM_DCBCTL	500**N**h
18Ah	16	EPWM_RESERVED_47	500**N**h
18Eh	16	EPWM_DCFCTL	500**N**h
190h	16	EPWM_DCCAPCTL	500**N**h
192h	16	EPWM_DCFOFFSET	500**N**h

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Table 3-400. CONTROLSS_Gm_EPWMn Registers Base Address Table (continued)

Offset	Length	Register Name	CONTROLSS_Gm_EPWMn Physical Address
194h	16	EPWM_DCFOFFSETCNT	500**N**h
196h	16	EPWM_DCFWINDOW	500**N**h
198h	16	EPWM_DCFWINDOWCNT	500**N**h
19Ah	16	EPWM_BLANKPULSEMIXSEL	500**N**h
19Ch	16	EPWM_DCCAPMIXSEL	500**N**h
19Eh	16	EPWM_DCCAP	500**N**h
1A0h	16	EPWM_RESERVED_48	500**N**h
1A4h	16	EPWM_DCAHTRIPSEL	500**N**h
1A6h	16	EPWM_DCALTRIPSEL	500**N**h
1A8h	16	EPWM_DCBHTRIPSEL	500**N**h
1AAh	16	EPWM_DCBLTRIPSEL	500**N**h
1ACh	16	EPWM_CAPCTL	500**N**h
1AEh	16	EPWM_CAPGATETRIPSEL	500**N**h
1B0h	16	EPWM_CAPINTRIPSEL	500**N**h
1B2h	16	EPWM_CAPTRIPSEL	500**N**h
1B4h	16	EPWM_RESERVED_49	500**N**h
1ECh	16	EPWM_SPARE1	500**N**h
1EEh	16	EPWM_RESERVED_50	500**N**h
1F0h	16	EPWM_SPARE2	500**N**h
1F2h	16	EPWM_RESERVED_51	500**N**h
1F8h	16	EPWM_RESERVED_52	500**N**h
1FAh	16	EPWM_HWVDELVAL	500**N**h
1FCh	16	EPWM_VCNTVAL	500**N**h
1FEh	16	EPWM_RESERVED_53	500**N**h
C00h	32	EPWM_MINDBCFG	500**N**h
C04h	32	EPWM_MINDBDLY	500**N**h
C08h	32	EPWM_RESERVED_1	500**N**h
C20h	32	EPWM_LUTCTLA	500**N**h
C24h	32	EPWM_LUTCTLB	500**N**h
C28h	32	EPWM_RESERVED_2	500**N**h

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3.9.1 CONTROLSS_Gm_EPWMn_TBCTL Registers

3.9.1.1 Gm_EPWMn_TBCTL Register (Offset = 0h) [reset = h]

Short Description: Time Base Control Register

Long Description:

Return to Summary Table

Table 3-401. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-74. TBCTL Name Register

15	14	13	12	11	10	9	8
FREE_SOFT		PHSDIR		CLKDIV		HSPCLKDIV	
R/W		R/W		R/W		R/W	
0		0		0		1	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
HSPCLKDIV	SWFSYNC	RESERVED		PRDLD	PHSEN	CTRMODE	
R/W	R-0/W	R		R/W	R/W	R/W	
1	0	0		0	0	3	

Access Types Legend

Table 3-402. TBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	FREE_SOFT	R/W	0h	Emulation Mode Bits. These bits select the behavior of the ePWM time-base counter during emulation events 00: Stop after the next time-base counter increment or decrement 01: Stop when counter completes a whole cycle: - Up-count mode: stop when the time-base counter = period (TBCTR = TBPRD) - Down-count mode: stop when the time-base counter = 0x00 (TBCTR = 0x00) - Up-down-count mode: stop when the time-base counter = 0x00 (TBCTR = 0x00) 1x: Free run
13	PHSDIR	R/W	0h	Phase Direction Bit This bit is only used when the time-base counter is configured in the up-down-count mode. The PHSDIR bit indicates the direction the time-base counter (TBCTR) will count after a synchronization event occurs and a new phase value is loaded from the phase (TBPHS) register. This is irrespective of the direction of the counter before the synchronization event.. In the up-count and down-count modes this bit is ignored. 0: Count down after the synchronization event. 1: Count up after the synchronization event.
12 - 10	CLKDIV	R/W	0h	Time Base Clock Pre-Scale Bits These bits select the time base clock pre-scale value (TBCLK = EPWMCLK/(HSPCLKDIV * CLKDIV)): 000: /1 (default on reset) 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128
9 - 7	HSPCLKDIV	R/W	1h	High Speed Time Base Clock Pre-Scale Bits These bits determine part of the time-base clock prescale value. TBCLK = EPWMCLK / (HSPCLKDIV x CLKDIV). This divisor emulates the HSPCLK in the TMS320x281x system as used on the Event Manager (EV) peripheral. 000: /1 001: /2 (default on reset) 010: /4 011: /6 100: /8 101: /10 110: /12 111: /14
6	SWFSYNC	R-0/W	0h	Software Forced Sync Pulse 0: Writing a 0 has no effect and reads always return a 0. 1: Writing a 1 forces a one-time synchronization pulse to be generated. SWFSYNC can be enabled to affect EPWMxSYNCO by setting the EPWMSYNCOUTEN.SWEN bit.
5 - 4	RESERVED	R		Reserved

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Table 3-402. TBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PRDLD	R/W	0h	Active Period Reg Load from Shadow Select 0: The period register (TBPRD) is loaded from its shadow register when the time-base counter, TBCTR, is equal to zero and/or a sync event as determined by the TBCTL2[PRDLDSYNC] bit. A write/read to the TBPRD register accesses the shadow register. 1: Immediate Mode (Shadow register bypassed): A write or read to the TBPRD register accesses the active register.
2	PHSEN	R/W	0h	Counter Reg Load from Phase Reg Enable 0: Do not load the time-base counter (TBCTR) from the time-base phase register (TBPHS). 1: Allow Counter to be loaded from the Phase register (TBPHS) and shadow to active load events when an EPWMxSYNCI input signal occurs or a software-forced sync signal, see bit 6.
1 - 0	CTRMODE	R/W	3h	Counter Mode The time-base counter mode is normally configured once and not changed during normal operation. If you change the mode of the counter, the change will take effect at the next TBCLK edge and the current counter value shall increment or decrement from the value before the mode change. These bits set the time-base counter mode of operation as follows: 00: Up-count mode 01: Down-count mode 10: Up-down count mode 11: Freeze counter operation (default on reset)

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3.9.2 CONTROLSS_Gm_EPWMn_TBCTL2 Registers

3.9.2.1 Gm_EPWMn_TBCTL2 Register (Offset = 2h) [reset = h]

Short Description: Time Base Control Register 2

Long Description:

Return to Summary Table

Table 3-403. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-75. TBCTL2 Name Register

15	14	13	12	11	10	9	8
PRDLDSYNC		RESERVED		RESERVED			
R/W		R		R-0			
0		0		0			
7	6	5	4	3	2	1	0
OSHTSYNC	OSHTSYNCMODE	SELFCLRTRREM	RESERVED				
R-0/W	R/W	R/W	R-0				
0	0	0	0				

Access Types Legend

Table 3-404. TBCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	PRDLDSYNC	R/W	0h	Shadow to Active Period Register Load on SYNC event 00: Shadow to Active Load of TBPRD occurs only when TBCTR = 0 (same as legacy). 01: Shadow to Active Load of TBPRD occurs both when TBCTR = 0 and when SYNC occurs. 10: Shadow to Active Load of TBPRD occurs only when a SYNC is received. 11: Reserved Note: This bit selection is valid only if TBCTL[PRDLD]=0.
13 - 12	RESERVED	R		Reserved
11 - 8	RESERVED	R-0		Reserved
7	OSHTSYNC	R-0/W	0h	Oneshot sync bit 0: Writing a '0' has no effect. 1: Allow one sync pulse to propogate.
6	OSHTSYNCMODE	R/W	0h	Oneshot sync enable bit 0: Oneshot sync mode disabled 1: Oneshot sync mode enabled
5	SELFCLRTRREM	R/W	0h	Loop back sync pulse to enable self sync operation 0: Self clear function of TRREM disabled. 1: Self clear function of TRREM enabled
4 - 0	RESERVED	R-0		Reserved

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3.9.3 CONTROLSS_Gm_EPWMn_EPWMSYNCINSEL Registers

3.9.3.1 Gm_EPWMn_EPWMSYNCINSEL Register (Offset = 6h) [reset = h]

Short Description: EPWMxSYNCIN Source Select Register

Long Description:

Return to Summary Table

Table 3-405. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-76. EPWMSYNCINSEL Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED	SEL						
R	R/W						
0	1						

Access Types Legend

Table 3-406. EPWMSYNCINSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 7	RESERVED	R		Reserved
6 - 0	SEL	R/W	1h	These bits determine the source of the EPWMxSYNCI signal0x0: Disabled0x01: EPWM0.SYNCOUT.0x10: EPWM15.SYNCOUT0x11:EPWM16.SYNCOUT.0x20: EPWM31.SYNCOUT0x21: Reserved.0x40: ECAP0.SYNCOUT.0x49: ECAP9.SYNCPUT0x4A: Reserved.0x4F: Reserved0x50: InputXBar.Out[4]0x51: InputXBar.Out[20]0x52: Reserved.0x57: Reserved0x58: C2K_TimeSyncXBar..SYNCPWMOut00x59: C2K_TimeSyncXBar..SYNCPWMOut10x5A: Reserved0x5F: Reserved0x60: FSIRX0.RXTRIG[0]0x61: FSIRX0.RXTRIG[1]0x62: FSIRX0.RXTRIG[2]0x63: FSIRX0.RXTRIG[3]0x64: FSIRX1.RXTRIG[0]0x65: FSIRX1.RXTRIG[1]0x66: FSIRX1.RXTRIG[2]0x67: FSIRX1.RXTRIG[3]0x68: FSIRX2.RXTRIG[0]0x69: FSIRX2.RXTRIG[1]0x6A: FSIRX2.RXTRIG[2]0x6B: FSIRX2.RXTRIG[3]0x6C: FSIRX3.RXTRIG[0]0x6D: FSIRX3.RXTRIG[1]0x6E: FSIRX3.RXTRIG[2]0x6F: FSIRX3.RXTRIG[3]0x70: Reserved.0x7F: Reserved

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3.9.4 CONTROLSS_Gm_EPWMn_TBCTR Registers

3.9.4.1 Gm_EPWMn_TBCTR Register (Offset = 8h) [reset = h]

Short Description: Time Base Counter Register

Long Description:

Return to Summary Table

Table 3-407. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-77. TBCTR Name Register

15	14	13	12	11	10	9	8
TBCTR							
R/W							
0							
7	6	5	4	3	2	1	0
TBCTR							
R/W							
0							

Access Types Legend

Table 3-408. TBCTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	TBCTR	R/W	0h	Time Base Counter Register

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3.9.5 CONTROLSS_Gm_EPWMn_TBSTS Registers

3.9.5.1 Gm_EPWMn_TBSTS Register (Offset = Ah) [reset = h]

Short Description: Time Base Status Register

Long Description:

Return to Summary Table

Table 3-409. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-78. TBSTS Name Register

15	14	13	12	11	10	9	8
RESERVED							
R-0							
0							
7	6	5	4	3	2	1	0
RESERVED					CTRMAX	SYNCI	CTRDIR
R-0					R/W	R/W	R
0					0	0	1

Access Types Legend

Table 3-410. TBSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 3	RESERVED	R-0		Reserved
2	CTRMAX	R/W	0h	Time-Base Counter Max Latched Status Bit 0: Reading a 0 indicates the time-base counter never reached its maximum value. Writing a 0 will have no effect. 1: Reading a 1 on this bit indicates that the time-base counter reached the max value 0xFFFF. Writing a 1 to this bit will clear the latched event.
1	SYNCI	R/W	0h	Input Synchronization Latched Status Bit 0: Writing a 0 will have no effect. Reading a 0 indicates no external synchronization event has occurred. 1: Reading a 1 on this bit indicates that an external synchronization event has occurred (EPWMxSYNCI). Writing a 1 to this bit will clear the latched event.
0	CTRDIR	R	1h	Time Base Counter Direction Status Bit 0: Time-Base Counter is currently counting down. 1: Time-Base Counter is currently counting up. Note: This bit is only valid when the counter is not frozen.

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3.9.6 CONTROLSS_Gm_EPWMn_EPWMSYNCOUTEN Registers

3.9.6.1 Gm_EPWMn_EPWMSYNCOUTEN Register (Offset = Ch) [reset = h]

Short Description: EPWMxSYNCOUT Source Enable Register

Long Description:

Return to Summary Table

Table 3-411. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-79. EPWMSYNCOUTEN Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED	DCBEVT1EN	DCAEVT1EN	CMPDEN	CMPCEN	CMPBEN	ZEROEN	SWEN
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

Access Types Legend

Table 3-412. EPWMSYNCOUTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R		Reserved
7	RESERVED	R		Reserved
6	DCBEVT1EN	R/W	0h	This bit enables the DCBEVT1.sync event to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a DCBEVT1.sync event
5	DCAEVT1EN	R/W	0h	This bit enables the DCAEVT1.sync event to set the EPWMxSYNCOUT signal. 0 Disabled 1 The EPWMxSYNCOUT signal is pulsed for one PWM clock period upon a DCAEVT1.sync event
4	CMPDEN	R/W	0h	This bit enables the TBCTR = CMPD event to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a time-base counter equal to counter compare D event (TBCTR = CMPD)
3	CMPCEN	R/W	0h	This bit enables the TBCTR = CMPC event to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a time-base counter equal to counter compare C event (TBCTR = CMPC)
2	CMPBEN	R/W	0h	This bit enables the TBCTR = CMPB event to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a time-base counter equal to counter compare B event (TBCTR = CMPB)
1	ZEROEN	R/W	0h	This bit enables the TBCTR = 0x0000 event to set the EPWMxSYNCOUT signal. 0 Disabled 1 The EPWMxSYNCOUT signal is pulsed for one PWM clock period upon the value of TBCTR changing to 0x0000
0	SWEN	R/W	1h	This bit enables the TBCTL.SWFSYNC bit to set the EPWMxSYNCO signal. 0 Disabled 1 The EPWMxSYNCO signal is pulsed for one PWM clock period when the TBCTL.SWFSYNC bit is set

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3.9.7 CONTROLSS_Gm_EPWMn_TBCTL3 Registers

3.9.7.1 Gm_EPWMn_TBCTL3 Register (Offset = Eh) [reset = h]

Short Description: Time Base Control Register 3

Long Description:

Return to Summary Table

Table 3-413. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-80. TBCTL3 Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
RESERVED							OSSFRCEN
R							R/W
0							0

Access Types Legend

Table 3-414. TBCTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 1	RESERVED	R		Reserved
0	OSSFRCEN	R/W	0h	This bit determines which bit sets the EPWMxSYNCOUT One Shot Latch. 0 TBCTL2[OSHTSYNC] sets the One Shot Latch 1 GLDCTL2[OSHTLD] sets the One Shot Latch

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3.9.8 CONTROLSS_Gm_EPWMn_CMPCTL Registers

3.9.8.1 Gm_EPWMn_CMPCTL Register (Offset = 10h) [reset = h]

Short Description: Counter Compare Control Register

Long Description:

Return to Summary Table

Table 3-415. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-81. CMPCTL Name Register

15	14	13	12	11	10	9	8
LINKDUTYHR	RESERVED	LOADBSYNC		LOADASYNC		SHDWBFULL	SHDWAFULL
R/W	R-0	R/W		R/W		R	R
0	0	0		0		0	0
7	6	5	4	3	2	1	0
RESERVED	SHDWBMODE	RESERVED	SHDWAMODE	LOADBMODE		LOADAMODE	
R-0	R/W	R-0	R/W	R/W		R/W	
0	0	0	0	0		0	

Access Types Legend

Table 3-416. CMPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LINKDUTYHR	R/W	0h	CMPAHR, CMPBHR Register Linking: 0 PWMA and PWMB outputs generated independently and CMPAHR, CMPBHR are independent values as on Type-4 1 When this bit is set CMPBHR assumes the same value as CMPAHR. This is typically used in complimentary PWM output generation (Section 7 details of the operation)
14	RESERVED	R-0		Reserved
13 - 12	LOADBSYNC	R/W	0h	Shadow to Active CMPB Register Load on SYNC event 00: Shadow to Active Load of CMPB:CMPBHR occurs according to LOADBMODE (bits 1,0) (same as legacy) 01: Shadow to Active Load of CMPB:CMPBHR occurs both according to LOADBMODE bits and when SYNC occurs 10: Shadow to Active Load of CMPB:CMPBHR occurs only when a SYNC is received 11: Reserved Note: This bit is valid only if CMPCTL[SHDWBMODE] = 0.
11 - 10	LOADASYNC	R/W	0h	Shadow to Active CMPA Register Load on SYNC event 00: Shadow to Active Load of CMPA:CMPAHR occurs according to LOADAMODE (bits 1,0) (same as legacy) 01: Shadow to Active Load of CMPA:CMPAHR occurs both according to LOADAMODE bits and when SYNC occurs 10: Shadow to Active Load of CMPA:CMPAHR occurs only when a SYNC is received 11: Reserved Note: This bit is valid only if CMPCTL[SHDWAMODE] = 0.
9	SHDWBFULL	R	0h	Counter-compare B (CMPB) Shadow Register Full Status Flag This bit self clears once a loadstrobe occurs. 0: CMPB shadow FIFO not full yet 1: Indicates the CMPB shadow FIFO is full a CPU write will overwrite current shadow value
8	SHDWAFULL	R	0h	Counter-compare A (CMPA) Shadow Register Full Status Flag The flag bit is set when a 32-bit write to CMPA:CMPAHR register or a 16-bit write to CMPA register is made. A 16-bit write to CMPAHR register will not affect the flag. This bit self clears once a load-strobe occurs. 0: CMPA shadow FIFO not full yet 1: Indicates the CMPA shadow FIFO is full, a CPU write will overwrite the current shadow value
7	RESERVED	R-0		Reserved

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Table 3-416. CMPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SHDWBMODE	R/W	0h	Counter-compare B (CMPB) Register Operating Mode 0: Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register 1: Immediate mode. Only the active compare B register is used. All writes and reads directly access the active register for immediate compare action
5	RESERVED	R-0		Reserved
4	SHDWAMODE	R/W	0h	Counter-compare A (CMPA) Register Operating Mode 0: Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register 1: Immediate mode. Only the active compare register is used. All writes and reads directly access the active register for immediate compare action
3 - 2	LOADBMODE	R/W	0h	Active Counter-Compare B (CMPB) Load From Shadow Select Mode This bit has no effect in immediate mode (CMPCTL[SHDWBMODE] = 1). 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible)
1 - 0	LOADAMODE	R/W	0h	Active Counter-Compare A (CMPA) Load From Shadow Select Mode This bit has no effect in immediate mode (CMPCTL[SHDWAMODE] = 1). 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible)

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3.9.9 CONTROLSS_Gm_EPWMn_CMPCTL2 Registers

3.9.9.1 Gm_EPWMn_CMPCTL2 Register (Offset = 12h) [reset = h]

Short Description: Counter Compare Control Register 2

Long Description:

Return to Summary Table

Table 3-417. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-82. CMPCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED		LOADDSYNC		LOADCSYNC		RESERVED	
R-0		R/W		R/W		R-0	
0		0		0		0	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	SHDWDMODE	RESERVED	SHDWCMODE	LOADDMODE		LOADCMODE	
R-0	R/W	R-0	R/W	R/W		R/W	
0	0	0	0	0		0	

Access Types Legend

Table 3-418. CMPCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	RESERVED	R-0		Reserved
13 - 12	LOADDSYNC	R/W	0h	Shadow to Active CMPD Register Load on SYNC event 00: Shadow to Active Load of CMPD occurs according to LOADDMODE 01: Shadow to Active Load of CMPD occurs both according to LOADDMODE bits and when SYNC occurs 10: Shadow to Active Load of CMPD occurs only when a SYNC is received 11: Reserved Note: This bit is valid only if CMPCTL2[SHDWDMODE] = 0.
11 - 10	LOADCSYNC	R/W	0h	Shadow to Active CMPC Register Load on SYNC event 00: Shadow to Active Load of CMPC occurs according to LOADCMODE 01: Shadow to Active Load of CMPC occurs both according to LOADCMODE bits and when SYNC occurs 10: Shadow to Active Load of CMPC occurs only when a SYNC is received 11: Reserved Note: This bit is valid only if CMPCTL2[SHDWCMODE] = 0.
9 - 7	RESERVED	R-0		Reserved
6	SHDWDMODE	R/W	0h	Counter-Compare D Register Operating Mode 0: Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 1: Immediate mode - only the Active compare register is used. All writes/reads via the CPU directly access the Active register for immediate Compare action.
5	RESERVED	R-0		Reserved
4	SHDWCMODE	R/W	0h	Counter-Compare C Register Operating Mode 0: Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 1: Immediate mode - only the Active compare register is used. All writes/reads via the CPU directly access the Active register for immediate Compare action.
3 - 2	LOADDMODE	R/W	0h	Active Counter-Compare D (CMPD) Load from Shadow Select Mode 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: Has no effect in Immediate mode.

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Table 3-418. CMPCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1 - 0	LOADCMODE	R/W	0h	Active Counter-Compare C (CMPC) Load from Shadow Select Mode 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: Has no effect in Immediate mode.

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3.9.10 CONTROLSS_Gm_EPWMn_DBCTL Registers

3.9.10.1 Gm_EPWMn_DBCTL Register (Offset = 18h) [reset = h]

Short Description: Dead-Band Generator Control Register

Long Description:

Return to Summary Table

Table 3-419. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-83. DBCTL Name Register

15	14	13	12	11	10	9	8
HALFCYCLE	DEDB_MODE	OUTSWAP		SHDWDBFED MODE	SHDWDBRED MODE	LOADFEDMODE	
R/W	R/W	R/W		R/W	R/W	R/W	
0	0	0		0	0	0	
7	6	5	4	3	2	1	0
LOADREDMODE		IN_MODE		POLSEL		OUT_MODE	
R/W		R/W		R/W		R/W	
0		0		0		0	

Access Types Legend

Table 3-420. DBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	HALFCYCLE	R/W	0h	Half Cycle Clocking Enable Bit 0: Full cycle clocking enabled. The dead-band counters are clocked at the TBCLK rate. 1: Half cycle clocking enabled. The dead-band counters are clocked at TBCLK*2.
14	DEDB_MODE	R/W	0h	Dead Band Dual-Edge B Mode Control (S8 switch) 0: Rising edge delay applied to InA/InB as selected by S4 switch (IN-MODE bits) on A signal path only. Falling edge delay applied to InA/InB as selected by S5 switch (INMODE bits) on B signal path only. 1: Rising edge delay and falling edge delay applied to source selected by S4 switch (INMODE bits) and output to B signal path only. Note: When this bit is set to 1, user should always either set OUT_MODE bits such that Apath = InA OR OUTSWAP bits such that OutA=Bpath otherwise, OutA will be invalid.
13 - 12	OUTSWAP	R/W	0h	Dead Band Output Swap Control Bit 13 controls the S6 switch and bit 12 controls the S7 switch. 00: OutA and OutB signals are as defined by OUT-MODE bits. 01: OutA = A-path as defined by OUT-MODE bits. OutB = A-path as defined by OUT-MODE bits (rising edge delay or delay-bypassed A signal path). 10: OutA = B-path as defined by OUT-MODE bits (falling edge delay or delay-bypassed B signal path). OutB = B-path as defined by OUT-MODE bits. 11: OutA = B-path as defined by OUT-MODE bits (falling edge delay or delay-bypassed B signal path). OutB = A-path as defined by OUT-MODE bits (rising edge delay or delay-bypassed A signal path).
11	SHDWDBFEDMODE	R/W	0h	FED Dead-Band Load Mode 0: Immediate mode. Only the active DBFED register is used. All writes/reads via the CPU directly access the active register for immediate "FED dead-band action." 1: Shadow mode. Operates as a double buffer. All writes via the CPU access Shadow register. Default at Reset is Immediate mode (for compatibility with legacy).

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Table 3-420. DBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	SHDWDBREDMODE	R/W	0h	RED Dead-Band Load Mode 0: Immediate mode. Only the active DBRED register is used. All writes/reads via the CPU directly access the active register for immediate "RED dead-band action." 1: Shadow mode. Operates as a double buffer. All writes via the CPU access Shadow register. Default at Reset is Immediate mode (for compatibility with legacy).
9 - 8	LOADFEDMODE	R/W	0h	Active DBFED Load from Shadow Select Mode 00: Load on Counter = 0 (CNT_eq) 01: Load on Counter = Period (PRD_eq) 10: Load on either Counter = 0, or Counter = Period 11: Freeze (no loads possible) Note: has no effect in Immediate mode.
7 - 6	LOADREDMODE	R/W	0h	Active DBRED Load from Shadow Select Mode 00: Load on Counter = 0 (CNT_eq) 01: Load on Counter = Period (PRD_eq) 10: Load on either Counter = 0, or Counter = Period 11: Freeze (no loads possible) Note: has no effect in Immediate mode.
5 - 4	IN_MODE	R/W	0h	Dead-Band Input Mode Control Bit 5 controls the S5 switch and bit 4 controls the S4 switch shown. This allows you to select the input source to the falling-edge and rising-edge delay. To produce classical dead-band waveforms the default is EPWMxA In is the source for both falling and rising-edge delays. 00: EPWMxA In (from the action-qualifier) is the source for both falling-edge and rising-edge delay. 01: EPWMxB In (from the action-qualifier) is the source for rising-edge delayed signal. EPWMxA In (from the action-qualifier) is the source for falling-edge delayed signal. 10: EPWMxA In (from the action-qualifier) is the source for rising-edge delayed signal. EPWMxB In (from the action-qualifier) is the source for falling-edge delayed signal. 11: EPWMxB In (from the action-qualifier) is the source for both rising-edge delay and falling-edge delayed signal.
3 - 2	POLSEL	R/W	0h	Polarity Select Control Bit 3 controls the S3 switch and bit 2 controls the S2 switch. This allows you to selectively invert one of the delayed signals before it is sent out of the dead-band submodule. The following descriptions correspond to classical upper/lower switch control as found in one leg of a digital motor control inverter. These assume that DBCTL[OUT_MODE] = 1,1 and DBCTL[IN_MODE] = 0x0. Other enhanced modes are also possible, but not regarded as typical usage modes. 00: Active high (AH) mode. Neither EPWMxA nor EPWMxB is inverted (default). 01: Active low complementary (ALC) mode. EPWMxA is inverted. 10: Active high complementary (AHC). EPWMxB is inverted. 11: Active low (AL) mode. Both EPWMxA and EPWMxB are inverted.
1 - 0	OUT_MODE	R/W	0h	Dead-Band Output Mode Control Bit 1 controls the S1 switch and bit 0 controls the S0 switch. 00: DBM is fully disabled or by-passed. In this mode the POLSEL and IN-MODE bits have no effect. 01: Apath = InA (delay is by-passed for A signal path) Bpath = FED (Falling Edge Delay in B signal path) 10: Apath = RED (Rising Edge Delay in A signal path) Bpath = InB (delay is by-passed for B signal path) 11: DBM is fully enabled (i.e. both RED and FED active)

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3.9.11 CONTROLSS_Gm_EPWMn_DBCTL2 Registers

3.9.11.1 Gm_EPWMn_DBCTL2 Register (Offset = 1Ah) [reset = h]

Short Description: Dead-Band Generator Control Register 2

Long Description:

Return to Summary Table

Table 3-421. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-84. DBCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED							
R-0							
0							
7	6	5	4	3	2	1	0
RESERVED					SHDWDBCTLMODE	LOADDBCTLMODE	
R-0					R/W	R/W	
0					0	0	

Access Types Legend

Table 3-422. DBCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 3	RESERVED	R-0		Reserved
2	SHDWDBCTLMODE	R/W	0h	DBCTL Load Mode 0: Immediate mode - only the Active DBCTL register is used. All writes/reads via the CPU directly access the Active register. 1: Shadow mode - All writes and reads to bits [5:0] of the DBCTL register are shadowed. All other bits still access the active register.
1 - 0	LOADDBCTLMODE	R/W	0h	Active DBCTL Load from Shadow Select Mode 00: Load on Counter = 0 (CNT_eq) 01: Load on Counter = Period (PRD_eq) 10: Load on either Counter = 0, or Counter = Period 11: Freeze (no loads possible) Note: has no effect in Immediate mode

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3.9.12 CONTROLSS_Gm_EPWMn_AQCTL Registers

3.9.12.1 Gm_EPWMn_AQCTL Register (Offset = 20h) [reset = h]

Short Description: Action Qualifier Control Register

Long Description:

Return to Summary Table

Table 3-423. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-85. AQCTL Name Register

15	14	13	12	11	10	9	8
RESERVED				LDAQBSYNC		LDAQASYNC	
R-0				R/W		R/W	
0				0		0	
7	6	5	4	3	2	1	0
RESERVED	SHDWAQBMODE	RESERVED	SHDWAQAMODE	LDAQBMODE		LDAQAMODE	
R-0	R/W	R-0	R/W	R/W		R/W	
0	0	0	0	0		0	

Access Types Legend

Table 3-424. AQCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R-0		Reserved
11 - 10	LDAQBSYNC	R/W	0h	Shadow to Active AQCTLB Register Load on SYNC event 00: Shadow to Active Load of AQCTLB occurs according to LDAQBMODE 01: Shadow to Active Load of AQCTLB occurs both according to LDAQBMODE bits and when SYNC occurs. 10: Shadow to Active Load of AQCTLB occurs only when a SYNC is received. 11: Reserved Note: This bit is valid only if AQCTL[SHDWAQBMODE] = 1.
9 - 8	LDAQASYNC	R/W	0h	Shadow to Active AQCTLA Register Load on SYNC event 00: Shadow to Active Load of AQCTLA occurs according to LDAQAMODE 01: Shadow to Active Load of AQCTLA occurs both according to LDAQAMODE bits and when SYNC occurs. 10: Shadow to Active Load of AQCTLA occurs only when a SYNC is received. 11: Reserved Note: This bit is valid only if AQCTL[SHDWAQAMODE] = 1.
7	RESERVED	R-0		Reserved
6	SHDWAQBMODE	R/W	0h	Action Qualifier B Register operating mode 1: Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 0: Immediate mode - only the Active action qualifier register is used. All writes/reads via the CPU directly access the Active register.
5	RESERVED	R-0		Reserved
4	SHDWAQAMODE	R/W	0h	Action Qualifier A Register operating mode 1: Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register. 0: Immediate mode - only the Active action qualifier register is used. All writes/reads via the CPU directly access the Active register.

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Table 3-424. AQCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3 - 2	LDAQBMODE	R/W	0h	Active Action Qualifier B Load from Shadow Select Mode 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: has no effect in Immediate mode.
1 - 0	LDAQAMODE	R/W	0h	Active Action Qualifier A Load from Shadow Select Mode 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Freeze (no loads possible) Note: has no effect in Immediate mode.

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3.9.13 CONTROLSS_Gm_EPWMn_AQTSRCSEL Registers

3.9.13.1 Gm_EPWMn_AQTSRCSEL Register (Offset = 22h) [reset = h]

Short Description: Action Qualifier Trigger Event Source Select Register

Long Description:

Return to Summary Table

Table 3-425. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-86. AQTSRCSEL Name Register

15	14	13	12	11	10	9	8
RESERVED							
R-0							
0							
7	6	5	4	3	2	1	0
T2SEL				T1SEL			
R/W				R/W			
0				0			

Access Types Legend

Table 3-426. AQTSRCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R-0		Reserved
7 - 4	T2SEL	R/W	0h	T2 Event Source Select Bits 0000: DCAEVT1 0001: DCAEVT2 0010: DCBEVT1 0011: DCBEVT2 0100: TZ1 0101: TZ2 0110: TZ3 0111: EPWMxSYNCI 1000: DCEVTFILT Others: Reserved
3 - 0	T1SEL	R/W	0h	T1 Event Source Select Bits 0000: DCAEVT1 0001: DCAEVT2 0010: DCBEVT1 0011: DCBEVT2 0100: TZ1 0101: TZ2 0110: TZ3 0111: EPWMxSYNCI 1000: DCEVTFILT Others: Reserved

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3.9.14 CONTROLSS_Gm_EPWMn_PCCTL Registers

3.9.14.1 Gm_EPWMn_PCCTL Register (Offset = 28h) [reset = h]

Short Description: PWM Chopper Control Register

Long Description:

Return to Summary Table

Table 3-427. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-87. PCCTL Name Register

15	14	13	12	11	10	9	8
RESERVED						CHPDUTY	
R-0						R/W	
0						0	
7	6	5	4	3	2	1	0
CHPFREQ			OSHTWTH				CHPEN
R/W			R/W				R/W
0			0				0

Access Types Legend

Table 3-428. PCCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	R-0		Reserved
10 - 8	CHPDUTY	R/W	0h	Chopping Clock Duty Cycle 000: Duty = 1/8 (12.5%) 001: Duty = 2/8 (25.0%) 010: Duty = 3/8 (37.5%) 011: Duty = 4/8 (50.0%) 100: Duty = 5/8 (62.5%) 101: Duty = 6/8 (75.0%) 110: Duty = 7/8 (87.5%) 111: Reserved
7 - 5	CHPFREQ	R/W	0h	Chopping Clock Frequency 000: Divide by 1 (no prescale, = 12.5 MHz at 100 MHz TBCLK) 001: Divide by 2 (6.25 MHz at 100 MHz TBCLK) 010: Divide by 3 (4.16 MHz at 100 MHz TBCLK) 011: Divide by 4 (3.12 MHz at 100 MHz TBCLK) 100: Divide by 5 (2.50 MHz at 100 MHz TBCLK) 101: Divide by 6 (2.08 MHz at 100 MHz TBCLK) 110: Divide by 7 (1.78 MHz at 100 MHz TBCLK) 111: Divide by 8 (1.56 MHz at 100 MHz TBCLK)
4 - 1	OSHTWTH	R/W	0h	One-Shot Pulse Width 0000: 1 x EPWMCLK / 8 wide (= 80 ns at 100 MHz EPWMCLK) 0001: 2 x EPWMCLK / 8 wide (= 160 ns at 100 MHz EPWMCLK) 0010: 3 x EPWMCLK / 8 wide (= 240 ns at 100 MHz EPWMCLK) 0011: 4 x EPWMCLK / 8 wide (= 320 ns at 100 MHz EPWMCLK) 0100: 5 x EPWMCLK / 8 wide (= 400 ns at 100 MHz EPWMCLK) 0101: 6 x EPWMCLK / 8 wide (= 480 ns at 100 MHz EPWMCLK) 0110: 7 x EPWMCLK / 8 wide (= 560 ns at 100 MHz EPWMCLK) 0111: 8 x EPWMCLK / 8 wide (= 640 ns at 100 MHz EPWMCLK) 1000: 9 x EPWMCLK / 8 wide (= 720 ns at 100 MHz EPWMCLK) 1001: 10 x EPWMCLK / 8 wide (= 800 ns at 100 MHz EPWMCLK) 1010: 11 x EPWMCLK / 8 wide (= 880 ns at 100 MHz EPWMCLK) 1011: 12 x EPWMCLK / 8 wide (= 960 ns at 100 MHz EPWMCLK) 1100: 13 x EPWMCLK / 8 wide (= 1040 ns at 100 MHz EPWMCLK) 1101: 14 x EPWMCLK / 8 wide (= 1120 ns at 100 MHz EPWMCLK) 1110: 15 x EPWMCLK / 8 wide (= 1200 ns at 100MHz EPWMCLK) 1111: 16 x EPWMCLK / 8 wide (= 1280 ns at 100 MHz EPWMCLK)
0	CHPEN	R/W	0h	PWM-Chopping Enable 0: Disable (bypass) PWM chopping function 1: Enable chopping function

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3.9.15 CONTROLSS_Gm_EPWMn_VCAPCTL Registers

3.9.15.1 Gm_EPWMn_VCAPCTL Register (Offset = 30h) [reset = h]

Short Description: Valley Capture Control Register

Long Description:

Return to Summary Table

Table 3-429. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-88. VCAPCTL Name Register

15	14	13	12	11	10	9	8
RESERVED					EDGEFILTDLYSEL	VDELAYDIV	
R-0					R/W	R/W	
0					0	0	

7	6	5	4	3	2	1	0
VDELAYDIV	RESERVED		TRIGSEL			VCAPSTART	VCAPE
R/W	R-0		R/W			R-0/W	R/W
0	0		0			0	0

Access Types Legend

Table 3-430. VCAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	R-0		Reserved
10	EDGEFILTDLYSEL	R/W	0h	Valley Switching Mode Delay Selection 0: No delay applied to the edge filter output 1: HWDELAYVAL delay applied to the edge filter output
9 - 7	VDELAYDIV	R/W	0h	Valley Delay Mode Divide Enable 000: HWVDELVAL = SWVDELVAL 001: HWVDELVAL = VCNTVAL+SWVDELVAL 010: HWVDELVAL = VCNTVAL"1+SWVDELVAL 011: HWVDELVAL = VCNTVAL"2+SWVDELVAL 100: HWVDELVAL = VCNTVAL"4+SWVDELVAL Note: Delay value between the consecutive edge captures can optionally be divided by using these bits.
6 - 5	RESERVED	R-0		Reserved
4 - 2	TRIGSEL	R/W	0h	Status of Numbered of Captured Events 000: Capture sequence is triggered by software via writes to VCAPCTL[VCAPSTART]. 001: Capture sequence is triggered by CNT_zero event. 010: Capture sequence is triggered by PRD_eq event. 011: Capture sequence is triggered by CNT_zero or PRD_eq event. 100: Capture sequence is triggered by DCAEVT1 event. 101: Capture sequence is triggered by DCAEVT2 event. 110: Capture sequence is triggered by DCBEVT1 event. 111: Capture sequence is triggered by DCBEVT2 event. Note: Valley capture sequence triggered by the selected event in this register field. Once the chosen event occurs the capture sequence is armed. Event captures occur based of the event chosen in DCFCTL[SRCSEL] register. Note: Same event may not be chosen in both DCFCTL[SRCSEL] and VCAPCTL[TRIGSEL] registers. Note: Once the chosen event in VCAPCTL[TRIGSEL] occurs, irrespective of the currentcapture status, capture sequence is retriggered.

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Table 3-430. VCAPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	VCAPSTART	R-0/W	0h	Valley Capture Start 0: Writing a 0 has no effect 1: Trigger the capture sequence once if VCAPCTL[TRIGSEL]=0x0 Note: This bit is used to start valley capture sequence through software. VCAPCTL[TRIGSEL] has to be chosen for software trigger for this bit to have any effect. Writing of 1 will result in one capture sequence trigger.
0	VCAPE	R/W	0h	Valley Capture Enable/Disable 0: Disabled 1: Enabled

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3.9.16 CONTROLSS_Gm_EPWMn_VCNTCFG Registers

3.9.16.1 Gm_EPWMn_VCNTCFG Register (Offset = 32h) [reset = h]

Short Description: Valley Counter Config Register

Long Description:

Return to Summary Table

Table 3-431. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-89. VCNTCFG Name Register

15	14	13	12	11	10	9	8
STOPEDGESTS	RESERVED			STOPEDGE			
R	R-0			R/W			
0	0			0			
7	6	5	4	3	2	1	0
STARTEDGESTS	RESERVED			STARTEDGE			
R	R-0			R/W			
0	0			0			

Access Types Legend

Table 3-432. VCNTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	STOPEDGESTS	R	0h	Stop Edge Status Bit 0: Stop edge has not occurred 1: Stop edge occurred Note: This bit is set only after the trigger sequence is armed (upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL]) and STOPEDGE occurs. Note:This bit is reset by the occurrence of the trigger pulse selected through VCAPCTL[TRIGSEL]
14 - 12	RESERVED	R-0		Reserved
11 - 8	STOPEDGE	R/W	0h	Counter Stop Edge Selection Once the counter operation is armed, upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL] pulse - valley counter would stop counting upon the occurrence of chosen number of events thorough this bit field. Stop counting on occurrence of: 0000: Do not stop 0001 1st edge 0010: 2nd edge 0011: 3rd edge ... 1,1,1,1: 15th edge
7	STARTEDGESTS	R	0h	Start Edge Status Bit 0: Start edge has not occurred 1: Start edge occurred Note: This bit is set only after the trigger sequence is armed (upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL]) and STARTEDGE occurs. Note:This bit is reset by the occurrence of the trigger pulse selected through VCAPCTL[TRIGSEL]
6 - 4	RESERVED	R-0		Reserved
3 - 0	STARTEDGE	R/W	0h	Counter Start Edge Selection Once the counter operation is armed, upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL] pulse - valley counter would start counting upon the occurrence of chosen number of events thorough this bit field. Start counting on occurrence of 0000: Do not start 0001: 1st edge 0010: 2nd edge 0011: 3rd edge ... 1111: 15th edge

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3.9.17 CONTROLSS_Gm_EPWMn_HRCNFG Registers

3.9.17.1 Gm_EPWMn_HRCNFG Register (Offset = 40h) [reset = h]

Short Description: HRPWM Configuration Register This register is only accessible on EPWM modules with HRPWM capabilities.

Long Description:

Return to Summary Table

Table 3-433. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-90. HRCNFG Name Register

15	14	13	12	11	10	9	8
LINESEL		RESERVED	HRLOADB		CTLMODEB	EDGMODEB	
R/W		R-0	R/W		R/W	R/W	
0		0	0		0	0	
7	6	5	4	3	2	1	0
SWAPAB	AUTOCONV	SELOUTB	HRLOAD		CTLMODE	EDGMODE	
R/W	R/W	R/W	R/W		R/W	R/W	
0	0	0	0		0	0	

Access Types Legend

Table 3-434. HRCNFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	LINESEL	R/W	0h	Delay Line Selection Bits: Selects which of the 4 delay lines for a particular ePWM/EPWM module to send to CALIN for calibration.
13	RESERVED	R-0		Reserved
12 - 11	HRLOADB	R/W	0h	Shadow Mode Bit Selects the time event that loads the CMPBHR shadow value into the active register. 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Load on CMPB_EQ (Translator Event CMPB-3)
10	CTLMODEB	R/W	0h	Control Mode Bits Selects the register (CMP/TBPRD or TBPHS) that controls the MEP: 0: CMPBHR(8) or TBPRDHR(8) Register controls the edge position (i.e., this is duty or period control mode). (Default on Reset) 1: TBPHSHR(8) Register controls the edge position (i.e., this is phase control mode).
9 - 8	EDGMODEB	R/W	0h	Edge Mode Bits Selects the edge of the PWM that is controlled by the micro-edge position (MEP) logic: 00: HRPWM capability is disabled (default on reset) 01: MEP control of rising edge (CMPBHR) 10: MEP control of falling edge (CMPBHR) 11: MEP control of both edges (TBPHSHR or TBPRDHR)
7	SWAPAB	R/W	0h	Swap ePWM A & B Output Signals This bit enables the swapping of the A & B signal outputs. The selection is as follows: 0: ePWMxA and ePWMxB outputs are unchanged. 1: ePWMxA signal appears on ePWMxB output and ePWMxB signal appears on ePWMxA output.

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Table 3-434. HRCNFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	AUTOCONV	R/W	0h	Auto Convert Delay Line Value Selects whether the fractional duty cycle/period/phase in the CMPAHR/TBPRDHR/TBPHSHR register is automatically scaled by the MEP scale factor in the HRMSTEP register or manually scaled by calculations in application software. The SFO library function automatically updates the HRMSTEP register with the appropriate MEP scale factor. 0: Automatic HRMSTEP scaling is disabled. 1: Automatic HRMSTEP scaling is enabled. If application software is manually scaling the fractional duty cycle, or phase (i.e. software sets CMPAHR = (fraction(PWMduty * PWMperiod) * MEP Scale Factor)<<8 + 0x080 for duty cycle), then this mode must be disabled.
5	SELOUTB	R/W	0h	EPWMxB Output Select Bit This bit selects which signal is output on the ePWMxB channel output. The inversion will take the high resolution mode into account and the inverted signal will contain any high resolution modification. The inversion takes place as the last step in modifying the ePWMxB signal. 0: ePWMxB output is normal. 1: ePWMxB output is inverted version of ePWMxA signal.
4 - 3	HRLOAD	R/W	0h	Shadow Mode Bit Selects the time event that loads the CMPAHR shadow value into the active register. 00: Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01: Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10: Load on either CTR = Zero or CTR = PRD 11: Load on CMPA_EQ (Translator Event CMPA-3)
2	CTLMODE	R/W	0h	Control Mode Bits Selects the register (CMP/TBPRD or TBPHS) that controls the MEP: 0: CMPAHR(8) or TBPRDHR(8) Register controls the edge position (i.e., this is duty or period control mode). (Default on Reset) 1: TBPHSHR(8) Register controls the edge position (i.e., this is phase control mode).
1 - 0	EDGMODE	R/W	0h	Edge Mode Bits Selects the edge of the PWM that is controlled by the micro-edge position (MEP) logic: 00: HRPWM capability is disabled (default on reset) 01: MEP control of rising edge (CMPAHR) 10: MEP control of falling edge (CMPAHR) 11: MEP control of both edges (TBPHSHR or TBPRDHR)

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3.9.18 CONTROLSS_Gm_EPWMn_HRCNFG2 Registers

3.9.18.1 Gm_EPWMn_HRCNFG2 Register (Offset = 4Eh) [reset = h]

Short Description: HRPWM Configuration 2 Register This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.

Long Description:

Return to Summary Table

Table 3-435. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-91. HRCNFG2 Name Register

15	14	13	12	11	10	9	8
NOBYPASS	DELLOADFRC	RESERVED					
R/W	R-0/W	R-0					
0	0	0					
7	6	5	4	3	2	1	0
RESERVED		CTLMODEDBFED		CTLMODEDBRED		EDGMODEDB	
R-0		R/W		R/W		R/W	
0		0		0		0	

Access Types Legend

Table 3-436. HRCNFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NOBYPASS	R/W	0h	No Bypass Delay Line Update Bit: For internal test purposes, this bit disables the 1 SYSCLK cycle bypass before delay line is updated.
14	DELLOADFRC	R-0/W	0h	Delay Line Load Software Force: For internal test purposes, software force generates a pulse which forces a delay line update (similar to PRD_eq/CNT_zero strobe).
13 - 6	RESERVED	R-0		Reserved
5 - 4	CTLMODEDBFED	R/W	0h	Shadow Mode Bit - selection should match DBCTL[LOADFEDMODE] Selects the time event that loads the DBFEDHR shadow value into the active register. 00 Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01 Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10 Load on either CTR = Zero or CTR = PRD 11 Reserved
3 - 2	CTLMODEDBRED	R/W	0h	Shadow Mode Bit - selection should match DBCTL[LOADREDMODE] Selects the time event that loads the DBREDHR shadow value into the active register. 00 Load on CTR = Zero: Time-base counter equal to zero (TBCTR = 0x0000) 01 Load on CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 10 Load on either CTR = Zero or CTR = PRD 11 Reserved
1 - 0	EDGMODEDB	R/W	0h	Edge Mode Bits Selects the edge of the PWM that is controlled by the micro-edge position (MEP) logic: 00 HRPWM capability is disabled (default on reset) 01 MEP control of rising edge (DBREDHR) 10 MEP control of falling edge (DBFEDHR) 11 MEP control of both edges (rising edge of DBREDHR or falling edge of DBFEDHR)

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3.9.19 CONTROLSS_Gm_EPWMn_HRPCTL Registers

3.9.19.1 Gm_EPWMn_HRPCTL Register (Offset = 5Ah) [reset = h]

Short Description: High Resolution Period Control Register This register is only accessible on EPWM modules with HRPWM capabilities.

Long Description:

Return to Summary Table

Table 3-437. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-92. HRPCTL Name Register

15	14	13	12	11	10	9	8
RESERVED							
R-0							
0							
7	6	5	4	3	2	1	0
RESERVED	PWMSYNCSELX			HRPSYNCE	TBPHSHRLOADE	PWMSYNCSEL	HRPE
R-0	R/W			R/W	R/W	R/W	R/W
0	0			0	0	0	0

Access Types Legend

Table 3-438. HRPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 7	RESERVED	R-0		Reserved
6 - 4	PWMSYNCSELX	R/W	0h	Extended selection bits for EPWMSYNCPER 000: EPWMSYNCPER is defined by PWMSYNCSEL - ' default condition (compatible with previous EPWM versions) 001: Reserved 010: Reserved 011: Reserved 100: CTR = CMPC, Count direction Up 101: CTR = CMPC, Count direction Down 110: CTR = CMPD, Count direction Up 111: CTR = CMPD, Count direction Down
3	HRPSYNCE	R/W	0h	SYNC Enable Bit (TRSYNCE)/High Resolution Period SYNC Enable Bit (HRPSYNCE)
2	TBPHSHRLOADE	R/W	0h	TBPHSHR Load Enable This bit allows you to synchronize ePWM modules with a high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital compare event. This allows for multiple ePWM modules operating at the same frequency to be phase aligned with high-resolution. 0: Disables synchronization of high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital compare event: 1: Synchronize the high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital comparator synchronization event. The phase is synchronized using the contents of the high-resolution phase TBPHSHR register. The TBCTL[PHSEN] bit which enables the loading of the TBCTR register with TBPHS register value on a SYNCIN or TBCTL[SWFSYNC] event works independently. However, users need to enable this bit also if they want to control phase in conjunction with the high-resolution period feature. This bit and the TBCTL[PHSEN] bit must be set to 1 when high-resolution period is enabled forup-down count mode even if TBPHSHR = 0x0000. This bit does not need to be set when only high-resolution duty is enabled.
1	PWMSYNCSEL	R/W	0h	PWMSYNC Source Select Bit: This bit selects the source for the EPWMSYNCPER signal that goes to the CMPSS and GPDAC: 0 CTR = PRD: Time-base counter equal to period (TBCTR = TBPRD) 1 CTR = zero: Time-base counter equal to zero (TBCTR = 0x00)

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Table 3-438. HRPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HRPE	R/W	0h	High Resolution Period Enable Bit 0: High resolution period feature disabled. In this mode the ePWM behaves as a Type 0 ePWM. 1: High resolution period enabled. In this mode the HRPWM module can control high-resolution of both the duty and frequency. When high-resolution period is enabled, TBCTL[CTRMODE] = 0,1 (down-count mode) is not supported.

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3.9.20 CONTROLSS_Gm_EPWMn_TRREM Registers

3.9.20.1 Gm_EPWMn_TRREM Register (Offset = 5Ch) [reset = h]

Short Description: HRPWM High Resolution Remainder Register This register is only accessible on EPWM modules with HRPWM capabilities.

Long Description:

Return to Summary Table

Table 3-439. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-93. TRREM Name Register

15	14	13	12	11	10	9	8
RESERVED					TRREM		
R-0					R/W		
0					0		
7	6	5	4	3	2	1	0
TRREM							
R/W							
0							

Access Types Legend

Table 3-440. TRREM Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	R-0		Reserved
10 - 0	TRREM	R/W	0h	HRPWM Remainder Bits: This 11-bit value keeps track of the remainder portion of the HRPWM algorithm calculations. This value keeps track of the remainder portion of the HRPWM hardware calculations. Notes: 1. The lower 8-bits of the TRREM register can be automatically initialized with the TBPHSHR value on a SYNCIN or TBCTL[SWFSYNC] event or DC event (if enabled). The user can also write a value with the CPU. 2. Priority of TRREM register updates: Sync (software or hardware) TBPHSHR copied to TRREM : Highest Priority HRPWM Hardware (updates TRREM register): Next priority CPU Write To TRREM Register: Lowest Priority 3. Bit 10 of TRREM register is not used in asymmetrical mode. This bit can be forced to zero. TRREM will be initialized to 0x0 and 0x100 in Up and Up-down modes respectively. Asymmetrical Mode: TRREM[7:0] = TBPHSHR[15:8] TRREM[10,9,8] = 0,0,0 Symmetrical Mode: TRREM[7:0] = TBPHSHR[15:8] TRREM[10,9,8] = 0,0,1

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3.9.21 CONTROLSS_Gm_EPWMn_GLDCTL Registers

3.9.21.1 Gm_EPWMn_GLDCTL Register (Offset = 68h) [reset = h]

Short Description: Global PWM Load Control Register

Long Description:

Return to Summary Table

Table 3-441. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-94. GLDCTL Name Register

15	14	13	12	11	10	9	8
RESERVED			GLDCNT			GLDPRD	
R-0			R			R/W	
0			0			0	
7	6	5	4	3	2	1	0
GLDPRD	RESERVED	OSHTMODE	GLDMODE				GLD
R/W	R-0	R/W	R/W				R/W
0	0	0	0				0

Access Types Legend

Table 3-442. GLDCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	R-0		Reserved
12 - 10	GLDCNT	R	0h	Global Load Strobe Counter Register These bits indicate how many selected events have occurred: 000: No events 001: 1 event 010: 2 events 011: 3 events 100: 4 events 101: 5 events 110: 6 events 111: 7 events
9 - 7	GLDPRD	R/W	0h	Global Load Strobe Period Select Register These bits select how many selected events need to occur before a load strobe is generated 000: Disable counter 001: Generate strobe on GLDCNT = 001 (1st event) 010: Generate strobe on GLDCNT = 010 (2nd event) 011: Generate strobe on GLDCNT = 011 (3rd event) 100: Generate strobe on GLDCNT = 011 (4th event) 101: Generate strobe on GLDCNT = 001 (5th event) 110: Generate strobe on GLDCNT = 010 (6th event) 111: Generate strobe on GLDCNT = 011 (7th event)
6	RESERVED	R-0		Reserved
5	OSHTMODE	R/W	0h	One Shot Load Mode Control Bit 0: One shot load mode is disabled and shadow to active loading happens continuously on all the chosen load strobes. 1: One shot mode is active. All load strobes are blocked until GLDCTL2[OSHTLD] is written with 1. Note: One Shot mode can only be used with global shadow to active load mode enabled (GLDCTL[GLD]=1)
4 - 1	GLDMODE	R/W	0h	Global Load Pulse selection for Shadow to Active Mode Reloads 0000: Load on Counter = 0 (CNT_ZRO) 0001: Load on Counter = Period (PRD_EQ) 0010: Load on either Counter = 0, or Counter = Period 0011: Load on SYNCEVT - this is logical OR of DCAEVT1.sync, DCBEVT1.sync, EPWMxSYNCI and TBCTL[SWFSYNC] 0100: Load on SYNCEVT or CNT_ZRO 0101: Load on SYNCEVT or PRD_EQ 0110: Load on SYNCEVT or CNT_ZRO or PRD_EQ 1000: Load on Counter = CMPCU (CMPC_EQ counter incrementing) 1001: Load on Counter = CMPCD (CMPC_EQ counter decrementing) 1010: Load on Counter = CMPDU (CMPD_EQ counter incrementing) 1011: Load on Counter = CMPDD (CMPD_EQ counter decrementing) 1100: Reserved ... 1110: Reserved 1111: Load on GLDCTL2[GFRCLD] write

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Table 3-442. GLDCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	GLD	R/W	0h	Global Shadow to Active Load Event Control 0: Shadow to active reload for all shadowed registers happens as per the individual reload control bits specified (Compatible with previous EPWM versions). 1: When set, all the shadow to active reload events are defined by GLDMODE bits in GLDCTL register. All the shadow registers use same reload pulse from shadow to active reloading. Individual LOADMODE bits are ignored.

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3.9.22 CONTROLSS_Gm_EPWMn_GLDCFG Registers

3.9.22.1 Gm_EPWMn_GLDCFG Register (Offset = 6Ah) [reset = h]

Short Description: Global PWM Load Config Register

Long Description:

Return to Summary Table

Table 3-443. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-95. GLDCFG Name Register

15	14	13	12	11	10	9	8
RESERVED					AQCSFRC	AQCTLB_AQCTLB2	AQCTLA_AQCTLA2
R-0					R/W	R/W	R/W
0					0	0	0
7	6	5	4	3	2	1	0
DBCTL	DBFED_DBFEDHR	DBRED_DBREDHR	CMPD	CMPC	CMPB_CMPBHR	CMPA_CMPAHR	TBPRD_TBPRDHR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-444. GLDCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	R-0		Reserved
10	AQCSFRC	R/W	0h	Global load event configuration for AQCSFRC 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1
9	AQCTLB_AQCTLB2	R/W	0h	Global load event configuration for AQCTLB_AQCTLB2 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1
8	AQCTLA_AQCTLA2	R/W	0h	Global load event configuration for AQCTLA_AQCTLA2 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1
7	DBCTL	R/W	0h	Global load event configuration for DBCTL 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1
6	DBFED_DBFEDHR	R/W	0h	Global load event configuration for DBFED_DBFEDHR 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1
5	DBRED_DBREDHR	R/W	0h	Global load event configuration for DBRED_DBREDHR 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1
4	CMPD	R/W	0h	Global load event configuration for CMPD 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1

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Table 3-444. GLDCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CMPC	R/W	0h	Global load event configuration for CMPC 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1
2	CMPB_CMPBHR	R/W	0h	Global load event configuration for CMPB_CMPBHR 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1
1	CMPA_CMPAHR	R/W	0h	Global load event configuration for CMPA_CMPAHR 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1
0	TBPRD_TBPRDHR	R/W	0h	Global load event configuration for TBPRD_TBPRDHR 0: Registers use local reload configuration even if GLDCTL(GLD)=1 (reload is compatible with previous EPWMs) 1: Registers use global load configuration if this bit is set and GLDCTL(GLD)=1

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3.9.23 CONTROLSS_Gm_EPWMn_EPWMXLINK Registers

3.9.23.1 Gm_EPWMn_EPWMXLINK Register (Offset = 70h) [reset = h]

Short Description: EPWMx Link Register This register controls which EPWMs are linked to other EPWM modules. The default reset value will vary for each module. The reset value will link each EPWM module to itself to prevent unintentional linking of modules.

Long Description:

Return to Summary Table

Table 3-445. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-96. EPWMXLINK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	GLDCTL2LINK					CMPDLINK					CMPCLINK				
R-0	R/W					R/W					R/W				
0	0					0					0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	CMPBLINK					CMPALINK					TBPRDLINK				
R-0	R/W					R/W					R/W				
0	0					0					0				

Access Types Legend

Table 3-446. EPWMXLINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R-0		Reserved
30 - 26	GLDCTL2LINK	R/W	0h	GLDCTL2 Link Bits Writes to the GLDCTL2 registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's GLDCTL2 registers. 00000: ePWM1 00001: ePWM2 00010: ePWM3 00011: ePWM4 00100: ePWM5 00101: ePWM6 00110: ePWM7 00111: ePWM8 01000: ePWM9 01001: ePWM10 01010: ePWM11 01011: ePWM12 01100: ePWM13 ... 11111: ePWM32
25 - 21	CMPDLINK	R/W	0h	CMPD Link Bits Writes to the CMPD registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's CMPD registers. 00000: ePWM1 00001: ePWM2 00010: ePWM3 00011: ePWM4 00100: ePWM5 00101: ePWM6 00110: ePWM7 00111: ePWM8 01000: ePWM9 01001: ePWM10 01010: ePWM11 01011: ePWM12 01100: ePWM13 ... 11111: ePWM32
20 - 16	CMPCLINK	R/W	0h	CMPC Link Bits Writes to the CMPC registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's CMPC registers. 00000: ePWM1 00001: ePWM2 00010: ePWM3 00011: ePWM4 00100: ePWM5 00101: ePWM6 00110: ePWM7 00111: ePWM8 01000: ePWM9 01001: ePWM10 01010: ePWM11 01011: ePWM12 01100: ePWM13 ... 11111: ePWM32
15	RESERVED	R-0		Reserved

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Table 3-446. EPWMXLINK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14 - 10	CMPBLINK	R/W	0h	CMPB_CMPBHR Link Bits Writes to the CMPB_CMPBHR registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's CMPB_CMPBHR registers. 00000: ePWM1 00001: ePWM2 00010: ePWM3 00011: ePWM4 00100: ePWM5 00101: ePWM6 00110: ePWM7 00111: ePWM8 01000: ePWM9 01001: ePWM10 01010: ePWM11 01011: ePWM12 01100: ePWM13 ... 11111: ePWM32
9 - 5	CMPALINK	R/W	0h	CMPA_CMPAHR Link Bits Writes to the CMPA_CMPAHR registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's CMPA_CMPAHR registers. 00000: ePWM1 00001: ePWM2 00010: ePWM3 00011: ePWM4 00100: ePWM5 00101: ePWM6 00110: ePWM7 00111: ePWM8 01000: ePWM9 01001: ePWM10 01010: ePWM11 01011: ePWM12 01100: ePWM13 ... 11111: ePWM32
4 - 0	TBPRDLINK	R/W	0h	TBPRD_TBPRDHR Link Bits Writes to the TBPRD:TBPRDHR registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's TBPRD_TBPRDHR registers. 00000: ePWM1 00001: ePWM2 00010: ePWM3 00011: ePWM4 00100: ePWM5 00101: ePWM6 00110: ePWM7 00111: ePWM8 01000: ePWM9 01001: ePWM10 01010: ePWM11 01011: ePWM12 01100: ePWM13 ... 11111: ePWM32

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3.9.24 CONTROLSS_Gm_EPWMn_EPWMXLINK2 Registers

3.9.24.1 Gm_EPWMn_EPWMXLINK2 Register (Offset = 74h) [reset = h]

Short Description: EPWMx Link 2 Register This register controls which EPWMs are linked to other EPWM modules. The default reset value will vary for each module. The reset value will link each EPWM module to itself to prevent unintentional linking of modules.

Long Description:

Return to Summary Table

Table 3-447. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-97. EPWMXLINK2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						DBFEDLINK					DBREDLINK				
R-0						R/W					R/W				
0						0					0				

Access Types Legend

Table 3-448. EPWMXLINK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 10	RESERVED	R-0		Reserved
9 - 5	DBFEDLINK	R/W	0h	DBFED_DBFEDHR Link Bits Writes to the DBFED:DBFEDHR registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's DBFED_DBFEDHR registers. 00000: ePWM1 00001: ePWM2 00010: ePWM3 00011: ePWM4 00100: ePWM5 00101: ePWM6 00110: ePWM7 00111: ePWM8 01000: ePWM9 01001: ePWM10 01010: ePWM11 01011: ePWM12 01100: ePWM13 ... 11111: ePWM32
4 - 0	DBREDLINK	R/W	0h	DBRED_DBREDHR Link Bits Writes to the DBRED:DBREDHR registers in the ePWM module selected by the following bit selections results in a simultaneous write to the current ePWM module's DBRED_DBREDHR registers. 00000: ePWM1 00001: ePWM2 00010: ePWM3 00011: ePWM4 00100: ePWM5 00101: ePWM6 00110: ePWM7 00111: ePWM8 01000: ePWM9 01001: ePWM10 01010: ePWM11 01011: ePWM12 01100: ePWM13 ... 11111: ePWM32

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3.9.25 CONTROLSS_Gm_EPWMn_ETEST Registers

3.9.25.1 Gm_EPWMn_ETEST Register (Offset = 7Ah) [reset = h]

Short Description: EPWM Test Register

Long Description:

Return to Summary Table

Table 3-449. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-98. ETEST Name Register

15	14	13	12	11	10	9	8
RESERVED							
R-0							
0							
7	6	5	4	3	2	1	0
RESERVED							CMPFIX_OVERRIDE
R-0							R/W
0							1

Access Types Legend

Table 3-450. ETEST Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 1	RESERVED	R-0		Reserved
0	CMPFIX_OVERRIDE	R/W	1h	0: Bug fix overriden 1: Bug fix takes effect

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3.9.26 CONTROLSS_Gm_EPWMn_EPWMREV Registers

3.9.26.1 Gm_EPWMn_EPWMREV Register (Offset = 7Ch) [reset = h]

Short Description: EPWM Revision Register

Long Description:

Return to Summary Table

Table 3-451. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-99. EPWMREV Name Register

15	14	13	12	11	10	9	8
TYPE							
R							
5							
7	6	5	4	3	2	1	0
REV							
R							
12648430							

Access Types Legend

Table 3-452. EPWMREV Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	TYPE	R	5h	EPWM Type Bits: These bits specify the EPWM type. These bits are changed if the functionality of the EPWM is changed or any feature is added or removed:
7 - 0	REV	R	C0FFEEh	EPWM Silicon Revision Bits: These bits specify the EPWM revision. These bits are changed if any bug fixes are performed:

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3.9.27 CONTROLSS_Gm_EPWMn_HRPWMREV Registers

3.9.27.1 Gm_EPWMn_HRPWMREV Register (Offset = 7Eh) [reset = h]

Short Description: High Resolution Revision Register

Long Description:

Return to Summary Table

Table 3-453. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-100. HRPWMREV Name Register

15	14	13	12	11	10	9	8
TYPE							
R							
3							
7	6	5	4	3	2	1	0
REV							
R							
0							

Access Types Legend

Table 3-454. HRPWMREV Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	TYPE	R	3h	HRPWM Type Bits: These bits specify the HRPWM type. These bits are changed if the functionality of the HRPWM is changed or any feature is added or removed:
7 - 0	REV	R	0h	HRPWM Silicon Revision Bits: These bits specify the HRPWM revision. These bits are changed if any bug fixes are performed:

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3.9.28 CONTROLSS_Gm_EPWMn_AQCTLA Registers

3.9.28.1 Gm_EPWMn_AQCTLA Register (Offset = 80h) [reset = h]

Short Description: Action Qualifier Control Register For Output A

Long Description:

Return to Summary Table

Table 3-455. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-101. AQCTLA Name Register

15	14	13	12	11	10	9	8
RESERVED				CBD		CBU	
R-0				R/W		R/W	
0				0		0	
7	6	5	4	3	2	1	0
CAD		CAU		PRD		ZRO	
R/W		R/W		R/W		R/W	
0		0		0		0	

Access Types Legend

Table 3-456. AQCTLA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R-0		Reserved
11 - 10	CBD	R/W	0h	Action When TBCTR = CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
9 - 8	CBU	R/W	0h	Action When TBCTR = CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
7 - 6	CAD	R/W	0h	Action When TBCTR = CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
5 - 4	CAU	R/W	0h	Action When TBCTR = CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
3 - 2	PRD	R/W	0h	Action When TBCTR = TBPRD Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.

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Table 3-456. AQCTLA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1 - 0	ZRO	R/W	0h	Action When TBCTR = 0 Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.

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3.9.29 CONTROLSS_Gm_EPWMn_AQCTLA2 Registers

3.9.29.1 Gm_EPWMn_AQCTLA2 Register (Offset = 82h) [reset = h]

Short Description: Additional Action Qualifier Control Register For Output A

Long Description:

Return to Summary Table

Table 3-457. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-102. AQCTLA2 Name Register

15	14	13	12	11	10	9	8
RESERVED							
R-0							
0							
7	6	5	4	3	2	1	0
T2D		T2U		T1D		T1U	
R/W		R/W		R/W		R/W	
0		0		0		0	

Access Types Legend

Table 3-458. AQCTLA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R-0		Reserved
7 - 6	T2D	R/W	0h	Action when event occurs on T2 in DOWN-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
5 - 4	T2U	R/W	0h	Action when event occurs on T2 in UP-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
3 - 2	T1D	R/W	0h	Action when event occurs on T1 in DOWN-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.
1 - 0	T1U	R/W	0h	Action when event occurs on T1 in UP-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxA output low. 10: Set: force EPWMxA output high. 11: Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.

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3.9.30 CONTROLSS_Gm_EPWMn_AQCTLB Registers

3.9.30.1 Gm_EPWMn_AQCTLB Register (Offset = 84h) [reset = h]

Short Description: Action Qualifier Control Register For Output B

Long Description:

Return to Summary Table

Table 3-459. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-103. AQCTLB Name Register

15	14	13	12	11	10	9	8
RESERVED				CBD		CBU	
R-0				R/W		R/W	
0				0		0	
7	6	5	4	3	2	1	0
CAD		CAU		PRD		ZRO	
R/W		R/W		R/W		R/W	
0		0		0		0	

Access Types Legend

Table 3-460. AQCTLB Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R-0		Reserved
11 - 10	CBD	R/W	0h	Action When TBCTR = CMPB on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
9 - 8	CBU	R/W	0h	Action When TBCTR = CMPB on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
7 - 6	CAD	R/W	0h	Action When TBCTR = CMPA on Down Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
5 - 4	CAU	R/W	0h	Action When TBCTR = CMPA on Up Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
3 - 2	PRD	R/W	0h	Action When TBCTR = TBPRD Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.

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Table 3-460. AQCTLB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1 - 0	ZRO	R/W	0h	Action When TBCTR = 0 Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.

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3.9.31 CONTROLSS_Gm_EPWMn_AQCTLB2 Registers

3.9.31.1 Gm_EPWMn_AQCTLB2 Register (Offset = 86h) [reset = h]

Short Description: Additional Action Qualifier Control Register For Output B

Long Description:

Return to Summary Table

Table 3-461. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-104. AQCTLB2 Name Register

15	14	13	12	11	10	9	8
RESERVED							
R-0							
0							
7	6	5	4	3	2	1	0
T2D		T2U		T1D		T1U	
R/W		R/W		R/W		R/W	
0		0		0		0	

Access Types Legend

Table 3-462. AQCTLB2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R-0		Reserved
7 - 6	T2D	R/W	0h	Action when event occurs on T2 in DOWN-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
5 - 4	T2U	R/W	0h	Action when event occurs on T2 in UP-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
3 - 2	T1D	R/W	0h	Action when event occurs on T1 in DOWN-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.
1 - 0	T1U	R/W	0h	Action when event occurs on T1 in UP-Count Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 00: Do nothing (action disabled) 01: Clear: force EPWMxB output low. 10: Set: force EPWMxB output high. 11: Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.

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3.9.32 CONTROLSS_Gm_EPWMn_AQSFRC Registers

3.9.32.1 Gm_EPWMn_AQSFRC Register (Offset = 8Eh) [reset = h]

Short Description: Action Qualifier Software Force Register

Long Description:

Return to Summary Table

Table 3-463. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-105. AQSFRC Name Register

15	14	13	12	11	10	9	8
RESERVED							
R-0							
0							
7	6	5	4	3	2	1	0
RLDCSF		OTSFB	ACTSFB		OTSFA	ACTSFA	
R/W		R-0/W	R/W		R-0/W	R/W	
0		0	0		0	0	

Access Types Legend

Table 3-464. AQSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R-0		Reserved
7 - 6	RLDCSF	R/W	0h	AQCSFRC Active Register Reload From Shadow Options 00: Load on event counter equals zero 01: Load on event counter equals period 10: Load on event counter equals zero or counter equals period 11: Load immediately (the active register is directly accessed by the CPU and is not loaded from the shadow register).
5	OTSFB	R-0/W	0h	One-Time Software Forced Event on Output B 0: Writing a 0 (zero) has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete (i.e., a forced event is initiated.). This is a one-shot forced event. It can be overridden by another subsequent event on output B. 1: Initiates a single software forced event
4 - 3	ACTSFB	R/W	0h	Action When One-Time Software Force B is Invoked 00: Does nothing (action disabled) 01: Clear (low) 10: Set (high) 11: Toggle (Low -' High, High -' Low) Note: This action is not qualified by counter direction (CNT_dir)
2	OTSFA	R-0/W	0h	One-Time Software Forced Event on Output A 0: Writing a 0 (zero) has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete (i.e., a forced event is initiated). This is a one-shot forced event. It can be overridden by another subsequent event on output A. 1: Initiates a single software forced event
1 - 0	ACTSFA	R/W	0h	Action When One-Time Software Force A Is Invoked 00: Does nothing (action disabled) 01: Clear (low) 10: Set (high) 11: Toggle (Low -' High, High -' Low) Note: This action is not qualified by counter direction (CNT_dir)

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3.9.33 CONTROLSS_Gm_EPWMn_AQCSFRC Registers

3.9.33.1 Gm_EPWMn_AQCSFRC Register (Offset = 92h) [reset = h]

Short Description: Action Qualifier Continuous S/W Force Register

Long Description:

Return to Summary Table

Table 3-465. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-106. AQCSFRC Name Register

15	14	13	12	11	10	9	8
RESERVED							
R-0							
0							
7	6	5	4	3	2	1	0
RESERVED				CSFB		CSFA	
R-0				R/W		R/W	
0				0		0	

Access Types Legend

Table 3-466. AQCSFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	R-0		Reserved
3 - 2	CSFB	R/W	0h	Continuous Software Force on Output B In immediate mode, a continuous force takes effect on the next TBCLK edge. In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register. To configure shadow mode, use AQSFRC[RLDCSF]. 00: Software forcing is disabled and has no effect 01: Forces a continuous low on output B 10: Forces a continuous high on output B 11: Software forcing is disabled and has no effect
1 - 0	CSFA	R/W	0h	Continuous Software Force on Output A In immediate mode, a continuous force takes effect on the next TBCLK edge. In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register. 00: Software forcing is disabled and has no effect 01: Forces a continuous low on output A 10: Forces a continuous high on output A 11: Software forcing is disabled and has no effect

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3.9.34 CONTROLSS_Gm_EPWMn_DBREDHR Registers

3.9.34.1 Gm_EPWMn_DBREDHR Register (Offset = A0h) [reset = h]

Short Description: Dead-Band Generator Rising Edge Delay High Resolution Mirror Register

Long Description:

Return to Summary Table

Table 3-467. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-107. DBREDHR Name Register

15	14	13	12	11	10	9	8
DBREDHR							RESERVED
R/W							R
0							0
7	6	5	4	3	2	1	0
DBREDHR_DELAY							RESERVED
R							R
0							0

Access Types Legend

Table 3-468. DBREDHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9	DBREDHR	R/W	0h	Dead Band Rising Edge Delay High Resolution Bits
8	RESERVED	R		Reserved
7 - 1	DBREDHR_DELAY	R	0h	These 7-bits contain the results of OTTO calculation (if auto-conversion is enabled)
0	RESERVED	R		Reserved

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3.9.35 CONTROLSS_Gm_EPWMn_DBRED Registers

3.9.35.1 Gm_EPWMn_DBRED Register (Offset = A2h) [reset = h]

Short Description: Dead-Band Generator Rising Edge Delay High Resolution Mirror Register

Long Description:

Return to Summary Table

Table 3-469. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-108. DBRED Name Register

15	14	13	12	11	10	9	8
RESERVED		DBRED					
R		R/W					
0		0					
7	6	5	4	3	2	1	0
DBRED							
R/W							
0							

Access Types Legend

Table 3-470. DBRED Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	RESERVED	R		Reserved
13 - 0	DBRED	R/W	0h	Rising edge delay value

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3.9.36 CONTROLSS_Gm_EPWMn_DBFEDHR Registers

3.9.36.1 Gm_EPWMn_DBFEDHR Register (Offset = A4h) [reset = h]

Short Description: Dead-Band Generator Falling Edge Delay High Resolution Register

Long Description:

Return to Summary Table

Table 3-471. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-109. DBFEDHR Name Register

15	14	13	12	11	10	9	8
DBFEDHR							RESERVED
R/W							R
0							0
7	6	5	4	3	2	1	0
DBFEDHR_DELAY							RESERVED
R							R
0							0

Access Types Legend

Table 3-472. DBFEDHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9	DBFEDHR	R/W	0h	Dead Band Falling Edge Delay High Resolution Bits
8	RESERVED	R		Reserved
7 - 1	DBFEDHR_DELAY	R	0h	These 7-bits contain the results of OTTO calculation (if auto-conversion is enabled)
0	RESERVED	R		Reserved

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3.9.37 CONTROLSS_Gm_EPWMn_DBFED Registers

3.9.37.1 Gm_EPWMn_DBFED Register (Offset = A6h) [reset = h]

Short Description: Dead-Band Generator Falling Edge Delay Count Register

Long Description:

Return to Summary Table

Table 3-473. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-110. DBFED Name Register

15	14	13	12	11	10	9	8
RESERVED		DBFED					
R		R/W					
0		0					
7	6	5	4	3	2	1	0
DBFED							
R/W							
0							

Access Types Legend

Table 3-474. DBFED Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	RESERVED	R		Reserved
13 - 0	DBFED	R/W	0h	Falling Edge Delay Count 14-bit counter

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3.9.38 CONTROLSS_Gm_EPWMn_TBPHS Registers

3.9.38.1 Gm_EPWMn_TBPHS Register (Offset = C0h) [reset = h]

Short Description: Time Base Phase High

Long Description:

Return to Summary Table

Table 3-475. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-111. TBPHS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBPHS															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBPHSHR															
R/W															
0															

Access Types Legend

Table 3-476. TBPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	TBPHS	R/W	0h	Phase Offset Register These bits set time-base counter phase of the selected ePWM relative to the time-base that is supplying the synchronization input signal. - If TBCTL[PHSEN] = 0, then the synchronization event is ignored and the time-base counter is not loaded with the phase. - If TBCTL[PHSEN] = 1, then the time-base counter (TBCTR) will be loaded with the phase (TBPHS) when a synchronization event occurs. The synchronization event can be initiated by the input synchronization signal (EPWMxSYNCI) or by a software forced synchronization.
15 - 0	TBPHSHR	R/W	0h	Phase Offset (High Resolution) Register. TBPHSHR must not be used. Instead TRREM (HRPWM remainder register) must be used to mimic the functionality of TBPHSHR. The lower 8 bits in this register are ignored - writes are ignored and reads return zero

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3.9.39 CONTROLSS_Gm_EPWMn_TBPRDHR Registers

3.9.39.1 Gm_EPWMn_TBPRDHR Register (Offset = C4h) [reset = h]

Short Description: Time Base Period High Resolution Register

Long Description:

Return to Summary Table

Table 3-477. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-112. TBPRDHR Name Register

15	14	13	12	11	10	9	8
TBPRDHR							
R/W							
0							
7	6	5	4	3	2	1	0
TBPRDHR							
R/W							
0							

Access Types Legend

Table 3-478. TBPRDHR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	TBPRDHR	R/W	0h	Period High Resolution Bits The upper 8-bits contain the high-resolution portion of the period value. The TBPRDHR register is not affected by the TBCTL[PRDLD] bit. Reads from this register always reflect the shadow register. Likewise writes are also to the shadow register. The TBPRDHR register is only used when the high resolution period feature is enabled. This register is only available with ePWM modules which support high-resolution period control. The lower 8 bits in this register are ignored - writes are ignored and reads return zero

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3.9.40 CONTROLSS_Gm_EPWMn_TBPRD Registers

3.9.40.1 Gm_EPWMn_TBPRD Register (Offset = C6h) [reset = h]

Short Description: Time Base Period Register

Long Description:

Return to Summary Table

Table 3-479. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-113. TBPRD Name Register

15	14	13	12	11	10	9	8
TBPRD							
R/W							
0							
7	6	5	4	3	2	1	0
TBPRD							
R/W							
0							

Access Types Legend

Table 3-480. TBPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	TBPRD	R/W	0h	Time Base Period Register These bits determine the period of the time-base counter. This sets the PWM frequency. Shadowing of this register is enabled and disabled by the TBCTL[PRDLD] bit. By default this register is shadowed. - If TBCTL[PRDLD] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the active register will be loaded from the shadow register when the time-base counter equals zero. - If TBCTL[PRDLD] = 1, then the shadow is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware. - The active and shadow registers share the same memory map address.

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3.9.41 CONTROLSS_Gm_EPWMn_TBPRDHRB Registers

3.9.41.1 Gm_EPWMn_TBPRDHRB Register (Offset = C8h) [reset = h]

Short Description: Calculation Result for EPWMxB

Long Description:

Return to Summary Table

Table 3-481. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-114. TBPRDHRB Name Register

15	14	13	12	11	10	9	8
TBPRDHRB							
R/W							
0							
7	6	5	4	3	2	1	0
TBPRDHRB_DELAY							
R/W							
0							

Access Types Legend

Table 3-482. TBPRDHRB Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	TBPRDHRB	R/W	0h	TBPRD High Resolution Calculation (2) Results for EPWMxB HRPWM Equations
7 - 0	TBPRDHRB_DELAY	R/W	0h	TBPRDHRB Delay

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3.9.42 CONTROLSS_Gm_EPWMn_CMPA Registers

3.9.42.1 Gm_EPWMn_CMPA Register (Offset = D4h) [reset = h]

Short Description: Counter Compare A Register

Long Description:

Return to Summary Table

Table 3-483. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-115. CMPA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CMPA															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMPAHR															
R/W															
0															

Access Types Legend

Table 3-484. CMPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CMPA	R/W	0h	Compare A Register The value in the active CMPA register is continuously compared to the time-base counter (TBCTR). When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare A" event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers. The actions that can be defined in the AQCTLA and AQCTLB registers include: - Do nothing the event is ignored. - Clear: Pull the EPWMxA and/or EPWMxB signal low - Set: Pull the EPWMxA and/or EPWMxB signal high - Toggle the EPWMxA and/or EPWMxB signal Shadowing of this register is enabled and disabled by the CMPCTL[SHDWAMODE] bit. By default this register is shadowed. - If CMPCTL[SHDWAMODE] = 0, then the shadow is enabled and anywrite or read will automatically go to the shadow register. In this case, the CMPCTL[LOADAMODE] bit field determines which event will load the active register from the shadow register. - Before a write, the CMPCTL[SHDWAFULL] bit can be read to determine if the shadow register is currently full. - If CMPCTL[SHDWAMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware. - In either mode, the active and shadow registers share the same memory map address.
15 - 0	CMPAHR	R/W	0h	Compare A HRPWM Extension Register The UPPER 8-bits contain the high-resolution portion (most significant 8-bits) of the counter-compare A value. CMPA:CMPAHR can be accessed in a single 32-bit read/write. Shadowing is enabled and disabled by the CMPCTL[SHDWAMODE] bit as described for the CMPA register. The lower 8 bits in this register are ignored

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3.9.43 CONTROLSS_Gm_EPWMn_CMPB Registers

3.9.43.1 Gm_EPWMn_CMPB Register (Offset = D8h) [reset = h]

Short Description: Compare B Register

Long Description:

Return to Summary Table

Table 3-485. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-116. CMPB Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CMPB															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMPBHR															
R/W															
0															

Access Types Legend

Table 3-486. CMPB Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CMPB	R/W	0h	Compare B Register The value in the active CMPB register is continuously compared to the time-base counter (TBCTR). When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare B" event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers. The actions that can be defined in the AQCTLA and AQCTLB registers include: - Do nothing the event is ignored. - Clear: Pull the EPWMxA and/or EPWMxB signal low - Set: Pull the EPWMxA and/or EPWMxB signal high - Toggle the EPWMxA and/or EPWMxB signal Shadowing of this register is enabled and disabled by the CMPCTL[SHDWBMODE] bit. By default this register is shadowed. - If CMPCTL[SHDWBMODE] = 0, then the shadow is enabled and anywrite or read will automatically go to the shadow register. In this case, the CMPCTL[LOADBMODE] bit field determines which event will load the active register from the shadow register. - Before a write, the CMPCTL[SHDWBFULL] bit can be read to determine if the shadow register is currently full. - If CMPCTL[SHDWBMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware. - In either mode, the active and shadow registers share the same memory map address.
15 - 0	CMPBHR	R/W	0h	Compare B High Resolution Bits The lower 8 bits in this register are ignored

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3.9.44 CONTROLSS_Gm_EPWMn_CMPC Registers

3.9.44.1 Gm_EPWMn_CMPC Register (Offset = DEh) [reset = h]

Short Description: Counter Compare C Register LINK feature access should always be 16-bit

Long Description:

Return to Summary Table

Table 3-487. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-117. CMPC Name Register

15	14	13	12	11	10	9	8
CMPC							
R/W							
0							
7	6	5	4	3	2	1	0
CMPC							
R/W							
0							

Access Types Legend

Table 3-488. CMPC Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	CMPC	R/W	0h	Compare C Register The value in the active CMPC register is continuously compared to the time-base counter (TBCTR). When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare C" event. Shadowing of this register is enabled and disabled by the CMPCTL2[SHDWCMODE] bit. By default this register is shadowed. - If CMPCTL2[SHDWCMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL2[LOADCMODE] bit field determines which event will load the active register from the shadow register: - If CMPCTL2[SHDWCMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register that is, the register actively controlling the hardware. - In either mode, the active and shadow registers share the same memory map address.

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3.9.45 CONTROLSS_Gm_EPWMn_CMPD Registers

3.9.45.1 Gm_EPWMn_CMPD Register (Offset = E2h) [reset = h]

Short Description: Counter Compare D Register LINK feature access should always be 16-bit

Long Description:

Return to Summary Table

Table 3-489. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-118. CMPD Name Register

15	14	13	12	11	10	9	8
CMPD							
R/W							
0							
7	6	5	4	3	2	1	0
CMPD							
R/W							
0							

Access Types Legend

Table 3-490. CMPD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	CMPD	R/W	0h	Compare D Register The value in the active CMPD register is continuously compared to the time-base counter (TBCTR). When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare D" event. Shadowing of this register is enabled and disabled by the CMPCTL2[SHDWDMODE] bit. By default this register is shadowed. - If CMPCTL2[SHDWDMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL2[LOADDMODE] bit field determines which event will load the active register from the shadow register: - If CMPCTL2[SHDWDMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register that is, the register actively controlling the hardware. - In either mode, the active and shadow registers share the same memory map address.

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3.9.46 CONTROLSS_Gm_EPWMn_GLDCTL2 Registers

3.9.46.1 Gm_EPWMn_GLDCTL2 Register (Offset = E8h) [reset = h]

Short Description: Global PWM Load Control Register 2

Long Description:

Return to Summary Table

Table 3-491. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-119. GLDCTL2 Name Register

15	14	13	12	11	10	9	8
RESERVED							
R-0							
0							
7	6	5	4	3	2	1	0
RESERVED						GFRCLD	OSHTLD
R-0						R-0/W	R-0/W
0						0	0

Access Types Legend

Table 3-492. GLDCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 2	RESERVED	R-0		Reserved
1	GFRCLD	R-0/W	0h	Force Load Event in One Shot Mode 0: Writing of 0 will be ignored. Always reads back a 0. 1: Force one load event at the input of the event pre-scale counter as shown in the diagram below. This bit is intended to be used for testing and/or software force loading of the events in global load mode.
0	OSHTLD	R-0/W	0h	Enable Reload Event in One Shot Mode 0: Writing of 0 will be ignored. Always reads back a 0. 1: Turns the one shot latch condition ON. Upon occurrence of a chosen load strobe, one shadow to active reload occurs and the latch will be cleared. Hence writing 1 to this bit would allow one load strobe event to pass through and block further strobe events.

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3.9.47 CONTROLSS_Gm_EPWMn_SWVDELVAL Registers

3.9.47.1 Gm_EPWMn_SWVDELVAL Register (Offset = EEh) [reset = h]

Short Description: Software Valley Mode Delay Register

Long Description:

Return to Summary Table

Table 3-493. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-120. SWVDELVAL Name Register

15	14	13	12	11	10	9	8
SWVDELVAL							
R/W							
0							
7	6	5	4	3	2	1	0
SWVDELVAL							
R/W							
0							

Access Types Legend

Table 3-494. SWVDELVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SWVDELVAL	R/W	0h	Software Valley Delay Value Register This register can be optionally used define offset value for the hardware calculated delay HWDELAYVAL as defined in VCAPCTL[VDELAYDIV] bits.

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3.9.48 CONTROLSS_Gm_EPWMn_TZSEL Registers

3.9.48.1 Gm_EPWMn_TZSEL Register (Offset = 100h) [reset = h]

Short Description: Trip Zone Select Register

Long Description:

Return to Summary Table

Table 3-495. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-121. TZSEL Name Register

15	14	13	12	11	10	9	8
DCBEVT1	DCAEVT1	OSHT6	OSHT5	OSHT4	OSHT3	OSHT2	OSHT1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
DCBEVT2	DCAEVT2	CBC6	CBC5	CBC4	CBC3	CBC2	CBC1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-496. TZSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DCBEVT1	R/W	0h	Digital Compare Output B Event 1 Select 0: Disable DCBEVT1 as one-shot-trip source for this ePWM module. 1: Enable DCBEVT1 as one-shot-trip source for this ePWM module.
14	DCAEVT1	R/W	0h	Digital Compare Output A Event 1 Select 0: Disable DCAEVT1 as one-shot-trip source for this ePWM module. 1: Enable DCAEVT1 as one-shot-trip source for this ePWM module.
13	OSHT6	R/W	0h	Trip-zone 6 (TZ6) Select 0: Disable TZ6 as a one-shot trip source for this ePWM module 1: Enable TZ6 as a one-shot trip source for this ePWM module
12	OSHT5	R/W	0h	Trip-zone 5 (TZ5) Select 0: Disable TZ5 as a one-shot trip source for this ePWM module 1: Enable TZ5 as a one-shot trip source for this ePWM module
11	OSHT4	R/W	0h	Trip-zone 4 (TZ4) Select 0: Disable TZ4 as a one-shot trip source for this ePWM module 1: Enable TZ4 as a one-shot trip source for this ePWM module
10	OSHT3	R/W	0h	Trip-zone 3 (TZ3) Select 0: Disable TZ3 as a one-shot trip source for this ePWM module 1: Enable TZ3 as a one-shot trip source for this ePWM module
9	OSHT2	R/W	0h	Trip-zone 2 (TZ2) Select 0: Disable TZ2 as a one-shot trip source for this ePWM module 1: Enable TZ2 as a one-shot trip source for this ePWM module
8	OSHT1	R/W	0h	Trip-zone 1 (TZ1) Select 0: Disable TZ1 as a one-shot trip source for this ePWM module 1: Enable TZ1 as a one-shot trip source for this ePWM module
7	DCBEVT2	R/W	0h	Digital Compare Output B Event 2 Select 0: Disable DCBEVT2 as a CBC trip source for this ePWM module 1: Enable DCBEVT2 as a CBC trip source for this ePWM module
6	DCAEVT2	R/W	0h	Digital Compare Output A Event 2 Select 0: Disable DCAEVT2 as a CBC trip source for this ePWM module 1: Enable DCAEVT2 as a CBC trip source for this ePWM module

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Table 3-496. TZSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CBC6	R/W	0h	Trip-zone 6 (TZ6) Select 0: Disable TZ6 as a CBC trip source for this ePWM module 1: Enable TZ6 as a CBC trip source for this ePWM module
4	CBC5	R/W	0h	Trip-zone 5 (TZ5) Select 0: Disable TZ5 as a CBC trip source for this ePWM module 1: Enable TZ5 as a CBC trip source for this ePWM module
3	CBC4	R/W	0h	Trip-zone 4 (TZ4) Select 0: Disable TZ4 as a CBC trip source for this ePWM module 1: Enable TZ4 as a CBC trip source for this ePWM module
2	CBC3	R/W	0h	Trip-zone 3 (TZ3) Select 0: Disable TZ3 as a CBC trip source for this ePWM module 1: Enable TZ3 as a CBC trip source for this ePWM module
1	CBC2	R/W	0h	Trip-zone 2 (TZ2) Select 0: Disable TZ2 as a CBC trip source for this ePWM module 1: Enable TZ2 as a CBC trip source for this ePWM module
0	CBC1	R/W	0h	Trip-zone 1 (TZ1) Select 0: Disable TZ1 as a CBC trip source for this ePWM module 1: Enable TZ1 as a CBC trip source for this ePWM module

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3.9.49 CONTROLSS_Gm_EPWMn_TZSEL2 Registers

3.9.49.1 Gm_EPWMn_TZSEL2 Register (Offset = 102h) [reset = h]

Short Description: Trip Zone Select Register 2

Long Description:

Return to Summary Table

Table 3-497. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-122. TZSEL2 Name Register

15	14	13	12	11	10	9	8
RESERVED							CAPEVTOST
R-0							R/W
0							0
7	6	5	4	3	2	1	0
RESERVED							CAPEVTCBC
R-0							R/W
0							0

Access Types Legend

Table 3-498. TZSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9	RESERVED	R-0		Reserved
8	CAPEVTOST	R/W	0h	CAPEVT OST Select 0: Disable CAPEVT as a one-shot trip source for this ePWM module 1: Enable CAPEVT as a one-shot trip source for this ePWM module
7 - 1	RESERVED	R-0		Reserved
0	CAPEVTCBC	R/W	0h	CAPEVT CBC mode Select 0: Disable CAPEVT as a CBC trip source for this ePWM module 1: Enable CAPEVT as a CBC trip source for this ePWM module

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3.9.50 CONTROLSS_Gm_EPWMn_TZDCSEL Registers

3.9.50.1 Gm_EPWMn_TZDCSEL Register (Offset = 104h) [reset = h]

Short Description: Trip Zone Digital Comparator Select Register

Long Description:

Return to Summary Table

Table 3-499. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-123. TZDCSEL Name Register

15	14	13	12	11	10	9	8
RESERVED				DCBEVT2			DCBEVT1
R-0				R/W			R/W
0				0			0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DCBEVT1		DCAEVT2			DCAEVT1		
R/W		R/W			R/W		
0		0			0		

Access Types Legend

Table 3-500. TZDCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R-0		Reserved
11 - 9	DCBEVT2	R/W	0h	Digital Compare Output B Event 2 Selection 000: Event disabled 001: DCBH = low, DCBL = don't care 010: DCBH = high, DCBL = don't care 011: DCBL = low, DCBH = don't care 100: DCBL = high, DCBH = don't care 101: DCBL = high, DCBH = low 110: Reserved 111: Reserved
8 - 6	DCBEVT1	R/W	0h	Digital Compare Output B Event 1 Selection 000: Event disabled 001: DCBH = low, DCBL = don't care 010: DCBH = high, DCBL = don't care 011: DCBL = low, DCBH = don't care 100: DCBL = high, DCBH = don't care 101: DCBL = high, DCBH = low 110: Reserved 111: Reserved
5 - 3	DCAEVT2	R/W	0h	Digital Compare Output A Event 2 Selection 000: Event disabled 001: DCAH = low, DCAL = don't care 010: DCAH = high, DCAL = don't care 011: DCAL = low, DCAH = don't care 100: DCAL = high, DCAH = don't care 101: DCAL = high, DCAH = low 110: Reserved 111: Reserved
2 - 0	DCAEVT1	R/W	0h	Digital Compare Output A Event 1 Selection 000: Event disabled 001: DCAH = low, DCAL = don't care 010: DCAH = high, DCAL = don't care 011: DCAL = low, DCAH = don't care 100: DCAL = high, DCAH = don't care 101: DCAL = high, DCAH = low 110: Reserved 111: Reserved

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3.9.51 CONTROLSS_Gm_EPWMn_TZCTL Registers

3.9.51.1 Gm_EPWMn_TZCTL Register (Offset = 108h) [reset = h]

Short Description: Trip Zone Control Register

Long Description:

Return to Summary Table

Table 3-501. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-124. TZCTL Name Register

15	14	13	12	11	10	9	8
RESERVED				DCBEVT2		DCBEVT1	
R-0				R/W		R/W	
0				0		0	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DCAEVT2		DCAEVT1		TZB		TZA	
R/W		R/W		R/W		R/W	
0		0		0		0	

Access Types Legend

Table 3-502. TZCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R-0		Reserved
11 - 10	DCBEVT2	R/W	0h	Digital Compare Output B Event 2 Action On EPWMxB 00: High-impedance (EPWMxB = High-impedance state) 01: Force EPWMxB to a high state. 10: Force EPWMxB to a low state. 11: Do Nothing, trip action is disabled
9 - 8	DCBEVT1	R/W	0h	Digital Compare Output B Event 1 Action On EPWMxB 00: High-impedance (EPWMxB = High-impedance state) 01: Force EPWMxB to a high state. 10: Force EPWMxB to a low state. 11: Do Nothing, trip action is disabled
7 - 6	DCAEVT2	R/W	0h	Digital Compare Output A Event 2 Action On EPWMxA 00: High-impedance (EPWMxA = High-impedance state) 01: Force EPWMxA to a high state. 10: Force EPWMxA to a low state. 11: Do Nothing, trip action is disabled
5 - 4	DCAEVT1	R/W	0h	Digital Compare Output A Event 1 Action On EPWMxA 00: High-impedance (EPWMxA = High-impedance state) 01: Force EPWMxA to a high state. 10: Force EPWMxA to a low state. 11: Do Nothing, trip action is disabled
3 - 2	TZB	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2Trip Action On EPWMxB When a trip event occurs the following action is taken on output EPWMxB. Which trip-zone pins can cause an event is defined in the TZSEL register. 00: High-impedance (EPWMxB = High-impedance state) 01: Force EPWMxB to a high state 10: Force EPWMxB to a low state 11: Do nothing, no action is taken on EPWMxB.
1 - 0	TZA	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxA When a trip event occurs the following action is taken on output EPWMxA. Which trip-zone pins can cause an event is defined in the TZSEL register. 00: High-impedance (EPWMxA = High-impedance state) 01: Force EPWMxA to a high state 10: Force EPWMxA to a low state 11: Do nothing, no action is taken on EPWMxA.

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3.9.52 CONTROLSS_Gm_EPWMn_TZCTL2 Registers

3.9.52.1 Gm_EPWMn_TZCTL2 Register (Offset = 10Ah) [reset = h]

Short Description: Additional Trip Zone Control Register

Long Description:

Return to Summary Table

Table 3-503. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-125. TZCTL2 Name Register

15	14	13	12	11	10	9	8
ETZE	RESERVED			TZBD			TZBU
R/W	R-0			R/W			R/W
0	0			0			0
7	6	5	4	3	2	1	0
TZBU		TZAD			TZAU		
R/W		R/W			R/W		
0		0			0		

Access Types Legend

Table 3-504. TZCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ETZE	R/W	0h	TZCTL2 Enable 0: Use trip action from TZCTL (legacy EPWM compatibility) 1: Use trip action defined in TZCTL2, TZCTLDCA and TZCTLDCB. Settings in TZCTL are ignored
14 - 12	RESERVED	R-0		Reserved
11 - 9	TZBD	R/W	0h	TZ1 to TZ6 Trip Action On EPWMxB while Count direction is DOWN 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -' High, High -' Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled
8 - 6	TZBU	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxB while Count direction is UP 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -' High, High -' Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled
5 - 3	TZAD	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxA while Count direction is DOWN 000: HiZ (EPWMxA = HiZ state) 001: Forced Hi (EPWMxA = High state) 010: Forced Lo (EPWMxA = Lo state) 011: Toggle (Low -' High, High -' Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled
2 - 0	TZAU	R/W	0h	TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxA while Count direction is UP 000: HiZ (EPWMxA = HiZ state) 001: Forced Hi (EPWMxA = High state) 010: Forced Lo (EPWMxA = Lo state) 011: Toggle (Low -' High, High -' Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled

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3.9.53 CONTROLSS_Gm_EPWMn_TZCTLDCA Registers

3.9.53.1 Gm_EPWMn_TZCTLDCA Register (Offset = 10Ch) [reset = h]

Short Description: Trip Zone Control Register Digital Compare A

Long Description:

Return to Summary Table

Table 3-505. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-126. TZCTLDCA Name Register

15	14	13	12	11	10	9	8
RESERVED				DCAEVT2D			DCAEVT2U
R-0				R/W			R/W
0				0			0
7	6	5	4	3	2	1	0
DCAEVT2U		DCAEVT1D			DCAEVT1U		
R/W		R/W			R/W		
0		0			0		

Access Types Legend

Table 3-506. TZCTLDCA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R-0		Reserved
11 - 9	DCAEVT2D	R/W	0h	Digital Compare Output A Event 2 Action On EPWMxA while Count direction is DOWN 000: HiZ (EPWMxA = HiZ state) 001: Forced Hi (EPWMxA = High state) 010: Forced Lo (EPWMxA = Lo state) 011: Toggle (Low -' High, High -' Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled
8 - 6	DCAEVT2U	R/W	0h	Digital Compare Output A Event 2 Action On EPWMxA while Count direction is UP 000: HiZ (EPWMxA = HiZ state) 001: Forced Hi (EPWMxA = High state) 010: Forced Lo (EPWMxA = Lo state) 011: Toggle (Low -' High, High -' Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled
5 - 3	DCAEVT1D	R/W	0h	Digital Compare Output A Event 1 Action On EPWMxA while Count direction is DOWN 000: HiZ (EPWMxA = HiZ state) 001: Forced Hi (EPWMxA = High state) 010: Forced Lo (EPWMxA = Lo state) 011: Toggle (Low -' High, High -' Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled
2 - 0	DCAEVT1U	R/W	0h	Digital Compare Output A Event 1 Action On EPWMxA while Count direction is UP 000: HiZ (EPWMxA = HiZ state) 001: Forced Hi (EPWMxA = High state) 010: Forced Lo (EPWMxA = Lo state) 011: Toggle (Low -' High, High -' Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled

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3.9.54 CONTROLSS_Gm_EPWMn_TZCTLDCB Registers

3.9.54.1 Gm_EPWMn_TZCTLDCB Register (Offset = 10Eh) [reset = h]

Short Description: Trip Zone Control Register Digital Compare B

Long Description:

Return to Summary Table

Table 3-507. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-127. TZCTLDCB Name Register

15	14	13	12	11	10	9	8
RESERVED				DCBEVT2D			DCBEVT2U
R-0				R/W			R/W
0				0			0
7	6	5	4	3	2	1	0
DCBEVT2U		DCBEVT1D			DCBEVT1U		
R/W		R/W			R/W		
0		0			0		

Access Types Legend

Table 3-508. TZCTLDCB Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R-0		Reserved
11 - 9	DCBEVT2D	R/W	0h	Digital Compare Output B Event 2 Action On EPWMxB while Count direction is DOWN 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -' High, High -' Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled
8 - 6	DCBEVT2U	R/W	0h	Digital Compare Output B Event 2 Action On EPWMxB while Count direction is UP 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -' High, High -' Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled
5 - 3	DCBEVT1D	R/W	0h	Digital Compare Output B Event 1 Action On EPWMxB while Count direction is DOWN 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -' High, High -' Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled
2 - 0	DCBEVT1U	R/W	0h	Digital Compare Output B Event 1 Action On EPWMxB while Count direction is UP 000: HiZ (EPWMxB = HiZ state) 001: Forced Hi (EPWMxB = High state) 010: Forced Lo (EPWMxB = Lo state) 011: Toggle (Low -' High, High -' Low) 100: Reserved 101: Reserved 110: Reserved 111: Do Nothing, trip action is disabled

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3.9.55 CONTROLSS_Gm_EPWMn_TZEINT Registers

3.9.55.1 Gm_EPWMn_TZEINT Register (Offset = 11Ah) [reset = h]

Short Description: Trip Zone Enable Interrupt Register

Long Description:

Return to Summary Table

Table 3-509. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-128. TZEINT Name Register

15	14	13	12	11	10	9	8
RESERVED							
R-0							
0							
7	6	5	4	3	2	1	0
CAPEVT	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1	OST	CBC	RESERVED
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R-0
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-510. TZEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R-0		Reserved
7	CAPEVT	R/W	0h	Capture Event Interrupt Enable 0: Disabled 1: Enabled
6	DCBEVT2	R/W	0h	Digital Compare Output B Event 2 Interrupt Enable 0: Disabled 1: Enabled
5	DCBEVT1	R/W	0h	Digital Compare Output B Event 1 Interrupt Enable 0: Disabled 1: Enabled
4	DCAEVT2	R/W	0h	Digital Compare Output A Event 2 Interrupt Enable 0: Disabled 1: Enabled
3	DCAEVT1	R/W	0h	Digital Compare Output A Event 1 Interrupt Enable 0: Disabled 1: Enabled
2	OST	R/W	0h	Trip-zone One-Shot Interrupt Enable 0: Disable one-shot interrupt generation 1: Enable Interrupt generation a one-shot trip event will cause a EPWMx_TZINT PIE interrupt.
1	CBC	R/W	0h	Trip-zone Cycle-by-Cycle Interrupt Enable 0: Disable cycle-by-cycle interrupt generation. 1: Enable interrupt generation a cycle-by-cycle trip event will cause an EPWMx_TZINT PIE interrupt.
0	RESERVED	R-0		Reserved

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3.9.56 CONTROLSS_Gm_EPWMn_TZFLG Registers

3.9.56.1 Gm_EPWMn_TZFLG Register (Offset = 126h) [reset = h]

Short Description: Trip Zone Flag Register

Long Description:

Return to Summary Table

Table 3-511. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-129. TZFLG Name Register

15	14	13	12	11	10	9	8
RESERVED							
R-0							
0							
7	6	5	4	3	2	1	0
CAPEVT	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1	OST	CBC	INT
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-512. TZFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R-0		Reserved
7	CAPEVT	R	0h	Latched Status Flag for Capture Event 0: Indicates no trip event has occurred on CAPEVT 1: Indicates a trip event has occurred for the event defined for CAPEVT
6	DCBEVT2	R	0h	Latched Status Flag for Digital Compare Output B Event 2 0: Indicates no trip event has occurred on DCBEVT2 1: Indicates a trip event has occurred for the event defined for DCBEVT2
5	DCBEVT1	R	0h	Latched Status Flag for Digital Compare Output B Event 1 0: Indicates no trip event has occurred on DCBEVT1 1: Indicates a trip event has occurred for the event defined for DCBEVT1
4	DCAEVT2	R	0h	Latched Status Flag for Digital Compare Output A Event 2 0: Indicates no trip event has occurred on DCAEVT2 1: Indicates a trip event has occurred for the event defined for DCAEVT2
3	DCAEVT1	R	0h	Latched Status Flag for Digital Compare Output A Event 1 0: Indicates no trip event has occurred on DCAEVT1 1: Indicates a trip event has occurred for the event defined for DCAEVT1
2	OST	R	0h	Latched Status Flag for A One-Shot Trip Event 0: No one-shot trip event has occurred. 1: Indicates a trip event has occurred on a pin selected as a one-shot trip source. This bit is cleared by writing the appropriate value to the TZCLR register.
1	CBC	R	0h	Latched Status Flag for Cycle-By-Cycle Trip Event 0: No cycle-by-cycle trip event has occurred. 1: Indicates a trip event has occurred on a signal selected as a cycle-by-cycle trip source. The TZFLG[CBC] bit will remain set until it is manually cleared by the user. If the cycle-by-cycle trip event is still present when the CBC bit is cleared, then CBC will be immediately set again. The specified condition on the signal is automatically cleared when the ePWM time-base counter reaches zero (TBCTR = 0x00) if the trip condition is no longer present. The condition on the signal is only cleared when the TBCTR = 0x00 no matter where in the cycle the CBC flag is cleared. This bit is cleared by writing the appropriate value to the TZCLR register.

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Table 3-512. TZFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT	R	0h	Latched Trip Interrupt Status Flag 0: Indicates no interrupt has been generated. 1: Indicates an EPWMx_TZINT PIE interrupt was generated because of a trip condition. No further EPWMx_TZINT PIE interrupts will be generated until this flag is cleared. If the interrupt flag is cleared when either CBC or OST is set, then another interrupt pulse will be generated. Clearing all flag bits will prevent further interrupts. This bit is cleared by writing the appropriate value to the TZCLR register.

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3.9.57 CONTROLSS_Gm_EPWMn_TZCBCFLG Registers

3.9.57.1 Gm_EPWMn_TZCBCFLG Register (Offset = 128h) [reset = h]

Short Description: Trip Zone CBC Flag Register

Long Description:

Return to Summary Table

Table 3-513. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-130. TZCBCFLG Name Register

15	14	13	12	11	10	9	8
RESERVED							CAPEVT
R-0							R
0							0
7	6	5	4	3	2	1	0
DCBEVT2	DCAEVT2	CBC6	CBC5	CBC4	CBC3	CBC2	CBC1
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-514. TZCBCFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9	RESERVED	R-0		Reserved
8	CAPEVT	R	0h	Latched Status Flag for Capture Event 0: Indicates no trip event has occurred on CAPEVT 1: Indicates a trip event has occurred for the event defined for CAPEVT
7	DCBEVT2	R	0h	Latched Status Flag for Digital Compare B Output Event 2 Trip Latch 0: Reading a 0 indicates that no trip has occurred on DCBEVT2. 1: Reading a 1 indicates a trip has occured on the DCBEVT2 selected event.
6	DCAEVT2	R	0h	Latched Status Flag for Digital Compare A Output Event 2 Trip Latch 0: Reading a 0 indicates that no trip has occurred on DCAEVT2. 1: Reading a 1 indicates a trip has occured on the DCAEVT2 selected event.
5	CBC6	R	0h	Latched Status Flag for CBC6 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC6. 1: Reading a 1 indicates a trip has occured on the CBC6 selected event.
4	CBC5	R	0h	Latched Status Flag for CBC5 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC5. 1: Reading a 1 indicates a trip has occured on the CBC5 selected event.
3	CBC4	R	0h	Latched Status Flag for CBC4 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC4. 1: Reading a 1 indicates a trip has occured on the CBC4 selected event.
2	CBC3	R	0h	Latched Status Flag for CBC3 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC3. 1: Reading a 1 indicates a trip has occured on the CBC3 selected event.
1	CBC2	R	0h	Latched Status Flag for CBC2 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC2. 1: Reading a 1 indicates a trip has occured on the CBC2 selected event.
0	CBC1	R	0h	Latched Status Flag for CBC1 Trip Latch 0: Reading a 0 indicates that no trip has occurred on CBC1. 1: Reading a 1 indicates a trip has occured on the CBC1 selected event.

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3.9.58 CONTROLSS_Gm_EPWMn_TZOSTFLG Registers

3.9.58.1 Gm_EPWMn_TZOSTFLG Register (Offset = 12Ah) [reset = h]

Short Description: Trip Zone OST Flag Register

Long Description:

Return to Summary Table

Table 3-515. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-131. TZOSTFLG Name Register

15	14	13	12	11	10	9	8
RESERVED							CAPEVT
R-0							R
0							0
7	6	5	4	3	2	1	0
DCBEVT1	DCAEVT1	OST6	OST5	OST4	OST3	OST2	OST1
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-516. TZOSTFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9	RESERVED	R-0		Reserved
8	CAPEVT	R	0h	Latched Status Flag for Capture Event 0: Indicates no trip event has occurred on CAPEVT 1: Indicates a trip event has occurred for the event defined for CAPEVT
7	DCBEVT1	R	0h	Latched Status Flag for Digital Compare B Output Event 1 Trip Latch 0: Reading a 0 indicates that no trip has occurred on DCBEVT1. 1: Reading a 1 indicates a trip has occured on the DCBEVT1 selected event.
6	DCAEVT1	R	0h	Latched Status Flag for Digital Compare A Output Event 1 Trip Latch 0: Reading a 0 indicates that no trip has occurred on DCAEVT1. 1: Reading a 1 indicates a trip has occured on the DCAEVT1 selected event.
5	OST6	R	0h	Latched Status Flag for OST6 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST6. 1: Reading a 1 indicates a trip has occured on the OST6 selected event.
4	OST5	R	0h	Latched Status Flag for OST5 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST5. 1: Reading a 1 indicates a trip has occured on the OST5 selected event.
3	OST4	R	0h	Latched Status Flag for OST4 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST4. 1: Reading a 1 indicates a trip has occured on the OST4 selected event.
2	OST3	R	0h	Latched Status Flag for OST3 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST3. 1: Reading a 1 indicates a trip has occured on the OST3 selected event.
1	OST2	R	0h	Latched Status Flag for OST2 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST2. 1: Reading a 1 indicates a trip has occured on the OST2 selected event.
0	OST1	R	0h	Latched Status Flag for OST1 Trip Latch 0: Reading a 0 indicates that no trip has occurred on OST1. 1: Reading a 1 indicates a trip has occured on the OST1 selected event.

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3.9.59 CONTROLSS_Gm_EPWMn_TZCLR Registers

3.9.59.1 Gm_EPWMn_TZCLR Register (Offset = 12Eh) [reset = h]

Short Description: Trip Zone Clear Register

Long Description:

Return to Summary Table

Table 3-517. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-132. TZCLR Name Register

15	14	13	12	11	10	9	8
CBCPULSE		RESERVED					
R/W		R-0					
0		0					
7	6	5	4	3	2	1	0
CAPEVT	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1	OST	CBC	INT
R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-518. TZCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	CBCPULSE	R/W	0h	Clear Pulse for Cycle-By-Cycle (CBC) Trip Latch This bit field determines which pulse clears the CBC trip latch. 00: CTR = zero pulse clears CBC trip latch. (Same as legacy designs.) 01: CTR = PRD pulse clears CBC trip latch. 10: CTR = zero or CTR = PRD pulse clears CBC trip latch. 11: CBC trip latch is not cleared
13 - 8	RESERVED	R-0		Reserved
7	CAPEVT	R-0/W	0h	Clear Flag for Capture Event 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 clears the CAPEVT event trip condition.
6	DCBEVT2	R-0/W	0h	Clear Flag for Digital Compare Output B Event 2 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 clears the DCBEVT2 event trip condition.
5	DCBEVT1	R-0/W	0h	Clear Flag for Digital Compare Output B Event 1 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 clears the DCBEVT1 event trip condition.
4	DCAEVT2	R-0/W	0h	Clear Flag for Digital Compare Output A Event 2 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 clears the DCAEVT2 event trip condition.
3	DCAEVT1	R-0/W	0h	Clear Flag for Digital Compare Output A Event 1 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 clears the DCAEVT1 event trip condition.
2	OST	R-0/W	0h	Clear Flag for One-Shot Trip (OST) Latch 0: Has no effect. Always reads back a 0. 1: Clears this Trip (set) condition.
1	CBC	R-0/W	0h	Clear Flag for Cycle-By-Cycle (CBC) Trip Latch 0: Has no effect. Always reads back a 0. 1: Clears this Trip (set) condition.

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Table 3-518. TZCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT	R-0/W	0h	Global Interrupt Clear Flag 0: Has no effect. Always reads back a 0. 1: Clears the trip-interrupt flag for this ePWM module (TZFLG[INT]). NOTE: No further EPWMx_TZINT PIE interrupts will be generated until the flag is cleared. If the TZFLG[INT] bit is cleared and any of the other flag bits are set, then another interrupt pulse will be generated. Clearing all flag bits will prevent further interrupts.

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3.9.60 CONTROLSS_Gm_EPWMn_TZCBCCLR Registers

3.9.60.1 Gm_EPWMn_TZCBCCLR Register (Offset = 130h) [reset = h]

Short Description: Trip Zone CBC Clear Register

Long Description:

Return to Summary Table

Table 3-519. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-133. TZCBCCLR Name Register

15	14	13	12	11	10	9	8
RESERVED							CAPEVT
R-0							R-0/W
0							0
7	6	5	4	3	2	1	0
DCBEVT2	DCAEVT2	CBC6	CBC5	CBC4	CBC3	CBC2	CBC1
R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-520. TZCBCCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9	RESERVED	R-0		Reserved
8	CAPEVT	R-0/W	0h	Clear Flag for CAPEVT selected for CBC 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CAPEVT] bit.
7	DCBEVT2	R-0/W	0h	Clear Flag for Digital Compare Output B Event 2 selected for CBC 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[DCBEVT2] bit.
6	DCAEVT2	R-0/W	0h	Clear Flag for Digital Compare Output A Event 2 selected for CBC 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[DCAEVT2] bit.
5	CBC6	R-0/W	0h	Clear Flag for Cycle-By-Cycle (CBC6) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC6] bit.
4	CBC5	R-0/W	0h	Clear Flag for Cycle-By-Cycle (CBC5) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC5] bit.
3	CBC4	R-0/W	0h	Clear Flag for Cycle-By-Cycle (CBC4) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC4] bit.
2	CBC3	R-0/W	0h	Clear Flag for Cycle-By-Cycle (CBC3) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC3] bit.
1	CBC2	R-0/W	0h	Clear Flag for Cycle-By-Cycle (CBC2) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC2] bit.
0	CBC1	R-0/W	0h	Clear Flag for Cycle-By-Cycle (CBC1) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZCBCFLG[CBC1] bit.

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3.9.61 CONTROLSS_Gm_EPWMn_TZOSTCLR Registers

3.9.61.1 Gm_EPWMn_TZOSTCLR Register (Offset = 132h) [reset = h]

Short Description: Trip Zone OST Clear Register

Long Description:

Return to Summary Table

Table 3-521. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-134. TZOSTCLR Name Register

15	14	13	12	11	10	9	8
RESERVED							CAPEVT
R-0							R-0/W
0							0
7	6	5	4	3	2	1	0
DCBEVT1	DCAEVT1	OST6	OST5	OST4	OST3	OST2	OST1
R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-522. TZOSTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9	RESERVED	R-0		Reserved
8	CAPEVT	R-0/W	0h	Clear Flag for CAPEVT selected for OST 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[CAPEVT] bit.
7	DCBEVT1	R-0/W	0h	Clear Flag for Digital Compare Output B Event 1 selected for OST 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[DCBEVT1] bit.
6	DCAEVT1	R-0/W	0h	Clear Flag for Digital Compare Output A Event 1 selected for OST 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[DCAEVT1] bit.
5	OST6	R-0/W	0h	Clear Flag for Oneshot (OST6) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST6] bit.
4	OST5	R-0/W	0h	Clear Flag for Oneshot (OST5) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST5] bit.
3	OST4	R-0/W	0h	Clear Flag for Oneshot (OST4) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST4] bit.
2	OST3	R-0/W	0h	Clear Flag for Oneshot (OST3) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST3] bit.
1	OST2	R-0/W	0h	Clear Flag for Oneshot (OST2) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST2] bit.
0	OST1	R-0/W	0h	Clear Flag for Oneshot (OST1) Trip Latch 0: Writing a 0 has no effect. 1: Writing a 1 will clear the TZOSTFLG[OST1] bit.

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3.9.62 CONTROLSS_Gm_EPWMn_TZFRC Registers

3.9.62.1 Gm_EPWMn_TZFRC Register (Offset = 136h) [reset = h]

Short Description: Trip Zone Force Register

Long Description:

Return to Summary Table

Table 3-523. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-135. TZFRC Name Register

15	14	13	12	11	10	9	8
RESERVED							
R-0							
0							
7	6	5	4	3	2	1	0
CAPEVT	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1	OST	CBC	RESERVED
R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0/W	R-0
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-524. TZFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R-0		Reserved
7	CAPEVT	R-0/W	0h	Force Flag for Capture Event Output 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 forces the CAPEVT event trip condition and sets the TZFLG[CAPEVT] bit.
6	DCBEVT2	R-0/W	0h	Force Flag for Digital Compare Output B Event 2 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 forces the DCBEVT2 event trip condition and sets the TZFLG[DCBEVT2] bit.
5	DCBEVT1	R-0/W	0h	Force Flag for Digital Compare Output B Event 1 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 forces the DCBEVT1 event trip condition and sets the TZFLG[DCBEVT1] bit.
4	DCAEVT2	R-0/W	0h	Force Flag for Digital Compare Output A Event 2 0: Writing 0 has no effect. This bit always reads back 0. 1: Writing 1 forces the DCAEVT2 event trip condition and sets the TZFLG[DCAEVT2] bit.
3	DCAEVT1	R-0/W	0h	Force Flag for Digital Compare Output A Event 1 0: Writing 0 has no effect. This bit always reads back 0 1: Writing 1 forces the DCAEVT1 event trip condition and sets the TZFLG[DCAEVT1] bit.
2	OST	R-0/W	0h	Force a One-Shot Trip Event via Software 0: Writing of 0 is ignored. Always reads back a 0. 1: Forces a one-shot trip event and sets the TZFLG[OST] bit.
1	CBC	R-0/W	0h	Force a Cycle-by-Cycle Trip Event via Software 0: Writing of 0 is ignored. Always reads back a 0. 1: Forces a cycle-by-cycle trip event and sets the TZFLG[CBC] bit.
0	RESERVED	R-0		Reserved

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3.9.63 CONTROLSS_Gm_EPWMn_TZTRIPOUTSEL Registers

3.9.63.1 Gm_EPWMn_TZTRIPOUTSEL Register (Offset = 13Ah) [reset = h]

Short Description: Trip Zone Force Register

Long Description:

Return to Summary Table

Table 3-525. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-136. TZTRIPOUTSEL Name Register

15	14	13	12	11	10	9	8
RESERVED			CAPEVT	DCBEVT2	DCBEVT1	DCAEVT2	DCAEVT1
R-0			R/W	R/W	R/W	R/W	R/W
0			0	0	0	0	0
7	6	5	4	3	2	1	0
TZ6	TZ5	TZ4	TZ3	TZ2	TZ1	CBC	OST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-526. TZTRIPOUTSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	R-0		Reserved
12	CAPEVT	R/W	0h	CAPEVT Select 0: Disable TZ6 as a TRIPOUT source for this ePWM module 1: Enable TZ6 as a TRIPOUT source for this ePWM module
11	DCBEVT2	R/W	0h	DCBEVT2 Select 0: Disable TZ6 as a TRIPOUT source for this ePWM module 1: Enable TZ6 as a TRIPOUT source for this ePWM module
10	DCBEVT1	R/W	0h	DCBEVT1 Select 0: Disable TZ6 as a TRIPOUT source for this ePWM module 1: Enable TZ6 as a TRIPOUT source for this ePWM module
9	DCAEVT2	R/W	0h	DCAEVT2 Select 0: Disable TZ6 as a TRIPOUT source for this ePWM module 1: Enable TZ6 as a TRIPOUT source for this ePWM module
8	DCAEVT1	R/W	0h	DCAEVT1 Select 0: Disable TZ6 as a TRIPOUT source for this ePWM module 1: Enable TZ6 as a TRIPOUT source for this ePWM module
7	TZ6	R/W	0h	Trip-zone 6 (TZ6) Select 0: Disable TZ6 as a TRIPOUT source for this ePWM module 1: Enable TZ6 as a TRIPOUT source for this ePWM module
6	TZ5	R/W	0h	Trip-zone 5 (TZ5) Select 0: Disable TZ5 as a TRIPOUT source for this ePWM module 1: Enable TZ5 as a TRIPOUT source for this ePWM module
5	TZ4	R/W	0h	Trip-zone 4 (TZ4) Select 0: Disable TZ4 as a TRIPOUT source for this ePWM module 1: Enable TZ4 as a TRIPOUT source for this ePWM module
4	TZ3	R/W	0h	Trip-zone 3 (TZ3) Select 0: Disable TZ3 as a TRIPOUT source for this ePWM module 1: Enable TZ3 as a TRIPOUT source for this ePWM module
3	TZ2	R/W	0h	Trip-zone 2 (TZ2) Select 0: Disable TZ2 as a TRIPOUT source for this ePWM module 1: Enable TZ2 as a TRIPOUT source for this ePWM module

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Table 3-526. TZTRIPOUTSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TZ1	R/W	0h	Trip-zone 1 (TZ1) Select 0: Disable TZ1 as a TRIPOUT source for this ePWM module 1: Enable TZ1 as a TRIPOUT source for this ePWM module
1	CBC	R/W	0h	CBC Select 0: Disable TZ1 as a TRIPOUT source for this ePWM module 1: Enable TZ1 as a TRIPOUT source for this ePWM module
0	OST	R/W	0h	OST Select 0: Disable TZ1 as a TRIPOUT source for this ePWM module 1: Enable TZ1 as a TRIPOUT source for this ePWM module

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3.9.64 CONTROLSS_Gm_EPWMn_ETSEL Registers

3.9.64.1 Gm_EPWMn_ETSEL Register (Offset = 148h) [reset = h]

Short Description: Event Trigger Selection Register

Long Description:

Return to Summary Table

Table 3-527. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-137. ETSEL Name Register

15	14	13	12	11	10	9	8
SOCBEN	SOCBSEL			SOCAEN	SOCASEL		
R/W	R/W			R/W	R/W		
0	0			0	0		
7	6	5	4	3	2	1	0
RESERVED	INTSELCMP	SOCBSELCMP	SOCASELCMP	INTEN	INTSEL		
R-0	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0		

Access Types Legend

Table 3-528. ETSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOCBEN	R/W	0h	Enable the ADC Start of Conversion B (EPWMxSOCB) Pulse 0: Disable EPWMxSOCB. 1: Enable EPWMxSOCB pulse.
14 - 12	SOCBSEL	R/W	0h	EPWMxSOCB Selection Options These bits determine when a EPWMxSOCB pulse will be generated. 000: Enable DCBEVT1.soc event 001: Enable event time-base counter equal to zero. (TBCTR = 0x00) 010: Enable event time-base counter equal to period (TBCTR = TBPRD) 011: Enable event time-base counter based on mixed events (ETSOCBMIX). ETSOCBMIX is configured in the ETSOCBMIXEN register. 100: Enable event time-base counter equal to CMPA when the timer is incrementing or CMPC when the timer is incrementing 101: Enable event time-base counter equal to CMPA when the timer is decrementing or CMPC when the timer is decrementing 110: Enable event: time-base counter equal to CMPB when the timer is incrementing or CMPD when the timer is incrementing 111: Enable event: time-base counter equal to CMPB when the timer is decrementing or CMPD when the timer is decrementing (*) Event selected is determined by SOCBSELCMP bit.
11	SOCAEN	R/W	0h	Enable the ADC Start of Conversion A (EPWMxSOCA) Pulse 0: Disable EPWMxSOCA. 1: Enable EPWMxSOCA pulse.

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Table 3-528. ETSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10 - 8	SOCASEL	R/W	0h	EPWMxSOCA Selection Options These bits determine when a EPWMxSOCA pulse will be generated. 000: Enable DCAEVT1.soc event 001: Enable event time-base counter equal to zero. (TBCTR = 0x00) 010: Enable event time-base counter equal to period (TBCTR = TBPRD) 011: Enable event time-base counter based on mixed events (ETSOCAMIX). ETSOCAMIX is configured in the ETSOCAMIXEN register. 100: Enable event time-base counter equal to CMPA when the timer is incrementing or CMPC when the timer is incrementing 101: Enable event time-base counter equal to CMPA when the timer is decrementing or CMPC when the timer is decrementing 110: Enable event: time-base counter equal to CMPB when the timer is incrementing or CMPD when the timer is incrementing 111: Enable event: time-base counter equal to CMPB when the timer is decrementing or CMPD when the timer is decrementing (*) Event selected is determined by SOCASELCMP bit.
7	RESERVED	R-0		Reserved
6	INTSELCMP	R/W	0h	EPWMxINT Compare Register Selection Options 0: Enable event time-base counter equal to CMPA when the timer is incrementing / Enable event time-base counter equal to CMPA when the timer is decrementing / Enable event: time-base counter equal to CMPB when the timer is incrementing / Enable event: time-base counter equal to CMPB when the timer is decrementing to INTSEL selection mux. 1: Enable event time-base counter equal to CMPC when the timer is incrementing / Enable event time-base counter equal to CMPC when the timer is decrementing / Enable event: time-base counter equal to CMPD when the timer is incrementing / Enable event: time-base counter equal to CMPD when the timer is decrementing to INTSEL selection mux.
5	SOCBSELCMP	R/W	0h	EPWMxSOCB Compare Register Selection Options 0: Enable event time-base counter equal to CMPA when the timer is incrementing / Enable event time-base counter equal to CMPA when the timer is decrementing / Enable event: time-base counter equal to CMPB when the timer is incrementing / Enable event: time-base counter equal to CMPB when the timer is decrementing to SOCBSEL selection mux. 1: Enable event time-base counter equal to CMPC when the timer is incrementing / Enable event time-base counter equal to CMPC when the timer is decrementing / Enable event: time-base counter equal to CMPD when the timer is incrementing / Enable event: time-base counter equal to CMPD when the timer is decrementing to SOCBSEL selection mux.
4	SOCASELCMP	R/W	0h	EPWMxSOCA Compare Register Selection Options 0: Enable event time-base counter equal to CMPA when the timer is incrementing / Enable event time-base counter equal to CMPA when the timer is decrementing / Enable event: time-base counter equal to CMPB when the timer is incrementing / Enable event: time-base counter equal to CMPB when the timer is decrementing to SOCASEL selection mux. 1: Enable event time-base counter equal to CMPC when the timer is incrementing / Enable event time-base counter equal to CMPC when the timer is decrementing / Enable event: time-base counter equal to CMPD when the timer is incrementing / Enable event: time-base counter equal to CMPD when the timer is decrementing to SOCASEL selection mux.
3	INTEN	R/W	0h	Enable ePWM Interrupt (EPWMx_INT) Generation 0: Disable EPWMx_INT generation 1: Enable EPWMx_INT generation

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Table 3-528. ETSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2 - 0	INTSEL	R/W	0h	ePWM Interrupt (EPWMx_INT) Selection Options 000: Reserved 001: Enable event time-base counter equal to zero. (TBCTR = 0x00) 010: Enable event time-base counter equal to period (TBCTR = TBPRD) 011: Enable event time-base counter based on mixed events (ETINTMIX). ETINTMIX is configured in the ETINTMIXEN register. 100: Enable event time-base counter equal to CMPA when the timer is incrementing or CMPC when the timer is incrementing 101: Enable event time-base counter equal to CMPA when the timer is decrementing or CMPC when the timer is decrementing 110: Enable event: time-base counter equal to CMPB when the timer is incrementing or CMPD when the timer is incrementing 111: Enable event: time-base counter equal to CMPB when the timer is decrementing or CMPD when the timer is decrementing (*) Event selected is determined by INTSELCMP bit.

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3.9.65 CONTROLSS_Gm_EPWMn_ETPS Registers

3.9.65.1 Gm_EPWMn_ETPS Register (Offset = 14Ch) [reset = h]

Short Description: Event Trigger Pre-Scale Register

Long Description:

Return to Summary Table

Table 3-529. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-138. ETPS Name Register

15	14	13	12	11	10	9	8
SOCBCNT		SOCBPRD		SOCACNT		SOCAPRD	
R		R/W		R		R/W	
0		0		0		0	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		SOCPSSEL	INTPSSEL	INTCNT		INTPRD	
R-0		R/W	R/W	R		R/W	
0		0	0	0		0	

Access Types Legend

Table 3-530. ETPS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	SOCBCNT	R	0h	ePWM ADC Start-of-Conversion B Event (EPWMxSOCB) Counter Register These bits indicate how many selected ETSEL[SOCBSEL] events have occurred: 00: No events have occurred. 01: 1 event has occurred. 10: 2 events have occurred. 11: 3 events have occurred.
13 - 12	SOCBPRD	R/W	0h	ePWM ADC Start-of-Conversion B Event (EPWMxSOCB) Period Select These bits determine how many selected ETSEL[SOCBSEL] events need to occur before an EPWMxSOCB pulse is generated. To be generated, the pulse must be enabled (ETSEL[SOCBEN] = 1). The SOCB pulse will be generated even if the status flag is set from a previous start of conversion (ETFLG[SOCB] = 1). Once the SOCB pulse is generated, the ETPS[SOCBCNT] bits will automatically be cleared. 00: Disable the SOCB event counter. No EPWMxSOCB pulse will be generated 01: Generate the EPWMxSOCB pulse on the first event: ETPS[SOCBCNT] = 0,1 10: Generate the EPWMxSOCB pulse on the second event: ETPS[SOCBCNT] = 1,0 11: Generate the EPWMxSOCB pulse on the third event: ETPS[SOCBCNT] = 1,1
11 - 10	SOCACNT	R	0h	ePWM ADC Start-of-Conversion A Event (EPWMxSOCA) Counter Register These bits indicate how many selected ETSEL[SOCASEL] events have occurred: 00: No events have occurred. 01: 1 event has occurred. 10: 2 events have occurred. 11: 3 events have occurred.
9 - 8	SOCAPRD	R/W	0h	ePWM ADC Start-of-Conversion A Event (EPWMxSOCA) Period Select These bits determine how many selected ETSEL[SOCASEL] events need to occur before an EPWMxSOCA pulse is generated. To be generated, the pulse must be enabled (ETSEL[SOCAEN] = 1). The SOCA pulse will be generated even if the status flag is set from a previous start of conversion (ETFLG[SOCA] = 1). Once the SOCA pulse is generated, the ETPS[SOCACNT] bits will automatically be cleared. 00: Disable the SOCA event counter. No EPWMxSOCA pulse will be generated 01: Generate the EPWMxSOCA pulse on the first event: ETPS[SOCACNT] = 0,1 10: Generate the EPWMxSOCA pulse on the second event: ETPS[SOCACNT] = 1,0 11: Generate the EPWMxSOCA pulse on the third event: ETPS[SOCACNT] = 1,1
7 - 6	RESERVED	R-0		Reserved

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Table 3-530. ETPS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SOCPSSEL	R/W	0h	EPWMxSOC A/B Pre-Scale Selection Bits 0: Selects ETPS [SOCACNT/SOCBCNT] and [SOCAPRD/SOCBPRD] registers to determine frequency of events (interrupt once every 0-3 events). 1: Selects ETSOCPS [SOCACNT2/SOCBCNT2] and [SOCAPRD2/ SOCBPRD2] registers to determine frequency of events (interrupt once every 0-15 events).
4	INTPSSEL	R/W	0h	EPWMxINTn Pre-Scale Selection Bits 0: Selects ETPS [INTCNT, and INTPRD] registers to determine frequency of events (interrupt once every 0-3 events). 1: Selects ETINTPS [INTCNT2, and INTPRD2] registers to determine frequency of events (interrupt once every 0-15 events).
3 - 2	INTCNT	R	0h	ePWM Interrupt Event (EPWMx_INT) Counter Register These bits indicate how many selected ETSEL[INTSEL] events have occurred. These bits are automatically cleared when an interrupt pulse is generated. If interrupts are disabled, ETSEL[INT] = 0 or the interrupt flag is set, ETFLG[INT] = 1, the counter will stop counting events when it reaches the period value ETPS[INTCNT] = ETPS[INTPRD]. 00: No events have occurred. 01: 1 event has occurred. 10: 2 events have occurred. 11: 3 events have occurred.
1 - 0	INTPRD	R/W	0h	ePWM Interrupt (EPWMx_INT) Period Select These bits determine how many selected ETSEL[INTSEL] events need to occur before an interrupt is generated. To be generated, the interrupt must be enabled (ETSEL[INT] = 1). If the interrupt status flag is set from a previous interrupt (ETFLG[INT] = 1) then no interrupt will be generated until the flag is cleared via the ETCLR[INT] bit. This allows for one interrupt to be pending while another is still being serviced. Once the interrupt is generated, the ETPS[INTCNT] bits will automatically be cleared. Writing a INTPRD value that is the same as the current counter value will trigger an interrupt if it is enabled and the status flag is clear. Writing a INTPRD value that is less than the current counter value will result in an undefined state. If a counter event occurs at the same instant as a new zero or non-zero INTPRD value is written, the counter is incremented. 00: Disable the interruptevent counter. No interrupt will be generated and ETFRC[INT] is ignored. 01: Generate an interrupt on the first event INTCNT = 01 (first event) 10: Generate interrupt on ETPS[INTCNT] = 1,0 (second event) 11: Generate interrupt on ETPS[INTCNT] = 1,1 (third event)

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3.9.66 CONTROLSS_Gm_EPWMn_ETFLG Registers

3.9.66.1 Gm_EPWMn_ETFLG Register (Offset = 150h) [reset = h]

Short Description: Event Trigger Flag Register

Long Description:

Return to Summary Table

Table 3-531. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-139. ETFLG Name Register

15	14	13	12	11	10	9	8
RESERVED							
R-0							
0							
7	6	5	4	3	2	1	0
RESERVED				SOCB	SOCA	RESERVED	INT
R-0				R	R	R-0	R
0				0	0	0	0

Access Types Legend

Table 3-532. ETFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	R-0		Reserved
3	SOCB	R	0h	Latched ePWM ADC Start-of-Conversion A (EPWMxSOCB) Status Flag Unlike the ETFLG[INT] flag, the EPWMxSOCB output will continue to pulse even if the flag bit is set. 0: Indicates no event occurred 1: Indicates that a start of conversion pulse was generated on EPWMxSOCB. The EPWMxSOCB output will continue to be generated even if the flag bit is set.
2	SOCA	R	0h	Latched ePWM ADC Start-of-Conversion A (EPWMxSOCA) Status Flag Unlike the ETFLG[INT] flag, the EPWMxSOCA output will continue to pulse even if the flag bit is set. 0: Indicates no event occurred 1: Indicates that a start of conversion pulse was generated on EPWMxSOCA. The EPWMxSOCA output will continue to be generated even if the flag bit is set.
1	RESERVED	R-0		Reserved
0	INT	R	0h	Latched ePWM Interrupt (EPWMx_INT) Status Flag 0: Indicates no event occurred 1: Indicates that an ePWMx interrupt (EPWMx_INT) was generated. No further interrupts will be generated until the flag bit is cleared. Up to one interrupt can be pending while the ETFLG[INT] bit is still set. If an interrupt is pending, it will not be generated until after the ETFLG[INT] bit is cleared.

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3.9.67 CONTROLSS_Gm_EPWMn_ETCLR Registers

3.9.67.1 Gm_EPWMn_ETCLR Register (Offset = 154h) [reset = h]

Short Description: Event Trigger Clear Register

Long Description:

Return to Summary Table

Table 3-533. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-140. ETCLR Name Register

15	14	13	12	11	10	9	8
RESERVED							
R-0							
0							
7	6	5	4	3	2	1	0
RESERVED				SOCB	SOCA	RESERVED	INT
R-0				R-0/W	R-0/W	R-0	R-0/W
0				0	0	0	0

Access Types Legend

Table 3-534. ETCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	R-0		Reserved
3	SOCB	R-0/W	0h	ePWM ADC Start-of-Conversion A (EPWMxSOCB) Flag Clear Bit 0: Writing a 0 has no effect. Always reads back a 0 1: Clears the ETFLG[SOCB] flag bit
2	SOCA	R-0/W	0h	ePWM ADC Start-of-Conversion A (EPWMxSOCA) Flag Clear Bit 0: Writing a 0 has no effect. Always reads back a 0 1: Clears the ETFLG[SOCA] flag bit
1	RESERVED	R-0		Reserved
0	INT	R-0/W	0h	ePWM Interrupt (EPWMx_INT) Flag Clear Bit 0: Writing a 0 has no effect. Always reads back a 0 1: Clears the ETFLG[INT] flag bit and enable further interrupts pulses to be generated

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3.9.68 CONTROLSS_Gm_EPWMn_ETFRC Registers

3.9.68.1 Gm_EPWMn_ETFRC Register (Offset = 158h) [reset = h]

Short Description: Event Trigger Force Register

Long Description:

Return to Summary Table

Table 3-535. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-141. ETFRC Name Register

15	14	13	12	11	10	9	8
RESERVED							
R-0							
0							
7	6	5	4	3	2	1	0
RESERVED				SOCB	SOCA	RESERVED	INT
R-0				R-0/W	R-0/W	R-0	R-0/W
0				0	0	0	0

Access Types Legend

Table 3-536. ETFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	R-0		Reserved
3	SOCB	R-0/W	0h	SOCB Force Bit The SOCB pulse will only be generated if the event is enabled in the ETSEL register. The ETFLG[SOCB] flag bit will be set regardless. 0: Writing 0 to this bit will be ignored. Always reads back a 0. 1: Generates a pulse on EPWMxSOCB and set the SOCBFLG bit. This bit is used for test purposes.
2	SOCA	R-0/W	0h	SOCA Force Bit The SOCA pulse will only be generated if the event is enabled in the ETSEL register. The ETFLG[SOCA] flag bit will be set regardless. 0: Writing 0 to this bit will be ignored. Always reads back a 0. 1: Generates a pulse on EPWMxSOCA and set the SOCAFLG bit. This bit is used for test purposes.
1	RESERVED	R-0		Reserved
0	INT	R-0/W	0h	INT Force Bit The interrupt will only be generated if the event is enabled in the ETSEL register. The INT flag bit will be set regardless. 0: Writing 0 to this bit will be ignored. Always reads back a 0. 1: Generates an interrupt on EPWMxINT and set the INT flag bit. This bit is used for test purposes.

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3.9.69 CONTROLSS_Gm_EPWMn_ETINTPS Registers

3.9.69.1 Gm_EPWMn_ETINTPS Register (Offset = 15Ch) [reset = h]

Short Description: Event-Trigger Interrupt Pre-Scale Register

Long Description:

Return to Summary Table

Table 3-537. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-142. ETINTPS Name Register

15	14	13	12	11	10	9	8
RESERVED							
R-0							
0							
7	6	5	4	3	2	1	0
INTCNT2				INTPRD2			
R				R/W			
0				0			

Access Types Legend

Table 3-538. ETINTPS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R-0		Reserved
7 - 4	INTCNT2	R	0h	EPWMxINT Counter 2 When ETPS[INTPSSEL]=1, these bits indicate how many selected events have occurred: 0000: No events 0001: 1 event 0010: 2 events 0011: 3 events 0100: 4 events ... 1111: 15 events
3 - 0	INTPRD2	R/W	0h	EPWMxINT Period 2 Select When ETPS[INTPSSEL] = 1, these bits select how many selected events need to occur before an interrupt is generated: 0000: Disable counter 0001: Generate interrupt on INTCNT = 1 (first event) 0010: Generate interrupt on INTCNT = 2 (second event) 0011: Generate interrupt on INTCNT = 3 (third event) 0100: Generate interrupt on INTCNT = 4 (fourth event) ... 1111: Generate interrupt on INTCNT = 15 (fifteenth event)

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3.9.70 CONTROLSS_Gm_EPWMn_ETSOCPS Registers

3.9.70.1 Gm_EPWMn_ETSOCPS Register (Offset = 160h) [reset = h]

Short Description: Event-Trigger SOC Pre-Scale Register

Long Description:

Return to Summary Table

Table 3-539. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-143. ETSOCPS Name Register

15	14	13	12	11	10	9	8
SOCBCNT2				SOCBPRD2			
R				R/W			
0				0			
7	6	5	4	3	2	1	0
SOCACNT2				SOCAPRD2			
R				R/W			
0				0			

Access Types Legend

Table 3-540. ETSOCPS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	SOCBCNT2	R	0h	EPWMxSOCB Counter 2 When ETPS[SOCPSSEL] = 1, these bits indicate how many selected events have occurred: 0000: No events 0001: 1 event 0010: 2 events 0011: 3 events 0100: 4 events ... 1111: 15 events
11 - 8	SOCBPRD2	R/W	0h	EPWMxSOCB Period 2 Select When ETPS[SOCPSSEL] = 1, these bits select how many selected event need to occur before an SOCB pulse is generated: 0000: Disable counter 0001: Generate interrupt on SOCBCNT2 = 1 (first event) 0010: Generate interrupt on SOCBCNT2 = 2 (second event) 0011: Generate interrupt on SOCBCNT2 = 3 (third event) 0100: Generate interrupt on SOCBCNT2 = 4 (fourth event) ... 1111: Generate interrupt on SOCBCNT2 = 15 (fifteenth event)
7 - 4	SOCACNT2	R	0h	EPWMxSOCA Counter 2 When ETPS[SOCPSSEL] = 1, these bits indicate how many selected events have occurred: 0000: No events 0001: 1 event 0010: 2 events 0011: 3 events 0100: 4 events ... 1111: 15 events
3 - 0	SOCAPRD2	R/W	0h	EPWMxSOCA Period 2 Select When ETPS[SOCPSSEL] = 1, these bits select how many selected event need to occur before an SOCA pulse is generated: 0000: Disable counter 0001: Generate interrupt on SOCACNT2 = 1 (first event) 0010: Generate interrupt on SOCACNT2 = 2 (second event) 0011: Generate interrupt on SOCACNT2 = 3 (third event) 0100: Generate interrupt on SOCACNT2 = 4 (fourth event) ... 1111: Generate interrupt on SOCACNT2 = 15 (fifteenth event)

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3.9.71 CONTROLSS_Gm_EPWMn_ETCNTINITCTL Registers

3.9.71.1 Gm_EPWMn_ETCNTINITCTL Register (Offset = 164h) [reset = h]

Short Description: Event-Trigger Counter Initialization Control Register

Long Description:

Return to Summary Table

Table 3-541. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-144. ETCNTINITCTL Name Register

15	14	13	12	11	10	9	8
SOCBINITEN	SOCAINITEN	INTINITEN	SOCBINITFRC	SOCAINITFRC	INTINITFRC	RESERVED	
R/W	R/W	R/W	R-0/W	R-0/W	R-0/W	R-0	
0	0	0	0	0	0	0	
7	6	5	4	3	2	1	0
RESERVED							
R-0							
0							

Access Types Legend

Table 3-542. ETCNTINITCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SOCBINITEN	R/W	0h	EPWMxSOCB Counter 2 Initialization Enable 0: Has no effect. 1: Enable initialization of EPWMxSOCB counter with contents of ETCNTINIT[SOCBINIT] on a SYNC event or software force.
14	SOCAINITEN	R/W	0h	EPWMxSOCA Counter 2 Initialization Enable 0: Has no effect. 1: Enable initialization of EPWMxSOCA counter with contents of ETCNTINIT[SOCAINIT] on a SYNC event or software force.
13	INTINITEN	R/W	0h	EPWMxINT Counter 2 Initialization Enable 0: Has no effect. 1: Enable initialization of EPWMxINT counter 2 with contents of ETCNTINIT[INTINIT] on a SYNC event or software force.
12	SOCBINITFRC	R-0/W	0h	EPWMxSOCB Counter 2 Initialization Force 0: Has no effect. 1: This bit forces the ET EPWMxSOCB counter to be initialized with the contents of ETCNTINIT[SOCBINIT].
11	SOCAINITFRC	R-0/W	0h	EPWMxSOCA Counter 2 Initialization Force 0: Has no effect. 1: This bit forces the ET EPWMxSOCA counter to be initialized with the contents of ETCNTINIT[SOCAINIT].
10	INTINITFRC	R-0/W	0h	EPWMxINT Counter 2 Initialization Force 0: Has no effect. 1: This bit forces the ET EPWMxINT counter to be initialized with the contents of ETCNTINIT[INTINIT].
9 - 0	RESERVED	R-0		Reserved

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3.9.72 CONTROLSS_Gm_EPWMn_ETCNTINIT Registers

3.9.72.1 Gm_EPWMn_ETCNTINIT Register (Offset = 168h) [reset = h]

Short Description: Event-Trigger Counter Initialization Register

Long Description:

Return to Summary Table

Table 3-543. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-145. ETCNTINIT Name Register

15	14	13	12	11	10	9	8
RESERVED				SOCBINIT			
R				R/W			
0				0			
7	6	5	4	3	2	1	0
SOCAINIT				INTINIT			
R/W				R/W			
0				0			

Access Types Legend

Table 3-544. ETCNTINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	R		Reserved
11 - 8	SOCBINIT	R/W	0h	EPWMxSOCB Counter 2 Initialization Bits The ET EPWMxSOCB counter is initialized with the contents of this register on an ePWM SYNC event or a software force.
7 - 4	SOCAINIT	R/W	0h	EPWMxSOCA Counter 2 Initialization Bits The ET EPWMxSOCA counter is initialized with the contents of this register on an ePWM SYNC event or a software force.
3 - 0	INTINIT	R/W	0h	EPWMxINT Counter 2 Initialization Bits The ET EPWMxINT counter is initialized with the contents of this register on an ePWM SYNC event or a software force.

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3.9.73 CONTROLSS_Gm_EPWMn_ETINTMIXEN Registers

3.9.73.1 Gm_EPWMn_ETINTMIXEN Register (Offset = 16Ch) [reset = h]

Short Description: Event-Trigger Mixed INT Selection

Long Description:

Return to Summary Table

Table 3-545. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-146. ETINTMIXEN Name Register

15	14	13	12	11	10	9	8
RESERVED					DCAEVT1	CDD	CDU
R-0					R/W	R/W	R/W
0					0	0	0
7	6	5	4	3	2	1	0
CCD	CCU	CBD	CBU	CAD	CAU	PRD	ZRO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	1

Access Types Legend

Table 3-546. ETINTMIXEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	R-0		Reserved
10	DCAEVT1	R/W	0h	Enable DCAEVT1.inter to the mixed ET interrupt trigger signal (ETINTMIX). 0: DCAEVT1.soc event is not enabled 1: Enable DCAEVT1.soc event
9	CDD	R/W	0h	Enable event time-base counter equal to CMPD when the timer is decrementing to the mixed ET interrupt trigger signal (ETINTMIX). 0: CMPD down-count match enable event is not enabled 1: Enable CMPD down-count match enable event
8	CDU	R/W	0h	Enable event time-base counter equal to CMPD when the timer is incrementing to the mixed ET interrupt trigger signal (ETINTMIX). 0: CMPD up-count match enable event is not enabled 1: Enable CMPD up-count match enable event
7	CCD	R/W	0h	Enable event time-base counter equal to CMPC when the timer is decrementing to the mixed ET interrupt trigger signal (ETINTMIX). 0: CMPC down-count match enable event is not enabled 1: Enable CMPC down-count match enable event
6	CCU	R/W	0h	Enable event time-base counter equal to CMPC when the timer is incrementing to the mixed ET interrupt trigger signal (ETINTMIX). 0: CMPC up-count match enable event is not enabled 1: Enable CMPC up-count match enable event
5	CBD	R/W	0h	Enable event time-base counter equal to CMPB when the timer is decrementing to the mixed ET interrupt trigger signal (ETINTMIX). 0: CMPB down-count match enable event is not enabled 1: Enable CMPB down-count match enable event
4	CBU	R/W	0h	Enable event time-base counter equal to CMPB when the timer is incrementing to the mixed ET interrupt trigger signal (ETINTMIX). 0: CMPB up-count match enable event is not enabled 1: Enable CMPB up-count match enable event
3	CAD	R/W	0h	Enable event time-base counter equal to CMPA when the timer is decrementing to the mixed ET interrupt trigger signal (ETINTMIX). 0: CMPA down-count match enable event is not enabled 1: Enable CMPA down-count match enable event

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Table 3-546. ETINTMIXEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CAU	R/W	0h	Enable event time-base counter equal to CMPA when the timer is incrementing to the mixed ET interrupt trigger signal (ETINTMIX). 0: CMPA up-count match enable event is not enabled 1: Enable CMPA up-count match enable event
1	PRD	R/W	1h	Enable event time-base counter equal to period (TBCTR = TBPRD) to the mixed ET interrupt trigger signal (ETINTMIX). 0: Period match event is not enabled 1: Enable period match event
0	ZRO	R/W	1h	Enable event time-base counter equal to zero (TBCTR = 0x00) to the mixed ET interrupt trigger signal (ETINTMIX). 0: Zero match event is not enabled 1: Enable zero match event

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3.9.74 CONTROLSS_Gm_EPWMn_ETSOCAMIXEN Registers

3.9.74.1 Gm_EPWMn_ETSOCAMIXEN Register (Offset = 170h) [reset = h]

Short Description: Event-Trigger Mixed SOCA Selection

Long Description:

Return to Summary Table

Table 3-547. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-147. ETSOCAMIXEN Name Register

15	14	13	12	11	10	9	8
RESERVED					DCAEVT1	CDD	CDU
R-0					R/W	R/W	R/W
0					0	0	0
7	6	5	4	3	2	1	0
CCD	CCU	CBD	CBU	CAD	CAU	PRD	ZRO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	1

Access Types Legend

Table 3-548. ETSOCAMIXEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	R-0		Reserved
10	DCAEVT1	R/W	0h	Enable DCAEVT1.inter to the mixed ET SOCA trigger signal (ETSOCAMIX). 0: DCAEVT1.soc event is not enabled 1: Enable DCAEVT1.soc event
9	CDD	R/W	0h	Enable event time-base counter equal to CMPD when the timer is decrementing to the mixed ET SOCA trigger signal (ETSOCAMIX). 0: CMPD down-count match enable event is not enabled 1: Enable CMPD down-count match enable event
8	CDU	R/W	0h	Enable event time-base counter equal to CMPD when the timer is incrementing to the mixed ET SOCA trigger signal (ETSOCAMIX). 0: CMPD up-count match enable event is not enabled 1: Enable CMPD up-count match enable event
7	CCD	R/W	0h	Enable event time-base counter equal to CMPC when the timer is decrementing to the mixed ET SOCA trigger signal (ETSOCAMIX). 0: CMPC down-count match enable event is not enabled 1: Enable CMPC down-count match enable event
6	CCU	R/W	0h	Enable event time-base counter equal to CMPC when the timer is incrementing to the mixed ET SOCA trigger signal (ETSOCAMIX). 0: CMPC up-count match enable event is not enabled 1: Enable CMPC up-count match enable event
5	CBD	R/W	0h	Enable event time-base counter equal to CMPB when the timer is decrementing to the mixed ET SOCA trigger signal (ETSOCAMIX). 0: CMPB down-count match enable event is not enabled 1: Enable CMPB down-count match enable event
4	CBU	R/W	0h	Enable event time-base counter equal to CMPB when the timer is incrementing to the mixed ET SOCA trigger signal (ETSOCAMIX). 0: CMPB up-count match enable event is not enabled 1: Enable CMPB up-count match enable event
3	CAD	R/W	0h	Enable event time-base counter equal to CMPA when the timer is decrementing to the mixed ET SOCA trigger signal (ETSOCAMIX). 0: CMPA down-count match enable event is not enabled 1: Enable CMPA down-count match enable event

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Table 3-548. ETSOCAMIXEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CAU	R/W	0h	Enable event time-base counter equal to CMPA when the timer is incrementing to the mixed ET SOCA trigger signal (ETSOCAMIX). 0: CMPA up-count match enable event is not enabled 1: Enable CMPA up-count match enable event
1	PRD	R/W	1h	Enable event time-base counter equal to period (TBCTR = TBPRD) to the mixed ET SOCA trigger signal (ETSOCAMIX). 0: Period match event is not enabled 1: Enable period match event
0	ZRO	R/W	1h	Enable event time-base counter equal to zero (TBCTR = 0x00) to the mixed ET SOCA trigger signal (ETSOCAMIX). 0: Zero match event is not enabled 1: Enable zero match event

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3.9.75 CONTROLSS_Gm_EPWMn_ETSOCBMIXEN Registers

3.9.75.1 Gm_EPWMn_ETSOCBMIXEN Register (Offset = 174h) [reset = h]

Short Description: Event-Trigger Mixed SOCB Selection

Long Description:

Return to Summary Table

Table 3-549. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-148. ETSOCBMIXEN Name Register

15	14	13	12	11	10	9	8
RESERVED					DCBEVT1	CDD	CDU
R-0					R/W	R/W	R/W
0					0	0	0
7	6	5	4	3	2	1	0
CCD	CCU	CBD	CBU	CAD	CAU	PRD	ZRO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	1

Access Types Legend

Table 3-550. ETSOCBMIXEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	R-0		Reserved
10	DCBEVT1	R/W	0h	Enable DCBEVT1.inter to the mixed ET SOCB trigger signal (ETSOCBMIX). 0: DCBEVT1.soc event is not enabled 1: Enable DCBEVT1.soc event
9	CDD	R/W	0h	Enable event time-base counter equal to CMPD when the timer is decrementing to the mixed ET SOCB trigger signal (ETSOCBMIX). 0: CMPD down-count match enable event is not enabled 1: Enable CMPD down-count match enable event
8	CDU	R/W	0h	Enable event time-base counter equal to CMPD when the timer is incrementing to the mixed ET SOCB trigger signal (ETSOCBMIX). 0: CMPD up-count match enable event is not enabled 1: Enable CMPD up-count match enable event
7	CCD	R/W	0h	Enable event time-base counter equal to CMPC when the timer is decrementing to the mixed ET SOCB trigger signal (ETSOCBMIX). 0: CMPC down-count match enable event is not enabled 1: Enable CMPC down-count match enable event
6	CCU	R/W	0h	Enable event time-base counter equal to CMPC when the timer is incrementing to the mixed ET SOCB trigger signal (ETSOCBMIX). 0: CMPC up-count match enable event is not enabled 1: Enable CMPC up-count match enable event
5	CBD	R/W	0h	Enable event time-base counter equal to CMPB when the timer is decrementing to the mixed ET SOCB trigger signal (ETSOCBMIX). 0: CMPB down-count match enable event is not enabled 1: Enable CMPB down-count match enable event
4	CBU	R/W	0h	Enable event time-base counter equal to CMPB when the timer is incrementing to the mixed ET SOCB trigger signal (ETSOCBMIX). 0: CMPB up-count match enable event is not enabled 1: Enable CMPB up-count match enable event
3	CAD	R/W	0h	Enable event time-base counter equal to CMPA when the timer is decrementing to the mixed ET SOCB trigger signal (ETSOCBMIX). 0: CMPA down-count match enable event is not enabled 1: Enable CMPA down-count match enable event

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Table 3-550. ETSOCBMIXEN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CAU	R/W	0h	Enable event time-base counter equal to CMPA when the timer is incrementing to the mixed ET SOCB trigger signal (ETSOCBMIX). 0: CMPA up-count match enable event is not enabled 1: Enable CMPA up-count match enable event
1	PRD	R/W	1h	Enable event time-base counter equal to period (TBCTR = TBPRD) to the mixed ET SOCB trigger signal (ETSOCBMIX). 0: Period match event is not enabled 1: Enable period match event
0	ZRO	R/W	1h	Enable event time-base counter equal to zero (TBCTR = 0x00) to the mixed ET SOCB trigger signal (ETSOCBMIX). 0: Zero match event is not enabled 1: Enable zero match event

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3.9.76 CONTROLSS_Gm_EPWMn_DCTRIPSEL Registers

3.9.76.1 Gm_EPWMn_DCTRIPSEL Register (Offset = 180h) [reset = h]

Short Description: Digital Compare Trip Select Register

Long Description:

Return to Summary Table

Table 3-551. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-149. DCTRIPSEL Name Register

15	14	13	12	11	10	9	8
DCBLCOMPSEL				DCBHCOMPSEL			
R/W				R/W			
0				0			
7	6	5	4	3	2	1	0
DCALCOMPSEL				DCAHCOMPSEL			
R/W				R/W			
0				0			

Access Types Legend

Table 3-552. DCTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	DCBLCOMPSEL	R/W	0h	Digital Compare B Low Input Select Bits 0000: TRIPIN1 0001: TRIPIN2 0010: TRIPIN3 0011: TRIPIN4 ... 1011: TRIPIN12 1100: Reserved 1101: TRIPIN14 1110: TRIPIN15 1111: Trip combination input (all trip inputs selected by DCBLTRIPSEL register ORed together)
11 - 8	DCBHCOMPSEL	R/W	0h	Digital Compare B High Input Select Bits 0000: TRIPIN1 0001: TRIPIN2 0010: TRIPIN3 0011: TRIPIN4 ... 1011: TRIPIN12 1100: Reserved 1101: TRIPIN14 1110: TRIPIN15 1111: Trip combination input (all trip inputs selected by DCBHTRIPSEL register ORed together)
7 - 4	DCALCOMPSEL	R/W	0h	Digital Compare A Low Input Select Bits 0000: TRIPIN1 0001: TRIPIN2 0010: TRIPIN3 0011: TRIPIN4 ... 1011: TRIPIN12 1100: Reserved 1101: TRIPIN14 1110: TRIPIN15 1111: Trip combination input (all trip inputs selected by DCALTRIPSEL register ORed together)
3 - 0	DCAHCOMPSEL	R/W	0h	Digital Compare A High Input Select Bits 0000: TRIPIN1 0001: TRIPIN2 0010: TRIPIN3 0011: TRIPIN4 ... 1011: TRIPIN12 1100: Reserved 1101: TRIPIN14 1110: TRIPIN15 1111: Trip combination input (all trip inputs selected by DCAHTRIPSEL register ORed together)

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3.9.77 CONTROLSS_Gm_EPWMn_DCACTL Registers

3.9.77.1 Gm_EPWMn_DCACTL Register (Offset = 186h) [reset = h]

Short Description: Digital Compare A Control Register

Long Description:

Return to Summary Table

Table 3-553. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-150. DCACTL Name Register

15	14	13	12	11	10	9	8
EVT2LAT	EVT2LATCLRSEL		EVT2LATSEL	RESERVED		EVT2FRCSYNCSEL	EVT2SRCSEL
R	R/W		R/W	R-0		R/W	R/W
0	0		0	0		0	0
7	6	5	4	3	2	1	0
EVT1LAT	EVT1LATCLRSEL		EVT1LATSEL	EVT1SYNCE	EVT1SOCE	EVT1FRCSYNCSEL	EVT1SRCSEL
R	R/W		R/W	R/W	R/W	R/W	R/W
0	0		0	0	0	0	0

Access Types Legend

Table 3-554. DCACTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	EVT2LAT	R	0h	Indicates the status of DCAEVT2LAT signal. 0 The DCAEVT2LAT latch is cleared. 1 The DCAEVT2LAT latch is set.
14 - 13	EVT2LATCLRSEL	R/W	0h	DCAEVT2 Latched clear source select: 00 CNT_ZERO event clears DCAEVT2 latch. 01 PRD_EQ event clears DCAEVT2 latch. 10 CNT_ZERO event or PRD_EQ event clears DCAEVT2 latch. 11 Reserved.
12	EVT2LATSEL	R/W	0h	DCAEVT2 Latched signal select: 0 Does not select the DCAEVT2 latched signal (Refer figure "Modifications to DCAEVT1.force/ DCAEVT2.force generation.") as source of DCAEVT2.force. 1 Selects the DCAEVT2 latched signal as source of DCAEVT2.force.
11 - 10	RESERVED	R-0		Reserved
9	EVT2FRCSYNCSEL	R/W	0h	DCAEVT2 Force Synchronization Signal Select 0: Source is synchronized with EPWMCLK 1: Source is passed through asynchronously
8	EVT2SRCSEL	R/W	0h	DCAEVT2 Source Signal Select 0: Source Is DCAEVT2 Signal 1: Source Is DCEVTFILT Signal
7	EVT1LAT	R	0h	Indicates the status of DCAEVT1LAT signal. 0 The DCAEVT1LAT latch is cleared. 1 The DCAEVT1LAT latch is set.
6 - 5	EVT1LATCLRSEL	R/W	0h	DCAEVT1 Latched clear source select: 00 CNT_ZERO event clears DCAEVT1 latch. 01 PRD_EQ event clears DCAEVT1 latch. 10 CNT_ZERO event or PRD_EQ event clears DCAEVT1 latch. 11 Reserved.
4	EVT1LATSEL	R/W	0h	DCAEVT1 Latched signal select: 0 Does not select the DCAEVT1 latched signal (Refer figure "Modifications to DCAEVT1.force/ DCAEVT2.force generation.") as source of DCAEVT1.force. 1 Selects the DCAEVT1 latched signal as source of DCAEVT1.force.
3	EVT1SYNCE	R/W	0h	DCAEVT1 SYNC, Enable/Disable 0: SYNC Generation Disabled 1: SYNC Generation Enabled

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Table 3-554. DCACTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EVT1SOCE	R/W	0h	DCAEVT1 SOC, Enable/Disable 0: SOC Generation Disabled 1: SOC Generation Enabled
1	EVT1FRCSYNCSEL	R/W	0h	DCAEVT1 Force Synchronization Signal Select 0: Source is synchronized with EPWMCLK 1: Source is passed through asynchronously
0	EVT1SRCSEL	R/W	0h	DCAEVT1 Source Signal Select 0: Source Is DCAEVT1 Signal 1: Source Is DCEVTFILT Signal

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3.9.78 CONTROLSS_Gm_EPWMn_DCBCTL Registers

3.9.78.1 Gm_EPWMn_DCBCTL Register (Offset = 188h) [reset = h]

Short Description: Digital Compare B Control Register

Long Description:

Return to Summary Table

Table 3-555. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-151. DCBCTL Name Register

15	14	13	12	11	10	9	8
EVT2LAT	EVT2LATCLRSEL		EVT2LATSEL	RESERVED		EVT2FRCSYNCSEL	EVT2SRCSEL
R	R/W		R/W	R-0		R/W	R/W
0	0		0	0		0	0
7	6	5	4	3	2	1	0
EVT1LAT	EVT1LATCLRSEL		EVT1LATSEL	EVT1SYNCE	EVT1SOCE	EVT1FRCSYNCSEL	EVT1SRCSEL
R	R/W		R/W	R/W	R/W	R/W	R/W
0	0		0	0	0	0	0

Access Types Legend

Table 3-556. DCBCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	EVT2LAT	R	0h	Indicates the status of DCBEVT2LAT signal. 0 The DCBEVT2LAT latch is cleared. 1 The DCBEVT2LAT latch is set.
14 - 13	EVT2LATCLRSEL	R/W	0h	DCBEVT2 Latched clear source select: 00 CNT_ZERO event clears DCBEVT2 latch. 01 PRD_EQ event clears DCBEVT2 latch. 10 CNT_ZERO event or PRD_EQ event clears DCBEVT2 latch. 11 Reserved.
12	EVT2LATSEL	R/W	0h	DCBEVT2 Latched signal select: 0 Does not select the DCBEVT2 latched signal (Refer figure "Modifications to DCBEVT1.force/ DCBEVT2.force generation.") as source of DCBEVT2.force. 1 Selects the DCBEVT2 latched signal as source of DCBEVT2.force.
11 - 10	RESERVED	R-0		Reserved
9	EVT2FRCSYNCSEL	R/W	0h	DCBEVT2 Force Synchronization Signal Select 0: Source is synchronized with EPWMCLK 1: Source is passed through asynchronously
8	EVT2SRCSEL	R/W	0h	DCBEVT2 Source Signal Select 0: Source Is DCBEVT2 Signal 1: Source Is DCEVTFILT Signal
7	EVT1LAT	R	0h	Indicates the status of DCBEVT1LAT signal. 0 The DCBEVT1LAT latch is cleared. 1 The DCBEVT1LAT latch is set.
6 - 5	EVT1LATCLRSEL	R/W	0h	DCBEVT1 Latched clear source select: 00 CNT_ZERO event clears DCBEVT1 latch. 01 PRD_EQ event clears DCBEVT1 latch. 10 CNT_ZERO event or PRD_EQ event clears DCBEVT1 latch. 11 Reserved.
4	EVT1LATSEL	R/W	0h	DCBEVT1 Latched signal select: 0 Does not select the DCBEVT1 latched signal (Refer figure "Modifications to DCBEVT1.force/ DCBEVT2.force generation.") as source of DCBEVT1.force. 1 Selects the DCBEVT1 latched signal as source of DCBEVT1.force.
3	EVT1SYNCE	R/W	0h	DCBEVT1 SYNC, Enable/Disable 0: SYNC Generation Disabled 1: SYNC Generation Enabled

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Table 3-556. DCBCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	EVT1SOCE	R/W	0h	DCBEVT1 SOC, Enable/Disable 0: SOC Generation Disabled 1: SOC Generation Enabled
1	EVT1FRCSYNCSEL	R/W	0h	DCBEVT1 Force Synchronization Signal Select 0: Source is synchronized with EPWMCLK 1: Source is passed through asynchronously
0	EVT1SRCSEL	R/W	0h	DCBEVT1 Source Signal Select 0: Source Is DCBEVT1 Signal 1: Source Is DCEVTFILT Signal

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3.9.79 CONTROLSS_Gm_EPWMn_DCFCTL Registers

3.9.79.1 Gm_EPWMn_DCFCTL Register (Offset = 18Eh) [reset = h]

Short Description: Digital Compare Filter Control Register

Long Description:

Return to Summary Table

Table 3-557. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-152. DCFCTL Name Register

15	14	13	12	11	10	9	8
EDGESTATUS			EDGECOUNT			EDGEMODE	
R			R/W			R/W	
0			0			0	
7	6	5	4	3	2	1	0
RESERVED	EDGEFILTSEL	PULSESEL		BLANKINV	BLANKE	SRCSEL	
R-0	R/W	R/W		R/W	R/W	R/W	
0	0	0		0	0	0	

Access Types Legend

Table 3-558. DCFCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	EDGESTATUS	R	0h	Edge Status: These bits reflect the total number of edges currently captured. When the value matches the EDGECOUNT, the status bits are set to zero. and a TBCLK wide pulse is generated which can then be output on the DCEVTFILT signal. The edge counter can be reset by writing 000 to the EDGECOUNT value:
12 - 10	EDGECOUNT	R/W	0h	Edge Count: These bits select how many edges to count before generating a TBCLK wide pulse on the DCEVTFILT signal: 000: no edges, reset current EDGESTATUS bits to 0,0,0 001: 1 edge 010: 2 edges 011: 3 edges 100: 4 edges 101: 5 edges 110: 6 edges 111: 7 edges
9 - 8	EDGEMODE	R/W	0h	Edge Mode Select: 00: Low To High Edge 01: High To Low Edge 10: Both Edges 11: Reserved
7	RESERVED	R-0		Reserved
6	EDGEFILTSEL	R/W	0h	Edge Filter Select: 0: Edge Filter Not Selected 1: Edge Filter Selected
5 - 4	PULSESEL	R/W	0h	Pulse Select For Blanking & Capture Alignment 00: Time-base counter equal to period (TBCTR = TBPRD) 01: Time-base counter equal to zero (TBCTR = 0x00) 10: Time-base counter equal to zero (TBCTR = 0x00) or period (TBCTR = TBPRD) 11: Blank Pulse Mix
3	BLANKINV	R/W	0h	Blanking Window Inversion 0: Blanking window not inverted 1: Blanking window inverted
2	BLANKE	R/W	0h	Blanking Window Enable/Disable 0: Blanking window is disabled 1: Blanking window is enabled
1 - 0	SRCSEL	R/W	0h	Filter Block Signal Source Select 00: Source Is DCAEVT1 Signal 01: Source Is DCAEVT2 Signal 10: Source Is DCBEVT1 Signal 11: Source Is DCBEVT2 Signal

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3.9.80 CONTROLSS_Gm_EPWMn_DCCAPCTL Registers

3.9.80.1 Gm_EPWMn_DCCAPCTL Register (Offset = 190h) [reset = h]

Short Description: Digital Compare Capture Control Register

Long Description:

Return to Summary Table

Table 3-559. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-153. DCCAPCTL Name Register

15	14	13	12	11	10	9	8
CAPMODE	CAPCLR	CAPSTS	RESERVED				
R/W	R-0/W	R	R-0				
0	0	0	0				
7	6	5	4	3	2	1	0
RESERVED						SHDWMODE	CAPE
R-0						R/W	R/W
0						0	0

Access Types Legend

Table 3-560. DCCAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CAPMODE	R/W	0h	Counter Capture Mode 0: When a DCEVTFILT occurs and the counter capture is enabled, then the current TBCNT value is captured in the active register. When the respective trip event occurs, further trip (capture) events are ignored until the next PRD_eq or CNT_zero event (as selected by the PULSESEL bit in the DCFCTL register) re-triggers the capture mechanism. If active mode is enabled, via SHDWMODE bit in DCCAPCTL register, CPU reads of this register will return the active register value. If shadow mode is enabled, via SHDWMODE bit in DCCAPCTL register, the active register is copied to the shadow register on the PRD_eq or CNT_zero event (whichever is selected by PULSESEL bit in DCFCTL register). CPU reads of this register will return the shadow register value. 1: When a DCEVTFILT occurs and the counter capture is enabled, then the current TBCNT value is captured in the active register. When the respective trip event occurs - itwill set the CAPSTS flag and further trip (capture) events are ignored until this bit is cleared. CAPSTS can be cleared by writing to CAPCLR bit in DCCAPCTL register and it re-triggers the capture mechanism. If active mode is enabled, via SHDWMODE bit in DCCAPCTL register, CPU reads of this register will return the active register value. If shadow mode is enabled, via SHDWMODE bit in DCCAPCTL register, the active register is copied to the shadow register on the PRD_eq or CNT_zero event (whichever is selected by PULSESEL bit in DCFCTL register). CPU reads of this register will return the shadow register value.
14	CAPCLR	R-0/W	0h	DC Capture Latched Status Clear Flag 0: Writing a 0 has no effect. 1: Writing a 1 will clear this CAPSTS (set) condition.
13	CAPSTS	R	0h	Latched Status Flag for Capture Event 0: No DC capture event occurred. 1: A DC capture event has occurred.
12 - 2	RESERVED	R-0		Reserved

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Table 3-560. DCCAPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SHDWMODE	R/W	0h	TBCTR Counter Capture Shadow Select Mode 0: Enable shadow mode. The DCCAP active register is copied to shadow register on a TBCTR = TBPRD or TBCTR = zero event as defined by the DCFCTL[PULSESEL] bit. CPU reads of the DCCAP register will return the shadow register contents. 1: Active Mode. In this mode the shadow register is disabled. CPU reads from the DCCAP register will always return the active register contents.
0	CAPE	R/W	0h	TBCTR Counter Capture Enable/Disable 0: Disable the time-base counter capture. 1: Enable the time-base counter capture.

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3.9.81 CONTROLSS_Gm_EPWMn_DCFOFFSET Registers

3.9.81.1 Gm_EPWMn_DCFOFFSET Register (Offset = 192h) [reset = h]

Short Description: Digital Compare Filter Offset Register

Long Description:

Return to Summary Table

Table 3-561. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-154. DCFOFFSET Name Register

15	14	13	12	11	10	9	8
DCFOFFSET							
R/W							
0							
7	6	5	4	3	2	1	0
DCFOFFSET							
R/W							
0							

Access Types Legend

Table 3-562. DCFOFFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	DCFOFFSET	R/W	0h	Blanking Window Offset These 16-bits specify the number of TBCLK cycles from the blanking window reference to the point when the blanking window is applied. The blanking window reference is either period or zero as defined by the DCFCTL[PULSESEL] bit. This offset register is shadowed and the active register is loaded at the reference point defined by DCFCTL[PULSESEL]. The offset counter is also initialized and begins to count down when the active register is loaded. When the counter expires, the blanking window is applied. If the blanking window is currently active, then the blanking window counter is restarted.

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3.9.82 CONTROLSS_Gm_EPWMn_DCFOFFSETCNT Registers

3.9.82.1 Gm_EPWMn_DCFOFFSETCNT Register (Offset = 194h) [reset = h]

Short Description: Digital Compare Filter Offset Counter Register

Long Description:

Return to Summary Table

Table 3-563. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-155. DCFOFFSETCNT Name Register

15	14	13	12	11	10	9	8
DCFOFFSETCNT							
R							
0							
7	6	5	4	3	2	1	0
DCFOFFSETCNT							
R							
0							

Access Types Legend

Table 3-564. DCFOFFSETCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	DCFOFFSETCNT	R	0h	Blanking Offset Counter These 16-bits are read only and indicate the current value of the offset counter. The counter counts down to zero and then stops until it is re-loaded on the next period or zero event as defined by the DCFCTL[PULSESEL] bit. The offset counter is not affected by the free/soft emulation bits. That is, it will always continue to count down if the device is halted by a emulation stop.

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3.9.83 CONTROLSS_Gm_EPWMn_DCFWINDOW Registers

3.9.83.1 Gm_EPWMn_DCFWINDOW Register (Offset = 196h) [reset = h]

Short Description: Digital Compare Filter Window Register

Long Description:

Return to Summary Table

Table 3-565. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-156. DCFWINDOW Name Register

15	14	13	12	11	10	9	8
DCFWINDOW							
R/W							
0							
7	6	5	4	3	2	1	0
DCFWINDOW							
R/W							
0							

Access Types Legend

Table 3-566. DCFWINDOW Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	DCFWINDOW	R/W	0h	Blanking Window Width 00h: No blanking window is generated. 01-FFFFh: Specifies the width of the blanking window in TBCLK cycles. The blanking window begins when the offset counter expires. When this occurs, the window counter is loaded and begins to count down. If the blanking window is currently active and the offset counter expires, the blanking window counter is not restarted and the blanking window is cut short prematurely. Care should be taken to avoid this situation. The blanking window can cross a PWM period boundary.

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3.9.84 CONTROLSS_Gm_EPWMn_DCFWINDOWCNT Registers

3.9.84.1 Gm_EPWMn_DCFWINDOWCNT Register (Offset = 198h) [reset = h]

Short Description: Digital Compare Filter Window Counter Register

Long Description:

Return to Summary Table

Table 3-567. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-157. DCFWINDOWCNT Name Register

15	14	13	12	11	10	9	8
DCFWINDOWCNT							
R							
0							
7	6	5	4	3	2	1	0
DCFWINDOWCNT							
R							
0							

Access Types Legend

Table 3-568. DCFWINDOWCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	DCFWINDOWCNT	R	0h	Blanking Window Counter These 16 bits are read only and indicate the current value of the window counter. The counter counts down to zero and then stops until it is re-loaded when the offset counter reaches zero again.

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3.9.85 CONTROLSS_Gm_EPWMn_BLANKPULSEMIXSEL Registers

3.9.85.1 Gm_EPWMn_BLANKPULSEMIXSEL Register (Offset = 19Ah) [reset = h]

Short Description: Blanking window trigger pulse select register

Long Description:

Return to Summary Table

Table 3-569. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-158. BLANKPULSEMIXSEL Name Register

15	14	13	12	11	10	9	8
RESERVED						CDD	CDU
R-0						R/W	R/W
0						0	0
7	6	5	4	3	2	1	0
CCD	CCU	CBD	CBU	CAD	CAU	PRD	ZRO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-570. BLANKPULSEMIXSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	R-0		Reserved
9	CDD	R/W	0h	Enable event time-base counter equal to CMPD when the timer is decrementing to the blanking window trigger (BLANKPULSEMIX). 0: CMPD down-count match enable event is not enabled 1: Enable CMPD down-count match enable event
8	CDU	R/W	0h	Enable event time-base counter equal to CMPD when the timer is incrementing to the blanking window trigger (BLANKPULSEMIX). 0: CMPD up-count match enable event is not enabled 1: Enable CMPD up-count match enable event
7	CCD	R/W	0h	Enable event time-base counter equal to CMPC when the timer is decrementing to the blanking window trigger (BLANKPULSEMIX). 0: CMPC down-count match enable event is not enabled 1: Enable CMPC down-count match enable event
6	CCU	R/W	0h	Enable event time-base counter equal to CMPC when the timer is incrementing to the blanking window trigger (BLANKPULSEMIX). 0: CMPC up-count match enable event is not enabled 1: Enable CMPC up-count match enable event
5	CBD	R/W	0h	Enable event time-base counter equal to CMPB when the timer is decrementing to the blanking window trigger (BLANKPULSEMIX). 0: CMPB down-count match enable event is not enabled 1: Enable CMPB down-count match enable event
4	CBU	R/W	0h	Enable event time-base counter equal to CMPB when the timer is incrementing to the mixed ET interrupt trigger signal (BLANKPULSEMIX). 0: CMPB up-count match enable event is not enabled 1: Enable CMPB up-count match enable event
3	CAD	R/W	0h	Enable event time-base counter equal to CMPA when the timer is decrementing to the blanking window trigger (BLANKPULSEMIX). 0: CMPA down-count match enable event is not enabled 1: Enable CMPA down-count match enable event

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Table 3-570. BLANKPULSEMIXSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CAU	R/W	0h	Enable event time-base counter equal to CMPA when the timer is incrementing to the blanking window trigger (BLANKPULSEMIX). 0: CMPA up-count match enable event is not enabled 1: Enable CMPA up-count match enable event
1	PRD	R/W	0h	Enable event time-base counter equal to period (TBCTR = TBPRD) to the blanking window trigger (BLANKPULSEMIX). 0: Period match event is not enabled 1: Enable period match event
0	ZRO	R/W	0h	Enable event time-base counter equal to zero (TBCTR = 0x00) to the blanking window trigger (BLANKPULSEMIX). 0: Zero match event is not enabled 1: Enable zero match event

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3.9.86 CONTROLSS_Gm_EPWMn_DCCAPMIXSEL Registers

3.9.86.1 Gm_EPWMn_DCCAPMIXSEL Register (Offset = 19Ch) [reset = h]

Short Description: Capture Event pulse select register

Long Description:

Return to Summary Table

Table 3-571. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-159. DCCAPMIXSEL Name Register

15	14	13	12	11	10	9	8
RESERVED						CDD	CDU
R-0						R/W	R/W
0						0	0
7	6	5	4	3	2	1	0
CCD	CCU	CBD	CBU	CAD	CAU	PRD	ZRO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-572. DCCAPMIXSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	R-0		Reserved
9	CDD	R/W	0h	Enable event time-base counter equal to CMPD when the timer is decrementing to the blanking window trigger (DCCAPMIX). 0: CMPD down-count match enable event is not enabled 1: Enable CMPD down-count match enable event
8	CDU	R/W	0h	Enable event time-base counter equal to CMPD when the timer is incrementing to the blanking window trigger (DCCAPMIX). 0: CMPD up-count match enable event is not enabled 1: Enable CMPD up-count match enable event
7	CCD	R/W	0h	Enable event time-base counter equal to CMPC when the timer is decrementing to the blanking window trigger (DCCAPMIX). 0: CMPC down-count match enable event is not enabled 1: Enable CMPC down-count match enable event
6	CCU	R/W	0h	Enable event time-base counter equal to CMPC when the timer is incrementing to the blanking window trigger (DCCAPMIX). 0: CMPC up-count match enable event is not enabled 1: Enable CMPC up-count match enable event
5	CBD	R/W	0h	Enable event time-base counter equal to CMPB when the timer is decrementing to the blanking window trigger (DCCAPMIX). 0: CMPB down-count match enable event is not enabled 1: Enable CMPB down-count match enable event
4	CBU	R/W	0h	Enable event time-base counter equal to CMPB when the timer is incrementing to the mixed ET interrupt trigger signal (DCCAPMIX). 0: CMPB up-count match enable event is not enabled 1: Enable CMPB up-count match enable event
3	CAD	R/W	0h	Enable event time-base counter equal to CMPA when the timer is decrementing to the blanking window trigger (DCCAPMIX). 0: CMPA down-count match enable event is not enabled 1: Enable CMPA down-count match enable event

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Table 3-572. DCCAPMIXSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CAU	R/W	0h	Enable event time-base counter equal to CMPA when the timer is incrementing to the blanking window trigger (DCCAPMIX). 0: CMPA up-count match enable event is not enabled 1: Enable CMPA up-count match enable event
1	PRD	R/W	0h	Enable event time-base counter equal to period (TBCTR = TBPRD) to the blanking window trigger (DCCAPMIX). 0: Period match event is not enabled 1: Enable period match event
0	ZRO	R/W	0h	Enable event time-base counter equal to zero (TBCTR = 0x00) to the blanking window trigger (DCCAPMIX). 0: Zero match event is not enabled 1: Enable zero match event

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3.9.87 CONTROLSS_Gm_EPWMn_DCCAP Registers

3.9.87.1 Gm_EPWMn_DCCAP Register (Offset = 19Eh) [reset = h]

Short Description: Digital Compare Counter Capture Register

Long Description:

Return to Summary Table

Table 3-573. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-160. DCCAP Name Register

15	14	13	12	11	10	9	8
DCCAP							
R							
0							
7	6	5	4	3	2	1	0
DCCAP							
R							
0							

Access Types Legend

Table 3-574. DCCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	DCCAP	R	0h	Digital Compare Time-Base Counter Capture To enable time-base counter capture, set the DCCAPCLT[CAPE] bit to 1. If enabled, reflects the value of the time-base counter (TBCTR) on the low to high edge transition of a filtered (DCEVTFLT) event. Further capture events are ignored until the next period or zero as selected by the DCFCTL[PULSESEL] bit. Shadowing of DCCAP is enabled and disabled by the DCCAPCTL[SHDWMODE] bit. By default this register is shadowed. - If DCCAPCTL[SHDWMODE] = 0, then the shadow is enabled. In this mode, the active register is copied to the shadow register on the TBCTR = TBPRD or TBCTR = zero as defined by the DCFCTL[PULSESEL] bit. CPU reads of this register will return the shadow register value. - If DCCAPCTL[SHDWMODE] = 1, then the shadow register is disabled. In this mode, CPU reads will return the active register value. The active and shadow registers share the same memory map address.

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3.9.88 CONTROLSS_Gm_EPWMn_DCAHTRIPSEL Registers

3.9.88.1 Gm_EPWMn_DCAHTRIPSEL Register (Offset = 1A4h) [reset = h]

Short Description: Digital Compare AH Trip Select

Long Description:

Return to Summary Table

Table 3-575. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-161. DCAHTRIPSEL Name Register

15	14	13	12	11	10	9	8
RESERVED	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-576. DCAHTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0: Trip Input 15 not selected as combinational ORed input 1: Trip Input 15 selected as combinational ORed input to DCAH mux
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0: Trip Input 14 not selected as combinational ORed input 1: Trip Input 14 selected as combinational ORed input to DCAH mux
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0: Trip Input 13 not selected as combinational ORed input 1: Trip Input 13 selected as combinational ORed input to DCAH mux
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0: Trip Input 12 not selected as combinational ORed input 1: Trip Input 12 selected as combinational ORed input to DCAH mux
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0: Trip Input 11 not selected as combinational ORed input 1: Trip Input 11 selected as combinational ORed input to DCAH mux
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0: Trip Input 10 not selected as combinational ORed input 1: Trip Input 10 selected as combinational ORed input to DCAH mux
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0: Trip Input 9 not selected as combinational ORed input 1: Trip Input 9 selected as combinational ORed input to DCAH mux
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0: Trip Input 8 not selected as combinational ORed input 1: Trip Input 8 selected as combinational ORed input to DCAH mux
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0: Trip Input 7 not selected as combinational ORed input 1: Trip Input 7 selected as combinational ORed input to DCAH mux
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0: Trip Input 6 not selected as combinational ORed input 1: Trip Input 6 selected as combinational ORed input to DCAH mux

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Table 3-576. DCAHTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0: Trip Input 5 not selected as combinational ORed input 1: Trip Input 5 selected as combinational ORed input to DCAH mux
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0: Trip Input 4 not selected as combinational ORed input 1: Trip Input 4 selected as combinational ORed input to DCAH mux
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0: Trip Input 3 not selected as combinational ORed input 1: Trip Input 3 selected as combinational ORed input to DCAH mux
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0: Trip Input 2 not selected as combinational ORed input 1: Trip Input 2 selected as combinational ORed input to DCAH mux
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0: Trip Input 1 not selected as combinational ORed input 1: Trip Input 1 selected as combinational ORed input to DCAH mux

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3.9.89 CONTROLSS_Gm_EPWMn_DCALTRIPSEL Registers

3.9.89.1 Gm_EPWMn_DCALTRIPSEL Register (Offset = 1A6h) [reset = h]

Short Description: Digital Compare AL Trip Select

Long Description:

Return to Summary Table

Table 3-577. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-162. DCALTRIPSEL Name Register

15	14	13	12	11	10	9	8
RESERVED	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-578. DCALTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0: Trip Input 15 not selected as combinational ORed input 1: Trip Input 15 selected as combinational ORed input to DCAL mux
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0: Trip Input 14 not selected as combinational ORed input 1: Trip Input 14 selected as combinational ORed input to DCAL mux
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0: Trip Input 13 not selected as combinational ORed input 1: Trip Input 13 selected as combinational ORed input to DCAL mux
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0: Trip Input 12 not selected as combinational ORed input 1: Trip Input 12 selected as combinational ORed input to DCAL mux
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0: Trip Input 11 not selected as combinational ORed input 1: Trip Input 11 selected as combinational ORed input to DCAL mux
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0: Trip Input 10 not selected as combinational ORed input 1: Trip Input 10 selected as combinational ORed input to DCAL mux
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0: Trip Input 9 not selected as combinational ORed input 1: Trip Input 9 selected as combinational ORed input to DCAL mux
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0: Trip Input 8 not selected as combinational ORed input 1: Trip Input 8 selected as combinational ORed input to DCAL mux
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0: Trip Input 7 not selected as combinational ORed input 1: Trip Input 7 selected as combinational ORed input to DCAL mux
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0: Trip Input 6 not selected as combinational ORed input 1: Trip Input 6 selected as combinational ORed input to DCAL mux

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Table 3-578. DCALTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0: Trip Input 5 not selected as combinational ORed input 1: Trip Input 5 selected as combinational ORed input to DCAL mux
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0: Trip Input 4 not selected as combinational ORed input 1: Trip Input 4 selected as combinational ORed input to DCAL mux
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0: Trip Input 3 not selected as combinational ORed input 1: Trip Input 3 selected as combinational ORed input to DCAL mux
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0: Trip Input 2 not selected as combinational ORed input 1: Trip Input 2 selected as combinational ORed input to DCAL mux
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0: Trip Input 1 not selected as combinational ORed input 1: Trip Input 1 selected as combinational ORed input to DCAL mux

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3.9.90 CONTROLSS_Gm_EPWMn_DCBHTRIPSEL Registers

3.9.90.1 Gm_EPWMn_DCBHTRIPSEL Register (Offset = 1A8h) [reset = h]

Short Description: Digital Compare BH Trip Select

Long Description:

Return to Summary Table

Table 3-579. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-163. DCBHTRIPSEL Name Register

15	14	13	12	11	10	9	8
RESERVED	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-580. DCBHTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0: Trip Input 15 not selected as combinational ORed input 1: Trip Input 15 selected as combinational ORed input to DCBH mux
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0: Trip Input 14 not selected as combinational ORed input 1: Trip Input 14 selected as combinational ORed input to DCBH mux
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0: Trip Input 13 not selected as combinational ORed input 1: Trip Input 13 selected as combinational ORed input to DCBH mux
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0: Trip Input 12 not selected as combinational ORed input 1: Trip Input 12 selected as combinational ORed input to DCBH mux
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0: Trip Input 11 not selected as combinational ORed input 1: Trip Input 11 selected as combinational ORed input to DCBH mux
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0: Trip Input 10 not selected as combinational ORed input 1: Trip Input 10 selected as combinational ORed input to DCBH mux
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0: Trip Input 9 not selected as combinational ORed input 1: Trip Input 9 selected as combinational ORed input to DCBH mux
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0: Trip Input 8 not selected as combinational ORed input 1: Trip Input 8 selected as combinational ORed input to DCBH mux
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0: Trip Input 7 not selected as combinational ORed input 1: Trip Input 7 selected as combinational ORed input to DCBH mux
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0: Trip Input 6 not selected as combinational ORed input 1: Trip Input 6 selected as combinational ORed input to DCBH mux

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Table 3-580. DCBHTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0: Trip Input 5 not selected as combinational ORed input 1: Trip Input 5 selected as combinational ORed input to DCBH mux
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0: Trip Input 4 not selected as combinational ORed input 1: Trip Input 4 selected as combinational ORed input to DCBH mux
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0: Trip Input 3 not selected as combinational ORed input 1: Trip Input 3 selected as combinational ORed input to DCBH mux
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0: Trip Input 2 not selected as combinational ORed input 1: Trip Input 2 selected as combinational ORed input to DCBH mux
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0: Trip Input 1 not selected as combinational ORed input 1: Trip Input 1 selected as combinational ORed input to DCBH mux

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3.9.91 CONTROLSS_Gm_EPWMn_DCBLTRIPSEL Registers

3.9.91.1 Gm_EPWMn_DCBLTRIPSEL Register (Offset = 1AAh) [reset = h]

Short Description: Digital Compare BL Trip Select

Long Description:

Return to Summary Table

Table 3-581. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-164. DCBLTRIPSEL Name Register

15	14	13	12	11	10	9	8
RESERVED	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-582. DCBLTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0: Trip Input 15 not selected as combinational ORed input 1: Trip Input 15 selected as combinational ORed input to DCAL mux
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0: Trip Input 14 not selected as combinational ORed input 1: Trip Input 14 selected as combinational ORed input to DCAL mux
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0: Trip Input 13 not selected as combinational ORed input 1: Trip Input 13 selected as combinational ORed input to DCAL mux
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0: Trip Input 12 not selected as combinational ORed input 1: Trip Input 12 selected as combinational ORed input to DCAL mux
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0: Trip Input 11 not selected as combinational ORed input 1: Trip Input 11 selected as combinational ORed input to DCAL mux
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0: Trip Input 10 not selected as combinational ORed input 1: Trip Input 10 selected as combinational ORed input to DCAL mux
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0: Trip Input 9 not selected as combinational ORed input 1: Trip Input 9 selected as combinational ORed input to DCAL mux
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0: Trip Input 8 not selected as combinational ORed input 1: Trip Input 8 selected as combinational ORed input to DCAL mux
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0: Trip Input 7 not selected as combinational ORed input 1: Trip Input 7 selected as combinational ORed input to DCAL mux
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0: Trip Input 6 not selected as combinational ORed input 1: Trip Input 6 selected as combinational ORed input to DCAL mux

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Table 3-582. DCBLTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0: Trip Input 5 not selected as combinational ORed input 1: Trip Input 5 selected as combinational ORed input to DCAL mux
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0: Trip Input 4 not selected as combinational ORed input 1: Trip Input 4 selected as combinational ORed input to DCAL mux
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0: Trip Input 3 not selected as combinational ORed input 1: Trip Input 3 selected as combinational ORed input to DCAL mux
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0: Trip Input 2 not selected as combinational ORed input 1: Trip Input 2 selected as combinational ORed input to DCAL mux
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0: Trip Input 1 not selected as combinational ORed input 1: Trip Input 1 selected as combinational ORed input to DCAL mux

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3.9.92 CONTROLSS_Gm_EPWMn_CAPCTL Registers

3.9.92.1 Gm_EPWMn_CAPCTL Register (Offset = 1ACh) [reset = h]

Short Description: Event Capture Control Register

Long Description:

Return to Summary Table

Table 3-583. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-165. CAPCTL Name Register

15	14	13	12	11	10	9	8
RESERVED							FRCLOAD
R							R-0/W
0							0
7	6	5	4	3	2	1	0
RESERVED			PULSECTL	CAPINPOL	CAPGATEPOL		SRCSEL
R			R/W	R/W	R/W		R/W
0			0	0	0		0

Access Types Legend

Table 3-584. CAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9	RESERVED	R		Reserved
8	FRCLOAD	R-0/W	0h	0: Writing of 0 is ignored. Always reads back a 0. 1: Forces a LOAD to occur on the DCCAP - an equivalent LOAD.active pulse
7 - 5	RESERVED	R		Reserved
4	PULSECTL	R/W	0h	Capture Input Polarity Select Mux: 0: Pulse selection determined by PULSESEL bits (common pulse selection for Blanking and Capture logic) 1: Pulse selection determined by CAPMIXSEL register (independent pulse selection for Blaning and Capture logic)
3	CAPINPOL	R/W	0h	Capture Input Polarity Select Mux: 0: CAPIN.sync not inverted 1: CAPIN.sync Inverted Default state assumption for these inputs can be active high. If the user is providing active low signal then invert option can be configured
2 - 1	CAPGATEPOL	R/W	0h	Capture Gate Input Polarity Select Mux: 00: Set to 1 - Gate is always ON 01: Set to 0 - Gate is always OFF 10: CAPGATE.sync 11: CAPGATE.sync Inverted Default state assumption for these inputs can be active high. If the user is providing active low signal then invert option can be configured
0	SRCSEL	R/W	0h	Capture Logic Input Select Mux: 0: DCEVTFILT (Sync) - same as Type-4 1: CAPIN.sync

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3.9.93 CONTROLSS_Gm_EPWMn_CAPGATETRIPSEL Registers

3.9.93.1 Gm_EPWMn_CAPGATETRIPSEL Register (Offset = 1AEh) [reset = h]

Short Description: Event Capture Gate Trip input select

Long Description:

Return to Summary Table

Table 3-585. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-166. CAPGATETRIPSEL Name Register

15	14	13	12	11	10	9	8
RESERVED	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-586. CAPGATETRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0: Trip Input 15 not selected as combinational ORed input 1: Trip Input 15 selected as combinational ORed input to CAPGATE mux
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0: Trip Input 14 not selected as combinational ORed input 1: Trip Input 14 selected as combinational ORed input to CAPGATE mux
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0: Trip Input 13 not selected as combinational ORed input 1: Trip Input 13 selected as combinational ORed input to CAPGATE mux
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0: Trip Input 12 not selected as combinational ORed input 1: Trip Input 12 selected as combinational ORed input to CAPGATE mux
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0: Trip Input 11 not selected as combinational ORed input 1: Trip Input 11 selected as combinational ORed input to CAPGATE mux
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0: Trip Input 10 not selected as combinational ORed input 1: Trip Input 10 selected as combinational ORed input to CAPGATE mux
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0: Trip Input 9 not selected as combinational ORed input 1: Trip Input 9 selected as combinational ORed input to CAPGATE mux
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0: Trip Input 8 not selected as combinational ORed input 1: Trip Input 8 selected as combinational ORed input to CAPGATE mux
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0: Trip Input 7 not selected as combinational ORed input 1: Trip Input 7 selected as combinational ORed input to CAPGATE mux
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0: Trip Input 6 not selected as combinational ORed input 1: Trip Input 6 selected as combinational ORed input to CAPGATE mux

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Table 3-586. CAPGATETRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0: Trip Input 5 not selected as combinational ORed input 1: Trip Input 5 selected as combinational ORed input to CAPGATE mux
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0: Trip Input 4 not selected as combinational ORed input 1: Trip Input 4 selected as combinational ORed input to CAPGATE mux
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0: Trip Input 3 not selected as combinational ORed input 1: Trip Input 3 selected as combinational ORed input to CAPGATE mux
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0: Trip Input 2 not selected as combinational ORed input 1: Trip Input 2 selected as combinational ORed input to CAPGATE mux
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0: Trip Input 1 not selected as combinational ORed input 1: Trip Input 1 selected as combinational ORed input to CAPGATE mux

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3.9.94 CONTROLSS_Gm_EPWMn_CAPINTRIPSEL Registers

3.9.94.1 Gm_EPWMn_CAPINTRIPSEL Register (Offset = 1B0h) [reset = h]

Short Description: Event Capture Trip input select

Long Description:

Return to Summary Table

Table 3-587. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-167. CAPINTRIPSEL Name Register

15	14	13	12	11	10	9	8
RESERVED	TRIPINPUT15	TRIPINPUT14	TRIPINPUT13	TRIPINPUT12	TRIPINPUT11	TRIPINPUT10	TRIPINPUT9
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
TRIPINPUT8	TRIPINPUT7	TRIPINPUT6	TRIPINPUT5	TRIPINPUT4	TRIPINPUT3	TRIPINPUT2	TRIPINPUT1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Access Types Legend

Table 3-588. CAPINTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R		Reserved
14	TRIPINPUT15	R/W	0h	TRIP Input 15 0: Trip Input 15 not selected as combinational ORed input 1: Trip Input 15 selected as combinational ORed input to CAPIN mux
13	TRIPINPUT14	R/W	0h	TRIP Input 14 0: Trip Input 14 not selected as combinational ORed input 1: Trip Input 14 selected as combinational ORed input to CAPIN mux
12	TRIPINPUT13	R/W	0h	TRIP Input 13 0: Trip Input 13 not selected as combinational ORed input 1: Trip Input 13 selected as combinational ORed input to CAPIN mux
11	TRIPINPUT12	R/W	0h	TRIP Input 12 0: Trip Input 12 not selected as combinational ORed input 1: Trip Input 12 selected as combinational ORed input to CAPIN mux
10	TRIPINPUT11	R/W	0h	TRIP Input 11 0: Trip Input 11 not selected as combinational ORed input 1: Trip Input 11 selected as combinational ORed input to CAPIN mux
9	TRIPINPUT10	R/W	0h	TRIP Input 10 0: Trip Input 10 not selected as combinational ORed input 1: Trip Input 10 selected as combinational ORed input to CAPIN mux
8	TRIPINPUT9	R/W	0h	TRIP Input 9 0: Trip Input 9 not selected as combinational ORed input 1: Trip Input 9 selected as combinational ORed input to CAPIN mux
7	TRIPINPUT8	R/W	0h	TRIP Input 8 0: Trip Input 8 not selected as combinational ORed input 1: Trip Input 8 selected as combinational ORed input to CAPIN mux
6	TRIPINPUT7	R/W	0h	TRIP Input 7 0: Trip Input 7 not selected as combinational ORed input 1: Trip Input 7 selected as combinational ORed input to CAPIN mux
5	TRIPINPUT6	R/W	0h	TRIP Input 6 0: Trip Input 6 not selected as combinational ORed input 1: Trip Input 6 selected as combinational ORed input to CAPIN mux

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Table 3-588. CAPINTRIPSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TRIPINPUT5	R/W	0h	TRIP Input 5 0: Trip Input 5 not selected as combinational ORed input 1: Trip Input 5 selected as combinational ORed input to CAPIN mux
3	TRIPINPUT4	R/W	0h	TRIP Input 4 0: Trip Input 4 not selected as combinational ORed input 1: Trip Input 4 selected as combinational ORed input to CAPIN mux
2	TRIPINPUT3	R/W	0h	TRIP Input 3 0: Trip Input 3 not selected as combinational ORed input 1: Trip Input 3 selected as combinational ORed input to CAPIN mux
1	TRIPINPUT2	R/W	0h	TRIP Input 2 0: Trip Input 2 not selected as combinational ORed input 1: Trip Input 2 selected as combinational ORed input to CAPIN mux
0	TRIPINPUT1	R/W	0h	TRIP Input 1 0: Trip Input 1 not selected as combinational ORed input 1: Trip Input 1 selected as combinational ORed input to CAPIN mux

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3.9.95 CONTROLSS_Gm_EPWMn_CAPTRIPSEL Registers

3.9.95.1 Gm_EPWMn_CAPTRIPSEL Register (Offset = 1B2h) [reset = h]

Short Description: Event Capture Signal Select

Long Description:

Return to Summary Table

Table 3-589. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-168. CAPTRIPSEL Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
CAPGATECOMPSEL				CAPINCOMPSEL			
R/W				R/W			
0				0			

Access Types Legend

Table 3-590. CAPTRIPSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R		Reserved
7 - 4	CAPGATECOMPSEL	R/W	0h	Digital Compare A Low Input Select Bits 0000: TRIPIN1 0001: TRIPIN2 0010: TRIPIN3 0011: TRIPIN4 ... 1011: TRIPIN12 1100: Reserved 1101: TRIPIN14 1110: TRIPIN15 1111: Trip combination input (all trip inputs selected by CAPGATETRIPSEL register ORed together)
3 - 0	CAPINCOMPSEL	R/W	0h	Digital Compare A High Input Select Bits 0000: TRIPIN1 0001: TRIPIN2 0010: TRIPIN3 0011: TRIPIN4 ... 1011: TRIPIN12 1100: Reserved 1101: TRIPIN14 1110: TRIPIN15 1111: Trip combination input (all trip inputs selected by CAPINTRIPSEL register ORed together)

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3.9.96 CONTROLSS_Gm_EPWMn_SPARE1 Registers

3.9.96.1 Gm_EPWMn_SPARE1 Register (Offset = 1ECh) [reset = h]

Short Description: Spare1 register

Long Description:

Return to Summary Table

Table 3-591. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-169. SPARE1 Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
SPARE1_BITS							
R/W							
0							

Access Types Legend

Table 3-592. SPARE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R		Reserved
7 - 0	SPARE1_BITS	R/W	0h	Not used in design currently

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3.9.97 CONTROLSS_Gm_EPWMn_SPARE2 Registers

3.9.97.1 Gm_EPWMn_SPARE2 Register (Offset = 1F0h) [reset = h]

Short Description: Spare2 register

Long Description:

Return to Summary Table

Table 3-593. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-170. SPARE2 Name Register

15	14	13	12	11	10	9	8
RESERVED							
R							
0							
7	6	5	4	3	2	1	0
SPARE2_BITS							
R/W							
0							

Access Types Legend

Table 3-594. SPARE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	R		Reserved
7 - 0	SPARE2_BITS	R/W	0h	Not used in design currently

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3.9.98 CONTROLSS_Gm_EPWMn_HWVDELVAL Registers

3.9.98.1 Gm_EPWMn_HWVDELVAL Register (Offset = 1FAh) [reset = h]

Short Description: Hardware Valley Mode Delay Register

Long Description:

Return to Summary Table

Table 3-595. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-171. HWVDELVAL Name Register

15	14	13	12	11	10	9	8
HWVDELVAL							
R							
0							
7	6	5	4	3	2	1	0
HWVDELVAL							
R							
0							

Access Types Legend

Table 3-596. HWVDELVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	HWVDELVAL	R	0h	Hardware Valley Delay Value Register This read only register reflects the hardware delay value calculated by the equations defined in VCAPCTL[VDELAYDIV]. This reflects the latest value from the hardware calculations and can change every time valley capture sequence is triggered and VCAP1 and VCAP2 values are updated.

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3.9.99 CONTROLSS_Gm_EPWMn_VCNTVAL Registers

3.9.99.1 Gm_EPWMn_VCNTVAL Register (Offset = 1FCh) [reset = h]

Short Description: Hardware Valley Counter Register

Long Description:

Return to Summary Table

Table 3-597. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-172. VCNTVAL Name Register

15	14	13	12	11	10	9	8
VCNTVAL							
R							
0							
7	6	5	4	3	2	1	0
VCNTVAL							
R							
0							

Access Types Legend

Table 3-598. VCNTVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	VCNTVAL	R	0h	Valley Time Base Counter Register This register reflects the captured VCNT value upon occurrence of STOPEDGE selected in VCNTCFG register.

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3.9.100 CONTROLSS_Gm_EPWMn_MINDBCFG Registers

3.9.100.1 Gm_EPWMn_MINDBCFG Register (Offset = C00h) [reset = h]

Short Description: Additional Compare 7 Active Register

Long Description:

Return to Summary Table

Table 3-599. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-173. MINDBCFG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							POLSELB	SELB				SELBLOCKB	INVERTB	RESERVED	ENABLEB
R							R/W	R/W				R/W	R/W	R	R/W
0							0	0				0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							POLSELA	SELA				SELBLOCKA	INVERTA	RESERVED	ENABLEA
R							R/W	R/W				R/W	R/W	R	R/W
0							0	0				0	0	0	0

Access Types Legend

Table 3-600. MINDBCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	RESERVED	R		Reserved
24	POLSELB	R/W	0h	Select signal for the AND OR logic of BLOCKB (output of SELBLOCKB mux) and PWMB signals 0 : Select BLOCKB is inverted and ANDed with PWMB. 1 : Select BLOCKB is Ored with PWMB.
23 - 20	SELB	R/W	0h	PWMB min dead band reference 0x0 : DEPWMB 0x1 : Output 1 from PWM output XBAR 0x2 : Output 2 from PWM output XBAR . . 0xf : Output 15 from PWM output XBAR
19	SELBLOCKB	R/W	0h	0 : Select BLOCKB as the blocking signal on PWMB. 1 : Select BLOCKA as the blocking signal on PWMB.
18	INVERTB	R/W	0h	0 : No inversion on the selected reference signal which is used in the min deadband logic on PWMB. 1 : Invert the selected reference signal which is used in the min deadband logic on PWMB.
17	RESERVED	R		Reserved
16	ENABLEB	R/W	0h	0 : Minimum dead band logic is disabled 1 : Minimum dead band logic is enabled
15 - 9	RESERVED	R		Reserved
8	POLSELA	R/W	0h	Select signal for the AND OR logic of BLOCKA (output of SELBLOCKA mux) and PWMA signals 0 : Select BLOCKA is inverted and ANDed with PWMA. 1 : Select BLOCKA is Ored with PWMA.
7 - 4	SELA	R/W	0h	PWMA min dead band reference 0x0 : DEPWMA 0x1 : Output 1 from PWM output XBAR 0x2 : Output 2 from PWM output XBAR . . 0xf : Output 15 from PWM output XBAR
3	SELBLOCKA	R/W	0h	0 : Select BLOCKA as the blocking signal on PWMA. 1 : Select BLOCKB as the blocking signal on PWMB.

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Table 3-600. MINDBCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INVERTA	R/W	0h	0 : No inversion on the selected reference signal which is used in the min deadband logic on PWMA. 1 : Invert the selected reference signal which is used in the min deadband logic on PWMA.
1	RESERVED	R		Reserved
0	ENABLEA	R/W	0h	0 : Minimum dead band logic is disabled 1 : Minimum dead band logic is enabled

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3.9.101 CONTROLSS_Gm_EPWMn_MINDBDLY Registers

3.9.101.1 Gm_EPWMn_MINDBDLY Register (Offset = C04h) [reset = h]

Short Description: Minimum dead band delay register

Long Description:

Return to Summary Table

Table 3-601. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-174. MINDBDLY Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DELAYB															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DELAYA															
R/W															
0															

Access Types Legend

Table 3-602. MINDBDLY Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DELAYB	R/W	0h	Minimum dead band delay on PWMB in terms of SYSCLK cycles. For delay value of 0, user should configure MINDBCFG[ENABLEA/B] = '0'. If MINDBCFG[ENABLEA/B] = '1' and MINDBDLY[DELAYA/B]='0' then delay is '1' cycle is applied.
15 - 0	DELAYA	R/W	0h	Minimum dead band delay on PWMA in terms of SYSCLK cycles. For delay value of 0, user should configure MINDBCFG[ENABLEA/B] = '0'. If MINDBCFG[ENABLEA/B] = '1' and MINDBDLY[DELAYA/B]='0' then delay is '1' cycle is applied.

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3.9.102 CONTROLSS_Gm_EPWMn_LUTCTLA Registers

3.9.102.1 Gm_EPWMn_LUTCTLA Register (Offset = C20h) [reset = h]

Short Description: LUT control register on PWMA

Long Description:

Return to Summary Table

Table 3-603. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-175. LUTCTLA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								LUTDEC7	LUTDEC6	LUTDEC5	LUTDEC4	LUTDEC3	LUTDEC2	LUTDEC1	LUTDEC0
R								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0								0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SELXBAR				RESERVED			BYPASS
R								R/W				R			R/W
0								0				0			1

Access Types Legend

Table 3-604. LUTCTLA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED	R		Reserved
23	LUTDEC7	R/W	0h	0 : Force 0 1 : Force 1
22	LUTDEC6	R/W	0h	0 : Force 0 1 : Force 1
21	LUTDEC5	R/W	0h	0 : Force 0 1 : Force 1
20	LUTDEC4	R/W	0h	0 : Force 0 1 : Force 1
19	LUTDEC3	R/W	0h	0 : Force 0 1 : Force 1
18	LUTDEC2	R/W	0h	0 : Force 0 1 : Force 1
17	LUTDEC1	R/W	0h	0 : Force 0 1 : Force 1
16	LUTDEC0	R/W	0h	0 : Force 0 1 : Force 1
15 - 8	RESERVED	R		Reserved
7 - 4	SELXBAR	R/W	0h	Selects one of the 16 outputs of ICSSXBAR to feed into IN3 of LUTA
3 - 1	RESERVED	R		Reserved
0	BYPASS	R/W	1h	1 : Bypass LUT logic on PWMA 0 : PWMA driven by LUTA

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3.9.103 CONTROLSS_Gm_EPWMn_LUTCTLB Registers

3.9.103.1 Gm_EPWMn_LUTCTLB Register (Offset = C24h) [reset = h]

Short Description: LUT control register on PWMB

Long Description:

Return to Summary Table

Table 3-605. Instance Table

Instance Name	Physical Address
CONTROLSS_Gm_EPWMn	500**N**h

Figure 3-176. LUTCTLB Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								LUTDEC7	LUTDEC6	LUTDEC5	LUTDEC4	LUTDEC3	LUTDEC2	LUTDEC1	LUTDEC0
R								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0								0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SELXBAR				RESERVED			BYPASS
R								R/W				R			R/W
0								0				0			1

Access Types Legend

Table 3-606. LUTCTLB Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED	R		Reserved
23	LUTDEC7	R/W	0h	0 : Force 0 1 : Force 1
22	LUTDEC6	R/W	0h	0 : Force 0 1 : Force 1
21	LUTDEC5	R/W	0h	0 : Force 0 1 : Force 1
20	LUTDEC4	R/W	0h	0 : Force 0 1 : Force 1
19	LUTDEC3	R/W	0h	0 : Force 0 1 : Force 1
18	LUTDEC2	R/W	0h	0 : Force 0 1 : Force 1
17	LUTDEC1	R/W	0h	0 : Force 0 1 : Force 1
16	LUTDEC0	R/W	0h	0 : Force 0 1 : Force 1
15 - 8	RESERVED	R		Reserved
7 - 4	SELXBAR	R/W	0h	Selects one of the 16 outputs of ICSSXBAR to feed into IN3 of LUTB
3 - 1	RESERVED	R		Reserved
0	BYPASS	R/W	1h	1 : Bypass LUT logic on PWMB 0 : PWMB driven by LUTB

3.9.104 Access Table

Table 3-607. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write
R-0/W	R-0/W	Read returns 0s/Write
R	R	Read
R-0	R-0	Read returns 0s
RWONCE WONCE	RWONCE WONCE	Read/Write Once

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3.10 EQEP Registers

Table 3-608. CONTROLSS_EQEP[0:2] Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_EQEP0 Physical Address	CONTROLSS_EQEP1 Physical Address	CONTROLSS_EQEP2 Physical Address
0h	32	EQEP_QPOSCNT	5027 0000h	5027 1000h	5027 2000h
4h	32	EQEP_QPOSINIT	5027 0004h	5027 1004h	5027 2004h
8h	32	EQEP_QPOSMAX	5027 0008h	5027 1008h	5027 2008h
Ch	32	EQEP_QPOSCMP	5027 000Ch	5027 100Ch	5027 200Ch
10h	32	EQEP_QPOSILAT	5027 0010h	5027 1010h	5027 2010h
14h	32	EQEP_QPOSSLAT	5027 0014h	5027 1014h	5027 2014h
18h	32	EQEP_QPOSLAT	5027 0018h	5027 1018h	5027 2018h
1Ch	32	EQEP_QUTMR	5027 001Ch	5027 101Ch	5027 201Ch
20h	32	EQEP_QUPRD	5027 0020h	5027 1020h	5027 2020h
24h	16	EQEP_QWDTMR	5027 0024h	5027 1024h	5027 2024h
26h	16	EQEP_QWDPRD	5027 0026h	5027 1026h	5027 2026h
28h	16	EQEP_QDECCTL	5027 0028h	5027 1028h	5027 2028h
2Ah	16	EQEP_QEPCTL	5027 002Ah	5027 102Ah	5027 202Ah
2Ch	16	EQEP_QCAPCTL	5027 002Ch	5027 102Ch	5027 202Ch
2Eh	16	EQEP_QPOSCTL	5027 002Eh	5027 102Eh	5027 202Eh
30h	16	EQEP_QEINT	5027 0030h	5027 1030h	5027 2030h
32h	16	EQEP_QFLG	5027 0032h	5027 1032h	5027 2032h
34h	16	EQEP_QCLR	5027 0034h	5027 1034h	5027 2034h
36h	16	EQEP_QFRC	5027 0036h	5027 1036h	5027 2036h
38h	16	EQEP_QEPSTS	5027 0038h	5027 1038h	5027 2038h
3Ah	16	EQEP_QCTMR	5027 003Ah	5027 103Ah	5027 203Ah
3Ch	16	EQEP_QCPRD	5027 003Ch	5027 103Ch	5027 203Ch
3Eh	16	EQEP_QCTMRLAT	5027 003Eh	5027 103Eh	5027 203Eh
40h	16	EQEP_QCPRDLAT	5027 0040h	5027 1040h	5027 2040h
60h	32	EQEP_REV	5027 0060h	5027 1060h	5027 2060h
64h	32	EQEP_QEPSTROBESEL	5027 0064h	5027 1064h	5027 2064h
68h	32	EQEP_QMACTRL	5027 0068h	5027 1068h	5027 2068h
6Ch	32	EQEP_QEPSRCSEL	5027 006Ch	5027 106Ch	5027 206Ch

3.10.1 EQEP Instance Count Note

Note

n = 0 to 2 for the EQEP registers defined below.

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3.10.2 CONTROLSS_EQEPn_QPOSCNT Registers

3.10.2.1 EQEPn_QPOSCNT Register (Offset = 0h) [reset = h]

Short Description: Position Counter

Long Description:

Return to Summary Table

Table 3-609. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0000h
CONTROLSS_EQEP1	5027 1000h
CONTROLSS_EQEP2	5027 2000h

Access Types Legend

Table 3-610. QPOSCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QPOSCNT	RW	0h	Position Counter This 32-bit position counter register counts up/down on every eQEP pulse based on direction input. This counter acts as a position integrator whose count value is proportional to position from a give reference point. This Register acts as a Read ONLY register while counter is counting up/down. Note: It is recommended to only write to the position counter register (QPOSCNT) during initialization, i.e. when the eQEP position counter is disabled (QPEN bit of QEPCTL is zero). Once the position counter is enabled (QPEN bit is one), writing to the eQEP position counter register (QPOSCNT) may cause unexpected results.

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3.10.3 CONTROLSS_EQEPn_QPOSINIT Registers

3.10.3.1 EQEPn_QPOSINIT Register (Offset = 4h) [reset = h]

Short Description: Position Counter Init

Long Description:

Return to Summary Table

Table 3-611. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0004h
CONTROLSS_EQEP1	5027 1004h
CONTROLSS_EQEP2	5027 2004h

Access Types Legend

Table 3-612. QPOSINIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QPOSINIT	RW	0h	Position Counter Init This register contains the position value that is used to initialize the position counter based on external strobe or index event. The position counter can be initialized through software. Writes to this register should always be full 32-bit writes.

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3.10.4 CONTROLSS_EQEPn_QPOSMAX Registers

3.10.4.1 EQEPn_QPOSMAX Register (Offset = 8h) [reset = h]

Short Description: Maximum Position Count

Long Description:

Return to Summary Table

Table 3-613. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0008h
CONTROLSS_EQEP1	5027 1008h
CONTROLSS_EQEP2	5027 2008h

Access Types Legend

Table 3-614. QPOSMAX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QPOSMAX	RW	0h	Maximum Position Count This register contains the maximum position counter value. Writes to this register should always be full 32-bit writes.

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3.10.5 CONTROLSS_EQEPn_QPOSCMP Registers

3.10.5.1 EQEPn_QPOSCMP Register (Offset = Ch) [reset = h]

Short Description: Position Compare

Long Description:

Return to Summary Table

Table 3-615. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 000Ch
CONTROLSS_EQEP1	5027 100Ch
CONTROLSS_EQEP2	5027 200Ch

Access Types Legend

Table 3-616. QPOSCMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QPOSCMP	RW	0h	Position Compare The position-compare value in this register is compared with the position counter (QPOSCNT) to generate sync output and/or interrupt on compare match.

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3.10.6 CONTROLSS_EQEPn_QPOSILAT Registers

3.10.6.1 EQEPn_QPOSILAT Register (Offset = 10h) [reset = h]

Short Description: Index Position Latch

Long Description:

Return to Summary Table

Table 3-617. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0010h
CONTROLSS_EQEP1	5027 1010h
CONTROLSS_EQEP2	5027 2010h

Access Types Legend

Table 3-618. QPOSILAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QPOSILAT	RO	0h	Index Position Latch The position-counter value is latched into this register on an index event as defined by the QEPCTL[IEL] bits.

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3.10.7 CONTROLSS_EQEPn_QPOSSLAT Registers

3.10.7.1 EQEPn_QPOSSLAT Register (Offset = 14h) [reset = h]

Short Description: Strobe Position Latch

Long Description:

Return to Summary Table

Table 3-619. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0014h
CONTROLSS_EQEP1	5027 1014h
CONTROLSS_EQEP2	5027 2014h

Access Types Legend

Table 3-620. QPOSSLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QPOSSLAT	RO	0h	Strobe Position Latch The position-counter value is latched into this register on a strobe event as defined by the QEPCTL[SEL] bits.

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3.10.8 CONTROLSS_EQEPn_QPOSLAT Registers

3.10.8.1 EQEPn_QPOSLAT Register (Offset = 18h) [reset = h]

Short Description: Position Latch

Long Description:

Return to Summary Table

Table 3-621. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0018h
CONTROLSS_EQEP1	5027 1018h
CONTROLSS_EQEP2	5027 2018h

Access Types Legend

Table 3-622. QPOSLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QPOSLAT	RO	0h	Position Latch The position-counter value is latched into this register on a unit time out event.

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3.10.9 CONTROLSS_EQEPn_QUTMR Registers

3.10.9.1 EQEPn_QUTMR Register (Offset = 1Ch) [reset = h]

Short Description: QEP Unit Timer

Long Description:

Return to Summary Table

Table 3-623. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 001Ch
CONTROLSS_EQEP1	5027 101Ch
CONTROLSS_EQEP2	5027 201Ch

Access Types Legend

Table 3-624. QUTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QUTMR	RW	0h	QEP Unit Timer This register acts as time base for unit time event generation. When this timer value matches the unit time period value a unit time event is generated.

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3.10.10 CONTROLSS_EQEPn_QUPRD Registers

3.10.10.1 EQEPn_QUPRD Register (Offset = 20h) [reset = h]

Short Description: QEP Unit Period

Long Description:

Return to Summary Table

Table 3-625. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0020h
CONTROLSS_EQEP1	5027 1020h
CONTROLSS_EQEP2	5027 2020h

Access Types Legend

Table 3-626. QUPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	QUPRD	RW	0h	QEP Unit Period This register contains the period count for the unit timer to generate periodic unit time events. These events latch the eQEP position information at periodic intervals and optionally generate an interrupt. Writes to this register should always be full 32-bit writes.

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3.10.11 CONTROLSS_EQEPn_QWDTMR Registers

3.10.11.1 EQEPn_QWDTMR Register (Offset = 24h) [reset = h]

Short Description: QEP Watchdog Timer

Long Description:

Return to Summary Table

Table 3-627. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0024h
CONTROLSS_EQEP1	5027 1024h
CONTROLSS_EQEP2	5027 2024h

Access Types Legend

Table 3-628. QWDTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	QWDTMR	RW	0h	QEP Watchdog Timer This register acts as time base for the watchdog to detect motor stalls. When this timer value matches with the watchdog's period value a watchdog timeout interrupt is generated. This register is reset upon edge transition in quadrature-clock indicating the motion.

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3.10.12 CONTROLSS_EQEPn_QWDPRD Registers

3.10.12.1 EQEPn_QWDPRD Register (Offset = 26h) [reset = h]

Short Description: QEP Watchdog Period

Long Description:

Return to Summary Table

Table 3-629. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0026h
CONTROLSS_EQEP1	5027 1026h
CONTROLSS_EQEP2	5027 2026h

Access Types Legend

Table 3-630. QWDPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	QWDPRD	RW	0h	QEP Watchdog Period This register contains the time-out count for the eQEP peripheral watch dog timer. When the watchdog timer value matches the watchdog period value, a watchdog timeout interrupt is generated.

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3.10.13 CONTROLSS_EQEPn_QDECCTL Registers

3.10.13.1 EQEPn_QDECCTL Register (Offset = 28h) [reset = h]

Short Description: Quadrature Decoder Control

Long Description:

Return to Summary Table

Table 3-631. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0028h
CONTROLSS_EQEP1	5027 1028h
CONTROLSS_EQEP2	5027 2028h

Access Types Legend

Table 3-632. QDECCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	QSRC	RW	0h	Position-counter source selection
13	SOEN	RW	0h	Sync output-enable 0 | SYNC_DISABLEDisable position-compare sync output 1 | SYNC_ENABLEEnable position-compare sync output
12	SPSEL	RW	0h	Sync output pin selection 0 | INDEX_PINIndex pin is used for sync output 1 | STROBE_PINStrobe pin is used for sync output
11	XCR	RW	0h	External Clock Rate 0 | XCR_2XRESOL2x resolution: Count the rising/falling edge 1 | XCR_1XRESOL1x resolution: Count the rising edge only
10	SWAP	RW	0h	CLK/DIR Signal Source for Position Counter 0 | SWAP_DISABLEQuadrature-clock inputs are not swapped 1 | SWAP_ENABLEQuadrature-clock inputs are swapped
9	IGATE	RW	0h	Index pulse gating option 0 | IGATE_DISABLEDisable gating of Index pulse 1 | IGATE_ENABLEGate the index pin with strobe
8	QAP	RW	0h	QEPA input polarity 0 | QAP_NOPOLARNo effect 1 | QAP_POLARNegates QEPA input
7	QBP	RW	0h	QEPB input polarity 0 | QBP_NOPOLARNo effect 1 | QBP_POLARNegates QEPB input
6	QIP	RW	0h	QEPI input polarity 0 | QIP_NOPOLARNo effect 1 | QIP_POLARNegates QEPI input
5	QSP	RW	0h	QEPS input polarity 0 | QSP_NOPOLARNo effect 1 | QSP_POLARNegates QEPS input
4 - 1	RESERVED	RO		Reserved
0	QIDIRE	RW	0h	0 - Compatible mode, Behavior same as existing devices 1 - Enhancement for Direction change during Index will be enabled

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3.10.14 CONTROLSS_EQEPn_QEPCTL Registers

3.10.14.1 EQEPn_QEPCTL Register (Offset = 2Ah) [reset = h]

Short Description: QEP Control

Long Description:

Return to Summary Table

Table 3-633. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 002Ah
CONTROLSS_EQEP1	5027 102Ah
CONTROLSS_EQEP2	5027 202Ah

Access Types Legend

Table 3-634. QEPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	FREE_SOFT	RW	0h	Emulation mode 0x0 | FREE_SOFT_0QPOSCNT behavior Position counter stops immediately on emulation suspend 0h (R/W) = QWDTMR behavior Watchdog counter stops immediately 0h (R/W) = QUTMR behavior Unit timer stops immediately 0h (R/W) = QCTMR behavior Capture Timer stops immediately 0x1 | FREE_SOFT_1QPOSCNT behavior Position counter continues to count until the rollover 1h (R/W) = QWDTMR behavior Watchdog counter counts until WD period match roll over 1h (R/W) = QUTMR behavior Unit timer counts until period rollover 1h (R/W) = QCTMR behavior Capture Timer counts until next unit period event 0x2 | FREE_SOFT_2QPOSCNT behavior Position counter is unaffected by emulation suspend 2h (R/W) = QWDTMR behavior Watchdog counter is unaffected by emulation suspend 2h (R/W) = QUTMR behavior Unit timer is unaffected by emulation suspend 2h (R/W) = QCTMR behavior Capture Timer is unaffected by emulation suspend 0x3 | FREE_SOFT_3Same as FREE_SOFT_2
13 - 12	PCRM	RW	0h	Postion counter reset 0x0 | PCRM_INDEXPosition counter reset on an index event 0x1 | PCRM_MAXPOSPosition counter reset on the maximum position 0x2 | PCRM_FIRSTINDEXPosition counter reset on the first index event 0x3 | PCRM_TIMEEVENTPosition counter reset on a unit time event
11 - 10	SEI	RW	0h	Strobe event initialization of position counter 0x0 | SEI_NOTHING0Does nothing (action disabled) 0x1 | SEI_NOTHING1Does nothing (action disabled) 0x2 | SEI_INITQEPSRISINGInitializes the position counter on rising edge of the QEPS signal 0x3 | SEI_INITQEPSCLOCKClockwise Direction: Initializes the position counter on the rising edge of QEPS strobe Counter Clockwise Direction: Initializes the position counter on the falling edge of QEPS strobe
9 - 8	IEI	RW	0h	Index event init of position count 0x0 | IEI_NOTHING0Do nothing (action disabled) 0x1 | IEI_NOTHING1Do nothing (action disabled) 0x2 | IEI_INITRISINGInitializes the position counter on the rising edge of the QEPI signal (QPOSCNT = QPOSINIT) 0x3 | IEI_INITFALLINGInitializes the position counter on the falling edge of QEPI signal (QPOSCNT = QPOSINIT)
7	SWI	RW	0h	Software init position counter 0 | SWI_NOTHINGDo nothing (action disabled) 1 | SWI_INITPOSInitialize position counter (QPOSCNT=QPOSINIT). This bit is not cleared automatically

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Table 3-634. QEPCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SEL	RW	0h	Strobe event latch of position counter 0 | SEL_QEPSRISINGThe position counter is latched on the rising edge of QEPS strobe (QPOSSLAT = POSCCNT). Latching on the falling edge can be done by inverting the strobe input using the QSP bit in the QDECCTL register 1 | SEL_QEPSCLOCKClockwise Direction: Position counter is latched on rising edge of QEPS strobe Counter Clockwise Direction: Position counter is latched on falling edge of QEPS strobe
5 - 4	IEL	RW	0h	Index event latch of position counter (software index marker) 0x0 | IEL_RSVDReserved 0x1 | IEL_POSRISINGLatches position counter on rising edge of the index signal 0x2 | IEL_POSFALLINGLatches position counter on falling edge of the index signal 0x3 | IEL_SIMSoftware index marker. Latches the position counter and quadrature direction flag on index event marker. The position counter is latched to the QPOSILAT register and the direction flag is latched in the QEPSTS[QDLF] bit. This mode is useful for software index marking.
3	QPEN	RW	0h	Quadrature position counter enable/software reset 0 | QPEN_RESETReset the eQEP peripheral internal operating flags/ read-only registers. Control/configuration registers are not disturbed by a software reset. When QPEN is disabled, some flags in the QFLG register do not get reset or cleared and show the actual state of that flag. 1 | QPEN_ENABLEeQEP position counter is enabled
2	QCLM	RW	0h	QEP capture latch mode 0 | QCLM_CPULatch on position counter read by CPU. Capture timer and capture period values are latched into QCTMRLAT and QCPRDLAT registers when CPU reads the QPOSCNT register. 1 | QCLM_TIMEOUTLatch on unit time out. Position counter, capture timer and capture period values are latched into QPOSLAT, QCTMRLAT and QCPRDLAT registers on unit time out.
1	UTE	RW	0h	QEP unit timer enable 0 | UTE_DISABLEDisable eQEP unit timer 1 | UTE_ENABLEEnable unit timer
0	WDE	RW	0h	QEP watchdog enable 0 | WDE_DISABLEDisable the eQEP watchdog timer 1 | WDE_ENABLEEnable the eQEP watchdog timer

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3.10.15 CONTROLSS_EQEPn_QCAPCTL Registers

3.10.15.1 EQEPn_QCAPCTL Register (Offset = 2Ch) [reset = h]

Short Description: Qaudrature Capture Control

Long Description:

Return to Summary Table

Table 3-635. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 002Ch
CONTROLSS_EQEP1	5027 102Ch
CONTROLSS_EQEP2	5027 202Ch

Access Types Legend

Table 3-636. QCAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CEN	RW	0h	Enable eQEP capture 0 | CEN_DISABLEeQEP capture unit is disabled 1 | CEN_ENABLEeQEP capture unit is enabled
14 - 7	RESERVED	RO		Reserved
6 - 4	CCPS	RW	0h	eQEP capture timer clock prescaler 0x0 | SYSCLKOUT1CAPCLK = SYSCLKOUT/1 0x1 | SYSCLKOUT2CAPCLK = SYSCLKOUT/2 0x2 | SYSCLKOUT4CAPCLK = SYSCLKOUT/4 0x3 | SYSCLKOUT8CAPCLK = SYSCLKOUT/8 0x4 | SYSCLKOUT16CAPCLK = SYSCLKOUT/16 0x5 | SYSCLKOUT32CAPCLK = SYSCLKOUT/32 0x6 | SYSCLKOUT64CAPCLK = SYSCLKOUT/64 0x7 | SYSCLKOUT128CAPCLK = SYSCLKOUT/128
3 - 0	UPPS	RW	0h	Unit position event prescaler 0x0 | QCLK1UPEVNT = QCLK/1 0x1 | QCLK2UPEVNT = QCLK/2 0x2 | QCLK4UPEVNT = QCLK/4 0x3 | QCLK8UPEVNT = QCLK/8 0x4 | QCLK16UPEVNT = QCLK/16 0x5 | QCLK32UPEVNT = QCLK/32 0x6 | QCLK64UPEVNT = QCLK/64 0x7 | QCLK128UPEVNT = QCLK/128 0x8 | QCLK256UPEVNT = QCLK/256 0x9 | QCLK512UPEVNT = QCLK/512 0xA | QCLK1024UPEVNT = QCLK/1024 0xB | QCLK2048UPEVNT = QCLK/2048 0xC | QCLK_RSVD0Reserved 0xD | QCLK_RSVD1Reserved 0xE | QCLK_RSVD2Reserved 0xF | QCLK_RSVD3Reserved

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3.10.16 CONTROLSS_EQEPn_QPOSCTL Registers

3.10.16.1 EQEPn_QPOSCTL Register (Offset = 2Eh) [reset = h]

Short Description: Position Compare Control

Long Description:

Return to Summary Table

Table 3-637. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 002Eh
CONTROLSS_EQEP1	5027 102Eh
CONTROLSS_EQEP2	5027 202Eh

Access Types Legend

Table 3-638. QPOSCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PCSHDW	RW	0h	Position compare of shadow enable 0 | PCSHDW_DISABLEShadow disabled, load Immediate 1 | PCSHDW_ENABLEShadow enabled
14	PCLOAD	RW	0h	Position compare of shadow load 0 | PCLOAD_0Load on QPOSCNT = 0 1 | PCLOAD_QPOSCMPLoad when QPOSCNT = QPOSCMP
13	PCPOL	RW	0h	Polarity of sync output 0 | PCPOL_HIGHActive HIGH pulse output 1 | PCPOL_LOWActive LOW pulse output
12	PCE	RW	0h	Position compare enable/disable 0 | PCE_DISABLEDisable position compare unit 1 | PCE_ENABLEEnable position compare unit
11 - 0	PCSPW	RW	0h	Select-position-compare sync output pulse width 0x000 | SYSCLKOUT41 * 4 * SYSCLKOUT cycles 0x001 | SYSCLKOUT82 * 4 * SYSCLKOUT cycles 0xFFF | SYSCLKOUT163844096 * 4 * SYSCLKOUT cycles

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3.10.17 CONTROLSS_EQEPn_QFLG Registers

3.10.17.1 EQEPn_QFLG Register (Offset = 32h) [reset = h]

Short Description: QEP Interrupt Flag

Long Description:

Return to Summary Table

Table 3-639. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0032h
CONTROLSS_EQEP1	5027 1032h
CONTROLSS_EQEP2	5027 2032h

Access Types Legend

Table 3-640. QFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	QMAE	RO	0h	QMA Error interrupt flag Read0 | QMAE_NOFLAGNo interrupt generated Read1 | QMAE_FLAGInterrupt was generated
11	UTO	RO	0h	Unit time out interrupt flag Read0 | UTO_NOFLAGNo interrupt generated Read1 | UTO_FLAGSet by eQEP unit timer period match
10	IEL	RO	0h	Index event latch interrupt flag Read0 | IEL_NOFLAGNo interrupt generated Read1 | IEL_FLAGThis bit is set after latching the QPOSCNT to QPOSILAT
9	SEL	RO	0h	Strobe event latch interrupt flag Read0 | SEL_NOFLAGNo interrupt generated Read1 | SEL_FLAGThis bit is set after latching the QPOSCNT to QPOSSLAT
8	PCM	RO	0h	eQEP compare match event interrupt flag Read0 | PCM_NOFLAGNo interrupt generated Read1 | PCM_FLAGThis bit is set on position-compare match
7	PCR	RO	0h	Position-compare ready interrupt flag Read0 | PCR_NOFLAGNo interrupt generated Read1 | PCR_FLAGThis bit is set after transferring the shadow register value to the active position compare register
6	PCO	RO	0h	Position counter overflow interrupt flag Read0 | PCO_NOFLAGNo interrupt generated Read1 | PCO_FLAGThis bit is set on position counter overflow.
5	PCU	RO	0h	Position counter underflow interrupt flag Read0 | PCU_NOFLAGNo interrupt generated Read1 | PCU_FLAGThis bit is set on position counter underflow.
4	WTO	RO	0h	Watchdog timeout interrupt flag Read0 | WTO_NOFLAGNo interrupt generated Read1 | WTO_FLAGSet by watchdog timeout
3	QDC	RO	0h	Quadrature direction change interrupt flag Read0 | QDC_NOFLAGNo interrupt generated Read1 | QDC_FLAGInterrupt was generated
2	PHE	RO	0h	Quadrature phase error interrupt flag Read0 | PHE_NOFLAGNo interrupt generated Read1 | PHE_FLAGSet on simultaneous transition of QEPA and QEPB
1	PCE	RO	0h	Position counter error interrupt flag Read0 | PCE_NOFLAGNo interrupt generated Read1 | PCE_FLAGPosition counter error
0	INT	RO	0h	Global interrupt status flag Read0 | INT_NOFLAGNo interrupt generated Read1 | INT_FLAGInterrupt was generated

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3.10.18 CONTROLSS_EQEPn_QCLR Registers

3.10.18.1 EQEPn_QCLR Register (Offset = 34h) [reset = h]

Short Description: QEP Interrupt Clear

Long Description:

Return to Summary Table

Table 3-641. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0034h
CONTROLSS_EQEP1	5027 1034h
CONTROLSS_EQEP2	5027 2034h

Access Types Legend

Table 3-642. QCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	QMAE	RW RRETURNS 0S	0h	Clear QMA Error interrupt flag 0 | QMAE_NOEFFECTNo effect 1 | QMAE_CLRClears the interrupt flag
11	UTO	RW RRETURNS 0S	0h	Clear unit time out interrupt flag 0 | UTO_NOEFFECTNo effect 1 | UTO_CLRClears the interrupt flag
10	IEL	RW RRETURNS 0S	0h	Clear index event latch interrupt flag 0 | IEL_NOEFFECTNo effect 1 | IEL_CLRClears the interrupt flag
9	SEL	RW RRETURNS 0S	0h	Clear strobe event latch interrupt flag 0 | SEL_NOEFFECTNo effect 1 | SEL_CLRClears the interrupt flag
8	PCM	RW RRETURNS 0S	0h	Clear eQEP compare match event interrupt flag 0 | PCM_NOEFFECTNo effect 1 | PCM_CLRClears the interrupt flag
7	PCR	RW RRETURNS 0S	0h	Clear position-compare ready interrupt flag 0 | PCR_NOEFFECTNo effect 1 | PCR_CLRClears the interrupt flag
6	PCO	RW RRETURNS 0S	0h	Clear position counter overflow interrupt flag 0 | PCO_NOEFFECTNo effect 1 | PCO_CLRClears the interrupt flag
5	PCU	RW RRETURNS 0S	0h	Clear position counter underflow interrupt flag 0 | PCU_NOEFFECTNo effect 1 | PCU_CLRClears the interrupt flag
4	WTO	RW RRETURNS 0S	0h	Clear watchdog timeout interrupt flag 0 | WTO_NOEFFECTNo effect 1 | WTO_CLRClears the interrupt flag
3	QDC	RW RRETURNS 0S	0h	Clear quadrature direction change interrupt flag 0 | QDC_NOEFFECTNo effect 1 | QDC_CLRClears the interrupt flag
2	PHE	RW RRETURNS 0S	0h	Clear quadrature phase error interrupt flag 0 | PHE_NOEFFECTNo effect 1 | PHE_CLRClears the interrupt flag
1	PCE	RW RRETURNS 0S	0h	Clear position counter error interrupt flag 0 | PCE_NOEFFECTNo effect 1 | PCE_CLRClears the interrupt flag

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Table 3-642. QCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	INT	RW RRETURNS 0S	0h	Global interrupt clear flag 0 | INT_NOEFFECTNo effect 1 | INT_CLRClears the interrupt flag

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3.10.19 CONTROLSS_EQEPn_QFRC Registers

3.10.19.1 EQEPn_QFRC Register (Offset = 36h) [reset = h]

Short Description: QEP Interrupt Force

Long Description:

Return to Summary Table

Table 3-643. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0036h
CONTROLSS_EQEP1	5027 1036h
CONTROLSS_EQEP2	5027 2036h

Access Types Legend

Table 3-644. QFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	QMAE	RW	0h	Force QMA error interrupt 0 | QMAE_NOEFFECTNo effect 1 | QMAE_FORCEForce the interrupt
11	UTO	RW	0h	Force unit time out interrupt 0 | UTO_NOEFFECTNo effect 1 | UTO_FORCEForce the interrupt
10	IEL	RW	0h	Force index event latch interrupt 0 | IEL_NOEFFECTNo effect 1 | IEL_FORCEForce the interrupt
9	SEL	RW	0h	Force strobe event latch interrupt 0 | SEL_NOEFFECTNo effect 1 | SEL_FORCEForce the interrupt
8	PCM	RW	0h	Force position-compare match interrupt 0 | PCM_NOEFFECTNo effect 1 | PCM_FORCEForce the interrupt
7	PCR	RW	0h	Force position-compare ready interrupt 0 | PCR_NOEFFECTNo effect 1 | PCR_FORCEForce the interrupt
6	PCO	RW	0h	Force position counter overflow interrupt 0 | PCO_NOEFFECTNo effect 1 | PCO_FORCEForce the interrupt
5	PCU	RW	0h	Force position counter underflow interrupt 0 | PCU_NOEFFECTNo effect 1 | PCU_FORCEForce the interrupt
4	WTO	RW	0h	Force watchdog time out interrupt 0 | WTO_NOEFFECTNo effect 1 | WTO_FORCEForce the interrupt
3	QDC	RW	0h	Force quadrature direction change interrupt 0 | QDC_NOEFFECTNo effect 1 | QDC_FORCEForce the interrupt
2	PHE	RW	0h	Force quadrature phase error interrupt 0 | PHE_NOEFFECTNo effect 1 | PHE_FORCEForce the interrupt
1	PCE	RW	0h	Force position counter error interrupt 0 | PCE_NOEFFECTNo effect 1 | PCE_FORCEForce the interrupt
0	RESERVED	RO		Reserved

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3.10.20 CONTROLSS_EQEPn_QEINT Registers

3.10.20.1 EQEPn_QEINT Register (Offset = 30h) [reset = h]

Short Description: QEP Interrupt Control

Long Description:

Return to Summary Table

Table 3-645. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0030h
CONTROLSS_EQEP1	5027 1030h
CONTROLSS_EQEP2	5027 2030h

Access Types Legend

Table 3-646. QEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	QMAE	RW	0h	QMA Error Interrupt enable 0 | QMAE_DISABLEInterrupt is disabled 1 | QMAE_ENABLEInterrupt is enabled
11	UTO	RW	0h	Unit time out interrupt enable 0 | UTO_DISABLEInterrupt is disabled 1 | UTO_ENABLEInterrupt is enabled
10	IEL	RW	0h	Index event latch interrupt enable 0 | IEL_DISABLEInterrupt is disabled 1 | IEL_ENABLEInterrupt is enabled
9	SEL	RW	0h	Strobe event latch interrupt enable 0 | SEL_DISABLEInterrupt is disabled 1 | SEL_ENABLEInterrupt is enabled
8	PCM	RW	0h	Position-compare match interrupt enable 0 | PCM_DISABLEInterrupt is disabled 1 | PCM_ENABLEInterrupt is enabled
7	PCR	RW	0h	Position-compare ready interrupt enable 0 | PCR_DISABLEInterrupt is disabled 1 | PCR_ENABLEInterrupt is enabled
6	PCO	RW	0h	Position counter overflow interrupt enable 0 | PCO_DISABLEInterrupt is disabled 1 | PCO_ENABLEInterrupt is enabled
5	PCU	RW	0h	Position counter underflow interrupt enable 0 | PCU_DISABLEInterrupt is disabled 1 | PCU_ENABLEInterrupt is enabled
4	WTO	RW	0h	Watchdog time out interrupt enable 0 | WTO_DISABLEInterrupt is disabled 1 | WTO_ENABLEInterrupt is enabled
3	QDC	RW	0h	Quadrature direction change interrupt enable 0 | QDC_DISABLEInterrupt is disabled 1 | QDC_ENABLEInterrupt is enabled
2	QPE	RW	0h	Quadrature phase error interrupt enable 0 | QPE_DISABLEInterrupt is disabled 1 | QPE_ENABLEInterrupt is enabled
1	PCE	RW	0h	Position counter error interrupt enable 0 | PCE_DISABLEInterrupt is disabled 1 | PCE_ENABLEInterrupt is enabled
0	RESERVED	RO		Reserved

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3.10.21 CONTROLSS_EQEPn_QEPSTS Registers

3.10.21.1 EQEPn_QEPSTS Register (Offset = 38h) [reset = h]

Short Description: QEP Status

Long Description:

Return to Summary Table

Table 3-647. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0038h
CONTROLSS_EQEP1	5027 1038h
CONTROLSS_EQEP2	5027 2038h

Access Types Legend

Table 3-648. QEPSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO		Reserved
7	UPEVNT	RW	1h	Unit position event flag 0 | UPEVNT_NODETCTNo unit position event detected 1 | UPEVNT_DETCTUnit position event detected. Write 1 to clear
6	FIDF	RO	0h	Direction on the first index marker Status of the direction is latched on the first index event marker. Read0 | FIDF_COUNTERCLKCounter-clockwise rotation (or reverse movement) on the first index event Read1 | FIDF_CLKClockwise rotation (or forward movement) on the first index event
5	QDF	RO	0h	Quadrature direction flag Read0 | QDF_COUNTERCLKCounter-clockwise rotation (or reverse movement) Read1 | QDF_CLKClockwise rotation (or forward movement)
4	QDLF	RO	0h	eQEP direction latch flag Read0 | QDLF_COUNTERCLKCounter-clockwise rotation (or reverse movement) on index event marker Read1 | QDLF_CLKClockwise rotation (or forward movement) on index event marker
3	COEF	RW	0h	Capture overflow error flag 0 | COEF_WRT1Overflow has not occurred. 1 | COEF_OVFOverflow occurred in eQEP Capture timer (QEPCTMR). This bit is cleared by writing a '1'.
2	CDEF	RW	0h	Capture direction error flag 0 | CDEF_WRT1Capture direction error has not occurred. 1 | CDEF_DIRECTDirection change occurred between the capture position event. This bit is cleared by writing a '1'.
1	FIMF	RW	0h	First index marker flag 0 | FIMF_WRT1First index pulse has not occurred. 1 | FIMF_SETINDEXSet by first occurrence of index pulse. This bit is cleared by writing a '1'.
0	PCEF	RO	0h	Position counter error flag. This bit is not sticky and it is updated for every index event. Read0 | PCEF_NOERRORNo error occurred during the last index transition Read1 | PCEF_ERRORPosition counter error

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3.10.22 CONTROLSS_EQEPn_QCTMR Registers

3.10.22.1 EQEPn_QCTMR Register (Offset = 3Ah) [reset = h]

Short Description: QEP Capture Timer

Long Description:

Return to Summary Table

Table 3-649. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 003Ah
CONTROLSS_EQEP1	5027 103Ah
CONTROLSS_EQEP2	5027 203Ah

Access Types Legend

Table 3-650. QCTMR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	QCTMR	RW	0h	This register provides time base for edge capture unit.

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3.10.23 CONTROLSS_EQEPn_QCPRD Registers

3.10.23.1 EQEPn_QCPRD Register (Offset = 3Ch) [reset = h]

Short Description: QEP Capture Period

Long Description:

Return to Summary Table

Table 3-651. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 003Ch
CONTROLSS_EQEP1	5027 103Ch
CONTROLSS_EQEP2	5027 203Ch

Access Types Legend

Table 3-652. QCPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	QCPRD	RW	0h	This register holds the period count value between the last successive eQEP position events

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3.10.24 CONTROLSS_EQEPn_QCTMRLAT Registers

3.10.24.1 EQEPn_QCTMRLAT Register (Offset = 3Eh) [reset = h]

Short Description: QEP Capture Latch

Long Description:

Return to Summary Table

Table 3-653. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 003Eh
CONTROLSS_EQEP1	5027 103Eh
CONTROLSS_EQEP2	5027 203Eh

Access Types Legend

Table 3-654. QCTMRLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	QCTMRLAT	RO	0h	The eQEP capture timer value can be latched into this register on two events viz., unit timeout event, reading the eQEP position counter.

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3.10.25 CONTROLSS_EQEPn_QCPRDLAT Registers

3.10.25.1 EQEPn_QCPRDLAT Register (Offset = 40h) [reset = h]

Short Description: QEP Capture Period Latch

Long Description:

Return to Summary Table

Table 3-655. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0040h
CONTROLSS_EQEP1	5027 1040h
CONTROLSS_EQEP2	5027 2040h

Access Types Legend

Table 3-656. QCPRDLAT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	QCPRDLAT	RO	0h	eQEP capture period value can be latched into this register on two events viz., unit timeout event, reading the eQEP position counter.

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3.10.26 CONTROLSS_EQEPn_REV Registers

3.10.26.1 EQEPn_REV Register (Offset = 60h) [reset = h]

Short Description: QEP Revision Number

Long Description:

Return to Summary Table

Table 3-657. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0060h
CONTROLSS_EQEP1	5027 1060h
CONTROLSS_EQEP2	5027 2060h

Access Types Legend

Table 3-658. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	RESERVED	RO RRETURNS 0S		Reserved
5 - 3	MINOR	RO	2h	This field specifies the Minor Revision number for the eQEP IP.
2 - 0	MAJOR	RO	1h	This field specifies the Major Revision number for the eQEP IP.

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3.10.27 CONTROLSS_EQEPn_QEPSTROBESEL Registers

3.10.27.1 EQEPn_QEPSTROBESEL Register (Offset = 64h) [reset = h]

Short Description: QEP Strobe select register

Long Description:

Return to Summary Table

Table 3-659. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0064h
CONTROLSS_EQEP1	5027 1064h
CONTROLSS_EQEP2	5027 2064h

Access Types Legend

Table 3-660. QEPSTROBESEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED	RO RRETURNS 0S		Reserved
1 - 0	STROBESEL	RW	0h	Strobe source select: 0x0 | QS_AFTER_POL_MUXQEP Strobe after polarity mux 0x1 | QS_AFTER_POL_MUXQEP Strobe after polarity mux 0x2 | Reserved 0x3 | Reserved

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3.10.28 CONTROLSS_EQEPn_QMACTRL Registers

3.10.28.1 EQEPn_QMACTRL Register (Offset = 68h) [reset = h]

Short Description: QMA Control register

Long Description:

Return to Summary Table

Table 3-661. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 0068h
CONTROLSS_EQEP1	5027 1068h
CONTROLSS_EQEP2	5027 2068h

Access Types Legend

Table 3-662. QMACTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	RESERVED	RO RRETURNS 0S		Reserved
2 - 0	MODE	RW	0h	Select Mode for QMA mode: 000 : QMA Module is bypassed. 001 : QMA Mode-1 operation selected 010 : QMA Mode-2 operation selected 011 : QMA Module is bypassed (reserved) 1xx : QMA Module is bypassed (reserved)

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3.10.29 CONTROLSS_EQEPn_QEPSRCSEL Registers

3.10.29.1 EQEPn_QEPSRCSEL Register (Offset = 6Ch) [reset = h]

Short Description: QEP Source Select Register

Long Description:

Return to Summary Table

Table 3-663. Instance Table

Instance Name	Physical Address
CONTROLSS_EQEP0	5027 006Ch
CONTROLSS_EQEP1	5027 106Ch
CONTROLSS_EQEP2	5027 206Ch

Access Types Legend

Table 3-664. QEPSRCSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED	RO RRETURNS 0S		Reserved
28 - 24	QEPSSEL	RW	0h	QEP Strobe source select: 0x0: Device Pin (Default) 0x1 to 0x1F : To be defined in SOC context Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running.
23 - 21	RESERVED	RO RRETURNS 0S		Reserved
20 - 16	QEPISEL	RW	0h	QEP Index source select: 0x0: Device Pin (Default) 0x1 to 0x1F : To be defined in SOC context Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running.
15 - 13	RESERVED	RO RRETURNS 0S		Reserved
12 - 8	QEPBSEL	RW	0h	QEPB source select: 0x0: Device Pin (Default) 0x1 to 0x1F : To be defined in SOC context Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running.
7 - 5	RESERVED	RO RRETURNS 0S		Reserved
4 - 0	QEPASEL	RW	0h	QEPA source select: 0x0: Device Pin (Default) 0x1 to 0x1F : To be defined in SOC context Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running.

3.10.30 Access Table

Table 3-665. Access Type Codes

Access Type	Code	Description
RW	RW	Read / Write
RO	RO	Read
RW RRETURNS0S	RW RRETURNS0S	Read returns 0s/Write
RO RRETURNS0S	RO RRETURNS0S	Read returns 0s

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3.11 FSI_RX Registers

Table 3-666. CONTROLSS_FSI_RX[0:1] Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_FSI_RX0 Physical Address	CONTROLSS_FSI_RX1 Physical Address
0h	16	FSI_RX_RX_MASTER_CTRL_ALTC_	5029 0000h	5029 1000h
8h	16	FSI_RX_RX_OPER_CTRL	5029 0008h	5029 1008h
Ch	16	FSI_RX_RX_FRAME_INFO	5029 000Ch	5029 100Ch
Eh	16	FSI_RX_RX_FRAME_TAG_UDATA	5029 000Eh	5029 100Eh
10h	16	FSI_RX_RX_DMA_CTRL	5029 0010h	5029 1010h
14h	16	FSI_RX_RX_EVT_STS_ALT1_	5029 0014h	5029 1014h
16h	16	FSI_RX_RX_CRC_INFO	5029 0016h	5029 1016h
18h	16	FSI_RX_RX_EVT_CLR_ALT1_	5029 0018h	5029 1018h
1Ah	16	FSI_RX_RX_EVT_FRC_ALT1_	5029 001Ah	5029 101Ah
1Ch	16	FSI_RX_RX_BUF_PTR_LOAD	5029 001Ch	5029 101Ch
1Eh	16	FSI_RX_RX_BUF_PTR_STS	5029 001Eh	5029 101Eh
20h	16	FSI_RX_RX_FRAME_WD_CTRL	5029 0020h	5029 1020h
24h	32	FSI_RX_RX_FRAME_WD_REF	5029 0024h	5029 1024h
28h	32	FSI_RX_RX_FRAME_WD_CNT	5029 0028h	5029 1028h
2Ch	16	FSI_RX_RX_PING_WD_CTRL	5029 002Ch	5029 102Ch
2Eh	16	FSI_RX_RX_PING_TAG	5029 002Eh	5029 102Eh
30h	32	FSI_RX_RX_PING_WD_REF	5029 0030h	5029 1030h
34h	32	FSI_RX_RX_PING_WD_CNT	5029 0034h	5029 1034h
38h	16	FSI_RX_RX_INT1_CTRL_ALT1_	5029 0038h	5029 1038h
3Ah	16	FSI_RX_RX_INT2_CTRL_ALT1_	5029 003Ah	5029 103Ah
3Ch	16	FSI_RX_RX_LOCK_CTRL	5029 003Ch	5029 103Ch
40h	32	FSI_RX_RX_ECC_DATA	5029 0040h	5029 1040h
44h	16	FSI_RX_RX_ECC_VAL	5029 0044h	5029 1044h
48h	32	FSI_RX_RX_ECC_SEC_DATA	5029 0048h	5029 1048h
4Ch	16	FSI_RX_RX_ECC_LOG	5029 004Ch	5029 104Ch
50h	16	FSI_RX_RX_FRAME_TAG_CMP	5029 0050h	5029 1050h
52h	16	FSI_RX_RX_PING_TAG_CMP	5029 0052h	5029 1052h
58h	32	FSI_RX_RX_TRIG_CTRL_0	5029 0058h	5029 1058h
5Ch	32	FSI_RX_RX_TRIG_WIDTH_0	5029 005Ch	5029 105Ch
60h	16	FSI_RX_RX_DLYLINE_CTRL	5029 0060h	5029 1060h
64h	32	FSI_RX_RX_TRIG_CTRL_1	5029 0064h	5029 1064h
68h	32	FSI_RX_RX_TRIG_CTRL_2	5029 0068h	5029 1068h
6Ch	32	FSI_RX_RX_TRIG_CTRL_3	5029 006Ch	5029 106Ch
70h	32	FSI_RX_RX_VIS_1	5029 0070h	5029 1070h
74h	16	FSI_RX_RX_UDATA_FILTER	5029 0074h	5029 1074h
80h	16	FSI_RX_RX_BUF_BASE	5029 0080h	5029 1080h

Table 3-667. CONTROLSS_FSI_RX[2:3] Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_FSI_RX2 Physical Address	CONTROLSS_FSI_RX3 Physical Address
0h	16	FSI_RX_RX_MASTER_CTRL_ALTC_	502B 0000h	502B 1000h
8h	16	FSI_RX_RX_OPER_CTRL	502B 0008h	502B 1008h
Ch	16	FSI_RX_RX_FRAME_INFO	502B 000Ch	502B 100Ch
Eh	16	FSI_RX_RX_FRAME_TAG_UDATA	502B 000Eh	502B 100Eh

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Table 3-667. CONTROLSS_FSI_RX[2:3] Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_FSI_RX2 Physical Address	CONTROLSS_FSI_RX3 Physical Address
10h	16	FSI_RX_RX_DMA_CTRL	502B 0010h	502B 1010h
14h	16	FSI_RX_RX_EVT_STS_ALT1_	502B 0014h	502B 1014h
16h	16	FSI_RX_RX_CRC_INFO	502B 0016h	502B 1016h
18h	16	FSI_RX_RX_EVT_CLR_ALT1_	502B 0018h	502B 1018h
1Ah	16	FSI_RX_RX_EVT_FRC_ALT1_	502B 001Ah	502B 101Ah
1Ch	16	FSI_RX_RX_BUF_PTR_LOAD	502B 001Ch	502B 101Ch
1Eh	16	FSI_RX_RX_BUF_PTR_STS	502B 001Eh	502B 101Eh
20h	16	FSI_RX_RX_FRAME_WD_CTRL	502B 0020h	502B 1020h
24h	32	FSI_RX_RX_FRAME_WD_REF	502B 0024h	502B 1024h
28h	32	FSI_RX_RX_FRAME_WD_CNT	502B 0028h	502B 1028h
2Ch	16	FSI_RX_RX_PING_WD_CTRL	502B 002Ch	502B 102Ch
2Eh	16	FSI_RX_RX_PING_TAG	502B 002Eh	502B 102Eh
30h	32	FSI_RX_RX_PING_WD_REF	502B 0030h	502B 1030h
34h	32	FSI_RX_RX_PING_WD_CNT	502B 0034h	502B 1034h
38h	16	FSI_RX_RX_INT1_CTRL_ALT1_	502B 0038h	502B 1038h
3Ah	16	FSI_RX_RX_INT2_CTRL_ALT1_	502B 003Ah	502B 103Ah
3Ch	16	FSI_RX_RX_LOCK_CTRL	502B 003Ch	502B 103Ch
40h	32	FSI_RX_RX_ECC_DATA	502B 0040h	502B 1040h
44h	16	FSI_RX_RX_ECC_VAL	502B 0044h	502B 1044h
48h	32	FSI_RX_RX_ECC_SEC_DATA	502B 0048h	502B 1048h
4Ch	16	FSI_RX_RX_ECC_LOG	502B 004Ch	502B 104Ch
50h	16	FSI_RX_RX_FRAME_TAG_CMP	502B 0050h	502B 1050h
52h	16	FSI_RX_RX_PING_TAG_CMP	502B 0052h	502B 1052h
58h	32	FSI_RX_RX_TRIG_CTRL_0	502B 0058h	502B 1058h
5Ch	32	FSI_RX_RX_TRIG_WIDTH_0	502B 005Ch	502B 105Ch
60h	16	FSI_RX_RX_DLYLINE_CTRL	502B 0060h	502B 1060h
64h	32	FSI_RX_RX_TRIG_CTRL_1	502B 0064h	502B 1064h
68h	32	FSI_RX_RX_TRIG_CTRL_2	502B 0068h	502B 1068h
6Ch	32	FSI_RX_RX_TRIG_CTRL_3	502B 006Ch	502B 106Ch
70h	32	FSI_RX_RX_VIS_1	502B 0070h	502B 1070h
74h	16	FSI_RX_RX_UDATA_FILTER	502B 0074h	502B 1074h
80h	16	FSI_RX_RX_BUF_BASE	502B 0080h	502B 1080h

3.11.1 FSI_RX Instance Count Note

Note

n = 0 to 3 for the FSI_RX registers defined below.

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3.11.2 CONTROLSS_FSI_RXn_RX_MASTER_CTRL_ALTC_ Registers

3.11.2.1 FSI_RXn_RX_MASTER_CTRL_ALTC_ Register (Offset = 0h) [reset = h]

Short Description: Receive master control register

Long Description:

Return to Summary Table

Table 3-668. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0000h
CONTROLSS_FSI_RX1	5029 1000h
CONTROLSS_FSI_RX2	502B 0000h
CONTROLSS_FSI_RX3	502B 1000h

Access Types Legend

Table 3-669. RX_MASTER_CTRL_ALTC_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	KEY	WO	0h	Write Key. In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every change to this register.
7 - 5	RESERVED	RO		Reserved
4	DATA_FILTER_EN	RW	0h	Data Filter Enable Bit. 0h (R/W) = Data filtering is disabled. 1h (R/W) = Data filtering is enabled.
3	INPUT_ISOLATE	RW	0h	When set to 1, the FSI RX inputs (RXCLK, RXD0 and RXD1) will be isolated from what is driven from the device pins and will be held at inactive level of '1'.This isolation facilitates the user to switch the RX inputs to a different set of device pins and hence any potential glitch that could occur during the process of switching will not affect the RX module itself.
2	SPI_PAIRING	RW	0h	Clock Pairing for SPI-like Behavior Enable bit This bit enables the internal clock pairing with the FSI TX module. This feature internally connects the TXCLK to RXCLK allowing the FSI TX module, acting as a SPI master, to clock data into the receiver and out of the transmitter like a standard SPI module. This configuration is valid when the Module is in SPI mode only (RX_OPER_CTRL.SPI_MODE = 1) 0h (R/W) = SPI clock pairing is not enabled. 1h (R/W) = SPI clock pairing is enabled. The RXCLK will be internally connected to the TXCLK of the corresponding FSI module. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.
1	INT_LOOPBACK	RW	0h	Internal Loopback Enable bit This bit enables the internal loopback functionality of the FSI receiver. By enabling this bit, a mux will select the signals coming directly from the corresponding FSI transmitter module rather than from the pins. 0h (R/W) = Internal loopback is disabled. The FSI RX module will receive signals coming from the pins. 1h (R/W) = Internal loopback is enabled. The FSI RX module will receive signals from the directly from FSI TX module rather than the pins. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.
0	CORE_RST	RW	0h	Receiver Master Core Reset bit This bit controls the receiver master core reset. In order to receive any frame, this bit must be cleared. Note: For reset to take affect, the FSI RX module must be held in reset for at least 4 SYSCLK cycles. 0h (R/W) = Receiver core is not in reset and can receive frames. 1h (R/W) = Receiver core is held in reset. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.

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3.11.3 CONTROLSS_FSI_RXn_RX_OPER_CTRL Registers

3.11.3.1 FSI_RXn_RX_OPER_CTRL Register (Offset = 8h) [reset = h]

Short Description: Receive operation control register

Long Description:

Return to Summary Table

Table 3-670. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0008h
CONTROLSS_FSI_RX1	5029 1008h
CONTROLSS_FSI_RX2	502B 0008h
CONTROLSS_FSI_RX3	502B 1008h

Access Types Legend

Table 3-671. RX_OPER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9	RESERVED	RO		Reserved
8	PING_WD_RST_MODE	RW	0h	Ping Watchdog Timeout Mode Select bit This bit selects the mode by which the ping watchdog counter is reset. The watchdog counter can be reset and restarted only by ping frames or by any received frame. 0h (R/W) = The ping watchdog counter will reset and restart only by ping frames. 1h (R/W) = The ping watchdog counter will reset and restart by any received frame.
7	ECC_SEL	RW	0h	ECC Data Width Select bit This bit selects between whether the ECC computation is done on 16-bit or 32-bit words. 0h (R/W) = 32-bit ECC is used. 1h (R/W) = 16-bit ECC is used.
6 - 3	N_WORDS	RW	0h	Number of Words to Receive This field defines the number of words which will be received in a DATA_N_WORD frame. This is a user-defined field that must match the corresponding field in the transmitter. Set this bitfield to be one less than the number of words to be received. This value is only applicable when the frame type received is DATA_N_WORD. 0h (R/W) = 1 data word frame (16-bit data). 1h (R/W) = 2 data word frame (32-bit data). .. Fh (R/W) = 16 data word frame (256-bit data).
2	SPI_MODE	RW	0h	SPI Mode Enable bit This bit enables and disables the SPI compatibility mode of the FSI RX. The received data must be formatted as an FSI frame in order for the data to properly be received. SPI compatibility mode will allow FSI RX to receive data that is sent using SPI signal format. Refer to the applicable section in the FSI TRM chapter for more information. 0h (R/W) = FSI is in normal mode of operation. 1h (R/W) = FSI is operating in SPI compatibility mode.
1 - 0	DATA_WIDTH	RW	0h	Receive Data Width Select bit These bits decide the number of data lines used for receiving data. 0h (R/W) = Data will be received on one data line, RXD0. 1h (R/W) = Data will be received on two data lines, RXD0 and RXD1. 2h, 3h (R/W) = Reserved

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3.11.4 CONTROLSS_FSI_RXn_RX_FRAME_INFO Registers

3.11.4.1 FSI_RXn_RX_FRAME_INFO Register (Offset = Ch) [reset = h]

Short Description: Receive frame control register

Long Description:

Return to Summary Table

Table 3-672. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 000Ch
CONTROLSS_FSI_RX1	5029 100Ch
CONTROLSS_FSI_RX2	502B 000Ch
CONTROLSS_FSI_RX3	502B 100Ch

Access Types Legend

Table 3-673. RX_FRAME_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3 - 0	FRAME_TYPE	RO	0h	Received Frame Type This field indicates the type of frame that was successfully received last. 0000b (R/W) = A ping frame was received 0100b (R/W) = A DATA_1_WORD frame was received (16-bit data). 0101b (R/W) = A DATA_2_WORD frame was received (32-bit data). 0110b (R/W) = A DATA_4_WORD frame was received (64-bit data). 0111b (R/W) = A DATA_6_WORD frame was received (96-bit data). 0011b (R/W) = A DATA_N_WORD frame was received. The N_WORD field will determine the number of words (1 to 16) to be sent. The number of words received must equal the value programmed in RX_OPER_CTRL.N_WORDS. 1111b (R/W) = An error frame was received. This frame can be used during error conditions or any condition where the transmitter wants to signal the receiver for attention. However, the user software is at liberty to use this for any purpose. 0001b, 0010b, and 1000b through 1110b are Reserved and should not be used.

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3.11.5 CONTROLSS_FSI_RXn_RX_FRAME_TAG_UDATA Registers

3.11.5.1 FSI_RXn_RX_FRAME_TAG_UDATA Register (Offset = Eh) [reset = h]

Short Description: Receive frame tag and user data register

Long Description:

Return to Summary Table

Table 3-674. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 000Eh
CONTROLSS_FSI_RX1	5029 100Eh
CONTROLSS_FSI_RX2	502B 000Eh
CONTROLSS_FSI_RX3	502B 100Eh

Access Types Legend

Table 3-675. RX_FRAME_TAG_UDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	USER_DATA	RO	0h	Received User Data This field contains the 8-bit user data field of the last successfully received frame.
7 - 5	RESERVED	RO		Reserved
4 - 1	FRAME_TAG	RO	0h	Received Frame Tag This field contains the 4-bit frame tag from the last successfully received frame. This is intentionally shifted into bits 4:1 so that the register can be used as a 32-bit address index based on the received tag.
0	RESERVED	RO		Zero bit This bit will always read as 0. This is intentionally provided to create a 32-bit offset if required. Using the FRAME_TAG and ZERO bits of this register (bits 4:0), application software can directly index into an array of 32-bit data.

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3.11.6 CONTROLSS_FSI_RXn_RX_DMA_CTRL Registers

3.11.6.1 FSI_RXn_RX_DMA_CTRL Register (Offset = 10h) [reset = h]

Short Description: Receive DMA event control register

Long Description:

Return to Summary Table

Table 3-676. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0010h
CONTROLSS_FSI_RX1	5029 1010h
CONTROLSS_FSI_RX2	502B 0010h
CONTROLSS_FSI_RX3	502B 1010h

Access Types Legend

Table 3-677. RX_DMA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 1	RESERVED	RO		Reserved
0	DMA_EVT_EN	RW	0h	DMA Event Enable bit This bit will enable a DMA Event to be generated upon the completion of a frame reception. 0h (R/W) = A DMA event will not be generated. 1h (R/W) = A DMA event will be generated upon the reception of a frame. Note: The DMA event will only be generated for data frames.

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3.11.7 CONTROLSS_FSI_RXn_RX_EVT_STS_ALT1_ Registers

3.11.7.1 FSI_RXn_RX_EVT_STS_ALT1_ Register (Offset = 14h) [reset = h]

Short Description: Receive event and error status flag register

Long Description:

Return to Summary Table

Table 3-678. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0014h
CONTROLSS_FSI_RX1	5029 1014h
CONTROLSS_FSI_RX2	502B 0014h
CONTROLSS_FSI_RX3	502B 1014h

Access Types Legend

Table 3-679. RX_EVT_STS_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	ERROR_TAG_MATCH	RO	0h	Error Tag Match Flag This bit indicates that an error frame was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No tag-matched error frame received. 1h (R) = A tag-matched error frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
13	DATA_TAG_MATCH	RO	0h	Data Tag Match Flag This bit indicates that a dataframe was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No tag-matched data frame received. 1h (R) = A tag-matched data frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
12	PING_TAG_MATCH	RO	0h	Ping Tag Match Flag This bit indicates that a ping frame was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No tag-matched ping frame received. 1h (R) = A tag-matched ping frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
11	DATA_FRAME	RO	0h	Data Frame Received Flag This bit indicates that an data frame has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No data frame has been received. 1h (R) = A data frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
10	FRAME_OVERRUN	RO	0h	Frame Overrun Flag This bit indicates that a frame overrun condition has occured. This bit gets set to 1 when a new DATA/ERROR frame is received and the corresponding DATA_FRAME_RCVD/ ERROR_FRAME_RCVD flag is still set to 1. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Frame overrun has not ocurred. 1h (R) = Frame overrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
9	PING_FRAME	RO	0h	Ping Frame Received Flag This bit indicates that an ping frame has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No ping frame has been received. 1h (R) = A ping frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.

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Table 3-679. RX_EVT_STS_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	ERR_FRAME	RO	0h	Error Frame Received Flag This bit indicates that an error frame has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No error frame has been received. 1h (R) = An error frame has been received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
7	BUF_UNDERRUN	RO	0h	Receive Buffer Underrun Flag This bit indicates that a buffer underrun condition has occured in the receive buffer. This will happen when software reads the buffer which is empty and has no valid data. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Receive Buffer Underrun has not ocurred. 1h (R) = Receive Buffer Underrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
6	FRAME_DONE	RO	0h	Frame Done Flag This bit indicates that a frame has been successfully received without error. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = No frame has been successfully received. 1h (R) = A frame has been successfully received. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
5	BUF_OVERRUN	RO	0h	Receive Buffer Overrun Flag This bit indicates that a buffer overrun condition has occured in the receive buffer. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Receive buffer overrun has not ocurred. 1h (R) = Receive buffer overrun has ocurred. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
4	EOF_ERR	RO	0h	End-of-Frame Error Flag This bit indicates that an invalid end-of-frame bit pattern has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Invalid end-of-frame has not been received. 1h (R) = Invalid end-of-frame has been received To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
3	TYPE_ERR	RO	0h	Frame Type Error Flag This bit inditcates that an invalid frame type has been received. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Invalid frame type has not been received. 1h (R) = Invalid frame type has been received To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
2	CRC_ERR	RO	0h	CRC Error Flag This bit indicates that a CRC error has occured. A CRC error will be generated on a data frame where the received CRC and the computed CRC do not match. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = CRC error has not occured. 1h (R) = CRC error has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
1	FRAME_WD_TO	RO	0h	Frame Watchdog Timeout Flag This bit indicates that the frame watchdog timer has timed out. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Frame watchdog timeout has not occured. 1h (R) = Frame watchdog timeout has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.
0	PING_WD_TO	RO	0h	Ping Watchdog Timeout Flag This bit indicates that the ping watchdog timer has timed out. Software can also force this bit to get set by writing to the RX_EVT_FRC register. 0h (R) = Ping watchdog timeout has not occured. 1h (R) = Ping watchdog timeout has occured. To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.

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3.11.8 CONTROLSS_FSI_RXn_RX_CRC_INFO Registers

3.11.8.1 FSI_RXn_RX_CRC_INFO Register (Offset = 16h) [reset = h]

Short Description: Receive CRC info of received and computed CRC

Long Description:

Return to Summary Table

Table 3-680. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0016h
CONTROLSS_FSI_RX1	5029 1016h
CONTROLSS_FSI_RX2	502B 0016h
CONTROLSS_FSI_RX3	502B 1016h

Access Types Legend

Table 3-681. RX_CRC_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	CALC_CRC	RO	0h	Harware Calculated CRC Value This bitfield contains the CRC value that was calculated on the last received data. The contents of this bitfield are valid only when data frames are received. Note: The contents of this bitfield are invalid for ping and error frames.
7 - 0	RX_CRC	RO	0h	Received CRC Value This bitfield contains the CRC value that was last received a frame. The contents of this bitfield are valid only when data frames are received. Note: The contents of this bitfield are invalid for ping and error frames.

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3.11.9 CONTROLSS_FSI_RXn_RX_EVT_CLR_ALT1_ Registers

3.11.9.1 FSI_RXn_RX_EVT_CLR_ALT1_ Register (Offset = 18h) [reset = h]

Short Description: Receive event and error clear register

Long Description:

Return to Summary Table

Table 3-682. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0018h
CONTROLSS_FSI_RX1	5029 1018h
CONTROLSS_FSI_RX2	502B 0018h
CONTROLSS_FSI_RX3	502B 1018h

Access Types Legend

Table 3-683. RX_EVT_CLR_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	ERROR_TAG_MATCH	WO	0h	Error Tag Match Glag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
13	DATA_TAG_MATCH	WO	0h	Data Tag Match Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
12	PING_TAG_MATCH	WO	0h	Ping Tag Match Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
11	DATA_FRAME	WO	0h	Data Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
10	FRAME_OVERRUN	WO	0h	Frame Overrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
9	PING_FRAME	WO	0h	Ping Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
8	ERR_FRAME	WO	0h	Error Frame Received Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
7	BUF_UNDERRUN	WO	0h	Receive Buffer Underrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (R/W) = Writing a 0 to this bit will have no effect. 1h (R/W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
6	FRAME_DONE	WO	0h	Frame Done Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.

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Table 3-683. RX_EVT_CLR_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	BUF_OVERRUN	WO	0h	Receive Buffer Overrun Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
4	EOF_ERR	WO	0h	End-of-Frame Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
3	TYPE_ERR	WO	0h	Frame Type Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
2	CRC_ERR	WO	0h	CRC Error Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
1	FRAME_WD_TO	WO	0h	Frame Watchdog Timeout Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.
0	PING_WD_TO	WO	0h	Ping Watchdog Timeout Flag Clear bit This bit clears the corresponding bit in the RX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.

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3.11.10 CONTROLSS_FSI_RXn_RX_EVT_FRC_ALT1_ Registers

3.11.10.1 FSI_RXn_RX_EVT_FRC_ALT1_ Register (Offset = 1Ah) [reset = h]

Short Description: Receive event and error flag force register

Long Description:

Return to Summary Table

Table 3-684. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 001Ah
CONTROLSS_FSI_RX1	5029 101Ah
CONTROLSS_FSI_RX2	502B 001Ah
CONTROLSS_FSI_RX3	502B 101Ah

Access Types Legend

Table 3-685. RX_EVT_FRC_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	ERROR_TAG_MATCH	WO	0h	Error Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
13	DATA_TAG_MATCH	WO	0h	Data Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
12	PING_TAG_MATCH	WO	0h	Ping Tag Match Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
11	DATA_FRAME	WO	0h	Data Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
10	FRAME_OVERRUN	WO	0h	Frame Overrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
9	PING_FRAME	WO	0h	Ping Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.

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Table 3-685. RX_EVT_FRC_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	ERR_FRAME	WO	0h	Error Frame Received Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
7	BUF_UNDERRUN	WO	0h	Receive Buffer Underrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
6	FRAME_DONE	WO	0h	Frame Done Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
5	BUF_OVERRUN	WO	0h	Receive Buffer Overrun Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
4	EOF_ERR	WO	0h	End-of-Frame Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
3	TYPE_ERR	WO	0h	Frame Type Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
2	CRC_ERR	WO	0h	CRC Error Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
1	FRAME_WD_TO	WO	0h	Frame Watchdog Timeout Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.
0	PING_WD_TO	WO	0h	Ping Watchdog Timeout Flag Force bit This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding bit in the RX_EVT_STS Register.

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3.11.11 CONTROLSS_FSI_RXn_RX_BUF_PTR_LOAD Registers

3.11.11.1 FSI_RXn_RX_BUF_PTR_LOAD Register (Offset = 1Ch) [reset = h]

Short Description: Receive buffer pointer load register

Long Description:

Return to Summary Table

Table 3-686. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 001Ch
CONTROLSS_FSI_RX1	5029 101Ch
CONTROLSS_FSI_RX2	502B 001Ch
CONTROLSS_FSI_RX3	502B 101Ch

Access Types Legend

Table 3-687. RX_BUF_PTR_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3 - 0	BUF_PTR_LOAD	RW	0h	Buffer Pointer Load. This is the value to be loaded into the receive word pointer when written. This is to allow software to force the receiver to start storing the received data starting at a specific location in the buffer. NOTE: The value of the CURR_BUF_PTR in the RX_BUF_PTR_STS will not get reflected immediately. This will take effect only when there is a valid receive operation with incoming clocks after (3 RXCLK + 3 SYCLK) cycles.

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3.11.12 CONTROLSS_FSI_RXn_RX_BUF_PTR_STS Registers

3.11.12.1 FSI_RXn_RX_BUF_PTR_STS Register (Offset = 1Eh) [reset = h]

Short Description: Receive buffer pointer status register

Long Description:

Return to Summary Table

Table 3-688. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 001Eh
CONTROLSS_FSI_RX1	5029 101Eh
CONTROLSS_FSI_RX2	502B 001Eh
CONTROLSS_FSI_RX3	502B 101Eh

Access Types Legend

Table 3-689. RX_BUF_PTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12 - 8	CURR_WORD_CNT	RO	0h	Words Available in the Receive Buffer This bitfield indicates the number of valid data words present in the receive buffer that have not been read by the application software. This bitfield is only valid when there is no active transfer. Note: This value will not be valid if there has been a buffer overrun or underrun condition.
7 - 4	RESERVED	RO		Reserved
3 - 0	CURR_BUF_PTR	RO	0h	Current Buffer Pointer Index This bitfield will show the current index of the buffer pointer. This value is only valid when there is no active transmission.

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3.11.13 CONTROLSS_FSI_RXn_RX_FRAME_WD_CTRL Registers

3.11.13.1 FSI_RXn_RX_FRAME_WD_CTRL Register (Offset = 20h) [reset = h]

Short Description: Receive frame watchdog control register

Long Description:

Return to Summary Table

Table 3-690. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0020h
CONTROLSS_FSI_RX1	5029 1020h
CONTROLSS_FSI_RX2	502B 0020h
CONTROLSS_FSI_RX3	502B 1020h

Access Types Legend

Table 3-691. RX_FRAME_WD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 2	RESERVED	RO		Reserved
1	FRAME_WD_EN	RW	0h	Frame Watchdog Counter Enable bit This bit will enable or disable the frame watchdog counter. The counter (RX_FRAME_WD_CNT) will begin counting from 0 when a valid start-of-frame pattern is received. When the reference value (RX_FRAME_WD_REF) is reached, it will generate a frame watchdog timeout event (RX_EVT_STS.FRAME_WD_TO) and the counter value will reset to 0 and continue counting on the next valid start-of-frame. 0h (R/W) = The frame watchdog counter is disabled and not running. 1h (R/W) = The frame watchdog counter logic is enabled and running.
0	FRAME_WD_CNT_RST	RW	0h	Frame Watchdog Counter Reset bit This bit will reset the frame watchdog counter to 0. Writing a 1 to this bit will reset the frame watchdog counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter 0h (R/W) = Clear the FRAME_WD_CNT_RST. 1h (W) = The frame watchdog counter will be reset to 0.

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3.11.14 CONTROLSS_FSI_RXn_RX_FRAME_WD_REF Registers

3.11.14.1 FSI_RXn_RX_FRAME_WD_REF Register (Offset = 24h) [reset = h]

Short Description: Receive frame watchdog counter reference

Long Description:

Return to Summary Table

Table 3-692. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0024h
CONTROLSS_FSI_RX1	5029 1024h
CONTROLSS_FSI_RX2	502B 0024h
CONTROLSS_FSI_RX3	502B 1024h

Access Types Legend

Table 3-693. RX_FRAME_WD_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FRAME_WD_REF	RW	0h	Frame Watchdog Counter Reference Value This is the 32-bit reference value for the frame watchdog timeout counter. The counter will count up starting from 0 at a valid start-of-frame pattern and continue counting until this value is reached.

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3.11.15 CONTROLSS_FSI_RXn_RX_FRAME_WD_CNT Registers

3.11.15.1 FSI_RXn_RX_FRAME_WD_CNT Register (Offset = 28h) [reset = h]

Short Description: Receive frame watchdog current count

Long Description:

Return to Summary Table

Table 3-694. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0028h
CONTROLSS_FSI_RX1	5029 1028h
CONTROLSS_FSI_RX2	502B 0028h
CONTROLSS_FSI_RX3	502B 1028h

Access Types Legend

Table 3-695. RX_FRAME_WD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FRAME_WD_CNT	RO	0h	Frame Watchdog Counter Value This is the 32-bit read-only register which shows the current value of the frame watchdog counter. This counter is reset to 0 in a variety of ways: A write to FRME_WD_CNT_RST, a match with FRAME_WD_REF, or the reception of a successful data frame.

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3.11.16 CONTROLSS_FSI_RXn_RX_PING_WD_CTRL Registers

3.11.16.1 FSI_RXn_RX_PING_WD_CTRL Register (Offset = 2Ch) [reset = h]

Short Description: Receive ping watchdog control register

Long Description:

Return to Summary Table

Table 3-696. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 002Ch
CONTROLSS_FSI_RX1	5029 102Ch
CONTROLSS_FSI_RX2	502B 002Ch
CONTROLSS_FSI_RX3	502B 102Ch

Access Types Legend

Table 3-697. RX_PING_WD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 2	RESERVED	RO		Reserved
1	PING_WD_EN	RW	0h	Ping Watchdog Counter Enable bit This bit will enable or disable the ping watchdog counter. The counter (RX_PING_WD_CNT) will begin counting from 0 when it is enabled. When the reference value (RX_PING_WD_REF) is reached, it will generate a ping watchdog timeout event (RX_EVT_STS.PING_WD_TO) and the counter value will reset to 0, and resume counting 0h (R/W) = The ping watchdog counter is disabled and not running. 1h (R/W) = The ping watchdog counter logic is enabled and running.
0	PING_WD_RST	RW	0h	Ping Watchdog Counter Reset bit This bit will reset the ping watchdog counter to 0. Writing a 1 to this bit will reset the ping watchdog counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter 0h (R/W) = Clear the PING_WD_RST. 1h (W) = The ping watchdog counter will be reset to 0.

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3.11.17 CONTROLSS_FSI_RXn_RX_PING_TAG Registers

3.11.17.1 FSI_RXn_RX_PING_TAG Register (Offset = 2Eh) [reset = h]

Short Description: Receive ping tag register

Long Description:

Return to Summary Table

Table 3-698. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 002Eh
CONTROLSS_FSI_RX1	5029 102Eh
CONTROLSS_FSI_RX2	502B 002Eh
CONTROLSS_FSI_RX3	502B 102Eh

Access Types Legend

Table 3-699. RX_PING_TAG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 5	RESERVED	RO		Reserved
4 - 1	PING_TAG	RO	0h	Received Ping Frame Tag This field contains the 4-bit frame tag from the last successfully received ping frame. This is intentionally shifted into bits 4:1 so that the register can be used as a 32-bit address index based on the received tag.
0	RESERVED	RO		Zero bit This bit will always read as 0. This is intentionally provided to create a 32-bit offset if required. Using the PING_TAG and ZERO bits of this register (bits 4:0), application software can directly index into an array of 32-bit data.

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3.11.18 CONTROLSS_FSI_RXn_RX_PING_WD_REF Registers

3.11.18.1 FSI_RXn_RX_PING_WD_REF Register (Offset = 30h) [reset = h]

Short Description: Receive ping watchdog counter reference

Long Description:

Return to Summary Table

Table 3-700. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0030h
CONTROLSS_FSI_RX1	5029 1030h
CONTROLSS_FSI_RX2	502B 0030h
CONTROLSS_FSI_RX3	502B 1030h

Access Types Legend

Table 3-701. RX_PING_WD_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PING_WD_REF	RW	0h	Ping Watchdog Counter Reference Value This is the 32-bit reference value for the ping watchdog timeout counter. The counter will count up starting from 0 and continue counting until this value is reached.

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3.11.19 CONTROLSS_FSI_RXn_RX_PING_WD_CNT Registers

3.11.19.1 FSI_RXn_RX_PING_WD_CNT Register (Offset = 34h) [reset = h]

Short Description: Receive pingwatchdog current count

Long Description:

Return to Summary Table

Table 3-702. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0034h
CONTROLSS_FSI_RX1	5029 1034h
CONTROLSS_FSI_RX2	502B 0034h
CONTROLSS_FSI_RX3	502B 1034h

Access Types Legend

Table 3-703. RX_PING_WD_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PING_WD_CNT	RO	0h	Ping Watchdog Counter Value This is the 32-bit read-only register which shows the current value of the ping watchdog counter. This counter is reset to 0 in a variety of ways: A write to PING_WD_RST, a match with PING_WD_REF, or the reception of a ping frame.

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3.11.20 CONTROLSS_FSI_RXn_RX_INT1_CTRL_ALT1_ Registers

3.11.20.1 FSI_RXn_RX_INT1_CTRL_ALT1_ Register (Offset = 38h) [reset = h]

Short Description: Receive interrupt control register for RX_INT1

Long Description:

Return to Summary Table

Table 3-704. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0038h
CONTROLSS_FSI_RX1	5029 1038h
CONTROLSS_FSI_RX2	502B 0038h
CONTROLSS_FSI_RX3	502B 1038h

Access Types Legend

Table 3-705. RX_INT1_CTRL_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	INT1_EN_ERROR_TAG_MATCH	RW	0h	Enable Error Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = An error frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
13	INT1_EN_DATA_TAG_MATCH	RW	0h	Enable Data Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A data frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
12	INT1_EN_PING_TAG_MATCH	RW	0h	Enable Ping Frame Received with Tag Match Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A ping frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
11	INT1_EN_DATA_FRAME	RW	0h	Enable Data Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A data frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
10	INT1_EN_FRAME_OVERRUN	RW	0h	Enable Frame Overrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A frame overrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
9	INT1_EN_PING_FRAME	RW	0h	Enable Ping Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A ping frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register

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Table 3-705. RX_INT1_CTRL_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT1_EN_ERR_FRAME	RW	0h	Enable ERROR Frame Received Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A error frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
7	INT1_EN_UNDERRUN	RW	0h	Enable Buffer Underrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A buffer underrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
6	INT1_EN_FRAME_DONE	RW	0h	Enable Frame Done Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A frame done event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
5	INT1_EN_OVERRUN	RW	0h	Enable Receive Buffer Overrun Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A receive buffer overrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
4	INT1_EN_EOF_ERR	RW	0h	Enable End-of-Frame Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = An end-of-frame error event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
3	INT1_EN_TYPE_ERR	RW	0h	Enable Frame Type Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A frame type error event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
2	INT1_EN_CRC_ERR	RW	0h	Enable CRC Error Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A CRC error will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
1	INT1_EN_FRAME_WD_TO	RW	0h	Enable Frame Watchdog Timeout Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A frame watchdog timeout event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
0	INT1_EN_PING_WD_TO	RW	0h	Enable Ping Watchdog Timeout Interrupt to INT1 bit This is an enable register which decides whether an interrupt (RX_INT1) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT1. 1h (R/W) = A ping watchdog timeout event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register

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3.11.21 CONTROLSS_FSI_RXn_RX_INT2_CTRL_ALT1_ Registers

3.11.21.1 FSI_RXn_RX_INT2_CTRL_ALT1_ Register (Offset = 3Ah) [reset = h]

Short Description: Receive interrupt control register for RX_INT2

Long Description:

Return to Summary Table

Table 3-706. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 003Ah
CONTROLSS_FSI_RX1	5029 103Ah
CONTROLSS_FSI_RX2	502B 003Ah
CONTROLSS_FSI_RX3	502B 103Ah

Access Types Legend

Table 3-707. RX_INT2_CTRL_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	INT2_EN_ERROR_TAG_MATCH	RW	0h	Enable Error Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = An error frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
13	INT2_EN_DATA_TAG_MATCH	RW	0h	Enable Data Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A data frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
12	INT2_EN_PING_TAG_MATCH	RW	0h	Enable Ping Frame Received with Tag Match Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A ping frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
11	INT2_EN_DATA_FRAME	RW	0h	Enable Data Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A data frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
10	INT2_EN_FRAME_OVERRUN	RW	0h	Enable Frame Overrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A frame overrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
9	INT2_EN_PING_FRAME	RW	0h	Enable Ping Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A ping frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register

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Table 3-707. RX_INT2_CTRL_ALT1_ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	INT2_EN_ERR_FRAME	RW	0h	Enable Error Frame Received Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A error frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
7	INT2_EN_UNDERRUN	RW	0h	Enable Buffer Underrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A buffer underrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
6	INT2_EN_FRAME_DONE	RW	0h	Enable Frame Done Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A frame done event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
5	INT2_EN_OVERRUN	RW	0h	Enable Buffer Overrun Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A buffer overrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
4	INT2_EN_EOF_ERR	RW	0h	Enable End-of-Frame Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = An end-of-frame error event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
3	INT2_EN_TYPE_ERR	RW	0h	Enable Frame Type Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A frame type error event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
2	INT2_EN_CRC_ERR	RW	0h	Enable CRC Error Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A CRC error will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
1	INT2_EN_FRAME_WD_TO	RW	0h	Enable Frame Watchdog Timeout Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A frame watchdog timeout event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register
0	INT2_EN_PING_WD_TO	RW	0h	Enable Ping Watchdog Timeout Interrupt to INT2 bit This is an enable register which decides whether an interrupt (RX_INT2) will be generated on the enabled event. 0h (R/W) = This event will not trigger an interrupt on RX_INT2. 1h (R/W) = A ping watchdog timeout event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register

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3.11.22 CONTROLSS_FSI_RXn_RX_LOCK_CTRL Registers

3.11.22.1 FSI_RXn_RX_LOCK_CTRL Register (Offset = 3Ch) [reset = h]

Short Description: Receive lock control register

Long Description:

Return to Summary Table

Table 3-708. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 003Ch
CONTROLSS_FSI_RX1	5029 103Ch
CONTROLSS_FSI_RX2	502B 003Ch
CONTROLSS_FSI_RX3	502B 103Ch

Access Types Legend

Table 3-709. RX_LOCK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	KEY	WO	0h	Write Key. In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every change to this register.
7 - 1	RESERVED	RO		Reserved
0	LOCK	RW	0h	Control Register Lock Enable bit This bit locks the contents of all the receive control registers that support a lock protection. Once locked, further writes will not take effect until SYSRS unlocks the register. Once set, further writes even to this bit will be ignored. 0h (R/W) = Receive control registers can be modified and are not locked. 1h (R/W) = Receive control registers are locked and cannot be modified until this bit is cleared by SYSRS. Any further writes to this bit are ignored. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.

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3.11.23 CONTROLSS_FSI_RXn_RX_ECC_DATA Registers

3.11.23.1 FSI_RXn_RX_ECC_DATA Register (Offset = 40h) [reset = h]

Short Description: Receive ECC data register

Long Description:

Return to Summary Table

Table 3-710. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0040h
CONTROLSS_FSI_RX1	5029 1040h
CONTROLSS_FSI_RX2	502B 0040h
CONTROLSS_FSI_RX3	502B 1040h

Access Types Legend

Table 3-711. RX_ECC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA_HIGH	RW	0h	Upper 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC(SEC-DED) the entire 32-bit register and update TX_ECC_VAL register with the results. Software should write to these 16 bits of the register in a 32-bit write when needing to compute ECC for 32-bits for the full TX_ECC_DATA register.
15 - 0	DATA_LOW	RW	0h	Lower 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC(SEC-DED) for these 16 bits and update the TX_ECC_VAL register with the results. Software should write to these register bits as a 16-bit write when needing to compute ECC for 16-bits.

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3.11.24 CONTROLSS_FSI_RXn_RX_ECC_VAL Registers

3.11.24.1 FSI_RXn_RX_ECC_VAL Register (Offset = 44h) [reset = h]

Short Description: Receive ECC value register

Long Description:

Return to Summary Table

Table 3-712. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0044h
CONTROLSS_FSI_RX1	5029 1044h
CONTROLSS_FSI_RX2	502B 0044h
CONTROLSS_FSI_RX3	502B 1044h

Access Types Legend

Table 3-713. RX_ECC_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 7	RESERVED	RO		Reserved
6 - 0	ECC_VAL	RW	0h	ECC Value for SEC-DED check This field contains the ECC value to be used for SEC-DED either for 16-bit or 32-bit data in the RX_ECC_DATA register.

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3.11.25 CONTROLSS_FSI_RXn_RX_ECC_SEC_DATA Registers

3.11.25.1 FSI_RXn_RX_ECC_SEC_DATA Register (Offset = 48h) [reset = h]

Short Description: Receive ECC corrected data register

Long Description:

Return to Summary Table

Table 3-714. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0048h
CONTROLSS_FSI_RX1	5029 1048h
CONTROLSS_FSI_RX2	502B 0048h
CONTROLSS_FSI_RX3	502B 1048h

Access Types Legend

Table 3-715. RX_ECC_SEC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEC_DATA	RO	0h	ECC Single Error Corrected Data The ECC corrected data will be available in this register. This value is valid only when there are no bit errors, or a single bit error was detected. Otherwise, the contents of this register are invalid and should not be used.

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3.11.26 CONTROLSS_FSI_RXn_RX_ECC_LOG Registers

3.11.26.1 FSI_RXn_RX_ECC_LOG Register (Offset = 4Ch) [reset = h]

Short Description: Receive ECC log and status register

Long Description:

Return to Summary Table

Table 3-716. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 004Ch
CONTROLSS_FSI_RX1	5029 104Ch
CONTROLSS_FSI_RX2	502B 004Ch
CONTROLSS_FSI_RX3	502B 104Ch

Access Types Legend

Table 3-717. RX_ECC_LOG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 2	RESERVED	RO		Reserved
1	MBE	RO	1h	Multiple Bit Errors Detected This bit indicates the occurrence of multiple bit errors.The data is corrupted and cannot be corrected. If this bit is set, the data present in RX_ECC_SEC_DATA is invalid and should not be used. 0h (R) Multiple Bit Errors were not detected. Check the SBE bit for single bit errors. 1h (R) Multiple Bit Errors were detected. The data is not able to be corrected. The value present in RX_ECC_SEC_DATA is invalid and should not be used.
0	SBE	RO	1h	Single Bit Error Detected This bit indicates the occurrence of a single bit error in the data. The data is autocorrected and placed into the RX_ECC_SEC_DATA register. This bit is valid only if MBE is 0. 0h (R) No bit errors were detected. The value in RX_ECC_SEC_DATA is correct. 1h (R) A single bit error was detected and corrected. The corrected data is present in RX_ECC_SEC_DATA.

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3.11.27 CONTROLSS_FSI_RXn_RX_FRAME_TAG_CMP Registers

3.11.27.1 FSI_RXn_RX_FRAME_TAG_CMP Register (Offset = 50h) [reset = h]

Short Description: Receive frame tag compare register

Long Description:

Return to Summary Table

Table 3-718. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0050h
CONTROLSS_FSI_RX1	5029 1050h
CONTROLSS_FSI_RX2	502B 0050h
CONTROLSS_FSI_RX3	502B 1050h

Access Types Legend

Table 3-719. RX_FRAME_TAG_CMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9	BROADCAST_EN	RW	0h	Broadcast Enable bit This will enable the reception of a ping frame broadcast. When this bit is set, bit 3 of the received tag will be treated as a broadcast notification. If bit 3 of the received tag is set to 1, a ping tag match event will be triggered regardless of the. A match caused by the comparison of TAG_MASK and TAG_REF will still be considered a match and the frame tag match event will be triggered as normal This bit only takes effect only if CMP_EN is set to 1. 0h (R/W) Broadcast frame match disabled. 1h (R/W) Broadcast frame match enabled.
8	CMP_EN	RW	0h	Frame Tag Compare Enable bit Set this bit to enable the comparison of an incoming frame tag and the value stored in the frame tag reference. A match caused by the comparison of TAG_MASK, TAG_REF, and the incoming frame tag will trigger the apprpriate frame tag match event. 0h (R/W) Frame tag comparison is disabled. 1h (R/W) Frame tag comparison is enabled.
7 - 4	TAG_MASK	RW	0h	Frame Tag Mask Any bit position in this register set to 0 will be used in the comparison of the incoming frame tag and the value stored in TAG_REF. A bit position set to 1 will be ignored in the tag comparison. This mask value is used only for non-ping frames.
3 - 0	TAG_REF	RW	0h	Frame Tag Reference The reference tag to check against when comparing the TAG_MASK and the incoming frame tag. This reference value is used only for non-ping frames.

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3.11.28 CONTROLSS_FSI_RXn_RX_PING_TAG_CMP Registers

3.11.28.1 FSI_RXn_RX_PING_TAG_CMP Register (Offset = 52h) [reset = h]

Short Description: Receive ping tag compare register

Long Description:

Return to Summary Table

Table 3-720. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0052h
CONTROLSS_FSI_RX1	5029 1052h
CONTROLSS_FSI_RX2	502B 0052h
CONTROLSS_FSI_RX3	502B 1052h

Access Types Legend

Table 3-721. RX_PING_TAG_CMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9	BROADCAST_EN	RW	0h	Broadcast Enable bit This will enable the reception of a ping frame broadcast. When this bit is set, bit 3 of the received tag will be treated as a broadcast notification. If bit 3 of the received tag is set to 1, a ping tag match event will be triggered regardless of the. A match caused by the comparison of TAG_MASK and TAG_REF will still be considered a match and the ping tag match event will be triggered as normal This bit only takes effect only if CMP_EN is set to 1. 0h (R/W) Broadcast frame match disabled. 1h (R/W) Broadcast frame match enabled.
8	CMP_EN	RW	0h	Ping Tag Compare Enable bit Set this bit to enable the comparison of an incoming ping tag and the value stored in the ping tag reference. A match caused by the comparison of TAG_MASK, TAG_REF, and the incoming ping tag will trigger a ping frame tag match event. 0h (R/W) Ping tag comparison is disabled. 1h (R/W) Ping tag comparison is enabled.
7 - 4	TAG_MASK	RW	0h	Ping Tag Mask Any bit position in this register set to 0 will be used in the comparison of the incoming ping frame tag and the value stored in TAG_REF. A bit position set to 1 will be ignored in the tag comparison. This mask value is used only for ping frames.
3 - 0	TAG_REF	RW	0h	Ping Tag Reference The reference tag to check against when comparing the TAG_MASK and the incoming ping tag. This reference value is used only for ping frames.

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3.11.29 CONTROLSS_FSI_RXn_RX_TRIG_CTRL_0 Registers

3.11.29.1 FSI_RXn_RX_TRIG_CTRL_0 Register (Offset = 58h) [reset = h]

Short Description: Receive Trigger Control register 0

Long Description:

Return to Summary Table

Table 3-722. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0058h
CONTROLSS_FSI_RX1	5029 1058h
CONTROLSS_FSI_RX2	502B 0058h
CONTROLSS_FSI_RX3	502B 1058h

Access Types Legend

Table 3-723. RX_TRIG_CTRL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RX_TRIG_DLY	RW	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value.
7 - 5	RESERVED	RO		Reserved
4 - 1	TRIG_SEL	RW	0h	This is the mux select value which selects which of the inputs will be used as the trigger source.
0	TRIG_EN	RW	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module.

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3.11.30 CONTROLSS_FSI_RXn_RX_TRIG_WIDTH_0 Registers

3.11.30.1 FSI_RXn_RX_TRIG_WIDTH_0 Register (Offset = 5Ch) [reset = h]

Short Description: Receive Trigger Wdith register 0

Long Description:

Return to Summary Table

Table 3-724. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 005Ch
CONTROLSS_FSI_RX1	5029 105Ch
CONTROLSS_FSI_RX2	502B 005Ch
CONTROLSS_FSI_RX3	502B 105Ch

Access Types Legend

Table 3-725. RX_TRIG_WIDTH_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO		Reserved
15 - 0	RX_TRIG_WIDTH	RW	0h	This register decides the width(in SYSCLK cycles) of wide pulse output of the RX trigger module.

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3.11.31 CONTROLSS_FSI_RXn_RX_DLYLINE_CTRL Registers

3.11.31.1 FSI_RXn_RX_DLYLINE_CTRL Register (Offset = 60h) [reset = h]

Short Description: Receive delay line control register

Long Description:

Return to Summary Table

Table 3-726. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0060h
CONTROLSS_FSI_RX1	5029 1060h
CONTROLSS_FSI_RX2	502B 0060h
CONTROLSS_FSI_RX3	502B 1060h

Access Types Legend

Table 3-727. RX_DLYLINE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14 - 10	RXD1_DLY	RW	0h	Delay Line Tap Select for RXD1 This bitfield selects the number of delay elements inserted into the RXD1 path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the RXD1 path. RXD1 is taken directly from the pin. 1h (R/W) One delay element is included in the RXD1 path. 2h (R/W) Two delay elements are included in the RXD1 path. ... 1Fh (R/W) 31 delay elements are included in the RXD1 path, the maximum.
9 - 5	RXD0_DLY	RW	0h	Delay Line Tap Select for RXD0 This bitfield selects the number of delay elements inserted into the RXD0 path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the RXD0 path. RXD0 is taken directly from the pin. 1h (R/W) One delay element is included in the RXD0 path. 2h (R/W) Two delay elements are included in the RXD0 path. ... 1Fh (R/W) 31 delay elements are included in the RXD0 path, the maximum.
4 - 0	RXCLK_DLY	RW	0h	Delay Line Tap Select for RXCLK This bitfield selects the number of delay elements inserted into the RXCLK path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the RXCLK path. RXCLK is taken directly from the pin. 1h (R/W) One delay element is included in the RXCLK path. 2h (R/W) Two delay elements are included in the RXCLK path. ... 1Fh (R/W) 31 delay elements are included in the RXCLK path, the maximum.

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3.11.32 CONTROLSS_FSI_RXn_RX_TRIG_CTRL_1 Registers

3.11.32.1 FSI_RXn_RX_TRIG_CTRL_1 Register (Offset = 64h) [reset = h]

Short Description: Receive Trigger Control register 1

Long Description:

Return to Summary Table

Table 3-728. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0064h
CONTROLSS_FSI_RX1	5029 1064h
CONTROLSS_FSI_RX2	502B 0064h
CONTROLSS_FSI_RX3	502B 1064h

Access Types Legend

Table 3-729. RX_TRIG_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RX_TRIG_DLY	RW	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value.
7 - 5	RESERVED	RO		Reserved
4 - 1	TRIG_SEL	RW	0h	This is the mux select value which selects which of the inputs will be used as the trigger source.
0	TRIG_EN	RW	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module.

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3.11.33 CONTROLSS_FSI_RXn_RX_TRIG_CTRL_2 Registers

3.11.33.1 FSI_RXn_RX_TRIG_CTRL_2 Register (Offset = 68h) [reset = h]

Short Description: Receive Trigger Control register 2

Long Description:

Return to Summary Table

Table 3-730. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0068h
CONTROLSS_FSI_RX1	5029 1068h
CONTROLSS_FSI_RX2	502B 0068h
CONTROLSS_FSI_RX3	502B 1068h

Access Types Legend

Table 3-731. RX_TRIG_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RX_TRIG_DLY	RW	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value.
7 - 5	RESERVED	RO		Reserved
4 - 1	TRIG_SEL	RW	0h	This is the mux select value which selects which of the inputs will be used as the trigger source.
0	TRIG_EN	RW	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module.

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3.11.34 CONTROLSS_FSI_RXn_RX_TRIG_CTRL_3 Registers

3.11.34.1 FSI_RXn_RX_TRIG_CTRL_3 Register (Offset = 6Ch) [reset = h]

Short Description: Receive Trigger Control register 3

Long Description:

Return to Summary Table

Table 3-732. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 006Ch
CONTROLSS_FSI_RX1	5029 106Ch
CONTROLSS_FSI_RX2	502B 006Ch
CONTROLSS_FSI_RX3	502B 106Ch

Access Types Legend

Table 3-733. RX_TRIG_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RX_TRIG_DLY	RW	0h	This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value.
7 - 5	RESERVED	RO		Reserved
4 - 1	TRIG_SEL	RW	0h	This is the mux select value which selects which of the inputs will be used as the trigger source.
0	TRIG_EN	RW	0h	This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module.

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3.11.35 CONTROLSS_FSI_RXn_RX_VIS_1 Registers

3.11.35.1 FSI_RXn_RX_VIS_1 Register (Offset = 70h) [reset = h]

Short Description: Receive debug visibility register 1

Long Description:

Return to Summary Table

Table 3-734. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0070h
CONTROLSS_FSI_RX1	5029 1070h
CONTROLSS_FSI_RX2	502B 0070h
CONTROLSS_FSI_RX3	502B 1070h

Access Types Legend

Table 3-735. RX_VIS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RESERVED	RO		Reserved
3	RX_CORE_STS	RO	0h	Receiver Core Status bit This bit indicates the status of the receiver core. If this bit is set, the receiver should undergo a reset and subsequent resynchronization with the transmitter. This bit will be always be set when the receiver has detected and end of frame error or a frame type error. This bit can also be set if the receiver becomes corrupted due to noise on the signal lines. If the receiver has experienced a ping watchdog or frame watchdog timeout, this bit should be read to determine if the cause was due to a corrupt transaction, thus putting the receiver core into an unrecoverable state. Only a soft reset will reset the recevier core and thus reset this bit. 0h (R) The receiver core is operating normally. 1h (R) The receiver core has entered into an error state and should be reset.
2 - 0	RESERVED	RO		Reserved

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3.11.36 CONTROLSS_FSI_RXn_RX_UDATA_FILTER Registers

3.11.36.1 FSI_RXn_RX_UDATA_FILTER Register (Offset = 74h) [reset = h]

Short Description: Receive User Data Filter Control register

Long Description:

Return to Summary Table

Table 3-736. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0074h
CONTROLSS_FSI_RX1	5029 1074h
CONTROLSS_FSI_RX2	502B 0074h
CONTROLSS_FSI_RX3	502B 1074h

Access Types Legend

Table 3-737. RX_UDATA_FILTER Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	UDATA_MASK	RW	0h	Bit Mask to be used for comparing the USERDATA field when filtering is enabled. Every bit that is '1' in this register will be masked for comparison. If a bit position is '1', then it will be considered a successful match for that bit position.
7 - 0	UDATA_REG	RW	0h	Reference to be used for comparing the USERDATA field when filtering is enabled.

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3.11.37 CONTROLSS_FSI_RXn_RX_BUF_BASE Registers

3.11.37.1 FSI_RXn_RX_BUF_BASE Register (Offset = 80h) [reset = h]

Short Description: Base address for receive data buffer

Long Description:

Return to Summary Table

Table 3-738. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_RX0	5029 0080h
CONTROLSS_FSI_RX1	5029 1080h
CONTROLSS_FSI_RX2	502B 0080h
CONTROLSS_FSI_RX3	502B 1080h

Access Types Legend

Table 3-739. RX_BUF_BASE Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BASE_ADDRESS	RO	0h	Receive Data Buffer Base Address This is the base address of the 16-word data buffer used by the receiver.

3.11.38 Access Table

Table 3-740. Access Type Codes

Access Type	Code	Description
WO	WO	Write
RO	RO	Read
RW	RW	Read / Write

3.12 FSI_TX Registers

Table 3-741. CONTROLSS_FSI_TX[0:1] Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_FSI_TX0 Physical Address	CONTROLSS_FSI_TX1 Physical Address
0h	16	FSI_TX_TX_MASTER_CTRL	5028 0000h	5028 1000h
4h	16	FSI_TX_TX_CLK_CTRL	5028 0004h	5028 1004h
8h	16	FSI_TX_TX_OPER_CTRL_LO_ALT2_	5028 0008h	5028 1008h
Ah	16	FSI_TX_TX_OPER_CTRL_HI_ALT1_	5028 000Ah	5028 100Ah
Ch	16	FSI_TX_TX_FRAME_CTRL	5028 000Ch	5028 100Ch
Eh	16	FSI_TX_TX_FRAME_TAG_UDATA	5028 000Eh	5028 100Eh
10h	16	FSI_TX_TX_BUF_PTR_LOAD	5028 0010h	5028 1010h
12h	16	FSI_TX_TX_BUF_PTR_STS	5028 0012h	5028 1012h
14h	16	FSI_TX_TX_PING_CTRL_ALT1_	5028 0014h	5028 1014h
16h	16	FSI_TX_TX_PING_TAG	5028 0016h	5028 1016h
18h	32	FSI_TX_TX_PING_TO_REF	5028 0018h	5028 1018h
1Ch	32	FSI_TX_TX_PING_TO_CNT	5028 001Ch	5028 101Ch
20h	16	FSI_TX_TX_INT_CTRL	5028 0020h	5028 1020h
22h	16	FSI_TX_TX_DMA_CTRL	5028 0022h	5028 1022h
24h	16	FSI_TX_TX_LOCK_CTRL	5028 0024h	5028 1024h
28h	16	FSI_TX_TX_EVT_STS	5028 0028h	5028 1028h
2Ch	16	FSI_TX_TX_EVT_CLR	5028 002Ch	5028 102Ch

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Table 3-741. CONTROLSS_FSI_TX[0:1] Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_FSI_TX0 Physical Address	CONTROLSS_FSI_TX1 Physical Address
2Eh	16	FSI_TX_TX_EVT_FRC	5028 002Eh	5028 102Eh
30h	16	FSI_TX_TX_USER_CRC	5028 0030h	5028 1030h
40h	32	FSI_TX_TX_ECC_DATA	5028 0040h	5028 1040h
44h	16	FSI_TX_TX_ECC_VAL	5028 0044h	5028 1044h
48h	16	FSI_TX_TX_DLYLINE_CTRL	5028 0048h	5028 1048h
80h	16	FSI_TX_TX_BUF_BASE	5028 0080h	5028 1080h

Table 3-742. CONTROLSS_FSI_TX[2:3] Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_FSI_TX2 Physical Address	CONTROLSS_FSI_TX3 Physical Address
0h	16	FSI_TX_TX_MASTER_CTRL	502A 0000h	502A 1000h
4h	16	FSI_TX_TX_CLK_CTRL	502A 0004h	502A 1004h
8h	16	FSI_TX_TX_OPER_CTRL_LO_ALT2_	502A 0008h	502A 1008h
Ah	16	FSI_TX_TX_OPER_CTRL_HI_ALT1_	502A 000Ah	502A 100Ah
Ch	16	FSI_TX_TX_FRAME_CTRL	502A 000Ch	502A 100Ch
Eh	16	FSI_TX_TX_FRAME_TAG_UDATA	502A 000Eh	502A 100Eh
10h	16	FSI_TX_TX_BUF_PTR_LOAD	502A 0010h	502A 1010h
12h	16	FSI_TX_TX_BUF_PTR_STS	502A 0012h	502A 1012h
14h	16	FSI_TX_TX_PING_CTRL_ALT1_	502A 0014h	502A 1014h
16h	16	FSI_TX_TX_PING_TAG	502A 0016h	502A 1016h
18h	32	FSI_TX_TX_PING_TO_REF	502A 0018h	502A 1018h
1Ch	32	FSI_TX_TX_PING_TO_CNT	502A 001Ch	502A 101Ch
20h	16	FSI_TX_TX_INT_CTRL	502A 0020h	502A 1020h
22h	16	FSI_TX_TX_DMA_CTRL	502A 0022h	502A 1022h
24h	16	FSI_TX_TX_LOCK_CTRL	502A 0024h	502A 1024h
28h	16	FSI_TX_TX_EVT_STS	502A 0028h	502A 1028h
2Ch	16	FSI_TX_TX_EVT_CLR	502A 002Ch	502A 102Ch
2Eh	16	FSI_TX_TX_EVT_FRC	502A 002Eh	502A 102Eh
30h	16	FSI_TX_TX_USER_CRC	502A 0030h	502A 1030h
40h	32	FSI_TX_TX_ECC_DATA	502A 0040h	502A 1040h
44h	16	FSI_TX_TX_ECC_VAL	502A 0044h	502A 1044h
48h	16	FSI_TX_TX_DLYLINE_CTRL	502A 0048h	502A 1048h
80h	16	FSI_TX_TX_BUF_BASE	502A 0080h	502A 1080h

3.12.1 FSI_TX Instance Count Note

Note

n = 0 to 3 for the FSI_TX registers defined below.

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3.12.2 CONTROLSS_FSI_TXn_TX_MASTER_CTRL Registers

3.12.2.1 FSI_TXn_TX_MASTER_CTRL Register (Offset = 0h) [reset = h]

Short Description: Transmit master control register

Long Description:

Return to Summary Table

Table 3-743. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0000h
CONTROLSS_FSI_TX1	5028 1000h
CONTROLSS_FSI_TX2	5028 2000h
CONTROLSS_FSI_TX3	5028 3000h

Access Types Legend

Table 3-744. TX_MASTER_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	KEY	WO	0h	Write Key In order to write to any bit in this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every change to this register.
7 - 2	RESERVED	RO		Reserved
1	FLUSH	RW	0h	Flush Operation Start bit This bit will cause the transmitter to initiate a flush pattern of a single toggle on the TXD0 and TXD1 followed by five full cycles of TXCLK. This bit should be written only when the CORE_RST bit is 0 and the clock to the Transmitter core is turned on. 0h (R/W) = Clear this bit. 1h (R/W) = Setting this bit will Initiate flush sequence. To properly execute a flush sequence, Set FLUSH to 1, wait for five TXCLK cycles then clear FLUSH to 0. Note: The KEY field must contain 0xA5 for any write to this bit to take effect. The software must keep this bit set to 1 for at least five TXCLK cycles before setting it back to 0.
0	CORE_RST	RW	0h	Transmitter Master Core Reset bit This bit controls the transmitter master core reset. In order to send any frame, this bit must be cleared. 0h (R/W) = Transmitter core is not in reset and can transmit frames. 1h (R/W) = Transmitter core is held in reset. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.

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3.12.3 CONTROLSS_FSI_TXn_TX_CLK_CTRL Registers

3.12.3.1 FSI_TXn_TX_CLK_CTRL Register (Offset = 4h) [reset = h]

Short Description: Transmit clock control register

Long Description:

Return to Summary Table

Table 3-745. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0004h
CONTROLSS_FSI_TX1	5028 1004h
CONTROLSS_FSI_TX2	5028 2004h
CONTROLSS_FSI_TX3	5028 3004h

Access Types Legend

Table 3-746. TX_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 2	PRESCALE_VAL	RW	0h	Clock Divider Prescale Value The input clock is divided by this 8-bit value and fed into the transmitter core. This divided clock is the rate at which TXCLK will operate. 0h (R/W) = Reserved 1h (R/W) = Input clock /1 2h (R/W) = Input clock /2 3h (R/W) = Input clock /3 4h (R/W) = Input clock /4 ... FFh (R/W) = Input clock /255 TXCLKIN = Input clock / PRESCALE_VAL In FSI mode: TXCLK = TXCLKIN / 2 In SPI mode: TXCLK = TXCLKIN
1	CLK_EN	RW	0h	Clock Divider Enable bit This bit will enable and disable the input clock divider and start the clock to the transmitter core. 0h (R/W) = The input clock divider is not enabled and the clock is not connected to the transmitter core. 1h (R/W) = The input clock to the transmitter core is being divided by the PRESCALE_VAL and enabled.
0	CLK_RST	RW	0h	Clock Divider Reset bit This bit will reset the clock counter in the clock divider. 0h (R/W) = The clock divider is set based on the value in PRESCALE_VAL. The input clock will be divided by PRESCALE_VAL if CLK_EN is set. 1h (R/W) = The clock divider will be reset to 0 and will stay reset until software writes a 0 to this bit.

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3.12.4 CONTROLSS_FSI_TXn_TX_OPER_CTRL_LO_ALT2_ Registers

3.12.4.1 FSI_TXn_TX_OPER_CTRL_LO_ALT2_ Register (Offset = 8h) [reset = h]

Short Description: Transmit operation control register low

Long Description:

Return to Summary Table

Table 3-747. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0008h
CONTROLSS_FSI_TX1	5028 1008h
CONTROLSS_FSI_TX2	5028 2008h
CONTROLSS_FSI_TX3	5028 3008h

Access Types Legend

Table 3-748. TX_OPER_CTRL_LO_ALT2_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO		Reserved
10	SEL_TDM_IN	RW	0h	Input TDM port Select bit This bit selects the input port for the transmitter core between the TDM input pins or the RX module. When this bit is '0', the inputs selected for TDM are from the TDM input pins. When this bit is '1', then inputs selected for TDM are from the RX module.
9	TDM_ENABLE	RW	0h	Transmit TDM Mode Enable bit. This bit enables the TDM Mode for multi-slave TDM operation. 0h (R/W) Transmit TDM Mode is not enabled. 1h (R/W) Transmit TDM Mode is enabled.
8	SEL_PLLCLK	RW	0h	Input Clock Select bit This bit selects the input clock source for the transmitter core. 0h (R/W) = SYSCLK is the source of the transmitter clock into the clock prescaler. 1h (R/W) = PLLRAWCLK is the source of the transmitter core clock into the clock prescaler.
7	PING_TO_MODE	RW	0h	Ping Counter Reset Mode Select bit This bit selects when the ping counter will reset. 0h (R/W) = The ping counter will reset and restart only on hardware initiated ping frames, when ping counter has timed out. 1h (R/W) = The ping counter will reset and restart on any software initiated frame as well as a ping counter timeout
6	SW_CRC	RW	0h	CRC Source Select bit This bit selects the source of the CRC value that is transmitted. 0h (R/W) = The transmitted CRC value is computed by hardware. 1h (R/W) = The transmitted CRC value is sourced from the value programmed in the TX_USER_CRC register.
5 - 3	START_MODE	RW	0h	Transmission Start Mode Select bit These bits select the method by which a new frame transmission is started. 0h (R/W) = Only a software write to TX_FRAME_CTRL.START initiate a new transmission. 1h (R/W) = The configured external trigger will initiate a new transmission. 2h (R/W) = Either writing to TX_FRAME_CTRL.START or the TX_FRAME_TAG_UDATA register will initiate a new transmission. All other combinations of bits are illegal and reserved for future use.
2	SPI_MODE	RW	0h	SPI Mode Select bit This bit enables and disables SPI compatibility mode. 0h (R/W) = FSI is in normal mode of operation. 1h (R/W) = FSI is operating in SPI compatibility mode.
1 - 0	DATA_WIDTH	RW	0h	Transmit Data Width Select bits These bits define the number of data lines used by the transmitter. 0h (R/W) = Data will be transmitted on one data line (TXD0) 1h (R/W) = Data will be transmitted on two data lines (TXD0 and TXD1). The format of the data is described in the preceeding chapter. 2h, 3h (R/W) = Reserved

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3.12.5 CONTROLSS_FSI_TXn_TX_OPER_CTRL_HI_ALT1_ Registers

3.12.5.1 FSI_TXn_TX_OPER_CTRL_HI_ALT1_ Register (Offset = Ah) [reset = h]

Short Description: Transmit operation control register high

Long Description:

Return to Summary Table

Table 3-749. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 000Ah
CONTROLSS_FSI_TX1	5028 100Ah
CONTROLSS_FSI_TX2	5028 200Ah
CONTROLSS_FSI_TX3	5028 300Ah

Access Types Legend

Table 3-750. TX_OPER_CTRL_HI_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12 - 7	EXT_TRIG_SEL	RW	0h	External Trigger Select bit These bits define which of the 64 external inputs will be used as the source for the external input trigger. 00h (R/W) = Trigger 1 is the source. 01h (R/W) = Trigger 2 is the source. 02h (R/W) = Trigger 3 is the source. ... 3Fh (R/W) = Trigger 64 is the source.
6	ECC_SEL	RW	0h	ECC Data Width Select bit This bit selects between 16-bit and 32-bit ECC computation. 0h (R/W) = 32-bit ECC is used. 1h (R/W) = 16-bit ECC is used.
5	FORCE_ERR	RW	0h	Error Frame Force bit This bit will force the the CRC value of the transmitted data frame to 0 whenever there is a buffer overrun or underrun condition. This can be used to force a corrupted CRC as the data is not guaranteed to be reliable. The receiver will treat the data as invalid and can handle this as needed. Note: DO NOT use FORCE_ERR if using the SW CRC mode (FSI Transmit). 0h (R/W) = The CRC will not be forced to 0. 1h (R/W) = The CRC will be forced to 0 in a buffer overrun or underrun condition.
4 - 0	RESERVED	RO		Reserved

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3.12.6 CONTROLSS_FSI_TXn_TX_FRAME_CTRL Registers

3.12.6.1 FSI_TXn_TX_FRAME_CTRL Register (Offset = Ch) [reset = h]

Short Description: Transmit frame control register

Long Description:

Return to Summary Table

Table 3-751. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 000Ch
CONTROLSS_FSI_TX1	5028 100Ch
CONTROLSS_FSI_TX2	5028 200Ch
CONTROLSS_FSI_TX3	5028 300Ch

Access Types Legend

Table 3-752. TX_FRAME_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	START	RW	0h	Start Transmission bit This bit will cause the FSI to start transmitting the next frame. 0h (R/W) = Writing a 0 to this bit will have no effect. 1h (R/W) = Start the next transmission. This bit will be cleared by hardware.
14 - 8	RESERVED	RO		Reserved
7 - 4	N_WORDS	RW	0h	Number of Words to be Transmitted This field defines the number of words which will be transmitted in a DATA_N_WORD frame. This is a user-defined field that must match the corresponding field in the receiver. Set this bitfield to be one less than the number of words to be transmitted. 0h (R/W) = 1 data word frame (16-bit data). 1h (R/W) = 2 data word frame (32-bit data). .. Fh (R/W) = 16 data word frame (256-bit data).
3 - 0	FRAME_TYPE	RW	0h	Transmit Frame Type This field determines the type of frame that will be transmitted next. 0000b (R/W) = Ping Frame. This frame can be sent either by software or automatically by hardware. 0100b (R/W) = DATA_1_WORD Frame. One word data frame (16-bit data). 0101b (R/W) = DATA_2_WORD Frame. Two word data frame (32-bit data). 0110b (R/W) = DATA_4_WORD Frame. Four word data frame (64-bit data). 0111b (R/W) = DATA_6_WORD Frame. Six word data frame (96-bit data). 0011b (R/W) = DATA_N_WORD Frame. The N_WORDS field will determine the number of words (1 to 16) to be sent. Both the transmitter and receiver must have the same value programmed. 1111b (R/W) = Error Frame. This frame can be used during error conditions or any condition where the transmitter wants to notify the receiver of a high priorty status. However, the user software is at liberty to use this for any purpose. 0001b, 0010b, and 1000b through 1110b are Reserved and should not be used.

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3.12.7 CONTROLSS_FSI_TXn_TX_FRAME_TAG_UDATA Registers

3.12.7.1 FSI_TXn_TX_FRAME_TAG_UDATA Register (Offset = Eh) [reset = h]

Short Description: Transmit frame tag and user data register

Long Description:

Return to Summary Table

Table 3-753. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 000Eh
CONTROLSS_FSI_TX1	5028 100Eh
CONTROLSS_FSI_TX2	5028 200Eh
CONTROLSS_FSI_TX3	5028 300Eh

Access Types Legend

Table 3-754. TX_FRAME_TAG_UDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	USER_DATA	RW	0h	User Data bits This is a user-defined value that will be loaded into the the user data phase of the frame. This 8-bit value can be used by the receiver for any application need. This value will not impact any hardware behavior.
7 - 4	RESERVED	RO		Reserved
3 - 0	FRAME_TAG	RW	0h	This will be used only for software initiated transmissions. Frame tag bits This is a user-defined value that will be loaded into the frame tag phase of the next transmission. The receiver may use the frame tag for any application need. This value will not impact any hardware behavior For external triggers do not use this register. Use the TX_PING_TAG register instead.

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3.12.8 CONTROLSS_FSI_TXn_TX_BUF_PTR_LOAD Registers

3.12.8.1 FSI_TXn_TX_BUF_PTR_LOAD Register (Offset = 10h) [reset = h]

Short Description: Transmit buffer pointer control load register

Long Description:

Return to Summary Table

Table 3-755. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0010h
CONTROLSS_FSI_TX1	5028 1010h
CONTROLSS_FSI_TX2	5028 2010h
CONTROLSS_FSI_TX3	5028 3010h

Access Types Legend

Table 3-756. TX_BUF_PTR_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3 - 0	BUF_PTR_LOAD	RW	0h	Buffer Pointer Load bits These bits are used to force the transmit buffer pointer to a desired index within the transmit buffer. The next transmission will begin picking data from this index and increment appropriately. This value will be reflected in TX_BUF_PTR_STS only after a minimum 3 SYSCLK cycles + 3 TXCLK cycles. This value should not be written while there is an active transmission as it may corrupt the ongoing frame or other undefined behavior.

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3.12.9 CONTROLSS_FSI_TXn_TX_BUF_PTR_STS Registers

3.12.9.1 FSI_TXn_TX_BUF_PTR_STS Register (Offset = 12h) [reset = h]

Short Description: Transmit buffer pointer control status register

Long Description:

Return to Summary Table

Table 3-757. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0012h
CONTROLSS_FSI_TX1	5028 1012h
CONTROLSS_FSI_TX2	5028 2012h
CONTROLSS_FSI_TX3	5028 3012h

Access Types Legend

Table 3-758. TX_BUF_PTR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12 - 8	CURR_WORD_CNT	RO	0h	Words Remaining in the transmit buffer This value indicates the number of words present in the data buffer which have not yet been transmitted. This value is only valid when there is no active transmission. Note: This value will not be valid if there is a buffer overrun or underrun condition.
7 - 4	RESERVED	RO		Reserved
3 - 0	CURR_BUF_PTR	RO	0h	Current Buffer Pointer Index This bitfield will show the current index of the buffer pointer. This value is only valid when there is no active transmission.

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3.12.10 CONTROLSS_FSI_TXn_TX_PING_CTRL_ALT1_ Registers

3.12.10.1 FSI_TXn_TX_PING_CTRL_ALT1_ Register (Offset = 14h) [reset = h]

Short Description: Transmit ping control register

Long Description:

Return to Summary Table

Table 3-759. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0014h
CONTROLSS_FSI_TX1	5028 1014h
CONTROLSS_FSI_TX2	5028 2014h
CONTROLSS_FSI_TX3	5028 3014h

Access Types Legend

Table 3-760. TX_PING_CTRL_ALT1_ Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 9	RESERVED	RO		Reserved
8 - 3	EXT_TRIG_SEL	RW	0h	External Trigger Select bits This bitfield will select one of the 64 external trigger inputs to as the source to generate a ping frame. A ping frame will only be generated if the EXT_TRIG_EN bit is set. 0h (R/W) = Trigger 1 will be used to generate a ping frame. 1h (R/W) = Trigger 2 will be used to generate a ping frame. .. 3Fh (R/W) = Trigger 64 will be used to generate a ping frame.
2	EXT_TRIG_EN	RW	0h	External Trigger Enable bit This bit will allow the external trigger logic to generate a ping frame. 0h (R/W) = External triggers will not be used to generate ping frames. 1h (R/W) = The selected external trigger (selected by EXT_TRIG_SEL bits) will be able to generate a ping frame. The ping timer will be ignored if this bit is set.
1	TIMER_EN	RW	0h	Ping Timer Enable bit This bit will enable the ping timer for generating periodic ping frames. 0h (R/W) = The ping timer is disabled and will not generate ping frames. 1h (R/W) = The ping timer is enabled and can be used to generate ping frames.Once the timer count reaches the value set by the TX_PING_TO_REF register, it will initiate a ping frame transmission. Note: If the ping timer is used, EXT_TRIG_EN should not be set as it will override this function.
0	CNT_RST	RW	0h	Ping Counter Reset bit Writing a 1 to this bit will reset the ping counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter. 0h (R/W) = Clear the CNT_RST. 1h (R/W) = The ping counter will be reset to 0.

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3.12.11 CONTROLSS_FSI_TXn_TX_PING_TAG Registers

3.12.11.1 FSI_TXn_TX_PING_TAG Register (Offset = 16h) [reset = h]

Short Description: Transmit ping tag register

Long Description:

Return to Summary Table

Table 3-761. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0016h
CONTROLSS_FSI_TX1	5028 1016h
CONTROLSS_FSI_TX2	5028 2016h
CONTROLSS_FSI_TX3	5028 3016h

Access Types Legend

Table 3-762. TX_PING_TAG Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3 - 0	TAG	RW	0h	Ping Frame Tag This field contains a 4-bit tag which will be sent in any ping frame that is initiated by an external trigger or the ping timer. This field is user-defined and can be set based on the application requirement. If a ping frame is generated manually, the transmitted tag will be from TX_FRAME_TAG_UDATA.FRAME_TAG, not this value.

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3.12.12 CONTROLSS_FSI_TXn_TX_PING_TO_REF Registers

3.12.12.1 FSI_TXn_TX_PING_TO_REF Register (Offset = 18h) [reset = h]

Short Description: Transmit ping timeout counter reference

Long Description:

Return to Summary Table

Table 3-763. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0018h
CONTROLSS_FSI_TX1	5028 1018h
CONTROLSS_FSI_TX2	5028 2018h
CONTROLSS_FSI_TX3	5028 3018h

Access Types Legend

Table 3-764. TX_PING_TO_REF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TO_REF	RW	0h	Ping Timer Reference Value. This is the 32-bit reference value for the ping timer. The timer will increment the counter starting from 0. When the reference value is reached, it will generate a timeout event, triggering a ping frame transmission. The counter will then reset to 0 and continue counting.

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3.12.13 CONTROLSS_FSI_TXn_TX_PING_TO_CNT Registers

3.12.13.1 FSI_TXn_TX_PING_TO_CNT Register (Offset = 1Ch) [reset = h]

Short Description: Transmit ping timeout current count

Long Description:

Return to Summary Table

Table 3-765. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 001Ch
CONTROLSS_FSI_TX1	5028 101Ch
CONTROLSS_FSI_TX2	5028 201Ch
CONTROLSS_FSI_TX3	5028 301Ch

Access Types Legend

Table 3-766. TX_PING_TO_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TO_CNT	RO	0h	Ping Timer Counter Value This register contains the current value of the ping timer counter. After reset, this counter will increment until it reaches the reference value (TX_PING_TO_REF), at which point it generates a ping frame transmission. After this point, the counter will reset to 0 and continue counting. This is a free-running counter

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3.12.14 CONTROLSS_FSI_TXn_TX_INT_CTRL Registers

3.12.14.1 FSI_TXn_TX_INT_CTRL Register (Offset = 20h) [reset = h]

Short Description: Transmit interrupt event control register

Long Description:

Return to Summary Table

Table 3-767. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0020h
CONTROLSS_FSI_TX1	5028 1020h
CONTROLSS_FSI_TX2	5028 2020h
CONTROLSS_FSI_TX3	5028 3020h

Access Types Legend

Table 3-768. TX_INT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 12	RESERVED	RO		Reserved
11	INT2_EN_PING_TO	RW	0h	Enable PING Timer Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT2. 1h (R/W) = The ping timer event will trigger an interrupt on TX_INT2.
10	INT2_EN_BUF_OVERRUN	RW	0h	Enable Buffer Overrun Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT2. 1h (R/W) = A Buffer Overrun condition will trigger an interrupt on TX_INT2.
9	INT2_EN_BUF_UNDERRUN	RW	0h	Enable Buffer Underrun Interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT2. 1h (R/W) = A Buffer Underrun condition will trigger an interrupt on TX_INT2.
8	INT2_EN_FRAME_DONE	RW	0h	Enable Frame Done interrupt to INT2 This bit allows the event to generate an interrupt on the INT2 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT2. 1h (R/W) = A Frame Done event will trigger an interrupt on TX_INT2.
7 - 4	RESERVED	RO		Reserved
3	INT1_EN_PING_TO	RW	0h	Enable Ping Timer Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT1. 1h (R/W) = The ping timer event will trigger an interrupt on TX_INT1.
2	INT1_EN_BUF_OVERRUN	RW	0h	Enable Buffer Overrun Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT1. 1h (R/W) = A Buffer Overrun condition will trigger an interrupt on TX_INT1.
1	INT1_EN_BUF_UNDERRUN	RW	0h	Enable Buffer Underrun Interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT1. 1h (R/W) = A Buffer Underrun condition will trigger an interrupt on TX_INT1.
0	INT1_EN_FRAME_DONE	RW	0h	Enable Frame Done interrupt to INT1 This bit allows the event to generate an interrupt on the INT1 line. 0h (R/W) = This event will not trigger an interrupt on TX_INT1. 1h (R/W) = A Frame Done event will trigger an interrupt on TX_INT1.

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3.12.15 CONTROLSS_FSI_TXn_TX_DMA_CTRL Registers

3.12.15.1 FSI_TXn_TX_DMA_CTRL Register (Offset = 22h) [reset = h]

Short Description: Transmit DMA event control register

Long Description:

Return to Summary Table

Table 3-769. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0022h
CONTROLSS_FSI_TX1	5028 1022h
CONTROLSS_FSI_TX2	5028 2022h
CONTROLSS_FSI_TX3	5028 3022h

Access Types Legend

Table 3-770. TX_DMA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 1	RESERVED	RO		Reserved
0	DMA_EVT_EN	RW	0h	DMA Event Enable bit This bit will enable the DMA event to be generated upon the completion of a transmit frame. 0h (R/W) = A DMA event will not be generated. 1h (R/W) = A DMA event will be generated upon the completion of a transmitted frame. Note: The DMA event will only be generated for data frames.

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3.12.16 CONTROLSS_FSI_TXn_TX_LOCK_CTRL Registers

3.12.16.1 FSI_TXn_TX_LOCK_CTRL Register (Offset = 24h) [reset = h]

Short Description: Transmit lock control register

Long Description:

Return to Summary Table

Table 3-771. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0024h
CONTROLSS_FSI_TX1	5028 1024h
CONTROLSS_FSI_TX2	5028 2024h
CONTROLSS_FSI_TX3	5028 3024h

Access Types Legend

Table 3-772. TX_LOCK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	KEY	WO	0h	Write Key In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after writing, so it must be written again for every change to this register.
7 - 1	RESERVED	RO		Reserved
0	LOCK	RW	0h	Control Register Lock Enable bit This bit locks the contents of all the transmit control registers that support a lock protection. Once locked, further writes will not take effect until a SYSRS has reset this register. Once set, further writes to this bit will be ignored. 0h (R/W) = Transmit control registers can be modified and are not locked. 1h (R/W) = Transmit control registers are locked and cannot be modified until this bit is cleared by SYSRS. Any further writes to this bit are ignored. Note: The KEY field must contatin 0xA5 for any write to this bit to take effect.

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3.12.17 CONTROLSS_FSI_TXn_TX_EVT_STS Registers

3.12.17.1 FSI_TXn_TX_EVT_STS Register (Offset = 28h) [reset = h]

Short Description: Transmit event and error status flag register

Long Description:

Return to Summary Table

Table 3-773. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0028h
CONTROLSS_FSI_TX1	5028 1028h
CONTROLSS_FSI_TX2	5028 2028h
CONTROLSS_FSI_TX3	5028 3028h

Access Types Legend

Table 3-774. TX_EVT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3	PING_TRIGGERED	RO	0h	Ping Frame Triggered Flag Bit This bit indicates that a ping frame has been triggered. This bit is set by hardware when either the ping timer or an external trigger event have occured. Software can also force this bit to get set by writing to the TX_EVT_FRC register. 0h (R) = A ping frame has not been triggered. 1h (R) = A ping frame has been triggered by either the ping timer or external trigger. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register.
2	BUF_OVERRUN	RO	0h	Buffer Overrun Flag Bit This bit inditcates that buffer overrun has occured.Software can also force this bit to get set by writing to the TX_EVT_FRC register. 0h (R) = Buffer Overrun has not occured. 1h (R) = Buffer Overrun has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register.
1	BUF_UNDERRUN	RO	0h	Buffer Underrun Flag Bit This bit inditcates that buffer underrun has occured.Software can also force this bit to get set by writing to the TX_EVT_FRC register. 0h (R) = Buffer Underrun has not occured. 1h (R) = Buffer Underrun has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register.
0	FRAME_DONE	RO	0h	Frame Done Flag Bit This bit inditcates a Frame Done condition. This bit is set by hardware when a frame transmission has been completed. Software can also force this bit to get set by writing to the TX_EVT_FRC register. 0h (R) = Frame Done condition has not occured. 1h (R) = Frame Done condition has occured. To clear this bit, write to the corresponding bit in the TX_EVT_CLR register.

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3.12.18 CONTROLSS_FSI_TXn_TX_EVT_CLR Registers

3.12.18.1 FSI_TXn_TX_EVT_CLR Register (Offset = 2Ch) [reset = h]

Short Description: Transmit event and error clear register

Long Description:

Return to Summary Table

Table 3-775. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 002Ch
CONTROLSS_FSI_TX1	5028 102Ch
CONTROLSS_FSI_TX2	5028 202Ch
CONTROLSS_FSI_TX3	5028 302Ch

Access Types Legend

Table 3-776. TX_EVT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3	PING_TRIGGERED	WO	0h	Ping Frame Triggered Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0. Note: This bit may not always be cleared when writing to the corresponding TX_EVT_CLR bit. If PING_TIMEOUT MODE is configured to be 0, a hardware ping timeout may occur when another frame is actively being transmitted. In this case, if this bit still shows as 1 after the clear bit is written then the ping frame has been triggered but not serviced. This bit does not indicate that the ping frame has been completely sent, only that it has been triggered by the timeout event.
2	BUF_OVERRUN	WO	0h	Buffer Overrun Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0.
1	BUF_UNDERRUN	WO	0h	Buffer Underrun Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0.
0	FRAME_DONE	WO	0h	Frame Done Flag Clear bit This bit clears the corresponding bit in the TX_EVT_STS register. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0.

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3.12.19 CONTROLSS_FSI_TXn_TX_EVT_FRC Registers

3.12.19.1 FSI_TXn_TX_EVT_FRC Register (Offset = 2Eh) [reset = h]

Short Description: Transmit event and error flag force register

Long Description:

Return to Summary Table

Table 3-777. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 002Eh
CONTROLSS_FSI_TX1	5028 102Eh
CONTROLSS_FSI_TX2	5028 202Eh
CONTROLSS_FSI_TX3	5028 302Eh

Access Types Legend

Table 3-778. TX_EVT_FRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 4	RESERVED	RO		Reserved
3	PING_TRIGGERED	WO	0h	Ping Frame Triggered Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding flag bit in the TX_EVT_STS Register.
2	BUF_OVERRUN	WO	0h	Buffer Overrun Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (R/W) = Writing a 0 to this bit will have no effect. 1h (R/W) = Force the corresponding flag bit in the TX_EVT_STS Register.
1	BUF_UNDERRUN	WO	0h	Buffer Underrun Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding flag bit in the TX_EVT_STS Register.
0	FRAME_DONE	WO	0h	Frame Done Flag Force bit This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR. 0h (W) = Writing a 0 to this bit will have no effect. 1h (W) = Force the corresponding flag bit in the TX_EVT_STS Register.

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3.12.20 CONTROLSS_FSI_TXn_TX_USER_CRC Registers

3.12.20.1 FSI_TXn_TX_USER_CRC Register (Offset = 30h) [reset = h]

Short Description: Transmit user-defined CRC register

Long Description:

Return to Summary Table

Table 3-779. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0030h
CONTROLSS_FSI_TX1	5028 1030h
CONTROLSS_FSI_TX2	5028 2030h
CONTROLSS_FSI_TX3	5028 3030h

Access Types Legend

Table 3-780. TX_USER_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO		Reserved
7 - 0	USER_CRC	RW	0h	User-defined CRC This register contains the 8-bit CRC value to be transmitted in the next frame if the transmission is set for user-defined CRC option (TX_OPER_CTRL_LO.SW_CRC = 1). This register is ignored if the hardware CRC generation is enabled.

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3.12.21 CONTROLSS_FSI_TXn_TX_ECC_DATA Registers

3.12.21.1 FSI_TXn_TX_ECC_DATA Register (Offset = 40h) [reset = h]

Short Description: Transmit ECC data register

Long Description:

Return to Summary Table

Table 3-781. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0040h
CONTROLSS_FSI_TX1	5028 1040h
CONTROLSS_FSI_TX2	5028 2040h
CONTROLSS_FSI_TX3	5028 3040h

Access Types Legend

Table 3-782. TX_ECC_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA_HIGH	RW	0h	Upper 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC(SEC-DED) the entire 32-bit register and update TX_ECC_VAL register with the results. Software should write to these 16 bits of the register in a 32-bit write when needing to compute ECC for 32-bits for the full TX_ECC_DATA register.
15 - 0	DATA_LOW	RW	0h	Lower 16 bits of ECC Data Writing to this bitfield will cause the ECC logic to compute the ECC(SEC-DED) for these 16 bits and update the TX_ECC_VAL register with the results. Software should write to these register bits as a 16-bit write when needing to compute ECC for 16-bits.

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3.12.22 CONTROLSS_FSI_TXn_TX_ECC_VAL Registers

3.12.22.1 FSI_TXn_TX_ECC_VAL Register (Offset = 44h) [reset = h]

Short Description: Transmit ECC value register

Long Description:

Return to Summary Table

Table 3-783. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0044h
CONTROLSS_FSI_TX1	5028 1044h
CONTROLSS_FSI_TX2	5028 2044h
CONTROLSS_FSI_TX3	5028 3044h

Access Types Legend

Table 3-784. TX_ECC_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 7	RESERVED	RO		Reserved
6 - 0	ECC_VAL	RO	44Ch	Computed ECC Value This field contains the ECC value computed using SEC-DED either for 16-bit or 32-bit data in the TX_ECC_DATA register.

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3.12.23 CONTROLSS_FSI_TXn_TX_DLYLINE_CTRL Registers

3.12.23.1 FSI_TXn_TX_DLYLINE_CTRL Register (Offset = 48h) [reset = h]

Short Description: Transmit delay Line control register

Long Description:

Return to Summary Table

Table 3-785. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0048h
CONTROLSS_FSI_TX1	5028 1048h
CONTROLSS_FSI_TX2	5028 2048h
CONTROLSS_FSI_TX3	5028 3048h

Access Types Legend

Table 3-786. TX_DLYLINE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14 - 10	TXD1_DLY	RW	0h	Delay Line Tap Select for TXD1 This bitfield selects the number of delay elements inserted into the TXD1 path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the TXD1 path. TXD1 is taken directly from the pin. 1h (R/W) One delay element is included in the TXD1 path. 2h (R/W) Two delay elements are included in the TXD1 path. ... 1Fh (R/W) 31 delay elements are included in the TXD1 path, the maximum.
9 - 5	TXD0_DLY	RW	0h	Delay Line Tap Select for TXD0 This bitfield selects the number of delay elements inserted into the TXD0 path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the TXD0 path. TXD0 is taken directly from the pin. 1h (R/W) One delay element is included in the TXD0 path. 2h (R/W) Two delay elements are included in the TXD0 path. ... 1Fh (R/W) 31 delay elements are included in the TXD0 path, the maximum.
4 - 0	TXCLK_DLY	RW	0h	Delay Line Tap Select for TXCLK This bitfield selects the number of delay elements inserted into the RXCLK path from the pin boundary to the receiver core. 0h (R/W) Zero delay elements are included in the TXCLK path. TXCLK is taken directly from the pin. 1h (R/W) One delay element is included in the TXCLK path. 2h (R/W) Two delay elements are included in the TXCLK path. ... 1Fh (R/W) 31 delay elements are included in the TXCLK path, the maximum.

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3.12.24 CONTROLSS_FSI_TXn_TX_BUF_BASE Registers

3.12.24.1 FSI_TXn_TX_BUF_BASE Register (Offset = 80h) [reset = h]

Short Description: Base address for transmit buffer

Long Description:

Return to Summary Table

Table 3-787. Instance Table

Instance Name	Physical Address
CONTROLSS_FSI_TX0	5028 0080h
CONTROLSS_FSI_TX1	5028 1080h
CONTROLSS_FSI_TX2	5028 2080h
CONTROLSS_FSI_TX3	5028 3080h

Access Types Legend

Table 3-788. TX_BUF_BASE Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BASE_ADDRESS	RW	0h	Transmit Data Buffer Base Address This is the base address of the 16-word data buffer used by the transmitter.

3.12.25 Access Table

Table 3-789. Access Type Codes

Access Type	Code	Description
WO	WO	Write
RO	RO	Read
RW	RW	Read / Write

3.13 GLOBAL_CTRL Registers

Table 3-790. CONTROLSS_GLOBAL_CTRL Register Base Address Table

Offset	Length	Register Name	CONTROLSS_GLOBAL_CTRL Physical Address
0h	32	GLOBAL_CTRL_PID	502F 0000h
4h	32	GLOBAL_CTRL_EPWM_STATICXBAR_SEL0	502F 0004h
8h	32	GLOBAL_CTRL_EPWM_STATICXBAR_SEL1	502F 0008h
10h	32	GLOBAL_CTRL_EPWM_CLKSYNC	502F 0010h
18h	0	GLOBAL_CTRL_SDFM1_CLK0_SEL	502F 0018h
20h	8	GLOBAL_CTRL_EMUSTOPN_MASK	502F 0020h
28h	32	GLOBAL_CTRL_CLB_AQ_EN0	502F 0028h
30h	32	GLOBAL_CTRL_CLB_AQ_EN1	502F 0030h
38h	32	GLOBAL_CTRL_CLB_DB_EN0	502F 0038h
40h	32	GLOBAL_CTRL_CLB_DB_EN1	502F 0040h
100h	8	GLOBAL_CTRL_EPWM0_CLK_GATE	502F 0100h
104h	8	GLOBAL_CTRL_EPWM1_CLK_GATE	502F 0104h
108h	8	GLOBAL_CTRL_EPWM2_CLK_GATE	502F 0108h
10Ch	8	GLOBAL_CTRL_EPWM3_CLK_GATE	502F 010Ch
110h	8	GLOBAL_CTRL_EPWM4_CLK_GATE	502F 0110h
114h	8	GLOBAL_CTRL_EPWM5_CLK_GATE	502F 0114h
118h	8	GLOBAL_CTRL_EPWM6_CLK_GATE	502F 0118h

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Table 3-790. CONTROLSS_GLOBAL_CTRL Register Base Address Table (continued)

Offset	Length	Register Name	CONTROLSS_GLOBAL_CTRL Physical Address
11Ch	8	GLOBAL_CTRL_EPWM7_CLK_GATE	502F 011Ch
120h	8	GLOBAL_CTRL_EPWM8_CLK_GATE	502F 0120h
124h	8	GLOBAL_CTRL_EPWM9_CLK_GATE	502F 0124h
128h	8	GLOBAL_CTRL_EPWM10_CLK_GATE	502F 0128h
12Ch	8	GLOBAL_CTRL_EPWM11_CLK_GATE	502F 012Ch
130h	8	GLOBAL_CTRL_EPWM12_CLK_GATE	502F 0130h
134h	8	GLOBAL_CTRL_EPWM13_CLK_GATE	502F 0134h
138h	8	GLOBAL_CTRL_EPWM14_CLK_GATE	502F 0138h
13Ch	8	GLOBAL_CTRL_EPWM15_CLK_GATE	502F 013Ch
140h	8	GLOBAL_CTRL_EPWM16_CLK_GATE	502F 0140h
144h	8	GLOBAL_CTRL_EPWM17_CLK_GATE	502F 0144h
148h	8	GLOBAL_CTRL_EPWM18_CLK_GATE	502F 0148h
14Ch	8	GLOBAL_CTRL_EPWM19_CLK_GATE	502F 014Ch
150h	8	GLOBAL_CTRL_EPWM20_CLK_GATE	502F 0150h
154h	8	GLOBAL_CTRL_EPWM21_CLK_GATE	502F 0154h
158h	8	GLOBAL_CTRL_EPWM22_CLK_GATE	502F 0158h
15Ch	8	GLOBAL_CTRL_EPWM23_CLK_GATE	502F 015Ch
160h	8	GLOBAL_CTRL_EPWM24_CLK_GATE	502F 0160h
164h	8	GLOBAL_CTRL_EPWM25_CLK_GATE	502F 0164h
168h	8	GLOBAL_CTRL_EPWM26_CLK_GATE	502F 0168h
16Ch	8	GLOBAL_CTRL_EPWM27_CLK_GATE	502F 016Ch
170h	8	GLOBAL_CTRL_EPWM28_CLK_GATE	502F 0170h
174h	8	GLOBAL_CTRL_EPWM29_CLK_GATE	502F 0174h
178h	8	GLOBAL_CTRL_EPWM30_CLK_GATE	502F 0178h
17Ch	8	GLOBAL_CTRL_EPWM31_CLK_GATE	502F 017Ch
180h	8	GLOBAL_CTRL_FSI_TX0_CLK_GATE	502F 0180h
184h	8	GLOBAL_CTRL_FSI_TX1_CLK_GATE	502F 0184h
188h	8	GLOBAL_CTRL_FSI_TX2_CLK_GATE	502F 0188h
18Ch	8	GLOBAL_CTRL_FSI_TX3_CLK_GATE	502F 018Ch
190h	8	GLOBAL_CTRL_FSI_RX0_CLK_GATE	502F 0190h
194h	8	GLOBAL_CTRL_FSI_RX1_CLK_GATE	502F 0194h
198h	8	GLOBAL_CTRL_FSI_RX2_CLK_GATE	502F 0198h
19Ch	8	GLOBAL_CTRL_FSI_RX3_CLK_GATE	502F 019Ch
1A0h	8	GLOBAL_CTRL_CMPSSA0_CLK_GATE	502F 01A0h
1A4h	8	GLOBAL_CTRL_CMPSSA1_CLK_GATE	502F 01A4h
1A8h	8	GLOBAL_CTRL_CMPSSA2_CLK_GATE	502F 01A8h
1ACh	8	GLOBAL_CTRL_CMPSSA3_CLK_GATE	502F 01ACh
1B0h	8	GLOBAL_CTRL_CMPSSA4_CLK_GATE	502F 01B0h
1B4h	8	GLOBAL_CTRL_CMPSSA5_CLK_GATE	502F 01B4h
1B8h	8	GLOBAL_CTRL_CMPSSA6_CLK_GATE	502F 01B8h
1BCh	8	GLOBAL_CTRL_CMPSSA7_CLK_GATE	502F 01BCh
1C0h	8	GLOBAL_CTRL_CMPSSA8_CLK_GATE	502F 01C0h
1C4h	8	GLOBAL_CTRL_CMPSSA9_CLK_GATE	502F 01C4h
1D0h	8	GLOBAL_CTRL_CMPSSB0_CLK_GATE	502F 01D0h
1D4h	8	GLOBAL_CTRL_CMPSSB1_CLK_GATE	502F 01D4h
1D8h	8	GLOBAL_CTRL_CMPSSB2_CLK_GATE	502F 01D8h

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Table 3-790. CONTROLSS_GLOBAL_CTRL Register Base Address Table (continued)

Offset	Length	Register Name	CONTROLSS_GLOBAL_CTRL Physical Address
1DCh	8	GLOBAL_CTRL_CMPSSB3_CLK_GATE	502F 01DCh
1E0h	8	GLOBAL_CTRL_CMPSSB4_CLK_GATE	502F 01E0h
1E4h	8	GLOBAL_CTRL_CMPSSB5_CLK_GATE	502F 01E4h
1E8h	8	GLOBAL_CTRL_CMPSSB6_CLK_GATE	502F 01E8h
1ECh	8	GLOBAL_CTRL_CMPSSB7_CLK_GATE	502F 01ECh
1F0h	8	GLOBAL_CTRL_CMPSSB8_CLK_GATE	502F 01F0h
1F4h	8	GLOBAL_CTRL_CMPSSB9_CLK_GATE	502F 01F4h
200h	8	GLOBAL_CTRL_ECAP0_CLK_GATE	502F 0200h
204h	8	GLOBAL_CTRL_ECAP1_CLK_GATE	502F 0204h
208h	8	GLOBAL_CTRL_ECAP2_CLK_GATE	502F 0208h
20Ch	8	GLOBAL_CTRL_ECAP3_CLK_GATE	502F 020Ch
210h	8	GLOBAL_CTRL_ECAP4_CLK_GATE	502F 0210h
214h	8	GLOBAL_CTRL_ECAP5_CLK_GATE	502F 0214h
218h	8	GLOBAL_CTRL_ECAP6_CLK_GATE	502F 0218h
21Ch	8	GLOBAL_CTRL_ECAP7_CLK_GATE	502F 021Ch
220h	8	GLOBAL_CTRL_ECAP8_CLK_GATE	502F 0220h
224h	8	GLOBAL_CTRL_ECAP9_CLK_GATE	502F 0224h
240h	8	GLOBAL_CTRL_EQEP0_CLK_GATE	502F 0240h
244h	8	GLOBAL_CTRL_EQEP1_CLK_GATE	502F 0244h
248h	8	GLOBAL_CTRL_EQEP2_CLK_GATE	502F 0248h
250h	8	GLOBAL_CTRL_SDFM0_CLK_GATE	502F 0250h
254h	8	GLOBAL_CTRL_SDFM1_CLK_GATE	502F 0254h
258h	8	GLOBAL_CTRL_DAC_CLK_GATE	502F 0258h
25Ch	8	GLOBAL_CTRL_ADC0_CLK_GATE	502F 025Ch
260h	8	GLOBAL_CTRL_ADC1_CLK_GATE	502F 0260h
264h	8	GLOBAL_CTRL_ADC2_CLK_GATE	502F 0264h
268h	8	GLOBAL_CTRL_ADC3_CLK_GATE	502F 0268h
26Ch	8	GLOBAL_CTRL_ADC4_CLK_GATE	502F 026Ch
270h	8	GLOBAL_CTRL_OTTO0_CLK_GATE	502F 0270h
274h	8	GLOBAL_CTRL_OTTO1_CLK_GATE	502F 0274h
278h	8	GLOBAL_CTRL_OTTO2_CLK_GATE	502F 0278h
27Ch	8	GLOBAL_CTRL_OTTO3_CLK_GATE	502F 027Ch
280h	8	GLOBAL_CTRL_SDFM0_PLL_CLK_GATE	502F 0280h
284h	8	GLOBAL_CTRL_SDFM1_PLL_CLK_GATE	502F 0284h
288h	8	GLOBAL_CTRL_FSI_TX0_PLL_CLK_GATE	502F 0288h
28Ch	8	GLOBAL_CTRL_FSI_TX1_PLL_CLK_GATE	502F 028Ch
290h	8	GLOBAL_CTRL_FSI_TX2_PLL_CLK_GATE	502F 0290h
294h	8	GLOBAL_CTRL_FSI_TX3_PLL_CLK_GATE	502F 0294h
300h	8	GLOBAL_CTRL_EPWM0_RST	502F 0300h
304h	8	GLOBAL_CTRL_EPWM1_RST	502F 0304h
308h	8	GLOBAL_CTRL_EPWM2_RST	502F 0308h
30Ch	8	GLOBAL_CTRL_EPWM3_RST	502F 030Ch
310h	8	GLOBAL_CTRL_EPWM4_RST	502F 0310h
314h	8	GLOBAL_CTRL_EPWM5_RST	502F 0314h
318h	8	GLOBAL_CTRL_EPWM6_RST	502F 0318h
31Ch	8	GLOBAL_CTRL_EPWM7_RST	502F 031Ch

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Table 3-790. CONTROLSS_GLOBAL_CTRL Register Base Address Table (continued)

Offset	Length	Register Name	CONTROLSS_GLOBAL_CTRL Physical Address
320h	8	GLOBAL_CTRL_EPWM8_RST	502F 0320h
324h	8	GLOBAL_CTRL_EPWM9_RST	502F 0324h
328h	8	GLOBAL_CTRL_EPWM10_RST	502F 0328h
32Ch	8	GLOBAL_CTRL_EPWM11_RST	502F 032Ch
330h	8	GLOBAL_CTRL_EPWM12_RST	502F 0330h
334h	8	GLOBAL_CTRL_EPWM13_RST	502F 0334h
338h	8	GLOBAL_CTRL_EPWM14_RST	502F 0338h
33Ch	8	GLOBAL_CTRL_EPWM15_RST	502F 033Ch
340h	8	GLOBAL_CTRL_EPWM16_RST	502F 0340h
344h	8	GLOBAL_CTRL_EPWM17_RST	502F 0344h
348h	8	GLOBAL_CTRL_EPWM18_RST	502F 0348h
34Ch	8	GLOBAL_CTRL_EPWM19_RST	502F 034Ch
350h	8	GLOBAL_CTRL_EPWM20_RST	502F 0350h
354h	8	GLOBAL_CTRL_EPWM21_RST	502F 0354h
358h	8	GLOBAL_CTRL_EPWM22_RST	502F 0358h
35Ch	8	GLOBAL_CTRL_EPWM23_RST	502F 035Ch
360h	8	GLOBAL_CTRL_EPWM24_RST	502F 0360h
364h	8	GLOBAL_CTRL_EPWM25_RST	502F 0364h
368h	8	GLOBAL_CTRL_EPWM26_RST	502F 0368h
36Ch	8	GLOBAL_CTRL_EPWM27_RST	502F 036Ch
370h	8	GLOBAL_CTRL_EPWM28_RST	502F 0370h
374h	8	GLOBAL_CTRL_EPWM29_RST	502F 0374h
378h	8	GLOBAL_CTRL_EPWM30_RST	502F 0378h
37Ch	8	GLOBAL_CTRL_EPWM31_RST	502F 037Ch
380h	8	GLOBAL_CTRL_FSI_TX0_RST	502F 0380h
384h	8	GLOBAL_CTRL_FSI_TX1_RST	502F 0384h
388h	8	GLOBAL_CTRL_FSI_TX2_RST	502F 0388h
38Ch	8	GLOBAL_CTRL_FSI_TX3_RST	502F 038Ch
390h	8	GLOBAL_CTRL_FSI_RX0_RST	502F 0390h
394h	8	GLOBAL_CTRL_FSI_RX1_RST	502F 0394h
398h	8	GLOBAL_CTRL_FSI_RX2_RST	502F 0398h
39Ch	8	GLOBAL_CTRL_FSI_RX3_RST	502F 039Ch
3A0h	8	GLOBAL_CTRL_CMPSSA0_RST	502F 03A0h
3A4h	8	GLOBAL_CTRL_CMPSSA1_RST	502F 03A4h
3A8h	8	GLOBAL_CTRL_CMPSSA2_RST	502F 03A8h
3ACh	8	GLOBAL_CTRL_CMPSSA3_RST	502F 03ACh
3B0h	8	GLOBAL_CTRL_CMPSSA4_RST	502F 03B0h
3B4h	8	GLOBAL_CTRL_CMPSSA5_RST	502F 03B4h
3B8h	8	GLOBAL_CTRL_CMPSSA6_RST	502F 03B8h
3BCh	8	GLOBAL_CTRL_CMPSSA7_RST	502F 03BCh
3C0h	8	GLOBAL_CTRL_CMPSSA8_RST	502F 03C0h
3C4h	8	GLOBAL_CTRL_CMPSSA9_RST	502F 03C4h
3D0h	8	GLOBAL_CTRL_CMPSSB0_RST	502F 03D0h
3D4h	8	GLOBAL_CTRL_CMPSSB1_RST	502F 03D4h
3D8h	8	GLOBAL_CTRL_CMPSSB2_RST	502F 03D8h
3DCh	8	GLOBAL_CTRL_CMPSSB3_RST	502F 03DCh

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Table 3-790. CONTROLSS_GLOBAL_CTRL Register Base Address Table (continued)

Offset	Length	Register Name	CONTROLSS_GLOBAL_CTRL Physical Address
3E0h	8	GLOBAL_CTRL_CMPSSB4_RST	502F 03E0h
3E4h	8	GLOBAL_CTRL_CMPSSB5_RST	502F 03E4h
3E8h	8	GLOBAL_CTRL_CMPSSB6_RST	502F 03E8h
3ECh	8	GLOBAL_CTRL_CMPSSB7_RST	502F 03ECh
3F0h	8	GLOBAL_CTRL_CMPSSB8_RST	502F 03F0h
3F4h	8	GLOBAL_CTRL_CMPSSB9_RST	502F 03F4h
400h	8	GLOBAL_CTRL_ECAP0_RST	502F 0400h
404h	8	GLOBAL_CTRL_ECAP1_RST	502F 0404h
408h	8	GLOBAL_CTRL_ECAP2_RST	502F 0408h
40Ch	8	GLOBAL_CTRL_ECAP3_RST	502F 040Ch
410h	8	GLOBAL_CTRL_ECAP4_RST	502F 0410h
414h	8	GLOBAL_CTRL_ECAP5_RST	502F 0414h
418h	8	GLOBAL_CTRL_ECAP6_RST	502F 0418h
41Ch	8	GLOBAL_CTRL_ECAP7_RST	502F 041Ch
420h	8	GLOBAL_CTRL_ECAP8_RST	502F 0420h
424h	8	GLOBAL_CTRL_ECAP9_RST	502F 0424h
440h	8	GLOBAL_CTRL_EQEP0_RST	502F 0440h
444h	8	GLOBAL_CTRL_EQEP1_RST	502F 0444h
448h	8	GLOBAL_CTRL_EQEP2_RST	502F 0448h
450h	8	GLOBAL_CTRL_SDFM0_RST	502F 0450h
454h	8	GLOBAL_CTRL_SDFM1_RST	502F 0454h
458h	8	GLOBAL_CTRL_DAC_RST	502F 0458h
45Ch	8	GLOBAL_CTRL_ADC0_RST	502F 045Ch
460h	8	GLOBAL_CTRL_ADC1_RST	502F 0460h
464h	8	GLOBAL_CTRL_ADC2_RST	502F 0464h
468h	8	GLOBAL_CTRL_ADC3_RST	502F 0468h
46Ch	8	GLOBAL_CTRL_ADC4_RST	502F 046Ch
470h	8	GLOBAL_CTRL_OTTO0_RST	502F 0470h
474h	8	GLOBAL_CTRL_OTTO1_RST	502F 0474h
478h	8	GLOBAL_CTRL_OTTO2_RST	502F 0478h
47Ch	8	GLOBAL_CTRL_OTTO3_RST	502F 047Ch
500h	8	GLOBAL_CTRL_EPWM0_HALTEN	502F 0500h
504h	8	GLOBAL_CTRL_EPWM1_HALTEN	502F 0504h
508h	8	GLOBAL_CTRL_EPWM2_HALTEN	502F 0508h
50Ch	8	GLOBAL_CTRL_EPWM3_HALTEN	502F 050Ch
510h	8	GLOBAL_CTRL_EPWM4_HALTEN	502F 0510h
514h	8	GLOBAL_CTRL_EPWM5_HALTEN	502F 0514h
518h	8	GLOBAL_CTRL_EPWM6_HALTEN	502F 0518h
51Ch	8	GLOBAL_CTRL_EPWM7_HALTEN	502F 051Ch
520h	8	GLOBAL_CTRL_EPWM8_HALTEN	502F 0520h
524h	8	GLOBAL_CTRL_EPWM9_HALTEN	502F 0524h
528h	8	GLOBAL_CTRL_EPWM10_HALTEN	502F 0528h
52Ch	8	GLOBAL_CTRL_EPWM11_HALTEN	502F 052Ch
530h	8	GLOBAL_CTRL_EPWM12_HALTEN	502F 0530h
534h	8	GLOBAL_CTRL_EPWM13_HALTEN	502F 0534h
538h	8	GLOBAL_CTRL_EPWM14_HALTEN	502F 0538h

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Table 3-790. CONTROLSS_GLOBAL_CTRL Register Base Address Table (continued)

Offset	Length	Register Name	CONTROLSS_GLOBAL_CTRL Physical Address
53Ch	8	GLOBAL_CTRL_EPWM15_HALTEN	502F 053Ch
540h	8	GLOBAL_CTRL_EPWM16_HALTEN	502F 0540h
544h	8	GLOBAL_CTRL_EPWM17_HALTEN	502F 0544h
548h	8	GLOBAL_CTRL_EPWM18_HALTEN	502F 0548h
54Ch	8	GLOBAL_CTRL_EPWM19_HALTEN	502F 054Ch
550h	8	GLOBAL_CTRL_EPWM20_HALTEN	502F 0550h
554h	8	GLOBAL_CTRL_EPWM21_HALTEN	502F 0554h
558h	8	GLOBAL_CTRL_EPWM22_HALTEN	502F 0558h
55Ch	8	GLOBAL_CTRL_EPWM23_HALTEN	502F 055Ch
560h	8	GLOBAL_CTRL_EPWM24_HALTEN	502F 0560h
564h	8	GLOBAL_CTRL_EPWM25_HALTEN	502F 0564h
568h	8	GLOBAL_CTRL_EPWM26_HALTEN	502F 0568h
56Ch	8	GLOBAL_CTRL_EPWM27_HALTEN	502F 056Ch
570h	8	GLOBAL_CTRL_EPWM28_HALTEN	502F 0570h
574h	8	GLOBAL_CTRL_EPWM29_HALTEN	502F 0574h
578h	8	GLOBAL_CTRL_EPWM30_HALTEN	502F 0578h
57Ch	8	GLOBAL_CTRL_EPWM31_HALTEN	502F 057Ch
580h	8	GLOBAL_CTRL_CMPSSA0_HALTEN	502F 0580h
584h	8	GLOBAL_CTRL_CMPSSA1_HALTEN	502F 0584h
588h	8	GLOBAL_CTRL_CMPSSA2_HALTEN	502F 0588h
58Ch	8	GLOBAL_CTRL_CMPSSA3_HALTEN	502F 058Ch
590h	8	GLOBAL_CTRL_CMPSSA4_HALTEN	502F 0590h
594h	8	GLOBAL_CTRL_CMPSSA5_HALTEN	502F 0594h
598h	8	GLOBAL_CTRL_CMPSSA6_HALTEN	502F 0598h
59Ch	8	GLOBAL_CTRL_CMPSSA7_HALTEN	502F 059Ch
5A0h	8	GLOBAL_CTRL_CMPSSA8_HALTEN	502F 05A0h
5A4h	8	GLOBAL_CTRL_CMPSSA9_HALTEN	502F 05A4h
5A8h	8	GLOBAL_CTRL_CMPSSB0_HALTEN	502F 05A8h
5ACh	8	GLOBAL_CTRL_CMPSSB1_HALTEN	502F 05ACh
5B0h	8	GLOBAL_CTRL_CMPSSB2_HALTEN	502F 05B0h
5B4h	8	GLOBAL_CTRL_CMPSSB3_HALTEN	502F 05B4h
5B8h	8	GLOBAL_CTRL_CMPSSB4_HALTEN	502F 05B8h
5BCh	8	GLOBAL_CTRL_CMPSSB5_HALTEN	502F 05BCh
5C0h	8	GLOBAL_CTRL_CMPSSB6_HALTEN	502F 05C0h
5C4h	8	GLOBAL_CTRL_CMPSSB7_HALTEN	502F 05C4h
5C8h	8	GLOBAL_CTRL_CMPSSB8_HALTEN	502F 05C8h
5CCh	8	GLOBAL_CTRL_CMPSSB9_HALTEN	502F 05CCh
5D0h	8	GLOBAL_CTRL_ECAP0_HALTEN	502F 05D0h
5D4h	8	GLOBAL_CTRL_ECAP1_HALTEN	502F 05D4h
5D8h	8	GLOBAL_CTRL_ECAP2_HALTEN	502F 05D8h
5DCh	8	GLOBAL_CTRL_ECAP3_HALTEN	502F 05DCh
5E0h	8	GLOBAL_CTRL_ECAP4_HALTEN	502F 05E0h
5E4h	8	GLOBAL_CTRL_ECAP5_HALTEN	502F 05E4h
5E8h	8	GLOBAL_CTRL_ECAP6_HALTEN	502F 05E8h
5ECh	8	GLOBAL_CTRL_ECAP7_HALTEN	502F 05ECh
5F0h	8	GLOBAL_CTRL_ECAP8_HALTEN	502F 05F0h

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Table 3-790. CONTROLSS_GLOBAL_CTRL Register Base Address Table (continued)

Offset	Length	Register Name	CONTROLSS_GLOBAL_CTRL Physical Address
5F4h	8	GLOBAL_CTRL_ECAP9_HALTEN	502F 05F4h
5F8h	8	GLOBAL_CTRL_EQEP0_HALTEN	502F 05F8h
5FCh	8	GLOBAL_CTRL_EQEP1_HALTEN	502F 05FCh
600h	8	GLOBAL_CTRL_EQEP2_HALTEN	502F 0600h
1008h	32	GLOBAL_CTRL_LOCK0_KICK0	502F 1008h
100Ch	32	GLOBAL_CTRL_LOCK0_KICK1	502F 100Ch
1010h	8	GLOBAL_CTRL_INTR_RAW_STATUS	502F 1010h
1014h	8	GLOBAL_CTRL_INTR_ENABLED_STATUS_CLEAR	502F 1014h
1018h	8	GLOBAL_CTRL_INTR_ENABLE	502F 1018h
101Ch	8	GLOBAL_CTRL_INTR_ENABLE_CLEAR	502F 101Ch
1020h	8	GLOBAL_CTRL_EOI	502F 1020h
1024h	32	GLOBAL_CTRL_FAULT_ADDRESS	502F 1024h
1028h	8	GLOBAL_CTRL_FAULT_TYPE_STATUS	502F 1028h
102Ch	32	GLOBAL_CTRL_FAULT_ATTR_STATUS	502F 102Ch
1030h	0	GLOBAL_CTRL_FAULT_CLEAR	502F 1030h

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3.13.1 CONTROLSS_GLOBAL_CTRL_PID Registers

3.13.1.1 GLOBAL_CTRL_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

Return to Summary Table

Table 3-791. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0000h

Access Types Legend

Table 3-792. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	640B657B5780h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	Ah	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	2774h	Not Defined

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3.13.2 CONTROLSS_GLOBAL_CTRL_EPWM_STATICXBAR_SEL0 Registers

3.13.2.1 GLOBAL_CTRL_EPWM_STATICXBAR_SEL0 Register (Offset = 4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-793. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0004h

Access Types Legend

Table 3-794. EPWM_STATICXBAR_SEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	ETPWM15	RW	0h	ETPWM15 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
29 - 28	ETPWM14	RW	0h	ETPWM14 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
27 - 26	ETPWM13	RW	0h	ETPWM13 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
25 - 24	ETPWM12	RW	0h	ETPWM12 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
23 - 22	ETPWM11	RW	0h	ETPWM11 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
21 - 20	ETPWM10	RW	0h	ETPWM10 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
19 - 18	ETPWM9	RW	0h	ETPWM9 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
17 - 16	ETPWM8	RW	0h	ETPWM8 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
15 - 14	ETPWM7	RW	0h	ETPWM7 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
13 - 12	ETPWM6	RW	0h	ETPWM6 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
11 - 10	ETPWM5	RW	0h	ETPWM5 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
9 - 8	ETPWM4	RW	0h	ETPWM4 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
7 - 6	ETPWM3	RW	0h	ETPWM3 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
5 - 4	ETPWM2	RW	0h	ETPWM2 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
3 - 2	ETPWM1	RW	0h	ETPWM1 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
1 - 0	ETPWM0	RW	0h	ETPWM0 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3

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3.13.3 CONTROLSS_GLOBAL_CTRL_EPWM_STATICXBAR_SEL1 Registers

3.13.3.1 GLOBAL_CTRL_EPWM_STATICXBAR_SEL1 Register (Offset = 8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-795. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0008h

Access Types Legend

Table 3-796. EPWM_STATICXBAR_SEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	ETPWM31	RW	0h	ETPWM31 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
29 - 28	ETPWM30	RW	0h	ETPWM30 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
27 - 26	ETPWM29	RW	0h	ETPWM29 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
25 - 24	ETPWM28	RW	0h	ETPWM28 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
23 - 22	ETPWM27	RW	0h	ETPWM27 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
21 - 20	ETPWM26	RW	0h	ETPWM26 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
19 - 18	ETPWM25	RW	0h	ETPWM25 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
17 - 16	ETPWM24	RW	0h	ETPWM24 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
15 - 14	ETPWM23	RW	0h	ETPWM23 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
13 - 12	ETPWM22	RW	0h	ETPWM22 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
11 - 10	ETPWM21	RW	0h	ETPWM21 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
9 - 8	ETPWM20	RW	0h	ETPWM20 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
7 - 6	ETPWM19	RW	0h	ETPWM19 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
5 - 4	ETPWM18	RW	0h	ETPWM18 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
3 - 2	ETPWM17	RW	0h	ETPWM17 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3
1 - 0	ETPWM16	RW	0h	ETPWM16 access from PCR grouping - 00 = G0, 01 = G1, 01 = G2, 11 = G3

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3.13.4 CONTROLSS_GLOBAL_CTRL_EPWM_CLKSYNC Registers

3.13.4.1 GLOBAL_CTRL_EPWM_CLKSYNC Register (Offset = 10h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-797. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0010h

Access Types Legend

Table 3-798. EPWM_CLKSYNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	BIT	RW	0h	ETPWM clock sync for each EPWM instance1: will allow CLK SYNC when GBCLKSYNC is written in0: No CLK SYNC when GBCLKSYNC is written in

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3.13.5 CONTROLSS_GLOBAL_CTRL_SDFM1_CLK0_SEL Registers

3.13.5.1 GLOBAL_CTRL_SDFM1_CLK0_SEL Register (Offset = 18h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-799. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0018h

Access Types Legend

Table 3-800. SDFM1_CLK0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	SEL	RW	0h	SDFM1 clock CK0 select0: source is SDFM1 CK0 from Pinmux1: source is SDFM0 CK0 from Pinmux

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3.13.6 CONTROLSS_GLOBAL_CTRL_EMUSTOPN_MASK Registers

3.13.6.1 GLOBAL_CTRL_EMUSTOPN_MASK Register (Offset = 20h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-801. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0020h

Access Types Legend

Table 3-802. EMUSTOPN_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	Bit-mask for debug suspend cpu cores to EPWM0: CR5B1 enabled to control EMUSTOPn1: CR5B1 disabled to control EMUSTOPn
2	CR5A1	RW	0h	Bit-mask for debug suspend cpu cores to EPWM0: CR5A1 enabled to control EMUSTOPn1: CR5A1 disabled to control EMUSTOPn
1	CR5B0	RW	0h	Bit-mask for debug suspend cpu cores to EPWM0: CR5B0 enabled to control EMUSTOPn1: CR5B0 disabled to control EMUSTOPn
0	CR5A0	RW	0h	Bit-mask for debug suspend cpu cores to EPWM0: CR5A0 enabled to control EMUSTOPn1: CR5A0 disabled to control EMUSTOPn

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3.13.7 CONTROLSS_GLOBAL_CTRL_CLB_AQ_EN0 Registers

3.13.7.1 GLOBAL_CTRL_CLB_AQ_EN0 Register (Offset = 28h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-803. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0028h

Access Types Legend

Table 3-804. CLB_AQ_EN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ENABLE	RW	0h	Enable ICCS control to CLB_AQ signal of PWM[15:0]

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3.13.8 CONTROLSS_GLOBAL_CTRL_CLB_AQ_EN1 Registers

3.13.8.1 GLOBAL_CTRL_CLB_AQ_EN1 Register (Offset = 30h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-805. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0030h

Access Types Legend

Table 3-806. CLB_AQ_EN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ENABLE	RW	0h	Enable ICCS control to CLB_AQ signal of PWM[31:16]

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3.13.9 CONTROLSS_GLOBAL_CTRL_CLB_DB_EN0 Registers

3.13.9.1 GLOBAL_CTRL_CLB_DB_EN0 Register (Offset = 38h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-807. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0038h

Access Types Legend

Table 3-808. CLB_DB_EN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ENABLE	RW	0h	Enable ICCS control to CLB_DB signal of PWM[15:0]

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3.13.10 CONTROLSS_GLOBAL_CTRL_CLB_DB_EN1 Registers

3.13.10.1 GLOBAL_CTRL_CLB_DB_EN1 Register (Offset = 40h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-809. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0040h

Access Types Legend

Table 3-810. CLB_DB_EN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ENABLE	RW	0h	Enable ICCS control to CLB_DB signal of PWM[31:16]

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3.13.11 CONTROLSS_GLOBAL_CTRL_ETPWM0_CLK_GATE Registers

3.13.11.1 GLOBAL_CTRL_ETPWM0_CLK_GATE Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-811. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0100h

Access Types Legend

Table 3-812. ETPWM0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.12 CONTROLSS_GLOBAL_CTRL_ETPWM1_CLK_GATE Registers

3.13.12.1 GLOBAL_CTRL_ETPWM1_CLK_GATE Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-813. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0104h

Access Types Legend

Table 3-814. ETPWM1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.13 CONTROLSS_GLOBAL_CTRL_ETPWM2_CLK_GATE Registers

3.13.13.1 GLOBAL_CTRL_ETPWM2_CLK_GATE Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-815. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0108h

Access Types Legend

Table 3-816. ETPWM2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.14 CONTROLSS_GLOBAL_CTRL_ETPWM3_CLK_GATE Registers

3.13.14.1 GLOBAL_CTRL_ETPWM3_CLK_GATE Register (Offset = 10Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-817. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 010Ch

Access Types Legend

Table 3-818. ETPWM3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.15 CONTROLSS_GLOBAL_CTRL_ETPWM4_CLK_GATE Registers

3.13.15.1 GLOBAL_CTRL_ETPWM4_CLK_GATE Register (Offset = 110h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-819. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0110h

Access Types Legend

Table 3-820. ETPWM4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.16 CONTROLSS_GLOBAL_CTRL_ETPWM5_CLK_GATE Registers

3.13.16.1 GLOBAL_CTRL_ETPWM5_CLK_GATE Register (Offset = 114h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-821. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0114h

Access Types Legend

Table 3-822. ETPWM5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.17 CONTROLSS_GLOBAL_CTRL_ETPWM6_CLK_GATE Registers

3.13.17.1 GLOBAL_CTRL_ETPWM6_CLK_GATE Register (Offset = 118h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-823. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0118h

Access Types Legend

Table 3-824. ETPWM6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.18 CONTROLSS_GLOBAL_CTRL_ETPWM7_CLK_GATE Registers

3.13.18.1 GLOBAL_CTRL_ETPWM7_CLK_GATE Register (Offset = 11Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-825. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 011Ch

Access Types Legend

Table 3-826. ETPWM7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.19 CONTROLSS_GLOBAL_CTRL_ETPWM8_CLK_GATE Registers

3.13.19.1 GLOBAL_CTRL_ETPWM8_CLK_GATE Register (Offset = 120h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-827. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0120h

Access Types Legend

Table 3-828. ETPWM8_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.20 CONTROLSS_GLOBAL_CTRL_ETPWM9_CLK_GATE Registers

3.13.20.1 GLOBAL_CTRL_ETPWM9_CLK_GATE Register (Offset = 124h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-829. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0124h

Access Types Legend

Table 3-830. ETPWM9_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.21 CONTROLSS_GLOBAL_CTRL_ETPWM10_CLK_GATE Registers

3.13.21.1 GLOBAL_CTRL_ETPWM10_CLK_GATE Register (Offset = 128h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-831. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0128h

Access Types Legend

Table 3-832. ETPWM10_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.22 CONTROLSS_GLOBAL_CTRL_ETPWM11_CLK_GATE Registers

3.13.22.1 GLOBAL_CTRL_ETPWM11_CLK_GATE Register (Offset = 12Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-833. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 012Ch

Access Types Legend

Table 3-834. ETPWM11_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.23 CONTROLSS_GLOBAL_CTRL_ETPWM12_CLK_GATE Registers

3.13.23.1 GLOBAL_CTRL_ETPWM12_CLK_GATE Register (Offset = 130h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-835. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0130h

Access Types Legend

Table 3-836. ETPWM12_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.24 CONTROLSS_GLOBAL_CTRL_ETPWM13_CLK_GATE Registers

3.13.24.1 GLOBAL_CTRL_ETPWM13_CLK_GATE Register (Offset = 134h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-837. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0134h

Access Types Legend

Table 3-838. ETPWM13_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.25 CONTROLSS_GLOBAL_CTRL_ETPWM14_CLK_GATE Registers

3.13.25.1 GLOBAL_CTRL_ETPWM14_CLK_GATE Register (Offset = 138h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-839. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0138h

Access Types Legend

Table 3-840. ETPWM14_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.26 CONTROLSS_GLOBAL_CTRL_ETPWM15_CLK_GATE Registers

3.13.26.1 GLOBAL_CTRL_ETPWM15_CLK_GATE Register (Offset = 13Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-841. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 013Ch

Access Types Legend

Table 3-842. ETPWM15_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.27 CONTROLSS_GLOBAL_CTRL_ETPWM16_CLK_GATE Registers

3.13.27.1 GLOBAL_CTRL_ETPWM16_CLK_GATE Register (Offset = 140h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-843. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0140h

Access Types Legend

Table 3-844. ETPWM16_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.28 CONTROLSS_GLOBAL_CTRL_ETPWM17_CLK_GATE Registers

3.13.28.1 GLOBAL_CTRL_ETPWM17_CLK_GATE Register (Offset = 144h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-845. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0144h

Access Types Legend

Table 3-846. ETPWM17_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.29 CONTROLSS_GLOBAL_CTRL_ETPWM18_CLK_GATE Registers

3.13.29.1 GLOBAL_CTRL_ETPWM18_CLK_GATE Register (Offset = 148h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-847. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0148h

Access Types Legend

Table 3-848. ETPWM18_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.30 CONTROLSS_GLOBAL_CTRL_ETPWM19_CLK_GATE Registers

3.13.30.1 GLOBAL_CTRL_ETPWM19_CLK_GATE Register (Offset = 14Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-849. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 014Ch

Access Types Legend

Table 3-850. ETPWM19_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.31 CONTROLSS_GLOBAL_CTRL_ETPWM20_CLK_GATE Registers

3.13.31.1 GLOBAL_CTRL_ETPWM20_CLK_GATE Register (Offset = 150h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-851. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0150h

Access Types Legend

Table 3-852. ETPWM20_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.32 CONTROLSS_GLOBAL_CTRL_ETPWM21_CLK_GATE Registers

3.13.32.1 GLOBAL_CTRL_ETPWM21_CLK_GATE Register (Offset = 154h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-853. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0154h

Access Types Legend

Table 3-854. ETPWM21_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.33 CONTROLSS_GLOBAL_CTRL_ETPWM22_CLK_GATE Registers

3.13.33.1 GLOBAL_CTRL_ETPWM22_CLK_GATE Register (Offset = 158h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-855. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0158h

Access Types Legend

Table 3-856. ETPWM22_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.34 CONTROLSS_GLOBAL_CTRL_ETPWM23_CLK_GATE Registers

3.13.34.1 GLOBAL_CTRL_ETPWM23_CLK_GATE Register (Offset = 15Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-857. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 015Ch

Access Types Legend

Table 3-858. ETPWM23_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.35 CONTROLSS_GLOBAL_CTRL_ETPWM24_CLK_GATE Registers

3.13.35.1 GLOBAL_CTRL_ETPWM24_CLK_GATE Register (Offset = 160h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-859. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0160h

Access Types Legend

Table 3-860. ETPWM24_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.36 CONTROLSS_GLOBAL_CTRL_ETPWM25_CLK_GATE Registers

3.13.36.1 GLOBAL_CTRL_ETPWM25_CLK_GATE Register (Offset = 164h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-861. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0164h

Access Types Legend

Table 3-862. ETPWM25_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.37 CONTROLSS_GLOBAL_CTRL_ETPWM26_CLK_GATE Registers

3.13.37.1 GLOBAL_CTRL_ETPWM26_CLK_GATE Register (Offset = 168h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-863. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0168h

Access Types Legend

Table 3-864. ETPWM26_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.38 CONTROLSS_GLOBAL_CTRL_ETPWM27_CLK_GATE Registers

3.13.38.1 GLOBAL_CTRL_ETPWM27_CLK_GATE Register (Offset = 16Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-865. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 016Ch

Access Types Legend

Table 3-866. ETPWM27_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.39 CONTROLSS_GLOBAL_CTRL_ETPWM28_CLK_GATE Registers

3.13.39.1 GLOBAL_CTRL_ETPWM28_CLK_GATE Register (Offset = 170h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-867. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0170h

Access Types Legend

Table 3-868. ETPWM28_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.40 CONTROLSS_GLOBAL_CTRL_ETPWM29_CLK_GATE Registers

3.13.40.1 GLOBAL_CTRL_ETPWM29_CLK_GATE Register (Offset = 174h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-869. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0174h

Access Types Legend

Table 3-870. ETPWM29_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.41 CONTROLSS_GLOBAL_CTRL_ETPWM30_CLK_GATE Registers

3.13.41.1 GLOBAL_CTRL_ETPWM30_CLK_GATE Register (Offset = 178h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-871. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0178h

Access Types Legend

Table 3-872. ETPWM30_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.42 CONTROLSS_GLOBAL_CTRL_ETPWM31_CLK_GATE Registers

3.13.42.1 GLOBAL_CTRL_ETPWM31_CLK_GATE Register (Offset = 17Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-873. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 017Ch

Access Types Legend

Table 3-874. ETPWM31_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding etpwm

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3.13.43 CONTROLSS_GLOBAL_CTRL_FSI_TX0_CLK_GATE Registers

3.13.43.1 GLOBAL_CTRL_FSI_TX0_CLK_GATE Register (Offset = 180h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-875. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0180h

Access Types Legend

Table 3-876. FSI_TX0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi_tx

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3.13.44 CONTROLSS_GLOBAL_CTRL_FSI_TX1_CLK_GATE Registers

3.13.44.1 GLOBAL_CTRL_FSI_TX1_CLK_GATE Register (Offset = 184h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-877. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0184h

Access Types Legend

Table 3-878. FSI_TX1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi_tx

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3.13.45 CONTROLSS_GLOBAL_CTRL_FSI_TX2_CLK_GATE Registers

3.13.45.1 GLOBAL_CTRL_FSI_TX2_CLK_GATE Register (Offset = 188h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-879. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0188h

Access Types Legend

Table 3-880. FSI_TX2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi_tx

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3.13.46 CONTROLSS_GLOBAL_CTRL_FSI_TX3_CLK_GATE Registers

3.13.46.1 GLOBAL_CTRL_FSI_TX3_CLK_GATE Register (Offset = 18Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-881. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 018Ch

Access Types Legend

Table 3-882. FSI_TX3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi_tx

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3.13.47 CONTROLSS_GLOBAL_CTRL_FSI_RX0_CLK_GATE Registers

3.13.47.1 GLOBAL_CTRL_FSI_RX0_CLK_GATE Register (Offset = 190h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-883. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0190h

Access Types Legend

Table 3-884. FSI_RX0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi_rx

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3.13.48 CONTROLSS_GLOBAL_CTRL_FSI_RX1_CLK_GATE Registers

3.13.48.1 GLOBAL_CTRL_FSI_RX1_CLK_GATE Register (Offset = 194h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-885. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0194h

Access Types Legend

Table 3-886. FSI_RX1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi_rx

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3.13.49 CONTROLSS_GLOBAL_CTRL_FSI_RX2_CLK_GATE Registers

3.13.49.1 GLOBAL_CTRL_FSI_RX2_CLK_GATE Register (Offset = 198h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-887. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0198h

Access Types Legend

Table 3-888. FSI_RX2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi_rx

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3.13.50 CONTROLSS_GLOBAL_CTRL_CMPSSA0_CLK_GATE Registers

3.13.50.1 GLOBAL_CTRL_CMPSSA0_CLK_GATE Register (Offset = 1A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-889. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01A0h

Access Types Legend

Table 3-890. CMPSSA0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

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3.13.51 CONTROLSS_GLOBAL_CTRL_CMPSSA1_CLK_GATE Registers

3.13.51.1 GLOBAL_CTRL_CMPSSA1_CLK_GATE Register (Offset = 1A4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-891. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01A4h

Access Types Legend

Table 3-892. CMPSSA1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

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3.13.52 CONTROLSS_GLOBAL_CTRL_CMPSSA2_CLK_GATE Registers

3.13.52.1 GLOBAL_CTRL_CMPSSA2_CLK_GATE Register (Offset = 1A8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-893. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01A8h

Access Types Legend

Table 3-894. CMPSSA2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

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3.13.53 CONTROLSS_GLOBAL_CTRL_CMPSSA3_CLK_GATE Registers

3.13.53.1 GLOBAL_CTRL_CMPSSA3_CLK_GATE Register (Offset = 1ACh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-895. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01ACh

Access Types Legend

Table 3-896. CMPSSA3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

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3.13.54 CONTROLSS_GLOBAL_CTRL_CMPSSA4_CLK_GATE Registers

3.13.54.1 GLOBAL_CTRL_CMPSSA4_CLK_GATE Register (Offset = 1B0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-897. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01B0h

Access Types Legend

Table 3-898. CMPSSA4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

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3.13.55 CONTROLSS_GLOBAL_CTRL_CMPSSA5_CLK_GATE Registers

3.13.55.1 GLOBAL_CTRL_CMPSSA5_CLK_GATE Register (Offset = 1B4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-899. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01B4h

Access Types Legend

Table 3-900. CMPSSA5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

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3.13.56 CONTROLSS_GLOBAL_CTRL_CMPSSA6_CLK_GATE Registers

3.13.56.1 GLOBAL_CTRL_CMPSSA6_CLK_GATE Register (Offset = 1B8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-901. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01B8h

Access Types Legend

Table 3-902. CMPSSA6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

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3.13.57 CONTROLSS_GLOBAL_CTRL_CMPSSA7_CLK_GATE Registers

3.13.57.1 GLOBAL_CTRL_CMPSSA7_CLK_GATE Register (Offset = 1BCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-903. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01BCh

Access Types Legend

Table 3-904. CMPSSA7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

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3.13.58 CONTROLSS_GLOBAL_CTRL_CMPSSA8_CLK_GATE Registers

3.13.58.1 GLOBAL_CTRL_CMPSSA8_CLK_GATE Register (Offset = 1C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-905. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01C0h

Access Types Legend

Table 3-906. CMPSSA8_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

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3.13.59 CONTROLSS_GLOBAL_CTRL_CMPSSA9_CLK_GATE Registers

3.13.59.1 GLOBAL_CTRL_CMPSSA9_CLK_GATE Register (Offset = 1C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-907. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01C4h

Access Types Legend

Table 3-908. CMPSSA9_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss12b

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3.13.60 CONTROLSS_GLOBAL_CTRL_CMPSSB0_CLK_GATE Registers

3.13.60.1 GLOBAL_CTRL_CMPSSB0_CLK_GATE Register (Offset = 1D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-909. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01D0h

Access Types Legend

Table 3-910. CMPSSB0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

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3.13.61 CONTROLSS_GLOBAL_CTRL_CMPSSB1_CLK_GATE Registers

3.13.61.1 GLOBAL_CTRL_CMPSSB1_CLK_GATE Register (Offset = 1D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-911. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01D4h

Access Types Legend

Table 3-912. CMPSSB1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

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3.13.62 CONTROLSS_GLOBAL_CTRL_CMPSSB2_CLK_GATE Registers

3.13.62.1 GLOBAL_CTRL_CMPSSB2_CLK_GATE Register (Offset = 1D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-913. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01D8h

Access Types Legend

Table 3-914. CMPSSB2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

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3.13.63 CONTROLSS_GLOBAL_CTRL_CMPSSB3_CLK_GATE Registers

3.13.63.1 GLOBAL_CTRL_CMPSSB3_CLK_GATE Register (Offset = 1DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-915. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01DCh

Access Types Legend

Table 3-916. CMPSSB3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

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3.13.64 CONTROLSS_GLOBAL_CTRL_CMPSSB4_CLK_GATE Registers

3.13.64.1 GLOBAL_CTRL_CMPSSB4_CLK_GATE Register (Offset = 1E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-917. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01E0h

Access Types Legend

Table 3-918. CMPSSB4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

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3.13.65 CONTROLSS_GLOBAL_CTRL_CMPSSB5_CLK_GATE Registers

3.13.65.1 GLOBAL_CTRL_CMPSSB5_CLK_GATE Register (Offset = 1E4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-919. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01E4h

Access Types Legend

Table 3-920. CMPSSB5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

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3.13.66 CONTROLSS_GLOBAL_CTRL_CMPSSB6_CLK_GATE Registers

3.13.66.1 GLOBAL_CTRL_CMPSSB6_CLK_GATE Register (Offset = 1E8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-921. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01E8h

Access Types Legend

Table 3-922. CMPSSB6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

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3.13.67 CONTROLSS_GLOBAL_CTRL_CMPSSB7_CLK_GATE Registers

3.13.67.1 GLOBAL_CTRL_CMPSSB7_CLK_GATE Register (Offset = 1ECh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-923. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01ECh

Access Types Legend

Table 3-924. CMPSSB7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

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3.13.68 CONTROLSS_GLOBAL_CTRL_CMPSSB8_CLK_GATE Registers

3.13.68.1 GLOBAL_CTRL_CMPSSB8_CLK_GATE Register (Offset = 1F0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-925. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01F0h

Access Types Legend

Table 3-926. CMPSSB8_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

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3.13.69 CONTROLSS_GLOBAL_CTRL_CMPSSB9_CLK_GATE Registers

3.13.69.1 GLOBAL_CTRL_CMPSSB9_CLK_GATE Register (Offset = 1F4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-927. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 01F4h

Access Types Legend

Table 3-928. CMPSSB9_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding cmpss8b

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3.13.70 CONTROLSS_GLOBAL_CTRL_ECAP0_CLK_GATE Registers

3.13.70.1 GLOBAL_CTRL_ECAP0_CLK_GATE Register (Offset = 200h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-929. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0200h

Access Types Legend

Table 3-930. ECAP0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

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3.13.71 CONTROLSS_GLOBAL_CTRL_ECAP1_CLK_GATE Registers

3.13.71.1 GLOBAL_CTRL_ECAP1_CLK_GATE Register (Offset = 204h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-931. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0204h

Access Types Legend

Table 3-932. ECAP1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

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3.13.72 CONTROLSS_GLOBAL_CTRL_ECAP2_CLK_GATE Registers

3.13.72.1 GLOBAL_CTRL_ECAP2_CLK_GATE Register (Offset = 208h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-933. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0208h

Access Types Legend

Table 3-934. ECAP2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

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3.13.73 CONTROLSS_GLOBAL_CTRL_ECAP3_CLK_GATE Registers

3.13.73.1 GLOBAL_CTRL_ECAP3_CLK_GATE Register (Offset = 20Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-935. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 020Ch

Access Types Legend

Table 3-936. ECAP3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

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3.13.74 CONTROLSS_GLOBAL_CTRL_ECAP4_CLK_GATE Registers

3.13.74.1 GLOBAL_CTRL_ECAP4_CLK_GATE Register (Offset = 210h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-937. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0210h

Access Types Legend

Table 3-938. ECAP4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

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3.13.75 CONTROLSS_GLOBAL_CTRL_ECAP5_CLK_GATE Registers

3.13.75.1 GLOBAL_CTRL_ECAP5_CLK_GATE Register (Offset = 214h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-939. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0214h

Access Types Legend

Table 3-940. ECAP5_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

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3.13.76 CONTROLSS_GLOBAL_CTRL_ECAP6_CLK_GATE Registers

3.13.76.1 GLOBAL_CTRL_ECAP6_CLK_GATE Register (Offset = 218h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-941. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0218h

Access Types Legend

Table 3-942. ECAP6_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

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3.13.77 CONTROLSS_GLOBAL_CTRL_FSI_RX3_CLK_GATE Registers

3.13.77.1 GLOBAL_CTRL_FSI_RX3_CLK_GATE Register (Offset = 19Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-943. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 019Ch

Access Types Legend

Table 3-944. FSI_RX3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi_rx

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3.13.78 CONTROLSS_GLOBAL_CTRL_ECAP7_CLK_GATE Registers

3.13.78.1 GLOBAL_CTRL_ECAP7_CLK_GATE Register (Offset = 21Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-945. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 021Ch

Access Types Legend

Table 3-946. ECAP7_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

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3.13.79 CONTROLSS_GLOBAL_CTRL_ECAP8_CLK_GATE Registers

3.13.79.1 GLOBAL_CTRL_ECAP8_CLK_GATE Register (Offset = 220h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-947. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0220h

Access Types Legend

Table 3-948. ECAP8_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

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3.13.80 CONTROLSS_GLOBAL_CTRL_ECAP9_CLK_GATE Registers

3.13.80.1 GLOBAL_CTRL_ECAP9_CLK_GATE Register (Offset = 224h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-949. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0224h

Access Types Legend

Table 3-950. ECAP9_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding ecap

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3.13.81 CONTROLSS_GLOBAL_CTRL_EQEP0_CLK_GATE Registers

3.13.81.1 GLOBAL_CTRL_EQEP0_CLK_GATE Register (Offset = 240h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-951. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0240h

Access Types Legend

Table 3-952. EQEP0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding eqep

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3.13.82 CONTROLSS_GLOBAL_CTRL_EQEP1_CLK_GATE Registers

3.13.82.1 GLOBAL_CTRL_EQEP1_CLK_GATE Register (Offset = 244h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-953. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0244h

Access Types Legend

Table 3-954. EQEP1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding eqep

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3.13.83 CONTROLSS_GLOBAL_CTRL_EQEP2_CLK_GATE Registers

3.13.83.1 GLOBAL_CTRL_EQEP2_CLK_GATE Register (Offset = 248h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-955. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0248h

Access Types Legend

Table 3-956. EQEP2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding eqep

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3.13.84 CONTROLSS_GLOBAL_CTRL_SDFM0_CLK_GATE Registers

3.13.84.1 GLOBAL_CTRL_SDFM0_CLK_GATE Register (Offset = 250h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-957. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0250h

Access Types Legend

Table 3-958. SDFM0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding sdfm

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3.13.85 CONTROLSS_GLOBAL_CTRL_SDFM1_CLK_GATE Registers

3.13.85.1 GLOBAL_CTRL_SDFM1_CLK_GATE Register (Offset = 254h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-959. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0254h

Access Types Legend

Table 3-960. SDFM1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding sdfm

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3.13.86 CONTROLSS_GLOBAL_CTRL_DAC_CLK_GATE Registers

3.13.86.1 GLOBAL_CTRL_DAC_CLK_GATE Register (Offset = 258h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-961. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0258h

Access Types Legend

Table 3-962. DAC_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for dac

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3.13.87 CONTROLSS_GLOBAL_CTRL_ADC0_CLK_GATE Registers

3.13.87.1 GLOBAL_CTRL_ADC0_CLK_GATE Register (Offset = 25Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-963. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 025Ch

Access Types Legend

Table 3-964. ADC0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding adc

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3.13.88 CONTROLSS_GLOBAL_CTRL_ADC1_CLK_GATE Registers

3.13.88.1 GLOBAL_CTRL_ADC1_CLK_GATE Register (Offset = 260h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-965. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0260h

Access Types Legend

Table 3-966. ADC1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding adc

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3.13.89 CONTROLSS_GLOBAL_CTRL_ADC2_CLK_GATE Registers

3.13.89.1 GLOBAL_CTRL_ADC2_CLK_GATE Register (Offset = 264h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-967. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0264h

Access Types Legend

Table 3-968. ADC2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding adc

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3.13.90 CONTROLSS_GLOBAL_CTRL_ADC3_CLK_GATE Registers

3.13.90.1 GLOBAL_CTRL_ADC3_CLK_GATE Register (Offset = 268h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-969. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0268h

Access Types Legend

Table 3-970. ADC3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding adc

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3.13.91 CONTROLSS_GLOBAL_CTRL_ADC4_CLK_GATE Registers

3.13.91.1 GLOBAL_CTRL_ADC4_CLK_GATE Register (Offset = 26Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-971. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 026Ch

Access Types Legend

Table 3-972. ADC4_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding adc

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3.13.92 CONTROLSS_GLOBAL_CTRL_OTTO0_CLK_GATE Registers

3.13.92.1 GLOBAL_CTRL_OTTO0_CLK_GATE Register (Offset = 270h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-973. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0270h

Access Types Legend

Table 3-974. OTTO0_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding otto

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3.13.93 CONTROLSS_GLOBAL_CTRL_OTTO1_CLK_GATE Registers

3.13.93.1 GLOBAL_CTRL_OTTO1_CLK_GATE Register (Offset = 274h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-975. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0274h

Access Types Legend

Table 3-976. OTTO1_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding otto

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3.13.94 CONTROLSS_GLOBAL_CTRL_OTTO2_CLK_GATE Registers

3.13.94.1 GLOBAL_CTRL_OTTO2_CLK_GATE Register (Offset = 278h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-977. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0278h

Access Types Legend

Table 3-978. OTTO2_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding otto

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3.13.95 CONTROLSS_GLOBAL_CTRL_OTTO3_CLK_GATE Registers

3.13.95.1 GLOBAL_CTRL_OTTO3_CLK_GATE Register (Offset = 27Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-979. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 027Ch

Access Types Legend

Table 3-980. OTTO3_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding otto

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3.13.96 CONTROLSS_GLOBAL_CTRL_SDFM0_PLL_CLK_GATE Registers

3.13.96.1 GLOBAL_CTRL_SDFM0_PLL_CLK_GATE Register (Offset = 280h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-981. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0280h

Access Types Legend

Table 3-982. SDFM0_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding sdfm pll clock

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3.13.97 CONTROLSS_GLOBAL_CTRL_SDFM1_PLL_CLK_GATE Registers

3.13.97.1 GLOBAL_CTRL_SDFM1_PLL_CLK_GATE Register (Offset = 284h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-983. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0284h

Access Types Legend

Table 3-984. SDFM1_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding sdfm pll clock

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3.13.98 CONTROLSS_GLOBAL_CTRL_FSI_TX0_PLL_CLK_GATE Registers

3.13.98.1 GLOBAL_CTRL_FSI_TX0_PLL_CLK_GATE Register (Offset = 288h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-985. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0288h

Access Types Legend

Table 3-986. FSI_TX0_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi rx pll clock

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3.13.99 CONTROLSS_GLOBAL_CTRL_FSI_TX1_PLL_CLK_GATE Registers

3.13.99.1 GLOBAL_CTRL_FSI_TX1_PLL_CLK_GATE Register (Offset = 28Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-987. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 028Ch

Access Types Legend

Table 3-988. FSI_TX1_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi rx pll clock

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3.13.100 CONTROLSS_GLOBAL_CTRL_FSI_TX2_PLL_CLK_GATE Registers

3.13.100.1 GLOBAL_CTRL_FSI_TX2_PLL_CLK_GATE Register (Offset = 290h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-989. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0290h

Access Types Legend

Table 3-990. FSI_TX2_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi rx pll clock

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3.13.101 CONTROLSS_GLOBAL_CTRL_FSI_TX3_PLL_CLK_GATE Registers

3.13.101.1 GLOBAL_CTRL_FSI_TX3_PLL_CLK_GATE Register (Offset = 294h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-991. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0294h

Access Types Legend

Table 3-992. FSI_TX3_PLL_CLK_GATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	CLK_GATE	RW	0h	writing '111' will gate clock for corresponding fsi rx pll clock

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3.13.102 CONTROLSS_GLOBAL_CTRL_ETPWM0_RST Registers

3.13.102.1 GLOBAL_CTRL_ETPWM0_RST Register (Offset = 300h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-993. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0300h

Access Types Legend

Table 3-994. ETPWM0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.103 CONTROLSS_GLOBAL_CTRL_ETPWM1_RST Registers

3.13.103.1 GLOBAL_CTRL_ETPWM1_RST Register (Offset = 304h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-995. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0304h

Access Types Legend

Table 3-996. ETPWM1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.104 CONTROLSS_GLOBAL_CTRL_ETPWM2_RST Registers

3.13.104.1 GLOBAL_CTRL_ETPWM2_RST Register (Offset = 308h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-997. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0308h

Access Types Legend

Table 3-998. ETPWM2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.105 CONTROLSS_GLOBAL_CTRL_ETPWM3_RST Registers

3.13.105.1 GLOBAL_CTRL_ETPWM3_RST Register (Offset = 30Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-999. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 030Ch

Access Types Legend

Table 3-1000. ETPWM3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.106 CONTROLSS_GLOBAL_CTRL_ETPWM4_RST Registers

3.13.106.1 GLOBAL_CTRL_ETPWM4_RST Register (Offset = 310h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1001. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0310h

Access Types Legend

Table 3-1002. ETPWM4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.107 CONTROLSS_GLOBAL_CTRL_ETPWM5_RST Registers

3.13.107.1 GLOBAL_CTRL_ETPWM5_RST Register (Offset = 314h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1003. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0314h

Access Types Legend

Table 3-1004. ETPWM5_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.108 CONTROLSS_GLOBAL_CTRL_ETPWM6_RST Registers

3.13.108.1 GLOBAL_CTRL_ETPWM6_RST Register (Offset = 318h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1005. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0318h

Access Types Legend

Table 3-1006. ETPWM6_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.109 CONTROLSS_GLOBAL_CTRL_ETPWM7_RST Registers

3.13.109.1 GLOBAL_CTRL_ETPWM7_RST Register (Offset = 31Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1007. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 031Ch

Access Types Legend

Table 3-1008. ETPWM7_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.110 CONTROLSS_GLOBAL_CTRL_ETPWM8_RST Registers

3.13.110.1 GLOBAL_CTRL_ETPWM8_RST Register (Offset = 320h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1009. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0320h

Access Types Legend

Table 3-1010. ETPWM8_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.111 CONTROLSS_GLOBAL_CTRL_ETPWM9_RST Registers

3.13.111.1 GLOBAL_CTRL_ETPWM9_RST Register (Offset = 324h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1011. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0324h

Access Types Legend

Table 3-1012. ETPWM9_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.112 CONTROLSS_GLOBAL_CTRL_ETPWM10_RST Registers

3.13.112.1 GLOBAL_CTRL_ETPWM10_RST Register (Offset = 328h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1013. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0328h

Access Types Legend

Table 3-1014. ETPWM10_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.113 CONTROLSS_GLOBAL_CTRL_ETPWM11_RST Registers

3.13.113.1 GLOBAL_CTRL_ETPWM11_RST Register (Offset = 32Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1015. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 032Ch

Access Types Legend

Table 3-1016. ETPWM11_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.114 CONTROLSS_GLOBAL_CTRL_ETPWM12_RST Registers

3.13.114.1 GLOBAL_CTRL_ETPWM12_RST Register (Offset = 330h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1017. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0330h

Access Types Legend

Table 3-1018. ETPWM12_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.115 CONTROLSS_GLOBAL_CTRL_ETPWM13_RST Registers

3.13.115.1 GLOBAL_CTRL_ETPWM13_RST Register (Offset = 334h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1019. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0334h

Access Types Legend

Table 3-1020. ETPWM13_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.116 CONTROLSS_GLOBAL_CTRL_ETPWM14_RST Registers

3.13.116.1 GLOBAL_CTRL_ETPWM14_RST Register (Offset = 338h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1021. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0338h

Access Types Legend

Table 3-1022. ETPWM14_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.117 CONTROLSS_GLOBAL_CTRL_ETPWM15_RST Registers

3.13.117.1 GLOBAL_CTRL_ETPWM15_RST Register (Offset = 33Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1023. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 033Ch

Access Types Legend

Table 3-1024. ETPWM15_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.118 CONTROLSS_GLOBAL_CTRL_ETPWM16_RST Registers

3.13.118.1 GLOBAL_CTRL_ETPWM16_RST Register (Offset = 340h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1025. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0340h

Access Types Legend

Table 3-1026. ETPWM16_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.119 CONTROLSS_GLOBAL_CTRL_ETPWM17_RST Registers

3.13.119.1 GLOBAL_CTRL_ETPWM17_RST Register (Offset = 344h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1027. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0344h

Access Types Legend

Table 3-1028. ETPWM17_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.120 CONTROLSS_GLOBAL_CTRL_ETPWM18_RST Registers

3.13.120.1 GLOBAL_CTRL_ETPWM18_RST Register (Offset = 348h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1029. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0348h

Access Types Legend

Table 3-1030. ETPWM18_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.121 CONTROLSS_GLOBAL_CTRL_ETPWM19_RST Registers

3.13.121.1 GLOBAL_CTRL_ETPWM19_RST Register (Offset = 34Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1031. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 034Ch

Access Types Legend

Table 3-1032. ETPWM19_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.122 CONTROLSS_GLOBAL_CTRL_ETPWM20_RST Registers

3.13.122.1 GLOBAL_CTRL_ETPWM20_RST Register (Offset = 350h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1033. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0350h

Access Types Legend

Table 3-1034. ETPWM20_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.123 CONTROLSS_GLOBAL_CTRL_ETPWM21_RST Registers

3.13.123.1 GLOBAL_CTRL_ETPWM21_RST Register (Offset = 354h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1035. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0354h

Access Types Legend

Table 3-1036. ETPWM21_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.124 CONTROLSS_GLOBAL_CTRL_ETPWM22_RST Registers

3.13.124.1 GLOBAL_CTRL_ETPWM22_RST Register (Offset = 358h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1037. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0358h

Access Types Legend

Table 3-1038. ETPWM22_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.125 CONTROLSS_GLOBAL_CTRL_ETPWM23_RST Registers

3.13.125.1 GLOBAL_CTRL_ETPWM23_RST Register (Offset = 35Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1039. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 035Ch

Access Types Legend

Table 3-1040. ETPWM23_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.126 CONTROLSS_GLOBAL_CTRL_ETPWM24_RST Registers

3.13.126.1 GLOBAL_CTRL_ETPWM24_RST Register (Offset = 360h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1041. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0360h

Access Types Legend

Table 3-1042. ETPWM24_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.127 CONTROLSS_GLOBAL_CTRL_ETPWM25_RST Registers

3.13.127.1 GLOBAL_CTRL_ETPWM25_RST Register (Offset = 364h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1043. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0364h

Access Types Legend

Table 3-1044. ETPWM25_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.128 CONTROLSS_GLOBAL_CTRL_ETPWM26_RST Registers

3.13.128.1 GLOBAL_CTRL_ETPWM26_RST Register (Offset = 368h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1045. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0368h

Access Types Legend

Table 3-1046. ETPWM26_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.129 CONTROLSS_GLOBAL_CTRL_ETPWM27_RST Registers

3.13.129.1 GLOBAL_CTRL_ETPWM27_RST Register (Offset = 36Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1047. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 036Ch

Access Types Legend

Table 3-1048. ETPWM27_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.130 CONTROLSS_GLOBAL_CTRL_ETPWM28_RST Registers

3.13.130.1 GLOBAL_CTRL_ETPWM28_RST Register (Offset = 370h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1049. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0370h

Access Types Legend

Table 3-1050. ETPWM28_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.131 CONTROLSS_GLOBAL_CTRL_ETPWM29_RST Registers

3.13.131.1 GLOBAL_CTRL_ETPWM29_RST Register (Offset = 374h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1051. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0374h

Access Types Legend

Table 3-1052. ETPWM29_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.132 CONTROLSS_GLOBAL_CTRL_ETPWM30_RST Registers

3.13.132.1 GLOBAL_CTRL_ETPWM30_RST Register (Offset = 378h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1053. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0378h

Access Types Legend

Table 3-1054. ETPWM30_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.133 CONTROLSS_GLOBAL_CTRL_ETPWM31_RST Registers

3.13.133.1 GLOBAL_CTRL_ETPWM31_RST Register (Offset = 37Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1055. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 037Ch

Access Types Legend

Table 3-1056. ETPWM31_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding etpwm

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3.13.134 CONTROLSS_GLOBAL_CTRL_FSI_TX0_RST Registers

3.13.134.1 GLOBAL_CTRL_FSI_TX0_RST Register (Offset = 380h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1057. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0380h

Access Types Legend

Table 3-1058. FSI_TX0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding fsi_tx

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3.13.135 CONTROLSS_GLOBAL_CTRL_FSI_TX1_RST Registers

3.13.135.1 GLOBAL_CTRL_FSI_TX1_RST Register (Offset = 384h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1059. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0384h

Access Types Legend

Table 3-1060. FSI_TX1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding fsi_tx

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3.13.136 CONTROLSS_GLOBAL_CTRL_FSI_TX2_RST Registers

3.13.136.1 GLOBAL_CTRL_FSI_TX2_RST Register (Offset = 388h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1061. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0388h

Access Types Legend

Table 3-1062. FSI_TX2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding fsi_tx

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3.13.137 CONTROLSS_GLOBAL_CTRL_FSI_TX3_RST Registers

3.13.137.1 GLOBAL_CTRL_FSI_TX3_RST Register (Offset = 38Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1063. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 038Ch

Access Types Legend

Table 3-1064. FSI_TX3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding fsi_tx

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3.13.138 CONTROLSS_GLOBAL_CTRL_FSI_RX0_RST Registers

3.13.138.1 GLOBAL_CTRL_FSI_RX0_RST Register (Offset = 390h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1065. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0390h

Access Types Legend

Table 3-1066. FSI_RX0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding fsi_rx

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3.13.139 CONTROLSS_GLOBAL_CTRL_FSI_RX1_RST Registers

3.13.139.1 GLOBAL_CTRL_FSI_RX1_RST Register (Offset = 394h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1067. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0394h

Access Types Legend

Table 3-1068. FSI_RX1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding fsi_rx

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3.13.140 CONTROLSS_GLOBAL_CTRL_FSI_RX2_RST Registers

3.13.140.1 GLOBAL_CTRL_FSI_RX2_RST Register (Offset = 398h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1069. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0398h

Access Types Legend

Table 3-1070. FSI_RX2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding fsi_rx

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3.13.141 CONTROLSS_GLOBAL_CTRL_FSI_RX3_RST Registers

3.13.141.1 GLOBAL_CTRL_FSI_RX3_RST Register (Offset = 39Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1071. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 039Ch

Access Types Legend

Table 3-1072. FSI_RX3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding fsi_rx

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3.13.142 CONTROLSS_GLOBAL_CTRL_CMPSSA0_RST Registers

3.13.142.1 GLOBAL_CTRL_CMPSSA0_RST Register (Offset = 3A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1073. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03A0h

Access Types Legend

Table 3-1074. CMPSSA0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

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3.13.143 CONTROLSS_GLOBAL_CTRL_CMPSSA1_RST Registers

3.13.143.1 GLOBAL_CTRL_CMPSSA1_RST Register (Offset = 3A4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1075. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03A4h

Access Types Legend

Table 3-1076. CMPSSA1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

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3.13.144 CONTROLSS_GLOBAL_CTRL_CMPSSA2_RST Registers

3.13.144.1 GLOBAL_CTRL_CMPSSA2_RST Register (Offset = 3A8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1077. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03A8h

Access Types Legend

Table 3-1078. CMPSSA2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

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3.13.145 CONTROLSS_GLOBAL_CTRL_CMPSSA3_RST Registers

3.13.145.1 GLOBAL_CTRL_CMPSSA3_RST Register (Offset = 3ACh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1079. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03ACh

Access Types Legend

Table 3-1080. CMPSSA3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

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3.13.146 CONTROLSS_GLOBAL_CTRL_CMPSSA5_RST Registers

3.13.146.1 GLOBAL_CTRL_CMPSSA5_RST Register (Offset = 3B4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1081. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03B4h

Access Types Legend

Table 3-1082. CMPSSA5_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

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3.13.147 CONTROLSS_GLOBAL_CTRL_CMPSSA4_RST Registers

3.13.147.1 GLOBAL_CTRL_CMPSSA4_RST Register (Offset = 3B0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1083. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03B0h

Access Types Legend

Table 3-1084. CMPSSA4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

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3.13.148 CONTROLSS_GLOBAL_CTRL_CMPSSA6_RST Registers

3.13.148.1 GLOBAL_CTRL_CMPSSA6_RST Register (Offset = 3B8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1085. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03B8h

Access Types Legend

Table 3-1086. CMPSSA6_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

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3.13.149 CONTROLSS_GLOBAL_CTRL_CMPSSA7_RST Registers

3.13.149.1 GLOBAL_CTRL_CMPSSA7_RST Register (Offset = 3BCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1087. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03BCh

Access Types Legend

Table 3-1088. CMPSSA7_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

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3.13.150 CONTROLSS_GLOBAL_CTRL_CMPSSA8_RST Registers

3.13.150.1 GLOBAL_CTRL_CMPSSA8_RST Register (Offset = 3C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1089. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03C0h

Access Types Legend

Table 3-1090. CMPSSA8_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

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3.13.151 CONTROLSS_GLOBAL_CTRL_CMPSSA9_RST Registers

3.13.151.1 GLOBAL_CTRL_CMPSSA9_RST Register (Offset = 3C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1091. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03C4h

Access Types Legend

Table 3-1092. CMPSSA9_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss12b

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3.13.152 CONTROLSS_GLOBAL_CTRL_CMPSSB0_RST Registers

3.13.152.1 GLOBAL_CTRL_CMPSSB0_RST Register (Offset = 3D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1093. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03D0h

Access Types Legend

Table 3-1094. CMPSSB0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

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3.13.153 CONTROLSS_GLOBAL_CTRL_CMPSSB1_RST Registers

3.13.153.1 GLOBAL_CTRL_CMPSSB1_RST Register (Offset = 3D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1095. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03D4h

Access Types Legend

Table 3-1096. CMPSSB1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

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3.13.154 CONTROLSS_GLOBAL_CTRL_CMPSSB2_RST Registers

3.13.154.1 GLOBAL_CTRL_CMPSSB2_RST Register (Offset = 3D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1097. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03D8h

Access Types Legend

Table 3-1098. CMPSSB2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

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3.13.155 CONTROLSS_GLOBAL_CTRL_CMPSSB3_RST Registers

3.13.155.1 GLOBAL_CTRL_CMPSSB3_RST Register (Offset = 3DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1099. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03DCh

Access Types Legend

Table 3-1100. CMPSSB3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

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3.13.156 CONTROLSS_GLOBAL_CTRL_CMPSSB4_RST Registers

3.13.156.1 GLOBAL_CTRL_CMPSSB4_RST Register (Offset = 3E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1101. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03E0h

Access Types Legend

Table 3-1102. CMPSSB4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

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3.13.157 CONTROLSS_GLOBAL_CTRL_CMPSSB5_RST Registers

3.13.157.1 GLOBAL_CTRL_CMPSSB5_RST Register (Offset = 3E4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1103. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03E4h

Access Types Legend

Table 3-1104. CMPSSB5_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

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3.13.158 CONTROLSS_GLOBAL_CTRL_CMPSSB6_RST Registers

3.13.158.1 GLOBAL_CTRL_CMPSSB6_RST Register (Offset = 3E8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1105. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03E8h

Access Types Legend

Table 3-1106. CMPSSB6_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

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3.13.159 CONTROLSS_GLOBAL_CTRL_CMPSSB7_RST Registers

3.13.159.1 GLOBAL_CTRL_CMPSSB7_RST Register (Offset = 3ECh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1107. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03ECh

Access Types Legend

Table 3-1108. CMPSSB7_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

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3.13.160 CONTROLSS_GLOBAL_CTRL_CMPSSB8_RST Registers

3.13.160.1 GLOBAL_CTRL_CMPSSB8_RST Register (Offset = 3F0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1109. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03F0h

Access Types Legend

Table 3-1110. CMPSSB8_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

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3.13.161 CONTROLSS_GLOBAL_CTRL_CMPSSB9_RST Registers

3.13.161.1 GLOBAL_CTRL_CMPSSB9_RST Register (Offset = 3F4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1111. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 03F4h

Access Types Legend

Table 3-1112. CMPSSB9_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding cmpss8b

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3.13.162 CONTROLSS_GLOBAL_CTRL_ECAP0_RST Registers

3.13.162.1 GLOBAL_CTRL_ECAP0_RST Register (Offset = 400h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1113. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0400h

Access Types Legend

Table 3-1114. ECAP0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

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3.13.163 CONTROLSS_GLOBAL_CTRL_ECAP1_RST Registers

3.13.163.1 GLOBAL_CTRL_ECAP1_RST Register (Offset = 404h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1115. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0404h

Access Types Legend

Table 3-1116. ECAP1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

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3.13.164 CONTROLSS_GLOBAL_CTRL_ECAP2_RST Registers

3.13.164.1 GLOBAL_CTRL_ECAP2_RST Register (Offset = 408h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1117. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0408h

Access Types Legend

Table 3-1118. ECAP2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

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3.13.165 CONTROLSS_GLOBAL_CTRL_ECAP3_RST Registers

3.13.165.1 GLOBAL_CTRL_ECAP3_RST Register (Offset = 40Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1119. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 040Ch

Access Types Legend

Table 3-1120. ECAP3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

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3.13.166 CONTROLSS_GLOBAL_CTRL_ECAP4_RST Registers

3.13.166.1 GLOBAL_CTRL_ECAP4_RST Register (Offset = 410h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1121. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0410h

Access Types Legend

Table 3-1122. ECAP4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

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3.13.167 CONTROLSS_GLOBAL_CTRL_ECAP5_RST Registers

3.13.167.1 GLOBAL_CTRL_ECAP5_RST Register (Offset = 414h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1123. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0414h

Access Types Legend

Table 3-1124. ECAP5_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

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3.13.168 CONTROLSS_GLOBAL_CTRL_ECAP6_RST Registers

3.13.168.1 GLOBAL_CTRL_ECAP6_RST Register (Offset = 418h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1125. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0418h

Access Types Legend

Table 3-1126. ECAP6_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

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3.13.169 CONTROLSS_GLOBAL_CTRL_ECAP7_RST Registers

3.13.169.1 GLOBAL_CTRL_ECAP7_RST Register (Offset = 41Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1127. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 041Ch

Access Types Legend

Table 3-1128. ECAP7_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

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3.13.170 CONTROLSS_GLOBAL_CTRL_ECAP8_RST Registers

3.13.170.1 GLOBAL_CTRL_ECAP8_RST Register (Offset = 420h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1129. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0420h

Access Types Legend

Table 3-1130. ECAP8_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

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3.13.171 CONTROLSS_GLOBAL_CTRL_ECAP9_RST Registers

3.13.171.1 GLOBAL_CTRL_ECAP9_RST Register (Offset = 424h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1131. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0424h

Access Types Legend

Table 3-1132. ECAP9_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding ecap

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3.13.172 CONTROLSS_GLOBAL_CTRL_EQEP0_RST Registers

3.13.172.1 GLOBAL_CTRL_EQEP0_RST Register (Offset = 440h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1133. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0440h

Access Types Legend

Table 3-1134. EQEP0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding eqep

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3.13.173 CONTROLSS_GLOBAL_CTRL_EQEP1_RST Registers

3.13.173.1 GLOBAL_CTRL_EQEP1_RST Register (Offset = 444h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1135. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0444h

Access Types Legend

Table 3-1136. EQEP1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding eqep

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3.13.174 CONTROLSS_GLOBAL_CTRL_EQEP2_RST Registers

3.13.174.1 GLOBAL_CTRL_EQEP2_RST Register (Offset = 448h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1137. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0448h

Access Types Legend

Table 3-1138. EQEP2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding eqep

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3.13.175 CONTROLSS_GLOBAL_CTRL_SDFM0_RST Registers

3.13.175.1 GLOBAL_CTRL_SDFM0_RST Register (Offset = 450h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1139. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0450h

Access Types Legend

Table 3-1140. SDFM0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding sdfm

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3.13.176 CONTROLSS_GLOBAL_CTRL_SDFM1_RST Registers

3.13.176.1 GLOBAL_CTRL_SDFM1_RST Register (Offset = 454h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1141. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0454h

Access Types Legend

Table 3-1142. SDFM1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding sdfm

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3.13.177 CONTROLSS_GLOBAL_CTRL_DAC_RST Registers

3.13.177.1 GLOBAL_CTRL_DAC_RST Register (Offset = 458h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1143. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0458h

Access Types Legend

Table 3-1144. DAC_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for dac

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3.13.178 CONTROLSS_GLOBAL_CTRL_ADC0_RST Registers

3.13.178.1 GLOBAL_CTRL_ADC0_RST Register (Offset = 45Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1145. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 045Ch

Access Types Legend

Table 3-1146. ADC0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding adc

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3.13.179 CONTROLSS_GLOBAL_CTRL_ADC1_RST Registers

3.13.179.1 GLOBAL_CTRL_ADC1_RST Register (Offset = 460h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1147. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0460h

Access Types Legend

Table 3-1148. ADC1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding adc

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3.13.180 CONTROLSS_GLOBAL_CTRL_ADC2_RST Registers

3.13.180.1 GLOBAL_CTRL_ADC2_RST Register (Offset = 464h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1149. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0464h

Access Types Legend

Table 3-1150. ADC2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding adc

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3.13.181 CONTROLSS_GLOBAL_CTRL_ADC3_RST Registers

3.13.181.1 GLOBAL_CTRL_ADC3_RST Register (Offset = 468h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1151. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0468h

Access Types Legend

Table 3-1152. ADC3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding adc

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3.13.182 CONTROLSS_GLOBAL_CTRL_ADC4_RST Registers

3.13.182.1 GLOBAL_CTRL_ADC4_RST Register (Offset = 46Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1153. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 046Ch

Access Types Legend

Table 3-1154. ADC4_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding adc

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3.13.183 CONTROLSS_GLOBAL_CTRL_OTTO0_RST Registers

3.13.183.1 GLOBAL_CTRL_OTTO0_RST Register (Offset = 470h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1155. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0470h

Access Types Legend

Table 3-1156. OTTO0_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding otto

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3.13.184 CONTROLSS_GLOBAL_CTRL_OTTO1_RST Registers

3.13.184.1 GLOBAL_CTRL_OTTO1_RST Register (Offset = 474h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1157. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0474h

Access Types Legend

Table 3-1158. OTTO1_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding otto

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3.13.185 CONTROLSS_GLOBAL_CTRL_OTTO2_RST Registers

3.13.185.1 GLOBAL_CTRL_OTTO2_RST Register (Offset = 478h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1159. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0478h

Access Types Legend

Table 3-1160. OTTO2_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding otto

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3.13.186 CONTROLSS_GLOBAL_CTRL_OTTO3_RST Registers

3.13.186.1 GLOBAL_CTRL_OTTO3_RST Register (Offset = 47Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1161. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 047Ch

Access Types Legend

Table 3-1162. OTTO3_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RST	RW	0h	writing '111' will generate reset for corresponding otto

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3.13.187 CONTROLSS_GLOBAL_CTRL_EPWM0_HALTEN Registers

3.13.187.1 GLOBAL_CTRL_EPWM0_HALTEN Register (Offset = 500h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1163. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0500h

Access Types Legend

Table 3-1164. EPWM0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.188 CONTROLSS_GLOBAL_CTRL_EPWM1_HALTEN Registers

3.13.188.1 GLOBAL_CTRL_EPWM1_HALTEN Register (Offset = 504h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1165. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0504h

Access Types Legend

Table 3-1166. EPWM1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.189 CONTROLSS_GLOBAL_CTRL_EPWM2_HALTEN Registers

3.13.189.1 GLOBAL_CTRL_EPWM2_HALTEN Register (Offset = 508h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1167. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0508h

Access Types Legend

Table 3-1168. EPWM2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.190 CONTROLSS_GLOBAL_CTRL_EPWM3_HALTEN Registers

3.13.190.1 GLOBAL_CTRL_EPWM3_HALTEN Register (Offset = 50Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1169. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 050Ch

Access Types Legend

Table 3-1170. EPWM3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.191 CONTROLSS_GLOBAL_CTRL_EPWM4_HALTEN Registers

3.13.191.1 GLOBAL_CTRL_EPWM4_HALTEN Register (Offset = 510h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1171. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0510h

Access Types Legend

Table 3-1172. EPWM4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.192 CONTROLSS_GLOBAL_CTRL_EPWM5_HALTEN Registers

3.13.192.1 GLOBAL_CTRL_EPWM5_HALTEN Register (Offset = 514h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1173. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0514h

Access Types Legend

Table 3-1174. EPWM5_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.193 CONTROLSS_GLOBAL_CTRL_EPWM6_HALTEN Registers

3.13.193.1 GLOBAL_CTRL_EPWM6_HALTEN Register (Offset = 518h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1175. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0518h

Access Types Legend

Table 3-1176. EPWM6_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.194 CONTROLSS_GLOBAL_CTRL_EPWM7_HALTEN Registers

3.13.194.1 GLOBAL_CTRL_EPWM7_HALTEN Register (Offset = 51Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1177. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 051Ch

Access Types Legend

Table 3-1178. EPWM7_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.195 CONTROLSS_GLOBAL_CTRL_EPWM8_HALTEN Registers

3.13.195.1 GLOBAL_CTRL_EPWM8_HALTEN Register (Offset = 520h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1179. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0520h

Access Types Legend

Table 3-1180. EPWM8_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.196 CONTROLSS_GLOBAL_CTRL_EPWM9_HALTEN Registers

3.13.196.1 GLOBAL_CTRL_EPWM9_HALTEN Register (Offset = 524h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1181. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0524h

Access Types Legend

Table 3-1182. EPWM9_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.197 CONTROLSS_GLOBAL_CTRL_EPWM10_HALTEN Registers

3.13.197.1 GLOBAL_CTRL_EPWM10_HALTEN Register (Offset = 528h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1183. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0528h

Access Types Legend

Table 3-1184. EPWM10_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.198 CONTROLSS_GLOBAL_CTRL_EPWM11_HALTEN Registers

3.13.198.1 GLOBAL_CTRL_EPWM11_HALTEN Register (Offset = 52Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1185. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 052Ch

Access Types Legend

Table 3-1186. EPWM11_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.199 CONTROLSS_GLOBAL_CTRL_EPWM12_HALTEN Registers

3.13.199.1 GLOBAL_CTRL_EPWM12_HALTEN Register (Offset = 530h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1187. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0530h

Access Types Legend

Table 3-1188. EPWM12_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.200 CONTROLSS_GLOBAL_CTRL_EPWM13_HALTEN Registers

3.13.200.1 GLOBAL_CTRL_EPWM13_HALTEN Register (Offset = 534h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1189. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0534h

Access Types Legend

Table 3-1190. EPWM13_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.201 CONTROLSS_GLOBAL_CTRL_EPWM14_HALTEN Registers

3.13.201.1 GLOBAL_CTRL_EPWM14_HALTEN Register (Offset = 538h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1191. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0538h

Access Types Legend

Table 3-1192. EPWM14_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.202 CONTROLSS_GLOBAL_CTRL_EPWM15_HALTEN Registers

3.13.202.1 GLOBAL_CTRL_EPWM15_HALTEN Register (Offset = 53Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1193. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 053Ch

Access Types Legend

Table 3-1194. EPWM15_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.203 CONTROLSS_GLOBAL_CTRL_EPWM16_HALTEN Registers

3.13.203.1 GLOBAL_CTRL_EPWM16_HALTEN Register (Offset = 540h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1195. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0540h

Access Types Legend

Table 3-1196. EPWM16_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.204 CONTROLSS_GLOBAL_CTRL_EPWM17_HALTEN Registers

3.13.204.1 GLOBAL_CTRL_EPWM17_HALTEN Register (Offset = 544h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1197. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0544h

Access Types Legend

Table 3-1198. EPWM17_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.205 CONTROLSS_GLOBAL_CTRL_EPWM18_HALTEN Registers

3.13.205.1 GLOBAL_CTRL_EPWM18_HALTEN Register (Offset = 548h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1199. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0548h

Access Types Legend

Table 3-1200. EPWM18_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.206 CONTROLSS_GLOBAL_CTRL_EPWM19_HALTEN Registers

3.13.206.1 GLOBAL_CTRL_EPWM19_HALTEN Register (Offset = 54Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1201. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 054Ch

Access Types Legend

Table 3-1202. EPWM19_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.207 CONTROLSS_GLOBAL_CTRL_EPWM20_HALTEN Registers

3.13.207.1 GLOBAL_CTRL_EPWM20_HALTEN Register (Offset = 550h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1203. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0550h

Access Types Legend

Table 3-1204. EPWM20_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.208 CONTROLSS_GLOBAL_CTRL_EPWM21_HALTEN Registers

3.13.208.1 GLOBAL_CTRL_EPWM21_HALTEN Register (Offset = 554h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1205. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0554h

Access Types Legend

Table 3-1206. EPWM21_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.209 CONTROLSS_GLOBAL_CTRL_EPWM22_HALTEN Registers

3.13.209.1 GLOBAL_CTRL_EPWM22_HALTEN Register (Offset = 558h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1207. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0558h

Access Types Legend

Table 3-1208. EPWM22_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.210 CONTROLSS_GLOBAL_CTRL_EPWM23_HALTEN Registers

3.13.210.1 GLOBAL_CTRL_EPWM23_HALTEN Register (Offset = 55Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1209. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 055Ch

Access Types Legend

Table 3-1210. EPWM23_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.211 CONTROLSS_GLOBAL_CTRL_EPWM24_HALTEN Registers

3.13.211.1 GLOBAL_CTRL_EPWM24_HALTEN Register (Offset = 560h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1211. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0560h

Access Types Legend

Table 3-1212. EPWM24_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.212 CONTROLSS_GLOBAL_CTRL_EPWM25_HALTEN Registers

3.13.212.1 GLOBAL_CTRL_EPWM25_HALTEN Register (Offset = 564h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1213. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0564h

Access Types Legend

Table 3-1214. EPWM25_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.213 CONTROLSS_GLOBAL_CTRL_EPWM26_HALTEN Registers

3.13.213.1 GLOBAL_CTRL_EPWM26_HALTEN Register (Offset = 568h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1215. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0568h

Access Types Legend

Table 3-1216. EPWM26_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.214 CONTROLSS_GLOBAL_CTRL_EPWM27_HALTEN Registers

3.13.214.1 GLOBAL_CTRL_EPWM27_HALTEN Register (Offset = 56Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1217. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 056Ch

Access Types Legend

Table 3-1218. EPWM27_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.215 CONTROLSS_GLOBAL_CTRL_EPWM28_HALTEN Registers

3.13.215.1 GLOBAL_CTRL_EPWM28_HALTEN Register (Offset = 570h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1219. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0570h

Access Types Legend

Table 3-1220. EPWM28_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.216 CONTROLSS_GLOBAL_CTRL_EPWM29_HALTEN Registers

3.13.216.1 GLOBAL_CTRL_EPWM29_HALTEN Register (Offset = 574h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1221. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0574h

Access Types Legend

Table 3-1222. EPWM29_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.217 CONTROLSS_GLOBAL_CTRL_EPWM30_HALTEN Registers

3.13.217.1 GLOBAL_CTRL_EPWM30_HALTEN Register (Offset = 578h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1223. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0578h

Access Types Legend

Table 3-1224. EPWM30_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.218 CONTROLSS_GLOBAL_CTRL_EPWM31_HALTEN Registers

3.13.218.1 GLOBAL_CTRL_EPWM31_HALTEN Register (Offset = 57Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1225. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 057Ch

Access Types Legend

Table 3-1226. EPWM31_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.219 CONTROLSS_GLOBAL_CTRL_CMPSSA0_HALTEN Registers

3.13.219.1 GLOBAL_CTRL_CMPSSA0_HALTEN Register (Offset = 580h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1227. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0580h

Access Types Legend

Table 3-1228. CMPSSA0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.220 CONTROLSS_GLOBAL_CTRL_CMPSSA1_HALTEN Registers

3.13.220.1 GLOBAL_CTRL_CMPSSA1_HALTEN Register (Offset = 584h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1229. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0584h

Access Types Legend

Table 3-1230. CMPSSA1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.221 CONTROLSS_GLOBAL_CTRL_CMPSSA2_HALTEN Registers

3.13.221.1 GLOBAL_CTRL_CMPSSA2_HALTEN Register (Offset = 588h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1231. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0588h

Access Types Legend

Table 3-1232. CMPSSA2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.222 CONTROLSS_GLOBAL_CTRL_CMPSSA3_HALTEN Registers

3.13.222.1 GLOBAL_CTRL_CMPSSA3_HALTEN Register (Offset = 58Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1233. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 058Ch

Access Types Legend

Table 3-1234. CMPSSA3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.223 CONTROLSS_GLOBAL_CTRL_CMPSSA4_HALTEN Registers

3.13.223.1 GLOBAL_CTRL_CMPSSA4_HALTEN Register (Offset = 590h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1235. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0590h

Access Types Legend

Table 3-1236. CMPSSA4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.224 CONTROLSS_GLOBAL_CTRL_CMPSSA5_HALTEN Registers

3.13.224.1 GLOBAL_CTRL_CMPSSA5_HALTEN Register (Offset = 594h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1237. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0594h

Access Types Legend

Table 3-1238. CMPSSA5_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.225 CONTROLSS_GLOBAL_CTRL_CMPSSA6_HALTEN Registers

3.13.225.1 GLOBAL_CTRL_CMPSSA6_HALTEN Register (Offset = 598h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1239. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0598h

Access Types Legend

Table 3-1240. CMPSSA6_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.226 CONTROLSS_GLOBAL_CTRL_CMPSSA7_HALTEN Registers

3.13.226.1 GLOBAL_CTRL_CMPSSA7_HALTEN Register (Offset = 59Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1241. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 059Ch

Access Types Legend

Table 3-1242. CMPSSA7_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.227 CONTROLSS_GLOBAL_CTRL_CMPSSA8_HALTEN Registers

3.13.227.1 GLOBAL_CTRL_CMPSSA8_HALTEN Register (Offset = 5A0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1243. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05A0h

Access Types Legend

Table 3-1244. CMPSSA8_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.228 CONTROLSS_GLOBAL_CTRL_CMPSSA9_HALTEN Registers

3.13.228.1 GLOBAL_CTRL_CMPSSA9_HALTEN Register (Offset = 5A4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1245. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05A4h

Access Types Legend

Table 3-1246. CMPSSA9_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.229 CONTROLSS_GLOBAL_CTRL_CMPSSB0_HALTEN Registers

3.13.229.1 GLOBAL_CTRL_CMPSSB0_HALTEN Register (Offset = 5A8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1247. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05A8h

Access Types Legend

Table 3-1248. CMPSSB0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.230 CONTROLSS_GLOBAL_CTRL_CMPSSB1_HALTEN Registers

3.13.230.1 GLOBAL_CTRL_CMPSSB1_HALTEN Register (Offset = 5ACh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1249. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05ACh

Access Types Legend

Table 3-1250. CMPSSB1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.231 CONTROLSS_GLOBAL_CTRL_CMPSSB2_HALTEN Registers

3.13.231.1 GLOBAL_CTRL_CMPSSB2_HALTEN Register (Offset = 5B0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1251. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05B0h

Access Types Legend

Table 3-1252. CMPSSB2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.232 CONTROLSS_GLOBAL_CTRL_CMPSSB3_HALTEN Registers

3.13.232.1 GLOBAL_CTRL_CMPSSB3_HALTEN Register (Offset = 5B4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1253. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05B4h

Access Types Legend

Table 3-1254. CMPSSB3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.233 CONTROLSS_GLOBAL_CTRL_CMPSSB4_HALTEN Registers

3.13.233.1 GLOBAL_CTRL_CMPSSB4_HALTEN Register (Offset = 5B8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1255. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05B8h

Access Types Legend

Table 3-1256. CMPSSB4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.234 CONTROLSS_GLOBAL_CTRL_CMPSSB5_HALTEN Registers

3.13.234.1 GLOBAL_CTRL_CMPSSB5_HALTEN Register (Offset = 5BCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1257. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05BCh

Access Types Legend

Table 3-1258. CMPSSB5_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.235 CONTROLSS_GLOBAL_CTRL_CMPSSB6_HALTEN Registers

3.13.235.1 GLOBAL_CTRL_CMPSSB6_HALTEN Register (Offset = 5C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1259. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05C0h

Access Types Legend

Table 3-1260. CMPSSB6_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.236 CONTROLSS_GLOBAL_CTRL_CMPSSB7_HALTEN Registers

3.13.236.1 GLOBAL_CTRL_CMPSSB7_HALTEN Register (Offset = 5C4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1261. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05C4h

Access Types Legend

Table 3-1262. CMPSSB7_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.237 CONTROLSS_GLOBAL_CTRL_CMPSSB8_HALTEN Registers

3.13.237.1 GLOBAL_CTRL_CMPSSB8_HALTEN Register (Offset = 5C8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1263. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05C8h

Access Types Legend

Table 3-1264. CMPSSB8_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.238 CONTROLSS_GLOBAL_CTRL_CMPSSB9_HALTEN Registers

3.13.238.1 GLOBAL_CTRL_CMPSSB9_HALTEN Register (Offset = 5CCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1265. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05CCh

Access Types Legend

Table 3-1266. CMPSSB9_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.239 CONTROLSS_GLOBAL_CTRL_ECAP0_HALTEN Registers

3.13.239.1 GLOBAL_CTRL_ECAP0_HALTEN Register (Offset = 5D0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1267. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05D0h

Access Types Legend

Table 3-1268. ECAP0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.240 CONTROLSS_GLOBAL_CTRL_ECAP1_HALTEN Registers

3.13.240.1 GLOBAL_CTRL_ECAP1_HALTEN Register (Offset = 5D4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1269. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05D4h

Access Types Legend

Table 3-1270. ECAP1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.241 CONTROLSS_GLOBAL_CTRL_ECAP2_HALTEN Registers

3.13.241.1 GLOBAL_CTRL_ECAP2_HALTEN Register (Offset = 5D8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1271. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05D8h

Access Types Legend

Table 3-1272. ECAP2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.242 CONTROLSS_GLOBAL_CTRL_ECAP3_HALTEN Registers

3.13.242.1 GLOBAL_CTRL_ECAP3_HALTEN Register (Offset = 5DCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1273. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05DCh

Access Types Legend

Table 3-1274. ECAP3_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.243 CONTROLSS_GLOBAL_CTRL_ECAP4_HALTEN Registers

3.13.243.1 GLOBAL_CTRL_ECAP4_HALTEN Register (Offset = 5E0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1275. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05E0h

Access Types Legend

Table 3-1276. ECAP4_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.244 CONTROLSS_GLOBAL_CTRL_ECAP5_HALTEN Registers

3.13.244.1 GLOBAL_CTRL_ECAP5_HALTEN Register (Offset = 5E4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1277. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05E4h

Access Types Legend

Table 3-1278. ECAP5_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.245 CONTROLSS_GLOBAL_CTRL_ECAP6_HALTEN Registers

3.13.245.1 GLOBAL_CTRL_ECAP6_HALTEN Register (Offset = 5E8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1279. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05E8h

Access Types Legend

Table 3-1280. ECAP6_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.246 CONTROLSS_GLOBAL_CTRL_ECAP7_HALTEN Registers

3.13.246.1 GLOBAL_CTRL_ECAP7_HALTEN Register (Offset = 5ECh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1281. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05ECh

Access Types Legend

Table 3-1282. ECAP7_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.247 CONTROLSS_GLOBAL_CTRL_ECAP8_HALTEN Registers

3.13.247.1 GLOBAL_CTRL_ECAP8_HALTEN Register (Offset = 5F0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1283. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05F0h

Access Types Legend

Table 3-1284. ECAP8_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.248 CONTROLSS_GLOBAL_CTRL_ECAP9_HALTEN Registers

3.13.248.1 GLOBAL_CTRL_ECAP9_HALTEN Register (Offset = 5F4h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1285. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05F4h

Access Types Legend

Table 3-1286. ECAP9_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.249 CONTROLSS_GLOBAL_CTRL_EQEP0_HALTEN Registers

3.13.249.1 GLOBAL_CTRL_EQEP0_HALTEN Register (Offset = 5F8h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1287. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05F8h

Access Types Legend

Table 3-1288. EQEP0_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.250 CONTROLSS_GLOBAL_CTRL_EQEP1_HALTEN Registers

3.13.250.1 GLOBAL_CTRL_EQEP1_HALTEN Register (Offset = 5FCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1289. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 05FCh

Access Types Legend

Table 3-1290. EQEP1_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.251 CONTROLSS_GLOBAL_CTRL_EQEP2_HALTEN Registers

3.13.251.1 GLOBAL_CTRL_EQEP2_HALTEN Register (Offset = 600h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1291. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 0600h

Access Types Legend

Table 3-1292. EQEP2_HALTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	CR5B1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
2	CR5A1	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
1	CR5B0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt
0	CR5A0	RW	0h	1'b0: IP Halt disabled with corresponding CPU halt1'b1: IP Halt enabled with corresponding CPU halt

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3.13.252 CONTROLSS_GLOBAL_CTRL_LOCK0_KICK0 Registers

3.13.252.1 GLOBAL_CTRL_LOCK0_KICK0 Register (Offset = 1008h) [reset = h]

Short Description: - KICK0 component

Long Description:

Return to Summary Table

Table 3-1293. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1008h

Access Types Legend

Table 3-1294. LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	LOCK0_KICK0	RW	0h	- KICK0 component

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3.13.253 CONTROLSS_GLOBAL_CTRL_LOCK0_KICK1 Registers

3.13.253.1 GLOBAL_CTRL_LOCK0_KICK1 Register (Offset = 100Ch) [reset = h]

Short Description: - KICK1 component

Long Description:

Return to Summary Table

Table 3-1295. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 100Ch

Access Types Legend

Table 3-1296. LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	LOCK0_KICK1	RW	0h	- KICK1 component

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3.13.254 CONTROLSS_GLOBAL_CTRL_INTR_RAW_STATUS Registers

3.13.254.1 GLOBAL_CTRL_INTR_RAW_STATUS Register (Offset = 1010h) [reset = h]

Short Description: Interrupt Raw Status/Set Register

Long Description:

Return to Summary Table

Table 3-1297. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1010h

Access Types Legend

Table 3-1298. INTR_RAW_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR	RW	0h	Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
2	KICK_ERR	RW	0h	Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
1	ADDR_ERR	RW	0h	Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.
0	PROT_ERR	RW	0h	Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.

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3.13.255 CONTROLSS_GLOBAL_CTRL_INTR_ENABLED_STATUS_CLEAR Registers

3.13.255.1 GLOBAL_CTRL_INTR_ENABLED_STATUS_CLEAR Register (Offset = 1014h) [reset = h]

Short Description: Interrupt Enabled Status/Clear register

Long Description:

Return to Summary Table

Table 3-1299. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1014h

Access Types Legend

Table 3-1300. INTR_ENABLED_STATUS_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	ENABLED_PROXY_ERR	RW	0h	Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
2	ENABLED_KICK_ERR	RW	0h	Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
1	ENABLED_ADDR_ERR	RW	0h	Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.
0	ENABLED_PROT_ERR	RW	0h	Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.

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3.13.256 CONTROLSS_GLOBAL_CTRL_INTR_ENABLE Registers

3.13.256.1 GLOBAL_CTRL_INTR_ENABLE Register (Offset = 1018h) [reset = h]

Short Description: Interrupt Enable register

Long Description:

Return to Summary Table

Table 3-1301. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1018h

Access Types Legend

Table 3-1302. INTR_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR_EN	RW	0h	Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
2	KICK_ERR_EN	RW	0h	Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN	RW	0h	Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.
0	PROT_ERR_EN	RW	0h	Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.

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3.13.257 CONTROLSS_GLOBAL_CTRL_INTR_ENABLE_CLEAR Registers

3.13.257.1 GLOBAL_CTRL_INTR_ENABLE_CLEAR Register (Offset = 101Ch) [reset = h]

Short Description: Interrupt Enable Clear register

Long Description:

Return to Summary Table

Table 3-1303. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 101Ch

Access Types Legend

Table 3-1304. INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	PROXY_ERR_EN_CLR	RW	0h	Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
2	KICK_ERR_EN_CLR	RW	0h	Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
1	ADDR_ERR_EN_CLR	RW	0h	Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.
0	PROT_ERR_EN_CLR	RW	0h	Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.

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3.13.258 CONTROLSS_GLOBAL_CTRL_EOI Registers

3.13.258.1 GLOBAL_CTRL_EOI Register (Offset = 1020h) [reset = h]

Short Description: EOI register

Long Description:

Return to Summary Table

Table 3-1305. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1020h

Access Types Legend

Table 3-1306. EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	EOI_VECTOR	RW	0h	EOI vector value. Write this with interrupt distribution value in the chip.

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3.13.259 CONTROLSS_GLOBAL_CTRL_FAULT_ADDRESS Registers

3.13.259.1 GLOBAL_CTRL_FAULT_ADDRESS Register (Offset = 1024h) [reset = h]

Short Description: Fault Address register

Long Description:

Return to Summary Table

Table 3-1307. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1024h

Access Types Legend

Table 3-1308. FAULT_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FAULT_ADDR	RO	0h	Fault Address.

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3.13.260 CONTROLSS_GLOBAL_CTRL_FAULT_TYPE_STATUS Registers

3.13.260.1 GLOBAL_CTRL_FAULT_TYPE_STATUS Register (Offset = 1028h) [reset = h]

Short Description: Fault Type Status register

Long Description:

Return to Summary Table

Table 3-1309. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1028h

Access Types Legend

Table 3-1310. FAULT_TYPE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	FAULT_NS	RO	0h	Non-secure access.
5 - 0	FAULT_TYPE	RO	0h	Fault Type 10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype ! = 1 01_0000 = Supervisor write fault - priv = 1 dir = 0 00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1 00_0100 = User read fault - priv = 0 dir = 1 dtype = 1 00_0010 = User write fault - priv = 0 dir = 0 00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1 00_0000 = No fault

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3.13.261 CONTROLSS_GLOBAL_CTRL_FAULT_ATTR_STATUS Registers

3.13.261.1 GLOBAL_CTRL_FAULT_ATTR_STATUS Register (Offset = 102Ch) [reset = h]

Short Description: Fault Attribute Status register

Long Description:

Return to Summary Table

Table 3-1311. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 102Ch

Access Types Legend

Table 3-1312. FAULT_ATTR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	FAULT_XID	RO	0h	XID.
19 - 8	FAULT_ROUTEID	RO	0h	Route ID.
7 - 0	FAULT_PRIVID	RO	0h	Privilege ID.

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3.13.262 CONTROLSS_GLOBAL_CTRL_FAULT_CLEAR Registers

3.13.262.1 GLOBAL_CTRL_FAULT_CLEAR Register (Offset = 1030h) [reset = h]

Short Description: Fault Clear register

Long Description:

Return to Summary Table

Table 3-1313. Instance Table

Instance Name	Physical Address
CONTROLSS_CTRL	502F 1030h

Access Types Legend

Table 3-1314. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
0	FAULT_CLR	WO	0h	Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect.

3.13.263 Access Table

Table 3-1315. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
WO	WO	Write

3.14 INPUTXBAR Registers

Table 3-1316. CONTROLSS_INPUTXBAR Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_INPUTXBAR Physical Address
0h	32	INPUTXBAR_PID	502D 0000h
100h	0	INPUTXBAR_INPUTXBAR0_GSEL	502D 0100h
104h	8	INPUTXBAR_INPUTXBAR0_G0	502D 0104h
108h	8	INPUTXBAR_INPUTXBAR0_G1	502D 0108h
140h	0	INPUTXBAR_INPUTXBAR1_GSEL	502D 0140h
144h	8	INPUTXBAR_INPUTXBAR1_G0	502D 0144h
148h	8	INPUTXBAR_INPUTXBAR1_G1	502D 0148h
180h	0	INPUTXBAR_INPUTXBAR2_GSEL	502D 0180h
184h	8	INPUTXBAR_INPUTXBAR2_G0	502D 0184h
188h	8	INPUTXBAR_INPUTXBAR2_G1	502D 0188h
1C0h	0	INPUTXBAR_INPUTXBAR3_GSEL	502D 01C0h
1C4h	8	INPUTXBAR_INPUTXBAR3_G0	502D 01C4h
1C8h	8	INPUTXBAR_INPUTXBAR3_G1	502D 01C8h
200h	0	INPUTXBAR_INPUTXBAR4_GSEL	502D 0200h
204h	8	INPUTXBAR_INPUTXBAR4_G0	502D 0204h
208h	8	INPUTXBAR_INPUTXBAR4_G1	502D 0208h
240h	0	INPUTXBAR_INPUTXBAR5_GSEL	502D 0240h
244h	8	INPUTXBAR_INPUTXBAR5_G0	502D 0244h
248h	8	INPUTXBAR_INPUTXBAR5_G1	502D 0248h
280h	0	INPUTXBAR_INPUTXBAR6_GSEL	502D 0280h

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Table 3-1316. CONTROLSS_INPUTXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_INPUTXBAR Physical Address
284h	8	INPUTXBAR_INPUTXBAR6_G0	502D 0284h
288h	8	INPUTXBAR_INPUTXBAR6_G1	502D 0288h
2C0h	0	INPUTXBAR_INPUTXBAR7_GSEL	502D 02C0h
2C4h	8	INPUTXBAR_INPUTXBAR7_G0	502D 02C4h
2C8h	8	INPUTXBAR_INPUTXBAR7_G1	502D 02C8h
300h	0	INPUTXBAR_INPUTXBAR8_GSEL	502D 0300h
304h	8	INPUTXBAR_INPUTXBAR8_G0	502D 0304h
308h	8	INPUTXBAR_INPUTXBAR8_G1	502D 0308h
340h	0	INPUTXBAR_INPUTXBAR9_GSEL	502D 0340h
344h	8	INPUTXBAR_INPUTXBAR9_G0	502D 0344h
348h	8	INPUTXBAR_INPUTXBAR9_G1	502D 0348h
380h	0	INPUTXBAR_INPUTXBAR10_GSEL	502D 0380h
384h	8	INPUTXBAR_INPUTXBAR10_G0	502D 0384h
388h	8	INPUTXBAR_INPUTXBAR10_G1	502D 0388h
3C0h	0	INPUTXBAR_INPUTXBAR11_GSEL	502D 03C0h
3C4h	8	INPUTXBAR_INPUTXBAR11_G0	502D 03C4h
3C8h	8	INPUTXBAR_INPUTXBAR11_G1	502D 03C8h
400h	0	INPUTXBAR_INPUTXBAR12_GSEL	502D 0400h
404h	8	INPUTXBAR_INPUTXBAR12_G0	502D 0404h
408h	8	INPUTXBAR_INPUTXBAR12_G1	502D 0408h
440h	0	INPUTXBAR_INPUTXBAR13_GSEL	502D 0440h
444h	8	INPUTXBAR_INPUTXBAR13_G0	502D 0444h
448h	8	INPUTXBAR_INPUTXBAR13_G1	502D 0448h
480h	0	INPUTXBAR_INPUTXBAR14_GSEL	502D 0480h
484h	8	INPUTXBAR_INPUTXBAR14_G0	502D 0484h
488h	8	INPUTXBAR_INPUTXBAR14_G1	502D 0488h
4C0h	0	INPUTXBAR_INPUTXBAR15_GSEL	502D 04C0h
4C4h	8	INPUTXBAR_INPUTXBAR15_G0	502D 04C4h
4C8h	8	INPUTXBAR_INPUTXBAR15_G1	502D 04C8h
500h	0	INPUTXBAR_INPUTXBAR16_GSEL	502D 0500h
504h	8	INPUTXBAR_INPUTXBAR16_G0	502D 0504h
508h	8	INPUTXBAR_INPUTXBAR16_G1	502D 0508h
540h	0	INPUTXBAR_INPUTXBAR17_GSEL	502D 0540h
544h	8	INPUTXBAR_INPUTXBAR17_G0	502D 0544h
548h	8	INPUTXBAR_INPUTXBAR17_G1	502D 0548h
580h	0	INPUTXBAR_INPUTXBAR18_GSEL	502D 0580h
584h	8	INPUTXBAR_INPUTXBAR18_G0	502D 0584h
588h	8	INPUTXBAR_INPUTXBAR18_G1	502D 0588h
5C0h	0	INPUTXBAR_INPUTXBAR19_GSEL	502D 05C0h
5C4h	8	INPUTXBAR_INPUTXBAR19_G0	502D 05C4h
5C8h	8	INPUTXBAR_INPUTXBAR19_G1	502D 05C8h
600h	0	INPUTXBAR_INPUTXBAR20_GSEL	502D 0600h
604h	8	INPUTXBAR_INPUTXBAR20_G0	502D 0604h
608h	8	INPUTXBAR_INPUTXBAR20_G1	502D 0608h
640h	0	INPUTXBAR_INPUTXBAR21_GSEL	502D 0640h
644h	8	INPUTXBAR_INPUTXBAR21_G0	502D 0644h

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Table 3-1316. CONTROLSS_INPUTXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_INPUTXBAR Physical Address
648h	8	INPUTXBAR_INPUTXBAR21_G1	502D 0648h
680h	0	INPUTXBAR_INPUTXBAR22_GSEL	502D 0680h
684h	8	INPUTXBAR_INPUTXBAR22_G0	502D 0684h
688h	8	INPUTXBAR_INPUTXBAR22_G1	502D 0688h
6C0h	0	INPUTXBAR_INPUTXBAR23_GSEL	502D 06C0h
6C4h	8	INPUTXBAR_INPUTXBAR23_G0	502D 06C4h
6C8h	8	INPUTXBAR_INPUTXBAR23_G1	502D 06C8h
700h	0	INPUTXBAR_INPUTXBAR24_GSEL	502D 0700h
704h	8	INPUTXBAR_INPUTXBAR24_G0	502D 0704h
708h	8	INPUTXBAR_INPUTXBAR24_G1	502D 0708h
740h	0	INPUTXBAR_INPUTXBAR25_GSEL	502D 0740h
744h	8	INPUTXBAR_INPUTXBAR25_G0	502D 0744h
748h	8	INPUTXBAR_INPUTXBAR25_G1	502D 0748h
780h	0	INPUTXBAR_INPUTXBAR26_GSEL	502D 0780h
784h	8	INPUTXBAR_INPUTXBAR26_G0	502D 0784h
788h	8	INPUTXBAR_INPUTXBAR26_G1	502D 0788h
7C0h	0	INPUTXBAR_INPUTXBAR27_GSEL	502D 07C0h
7C4h	8	INPUTXBAR_INPUTXBAR27_G0	502D 07C4h
7C8h	8	INPUTXBAR_INPUTXBAR27_G1	502D 07C8h
800h	0	INPUTXBAR_INPUTXBAR28_GSEL	502D 0800h
804h	8	INPUTXBAR_INPUTXBAR28_G0	502D 0804h
808h	8	INPUTXBAR_INPUTXBAR28_G1	502D 0808h
840h	0	INPUTXBAR_INPUTXBAR29_GSEL	502D 0840h
844h	8	INPUTXBAR_INPUTXBAR29_G0	502D 0844h
848h	8	INPUTXBAR_INPUTXBAR29_G1	502D 0848h
880h	0	INPUTXBAR_INPUTXBAR30_GSEL	502D 0880h
884h	8	INPUTXBAR_INPUTXBAR30_G0	502D 0884h
888h	8	INPUTXBAR_INPUTXBAR30_G1	502D 0888h
8C0h	0	INPUTXBAR_INPUTXBAR31_GSEL	502D 08C0h
8C4h	8	INPUTXBAR_INPUTXBAR31_G0	502D 08C4h
8C8h	8	INPUTXBAR_INPUTXBAR31_G1	502D 08C8h

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3.14.1 CONTROLSS_INPUTXBAR_PID Registers

3.14.1.1 INPUTXBAR_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

Return to Summary Table

Table 3-1317. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0000h

Access Types Legend

Table 3-1318. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	6180h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	2h	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	14h	Not Defined

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3.14.2 CONTROLSS_INPUTXBARn_GSEL Registers

3.14.2.1 INPUTXBARn_GSEL Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x100+0x40*n* where *n* goes from 0-31 (8)

Table 3-1319. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0**N**h

Access Types Legend

Table 3-1320. GSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GSEL	RW	0h	Select input source Group:0 G0 selected1 G1 selected

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3.14.3 CONTROLSS_INPUTXBARn_G0 Registers

3.14.3.1 INPUTXBARn_G0 Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description

:

N=0x104+0x40*n* where *n* goes from 0-31 (9)

Table 3-1321. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0**N**h

Access Types Legend

Table 3-1322. G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	SEL	RW	0h	Select input source:0 G0.0 selected..x G0.x selected

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3.14.4 CONTROLSS_INPUTXBARn_G1 Registers

3.14.4.1 INPUTXBARn_G1 Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x108+0x40*n* where *n* goes from 0-31 (10)

Table 3-1323. Instance Table

Instance Name	Physical Address
CONTROLSS_INPUTXBAR	502D 0**N**h

Access Types Legend

Table 3-1324. G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	SEL	RW	0h	Select input source:0 G1.0 selected..31 G1.31 selected

3.14.5 Access Table

Table 3-1325. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

3.15 INTXBAR Registers

Table 3-1326. CONTROLSS_INTXBAR Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_INTXBAR Physical Address
0h	32	INTXBAR_PID	502D 5000h
100h	32	INTXBAR_INTXBAR0_G0	502D 5100h
104h	32	INTXBAR_INTXBAR0_G1	502D 5104h
108h	24	INTXBAR_INTXBAR0_G2	502D 5108h
10Ch	16	INTXBAR_INTXBAR0_G3	502D 510Ch
110h	16	INTXBAR_INTXBAR0_G4	502D 5110h
114h	16	INTXBAR_INTXBAR0_G5	502D 5114h
118h	8	INTXBAR_INTXBAR0_G6	502D 5118h
140h	32	INTXBAR_INTXBAR1_G0	502D 5140h
144h	32	INTXBAR_INTXBAR1_G1	502D 5144h
148h	24	INTXBAR_INTXBAR1_G2	502D 5148h
14Ch	16	INTXBAR_INTXBAR1_G3	502D 514Ch
150h	16	INTXBAR_INTXBAR1_G4	502D 5150h
154h	16	INTXBAR_INTXBAR1_G5	502D 5154h
158h	8	INTXBAR_INTXBAR1_G6	502D 5158h
180h	32	INTXBAR_INTXBAR2_G0	502D 5180h
184h	32	INTXBAR_INTXBAR2_G1	502D 5184h
188h	24	INTXBAR_INTXBAR2_G2	502D 5188h
18Ch	16	INTXBAR_INTXBAR2_G3	502D 518Ch

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Table 3-1326. CONTROLSS_INTXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_INTXBAR Physical Address
190h	16	INTXBAR_INTXBAR2_G4	502D 5190h
194h	16	INTXBAR_INTXBAR2_G5	502D 5194h
198h	8	INTXBAR_INTXBAR2_G6	502D 5198h
1C0h	32	INTXBAR_INTXBAR3_G0	502D 51C0h
1C4h	32	INTXBAR_INTXBAR3_G1	502D 51C4h
1C8h	24	INTXBAR_INTXBAR3_G2	502D 51C8h
1CCh	16	INTXBAR_INTXBAR3_G3	502D 51CCh
1D0h	16	INTXBAR_INTXBAR3_G4	502D 51D0h
1D4h	16	INTXBAR_INTXBAR3_G5	502D 51D4h
1D8h	8	INTXBAR_INTXBAR3_G6	502D 51D8h
200h	32	INTXBAR_INTXBAR4_G0	502D 5200h
204h	32	INTXBAR_INTXBAR4_G1	502D 5204h
208h	24	INTXBAR_INTXBAR4_G2	502D 5208h
20Ch	16	INTXBAR_INTXBAR4_G3	502D 520Ch
210h	16	INTXBAR_INTXBAR4_G4	502D 5210h
214h	16	INTXBAR_INTXBAR4_G5	502D 5214h
218h	8	INTXBAR_INTXBAR4_G6	502D 5218h
240h	32	INTXBAR_INTXBAR5_G0	502D 5240h
244h	32	INTXBAR_INTXBAR5_G1	502D 5244h
248h	24	INTXBAR_INTXBAR5_G2	502D 5248h
24Ch	16	INTXBAR_INTXBAR5_G3	502D 524Ch
250h	16	INTXBAR_INTXBAR5_G4	502D 5250h
254h	16	INTXBAR_INTXBAR5_G5	502D 5254h
258h	8	INTXBAR_INTXBAR5_G6	502D 5258h
280h	32	INTXBAR_INTXBAR6_G0	502D 5280h
284h	32	INTXBAR_INTXBAR6_G1	502D 5284h
288h	24	INTXBAR_INTXBAR6_G2	502D 5288h
28Ch	16	INTXBAR_INTXBAR6_G3	502D 528Ch
290h	16	INTXBAR_INTXBAR6_G4	502D 5290h
294h	16	INTXBAR_INTXBAR6_G5	502D 5294h
298h	8	INTXBAR_INTXBAR6_G6	502D 5298h
2C0h	32	INTXBAR_INTXBAR7_G0	502D 52C0h
2C4h	32	INTXBAR_INTXBAR7_G1	502D 52C4h
2C8h	24	INTXBAR_INTXBAR7_G2	502D 52C8h
2CCh	16	INTXBAR_INTXBAR7_G3	502D 52CCh
2D0h	16	INTXBAR_INTXBAR7_G4	502D 52D0h
2D4h	16	INTXBAR_INTXBAR7_G5	502D 52D4h
2D8h	8	INTXBAR_INTXBAR7_G6	502D 52D8h
300h	32	INTXBAR_INTXBAR8_G0	502D 5300h
304h	32	INTXBAR_INTXBAR8_G1	502D 5304h
308h	24	INTXBAR_INTXBAR8_G2	502D 5308h
30Ch	16	INTXBAR_INTXBAR8_G3	502D 530Ch
310h	16	INTXBAR_INTXBAR8_G4	502D 5310h
314h	16	INTXBAR_INTXBAR8_G5	502D 5314h
318h	8	INTXBAR_INTXBAR8_G6	502D 5318h
340h	32	INTXBAR_INTXBAR9_G0	502D 5340h
344h	32	INTXBAR_INTXBAR9_G1	502D 5344h

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Table 3-1326. CONTROLSS_INTXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_INTXBAR Physical Address
348h	24	INTXBAR_INTXBAR9_G2	502D 5348h
34Ch	16	INTXBAR_INTXBAR9_G3	502D 534Ch
350h	16	INTXBAR_INTXBAR9_G4	502D 5350h
354h	16	INTXBAR_INTXBAR9_G5	502D 5354h
358h	8	INTXBAR_INTXBAR9_G6	502D 5358h
380h	32	INTXBAR_INTXBAR10_G0	502D 5380h
384h	32	INTXBAR_INTXBAR10_G1	502D 5384h
388h	24	INTXBAR_INTXBAR10_G2	502D 5388h
38Ch	16	INTXBAR_INTXBAR10_G3	502D 538Ch
390h	16	INTXBAR_INTXBAR10_G4	502D 5390h
394h	16	INTXBAR_INTXBAR10_G5	502D 5394h
398h	8	INTXBAR_INTXBAR10_G6	502D 5398h
3C0h	32	INTXBAR_INTXBAR11_G0	502D 53C0h
3C4h	32	INTXBAR_INTXBAR11_G1	502D 53C4h
3C8h	24	INTXBAR_INTXBAR11_G2	502D 53C8h
3CCh	16	INTXBAR_INTXBAR11_G3	502D 53CCh
3D0h	16	INTXBAR_INTXBAR11_G4	502D 53D0h
3D4h	16	INTXBAR_INTXBAR11_G5	502D 53D4h
3D8h	8	INTXBAR_INTXBAR11_G6	502D 53D8h
400h	32	INTXBAR_INTXBAR12_G0	502D 5400h
404h	32	INTXBAR_INTXBAR12_G1	502D 5404h
408h	24	INTXBAR_INTXBAR12_G2	502D 5408h
40Ch	16	INTXBAR_INTXBAR12_G3	502D 540Ch
410h	16	INTXBAR_INTXBAR12_G4	502D 5410h
414h	16	INTXBAR_INTXBAR12_G5	502D 5414h
418h	8	INTXBAR_INTXBAR12_G6	502D 5418h
440h	32	INTXBAR_INTXBAR13_G0	502D 5440h
444h	32	INTXBAR_INTXBAR13_G1	502D 5444h
448h	24	INTXBAR_INTXBAR13_G2	502D 5448h
44Ch	16	INTXBAR_INTXBAR13_G3	502D 544Ch
450h	16	INTXBAR_INTXBAR13_G4	502D 5450h
454h	16	INTXBAR_INTXBAR13_G5	502D 5454h
458h	8	INTXBAR_INTXBAR13_G6	502D 5458h
480h	32	INTXBAR_INTXBAR14_G0	502D 5480h
484h	32	INTXBAR_INTXBAR14_G1	502D 5484h
488h	24	INTXBAR_INTXBAR14_G2	502D 5488h
48Ch	16	INTXBAR_INTXBAR14_G3	502D 548Ch
490h	16	INTXBAR_INTXBAR14_G4	502D 5490h
494h	16	INTXBAR_INTXBAR14_G5	502D 5494h
498h	8	INTXBAR_INTXBAR14_G6	502D 5498h
4C0h	32	INTXBAR_INTXBAR15_G0	502D 54C0h
4C4h	32	INTXBAR_INTXBAR15_G1	502D 54C4h
4C8h	24	INTXBAR_INTXBAR15_G2	502D 54C8h
4CCh	16	INTXBAR_INTXBAR15_G3	502D 54CCh
4D0h	16	INTXBAR_INTXBAR15_G4	502D 54D0h
4D4h	16	INTXBAR_INTXBAR15_G5	502D 54D4h
4D8h	8	INTXBAR_INTXBAR15_G6	502D 54D8h

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Table 3-1326. CONTROLSS_INTXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_INTXBAR Physical Address
500h	32	INTXBAR_INTXBAR16_G0	502D 5500h
504h	32	INTXBAR_INTXBAR16_G1	502D 5504h
508h	24	INTXBAR_INTXBAR16_G2	502D 5508h
50Ch	16	INTXBAR_INTXBAR16_G3	502D 550Ch
510h	16	INTXBAR_INTXBAR16_G4	502D 5510h
514h	16	INTXBAR_INTXBAR16_G5	502D 5514h
518h	8	INTXBAR_INTXBAR16_G6	502D 5518h
540h	32	INTXBAR_INTXBAR17_G0	502D 5540h
544h	32	INTXBAR_INTXBAR17_G1	502D 5544h
548h	24	INTXBAR_INTXBAR17_G2	502D 5548h
54Ch	16	INTXBAR_INTXBAR17_G3	502D 554Ch
550h	16	INTXBAR_INTXBAR17_G4	502D 5550h
554h	16	INTXBAR_INTXBAR17_G5	502D 5554h
558h	8	INTXBAR_INTXBAR17_G6	502D 5558h
580h	32	INTXBAR_INTXBAR18_G0	502D 5580h
584h	32	INTXBAR_INTXBAR18_G1	502D 5584h
588h	24	INTXBAR_INTXBAR18_G2	502D 5588h
58Ch	16	INTXBAR_INTXBAR18_G3	502D 558Ch
590h	16	INTXBAR_INTXBAR18_G4	502D 5590h
594h	16	INTXBAR_INTXBAR18_G5	502D 5594h
598h	8	INTXBAR_INTXBAR18_G6	502D 5598h
5C0h	32	INTXBAR_INTXBAR19_G0	502D 55C0h
5C4h	32	INTXBAR_INTXBAR19_G1	502D 55C4h
5C8h	24	INTXBAR_INTXBAR19_G2	502D 55C8h
5CCh	16	INTXBAR_INTXBAR19_G3	502D 55CCh
5D0h	16	INTXBAR_INTXBAR19_G4	502D 55D0h
5D4h	16	INTXBAR_INTXBAR19_G5	502D 55D4h
5D8h	8	INTXBAR_INTXBAR19_G6	502D 55D8h
600h	32	INTXBAR_INTXBAR20_G0	502D 5600h
604h	32	INTXBAR_INTXBAR20_G1	502D 5604h
608h	24	INTXBAR_INTXBAR20_G2	502D 5608h
60Ch	16	INTXBAR_INTXBAR20_G3	502D 560Ch
610h	16	INTXBAR_INTXBAR20_G4	502D 5610h
614h	16	INTXBAR_INTXBAR20_G5	502D 5614h
618h	8	INTXBAR_INTXBAR20_G6	502D 5618h
640h	32	INTXBAR_INTXBAR21_G0	502D 5640h
644h	32	INTXBAR_INTXBAR21_G1	502D 5644h
648h	24	INTXBAR_INTXBAR21_G2	502D 5648h
64Ch	16	INTXBAR_INTXBAR21_G3	502D 564Ch
650h	16	INTXBAR_INTXBAR21_G4	502D 5650h
654h	16	INTXBAR_INTXBAR21_G5	502D 5654h
658h	8	INTXBAR_INTXBAR21_G6	502D 5658h
680h	32	INTXBAR_INTXBAR22_G0	502D 5680h
684h	32	INTXBAR_INTXBAR22_G1	502D 5684h
688h	24	INTXBAR_INTXBAR22_G2	502D 5688h
68Ch	16	INTXBAR_INTXBAR22_G3	502D 568Ch
690h	16	INTXBAR_INTXBAR22_G4	502D 5690h

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Table 3-1326. CONTROLSS_INTXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_INTXBAR Physical Address
694h	16	INTXBAR_INTXBAR22_G5	502D 5694h
698h	8	INTXBAR_INTXBAR22_G6	502D 5698h
6C0h	32	INTXBAR_INTXBAR23_G0	502D 56C0h
6C4h	32	INTXBAR_INTXBAR23_G1	502D 56C4h
6C8h	24	INTXBAR_INTXBAR23_G2	502D 56C8h
6CCh	16	INTXBAR_INTXBAR23_G3	502D 56CCh
6D0h	16	INTXBAR_INTXBAR23_G4	502D 56D0h
6D4h	16	INTXBAR_INTXBAR23_G5	502D 56D4h
6D8h	8	INTXBAR_INTXBAR23_G6	502D 56D8h
700h	32	INTXBAR_INTXBAR24_G0	502D 5700h
704h	32	INTXBAR_INTXBAR24_G1	502D 5704h
708h	24	INTXBAR_INTXBAR24_G2	502D 5708h
70Ch	16	INTXBAR_INTXBAR24_G3	502D 570Ch
710h	16	INTXBAR_INTXBAR24_G4	502D 5710h
714h	16	INTXBAR_INTXBAR24_G5	502D 5714h
718h	8	INTXBAR_INTXBAR24_G6	502D 5718h
740h	32	INTXBAR_INTXBAR25_G0	502D 5740h
744h	32	INTXBAR_INTXBAR25_G1	502D 5744h
748h	24	INTXBAR_INTXBAR25_G2	502D 5748h
74Ch	16	INTXBAR_INTXBAR25_G3	502D 574Ch
750h	16	INTXBAR_INTXBAR25_G4	502D 5750h
754h	16	INTXBAR_INTXBAR25_G5	502D 5754h
758h	8	INTXBAR_INTXBAR25_G6	502D 5758h
780h	32	INTXBAR_INTXBAR26_G0	502D 5780h
784h	32	INTXBAR_INTXBAR26_G1	502D 5784h
788h	24	INTXBAR_INTXBAR26_G2	502D 5788h
78Ch	16	INTXBAR_INTXBAR26_G3	502D 578Ch
790h	16	INTXBAR_INTXBAR26_G4	502D 5790h
794h	16	INTXBAR_INTXBAR26_G5	502D 5794h
798h	8	INTXBAR_INTXBAR26_G6	502D 5798h
7C0h	32	INTXBAR_INTXBAR27_G0	502D 57C0h
7C4h	32	INTXBAR_INTXBAR27_G1	502D 57C4h
7C8h	24	INTXBAR_INTXBAR27_G2	502D 57C8h
7CCh	16	INTXBAR_INTXBAR27_G3	502D 57CCh
7D0h	16	INTXBAR_INTXBAR27_G4	502D 57D0h
7D4h	16	INTXBAR_INTXBAR27_G5	502D 57D4h
7D8h	8	INTXBAR_INTXBAR27_G6	502D 57D8h
800h	32	INTXBAR_INTXBAR28_G0	502D 5800h
804h	32	INTXBAR_INTXBAR28_G1	502D 5804h
808h	24	INTXBAR_INTXBAR28_G2	502D 5808h
80Ch	16	INTXBAR_INTXBAR28_G3	502D 580Ch
810h	16	INTXBAR_INTXBAR28_G4	502D 5810h
814h	16	INTXBAR_INTXBAR28_G5	502D 5814h
818h	8	INTXBAR_INTXBAR28_G6	502D 5818h
840h	32	INTXBAR_INTXBAR29_G0	502D 5840h
844h	32	INTXBAR_INTXBAR29_G1	502D 5844h
848h	24	INTXBAR_INTXBAR29_G2	502D 5848h

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Table 3-1326. CONTROLSS_INTXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_INTXBAR Physical Address
84Ch	16	INTXBAR_INTXBAR29_G3	502D 584Ch
850h	16	INTXBAR_INTXBAR29_G4	502D 5850h
854h	16	INTXBAR_INTXBAR29_G5	502D 5854h
858h	8	INTXBAR_INTXBAR29_G6	502D 5858h
880h	32	INTXBAR_INTXBAR30_G0	502D 5880h
884h	32	INTXBAR_INTXBAR30_G1	502D 5884h
888h	24	INTXBAR_INTXBAR30_G2	502D 5888h
88Ch	16	INTXBAR_INTXBAR30_G3	502D 588Ch
890h	16	INTXBAR_INTXBAR30_G4	502D 5890h
894h	16	INTXBAR_INTXBAR30_G5	502D 5894h
898h	8	INTXBAR_INTXBAR30_G6	502D 5898h
8C0h	32	INTXBAR_INTXBAR31_G0	502D 58C0h
8C4h	32	INTXBAR_INTXBAR31_G1	502D 58C4h
8C8h	24	INTXBAR_INTXBAR31_G2	502D 58C8h
8CCh	16	INTXBAR_INTXBAR31_G3	502D 58CCh
8D0h	16	INTXBAR_INTXBAR31_G4	502D 58D0h
8D4h	16	INTXBAR_INTXBAR31_G5	502D 58D4h
8D8h	8	INTXBAR_INTXBAR31_G6	502D 58D8h

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3.15.1 CONTROLSS_INTXBAR_PID Registers

3.15.1.1 INTXBAR_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

Return to Summary Table

Table 3-1327. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5000h

Access Types Legend

Table 3-1328. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	6180h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	2h	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	14h	Not Defined

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3.15.2 CONTROLSS_INTXBARn_G0 Registers

3.15.2.1 INTXBARn_G0 Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x100+0x40*n* where *n* goes from 0-31 (11)

Table 3-1329. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5**N**h

Access Types Legend

Table 3-1330. G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM INT interrupt to corresponding xbar1: PWMx.INT is selected0: PWMx.INT is de-selected

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3.15.3 CONTROLSS_INTXBARn_G1 Registers

3.15.3.1 INTXBARn_G1 Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x104+0x40*n* where *n* goes from 0-31 (12)

Table 3-1331. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5**N**h

Access Types Legend

Table 3-1332. G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM TZINT interrupt to corresponding xbar1: PWMx.TZINT is selected0: PWMx.TZINT is de-selected

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3.15.4 CONTROLSS_INTXBARn_G2 Registers

3.15.4.1 INTXBARn_G2 Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x108+0x40*n* where *n* goes from 0-31 (13)

Table 3-1333. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5**N**h

Access Types Legend

Table 3-1334. G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
24 - 0	SEL	RW	0h	Corresponding INT XBar G2 Input Select0: ADC0.INT11: ADC0.INT22: ADC0.INT33: ADC0.INT44: ADC0.EVTINT5: ADC1.INT16: ADC1.INT27: ADC1.INT38: ADC1.INT49: ADC1.EVTINT10: ADC2.INT111: ADC2.INT212: ADC2.INT313: ADC2.INT414: ADC2.EVTINT15: ADC3.INT116: ADC3.INT217: ADC3.INT318: ADC3.INT419: ADC3.EVTINT20: ADC4.INT121: ADC4.INT222: ADC4.INT323: ADC4.INT424: ADC4.EVTINT

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3.15.5 CONTROLSS_INTXBARn_G3 Registers

3.15.5.1 INTXBARn_G3 Register (Offset = 10Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x10C+0x40*n* where *n* goes from 0-31 (14)

Table 3-1335. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5**N**h

Access Types Legend

Table 3-1336. G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	Corresponding INT XBar G3 Input Select0: FSIRX0.INT1N1: FSIRX0.INT2N2: FSIRX1.INT1N3: FSIRX1.INT2N4: FSIRX2.INT1N5: FSIRX2.INT2N6: FSIRX3.INT1N7: FSIRX3.INT2N8: FSITX0.INT1N9: FSITX0.INT2N10: FSITX1.INT1N11: FSITX1.INT2N12: FSITX2.INT1N13: FSITX2.INT2N14: FSITX3.INT1N15: FSITX3.INT2N

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3.15.6 CONTROLSS_INTXBARn_G4 Registers

3.15.6.1 INTXBARn_G4 Register (Offset = 110h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x110+0x40*n* where *n* goes from 0-31 (15)

Table 3-1337. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5**N**h

Access Types Legend

Table 3-1338. G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G4 Input Select0: SD0.ERR1: SD0.FILT1.DRINT2: SD0.FILT2.DRINT3: SD0.FILT3.DRINT4: SD0.FILT4.DRINT5: SD1.ERR6: SD1.FILT1.DRINT7: SD1.FILT2.DRINT8: SD1.FILT3.DRINT9: SD1.FILT4.DRINT

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3.15.7 CONTROLSS_INTXBARn_G5 Registers

3.15.7.1 INTXBARn_G5 Register (Offset = 114h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x114+0x40*n* where *n* goes from 0-31 (16)

Table 3-1339. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5**N**h

Access Types Legend

Table 3-1340. G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	SEL	RW	0h	Corresponding INT XBar G5 Input Select0: ECAP0.INT1: ECAP1.INT2: ECAP2.INT3: ECAP3.INT4: ECAP4.INT5: ECAP5.INT6: ECAP6.INT7: ECAP7.INT8: ECAP8.INT9: ECAP9.INT

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3.15.8 CONTROLSS_INTXBARn_G6 Registers

3.15.8.1 INTXBARn_G6 Register (Offset = 118h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x118+0x40*n* where *n* goes from 0-31 (17)

Table 3-1341. Instance Table

Instance Name	Physical Address
CONTROLSS_INTXBAR	502D 5**N**h

Access Types Legend

Table 3-1342. G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	SEL	RW	0h	Corresponding INT XBar G6 Input Select0: EQEP0.INT1: EQEP1.INT2: EQEP2.INT

3.15.9 Access Table

Table 3-1343. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

3.16 MDLXBAR Registers

Table 3-1344. CONTROLSS_MDLXBAR Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_MDLXBAR Physical Address
0h	32	MDLXBAR_PID	502D 3000h
100h	32	MDLXBAR_MDLXBAR0_G0	502D 3100h
104h	32	MDLXBAR_MDLXBAR0_G1	502D 3104h
108h	32	MDLXBAR_MDLXBAR0_G2	502D 3108h
140h	32	MDLXBAR_MDLXBAR1_G0	502D 3140h
144h	32	MDLXBAR_MDLXBAR1_G1	502D 3144h
148h	32	MDLXBAR_MDLXBAR1_G2	502D 3148h
180h	32	MDLXBAR_MDLXBAR2_G0	502D 3180h
184h	32	MDLXBAR_MDLXBAR2_G1	502D 3184h
188h	32	MDLXBAR_MDLXBAR2_G2	502D 3188h
1C0h	32	MDLXBAR_MDLXBAR3_G0	502D 31C0h
1C4h	32	MDLXBAR_MDLXBAR3_G1	502D 31C4h
1C8h	32	MDLXBAR_MDLXBAR3_G2	502D 31C8h
200h	32	MDLXBAR_MDLXBAR4_G0	502D 3200h
204h	32	MDLXBAR_MDLXBAR4_G1	502D 3204h
208h	32	MDLXBAR_MDLXBAR4_G2	502D 3208h
240h	32	MDLXBAR_MDLXBAR5_G0	502D 3240h

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Table 3-1344. CONTROLSS_MDLXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_MDLXBAR Physical Address
244h	32	MDLXBAR_MDLXBAR5_G1	502D 3244h
248h	32	MDLXBAR_MDLXBAR5_G2	502D 3248h
280h	32	MDLXBAR_MDLXBAR6_G0	502D 3280h
284h	32	MDLXBAR_MDLXBAR6_G1	502D 3284h
288h	32	MDLXBAR_MDLXBAR6_G2	502D 3288h
2C0h	32	MDLXBAR_MDLXBAR7_G0	502D 32C0h
2C4h	32	MDLXBAR_MDLXBAR7_G1	502D 32C4h
2C8h	32	MDLXBAR_MDLXBAR7_G2	502D 32C8h
300h	32	MDLXBAR_MDLXBAR8_G0	502D 3300h
304h	32	MDLXBAR_MDLXBAR8_G1	502D 3304h
308h	32	MDLXBAR_MDLXBAR8_G2	502D 3308h
340h	32	MDLXBAR_MDLXBAR9_G0	502D 3340h
344h	32	MDLXBAR_MDLXBAR9_G1	502D 3344h
348h	32	MDLXBAR_MDLXBAR9_G2	502D 3348h
380h	32	MDLXBAR_MDLXBAR10_G0	502D 3380h
384h	32	MDLXBAR_MDLXBAR10_G1	502D 3384h
388h	32	MDLXBAR_MDLXBAR10_G2	502D 3388h
3C0h	32	MDLXBAR_MDLXBAR11_G0	502D 33C0h
3C4h	32	MDLXBAR_MDLXBAR11_G1	502D 33C4h
3C8h	32	MDLXBAR_MDLXBAR11_G2	502D 33C8h
400h	32	MDLXBAR_MDLXBAR12_G0	502D 3400h
404h	32	MDLXBAR_MDLXBAR12_G1	502D 3404h
408h	32	MDLXBAR_MDLXBAR12_G2	502D 3408h
440h	32	MDLXBAR_MDLXBAR13_G0	502D 3440h
444h	32	MDLXBAR_MDLXBAR13_G1	502D 3444h
448h	32	MDLXBAR_MDLXBAR13_G2	502D 3448h
480h	32	MDLXBAR_MDLXBAR14_G0	502D 3480h
484h	32	MDLXBAR_MDLXBAR14_G1	502D 3484h
488h	32	MDLXBAR_MDLXBAR14_G2	502D 3488h
4C0h	32	MDLXBAR_MDLXBAR15_G0	502D 34C0h
4C4h	32	MDLXBAR_MDLXBAR15_G1	502D 34C4h
4C8h	32	MDLXBAR_MDLXBAR15_G2	502D 34C8h

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3.16.1 CONTROLSS_MDLXBAR_PID Registers

3.16.1.1 MDLXBAR_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

Return to Summary Table

Table 3-1345. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3000h

Access Types Legend

Table 3-1346. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	6180h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	2h	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	14h	Not Defined

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3.16.2 CONTROLSS_MDLXBARn_G0 Registers

3.16.2.1 MDLXBARn_G0 Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x100+0x40*n* where *n* goes from 0-15 (18)

Table 3-1347. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3**N**h

Access Types Legend

Table 3-1348. G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar0 G0 input bit select. Input source is PWMA sclk select1: PWMA sclk bit[x] selected0: PWMA sclk bit[x] is de-selected

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3.16.3 CONTROLSS_MDLXBARn_G1 Registers

3.16.3.1 MDLXBARn_G1 Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x104+0x40*n* where *n* goes from 0-15 (19)

Table 3-1349. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3**N**h

Access Types Legend

Table 3-1350. G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar0 G1 input bit select. Input source is PWMB sclk select1: PWMB sclk bit[x] selected0: PWMB sclk bit[x] is de-selected

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3.16.4 CONTROLSS_MDLXBARn_G2 Registers

3.16.4.1 MDLXBARn_G2 Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x108+0x40*n* where *n* goes from 0-15 (20)

Table 3-1351. Instance Table

Instance Name	Physical Address
CONTROLSS_MDLXBAR	502D 3**N**h

Access Types Legend

Table 3-1352. G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	MDL XBar0 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.16.5 Access Table

Table 3-1353. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

3.17 OTTOCAL Registers

Table 3-1354. CONTROLSS_OTTOCAL[0:2] Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_OTTOCAL 0 Physical Address	CONTROLSS_OTTOCAL 1 Physical Address	CONTROLSS_OTTOCAL 2 Physical Address
42h	16	OTTOCAL_HRPWR	502E 0042h	502E 1042h	502E 2042h
44h	16	OTTOCAL_HRCAL	502E 0044h	502E 1044h	502E 2044h
46h	16	OTTOCAL_HRPRD	502E 0046h	502E 1046h	502E 2046h
48h	16	OTTOCAL_HRCNT0	502E 0048h	502E 1048h	502E 2048h
4Ah	16	OTTOCAL_HRCNT1	502E 004Ah	502E 104Ah	502E 204Ah
4Ch	16	OTTOCAL_HRMSTEP	502E 004Ch	502E 104Ch	502E 204Ch

Table 3-1355. CONTROLSS_OTTOCAL3 Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_OTTOCAL3 Physical Address
42h	16	OTTOCAL_HRPWR	502E 3042h
44h	16	OTTOCAL_HRCAL	502E 3044h
46h	16	OTTOCAL_HRPRD	502E 3046h
48h	16	OTTOCAL_HRCNT0	502E 3048h
4Ah	16	OTTOCAL_HRCNT1	502E 304Ah
4Ch	16	OTTOCAL_HRMSTEP	502E 304Ch

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3.17.1 OTTOCAL Instance Count Note

Note

n = 0 to 3 for the OTTOCAL registers defined below.

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3.17.2 CONTROLSS_OTTOCALn_HRPWR Registers

3.17.2.1 OTTOCALn_HRPWR Register (Offset = 42h) [reset = h]

Short Description: HRPWM Power Register This register is only accessible on EPWM modules with HRPWM capabilities.

Long Description:

Return to Summary Table

Table 3-1356. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0042h
CONTROLSS_OTTOCAL1	502E 1042h
CONTROLSS_OTTOCAL2	502E 2042h
CONTROLSS_OTTOCAL3	502E 3042h

Access Types Legend

Table 3-1357. HRPWR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CALPWRON	RW	0h	MEP Calibration Power Bits (only available on ePWM1) 0: Disables MEP calibration logic in the HRPWM and reduces power consumption 1: Enables MEP calibration logic
14 - 10	RESERVED	RO RRETURNS 0S		Reserved
9 - 6	CALSEL	RW	0h	EPWM Delay Line Selection for Calibration: 0xxxb Select Calibration Delay Lone (DCAL) 1000b Select Delay Line from ePWM 1 1001b Select Delay Line from ePWM 2 1010b Select Delay Line from ePWM 3 1011b Select Delay Line from ePWM 4 1100b Select Delay Line from ePWM 5 1101b Select Delay Line from ePWM 6 1110b Select Delay Line from ePWM 7 1111b Select Delay Line from ePWM 8
5	TESTSEL	RW	0h	Test Mode Select Bit: This bit selects if a dummy delay is added in Oscillator Calibration mode to help reducing frequency when small delays are used: 0b: Extra delay not added 1b: Extra delay added
4	CALSTS	RO	0h	Calibration Status Bit: This bit, when set to 1, indicates that calibration is in progress.
3	CNTSEL	RW	0h	Counter Select Bit: This bit will have an effect on when calibration starts:
2	CALSTART	RW	0h	Calibration Start/Stop Bit: 0b: Stop/Freeze Calibration 1b: Start calibration and run
1 - 0	CALMODE	RW	0h	Not used

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3.17.3 CONTROLSS_OTTOCALn_HRCAL Registers

3.17.3.1 OTTOCALn_HRCAL Register (Offset = 44h) [reset = h]

Short Description: HRPWM Calibration Register

Long Description:

Return to Summary Table

Table 3-1358. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0044h
CONTROLSS_OTTOCAL1	502E 1044h
CONTROLSS_OTTOCAL2	502E 2044h
CONTROLSS_OTTOCAL3	502E 3044h

Access Types Legend

Table 3-1359. HRCAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO RRETURNS 0S		Reserved
7 - 0	HRCAL	RW	0h	These 8-bits are used to select the number of delay elements during oscillator calibration for the calibration delay line (DCAL) only. The user configures the desired delay and then initiates a calibration run. Based on the calibration run result, the delay is increased/decreased for the next calibration run.

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3.17.4 CONTROLSS_OTTOCALn_HRPRD Registers

3.17.4.1 OTTOCALn_HRPRD Register (Offset = 46h) [reset = h]

Short Description: HRPWM Period Register

Long Description:

Return to Summary Table

Table 3-1360. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0046h
CONTROLSS_OTTOCAL1	502E 1046h
CONTROLSS_OTTOCAL2	502E 2046h
CONTROLSS_OTTOCAL3	502E 3046h

Access Types Legend

Table 3-1361. HRPRD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	HRPRD	RW	0h	The user should manually clear/set the period before starting a new calibration run.

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3.17.5 CONTROLSS_OTTOCALn_HRCNT0 Registers

3.17.5.1 OTTOCALn_HRCNT0 Register (Offset = 48h) [reset = h]

Short Description: HRPWM Counter 0 Register

Long Description:

Return to Summary Table

Table 3-1362. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 0048h
CONTROLSS_OTTOCAL1	502E 1048h
CONTROLSS_OTTOCAL2	502E 2048h
CONTROLSS_OTTOCAL3	502E 3048h

Access Types Legend

Table 3-1363. HRCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	HRCNT0	RW	0h	The HRCNT0 counter increments on every ring oscillator clock pulse.

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3.17.6 CONTROLSS_OTTOCALn_HRCNT1 Registers

3.17.6.1 OTTOCALn_HRCNT1 Register (Offset = 4Ah) [reset = h]

Short Description: HRPWM Counter 1 Register

Long Description:

Return to Summary Table

Table 3-1364. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 004Ah
CONTROLSS_OTTOCAL1	502E 104Ah
CONTROLSS_OTTOCAL2	502E 204Ah
CONTROLSS_OTTOCAL3	502E 304Ah

Access Types Legend

Table 3-1365. HRCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	HRCNT1	RW	0h	The HRCNT1 counter increments on every system clock pulse.

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3.17.7 CONTROLSS_OTTOCALn_HRMSTEP Registers

3.17.7.1 OTTOCALn_HRMSTEP Register (Offset = 4Ch) [reset = h]

Short Description: HRPWM MEP Step Register This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.

Long Description:

Return to Summary Table

Table 3-1366. Instance Table

Instance Name	Physical Address
CONTROLSS_OTTOCAL0	502E 004Ch
CONTROLSS_OTTOCAL1	502E 104Ch
CONTROLSS_OTTOCAL2	502E 204Ch
CONTROLSS_OTTOCAL3	502E 304Ch

Access Types Legend

Table 3-1367. HRMSTEP Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO RRETURNS 0S		Reserved
7 - 0	HRMSTEP	RW	0h	High Resolution MEP Step When auto-conversion is enabled (HRCNFG[AUTOCONV] = 1), This 8-bit field contains the MEP_ScaleFactor (number of MEP steps per coarse steps) used by the hardware to automatically convert the value in the CMPAHR, CMPBHR, DBFEDHR, DBREDHR , TBPHSHR, or TBPRDHR register to a scaled micro-edge delay on the high-resolution ePWM output. The value in this register is written by the SFO calibration software at the end of each calibration run.

3.17.8 Access Table

Table 3-1368. Access Type Codes

Access Type	Code	Description
RW	RW	Read / Write
RO RRETURNS0S	RO RRETURNS0S	Read returns 0s
RO	RO	Read

3.18 OUTPUTXBAR Registers

Table 3-1369. CONTROLSS_OUTPUTXBAR Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_OUTPUTXBAR Physical Address
0h	32	OUTPUTXBAR_PID	502D 8000h
10h	16	OUTPUTXBAR_OUTPUTXBAR_STATUS	502D 8010h
14h	16	OUTPUTXBAR_OUTPUTXBAR_FLAGINVERT	502D 8014h
18h	16	OUTPUTXBAR_OUTPUTXBAR_FLAG	502D 8018h
1Ch	16	OUTPUTXBAR_OUTPUTXBAR_FLAG_CLR	502D 801Ch
20h	16	OUTPUTXBAR_OUTPUTXBAR_FLAGFORCE	502D 8020h
24h	16	OUTPUTXBAR_OUTPUTXBAR_OUTLATCH	502D 8024h
28h	16	OUTPUTXBAR_OUTPUTXBAR_OUTSTRETCH	502D 8028h

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Table 3-1369. CONTROLSS_OUTPUTXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_OUTPUTXBAR Physical Address
2Ch	16	OUTPUTXBAR_OUTPUTXBAR_OUTLENGTH	502D 802Ch
30h	16	OUTPUTXBAR_OUTPUTXBAR_OUTINVERT	502D 8030h
100h	32	OUTPUTXBAR_OUTPUTXBAR0_G0	502D 8100h
104h	32	OUTPUTXBAR_OUTPUTXBAR0_G1	502D 8104h
108h	32	OUTPUTXBAR_OUTPUTXBAR0_G2	502D 8108h
10Ch	32	OUTPUTXBAR_OUTPUTXBAR0_G3	502D 810Ch
110h	32	OUTPUTXBAR_OUTPUTXBAR0_G4	502D 8110h
114h	24	OUTPUTXBAR_OUTPUTXBAR0_G5	502D 8114h
118h	24	OUTPUTXBAR_OUTPUTXBAR0_G6	502D 8118h
11Ch	24	OUTPUTXBAR_OUTPUTXBAR0_G7	502D 811Ch
120h	24	OUTPUTXBAR_OUTPUTXBAR0_G8	502D 8120h
124h	24	OUTPUTXBAR_OUTPUTXBAR0_G9	502D 8124h
128h	16	OUTPUTXBAR_OUTPUTXBAR0_G10	502D 8128h
140h	32	OUTPUTXBAR_OUTPUTXBAR1_G0	502D 8140h
144h	32	OUTPUTXBAR_OUTPUTXBAR1_G1	502D 8144h
148h	32	OUTPUTXBAR_OUTPUTXBAR1_G2	502D 8148h
14Ch	32	OUTPUTXBAR_OUTPUTXBAR1_G3	502D 814Ch
150h	32	OUTPUTXBAR_OUTPUTXBAR1_G4	502D 8150h
154h	24	OUTPUTXBAR_OUTPUTXBAR1_G5	502D 8154h
158h	24	OUTPUTXBAR_OUTPUTXBAR1_G6	502D 8158h
15Ch	24	OUTPUTXBAR_OUTPUTXBAR1_G7	502D 815Ch
160h	24	OUTPUTXBAR_OUTPUTXBAR1_G8	502D 8160h
164h	24	OUTPUTXBAR_OUTPUTXBAR1_G9	502D 8164h
168h	16	OUTPUTXBAR_OUTPUTXBAR1_G10	502D 8168h
180h	32	OUTPUTXBAR_OUTPUTXBAR2_G0	502D 8180h
184h	32	OUTPUTXBAR_OUTPUTXBAR2_G1	502D 8184h
188h	32	OUTPUTXBAR_OUTPUTXBAR2_G2	502D 8188h
18Ch	32	OUTPUTXBAR_OUTPUTXBAR2_G3	502D 818Ch
190h	32	OUTPUTXBAR_OUTPUTXBAR2_G4	502D 8190h
194h	24	OUTPUTXBAR_OUTPUTXBAR2_G5	502D 8194h
198h	24	OUTPUTXBAR_OUTPUTXBAR2_G6	502D 8198h
19Ch	24	OUTPUTXBAR_OUTPUTXBAR2_G7	502D 819Ch
1A0h	24	OUTPUTXBAR_OUTPUTXBAR2_G8	502D 81A0h
1A4h	24	OUTPUTXBAR_OUTPUTXBAR2_G9	502D 81A4h
1A8h	16	OUTPUTXBAR_OUTPUTXBAR2_G10	502D 81A8h
1C0h	32	OUTPUTXBAR_OUTPUTXBAR3_G0	502D 81C0h
1C4h	32	OUTPUTXBAR_OUTPUTXBAR3_G1	502D 81C4h
1C8h	32	OUTPUTXBAR_OUTPUTXBAR3_G2	502D 81C8h
1CCh	32	OUTPUTXBAR_OUTPUTXBAR3_G3	502D 81CCh
1D0h	32	OUTPUTXBAR_OUTPUTXBAR3_G4	502D 81D0h
1D4h	24	OUTPUTXBAR_OUTPUTXBAR3_G5	502D 81D4h
1D8h	24	OUTPUTXBAR_OUTPUTXBAR3_G6	502D 81D8h
1DCh	24	OUTPUTXBAR_OUTPUTXBAR3_G7	502D 81DCh
1E0h	24	OUTPUTXBAR_OUTPUTXBAR3_G8	502D 81E0h
1E4h	24	OUTPUTXBAR_OUTPUTXBAR3_G9	502D 81E4h
1E8h	16	OUTPUTXBAR_OUTPUTXBAR3_G10	502D 81E8h

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Table 3-1369. CONTROLSS_OUTPUTXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_OUTPUTXBAR Physical Address
200h	32	OUTPUTXBAR_OUTPUTXBAR4_G0	502D 8200h
204h	32	OUTPUTXBAR_OUTPUTXBAR4_G1	502D 8204h
208h	32	OUTPUTXBAR_OUTPUTXBAR4_G2	502D 8208h
20Ch	32	OUTPUTXBAR_OUTPUTXBAR4_G3	502D 820Ch
210h	32	OUTPUTXBAR_OUTPUTXBAR4_G4	502D 8210h
214h	24	OUTPUTXBAR_OUTPUTXBAR4_G5	502D 8214h
218h	24	OUTPUTXBAR_OUTPUTXBAR4_G6	502D 8218h
21Ch	24	OUTPUTXBAR_OUTPUTXBAR4_G7	502D 821Ch
220h	24	OUTPUTXBAR_OUTPUTXBAR4_G8	502D 8220h
224h	24	OUTPUTXBAR_OUTPUTXBAR4_G9	502D 8224h
228h	16	OUTPUTXBAR_OUTPUTXBAR4_G10	502D 8228h
240h	32	OUTPUTXBAR_OUTPUTXBAR5_G0	502D 8240h
244h	32	OUTPUTXBAR_OUTPUTXBAR5_G1	502D 8244h
248h	32	OUTPUTXBAR_OUTPUTXBAR5_G2	502D 8248h
24Ch	32	OUTPUTXBAR_OUTPUTXBAR5_G3	502D 824Ch
250h	32	OUTPUTXBAR_OUTPUTXBAR5_G4	502D 8250h
254h	24	OUTPUTXBAR_OUTPUTXBAR5_G5	502D 8254h
258h	24	OUTPUTXBAR_OUTPUTXBAR5_G6	502D 8258h
25Ch	24	OUTPUTXBAR_OUTPUTXBAR5_G7	502D 825Ch
260h	24	OUTPUTXBAR_OUTPUTXBAR5_G8	502D 8260h
264h	24	OUTPUTXBAR_OUTPUTXBAR5_G9	502D 8264h
268h	16	OUTPUTXBAR_OUTPUTXBAR5_G10	502D 8268h
280h	32	OUTPUTXBAR_OUTPUTXBAR6_G0	502D 8280h
284h	32	OUTPUTXBAR_OUTPUTXBAR6_G1	502D 8284h
288h	32	OUTPUTXBAR_OUTPUTXBAR6_G2	502D 8288h
28Ch	32	OUTPUTXBAR_OUTPUTXBAR6_G3	502D 828Ch
290h	32	OUTPUTXBAR_OUTPUTXBAR6_G4	502D 8290h
294h	24	OUTPUTXBAR_OUTPUTXBAR6_G5	502D 8294h
298h	24	OUTPUTXBAR_OUTPUTXBAR6_G6	502D 8298h
29Ch	24	OUTPUTXBAR_OUTPUTXBAR6_G7	502D 829Ch
2A0h	24	OUTPUTXBAR_OUTPUTXBAR6_G8	502D 82A0h
2A4h	24	OUTPUTXBAR_OUTPUTXBAR6_G9	502D 82A4h
2A8h	16	OUTPUTXBAR_OUTPUTXBAR6_G10	502D 82A8h
2C0h	32	OUTPUTXBAR_OUTPUTXBAR7_G0	502D 82C0h
2C4h	32	OUTPUTXBAR_OUTPUTXBAR7_G1	502D 82C4h
2C8h	32	OUTPUTXBAR_OUTPUTXBAR7_G2	502D 82C8h
2CCh	32	OUTPUTXBAR_OUTPUTXBAR7_G3	502D 82CCh
2D0h	32	OUTPUTXBAR_OUTPUTXBAR7_G4	502D 82D0h
2D4h	24	OUTPUTXBAR_OUTPUTXBAR7_G5	502D 82D4h
2D8h	24	OUTPUTXBAR_OUTPUTXBAR7_G6	502D 82D8h
2DCh	24	OUTPUTXBAR_OUTPUTXBAR7_G7	502D 82DCh
2E0h	24	OUTPUTXBAR_OUTPUTXBAR7_G8	502D 82E0h
2E4h	24	OUTPUTXBAR_OUTPUTXBAR7_G9	502D 82E4h
2E8h	16	OUTPUTXBAR_OUTPUTXBAR7_G10	502D 82E8h
300h	32	OUTPUTXBAR_OUTPUTXBAR8_G0	502D 8300h
304h	32	OUTPUTXBAR_OUTPUTXBAR8_G1	502D 8304h

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Table 3-1369. CONTROLSS_OUTPUTXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_OUTPUTXBAR Physical Address
308h	32	OUTPUTXBAR_OUTPUTXBAR8_G2	502D 8308h
30Ch	32	OUTPUTXBAR_OUTPUTXBAR8_G3	502D 830Ch
310h	32	OUTPUTXBAR_OUTPUTXBAR8_G4	502D 8310h
314h	24	OUTPUTXBAR_OUTPUTXBAR8_G5	502D 8314h
318h	24	OUTPUTXBAR_OUTPUTXBAR8_G6	502D 8318h
31Ch	24	OUTPUTXBAR_OUTPUTXBAR8_G7	502D 831Ch
320h	24	OUTPUTXBAR_OUTPUTXBAR8_G8	502D 8320h
324h	24	OUTPUTXBAR_OUTPUTXBAR8_G9	502D 8324h
328h	16	OUTPUTXBAR_OUTPUTXBAR8_G10	502D 8328h
340h	32	OUTPUTXBAR_OUTPUTXBAR9_G0	502D 8340h
344h	32	OUTPUTXBAR_OUTPUTXBAR9_G1	502D 8344h
348h	32	OUTPUTXBAR_OUTPUTXBAR9_G2	502D 8348h
34Ch	32	OUTPUTXBAR_OUTPUTXBAR9_G3	502D 834Ch
350h	32	OUTPUTXBAR_OUTPUTXBAR9_G4	502D 8350h
354h	24	OUTPUTXBAR_OUTPUTXBAR9_G5	502D 8354h
358h	24	OUTPUTXBAR_OUTPUTXBAR9_G6	502D 8358h
35Ch	24	OUTPUTXBAR_OUTPUTXBAR9_G7	502D 835Ch
360h	24	OUTPUTXBAR_OUTPUTXBAR9_G8	502D 8360h
364h	24	OUTPUTXBAR_OUTPUTXBAR9_G9	502D 8364h
368h	16	OUTPUTXBAR_OUTPUTXBAR9_G10	502D 8368h
380h	32	OUTPUTXBAR_OUTPUTXBAR10_G0	502D 8380h
384h	32	OUTPUTXBAR_OUTPUTXBAR10_G1	502D 8384h
388h	32	OUTPUTXBAR_OUTPUTXBAR10_G2	502D 8388h
38Ch	32	OUTPUTXBAR_OUTPUTXBAR10_G3	502D 838Ch
390h	32	OUTPUTXBAR_OUTPUTXBAR10_G4	502D 8390h
394h	24	OUTPUTXBAR_OUTPUTXBAR10_G5	502D 8394h
398h	24	OUTPUTXBAR_OUTPUTXBAR10_G6	502D 8398h
39Ch	24	OUTPUTXBAR_OUTPUTXBAR10_G7	502D 839Ch
3A0h	24	OUTPUTXBAR_OUTPUTXBAR10_G8	502D 83A0h
3A4h	24	OUTPUTXBAR_OUTPUTXBAR10_G9	502D 83A4h
3A8h	16	OUTPUTXBAR_OUTPUTXBAR10_G10	502D 83A8h
3C0h	32	OUTPUTXBAR_OUTPUTXBAR11_G0	502D 83C0h
3C4h	32	OUTPUTXBAR_OUTPUTXBAR11_G1	502D 83C4h
3C8h	32	OUTPUTXBAR_OUTPUTXBAR11_G2	502D 83C8h
3CCh	32	OUTPUTXBAR_OUTPUTXBAR11_G3	502D 83CCh
3D0h	32	OUTPUTXBAR_OUTPUTXBAR11_G4	502D 83D0h
3D4h	24	OUTPUTXBAR_OUTPUTXBAR11_G5	502D 83D4h
3D8h	24	OUTPUTXBAR_OUTPUTXBAR11_G6	502D 83D8h
3DCh	24	OUTPUTXBAR_OUTPUTXBAR11_G7	502D 83DCh
3E0h	24	OUTPUTXBAR_OUTPUTXBAR11_G8	502D 83E0h
3E4h	24	OUTPUTXBAR_OUTPUTXBAR11_G9	502D 83E4h
3E8h	16	OUTPUTXBAR_OUTPUTXBAR11_G10	502D 83E8h
400h	32	OUTPUTXBAR_OUTPUTXBAR12_G0	502D 8400h
404h	32	OUTPUTXBAR_OUTPUTXBAR12_G1	502D 8404h
408h	32	OUTPUTXBAR_OUTPUTXBAR12_G2	502D 8408h
40Ch	32	OUTPUTXBAR_OUTPUTXBAR12_G3	502D 840Ch

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Table 3-1369. CONTROLSS_OUTPUTXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_OUTPUTXBAR Physical Address
410h	32	OUTPUTXBAR_OUTPUTXBAR12_G4	502D 8410h
414h	24	OUTPUTXBAR_OUTPUTXBAR12_G5	502D 8414h
418h	24	OUTPUTXBAR_OUTPUTXBAR12_G6	502D 8418h
41Ch	24	OUTPUTXBAR_OUTPUTXBAR12_G7	502D 841Ch
420h	24	OUTPUTXBAR_OUTPUTXBAR12_G8	502D 8420h
424h	24	OUTPUTXBAR_OUTPUTXBAR12_G9	502D 8424h
428h	16	OUTPUTXBAR_OUTPUTXBAR12_G10	502D 8428h
440h	32	OUTPUTXBAR_OUTPUTXBAR13_G0	502D 8440h
444h	32	OUTPUTXBAR_OUTPUTXBAR13_G1	502D 8444h
448h	32	OUTPUTXBAR_OUTPUTXBAR13_G2	502D 8448h
44Ch	32	OUTPUTXBAR_OUTPUTXBAR13_G3	502D 844Ch
450h	32	OUTPUTXBAR_OUTPUTXBAR13_G4	502D 8450h
454h	24	OUTPUTXBAR_OUTPUTXBAR13_G5	502D 8454h
458h	24	OUTPUTXBAR_OUTPUTXBAR13_G6	502D 8458h
45Ch	24	OUTPUTXBAR_OUTPUTXBAR13_G7	502D 845Ch
460h	24	OUTPUTXBAR_OUTPUTXBAR13_G8	502D 8460h
464h	24	OUTPUTXBAR_OUTPUTXBAR13_G9	502D 8464h
468h	16	OUTPUTXBAR_OUTPUTXBAR13_G10	502D 8468h
480h	32	OUTPUTXBAR_OUTPUTXBAR14_G0	502D 8480h
484h	32	OUTPUTXBAR_OUTPUTXBAR14_G1	502D 8484h
488h	32	OUTPUTXBAR_OUTPUTXBAR14_G2	502D 8488h
48Ch	32	OUTPUTXBAR_OUTPUTXBAR14_G3	502D 848Ch
490h	32	OUTPUTXBAR_OUTPUTXBAR14_G4	502D 8490h
494h	24	OUTPUTXBAR_OUTPUTXBAR14_G5	502D 8494h
498h	24	OUTPUTXBAR_OUTPUTXBAR14_G6	502D 8498h
49Ch	24	OUTPUTXBAR_OUTPUTXBAR14_G7	502D 849Ch
4A0h	24	OUTPUTXBAR_OUTPUTXBAR14_G8	502D 84A0h
4A4h	24	OUTPUTXBAR_OUTPUTXBAR14_G9	502D 84A4h
4A8h	16	OUTPUTXBAR_OUTPUTXBAR14_G10	502D 84A8h
4C0h	32	OUTPUTXBAR_OUTPUTXBAR15_G0	502D 84C0h
4C4h	32	OUTPUTXBAR_OUTPUTXBAR15_G1	502D 84C4h
4C8h	32	OUTPUTXBAR_OUTPUTXBAR15_G2	502D 84C8h
4CCh	32	OUTPUTXBAR_OUTPUTXBAR15_G3	502D 84CCh
4D0h	32	OUTPUTXBAR_OUTPUTXBAR15_G4	502D 84D0h
4D4h	24	OUTPUTXBAR_OUTPUTXBAR15_G5	502D 84D4h
4D8h	24	OUTPUTXBAR_OUTPUTXBAR15_G6	502D 84D8h
4DCh	24	OUTPUTXBAR_OUTPUTXBAR15_G7	502D 84DCh
4E0h	24	OUTPUTXBAR_OUTPUTXBAR15_G8	502D 84E0h
4E4h	24	OUTPUTXBAR_OUTPUTXBAR15_G9	502D 84E4h
4E8h	16	OUTPUTXBAR_OUTPUTXBAR15_G10	502D 84E8h

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3.18.1 CONTROLSS_OUTPUTXBAR_PID Registers

3.18.1.1 OUTPUTXBAR_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

Return to Summary Table

Table 3-1370. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8000h

Access Types Legend

Table 3-1371. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	6180h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	2h	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	14h	Not Defined

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3.18.2 CONTROLSS_OUTPUTXBAR_STATUS Registers

3.18.2.1 OUTPUTXBAR_STATUS Register (Offset = 10h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 3-1372. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8010h

Access Types Legend

Table 3-1373. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	STS	RO	0h	Status

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3.18.3 CONTROLSS_OUTPUTXBAR_FLAGINVERT Registers

3.18.3.1 FLAGINVERT Register (Offset = 14h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1374. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8014h

Access Types Legend

Table 3-1375. FLAGINVERT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	INVERT	RW	0h	FlagInvert

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3.18.4 CONTROLSS_OUTPUTXBAR_FLAG Registers

3.18.4.1 OUTPUTXBAR_FLAG Register (Offset = 18h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1376. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8018h

Access Types Legend

Table 3-1377. FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15	RW	0h	output xbar flag
14	BIT14	RW	0h	output xbar flag
13	BIT13	RW	0h	output xbar flag
12	BIT12	RW	0h	output xbar flag
11	BIT11	RW	0h	output xbar flag
10	BIT10	RW	0h	output xbar flag
9	BIT9	RW	0h	output xbar flag
8	BIT8	RW	0h	output xbar flag
7	BIT7	RW	0h	output xbar flag
6	BIT6	RW	0h	output xbar flag
5	BIT5	RW	0h	output xbar flag
4	BIT4	RW	0h	output xbar flag
3	BIT3	RW	0h	output xbar flag
2	BIT2	RW	0h	output xbar flag
1	BIT1	RW	0h	output xbar flag
0	BIT0	RW	0h	output xbar flag

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3.18.5 CONTROLSS_OUTPUTXBAR_FLAG_CLR Registers

3.18.5.1 OUTPUTXBAR_FLAG_CLR Register (Offset = 1Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1378. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 801Ch

Access Types Legend

Table 3-1379. FLAG_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIT15	RW	0h	output xbar flag clear
14	BIT14	RW	0h	output xbar flag clear
13	BIT13	RW	0h	output xbar flag clear
12	BIT12	RW	0h	output xbar flag clear
11	BIT11	RW	0h	output xbar flag clear
10	BIT10	RW	0h	output xbar flag clear
9	BIT9	RW	0h	output xbar flag clear
8	BIT8	RW	0h	output xbar flag clear
7	BIT7	RW	0h	output xbar flag clear
6	BIT6	RW	0h	output xbar flag clear
5	BIT5	RW	0h	output xbar flag clear
4	BIT4	RW	0h	output xbar flag clear
3	BIT3	RW	0h	output xbar flag clear
2	BIT2	RW	0h	output xbar flag clear
1	BIT1	RW	0h	output xbar flag clear
0	BIT0	RW	0h	output xbar flag clear

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3.18.6 CONTROLSS_OUTPUTXBAR_FLAGFORCE Registers

3.18.6.1 OUTPUTXBAR_FLAGFORCE Register (Offset = 20h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1380. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8020h

Access Types Legend

Table 3-1381. FLAGFORCE Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	FRC	RW	0h	FlagForce

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3.18.7 CONTROLSS_OUTPUTXBAR_OUTLATCH Registers

3.18.7.1 OUTPUTXBAR_OUTLATCH Register (Offset = 24h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1382. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8024h

Access Types Legend

Table 3-1383. OUTLATCH Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	LATCHSEL	RW	0h	OutLatch

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3.18.8 CONTROLSS_OUTPUTXBAR_OUTSTRETCH Registers

3.18.8.1 OUTPUTXBAR_OUTSTRETCH Register (Offset = 28h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1384. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8028h

Access Types Legend

Table 3-1385. OUTSTRETCH Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	STRETCHSEL	RW	0h	OutStretch

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3.18.9 CONTROLSS_OUTPUTXBAR_OUTLENGTH Registers

3.18.9.1 OUTPUTXBAR_OUTLENGTH Register (Offset = 2Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1386. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 802Ch

Access Types Legend

Table 3-1387. OUTLENGTH Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	LENGTHSEL	RW	0h	OutLength

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3.18.10 CONTROLSS_OUTPUTXBAR_OUTINVERT Registers

3.18.10.1 OUTPUTXBAR_OUTINVERT Register (Offset = 30h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1388. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8030h

Access Types Legend

Table 3-1389. OUTINVERT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	OUTINVERT	RW	0h	OutInvert

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3.18.11 CONTROLSS_OUTPUTXBARn_G0 Registers

3.18.11.1 OUTPUTXBARn_G0 Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x100+0x40*n* where *n* goes from 0-15 (21)

Table 3-1390. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8**N**h

Access Types Legend

Table 3-1391. G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G0: PWM XBar0 G0 input bit select. Input source is PWM[x].TRIPOUT1: PWM[x] TRIPOUT selected0: PWM[x] TRIPOUT is de-selected

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3.18.12 CONTROLSS_OUTPUTXBARn_G1 Registers

3.18.12.1 OUTPUTXBARn_G1 Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x104+0x40*n* where *n* goes from 0-15 (22)

Table 3-1392. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8**N**h

Access Types Legend

Table 3-1393. G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G1: OUTPUT XBar0 G1 input bit select. Input source is PWM[x].SOCA1: PWM[x] SOCA selected0: PWM[x] SOCA is de-selected

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3.18.13 CONTROLSS_OUTPUTXBARn_G2 Registers

3.18.13.1 OUTPUTXBARn_G2 Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x108+0x40*n* where *n* goes from 0-15 (23)

Table 3-1394. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8**N**h

Access Types Legend

Table 3-1395. G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G2: OUTPUT XBar0 G2 input bit select. Input source is PWM[x].SOCB1: PWM[x] SOCB selected0: PWM[x] SOCB is de-selected

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3.18.14 CONTROLSS_OUTPUTXBARn_G3 Registers

3.18.14.1 OUTPUTXBARn_G3 Register (Offset = 10Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x10C+0x40*n* where *n* goes from 0-15 (24)

Table 3-1396. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8**N**h

Access Types Legend

Table 3-1397. G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G3: OUTPUT XBar0 G3 input bit select. Input source is DEL[x].ACTIVE1: DEL[x] ACTIVE selected0: DEL[x] ACTIVE is de-selected

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3.18.15 CONTROLSS_OUTPUTXBARn_G4 Registers

3.18.15.1 OUTPUTXBARn_G4 Register (Offset = 110h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x110+0x40*n* where *n* goes from 0-15 (25)

Table 3-1398. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8**N**h

Access Types Legend

Table 3-1399. G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	G4: OUTPUT XBar0 G4 input bit select. Input source is DEL[x].TRIP1: DEL[x] TRIP selected0: DEL[x] TRIP is de-selected

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3.18.16 CONTROLSS_OUTPUTXBARn_G5 Registers

3.18.16.1 OUTPUTXBARn_G5 Register (Offset = 114h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x114+0x40*n* where *n* goes from 0-15 (26)

Table 3-1400. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8**N**h

Access Types Legend

Table 3-1401. G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	G5: OUTPUT XBar0 G5 input bit select.0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

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3.18.17 CONTROLSS_OUTPUTXBARn_G6 Registers

3.18.17.1 OUTPUTXBARn_G6 Register (Offset = 118h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x118+0x40*n* where *n* goes from 0-15 (27)

Table 3-1402. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8**N**h

Access Types Legend

Table 3-1403. G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G6: OUTPUT XBar0 G6 Input Select0: CMP12SS0.CTRIPOUTL1: CMP12SS0.CTRIPOUTH2: CMP12SS1.CTRIPOUTL3: CMP12SS1.CTRIPOUTH4: CMP12SS2.CTRIPOUTL5: CMP12SS2.CTRIPOUTH6: CMP12SS3.CTRIPOUTL7: CMP12SS3.CTRIPOUTH8: CMP12SS4.CTRIPOUTL9: CMP12SS4.CTRIPOUTH10: CMP12SS5.CTRIPOUTL11: CMP12SS5.CTRIPOUTH12: CMP12SS6.CTRIPOUTL13: CMP12SS6.CTRIPOUTH14: CMP12SS7.CTRIPOUTL15: CMP12SS7.CTRIPOUTH16: CMP12SS8.CTRIPOUTL17: CMP12SS8.CTRIPOUTH18: CMP12SS9.CTRIPOUTL19: CMP12SS9.CTRIPOUTH

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3.18.18 CONTROLSS_OUTPUTXBARn_G7 Registers

3.18.18.1 OUTPUTXBARn_G7 Register (Offset = 11Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x11C+0x40**n* where *n* goes from 0-15 (28)

Table 3-1404. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8**N**h

Access Types Legend

Table 3-1405. G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G7: OUTPUT XBar0 G7 Input Select0: CMP8SS0.CTRIPOUTL1: CMP8SS0.CTRIPOUTH2: CMP8SS1.CTRIPOUTL3: CMP8SS1.CTRIPOUTH4: CMP8SS2.CTRIPOUTL5: CMP8SS2.CTRIPOUTH6: CMP8SS3.CTRIPOUTL7: CMP8SS3.CTRIPOUTH8: CMP8SS4.CTRIPOUTL9: CMP8SS4.CTRIPOUTH10: CMP8SS5.CTRIPOUTL11: CMP8SS5.CTRIPOUTH12: CMP8SS6.CTRIPOUTL13: CMP8SS6.CTRIPOUTH14: CMP8SS7.CTRIPOUTL15: CMP8SS7.CTRIPOUTH16: CMP8SS8.CTRIPOUTL17: CMP8SS8.CTRIPOUTH18: CMP8SS9.CTRIPOUTL19: CMP8SS9.CTRIPOUTH

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3.18.19 CONTROLSS_OUTPUTXBARn_G8 Registers

3.18.19.1 OUTPUTXBARn_G8 Register (Offset = 120h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x120+0x40*n* where *n* goes from 0-15 (29)

Table 3-1406. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8**N**h

Access Types Legend

Table 3-1407. G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G8: OUTPUT XBar0 G8 Input Select0: ADC0.EVT11: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1 EVT48: ADC2.EVT19: ADC2 EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

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3.18.20 CONTROLSS_OUTPUTXBARn_G9 Registers

3.18.20.1 OUTPUTXBARn_G9 Register (Offset = 124h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x124+0x40*n* where *n* goes from 0-15 (30)

Table 3-1408. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8**N**h

Access Types Legend

Table 3-1409. G9 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	G9: OUTPUT XBar0 G9 Input Select0: PWMSyncOutXBar.SYNCOUT01: PWMSyncOutXBar.SYNCOUT12: PWMSyncOutXBar.SYNCOUT23: PWMSyncOutXBar.SYNCOUT34: EQEP0.I_OUT5: EQEP0.S_OUT6: EQEP1.I_OUT7: EQEP1.S_OUT8: EQEP2.I_OUT9: EQEP2.S_OUT10: ECAP0.OUT11: ECAP1.OUT12: ECAP2.OUT13: ECAP3.OUT14: ECAP4.OUT15: ECAP5.OUT16: ECAP6.OUT17: ECAP7.OUT18: ECAP8.OUT19: ECAP9.OUT

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3.18.21 CONTROLSS_OUTPUTXBARn_G10 Registers

3.18.21.1 OUTPUTXBARn_G10 Register (Offset = 128h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x128+0x40*n* where *n* goes from 0-15 (31)

Table 3-1410. Instance Table

Instance Name	Physical Address
CONTROLSS_OUTPUTXBAR	502D 8**N**h

Access Types Legend

Table 3-1411. G10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SEL	RW	0h	G10: OUTPUT XBar0 G10 Input Select3:0: FSIRX0.RX_TRIG07:4: FSIRX1.RX_TRIG011:8: FSIRX2.RX_TRIG015:12: FSIRX3.RX_TRIG0

3.18.22 Access Table

Table 3-1412. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

3.19 ICLXBAR Registers

Table 3-1413. CONTROLSS_ICLXBAR Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_ICLXBAR Physical Address
0h	32	ICLXBAR_PID	502D 4000h
100h	32	ICLXBAR_ICLXBAR0_G0	502D 4100h
104h	32	ICLXBAR_ICLXBAR0_G1	502D 4104h
108h	32	ICLXBAR_ICLXBAR0_G2	502D 4108h
140h	32	ICLXBAR_ICLXBAR1_G0	502D 4140h
144h	32	ICLXBAR_ICLXBAR1_G1	502D 4144h
148h	32	ICLXBAR_ICLXBAR1_G2	502D 4148h
180h	32	ICLXBAR_ICLXBAR2_G0	502D 4180h
184h	32	ICLXBAR_ICLXBAR2_G1	502D 4184h
188h	32	ICLXBAR_ICLXBAR2_G2	502D 4188h
1C0h	32	ICLXBAR_ICLXBAR3_G0	502D 41C0h
1C4h	32	ICLXBAR_ICLXBAR3_G1	502D 41C4h
1C8h	32	ICLXBAR_ICLXBAR3_G2	502D 41C8h
200h	32	ICLXBAR_ICLXBAR4_G0	502D 4200h
204h	32	ICLXBAR_ICLXBAR4_G1	502D 4204h
208h	32	ICLXBAR_ICLXBAR4_G2	502D 4208h
240h	32	ICLXBAR_ICLXBAR5_G0	502D 4240h
244h	32	ICLXBAR_ICLXBAR5_G1	502D 4244h

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Table 3-1413. CONTROLSS_ICLXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_ICLXBAR Physical Address
248h	32	ICLXBAR_ICLXBAR5_G2	502D 4248h
280h	32	ICLXBAR_ICLXBAR6_G0	502D 4280h
284h	32	ICLXBAR_ICLXBAR6_G1	502D 4284h
288h	32	ICLXBAR_ICLXBAR6_G2	502D 4288h
2C0h	32	ICLXBAR_ICLXBAR7_G0	502D 42C0h
2C4h	32	ICLXBAR_ICLXBAR7_G1	502D 42C4h
2C8h	32	ICLXBAR_ICLXBAR7_G2	502D 42C8h
300h	32	ICLXBAR_ICLXBAR8_G0	502D 4300h
304h	32	ICLXBAR_ICLXBAR8_G1	502D 4304h
308h	32	ICLXBAR_ICLXBAR8_G2	502D 4308h
340h	32	ICLXBAR_ICLXBAR9_G0	502D 4340h
344h	32	ICLXBAR_ICLXBAR9_G1	502D 4344h
348h	32	ICLXBAR_ICLXBAR9_G2	502D 4348h
380h	32	ICLXBAR_ICLXBAR10_G0	502D 4380h
384h	32	ICLXBAR_ICLXBAR10_G1	502D 4384h
388h	32	ICLXBAR_ICLXBAR10_G2	502D 4388h
3C0h	32	ICLXBAR_ICLXBAR11_G0	502D 43C0h
3C4h	32	ICLXBAR_ICLXBAR11_G1	502D 43C4h
3C8h	32	ICLXBAR_ICLXBAR11_G2	502D 43C8h
400h	32	ICLXBAR_ICLXBAR12_G0	502D 4400h
404h	32	ICLXBAR_ICLXBAR12_G1	502D 4404h
408h	32	ICLXBAR_ICLXBAR12_G2	502D 4408h
440h	32	ICLXBAR_ICLXBAR13_G0	502D 4440h
444h	32	ICLXBAR_ICLXBAR13_G1	502D 4444h
448h	32	ICLXBAR_ICLXBAR13_G2	502D 4448h
480h	32	ICLXBAR_ICLXBAR14_G0	502D 4480h
484h	32	ICLXBAR_ICLXBAR14_G1	502D 4484h
488h	32	ICLXBAR_ICLXBAR14_G2	502D 4488h
4C0h	32	ICLXBAR_ICLXBAR15_G0	502D 44C0h
4C4h	32	ICLXBAR_ICLXBAR15_G1	502D 44C4h
4C8h	32	ICLXBAR_ICLXBAR15_G2	502D 44C8h

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3.19.1 CONTROLSS_ICLXBAR_PID Registers

3.19.1.1 ICLXBAR_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

Return to Summary Table

Table 3-1414. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4000h

Access Types Legend

Table 3-1415. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	6180h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	2h	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	14h	Not Defined

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3.19.2 CONTROLSS_ICLXBARn_G0 Registers

3.19.2.1 ICLXBARn_G0 Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x100+0x40*n* where *n* goes from 0-15 (32)

Table 3-1416. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4**N**h

Access Types Legend

Table 3-1417. G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar0 G0 input bit select. Input source is PWMA hr select1: PWMA hr bit[x] selected0: PWMA hr bit[x] is de-selected

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3.19.3 CONTROLSS_ICLXBARn_G1 Registers

3.19.3.1 ICLXBARn_G1 Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x104+0x40*n* where *n* goes from 0-15 (33)

Table 3-1418. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4**N**h

Access Types Legend

Table 3-1419. G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar0 G1 input bit select. Input source is PWMB hr select1: PWMB hr bit[x] selected0: PWMB hr bit[x] is de-selected

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3.19.4 CONTROLSS_ICLXBARn_G2 Registers

3.19.4.1 ICLXBARn_G2 Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x108+0x40*n* where *n* goes from 0-15 (34)

Table 3-1420. Instance Table

Instance Name	Physical Address
CONTROLSS_ICLXBAR	502D 4**N**h

Access Types Legend

Table 3-1421. G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ICL XBar0 G2 input bit select. Input source is ICSS GPO selecty=0 when x =0 to 15, y=1 when x=16 to 311: ICSS_PORT[y].GPO[x] selected.0: ICSS_PORT[y].GPO[x] is de-selected

3.19.5 Access Table

Table 3-1422. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

3.20 PWMSYNCOUTXBAR Registers

Table 3-1423. CONTROLSS_PWMSYNCOUTXBAR Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_PWMSYNCOUTXBAR Physical Address
0h	32	PWMSYNCOUTXBAR_PID	502D 2000h
100h	32	PWMSYNCOUTXBAR_PWMSYNCOUTXBAR0_G0	502D 2100h
140h	32	PWMSYNCOUTXBAR_PWMSYNCOUTXBAR1_G0	502D 2140h
180h	32	PWMSYNCOUTXBAR_PWMSYNCOUTXBAR2_G0	502D 2180h
1C0h	32	PWMSYNCOUTXBAR_PWMSYNCOUTXBAR3_G0	502D 21C0h

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3.20.1 CONTROLSS_PWMSYNCOUTXBAR_PID Registers

3.20.1.1 PWMSYNCOUTXBAR_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

Return to Summary Table

Table 3-1424. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTXBAR	502D 2000h

Access Types Legend

Table 3-1425. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	6180h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	2h	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	14h	Not Defined

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3.20.2 CONTROLSS_PWMSYNCOUTXBAR0_G0 Registers

3.20.2.1 PWMSYNCOUTXBAR0_G0 Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1426. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTXBAR	502D 2100h

Access Types Legend

Table 3-1427. G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM pwmsyncout xbar0 select1: PWM[x] SYNCOUT selected0: PWM[x] SYNCOUT is de-selected

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3.20.3 CONTROLSS_PWMSYNCOUTXBAR1_G0 Registers

3.20.3.1 PWMSYNCOUTXBAR1_G0 Register (Offset = 140h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1428. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTXBAR	502D 2140h

Access Types Legend

Table 3-1429. G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM pwmsyncout xbar1 select1: PWM[x] SYNCOUT selected0: PWM[x] SYNCOUT is de-selected

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3.20.4 CONTROLSS_PWMSYNCOUTXBAR2_G0 Registers

3.20.4.1 PWMSYNCOUTXBAR2_G0 Register (Offset = 180h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1430. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTXBAR	502D 2180h

Access Types Legend

Table 3-1431. G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM pwmsyncout xbar2 select1: PWM[x] SYNCOUT selected0: PWM[x] SYNCOUT is de-selected

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3.20.5 CONTROLSS_PWMSYNCOUTXBAR3_G0 Registers

3.20.5.1 PWMSYNCOUTXBAR3_G0 Register (Offset = 1C0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1432. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMSYNCOUTXBAR	502D 21C0h

Access Types Legend

Table 3-1433. G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	ETPWM pwmsyncout xbar3 select1: PWM[x] SYNCOUT selected0: PWM[x] SYNCOUT is de-selected

3.20.6 Access Table

Table 3-1434. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

3.21 PWMXBAR Registers

Table 3-1435. CONTROLSS_PWMXBAR Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_PWMXBAR Physical Address
0h	32	PWMXBAR_PID	502D 1000h
10h	32	PWMXBAR_PWMXBAR_STATUS	502D 1010h
14h	32	PWMXBAR_PWMXBAR_FLAGINVERT	502D 1014h
18h	32	PWMXBAR_PWMXBAR_FLAG	502D 1018h
1Ch	32	PWMXBAR_PWMXBAR_FLAG_CLR	502D 101Ch
100h	24	PWMXBAR_PWMXBAR0_G0	502D 1100h
104h	24	PWMXBAR_PWMXBAR0_G1	502D 1104h
108h	24	PWMXBAR_PWMXBAR0_G2	502D 1108h
10Ch	24	PWMXBAR_PWMXBAR0_G3	502D 110Ch
110h	32	PWMXBAR_PWMXBAR0_G4	502D 1110h
114h	32	PWMXBAR_PWMXBAR0_G5	502D 1114h
118h	32	PWMXBAR_PWMXBAR0_G6	502D 1118h
11Ch	32	PWMXBAR_PWMXBAR0_G7	502D 111Ch
120h	32	PWMXBAR_PWMXBAR0_G8	502D 1120h
140h	24	PWMXBAR_PWMXBAR1_G0	502D 1140h
144h	24	PWMXBAR_PWMXBAR1_G1	502D 1144h
148h	24	PWMXBAR_PWMXBAR1_G2	502D 1148h
14Ch	24	PWMXBAR_PWMXBAR1_G3	502D 114Ch
150h	32	PWMXBAR_PWMXBAR1_G4	502D 1150h
154h	32	PWMXBAR_PWMXBAR1_G5	502D 1154h

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Table 3-1435. CONTROLSS_PWMXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_PWMXBAR Physical Address
158h	32	PWMXBAR_PWMXBAR1_G6	502D 1158h
15Ch	32	PWMXBAR_PWMXBAR1_G7	502D 115Ch
160h	32	PWMXBAR_PWMXBAR1_G8	502D 1160h
180h	24	PWMXBAR_PWMXBAR2_G0	502D 1180h
184h	24	PWMXBAR_PWMXBAR2_G1	502D 1184h
188h	24	PWMXBAR_PWMXBAR2_G2	502D 1188h
18Ch	24	PWMXBAR_PWMXBAR2_G3	502D 118Ch
190h	32	PWMXBAR_PWMXBAR2_G4	502D 1190h
194h	32	PWMXBAR_PWMXBAR2_G5	502D 1194h
198h	32	PWMXBAR_PWMXBAR2_G6	502D 1198h
19Ch	32	PWMXBAR_PWMXBAR2_G7	502D 119Ch
1A0h	32	PWMXBAR_PWMXBAR2_G8	502D 11A0h
1C0h	24	PWMXBAR_PWMXBAR3_G0	502D 11C0h
1C4h	24	PWMXBAR_PWMXBAR3_G1	502D 11C4h
1C8h	24	PWMXBAR_PWMXBAR3_G2	502D 11C8h
1CCh	24	PWMXBAR_PWMXBAR3_G3	502D 11CCh
1D0h	32	PWMXBAR_PWMXBAR3_G4	502D 11D0h
1D4h	32	PWMXBAR_PWMXBAR3_G5	502D 11D4h
1D8h	32	PWMXBAR_PWMXBAR3_G6	502D 11D8h
1DCh	32	PWMXBAR_PWMXBAR3_G7	502D 11DCh
1E0h	32	PWMXBAR_PWMXBAR3_G8	502D 11E0h
200h	24	PWMXBAR_PWMXBAR4_G0	502D 1200h
204h	24	PWMXBAR_PWMXBAR4_G1	502D 1204h
208h	24	PWMXBAR_PWMXBAR4_G2	502D 1208h
20Ch	24	PWMXBAR_PWMXBAR4_G3	502D 120Ch
210h	32	PWMXBAR_PWMXBAR4_G4	502D 1210h
214h	32	PWMXBAR_PWMXBAR4_G5	502D 1214h
218h	32	PWMXBAR_PWMXBAR4_G6	502D 1218h
21Ch	32	PWMXBAR_PWMXBAR4_G7	502D 121Ch
220h	32	PWMXBAR_PWMXBAR4_G8	502D 1220h
240h	24	PWMXBAR_PWMXBAR5_G0	502D 1240h
244h	24	PWMXBAR_PWMXBAR5_G1	502D 1244h
248h	24	PWMXBAR_PWMXBAR5_G2	502D 1248h
24Ch	24	PWMXBAR_PWMXBAR5_G3	502D 124Ch
250h	32	PWMXBAR_PWMXBAR5_G4	502D 1250h
254h	32	PWMXBAR_PWMXBAR5_G5	502D 1254h
258h	32	PWMXBAR_PWMXBAR5_G6	502D 1258h
25Ch	32	PWMXBAR_PWMXBAR5_G7	502D 125Ch
260h	32	PWMXBAR_PWMXBAR5_G8	502D 1260h
280h	24	PWMXBAR_PWMXBAR6_G0	502D 1280h
284h	24	PWMXBAR_PWMXBAR6_G1	502D 1284h
288h	24	PWMXBAR_PWMXBAR6_G2	502D 1288h
28Ch	24	PWMXBAR_PWMXBAR6_G3	502D 128Ch
290h	32	PWMXBAR_PWMXBAR6_G4	502D 1290h
294h	32	PWMXBAR_PWMXBAR6_G5	502D 1294h
298h	32	PWMXBAR_PWMXBAR6_G6	502D 1298h

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Table 3-1435. CONTROLSS_PWMXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_PWMXBAR Physical Address
29Ch	32	PWMXBAR_PWMXBAR6_G7	502D 129Ch
2A0h	32	PWMXBAR_PWMXBAR6_G8	502D 12A0h
2C0h	24	PWMXBAR_PWMXBAR7_G0	502D 12C0h
2C4h	24	PWMXBAR_PWMXBAR7_G1	502D 12C4h
2C8h	24	PWMXBAR_PWMXBAR7_G2	502D 12C8h
2CCh	24	PWMXBAR_PWMXBAR7_G3	502D 12CCh
2D0h	32	PWMXBAR_PWMXBAR7_G4	502D 12D0h
2D4h	32	PWMXBAR_PWMXBAR7_G5	502D 12D4h
2D8h	32	PWMXBAR_PWMXBAR7_G6	502D 12D8h
2DCh	32	PWMXBAR_PWMXBAR7_G7	502D 12DCh
2E0h	32	PWMXBAR_PWMXBAR7_G8	502D 12E0h
300h	24	PWMXBAR_PWMXBAR8_G0	502D 1300h
304h	24	PWMXBAR_PWMXBAR8_G1	502D 1304h
308h	24	PWMXBAR_PWMXBAR8_G2	502D 1308h
30Ch	24	PWMXBAR_PWMXBAR8_G3	502D 130Ch
310h	32	PWMXBAR_PWMXBAR8_G4	502D 1310h
314h	32	PWMXBAR_PWMXBAR8_G5	502D 1314h
318h	32	PWMXBAR_PWMXBAR8_G6	502D 1318h
31Ch	32	PWMXBAR_PWMXBAR8_G7	502D 131Ch
320h	32	PWMXBAR_PWMXBAR8_G8	502D 1320h
340h	24	PWMXBAR_PWMXBAR9_G0	502D 1340h
344h	24	PWMXBAR_PWMXBAR9_G1	502D 1344h
348h	24	PWMXBAR_PWMXBAR9_G2	502D 1348h
34Ch	24	PWMXBAR_PWMXBAR9_G3	502D 134Ch
350h	32	PWMXBAR_PWMXBAR9_G4	502D 1350h
354h	32	PWMXBAR_PWMXBAR9_G5	502D 1354h
358h	32	PWMXBAR_PWMXBAR9_G6	502D 1358h
35Ch	32	PWMXBAR_PWMXBAR9_G7	502D 135Ch
360h	32	PWMXBAR_PWMXBAR9_G8	502D 1360h
380h	24	PWMXBAR_PWMXBAR10_G0	502D 1380h
384h	24	PWMXBAR_PWMXBAR10_G1	502D 1384h
388h	24	PWMXBAR_PWMXBAR10_G2	502D 1388h
38Ch	24	PWMXBAR_PWMXBAR10_G3	502D 138Ch
390h	32	PWMXBAR_PWMXBAR10_G4	502D 1390h
394h	32	PWMXBAR_PWMXBAR10_G5	502D 1394h
398h	32	PWMXBAR_PWMXBAR10_G6	502D 1398h
39Ch	32	PWMXBAR_PWMXBAR10_G7	502D 139Ch
3A0h	32	PWMXBAR_PWMXBAR10_G8	502D 13A0h
3C0h	24	PWMXBAR_PWMXBAR11_G0	502D 13C0h
3C4h	24	PWMXBAR_PWMXBAR11_G1	502D 13C4h
3C8h	24	PWMXBAR_PWMXBAR11_G2	502D 13C8h
3CCh	24	PWMXBAR_PWMXBAR11_G3	502D 13CCh
3D0h	32	PWMXBAR_PWMXBAR11_G4	502D 13D0h
3D4h	32	PWMXBAR_PWMXBAR11_G5	502D 13D4h
3D8h	32	PWMXBAR_PWMXBAR11_G6	502D 13D8h
3DCh	32	PWMXBAR_PWMXBAR11_G7	502D 13DCh

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Table 3-1435. CONTROLSS_PWMXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_PWMXBAR Physical Address
3E0h	32	PWMXBAR_PWMXBAR11_G8	502D 13E0h
400h	24	PWMXBAR_PWMXBAR12_G0	502D 1400h
404h	24	PWMXBAR_PWMXBAR12_G1	502D 1404h
408h	24	PWMXBAR_PWMXBAR12_G2	502D 1408h
40Ch	24	PWMXBAR_PWMXBAR12_G3	502D 140Ch
410h	32	PWMXBAR_PWMXBAR12_G4	502D 1410h
414h	32	PWMXBAR_PWMXBAR12_G5	502D 1414h
418h	32	PWMXBAR_PWMXBAR12_G6	502D 1418h
41Ch	32	PWMXBAR_PWMXBAR12_G7	502D 141Ch
420h	32	PWMXBAR_PWMXBAR12_G8	502D 1420h
440h	24	PWMXBAR_PWMXBAR13_G0	502D 1440h
444h	24	PWMXBAR_PWMXBAR13_G1	502D 1444h
448h	24	PWMXBAR_PWMXBAR13_G2	502D 1448h
44Ch	24	PWMXBAR_PWMXBAR13_G3	502D 144Ch
450h	32	PWMXBAR_PWMXBAR13_G4	502D 1450h
454h	32	PWMXBAR_PWMXBAR13_G5	502D 1454h
458h	32	PWMXBAR_PWMXBAR13_G6	502D 1458h
45Ch	32	PWMXBAR_PWMXBAR13_G7	502D 145Ch
460h	32	PWMXBAR_PWMXBAR13_G8	502D 1460h
480h	24	PWMXBAR_PWMXBAR14_G0	502D 1480h
484h	24	PWMXBAR_PWMXBAR14_G1	502D 1484h
488h	24	PWMXBAR_PWMXBAR14_G2	502D 1488h
48Ch	24	PWMXBAR_PWMXBAR14_G3	502D 148Ch
490h	32	PWMXBAR_PWMXBAR14_G4	502D 1490h
494h	32	PWMXBAR_PWMXBAR14_G5	502D 1494h
498h	32	PWMXBAR_PWMXBAR14_G6	502D 1498h
49Ch	32	PWMXBAR_PWMXBAR14_G7	502D 149Ch
4A0h	32	PWMXBAR_PWMXBAR14_G8	502D 14A0h
4C0h	24	PWMXBAR_PWMXBAR15_G0	502D 14C0h
4C4h	24	PWMXBAR_PWMXBAR15_G1	502D 14C4h
4C8h	24	PWMXBAR_PWMXBAR15_G2	502D 14C8h
4CCh	24	PWMXBAR_PWMXBAR15_G3	502D 14CCh
4D0h	32	PWMXBAR_PWMXBAR15_G4	502D 14D0h
4D4h	32	PWMXBAR_PWMXBAR15_G5	502D 14D4h
4D8h	32	PWMXBAR_PWMXBAR15_G6	502D 14D8h
4DCh	32	PWMXBAR_PWMXBAR15_G7	502D 14DCh
4E0h	32	PWMXBAR_PWMXBAR15_G8	502D 14E0h
500h	24	PWMXBAR_PWMXBAR16_G0	502D 1500h
504h	24	PWMXBAR_PWMXBAR16_G1	502D 1504h
508h	24	PWMXBAR_PWMXBAR16_G2	502D 1508h
50Ch	24	PWMXBAR_PWMXBAR16_G3	502D 150Ch
510h	32	PWMXBAR_PWMXBAR16_G4	502D 1510h
514h	32	PWMXBAR_PWMXBAR16_G5	502D 1514h
518h	32	PWMXBAR_PWMXBAR16_G6	502D 1518h
51Ch	32	PWMXBAR_PWMXBAR16_G7	502D 151Ch
520h	32	PWMXBAR_PWMXBAR16_G8	502D 1520h

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Table 3-1435. CONTROLSS_PWMXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_PWMXBAR Physical Address
540h	24	PWMXBAR_PWMXBAR17_G0	502D 1540h
544h	24	PWMXBAR_PWMXBAR17_G1	502D 1544h
548h	24	PWMXBAR_PWMXBAR17_G2	502D 1548h
54Ch	24	PWMXBAR_PWMXBAR17_G3	502D 154Ch
550h	32	PWMXBAR_PWMXBAR17_G4	502D 1550h
554h	32	PWMXBAR_PWMXBAR17_G5	502D 1554h
558h	32	PWMXBAR_PWMXBAR17_G6	502D 1558h
55Ch	32	PWMXBAR_PWMXBAR17_G7	502D 155Ch
560h	32	PWMXBAR_PWMXBAR17_G8	502D 1560h
580h	24	PWMXBAR_PWMXBAR18_G0	502D 1580h
584h	24	PWMXBAR_PWMXBAR18_G1	502D 1584h
588h	24	PWMXBAR_PWMXBAR18_G2	502D 1588h
58Ch	24	PWMXBAR_PWMXBAR18_G3	502D 158Ch
590h	32	PWMXBAR_PWMXBAR18_G4	502D 1590h
594h	32	PWMXBAR_PWMXBAR18_G5	502D 1594h
598h	32	PWMXBAR_PWMXBAR18_G6	502D 1598h
59Ch	32	PWMXBAR_PWMXBAR18_G7	502D 159Ch
5A0h	32	PWMXBAR_PWMXBAR18_G8	502D 15A0h
5C0h	24	PWMXBAR_PWMXBAR19_G0	502D 15C0h
5C4h	24	PWMXBAR_PWMXBAR19_G1	502D 15C4h
5C8h	24	PWMXBAR_PWMXBAR19_G2	502D 15C8h
5CCh	24	PWMXBAR_PWMXBAR19_G3	502D 15CCh
5D0h	32	PWMXBAR_PWMXBAR19_G4	502D 15D0h
5D4h	32	PWMXBAR_PWMXBAR19_G5	502D 15D4h
5D8h	32	PWMXBAR_PWMXBAR19_G6	502D 15D8h
5DCh	32	PWMXBAR_PWMXBAR19_G7	502D 15DCh
5E0h	32	PWMXBAR_PWMXBAR19_G8	502D 15E0h
600h	24	PWMXBAR_PWMXBAR20_G0	502D 1600h
604h	24	PWMXBAR_PWMXBAR20_G1	502D 1604h
608h	24	PWMXBAR_PWMXBAR20_G2	502D 1608h
60Ch	24	PWMXBAR_PWMXBAR20_G3	502D 160Ch
610h	32	PWMXBAR_PWMXBAR20_G4	502D 1610h
614h	32	PWMXBAR_PWMXBAR20_G5	502D 1614h
618h	32	PWMXBAR_PWMXBAR20_G6	502D 1618h
61Ch	32	PWMXBAR_PWMXBAR20_G7	502D 161Ch
620h	32	PWMXBAR_PWMXBAR20_G8	502D 1620h
640h	24	PWMXBAR_PWMXBAR21_G0	502D 1640h
644h	24	PWMXBAR_PWMXBAR21_G1	502D 1644h
648h	24	PWMXBAR_PWMXBAR21_G2	502D 1648h
64Ch	24	PWMXBAR_PWMXBAR21_G3	502D 164Ch
650h	32	PWMXBAR_PWMXBAR21_G4	502D 1650h
654h	32	PWMXBAR_PWMXBAR21_G5	502D 1654h
658h	32	PWMXBAR_PWMXBAR21_G6	502D 1658h
65Ch	32	PWMXBAR_PWMXBAR21_G7	502D 165Ch
660h	32	PWMXBAR_PWMXBAR21_G8	502D 1660h
680h	24	PWMXBAR_PWMXBAR22_G0	502D 1680h

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Table 3-1435. CONTROLSS_PWMXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_PWMXBAR Physical Address
684h	24	PWMXBAR_PWMXBAR22_G1	502D 1684h
688h	24	PWMXBAR_PWMXBAR22_G2	502D 1688h
68Ch	24	PWMXBAR_PWMXBAR22_G3	502D 168Ch
690h	32	PWMXBAR_PWMXBAR22_G4	502D 1690h
694h	32	PWMXBAR_PWMXBAR22_G5	502D 1694h
698h	32	PWMXBAR_PWMXBAR22_G6	502D 1698h
69Ch	32	PWMXBAR_PWMXBAR22_G7	502D 169Ch
6A0h	32	PWMXBAR_PWMXBAR22_G8	502D 16A0h
6C0h	24	PWMXBAR_PWMXBAR23_G0	502D 16C0h
6C4h	24	PWMXBAR_PWMXBAR23_G1	502D 16C4h
6C8h	24	PWMXBAR_PWMXBAR23_G2	502D 16C8h
6CCh	24	PWMXBAR_PWMXBAR23_G3	502D 16CCh
6D0h	32	PWMXBAR_PWMXBAR23_G4	502D 16D0h
6D4h	32	PWMXBAR_PWMXBAR23_G5	502D 16D4h
6D8h	32	PWMXBAR_PWMXBAR23_G6	502D 16D8h
6DCh	32	PWMXBAR_PWMXBAR23_G7	502D 16DCh
6E0h	32	PWMXBAR_PWMXBAR23_G8	502D 16E0h
700h	24	PWMXBAR_PWMXBAR24_G0	502D 1700h
704h	24	PWMXBAR_PWMXBAR24_G1	502D 1704h
708h	24	PWMXBAR_PWMXBAR24_G2	502D 1708h
70Ch	24	PWMXBAR_PWMXBAR24_G3	502D 170Ch
710h	32	PWMXBAR_PWMXBAR24_G4	502D 1710h
714h	32	PWMXBAR_PWMXBAR24_G5	502D 1714h
718h	32	PWMXBAR_PWMXBAR24_G6	502D 1718h
71Ch	32	PWMXBAR_PWMXBAR24_G7	502D 171Ch
720h	32	PWMXBAR_PWMXBAR24_G8	502D 1720h
740h	24	PWMXBAR_PWMXBAR25_G0	502D 1740h
744h	24	PWMXBAR_PWMXBAR25_G1	502D 1744h
748h	24	PWMXBAR_PWMXBAR25_G2	502D 1748h
74Ch	24	PWMXBAR_PWMXBAR25_G3	502D 174Ch
750h	32	PWMXBAR_PWMXBAR25_G4	502D 1750h
754h	32	PWMXBAR_PWMXBAR25_G5	502D 1754h
758h	32	PWMXBAR_PWMXBAR25_G6	502D 1758h
75Ch	32	PWMXBAR_PWMXBAR25_G7	502D 175Ch
760h	32	PWMXBAR_PWMXBAR25_G8	502D 1760h
780h	24	PWMXBAR_PWMXBAR26_G0	502D 1780h
784h	24	PWMXBAR_PWMXBAR26_G1	502D 1784h
788h	24	PWMXBAR_PWMXBAR26_G2	502D 1788h
78Ch	24	PWMXBAR_PWMXBAR26_G3	502D 178Ch
790h	32	PWMXBAR_PWMXBAR26_G4	502D 1790h
794h	32	PWMXBAR_PWMXBAR26_G5	502D 1794h
798h	32	PWMXBAR_PWMXBAR26_G6	502D 1798h
79Ch	32	PWMXBAR_PWMXBAR26_G7	502D 179Ch
7A0h	32	PWMXBAR_PWMXBAR26_G8	502D 17A0h
7C0h	24	PWMXBAR_PWMXBAR27_G0	502D 17C0h
7C4h	24	PWMXBAR_PWMXBAR27_G1	502D 17C4h

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Table 3-1435. CONTROLSS_PWMXBAR Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_PWMXBAR Physical Address
7C8h	24	PWMXBAR_PWMXBAR27_G2	502D 17C8h
7CCh	24	PWMXBAR_PWMXBAR27_G3	502D 17CCh
7D0h	32	PWMXBAR_PWMXBAR27_G4	502D 17D0h
7D4h	32	PWMXBAR_PWMXBAR27_G5	502D 17D4h
7D8h	32	PWMXBAR_PWMXBAR27_G6	502D 17D8h
7DCh	32	PWMXBAR_PWMXBAR27_G7	502D 17DCh
7E0h	32	PWMXBAR_PWMXBAR27_G8	502D 17E0h
800h	24	PWMXBAR_PWMXBAR28_G0	502D 1800h
804h	24	PWMXBAR_PWMXBAR28_G1	502D 1804h
808h	24	PWMXBAR_PWMXBAR28_G2	502D 1808h
80Ch	24	PWMXBAR_PWMXBAR28_G3	502D 180Ch
810h	32	PWMXBAR_PWMXBAR28_G4	502D 1810h
814h	32	PWMXBAR_PWMXBAR28_G5	502D 1814h
818h	32	PWMXBAR_PWMXBAR28_G6	502D 1818h
81Ch	32	PWMXBAR_PWMXBAR28_G7	502D 181Ch
820h	32	PWMXBAR_PWMXBAR28_G8	502D 1820h
840h	24	PWMXBAR_PWMXBAR29_G0	502D 1840h
844h	24	PWMXBAR_PWMXBAR29_G1	502D 1844h
848h	24	PWMXBAR_PWMXBAR29_G2	502D 1848h
84Ch	24	PWMXBAR_PWMXBAR29_G3	502D 184Ch
850h	32	PWMXBAR_PWMXBAR29_G4	502D 1850h
854h	32	PWMXBAR_PWMXBAR29_G5	502D 1854h
858h	32	PWMXBAR_PWMXBAR29_G6	502D 1858h
85Ch	32	PWMXBAR_PWMXBAR29_G7	502D 185Ch
860h	32	PWMXBAR_PWMXBAR29_G8	502D 1860h

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3.21.1 CONTROLSS_PWMXBAR_PID Registers

3.21.1.1 PWMXBAR_PID Register (Offset = 0h) [reset = h]

Short Description: PID register

Long Description:

Return to Summary Table

Table 3-1436. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1000h

Access Types Legend

Table 3-1437. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PID_MSB16	RO	6180h	Not Defined
15 - 11	PID_MISC	RO	0h	Not Defined
10 - 8	PID_MAJOR	RO	2h	Not Defined
7 - 6	PID_CUSTOM	RO	0h	Not Defined
5 - 0	PID_MINOR	RO	14h	Not Defined

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3.21.2 CONTROLSS_PWMXBAR_STATUS Registers

3.21.2.1 PWMXBAR_STATUS Register (Offset = 10h) [reset = h]

Short Description: RO

Long Description:

Return to Summary Table

Table 3-1438. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1010h

Access Types Legend

Table 3-1439. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 0	STS	RO	0h	Output Signal Status

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3.21.3 CONTROLSS_PWMXBAR_FLAGINVERT Registers

3.21.3.1 PWMXBAR_FLAGINVERT Register (Offset = 14h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1440. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1014h

Access Types Legend

Table 3-1441. FLAGINVERT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 0	INVERT	RW	0h	Output Signal Invert Before Latch

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3.21.4 CONTROLSS_PWMXBAR_FLAG Registers

3.21.4.1 PWMXBAR_FLAG Register (Offset = 18h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1442. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1018h

Access Types Legend

Table 3-1443. FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29	BIT29	RW	0h	Output Signal Latched Flag
28	BIT28	RW	0h	Output Signal Latched Flag
27	BIT27	RW	0h	Output Signal Latched Flag
26	BIT26	RW	0h	Output Signal Latched Flag
25	BIT25	RW	0h	Output Signal Latched Flag
24	BIT24	RW	0h	Output Signal Latched Flag
23	BIT23	RW	0h	Output Signal Latched Flag
22	BIT22	RW	0h	Output Signal Latched Flag
21	BIT21	RW	0h	Output Signal Latched Flag
20	BIT20	RW	0h	Output Signal Latched Flag
19	BIT19	RW	0h	Output Signal Latched Flag
18	BIT18	RW	0h	Output Signal Latched Flag
17	BIT17	RW	0h	Output Signal Latched Flag
16	BIT16	RW	0h	Output Signal Latched Flag
15	BIT15	RW	0h	Output Signal Latched Flag
14	BIT14	RW	0h	Output Signal Latched Flag
13	BIT13	RW	0h	Output Signal Latched Flag
12	BIT12	RW	0h	Output Signal Latched Flag
11	BIT11	RW	0h	Output Signal Latched Flag
10	BIT10	RW	0h	Output Signal Latched Flag
9	BIT9	RW	0h	Output Signal Latched Flag
8	BIT8	RW	0h	Output Signal Latched Flag
7	BIT7	RW	0h	Output Signal Latched Flag
6	BIT6	RW	0h	Output Signal Latched Flag
5	BIT5	RW	0h	Output Signal Latched Flag
4	BIT4	RW	0h	Output Signal Latched Flag
3	BIT3	RW	0h	Output Signal Latched Flag
2	BIT2	RW	0h	Output Signal Latched Flag
1	BIT1	RW	0h	Output Signal Latched Flag
0	BIT0	RW	0h	Output Signal Latched Flag

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3.21.5 CONTROLSS_PWMXBAR_FLAG_CLR Registers

3.21.5.1 PWMXBAR_FLAG_CLR Register (Offset = 1Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 3-1444. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 101Ch

Access Types Legend

Table 3-1445. FLAG_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29	BIT29	RW	0h	Output Signal Latched Flag Clear
28	BIT28	RW	0h	Output Signal Latched Flag Clear
27	BIT27	RW	0h	Output Signal Latched Flag Clear
26	BIT26	RW	0h	Output Signal Latched Flag Clear
25	BIT25	RW	0h	Output Signal Latched Flag Clear
24	BIT24	RW	0h	Output Signal Latched Flag Clear
23	BIT23	RW	0h	Output Signal Latched Flag Clear
22	BIT22	RW	0h	Output Signal Latched Flag Clear
21	BIT21	RW	0h	Output Signal Latched Flag Clear
20	BIT20	RW	0h	Output Signal Latched Flag Clear
19	BIT19	RW	0h	Output Signal Latched Flag Clear
18	BIT18	RW	0h	Output Signal Latched Flag Clear
17	BIT17	RW	0h	Output Signal Latched Flag Clear
16	BIT16	RW	0h	Output Signal Latched Flag Clear
15	BIT15	RW	0h	Output Signal Latched Flag Clear
14	BIT14	RW	0h	Output Signal Latched Flag Clear
13	BIT13	RW	0h	Output Signal Latched Flag Clear
12	BIT12	RW	0h	Output Signal Latched Flag Clear
11	BIT11	RW	0h	Output Signal Latched Flag Clear
10	BIT10	RW	0h	Output Signal Latched Flag Clear
9	BIT9	RW	0h	Output Signal Latched Flag Clear
8	BIT8	RW	0h	Output Signal Latched Flag Clear
7	BIT7	RW	0h	Output Signal Latched Flag Clear
6	BIT6	RW	0h	Output Signal Latched Flag Clear
5	BIT5	RW	0h	Output Signal Latched Flag Clear
4	BIT4	RW	0h	Output Signal Latched Flag Clear
3	BIT3	RW	0h	Output Signal Latched Flag Clear
2	BIT2	RW	0h	Output Signal Latched Flag Clear
1	BIT1	RW	0h	Output Signal Latched Flag Clear
0	BIT0	RW	0h	Output Signal Latched Flag Clear

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3.21.6 CONTROLSS_PWMXBARn_G0 Registers

3.21.6.1 PWMXBARn_G0 Register (Offset = 100h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x100+0x40*n* where *n* goes from 0-29 (35)

Table 3-1446. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1**N**h

Access Types Legend

Table 3-1447. G0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar0 G0 Input Select0: CMP12SS0.CTRIPL1: CMP12SS0.CTRIPH2: CMP12SS1.CTRIPL3: CMP12SS1.CTRIPH4: CMP12SS2.CTRIPL5: CMP12SS2.CTRIPH6: CMP12SS3.CTRIPL7: CMP12SS3.CTRIPH8: CMP12SS4.CTRIPL9: CMP12SS4.CTRIPH10: CMP12SS5.CTRIPL11: CMP12SS5.CTRIPH12: CMP12SS6.CTRIPL13: CMP12SS6.CTRIPH14: CMP12SS7.CTRIPL15: CMP12SS7.CTRIPH16: CMP12SS8.CTRIPL17: CMP12SS8.CTRIPH18: CMP12SS9.CTRIPL19: CMP12SS9.CTRIPH

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3.21.7 CONTROLSS_PWMXBARn_G1 Registers

3.21.7.1 PWMXBARn_G1 Register (Offset = 104h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x104+0x40*n* where *n* goes from 0-29 (36)

Table 3-1448. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1**N**h

Access Types Legend

Table 3-1449. G1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar0 G1 Input Select0: CMP8SS0.CTRIPL1: CMP8SS0.CTRIPH2: CMP8SS1.CTRIPL3: CMP8SS1.CTRIPH4: CMP8SS2.CTRIPL5: CMP8SS2.CTRIPH6: CMP8SS3.CTRIPL7: CMP8SS3.CTRIPH8: CMP8SS4.CTRIPL9: CMP8SS4.CTRIPH10: CMP8SS5.CTRIPL11: CMP8SS5.CTRIPH12: CMP8SS6.CTRIPL13: CMP8SS6.CTRIPH14: CMP8SS7.CTRIPL15: CMP8SS7.CTRIPH16: CMP8SS8.CTRIPL17: CMP8SS8.CTRIPH18: CMP8SS9.CTRIPL19: CMP8SS9.CTRIPH

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3.21.8 CONTROLSS_PWMXBARn_G2 Registers

3.21.8.1 PWMXBARn_G2 Register (Offset = 108h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x108+0x40*n* where *n* goes from 0-29 (37)

Table 3-1450. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1**N**h

Access Types Legend

Table 3-1451. G2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	SEL	RW	0h	PWM XBar0 G2 Input Select0: SDFM0.FILT1CEVT11: SDFM0.FILT1CEVT22: SDFM0.FILT1COMPHZ3: SDFM0.FILT2CEVT14: SDFM0.FILT2CEVT25: SDFM0.FILT2COMPHZ6: SDFM0.FILT3CEVT17: SDFM0.FILT3CEVT28: SDFM0.FILT3COMPHZ9: SDFM0.FILT4CEVT110: SDFM0.FILT4CEVT211: SDFM0.FILT4COMPHZ12: SDFM1.FILT1CEVT113: SDFM1.FILT1CEVT214: SDFM1.FILT1COMPHZ15: SDFM1.FILT2CEVT116: SDFM1.FILT2CEVT217: SDFM1.FILT2COMPHZ18: SDFM1.FILT3CEVT119: SDFM1.FILT3CEVT220: SDFM1.FILT3COMPHZ21: SDFM1.FILT4CEVT122: SDFM1.FILT4CEVT223: SDFM1.FILT4COMPHZ

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3.21.9 CONTROLSS_PWMXBARn_G3 Registers

3.21.9.1 PWMXBARn_G3 Register (Offset = 10Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x108+0x40*n* where *n* goes from 0-29 (38)

Table 3-1452. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1**N**h

Access Types Legend

Table 3-1453. G3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	SEL	RW	0h	PWM XBar0 G3 Input Select1: ADC0.EVT22: ADC0.EVT33: ADC0.EVT44: ADC1.EVT15: ADC1.EVT26: ADC1.EVT37: ADC1.EVT48: ADC2.EVT19: ADC2.EVT210: ADC2.EVT311: ADC2.EVT412: ADC3.EVT113: ADC3.EVT214: ADC3.EVT315: ADC3.EVT416: ADC4.EVT117: ADC4.EVT218: ADC4.EVT319: ADC4.EVT4

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3.21.10 CONTROLSS_PWMXBARn_G4 Registers

3.21.10.1 PWMXBARn_G4 Register (Offset = 110h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x110+0x40*n* where *n* goes from 0-29 (39)

Table 3-1454. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1**N**h

Access Types Legend

Table 3-1455. G4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar0 G4 input bit select. Input source is INPUT XBAR.1: INPUT XBAR output bit[x] selected0: INPUT XBAR output bit[x] is de-selected

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3.21.11 CONTROLSS_PWMXBARn_G5 Registers

3.21.11.1 PWMXBARn_G5 Register (Offset = 114h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x114+0x40*n* where *n* goes from 0-29 (40)

Table 3-1456. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1**N**h

Access Types Legend

Table 3-1457. G5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar0 G5 input bit select. Input source is PWM TRIPOUT.1: PWM TRIPOUT bit[x] selected0: PWM TRIPOUT bit[x] is de-selected

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3.21.12 CONTROLSS_PWMXBARn_G6 Registers

3.21.12.1 PWMXBARn_G6 Register (Offset = 118h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x118+0x40*n* where *n* goes from 0-29 (41)

Table 3-1458. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1**N**h

Access Types Legend

Table 3-1459. G6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar0 G6 input bit select. Input source is PWM DEL TRIP1: PWM DEL TRIP bit[x] selected0: PWM DEL TRIP bit[x] is de-selected

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3.21.13 CONTROLSS_PWMXBARn_G7 Registers

3.21.13.1 PWMXBARn_G7 Register (Offset = 11Ch) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x11C+0x40**n* where *n* goes from 0-29 (42)

Table 3-1460. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1**N**h

Access Types Legend

Table 3-1461. G7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SEL	RW	0h	PWM XBar0 G7 input bit select. Input source is PWM DEL ACTIVE1: PWM DEL ACTIVE bit[x] selected0: PWM DEL ACTIVE bit[x] is de-selected

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3.21.14 CONTROLSS_PWMXBARn_G8 Registers

3.21.14.1 PWMXBARn_G8 Register (Offset = 120h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Equation Description:

N=0x120+0x40*n* where *n* goes from 0-29 (43)

Table 3-1462. Instance Table

Instance Name	Physical Address
CONTROLSS_PWMXBAR	502D 1**N**h

Access Types Legend

Table 3-1463. G8 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 0	SEL	RW	0h	PWM XBar0 G8 Input Select0: EQEP0.ERR1: EQEP1.ERR2: EQEP2.ERR6:3: FSIRX0.RX_TRIG410:7: FSIRX1.RX_TRIG414:11: FSIRX2.RX_TRIG418:15: FSIRX3.RX_TRIG428:19: ECAP[9:0].TRIPOUT

3.21.15 Access Table

Table 3-1464. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

3.22 SDFM Registers

Table 3-1465. CONTROLSS_SDFM[0:1] Registers Base Address Table

Offset	Length	Acronym	CONTROLSS_SDFM0 Physical Address	CONTROLSS_SDFM1 Physical Address
0h	32	SDFM_SDIFLG	5026 8000h	5026 9000h
4h	32	SDFM_SDIFLGCLR	5026 8004h	5026 9004h
8h	16	SDFM_SDCTL	5026 8008h	5026 9008h
Ch	16	SDFM_SDMFILEN	5026 800Ch	5026 900Ch
Eh	16	SDFM_SDSTATUS	5026 800Eh	5026 900Eh
20h	16	SDFM_SDCTLPARM1	5026 8020h	5026 9020h
22h	16	SDFM_SDDFPARM1	5026 8022h	5026 9022h
24h	16	SDFM_SDDPARM1	5026 8024h	5026 9024h
26h	16	SDFM_SDFLT1CMPH1	5026 8026h	5026 9026h
28h	16	SDFM_SDFLT1CMPL1	5026 8028h	5026 9028h
2Ah	16	SDFM_SDCPARM1	5026 802Ah	5026 902Ah
2Ch	32	SDFM_SDDATA1	5026 802Ch	5026 902Ch
30h	32	SDFM_SDDATFIFO1	5026 8030h	5026 9030h
34h	16	SDFM_SDCDATA1	5026 8034h	5026 9034h
36h	16	SDFM_SDFLT1CMPH2	5026 8036h	5026 9036h
38h	16	SDFM_SDFLT1CMPHZ	5026 8038h	5026 9038h

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Table 3-1465. CONTROLSS_SDFM[0:1] Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_SDFM0 Physical Address	CONTROLSS_SDFM1 Physical Address
3Ah	16	SDFM_SDFIFOCTL1	5026 803Ah	5026 903Ah
3Ch	16	SDFM_SDSYNC1	5026 803Ch	5026 903Ch
3Eh	16	SDFM_SDFLT1CMPL2	5026 803Eh	5026 903Eh
40h	16	SDFM_SDCTLPARM2	5026 8040h	5026 9040h
42h	16	SDFM_SDDFPARM2	5026 8042h	5026 9042h
44h	16	SDFM_SDDPARM2	5026 8044h	5026 9044h
46h	16	SDFM_SDFLT2CMPH1	5026 8046h	5026 9046h
48h	16	SDFM_SDFLT2CMPL1	5026 8048h	5026 9048h
4Ah	16	SDFM_SDCPARM2	5026 804Ah	5026 904Ah
4Ch	32	SDFM_SDDATA2	5026 804Ch	5026 904Ch
50h	32	SDFM_SDDATFIFO2	5026 8050h	5026 9050h
54h	16	SDFM_SDCDATA2	5026 8054h	5026 9054h
56h	16	SDFM_SDFLT2CMPH2	5026 8056h	5026 9056h
58h	16	SDFM_SDFLT2CMPHZ	5026 8058h	5026 9058h
5Ah	16	SDFM_SDFIFOCTL2	5026 805Ah	5026 905Ah
5Ch	16	SDFM_SDSYNC2	5026 805Ch	5026 905Ch
5Eh	16	SDFM_SDFLT2CMPL2	5026 805Eh	5026 905Eh
60h	16	SDFM_SDCTLPARM3	5026 8060h	5026 9060h
62h	16	SDFM_SDDFPARM3	5026 8062h	5026 9062h
64h	16	SDFM_SDDPARM3	5026 8064h	5026 9064h
66h	16	SDFM_SDFLT3CMPH1	5026 8066h	5026 9066h
68h	16	SDFM_SDFLT3CMPL1	5026 8068h	5026 9068h
6Ah	16	SDFM_SDCPARM3	5026 806Ah	5026 906Ah
6Ch	32	SDFM_SDDATA3	5026 806Ch	5026 906Ch
70h	32	SDFM_SDDATFIFO3	5026 8070h	5026 9070h
74h	16	SDFM_SDCDATA3	5026 8074h	5026 9074h
76h	16	SDFM_SDFLT3CMPH2	5026 8076h	5026 9076h
78h	16	SDFM_SDFLT3CMPHZ	5026 8078h	5026 9078h
7Ah	16	SDFM_SDFIFOCTL3	5026 807Ah	5026 907Ah
7Ch	16	SDFM_SDSYNC3	5026 807Ch	5026 907Ch
7Eh	16	SDFM_SDFLT3CMPL2	5026 807Eh	5026 907Eh
80h	16	SDFM_SDCTLPARM4	5026 8080h	5026 9080h
82h	16	SDFM_SDDFPARM4	5026 8082h	5026 9082h
84h	16	SDFM_SDDPARM4	5026 8084h	5026 9084h
86h	16	SDFM_SDFLT4CMPH1	5026 8086h	5026 9086h
88h	16	SDFM_SDFLT4CMPL1	5026 8088h	5026 9088h
8Ah	16	SDFM_SDCPARM4	5026 808Ah	5026 908Ah
8Ch	32	SDFM_SDDATA4	5026 808Ch	5026 908Ch
90h	32	SDFM_SDDATFIFO4	5026 8090h	5026 9090h
94h	16	SDFM_SDCDATA4	5026 8094h	5026 9094h
96h	16	SDFM_SDFLT4CMPH2	5026 8096h	5026 9096h
98h	16	SDFM_SDFLT4CMPHZ	5026 8098h	5026 9098h
9Ah	16	SDFM_SDFIFOCTL4	5026 809Ah	5026 909Ah
9Ch	16	SDFM_SDSYNC4	5026 809Ch	5026 909Ch
9Eh	16	SDFM_SDFLT4CMPL2	5026 809Eh	5026 909Eh
C0h	16	SDFM_SDCOMP1CTL	5026 80C0h	5026 90C0h

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Table 3-1465. CONTROLSS_SDFM[0:1] Registers Base Address Table (continued)

Offset	Length	Acronym	CONTROLSS_SDFM0 Physical Address	CONTROLSS_SDFM1 Physical Address
C2h	16	SDFM_SDCOMP1EVT2FLTCTL	5026 80C2h	5026 90C2h
C4h	16	SDFM_SDCOMP1EVT2FLTCLKCTL	5026 80C4h	5026 90C4h
C6h	16	SDFM_SDCOMP1EVT1FLTCTL	5026 80C6h	5026 90C6h
C8h	16	SDFM_SDCOMP1EVT1FLTCLKCTL	5026 80C8h	5026 90C8h
CEh	16	SDFM_SDCOMP1LOCK	5026 80CEh	5026 90CEh
D0h	16	SDFM_SDCOMP2CTL	5026 80D0h	5026 90D0h
D2h	16	SDFM_SDCOMP2EVT2FLTCTL	5026 80D2h	5026 90D2h
D4h	16	SDFM_SDCOMP2EVT2FLTCLKCTL	5026 80D4h	5026 90D4h
D6h	16	SDFM_SDCOMP2EVT1FLTCTL	5026 80D6h	5026 90D6h
D8h	16	SDFM_SDCOMP2EVT1FLTCLKCTL	5026 80D8h	5026 90D8h
DEh	16	SDFM_SDCOMP2LOCK	5026 80DEh	5026 90DEh
E0h	16	SDFM_SDCOMP3CTL	5026 80E0h	5026 90E0h
E2h	16	SDFM_SDCOMP3EVT2FLTCTL	5026 80E2h	5026 90E2h
E4h	16	SDFM_SDCOMP3EVT2FLTCLKCTL	5026 80E4h	5026 90E4h
E6h	16	SDFM_SDCOMP3EVT1FLTCTL	5026 80E6h	5026 90E6h
E8h	16	SDFM_SDCOMP3EVT1FLTCLKCTL	5026 80E8h	5026 90E8h
EEh	16	SDFM_SDCOMP3LOCK	5026 80EEh	5026 90EEh
F0h	16	SDFM_SDCOMP4CTL	5026 80F0h	5026 90F0h
F2h	16	SDFM_SDCOMP4EVT2FLTCTL	5026 80F2h	5026 90F2h
F4h	16	SDFM_SDCOMP4EVT2FLTCLKCTL	5026 80F4h	5026 90F4h
F6h	16	SDFM_SDCOMP4EVT1FLTCTL	5026 80F6h	5026 90F6h
F8h	16	SDFM_SDCOMP4EVT1FLTCLKCTL	5026 80F8h	5026 90F8h
FEh	16	SDFM_SDCOMP4LOCK	5026 80FEh	5026 90FEh

3.22.1 SDFM Instance Count Note

Note

n = 0 to 1 for the SDFM registers defined below.

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3.22.2 CONTROLSS_SDFMn_SDIFLG Registers

3.22.2.1 SDFMn_SDIFLG Register (Offset = 0h) [reset = h]

Short Description: SD Interrupt Flag Register

Long Description:

Return to Summary Table

Table 3-1466. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8000h
CONTROLSS_SDFM1	5026 9000h

Access Types Legend

Table 3-1467. SDIFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MIF	RO	0h	Set whenever any "error" interrupt (MF1-4,IFL1-4,IFH1-4,SDFFOVF1-4) is active
30 - 24	RESERVED	RO RRETURNS 0S		Reserved
23	SDFFINT4	RO	0h	SDFIFO data ready interrupt for Ch4
22	SDFFINT3	RO	0h	SDFIFO data ready interrupt for Ch3
21	SDFFINT2	RO	0h	SDFIFO data ready interrupt for Ch2
20	SDFFINT1	RO	0h	SDFIFO data ready interrupt for Ch1 0: SDFIFO data ready interrupt has NOT occurred 1: SDFIFO data ready interrupt has occurred
19	SDFFOVF4	RO	0h	FIFO Overflow Flag for Ch4
18	SDFFOVF3	RO	0h	FIFO Overflow Flag for Ch3
17	SDFFOVF2	RO	0h	FIFO Overflow Flag for Ch2
16	SDFFOVF1	RO	0h	FIFO Overflow Flag for Ch1 0 - FIFO has not overflowed 1 - FIFO overflowed. # words received in FIFO ' FIFO depth (16), NEW word is lost
15	AF4	RO	0h	Acknowledge flag for Filter 4 0: No new data available for Filter (in non-FIFO mode) 1: New data available for Filter (in non-FIFO mode)
14	AF3	RO	0h	Acknowledge flag for Filter 3 0: No new data available for Filter (in non-FIFO mode) 1: New data available for Filter (in non-FIFO mode)
13	AF2	RO	0h	Acknowledge flag for Filter 2 0: No new data available for Filter (in non-FIFO mode) 1: New data available for Filter (in non-FIFO mode)
12	AF1	RO	0h	Acknowledge flag for Filter 1 0: No new data available for Filter (in non-FIFO mode) 1: New data available for Filter (in non-FIFO mode)
11	MF4	RO	0h	Modulator Failure for Filter 4 0: Modulator is operating normally for Filter 1: Modulator failure for Filter
10	MF3	RO	0h	Modulator Failure for Filter 3 0: Modulator is operating normally for Filter 1: Modulator failure for Filter
9	MF2	RO	0h	Modulator Failure for Filter 2 0: Modulator is operating normally for Filter 1: Modulator failure for Filter
8	MF1	RO	0h	Modulator Failure for Filter 1 0: Modulator is operating normally for Filter 1: Modulator failure for Filter
7	FLT4_FLG_CEVT2	RO	0h	CEVT2 Interrupt flag for filter4 0: CEVT2 event has not occured 1: CEVT2 event has occurred
6	FLT4_FLG_CEVT1	RO	0h	CEVT1 Interrupt flag for filter4 0: CEVT1 event has not occured 1: CEVT1 event has occurred
5	FLT3_FLG_CEVT2	RO	0h	CEVT2 Interrupt flag for filter3 0: CEVT2 event has not occured 1: CEVT2 event has occurred

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Table 3-1467. SDIFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	FLT3_FLG_CEVT1	RO	0h	CEVT1 Interrupt flag for filter3 0: CEVT1 event has not occured 1: CEVT1 event has occurred
3	FLT2_FLG_CEVT2	RO	0h	CEVT2 Interrupt flag for filter2 0: CEVT2 event has not occured 1: CEVT2 event has occurred
2	FLT2_FLG_CEVT1	RO	0h	CEVT1 Interrupt flag for filter2 0: CEVT1 event has not occured 1: CEVT1 event has occurred
1	FLT1_FLG_CEVT2	RO	0h	CEVT2 Interrupt flag for filter1 0: CEVT2 event has not occured 1: CEVT2 event has occurred
0	FLT1_FLG_CEVT1	RO	0h	CEVT1 Interrupt flag for filter1 0: CEVT1 event has not occured 1: CEVT1 event has occurred

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3.22.3 CONTROLSS_SDFMn_SDIFLGCLR Registers

3.22.3.1 SDFMn_SDIFLGCLR Register (Offset = 4h) [reset = h]

Short Description: SD Module Interrupt Flag Clear Bits: Writing a "1" will clear the respective flag bit in the SDIFLG register. Writes of "0" are ignored. Note: If user writes a "1" to clear a bit on the same cycle that the hardware is trying to set the bit to "1", then hardware has priority and the bit will not be cleared.

Long Description:

Return to Summary Table

Table 3-1468. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8004h
CONTROLSS_SDFM1	5026 9004h

Access Types Legend

Table 3-1469. SDIFLGCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MIF	RW RRETURNS 0S	0h	Flag-clear bit for SDFM Master Interrupt flag. Writing a 1 to clear MIF flag in SDIFLG register Writes of "0" are ignored. Note: If the MIF flag is cleared and other Interrupts are still pending, MIF will again be set to 1 on the following SysClk cycle, and the INT output will be reasserted (pulsed low)
30 - 24	RESERVED	RO RRETURNS 0S		Reserved
23	SDFFINT4	RW RRETURNS 0S	0h	SDFIFO data ready Interrupt flag-clear bit for Ch4
22	SDFFINT3	RW RRETURNS 0S	0h	SDFIFO data ready Interrupt flag-clear bit for Ch3
21	SDFFINT2	RW RRETURNS 0S	0h	SDFIFO data ready Interrupt flag-clear bit for Ch2
20	SDFFINT1	RW RRETURNS 0S	0h	SDFIFO data ready Interrupt flag-clear bit for Ch1
19	SDFFOVF4	RW RRETURNS 0S	0h	SDFIFO overflow clear Ch4
18	SDFFOVF3	RW RRETURNS 0S	0h	SDFIFO overflow clear Ch3
17	SDFFOVF2	RW RRETURNS 0S	0h	SDFIFO overflow clear Ch2
16	SDFFOVF1	RW RRETURNS 0S	0h	SDFIFO overflow clear Ch1
15	AF4	RW RRETURNS 0S	0h	Flag-clear bit for Acknowledge flag for Filter 4
14	AF3	RW RRETURNS 0S	0h	Flag Clear bit for AF3

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Table 3-1469. SDIFLGCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	AF2	RW RRETURNS 0S	0h	Flag Clear bit for AF2
12	AF1	RW RRETURNS 0S	0h	Flag Clear bit for AF1
11	MF4	RW RRETURNS 0S	0h	Flag Clear bit for MF4
10	MF3	RW RRETURNS 0S	0h	Flag Clear bit for MF3
9	MF2	RW RRETURNS 0S	0h	Flag Clear bit for MF2
8	MF1	RW RRETURNS 0S	0h	Flag Clear bit for MF1
7	FLT4_FLG_CEVT2	RW RRETURNS 0S	0h	Flag Clear bit for FLT4_FLG_CEVT2
6	FLT4_FLG_CEVT1	RW RRETURNS 0S	0h	Flag Clear bit for FLT4_FLG_CEVT1
5	FLT3_FLG_CEVT2	RW RRETURNS 0S	0h	Flag Clear bit for FLT3_FLG_CEVT2
4	FLT3_FLG_CEVT1	RW RRETURNS 0S	0h	Flag Clear bit for FLT3_FLG_CEVT1
3	FLT2_FLG_CEVT2	RW RRETURNS 0S	0h	Flag Clear bit for FLT2_FLG_CEVT2
2	FLT2_FLG_CEVT1	RW RRETURNS 0S	0h	Flag Clear bit for FLT2_FLG_CEVT1
1	FLT1_FLG_CEVT2	RW RRETURNS 0S	0h	Flag Clear bit for FLT1_FLG_CEVT2
0	FLT1_FLG_CEVT1	RW RRETURNS 0S	0h	Flag Clear bit for FLT1_FLG_CEVT1

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3.22.4 CONTROLSS_SDFMn_SDCTL Registers

3.22.4.1 SDFMn_SDCTL Register (Offset = 8h) [reset = h]

Short Description: SD Control Register

Long Description:

Return to Summary Table

Table 3-1470. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8008h
CONTROLSS_SDFM1	5026 9008h

Access Types Legend

Table 3-1471. SDCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14	RESERVED	RO RRETURNS 0S		Reserved
13	MIE	RW	0h	Master SDy_ERR interrupt enable 0: SDy_ERR Interrupt and interrupt flags are disabled 1: SDy_ERR Interrupt and interrupt flags are enabled
12 - 4	RESERVED	RO RRETURNS 0S		Reserved
3	HZ4	RW RRETURNS 0S	0h	Flag Clear bit for HZ4
2	HZ3	RW RRETURNS 0S	0h	Flag Clear bit for HZ3
1	HZ2	RW RRETURNS 0S	0h	Flag Clear bit for HZ2
0	HZ1	RW RRETURNS 0S	0h	Flag Clear bit for HZ1

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3.22.5 CONTROLSS_SDFMn_SDMFILEN Registers

3.22.5.1 SDFMn_SDMFILEN Register (Offset = Ch) [reset = h]

Short Description: SD Master Filter Enable

Long Description:

Return to Summary Table

Table 3-1472. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 800Ch
CONTROLSS_SDFM1	5026 900Ch

Access Types Legend

Table 3-1473. SDMFILEN Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO RRETURNS 0S		Reserved
12	RESERVED	RO RRETURNS 0S		Reserved
11	MFE	RW	0h	Master Filter Enable 0: All the four data filter units of SDFM module are disabled. All FIFOs are cleared 1: Data filter units can be enabled if bit FEN is '1'.
10	RESERVED	RO RRETURNS 0S		Reserved
9	RESERVED	RO RRETURNS 0S		Reserved
8 - 7	RESERVED	RO RRETURNS 0S		Reserved
6 - 4	RESERVED	RO RRETURNS 0S		Reserved
3 - 0	RESERVED	RO RRETURNS 0S		Reserved

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3.22.6 CONTROLSS_SDFMn_SDSTATUS Registers

3.22.6.1 SDFMn_SDSTATUS Register (Offset = Eh) [reset = h]

Short Description: SD Status Register

Long Description:

Return to Summary Table

Table 3-1474. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 800Eh
CONTROLSS_SDFM1	5026 900Eh

Access Types Legend

Table 3-1475. SDSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	RESERVED	RO		Reserved
13	RESERVED	RO		Reserved
12	RESERVED	RO		Reserved
11	RESERVED	RO		Reserved
10	RESERVED	RO		Reserved
9	RESERVED	RO		Reserved
8	RESERVED	RO		Reserved
7 - 4	RESERVED	RO RRETURNS 0S		Reserved
3	HZ4	RO	0h	High-level Threshold crossing (Z) flag Ch4 Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0: Comparator filter output ' SDCMPHZ4.HLTZ 1: Comparator filter output '= SDCMPHZ4.HLTZ
2	HZ3	RO	0h	High-level Threshold crossing (Z) flag Ch3 Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0: Comparator filter output ' SDCMPHZ3.HLTZ 1: Comparator filter output '= SDCMPHZ3.HLTZ
1	HZ2	RO	0h	High-level Threshold crossing (Z) flag Ch2 Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0: Comparator filter output ' SDCMPHZ2.HLTZ 1: Comparator filter output '= SDCMPHZ2.HLTZ
0	HZ1	RO	0h	High-level Threshold crossing (Z) flag Ch1 Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt. 0: Comparator filter output ' SDCMPHZ1.HLTZ 1: Comparator filter output '= SDCMPHZ1.HLTZ

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3.22.7 CONTROLSS_SDFMn_SDCTLPARM1 Registers

3.22.7.1 SDFMn_SDCTLPARM1 Register (Offset = 20h) [reset = h]

Short Description: Control Parameter Register for Ch1

Long Description:

Return to Summary Table

Table 3-1476. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8020h
CONTROLSS_SDFM1	5026 9020h

Access Types Legend

Table 3-1477. SDCTLPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO		Reserved
7	RESERVED	RO RRETURNS 0S		Reserved
6	SDDATASYNC	RW	0h	0: SD Data is not passed through a synchronizer. 1: SD Data is passed through a synchronizer.
5	RESERVED	RO RRETURNS 0S		Reserved
4	SDCLKSYNC	RW	0h	0: SD Clock is not passed through a synchronizer. 1: SD Clock is passed through a synchronizer.
3	SDCLKSEL	RW	0h	SD1 Clock source select. 0: Clock source to SDFM filter is its channel clock. 1: Clock source to SDFM filter is SD1 filter clock.
2	RESERVED	RW		Reserved
1 - 0	MOD	RW	0h	Modulator clock modes 0: Mode 0: Modulator clock running at 1x data rate 1: Reserved 2: Reserved 3: Reserved

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3.22.8 CONTROLSS_SDFMn_SDDFPARM1 Registers

3.22.8.1 SDFMn_SDDFPARM1 Register (Offset = 22h) [reset = h]

Short Description: Data Filter Parameter Register for Ch1

Long Description:

Return to Summary Table

Table 3-1478. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8022h
CONTROLSS_SDFM1	5026 9022h

Access Types Legend

Table 3-1479. SDDFPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	SDSYNCEN	RW	0h	PWM synchronization (SDSYNC) of data filter 0: PWM synchronization of data filter is disabled 1: PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs
11 - 10	SST	RW	0h	Data filter structure 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure
9	AE	RW	0h	Data filter Acknowledge Enable 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter
8	FEN	RW	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO
7 - 0	DOSR	RW	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256.

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3.22.9 CONTROLSS_SDFMn_SDDPARM1 Registers

3.22.9.1 SDFMn_SDDPARM1 Register (Offset = 24h) [reset = h]

Short Description: Data Parameter Register for Ch1

Long Description:

Return to Summary Table

Table 3-1480. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8024h
CONTROLSS_SDFM1	5026 9024h

Access Types Legend

Table 3-1481. SDDPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	SH	RW	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen.
10	DR	RW	0h	Data filter Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement
9 - 0	RESERVED	RO RRETURNS 0S		Reserved

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3.22.10 CONTROLSS_SDFMn_SDFLT1CMPH1 Registers

3.22.10.1 SDFMn_SDFLT1CMPH1 Register (Offset = 26h) [reset = h]

Short Description: High-level Threshold Register for Ch1

Long Description:

Return to Summary Table

Table 3-1482. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8026h
CONTROLSS_SDFM1	5026 9026h

Access Types Legend

Table 3-1483. SDFLT1CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLT	RW	7FFFh	Unsigned high-level threshold for the comparator filter output.

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3.22.11 CONTROLSS_SDFMn_SDFLT1CMPL1 Registers

3.22.11.1 SDFMn_SDFLT1CMPL1 Register (Offset = 28h) [reset = h]

Short Description: Low-level Threshold Register for Ch1

Long Description:

Return to Summary Table

Table 3-1484. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8028h
CONTROLSS_SDFM1	5026 9028h

Access Types Legend

Table 3-1485. SDFLT1CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	LLT	RW	0h	Unsigned low-level threshold for the comparator filter output.

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3.22.12 CONTROLSS_SDFMn_SDCPARM1 Registers

3.22.12.1 SDFMn_SDCPARM1 Register (Offset = 2Ah) [reset = h]

Short Description: Comparator Filter Parameter Register for Ch1

Long Description:

Return to Summary Table

Table 3-1486. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 802Ah
CONTROLSS_SDFM1	5026 902Ah

Access Types Legend

Table 3-1487. SDCPARM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	CEVT2SEL	RW	0h	Comparator Event2 Select 00: COMPL1 01: COMPL1 OR COMPH1 10: COMPL2 11: COMPL2 OR COMPH2
13	CEN	RW	0h	Comparator Filter enable 0: Disable comparator filter 1: Enable comparator filter
12 - 11	CEVT1SEL	RW	0h	Comparator Event1 Select 00: COMPH1 01: COMPL1 OR COMPH1 10: COMPH2 11: COMPL2 OR COMPH2
10	HZEN	RW	0h	High level (Z) Threshold crossing output enable 0: Disable Higher level Threshold (Z) crossing 1: Enable Higher level Threhold (Z) crossing
9	MFIE	RW	0h	Modulator Failure Interrupt Enable 0: Disable modulator failure interrupt and its flag 1: Enable modulator failure interrupt and its flag
8 - 7	CS1_CS0	RW	0h	Comparator filter structure 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure
6	EN_CEVT2	RW	0h	CEVT2 interrupt enable 0: Disable CEVT2 interrupt 1: Enable CEVT2 interrupt
5	EN_CEVT1	RW	0h	CEVT1 interrupt enable 0: Disable CEVT1 interrupt 1: Enable CEVT1 interrupt
4 - 0	COSR	RW	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32

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3.22.13 CONTROLSS_SDFMn_SDDATA1 Registers

3.22.13.1 SDFMn_SDDATA1 Register (Offset = 2Ch) [reset = h]

Short Description: Data Filter Data Register (16 or 32bit) for Ch1

Long Description:

Return to Summary Table

Table 3-1488. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 802Ch
CONTROLSS_SDFM1	5026 902Ch

Access Types Legend

Table 3-1489. SDDATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA32HI	RO	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode
15 - 0	DATA16	RO	0h	Lo-order 16b in 32b mode

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3.22.14 CONTROLSS_SDFMn_SDDATFIFO1 Registers

3.22.14.1 SDFMn_SDDATFIFO1 Register (Offset = 30h) [reset = h]

Short Description: Filter Data FIFO Output(32b) for Ch1

Long Description:

Return to Summary Table

Table 3-1490. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8030h
CONTROLSS_SDFM1	5026 9030h

Access Types Legend

Table 3-1491. SDDATFIFO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA32HI	RO	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode
15 - 0	DATA16	RO	0h	Lo-order 16b in 32b mode

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3.22.15 CONTROLSS_SDFMn_SDCDATA1 Registers

3.22.15.1 SDFMn_SDCDATA1 Register (Offset = 34h) [reset = h]

Short Description: Comparator Filter Data Register (16b) for Ch1

Long Description:

Return to Summary Table

Table 3-1492. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8034h
CONTROLSS_SDFM1	5026 9034h

Access Types Legend

Table 3-1493. SDCDATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	DATA16	RO	0h	Comparator Data output - 16b only

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3.22.16 CONTROLSS_SDFMn_SDFLT1CMPH2 Registers

3.22.16.1 SDFMn_SDFLT1CMPH2 Register (Offset = 36h) [reset = h]

Short Description: Second high level threhold for CH1

Long Description:

Return to Summary Table

Table 3-1494. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8036h
CONTROLSS_SDFM1	5026 9036h

Access Types Legend

Table 3-1495. SDFLT1CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLT2	RW	7FFFh	Second Unsigned high-level threshold for the comparator filter output.

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3.22.17 CONTROLSS_SDFMn_SDFLT1CMPHZ Registers

3.22.17.1 SDFMn_SDFLT1CMPHZ Register (Offset = 38h) [reset = h]

Short Description: High-level (Z) Threshold Register for Ch1

Long Description:

Return to Summary Table

Table 3-1496. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8038h
CONTROLSS_SDFM1	5026 9038h

Access Types Legend

Table 3-1497. SDFLT1CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLTZ	RW	0h	Unsigned High-level threshold (Z) for the comparator filter output Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt.

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3.22.18 CONTROLSS_SDFMn_SDFIFOCTL1 Registers

3.22.18.1 SDFMn_SDFIFOCTL1 Register (Offset = 3Ah) [reset = h]

Short Description: FIFO Control Register for Ch1

Long Description:

Return to Summary Table

Table 3-1498. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 803Ah
CONTROLSS_SDFM1	5026 903Ah

Access Types Legend

Table 3-1499. SDFIFOCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	RW	0h	SDFIFO Overflow interrupt enable 0: SDFIFO Overflow condition will not generate an interrupt 1: SDFIFO overflow condition generates an interrupt on SDy_ERR
14	DRINTSEL	RW	0h	Data-Ready Interrupt (DRINT) source select 0 = AF1 (Select non-FIFO data-ready interrupt) 1 = SDFFINT1 (Select FIFO data-ready interrupt)
13	FFEN	RW	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared
12	FFIEN	RW	0h	SDFIFO data ready Interrupt Enable
11	RESERVED	RO RRETURNS 0S		Reserved
10 - 6	SDFFST	RO	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words
5	RESERVED	RO RRETURNS 0S		Reserved
4 - 0	SDFFIL	RW	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status (SDFFST) '= FIFO level (SDFFIL)

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3.22.19 CONTROLSS_SDFMn_SDSYNC1 Registers

3.22.19.1 SDFMn_SDSYNC1 Register (Offset = 3Ch) [reset = h]

Short Description: SD Filter Sync control for Ch1

Long Description:

Return to Summary Table

Table 3-1500. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 803Ch
CONTROLSS_SDFM1	5026 903Ch

Access Types Legend

Table 3-1501. SDSYNC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO RRETURNS 0S		Reserved
10	WTSCLREN	RW	1h	WTSYNFLG Clear-on-FIFOINT Enable 0: WTSYNFLG can only be cleared manually (using WTSYNCLR bit) 1: WTSYNFLG is cleared automatically on SDFFINT
9	FFSYNCCLREN	RW	0h	FIFO Clear-on-SDSYNC Enable 0: SDFIFO is not automaticaly cleared upon receiving SDSYNC 1: SDFIFO is automaticaly cleared upon receiving SDSYNC
8	WTSYNCLR	RW RRETURNS 0S	0h	Wait-for-Sync Flag Clear (always reads 0) 0: Write of 0 has no affect 1: Write of 1 clears WTSYNFLG
7	WTSYNFLG	RO	0h	Wait-for-Sync Flag 0: SDSYNC event has not occurred 1: SDSYNC event occurred.
6	WTSYNCEN	RW	0h	Wait-for-Sync Enable 0: Incoming Data written to SDFIFO on every Data-Ready (DR) Event 1: Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs
5 - 0	SYNCSEL	RW	0h	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table

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3.22.20 CONTROLSS_SDFMn_SDFLT1CMPL2 Registers

3.22.20.1 SDFMn_SDFLT1CMPL2 Register (Offset = 3Eh) [reset = h]

Short Description: Second low level threhold for CH1

Long Description:

Return to Summary Table

Table 3-1502. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 803Eh
CONTROLSS_SDFM1	5026 903Eh

Access Types Legend

Table 3-1503. SDFLT1CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	LLT2	RW	0h	Second Unsigned low-level threshold for the comparator filter output.

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3.22.21 CONTROLSS_SDFMn_SDCTLPARM2 Registers

3.22.21.1 SDFMn_SDCTLPARM2 Register (Offset = 40h) [reset = h]

Short Description: Control Parameter Register for Ch2

Long Description:

Return to Summary Table

Table 3-1504. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8040h
CONTROLSS_SDFM1	5026 9040h

Access Types Legend

Table 3-1505. SDCTLPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO		Reserved
7	RESERVED	RO RRETURNS 0S		Reserved
6	SDDATASYNC	RW	0h	0: SD Data is not passed through a synchronizer. 1: SD Data is passed through a synchronizer.
5	RESERVED	RO RRETURNS 0S		Reserved
4	SDCLKSYNC	RW	0h	0: SD Clock is not passed through a synchronizer. 1: SD Clock is passed through a synchronizer.
3	SDCLKSEL	RW	0h	SD2 Clock source select. 0: Clock source to SDFM filter is its channel clock. 1: Clock source to SDFM filter is SD1 filter clock.
2	RESERVED	RW		Reserved
1 - 0	MOD	RW	0h	Modulator clock modes 0: Mode 0: Modulator clock running at 1x data rate 1: Reserved 2: Reserved 3: Reserved

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3.22.22 CONTROLSS_SDFMn_SDDFPARM2 Registers

3.22.22.1 SDFMn_SDDFPARM2 Register (Offset = 42h) [reset = h]

Short Description: Data Filter Parameter Register for Ch2

Long Description:

Return to Summary Table

Table 3-1506. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8042h
CONTROLSS_SDFM1	5026 9042h

Access Types Legend

Table 3-1507. SDDFPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	SDSYNCEN	RW	0h	PWM synchronization (SDSYNC) of data filter 0: PWM synchronization of data filter is disabled 1: PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs
11 - 10	SST	RW	0h	Data filter structure 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure
9	AE	RW	0h	Data filter Acknowledge Enable 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter
8	FEN	RW	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO
7 - 0	DOSR	RW	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256.

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3.22.23 CONTROLSS_SDFMn_SDDPARM2 Registers

3.22.23.1 SDFMn_SDDPARM2 Register (Offset = 44h) [reset = h]

Short Description: Data Parameter Register for Ch2

Long Description:

Return to Summary Table

Table 3-1508. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8044h
CONTROLSS_SDFM1	5026 9044h

Access Types Legend

Table 3-1509. SDDPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	SH	RW	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen.
10	DR	RW	0h	Data filter Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement
9 - 0	RESERVED	RO RRETURNS 0S		Reserved

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3.22.24 CONTROLSS_SDFMn_SDFLT2CMPH1 Registers

3.22.24.1 SDFMn_SDFLT2CMPH1 Register (Offset = 46h) [reset = h]

Short Description: High-level Threshold Register for Ch2

Long Description:

Return to Summary Table

Table 3-1510. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8046h
CONTROLSS_SDFM1	5026 9046h

Access Types Legend

Table 3-1511. SDFLT2CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLT	RW	7FFFh	Unsigned high-level threshold for the comparator filter output.

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3.22.25 CONTROLSS_SDFMn_SDFLT2CMPL1 Registers

3.22.25.1 SDFMn_SDFLT2CMPL1 Register (Offset = 48h) [reset = h]

Short Description: Low-level Threshold Register for Ch2

Long Description:

Return to Summary Table

Table 3-1512. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8048h
CONTROLSS_SDFM1	5026 9048h

Access Types Legend

Table 3-1513. SDFLT2CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	LLT	RW	0h	Unsigned low-level threshold for the comparator filter output.

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3.22.26 CONTROLSS_SDFMn_SDCPARM2 Registers

3.22.26.1 SDFMn_SDCPARM2 Register (Offset = 4Ah) [reset = h]

Short Description: Comparator Filter Parameter Register for Ch2

Long Description:

Return to Summary Table

Table 3-1514. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 804Ah
CONTROLSS_SDFM1	5026 904Ah

Access Types Legend

Table 3-1515. SDCPARM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	CEVT2SEL	RW	0h	Comparator Event2 Select 00: COMPL1 01: COMPL1 OR COMPH1 10: COMPL2 11: COMPL2 OR COMPH2
13	CEN	RW	0h	Comparator Filter enable 0: Disable comparator filter 1: Enable comparator filter
12 - 11	CEVT1SEL	RW	0h	Comparator Event1 Select 00: COMPH1 01: COMPL1 OR COMPH1 10: COMPH2 11: COMPL2 OR COMPH2
10	HZEN	RW	0h	High level (Z) Threshold crossing output enable 0: Disable Higher level Threshold (Z) crossing 1: Enable Higher level Threhold (Z) crossing
9	MFIE	RW	0h	Modulator Failure Interrupt Enable 0: Disable modulator failure interrupt and its flag 1: Enable modulator failure interrupt and its flag
8 - 7	CS1_CS0	RW	0h	Comparator filter structure 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure
6	EN_CEVT2	RW	0h	CEVT2 interrupt enable 0: Disable CEVT2 interrupt 1: Enable CEVT2 interrupt
5	EN_CEVT1	RW	0h	CEVT1 interrupt enable 0: Disable CEVT1 interrupt 1: Enable CEVT1 interrupt
4 - 0	COSR	RW	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32

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3.22.27 CONTROLSS_SDFMn_SDDATA2 Registers

3.22.27.1 SDFMn_SDDATA2 Register (Offset = 4Ch) [reset = h]

Short Description: Data Filter Data Register (16 or 32bit) for Ch2

Long Description:

Return to Summary Table

Table 3-1516. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 804Ch
CONTROLSS_SDFM1	5026 904Ch

Access Types Legend

Table 3-1517. SDDATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA32HI	RO	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode
15 - 0	DATA16	RO	0h	Lo-order 16b in 32b mode

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3.22.28 CONTROLSS_SDFMn_SDDATFIFO2 Registers

3.22.28.1 SDFMn_SDDATFIFO2 Register (Offset = 50h) [reset = h]

Short Description: Filter Data FIFO Output(32b) for Ch2

Long Description:

Return to Summary Table

Table 3-1518. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8050h
CONTROLSS_SDFM1	5026 9050h

Access Types Legend

Table 3-1519. SDDATFIFO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA32HI	RO	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode
15 - 0	DATA16	RO	0h	Lo-order 16b in 32b mode

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3.22.29 CONTROLSS_SDFMn_SDCDATA2 Registers

3.22.29.1 SDFMn_SDCDATA2 Register (Offset = 54h) [reset = h]

Short Description: Comparator Filter Data Register (16b) for Ch2

Long Description:

Return to Summary Table

Table 3-1520. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8054h
CONTROLSS_SDFM1	5026 9054h

Access Types Legend

Table 3-1521. SDCDATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	DATA16	RO	0h	Comparator Data output - 16b only

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3.22.30 CONTROLSS_SDFMn_SDFLT2CMPH2 Registers

3.22.30.1 SDFMn_SDFLT2CMPH2 Register (Offset = 56h) [reset = h]

Short Description: Second high level threhold for CH2

Long Description:

Return to Summary Table

Table 3-1522. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8056h
CONTROLSS_SDFM1	5026 9056h

Access Types Legend

Table 3-1523. SDFLT2CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLT2	RW	7FFFh	Second Unsigned high-level threshold for the comparator filter output.

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3.22.31 CONTROLSS_SDFMn_SDFLT2CMPHZ Registers

3.22.31.1 SDFMn_SDFLT2CMPHZ Register (Offset = 58h) [reset = h]

Short Description: High-level (Z) Threshold Register for Ch2

Long Description:

Return to Summary Table

Table 3-1524. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8058h
CONTROLSS_SDFM1	5026 9058h

Access Types Legend

Table 3-1525. SDFLT2CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLTZ	RW	0h	Unsigned High-level threshold (Z) for the comparator filter output Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt.

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3.22.32 CONTROLSS_SDFMn_SDFIFOCTL2 Registers

3.22.32.1 SDFMn_SDFIFOCTL2 Register (Offset = 5Ah) [reset = h]

Short Description: FIFO Control Register for Ch2

Long Description:

Return to Summary Table

Table 3-1526. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 805Ah
CONTROLSS_SDFM1	5026 905Ah

Access Types Legend

Table 3-1527. SDFIFOCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	RW	0h	SDFIFO Overflow interrupt enable 0: SDFIFO Overflow condition will not generate an interrupt 1: SDFIFO overflow condition generates an interrupt on SDy_ERR
14	DRINTSEL	RW	0h	Data-Ready Interrupt (DRINT) source select 0 = AF1 (Select non-FIFO data-ready interrupt) 1 = SDFFINT1 (Select FIFO data-ready interrupt)
13	FFEN	RW	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared
12	FFIEN	RW	0h	SDFIFO data ready Interrupt Enable
11	RESERVED	RO RRETURNS 0S		Reserved
10 - 6	SDFFST	RO	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words
5	RESERVED	RO RRETURNS 0S		Reserved
4 - 0	SDFFIL	RW	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status (SDFFST) '= FIFO level (SDFFIL)

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3.22.33 CONTROLSS_SDFMn_SDSYNC2 Registers

3.22.33.1 SDFMn_SDSYNC2 Register (Offset = 5Ch) [reset = h]

Short Description: SD Filter Sync control for Ch2

Long Description:

Return to Summary Table

Table 3-1528. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 805Ch
CONTROLSS_SDFM1	5026 905Ch

Access Types Legend

Table 3-1529. SDSYNC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO RRETURNS 0S		Reserved
10	WTSCLREN	RW	1h	WTSYNFLG Clear-on-FIFOINT Enable 0: WTSYNFLG can only be cleared manually (using WTSYNCLR bit) 1: WTSYNFLG is cleared automatically on SDFFINT
9	FFSYNCCLREN	RW	0h	FIFO Clear-on-SDSYNC Enable 0: SDFIFO is not automaticaly cleared upon receiving SDSYNC 1: SDFIFO is automaticaly cleared upon receiving SDSYNC
8	WTSYNCLR	RW RRETURNS 0S	0h	Wait-for-Sync Flag Clear (always reads 0) 0: Write of 0 has no affect 1: Write of 1 clears WTSYNFLG
7	WTSYNFLG	RO	0h	Wait-for-Sync Flag 0: SDSYNC event has not occurred 1: SDSYNC event occurred.
6	WTSYNCEN	RW	0h	Wait-for-Sync Enable 0: Incoming Data written to SDFIFO on every Data-Ready (DR) Event 1: Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs
5 - 0	SYNCSEL	RW	0h	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table

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3.22.34 CONTROLSS_SDFMn_SDFLT2CMPL2 Registers

3.22.34.1 SDFMn_SDFLT2CMPL2 Register (Offset = 5Eh) [reset = h]

Short Description: Second low level threhold for CH2

Long Description:

Return to Summary Table

Table 3-1530. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 805Eh
CONTROLSS_SDFM1	5026 905Eh

Access Types Legend

Table 3-1531. SDFLT2CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	LLT2	RW	0h	Second Unsigned low-level threshold for the comparator filter output.

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3.22.35 CONTROLSS_SDFMn_SDCTLPARM3 Registers

3.22.35.1 SDFMn_SDCTLPARM3 Register (Offset = 60h) [reset = h]

Short Description: Control Parameter Register for Ch3

Long Description:

Return to Summary Table

Table 3-1532. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8060h
CONTROLSS_SDFM1	5026 9060h

Access Types Legend

Table 3-1533. SDCTLPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO		Reserved
7	RESERVED	RO RRETURNS 0S		Reserved
6	SDDATASYNC	RW	0h	0: SD Data is not passed through a synchronizer. 1: SD Data is passed through a synchronizer.
5	RESERVED	RO RRETURNS 0S		Reserved
4	SDCLKSYNC	RW	0h	0: SD Clock is not passed through a synchronizer. 1: SD Clock is passed through a synchronizer.
3	SDCLKSEL	RW	0h	SD3 Clock source select. 0: Clock source to SDFM filter is its channel clock. 1: Clock source to SDFM filter is SD1 filter clock.
2	RESERVED	RW		Reserved
1 - 0	MOD	RW	0h	Modulator clock modes 0: Mode 0: Modulator clock running at 1x data rate 1: Reserved 2: Reserved 3: Reserved

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3.22.36 CONTROLSS_SDFMn_SDDFPARM3 Registers

3.22.36.1 SDFMn_SDDFPARM3 Register (Offset = 62h) [reset = h]

Short Description: Data Filter Parameter Register for Ch3

Long Description:

Return to Summary Table

Table 3-1534. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8062h
CONTROLSS_SDFM1	5026 9062h

Access Types Legend

Table 3-1535. SDDFPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	SDSYNCEN	RW	0h	PWM synchronization (SDSYNC) of data filter 0: PWM synchronization of data filter is disabled 1: PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs
11 - 10	SST	RW	0h	Data filter structure 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure
9	AE	RW	0h	Data filter Acknowledge Enable 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter
8	FEN	RW	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO
7 - 0	DOSR	RW	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256.

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3.22.37 CONTROLSS_SDFMn_SDDPARM3 Registers

3.22.37.1 SDFMn_SDDPARM3 Register (Offset = 64h) [reset = h]

Short Description: Data Parameter Register for Ch3

Long Description:

Return to Summary Table

Table 3-1536. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8064h
CONTROLSS_SDFM1	5026 9064h

Access Types Legend

Table 3-1537. SDDPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	SH	RW	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen.
10	DR	RW	0h	Data filter Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement
9 - 0	RESERVED	RO RRETURNS 0S		Reserved

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3.22.38 CONTROLSS_SDFMn_SDFLT3CMPH1 Registers

3.22.38.1 SDFMn_SDFLT3CMPH1 Register (Offset = 66h) [reset = h]

Short Description: High-level Threshold Register for Ch3

Long Description:

Return to Summary Table

Table 3-1538. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8066h
CONTROLSS_SDFM1	5026 9066h

Access Types Legend

Table 3-1539. SDFLT3CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLT	RW	7FFFh	Unsigned high-level threshold for the comparator filter output.

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3.22.39 CONTROLSS_SDFMn_SDFLT3CMPL1 Registers

3.22.39.1 SDFMn_SDFLT3CMPL1 Register (Offset = 68h) [reset = h]

Short Description: Low-level Threshold Register for Ch3

Long Description:

Return to Summary Table

Table 3-1540. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8068h
CONTROLSS_SDFM1	5026 9068h

Access Types Legend

Table 3-1541. SDFLT3CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	LLT	RW	0h	Unsigned low-level threshold for the comparator filter output.

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3.22.40 CONTROLSS_SDFMn_SDCPARM3 Registers

3.22.40.1 SDFMn_SDCPARM3 Register (Offset = 6Ah) [reset = h]

Short Description: Comparator Filter Parameter Register for Ch3

Long Description:

Return to Summary Table

Table 3-1542. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 806Ah
CONTROLSS_SDFM1	5026 906Ah

Access Types Legend

Table 3-1543. SDCPARM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	CEVT2SEL	RW	0h	Comparator Event2 Select 00: COMPL1 01: COMPL1 OR COMPH1 10: COMPL2 11: COMPL2 OR COMPH2
13	CEN	RW	0h	Comparator Filter enable 0: Disable comparator filter 1: Enable comparator filter
12 - 11	CEVT1SEL	RW	0h	Comparator Event1 Select 00: COMPH1 01: COMPL1 OR COMPH1 10: COMPH2 11: COMPL2 OR COMPH2
10	HZEN	RW	0h	High level (Z) Threshold crossing output enable 0: Disable Higher level Threshold (Z) crossing 1: Enable Higher level Threhold (Z) crossing
9	MFIE	RW	0h	Modulator Failure Interrupt Enable 0: Disable modulator failure interrupt and its flag 1: Enable modulator failure interrupt and its flag
8 - 7	CS1_CS0	RW	0h	Comparator filter structure 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure
6	EN_CEVT2	RW	0h	CEVT2 interrupt enable 0: Disable CEVT2 interrupt 1: Enable CEVT2 interrupt
5	EN_CEVT1	RW	0h	CEVT1 interrupt enable 0: Disable CEVT1 interrupt 1: Enable CEVT1 interrupt
4 - 0	COSR	RW	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32

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3.22.41 CONTROLSS_SDFMn_SDDATA3 Registers

3.22.41.1 SDFMn_SDDATA3 Register (Offset = 6Ch) [reset = h]

Short Description: Data Filter Data Register (16 or 32bit) for Ch3

Long Description:

Return to Summary Table

Table 3-1544. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 806Ch
CONTROLSS_SDFM1	5026 906Ch

Access Types Legend

Table 3-1545. SDDATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA32HI	RO	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode
15 - 0	DATA16	RO	0h	Lo-order 16b in 32b mode

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3.22.42 CONTROLSS_SDFMn_SDDATFIFO3 Registers

3.22.42.1 SDFMn_SDDATFIFO3 Register (Offset = 70h) [reset = h]

Short Description: Filter Data FIFO Output(32b) for Ch3

Long Description:

Return to Summary Table

Table 3-1546. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8070h
CONTROLSS_SDFM1	5026 9070h

Access Types Legend

Table 3-1547. SDDATFIFO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA32HI	RO	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode
15 - 0	DATA16	RO	0h	Lo-order 16b in 32b mode

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3.22.43 CONTROLSS_SDFMn_SDCDATA3 Registers

3.22.43.1 SDFMn_SDCDATA3 Register (Offset = 74h) [reset = h]

Short Description: Comparator Filter Data Register (16b) for Ch3

Long Description:

Return to Summary Table

Table 3-1548. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8074h
CONTROLSS_SDFM1	5026 9074h

Access Types Legend

Table 3-1549. SDCDATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	DATA16	RO	0h	Comparator Data output - 16b only

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3.22.44 CONTROLSS_SDFMn_SDFLT3CMPH2 Registers

3.22.44.1 SDFMn_SDFLT3CMPH2 Register (Offset = 76h) [reset = h]

Short Description: Second high level threhold for CH3

Long Description:

Return to Summary Table

Table 3-1550. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8076h
CONTROLSS_SDFM1	5026 9076h

Access Types Legend

Table 3-1551. SDFLT3CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLT2	RW	7FFFh	Second Unsigned high-level threshold for the comparator filter output.

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3.22.45 CONTROLSS_SDFMn_SDFLT3CMPHZ Registers

3.22.45.1 SDFMn_SDFLT3CMPHZ Register (Offset = 78h) [reset = h]

Short Description: High-level (Z) Threshold Register for Ch3

Long Description:

Return to Summary Table

Table 3-1552. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8078h
CONTROLSS_SDFM1	5026 9078h

Access Types Legend

Table 3-1553. SDFLT3CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLTZ	RW	0h	Unsigned High-level threshold (Z) for the comparator filter output Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt.

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3.22.46 CONTROLSS_SDFMn_SDFIFOCTL3 Registers

3.22.46.1 SDFMn_SDFIFOCTL3 Register (Offset = 7Ah) [reset = h]

Short Description: FIFO Control Register for Ch3

Long Description:

Return to Summary Table

Table 3-1554. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 807Ah
CONTROLSS_SDFM1	5026 907Ah

Access Types Legend

Table 3-1555. SDFIFOCTL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	RW	0h	SDFIFO Overflow interrupt enable 0: SDFIFO Overflow condition will not generate an interrupt 1: SDFIFO overflow condition generates an interrupt on SDy_ERR
14	DRINTSEL	RW	0h	Data-Ready Interrupt (DRINT) source select 0 = AF1 (Select non-FIFO data-ready interrupt) 1 = SDFFINT1 (Select FIFO data-ready interrupt)
13	FFEN	RW	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared
12	FFIEN	RW	0h	SDFIFO data ready Interrupt Enable
11	RESERVED	RO RRETURNS 0S		Reserved
10 - 6	SDFFST	RO	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words
5	RESERVED	RO RRETURNS 0S		Reserved
4 - 0	SDFFIL	RW	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status (SDFFST) '= FIFO level (SDFFIL)

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3.22.47 CONTROLSS_SDFMn_SDSYNC3 Registers

3.22.47.1 SDFMn_SDSYNC3 Register (Offset = 7Ch) [reset = h]

Short Description: SD Filter Sync control for Ch3

Long Description:

Return to Summary Table

Table 3-1556. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 807Ch
CONTROLSS_SDFM1	5026 907Ch

Access Types Legend

Table 3-1557. SDSYNC3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO RRETURNS 0S		Reserved
10	WTSCLREN	RW	1h	WTSYNFLG Clear-on-FIFOINT Enable 0: WTSYNFLG can only be cleared manually (using WTSYNCLR bit) 1: WTSYNFLG is cleared automatically on SDFFINT
9	FFSYNCCLREN	RW	0h	FIFO Clear-on-SDSYNC Enable 0: SDFIFO is not automaticaly cleared upon receiving SDSYNC 1: SDFIFO is automaticaly cleared upon receiving SDSYNC
8	WTSYNCLR	RW RRETURNS 0S	0h	Wait-for-Sync Flag Clear (always reads 0) 0: Write of 0 has no affect 1: Write of 1 clears WTSYNFLG
7	WTSYNFLG	RO	0h	Wait-for-Sync Flag 0: SDSYNC event has not occurred 1: SDSYNC event occurred.
6	WTSYNCEN	RW	0h	Wait-for-Sync Enable 0: Incoming Data written to SDFIFO on every Data-Ready (DR) Event 1: Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs
5 - 0	SYNCSEL	RW	0h	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table

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3.22.48 CONTROLSS_SDFMn_SDFLT3CMPL2 Registers

3.22.48.1 SDFMn_SDFLT3CMPL2 Register (Offset = 7Eh) [reset = h]

Short Description: Second low level threhold for CH3

Long Description:

Return to Summary Table

Table 3-1558. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 807Eh
CONTROLSS_SDFM1	5026 907Eh

Access Types Legend

Table 3-1559. SDFLT3CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	LLT2	RW	0h	Second Unsigned low-level threshold for the comparator filter output.

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3.22.49 CONTROLSS_SDFMn_SDCTLPARM4 Registers

3.22.49.1 SDFMn_SDCTLPARM4 Register (Offset = 80h) [reset = h]

Short Description: Control Parameter Register for Ch4

Long Description:

Return to Summary Table

Table 3-1560. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8080h
CONTROLSS_SDFM1	5026 9080h

Access Types Legend

Table 3-1561. SDCTLPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	RESERVED	RO		Reserved
7	RESERVED	RO RRETURNS 0S		Reserved
6	SDDATASYNC	RW	0h	0: SD Data is not passed through a synchronizer. 1: SD Data is passed through a synchronizer.
5	RESERVED	RO RRETURNS 0S		Reserved
4	SDCLKSYNC	RW	0h	0: SD Clock is not passed through a synchronizer. 1: SD Clock is passed through a synchronizer.
3	SDCLKSEL	RW	0h	SD4 Clock source select. 0: Clock source to SDFM filter is its channel clock. 1: Clock source to SDFM filter is SD1 filter clock.
2	RESERVED	RW		Reserved
1 - 0	MOD	RW	0h	Modulator clock modes 0: Mode 0: Modulator clock running at 1x data rate 1: Reserved 2: Reserved 3: Reserved

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3.22.50 CONTROLSS_SDFMn_SDDFPARM4 Registers

3.22.50.1 SDFMn_SDDFPARM4 Register (Offset = 82h) [reset = h]

Short Description: Data Filter Parameter Register for Ch4

Long Description:

Return to Summary Table

Table 3-1562. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8082h
CONTROLSS_SDFM1	5026 9082h

Access Types Legend

Table 3-1563. SDDFPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 13	RESERVED	RO		Reserved
12	SDSYNCEN	RW	0h	PWM synchronization (SDSYNC) of data filter 0: PWM synchronization of data filter is disabled 1: PWM synchronization of data filter is enabled Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs
11 - 10	SST	RW	0h	Data filter structure 00: Data filter runs with a Sincfast structure 01: Data filter runs with a Sinc1 structure 10: Data filter runs with a Sinc2 structure 11: Data filter runs with a Sinc3 structure
9	AE	RW	0h	Data filter Acknowledge Enable 0: Acknowledge flag is disabled for the particular filter 1: Acknowledge flag is enabled for the particular filter
8	FEN	RW	0h	Filter Enable 0: The data filter is disabled and no data is produced 1: The data filter is enabled and data are produced in the data filter Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO
7 - 0	DOSR	RW	0h	Data filter Oversampling ratio The actual oversampling ratio of data filter is DOSR + 1 These bits set the oversampling ratio of the data filter. 0x0FF represents an oversampling ratio of 256.

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3.22.51 CONTROLSS_SDFMn_SDDPARM4 Registers

3.22.51.1 SDFMn_SDDPARM4 Register (Offset = 84h) [reset = h]

Short Description: Data Parameter Register for Ch4

Long Description:

Return to Summary Table

Table 3-1564. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8084h
CONTROLSS_SDFM1	5026 9084h

Access Types Legend

Table 3-1565. SDDPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	SH	RW	0h	Shift Control These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen.
10	DR	RW	0h	Data filter Data representation 0: Data stored in 16b 2's complement 1: Data stored in 32b 2's complement
9 - 0	RESERVED	RO RRETURNS 0S		Reserved

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3.22.52 CONTROLSS_SDFMn_SDFLT4CMPH1 Registers

3.22.52.1 SDFMn_SDFLT4CMPH1 Register (Offset = 86h) [reset = h]

Short Description: High-level Threshold Register for Ch4

Long Description:

Return to Summary Table

Table 3-1566. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8086h
CONTROLSS_SDFM1	5026 9086h

Access Types Legend

Table 3-1567. SDFLT4CMPH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLT	RW	7FFFh	Unsigned high-level threshold for the comparator filter output.

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3.22.53 CONTROLSS_SDFMn_SDFLT4CMPL1 Registers

3.22.53.1 SDFMn_SDFLT4CMPL1 Register (Offset = 88h) [reset = h]

Short Description: Low-level Threshold Register for Ch4

Long Description:

Return to Summary Table

Table 3-1568. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8088h
CONTROLSS_SDFM1	5026 9088h

Access Types Legend

Table 3-1569. SDFLT4CMPL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	LLT	RW	0h	Unsigned low-level threshold for the comparator filter output.

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3.22.54 CONTROLSS_SDFMn_SDCPARM4 Registers

3.22.54.1 SDFMn_SDCPARM4 Register (Offset = 8Ah) [reset = h]

Short Description: Comparator Filter Parameter Register for Ch4

Long Description:

Return to Summary Table

Table 3-1570. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 808Ah
CONTROLSS_SDFM1	5026 908Ah

Access Types Legend

Table 3-1571. SDCPARM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 14	CEVT2SEL	RW	0h	Comparator Event2 Select 00: COMPL1 01: COMPL1 OR COMPH1 10: COMPL2 11: COMPL2 OR COMPH2
13	CEN	RW	0h	Comparator Filter enable 0: Disable comparator filter 1: Enable comparator filter
12 - 11	CEVT1SEL	RW	0h	Comparator Event1 Select 00: COMPH1 01: COMPL1 OR COMPH1 10: COMPH2 11: COMPL2 OR COMPH2
10	HZEN	RW	0h	High level (Z) Threshold crossing output enable 0: Disable Higher level Threshold (Z) crossing 1: Enable Higher level Threhold (Z) crossing
9	MFIE	RW	0h	Modulator Failure Interrupt Enable 0: Disable modulator failure interrupt and its flag 1: Enable modulator failure interrupt and its flag
8 - 7	CS1_CS0	RW	0h	Comparator filter structure 00: Comparator filter runs with a sincfast structure 01: Comparator filter runs with a Sinc1 structure 10: Comparator filter runs with a Sinc2 structure 11: Comparator filter runs with a Sinc3 structure
6	EN_CEVT2	RW	0h	CEVT2 interrupt enable 0: Disable CEVT2 interrupt 1: Enable CEVT2 interrupt
5	EN_CEVT1	RW	0h	CEVT1 interrupt enable 0: Disable CEVT1 interrupt 1: Enable CEVT1 interrupt
4 - 0	COSR	RW	0h	Comparator Oversampling ratio. The actual rate is COSR + 1. These bits set the oversampling ratio of the filter. 0x1F represents an oversampling ratio of 32

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3.22.55 CONTROLSS_SDFMn_SDDATA4 Registers

3.22.55.1 SDFMn_SDDATA4 Register (Offset = 8Ch) [reset = h]

Short Description: Data Filter Data Register (16 or 32bit) for Ch4

Long Description:

Return to Summary Table

Table 3-1572. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 808Ch
CONTROLSS_SDFM1	5026 908Ch

Access Types Legend

Table 3-1573. SDDATA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA32HI	RO	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode
15 - 0	DATA16	RO	0h	Lo-order 16b in 32b mode

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3.22.56 CONTROLSS_SDFMn_SDDATFIFO4 Registers

3.22.56.1 SDFMn_SDDATFIFO4 Register (Offset = 90h) [reset = h]

Short Description: Filter Data FIFO Output(32b) for Ch4

Long Description:

Return to Summary Table

Table 3-1574. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8090h
CONTROLSS_SDFM1	5026 9090h

Access Types Legend

Table 3-1575. SDDATFIFO4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DATA32HI	RO	0h	Hi-order 16b in 32b mode, 16-bit Data in 16b mode
15 - 0	DATA16	RO	0h	Lo-order 16b in 32b mode

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3.22.57 CONTROLSS_SDFMn_SDCDATA4 Registers

3.22.57.1 SDFMn_SDCDATA4 Register (Offset = 94h) [reset = h]

Short Description: Comparator Filter Data Register (16b) for Ch4

Long Description:

Return to Summary Table

Table 3-1576. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8094h
CONTROLSS_SDFM1	5026 9094h

Access Types Legend

Table 3-1577. SDCDATA4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	DATA16	RO	0h	Comparator Data output - 16b only

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3.22.58 CONTROLSS_SDFMn_SDFLT4CMPH2 Registers

3.22.58.1 SDFMn_SDFLT4CMPH2 Register (Offset = 96h) [reset = h]

Short Description: Second high level threhold for CH4

Long Description:

Return to Summary Table

Table 3-1578. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8096h
CONTROLSS_SDFM1	5026 9096h

Access Types Legend

Table 3-1579. SDFLT4CMPH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLT2	RW	7FFFh	Second Unsigned high-level threshold for the comparator filter output.

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3.22.59 CONTROLSS_SDFMn_SDFLT4CMPHZ Registers

3.22.59.1 SDFMn_SDFLT4CMPHZ Register (Offset = 98h) [reset = h]

Short Description: High-level (Z) Threshold Register for Ch4

Long Description:

Return to Summary Table

Table 3-1580. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 8098h
CONTROLSS_SDFM1	5026 9098h

Access Types Legend

Table 3-1581. SDFLT4CMPHZ Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	HLTZ	RW	0h	Unsigned High-level threshold (Z) for the comparator filter output Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt.

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3.22.60 CONTROLSS_SDFMn_SDFIFOCTL4 Registers

3.22.60.1 SDFMn_SDFIFOCTL4 Register (Offset = 9Ah) [reset = h]

Short Description: FIFO Control Register for Ch4

Long Description:

Return to Summary Table

Table 3-1582. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 809Ah
CONTROLSS_SDFM1	5026 909Ah

Access Types Legend

Table 3-1583. SDFIFOCTL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	OVFIEN	RW	0h	SDFIFO Overflow interrupt enable 0: SDFIFO Overflow condition will not generate an interrupt 1: SDFIFO overflow condition generates an interrupt on SDy_ERR
14	DRINTSEL	RW	0h	Data-Ready Interrupt (DRINT) source select 0 = AF1 (Select non-FIFO data-ready interrupt) 1 = SDFFINT1 (Select FIFO data-ready interrupt)
13	FFEN	RW	0h	SDFIFO Enable 0: Disable FIFO operation 1: Enable FIFO operation Note: When FIFO is disabled, FIFO contents are cleared
12	FFIEN	RW	0h	SDFIFO data ready Interrupt Enable
11	RESERVED	RO RRETURNS 0S		Reserved
10 - 6	SDFFST	RO	0h	SDFIFO Status 00000 FIFO empty 00001 FIFO has 1 word . . . . 10000 FIFO has 16 words
5	RESERVED	RO RRETURNS 0S		Reserved
4 - 0	SDFFIL	RW	0h	SDFIFO interrupt level bits The FIFO will generate an interrupt when the FIFO status (SDFFST) '= FIFO level (SDFFIL)

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3.22.61 CONTROLSS_SDFMn_SDSYNC4 Registers

3.22.61.1 SDFMn_SDSYNC4 Register (Offset = 9Ch) [reset = h]

Short Description: SD Filter Sync control for Ch4

Long Description:

Return to Summary Table

Table 3-1584. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 809Ch
CONTROLSS_SDFM1	5026 909Ch

Access Types Legend

Table 3-1585. SDSYNC4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 11	RESERVED	RO RRETURNS 0S		Reserved
10	WTSCLREN	RW	1h	WTSYNFLG Clear-on-FIFOINT Enable 0: WTSYNFLG can only be cleared manually (using WTSYNCLR bit) 1: WTSYNFLG is cleared automatically on SDFFINT
9	FFSYNCCLREN	RW	0h	FIFO Clear-on-SDSYNC Enable 0: SDFIFO is not automaticaly cleared upon receiving SDSYNC 1: SDFIFO is automaticaly cleared upon receiving SDSYNC
8	WTSYNCLR	RW RRETURNS 0S	0h	Wait-for-Sync Flag Clear (always reads 0) 0: Write of 0 has no affect 1: Write of 1 clears WTSYNFLG
7	WTSYNFLG	RO	0h	Wait-for-Sync Flag 0: SDSYNC event has not occurred 1: SDSYNC event occurred.
6	WTSYNCEN	RW	0h	Wait-for-Sync Enable 0: Incoming Data written to SDFIFO on every Data-Ready (DR) Event 1: Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs
5 - 0	SYNCSEL	RW	0h	Defines source for the SDSYNC Input on this channel Refer SDSYNCx.SYNCSEL table

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3.22.62 CONTROLSS_SDFMn_SDFLT4CMPL2 Registers

3.22.62.1 SDFMn_SDFLT4CMPL2 Register (Offset = 9Eh) [reset = h]

Short Description: Second low level threhold for CH4

Long Description:

Return to Summary Table

Table 3-1586. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 809Eh
CONTROLSS_SDFM1	5026 909Eh

Access Types Legend

Table 3-1587. SDFLT4CMPL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO RRETURNS 0S		Reserved
14 - 0	LLT2	RW	0h	Second Unsigned low-level threshold for the comparator filter output.

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3.22.63 CONTROLSS_SDFMn_SDCOMP1CTL Registers

3.22.63.1 SDFMn_SDCOMP1CTL Register (Offset = C0h) [reset = h]

Short Description: SD Comparator event filter1 Control Register

Long Description:

Return to Summary Table

Table 3-1588. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80C0h
CONTROLSS_SDFM1	5026 90C0h

Access Types Legend

Table 3-1589. SDCOMP1CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	RESERVED	RO		Reserved
13 - 12	RESERVED	RO		Reserved
11 - 10	CEVT2DIGFILTSEL	RW	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved
9	RESERVED	RO		Reserved
8	RESERVED	RO		Reserved
7	RESERVED	RO		Reserved
6	RESERVED	RO		Reserved
5 - 4	RESERVED	RO		Reserved
3 - 2	CEVT1DIGFILTSEL	RW	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved
1	RESERVED	RO		Reserved
0	RESERVED	RO		Reserved

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3.22.64 CONTROLSS_SDFMn_SDCOMP1EVT2FLTCTL Registers

3.22.64.1 SDFMn_SDCOMP1EVT2FLTCTL Register (Offset = C2h) [reset = h]

Short Description: COMPL/CEVT2 Digital filter1 Control Register

Long Description:

Return to Summary Table

Table 3-1590. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80C2h
CONTROLSS_SDFM1	5026 90C2h

Access Types Legend

Table 3-1591. SDCOMP1EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8 - 4	SAMPWIN	RW	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

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3.22.65 CONTROLSS_SDFMn_SDCOMP1EVT2FLTCLKCTL Registers

3.22.65.1 SDFMn_SDCOMP1EVT2FLTCLKCTL Register (Offset = C4h) [reset = h]

Short Description: COMPL/CEVT2 Digital filter1 Clock Control Register

Long Description:

Return to Summary Table

Table 3-1592. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80C4h
CONTROLSS_SDFM1	5026 90C4h

Access Types Legend

Table 3-1593. SDCOMP1EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	CLKPRESCALE	RW	0h	Low filter sample clock prescale. Number of system clocks between samples.

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3.22.66 CONTROLSS_SDFMn_SDCOMP1EVT1FLTCTL Registers

3.22.66.1 SDFMn_SDCOMP1EVT1FLTCTL Register (Offset = C6h) [reset = h]

Short Description: COMPH/CEVT1 Digital filter1 Control Register

Long Description:

Return to Summary Table

Table 3-1594. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80C6h
CONTROLSS_SDFM1	5026 90C6h

Access Types Legend

Table 3-1595. SDCOMP1EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8 - 4	SAMPWIN	RW	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

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3.22.67 CONTROLSS_SDFMn_SDCOMP1EVT1FLTCLKCTL Registers

3.22.67.1 SDFMn_SDCOMP1EVT1FLTCLKCTL Register (Offset = C8h) [reset = h]

Short Description: COMPH/CEVT1 Digital filter1 Clock Control Register

Long Description:

Return to Summary Table

Table 3-1596. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80C8h
CONTROLSS_SDFM1	5026 90C8h

Access Types Legend

Table 3-1597. SDCOMP1EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	CLKPRESCALE	RW	0h	High filter sample clock prescale. Number of system clocks between samples.

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3.22.68 CONTROLSS_SDFMn_SDCOMP1LOCK Registers

3.22.68.1 SDFMn_SDCOMP1LOCK Register (Offset = CEh) [reset = h]

Short Description: SD compartor event filter1 Lock Register

Long Description:

Return to Summary Table

Table 3-1598. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80CEh
CONTROLSS_SDFM1	5026 90CEh

Access Types Legend

Table 3-1599. SDCOMP1LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 5	RESERVED	RO		Reserved
4	RESERVED	RO		Reserved
3	COMP	RW SONCE	0h	Lock write-access to the SDCOMP1EVT1/2FLTTCTL and COMP1FILCLKCTL registers. 0 SDCOMP1EVT1/2FLTCTL and SDCOMP1EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP1EVT1/2FLTCTL and SDCOMP1EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit.
2	RESERVED	RO		Reserved
1	RESERVED	RO		Reserved
0	SDCOMP1CTL	RW SONCE	0h	Lock write-access to the SDCOMP1CTL register. 0 SDCOMP1CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP1CTL register is locked. Only a system reset can clear this bit.

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3.22.69 CONTROLSS_SDFMn_SDCOMP2CTL Registers

3.22.69.1 SDFMn_SDCOMP2CTL Register (Offset = D0h) [reset = h]

Short Description: SD Comparator event filter2 Control Register

Long Description:

Return to Summary Table

Table 3-1600. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80D0h
CONTROLSS_SDFM1	5026 90D0h

Access Types Legend

Table 3-1601. SDCOMP2CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	RESERVED	RO		Reserved
13 - 12	RESERVED	RO		Reserved
11 - 10	CEVT2DIGFILTSEL	RW	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved
9	RESERVED	RO		Reserved
8	RESERVED	RO		Reserved
7	RESERVED	RO		Reserved
6	RESERVED	RO		Reserved
5 - 4	RESERVED	RO		Reserved
3 - 2	CEVT1DIGFILTSEL	RW	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved
1	RESERVED	RO		Reserved
0	RESERVED	RO		Reserved

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3.22.70 CONTROLSS_SDFMn_SDCOMP2EVT2FLTCTL Registers

3.22.70.1 SDFMn_SDCOMP2EVT2FLTCTL Register (Offset = D2h) [reset = h]

Short Description: COMPL/CEVT2 Digital filter2 Control Register

Long Description:

Return to Summary Table

Table 3-1602. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80D2h
CONTROLSS_SDFM1	5026 90D2h

Access Types Legend

Table 3-1603. SDCOMP2EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8 - 4	SAMPWIN	RW	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

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3.22.71 CONTROLSS_SDFMn_SDCOMP2EVT2FLTCLKCTL Registers

3.22.71.1 SDFMn_SDCOMP2EVT2FLTCLKCTL Register (Offset = D4h) [reset = h]

Short Description: COMPL/CEVT2 Digital filter2 Clock Control Register

Long Description:

Return to Summary Table

Table 3-1604. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80D4h
CONTROLSS_SDFM1	5026 90D4h

Access Types Legend

Table 3-1605. SDCOMP2EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	CLKPRESCALE	RW	0h	Low filter sample clock prescale. Number of system clocks between samples.

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3.22.72 CONTROLSS_SDFMn_SDCOMP2EVT1FLTCTL Registers

3.22.72.1 SDFMn_SDCOMP2EVT1FLTCTL Register (Offset = D6h) [reset = h]

Short Description: COMPH/CEVT1 Digital filter2 Control Register

Long Description:

Return to Summary Table

Table 3-1606. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80D6h
CONTROLSS_SDFM1	5026 90D6h

Access Types Legend

Table 3-1607. SDCOMP2EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8 - 4	SAMPWIN	RW	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

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3.22.73 CONTROLSS_SDFMn_SDCOMP2EVT1FLTCLKCTL Registers

3.22.73.1 SDFMn_SDCOMP2EVT1FLTCLKCTL Register (Offset = D8h) [reset = h]

Short Description: COMPH/CEVT1 Digital filter2 Clock Control Register

Long Description:

Return to Summary Table

Table 3-1608. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80D8h
CONTROLSS_SDFM1	5026 90D8h

Access Types Legend

Table 3-1609. SDCOMP2EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	CLKPRESCALE	RW	0h	High filter sample clock prescale. Number of system clocks between samples.

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3.22.74 CONTROLSS_SDFMn_SDCOMP2LOCK Registers

3.22.74.1 SDFMn_SDCOMP2LOCK Register (Offset = DEh) [reset = h]

Short Description: SD compartor event filter2 Lock Register

Long Description:

Return to Summary Table

Table 3-1610. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80DEh
CONTROLSS_SDFM1	5026 90DEh

Access Types Legend

Table 3-1611. SDCOMP2LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 5	RESERVED	RO		Reserved
4	RESERVED	RO		Reserved
3	COMP	RW SONCE	0h	Lock write-access to the SDCOMP2EVT1/2FLTTCTL and COMP2FILCLKCTL registers. 0 SDCOMP2EVT1/2FLTCTL and SDCOMP2EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP2EVT1/2FLTCTL and SDCOMP2EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit.
2	RESERVED	RO		Reserved
1	RESERVED	RO		Reserved
0	SDCOMP2CTL	RW SONCE	0h	Lock write-access to the SDCOMP2CTL register. 0 SDCOMP2CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP2CTL register is locked. Only a system reset can clear this bit.

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3.22.75 CONTROLSS_SDFMn_SDCOMP3CTL Registers

3.22.75.1 SDFMn_SDCOMP3CTL Register (Offset = E0h) [reset = h]

Short Description: SD Comparator event filter3 Control Register

Long Description:

Return to Summary Table

Table 3-1612. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80E0h
CONTROLSS_SDFM1	5026 90E0h

Access Types Legend

Table 3-1613. SDCOMP3CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	RESERVED	RO		Reserved
13 - 12	RESERVED	RO		Reserved
11 - 10	CEVT2DIGFILTSEL	RW	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved
9	RESERVED	RO		Reserved
8	RESERVED	RO		Reserved
7	RESERVED	RO		Reserved
6	RESERVED	RO		Reserved
5 - 4	RESERVED	RO		Reserved
3 - 2	CEVT1DIGFILTSEL	RW	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved
1	RESERVED	RO		Reserved
0	RESERVED	RO		Reserved

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3.22.76 CONTROLSS_SDFMn_SDCOMP3EVT2FLTCTL Registers

3.22.76.1 SDFMn_SDCOMP3EVT2FLTCTL Register (Offset = E2h) [reset = h]

Short Description: COMPL/CEVT2 Digital filter3 Control Register

Long Description:

Return to Summary Table

Table 3-1614. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80E2h
CONTROLSS_SDFM1	5026 90E2h

Access Types Legend

Table 3-1615. SDCOMP3EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8 - 4	SAMPWIN	RW	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

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3.22.77 CONTROLSS_SDFMn_SDCOMP3EVT2FLTCLKCTL Registers

3.22.77.1 SDFMn_SDCOMP3EVT2FLTCLKCTL Register (Offset = E4h) [reset = h]

Short Description: COMPL/CEVT2 Digital filter3 Clock Control Register

Long Description:

Return to Summary Table

Table 3-1616. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80E4h
CONTROLSS_SDFM1	5026 90E4h

Access Types Legend

Table 3-1617. SDCOMP3EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	CLKPRESCALE	RW	0h	Low filter sample clock prescale. Number of system clocks between samples.

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3.22.78 CONTROLSS_SDFMn_SDCOMP3EVT1FLTCTL Registers

3.22.78.1 SDFMn_SDCOMP3EVT1FLTCTL Register (Offset = E6h) [reset = h]

Short Description: COMPH/CEVT1 Digital filter3 Control Register

Long Description:

Return to Summary Table

Table 3-1618. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80E6h
CONTROLSS_SDFM1	5026 90E6h

Access Types Legend

Table 3-1619. SDCOMP3EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8 - 4	SAMPWIN	RW	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

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3.22.79 CONTROLSS_SDFMn_SDCOMP3EVT1FLTCLKCTL Registers

3.22.79.1 SDFMn_SDCOMP3EVT1FLTCLKCTL Register (Offset = E8h) [reset = h]

Short Description: COMPH/CEVT1 Digital filter3 Clock Control Register

Long Description:

Return to Summary Table

Table 3-1620. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80E8h
CONTROLSS_SDFM1	5026 90E8h

Access Types Legend

Table 3-1621. SDCOMP3EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	CLKPRESCALE	RW	0h	High filter sample clock prescale. Number of system clocks between samples.

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3.22.80 CONTROLSS_SDFMn_SDCOMP3LOCK Registers

3.22.80.1 SDFMn_SDCOMP3LOCK Register (Offset = EEh) [reset = h]

Short Description: SD compartor event filter3 Lock Register

Long Description:

Return to Summary Table

Table 3-1622. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80EEh
CONTROLSS_SDFM1	5026 90EEh

Access Types Legend

Table 3-1623. SDCOMP3LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 5	RESERVED	RO		Reserved
4	RESERVED	RO		Reserved
3	COMP	RW SONCE	0h	Lock write-access to the SDCOMP3EVT1/2FLTTCTL and COMP3FILCLKCTL registers. 0 SDCOMP3EVT1/2FLTCTL and SDCOMP3EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP3EVT1/2FLTCTL and SDCOMP3EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit.
2	RESERVED	RO		Reserved
1	RESERVED	RO		Reserved
0	SDCOMP3CTL	RW SONCE	0h	Lock write-access to the SDCOMP3CTL register. 0 SDCOMP3CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP3CTL register is locked. Only a system reset can clear this bit.

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3.22.81 CONTROLSS_SDFMn_SDCOMP4CTL Registers

3.22.81.1 SDFMn_SDCOMP4CTL Register (Offset = F0h) [reset = h]

Short Description: SD Comparator event filter4 Control Register

Long Description:

Return to Summary Table

Table 3-1624. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80F0h
CONTROLSS_SDFM1	5026 90F0h

Access Types Legend

Table 3-1625. SDCOMP4CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	RO		Reserved
14	RESERVED	RO		Reserved
13 - 12	RESERVED	RO		Reserved
11 - 10	CEVT2DIGFILTSEL	RW	0h	High comparator COMPH source select. 0 CEVT2 output drives COMPLOUT 1 Reserved 2 Output of digital filter drives COMPLOUT 3 Reserved
9	RESERVED	RO		Reserved
8	RESERVED	RO		Reserved
7	RESERVED	RO		Reserved
6	RESERVED	RO		Reserved
5 - 4	RESERVED	RO		Reserved
3 - 2	CEVT1DIGFILTSEL	RW	0h	High comparator COMPH source select. 0 CEVT1 output drives COMPHOUT 1 Reserved 2 Output of digital filter drives COMPHOUT 3 Reserved
1	RESERVED	RO		Reserved
0	RESERVED	RO		Reserved

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3.22.82 CONTROLSS_SDFMn_SDCOMP4EVT2FLTCTL Registers

3.22.82.1 SDFMn_SDCOMP4EVT2FLTCTL Register (Offset = F2h) [reset = h]

Short Description: COMPL/CEVT2 Digital filter4 Control Register

Long Description:

Return to Summary Table

Table 3-1626. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80F2h
CONTROLSS_SDFM1	5026 90F2h

Access Types Legend

Table 3-1627. SDCOMP4EVT2FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	Low filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8 - 4	SAMPWIN	RW	0h	Low filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

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3.22.83 CONTROLSS_SDFMn_SDCOMP4EVT2FLTCLKCTL Registers

3.22.83.1 SDFMn_SDCOMP4EVT2FLTCLKCTL Register (Offset = F4h) [reset = h]

Short Description: COMPL/CEVT2 Digital filter4 Clock Control Register

Long Description:

Return to Summary Table

Table 3-1628. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80F4h
CONTROLSS_SDFM1	5026 90F4h

Access Types Legend

Table 3-1629. SDCOMP4EVT2FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	CLKPRESCALE	RW	0h	Low filter sample clock prescale. Number of system clocks between samples.

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3.22.84 CONTROLSS_SDFMn_SDCOMP4EVT1FLTCTL Registers

3.22.84.1 SDFMn_SDCOMP4EVT1FLTCTL Register (Offset = F6h) [reset = h]

Short Description: COMPH/CEVT1 Digital filter4 Control Register

Long Description:

Return to Summary Table

Table 3-1630. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80F6h
CONTROLSS_SDFM1	5026 90F6h

Access Types Legend

Table 3-1631. SDCOMP4EVT1FLTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FILINIT	RW RRETURNS 0S	0h	High filter initialization. 0 No effect 1 Initialize all samples to the filter input value
14	RESERVED	RO		Reserved
13 - 9	THRESH	RW	0h	High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state.
8 - 4	SAMPWIN	RW	0h	High filter sample window size. Number of samples to monitor is SAMPWIN+1.
3 - 0	RESERVED	RO		Reserved

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3.22.85 CONTROLSS_SDFMn_SDCOMP4EVT1FLTCLKCTL Registers

3.22.85.1 SDFMn_SDCOMP4EVT1FLTCLKCTL Register (Offset = F8h) [reset = h]

Short Description: COMPH/CEVT1 Digital filter4 Clock Control Register

Long Description:

Return to Summary Table

Table 3-1632. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80F8h
CONTROLSS_SDFM1	5026 90F8h

Access Types Legend

Table 3-1633. SDCOMP4EVT1FLTCLKCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 10	RESERVED	RO		Reserved
9 - 0	CLKPRESCALE	RW	0h	High filter sample clock prescale. Number of system clocks between samples.

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3.22.86 CONTROLSS_SDFMn_SDCOMP4LOCK Registers

3.22.86.1 SDFMn_SDCOMP4LOCK Register (Offset = FEh) [reset = h]

Short Description: SD compartor event filter4 Lock Register

Long Description:

Return to Summary Table

Table 3-1634. Instance Table

Instance Name	Physical Address
CONTROLSS_SDFM0	5026 80FEh
CONTROLSS_SDFM1	5026 90FEh

Access Types Legend

Table 3-1635. SDCOMP4LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 5	RESERVED	RO		Reserved
4	RESERVED	RO		Reserved
3	COMP	RW SONCE	0h	Lock write-access to the SDCOMP4EVT1/2FLTTCTL and COMP4FILCLKCTL registers. 0 SDCOMP4EVT1/2FLTCTL and SDCOMP4EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect. 1 SDCOMP4EVT1/2FLTCTL and SDCOMP4EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit.
2	RESERVED	RO		Reserved
1	RESERVED	RO		Reserved
0	SDCOMP4CTL	RW SONCE	0h	Lock write-access to the SDCOMP4CTL register. 0 SDCOMP4CTL register is not locked. Write 0 to this bit has no effect. 1 SDCOMP4CTL register is locked. Only a system reset can clear this bit.

3.22.87 Access Table

Table 3-1636. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RO RRETURNS0S	RO RRETURNS0S	Read returns 0s
RW RRETURNS0S	RW RRETURNS0S	Read returns 0s/Write
RW	RW	Read / Write
RW SONCE	RW SONCE	Read/Write (Set Once)

3.23 TSXBAR_INTR Registers

Table 3-1637. SOC_TIMESYNC_XBAR0_TSXBAR_INTR Registers Base Address Table

Offset	Length	Acronym	SOC_TIMESYNC_XBAR0_TSXBAR_INTR Physical Address
0h	32	TSXBAR_INTR_PID	52E0 0000h
4h	16	TSXBAR_INTR_MUXCNTL	52E0 0004h

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3.23.1 SOC_TIMESYNC_XBAR0_TSXBAR_INTR_PID Registers

3.23.1.1 SOC_TIMESYNC_XBAR0_TSXBAR_INTR_PID Register (Offset = 0h) [reset = h]

Short Description: Identification register

Long Description:

Return to Summary Table

Table 3-1638. Instance Table

Instance Name	Physical Address
SOC_TIMESYNC_XBAR0	52E0 0000h

Access Types Legend

Table 3-1639. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	scheme
29 - 28	BU	RO	2h	bu
27 - 16	FUNCTION	RO	694h	function
15 - 11	RTLVER	RO	10h	rtl version
10 - 8	MAJREV	RO	1h	major version
7 - 6	CUSTOM	RO	0h	custom id
5 - 0	MINREV	RO	0h	minor version

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3.23.2 SOC_TIMESYNC_XBAR0_TSXBAR_INTR_MUXCNTL Registers

3.23.2.1 SOC_TIMESYNC_XBAR0_TSXBAR_INTR_MUXCNTL Register (Offset = 4h) [reset = h]

Short Description: Interrupt mux control register

Long Description:

Return to Summary Table

Table 3-1640. Instance Table

Instance Name	Physical Address
SOC_TIMESYNC_XBAR0	52E0 0004h

Access Types Legend

Table 3-1641. MUXCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
16	INT_ENABLE	RW	0h	interrupt output enable for interrupt N
	RESERVED	NONE		Reserved
4 - 0	ENABLE	RW	0h	Mux control for interrupt N

3.23.3 Access Table

Table 3-1642. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

4 System-on-chip (SoC) Registers

The System-on-chip (SoC) module registers are described in the following sections.

4.1 EXT_FLASH Registers

Table 4-1. EXT_FLASH[0:1] Registers Base Address Table

Offset	Length	Acronym	EXT_FLASH0 Physical Address	EXT_FLASH1 Physical Address
0h	32	EXT_FLASH_EXT_FLASH_START	6000 0000h	6200 0000h
1FFFFFCh	32	EXT_FLASH_EXT_FLASH_END	61FF FFFCh	63FF FFFCh

4.1.1 EXT_FLASH Instance Count Note

Note

n = 0 to 1 for the EXT_FLASH registers defined below.

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4.1.2 EXT_FLASHn_START Registers

4.1.2.1 EXT_FLASHn_START Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 4-2. Instance Table

Instance Name	Physical Address
EXT_FLASH0	6000 0000h
EXT_FLASH1	6200 0000h

Access Types Legend

Table 4-3. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MEM_START	RW	0h	External flash start Address

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4.1.3 EXT_FLASHn_END Registers

4.1.3.1 EXT_FLASHn_END Register (Offset = 1FFFFFCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 4-4. Instance Table

Instance Name	Physical Address
EXT_FLASH0	61FF FFFCh
EXT_FLASH1	63FF FFFCh

Access Types Legend

Table 4-5. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MEM_END	RW	0h	External flash end address

4.1.4 Access Table

Table 4-6. Access Type Codes

Access Type	Code	Description
RW	RW	Read / Write

4.2 EDMA_TRIGXBAR_INTR Registers

Table 4-7. EDMA_TRIGXBAR_INTR Registers Base Address Table

Offset	Length	Acronym	EDMA_TRIGXBAR_INTR Physical Address
0h	32	EDMA_TRIGXBAR_INTR_PID	52E0 1000h
4h	16	EDMA_TRIGXBAR_INTR_MUXCNTL	52E0 1004h

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4.2.1 EDMA_TRIGXBAR_INTR_PID Registers

4.2.1.1 EDMA_TRIGXBAR_INTR_PID Register (Offset = 0h) [reset = h]

Short Description: Identification register

Long Description:

Return to Summary Table

Table 4-8. Instance Table

Instance Name	Physical Address
EDMA_TRIG_XBAR	52E0 1000h

Access Types Legend

Table 4-9. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	scheme
29 - 28	BU	RO	2h	bu
27 - 16	FUNCTION	RO	694h	function
15 - 11	RTLVER	RO	10h	rtl version
10 - 8	MAJREV	RO	1h	major version
7 - 6	CUSTOM	RO	0h	custom id
5 - 0	MINREV	RO	0h	minor version

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4.2.2 EDMA_TRIGXBAR_INTR_MUXCNTL Registers

4.2.2.1 EDMA_TRIGXBAR_INTR_MUXCNTL Register (Offset = 4h) [reset = h]

Short Description: Interrupt mux control register

Long Description:

Return to Summary Table

Table 4-10. Instance Table

Instance Name	Physical Address
EDMA_TRIG_XBAR	52E0 1004h

Access Types Legend

Table 4-11. MUXCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
16	INT_ENABLE	R/W	0h	interrupt output enable for interrupt N
	RESERVED	NONE		Reserved
7 - 0	ENABLE	R/W	0h	Mux control for interrupt N

4.2.3 Access Table

Table 4-12. Access Type Codes

Access Type	Code	Description
RO	RO	Read
R/W	R/W	Read/Write

4.3 GPIO_XBAR_INTR Registers

Table 4-13. GPIO_XBAR_INTR Registers Base Address Table

Offset	Length	Acronym	GPIO_XBAR_INTR Physical Address
0h	32	GPIO_XBAR_INTR_PID	52E0 2000h
4h	16	GPIO_XBAR_INTR_MUXCNTL	52E0 2004h

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4.3.1 GPIO_XBAR_INTR_PID Registers

4.3.1.1 GPIO_XBAR_INTR_PID Register (Offset = 0h) [reset = h]

Short Description: Identification register

Long Description:

Return to Summary Table

Table 4-14. Instance Table

Instance Name	Physical Address
GPIO_INTR_XBAR	52E0 2000h

Access Types Legend

Table 4-15. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	scheme
29 - 28	BU	RO	2h	bu
27 - 16	FUNCTION	RO	694h	function
15 - 11	RTLVER	RO	10h	rtl version
10 - 8	MAJREV	RO	1h	major version
7 - 6	CUSTOM	RO	0h	custom id
5 - 0	MINREV	RO	0h	minor version

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4.3.2 GPIO_XBAR_INTR_MUXCNTL Registers

4.3.2.1 GPIO_XBAR_INTR_MUXCNTL Register (Offset = 4h) [reset = h]

Short Description: Interrupt mux control register

Long Description:

Return to Summary Table

Table 4-16. Instance Table

Instance Name	Physical Address
GPIO_INTR_XBAR	52E0 2004h

Access Types Legend

Table 4-17. MUXCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
16	INT_ENABLE	RW	0h	interrupt output enable for interrupt N
	RESERVED	NONE		Reserved
7 - 0	ENABLE	RW	0h	Mux control for interrupt N

4.3.3 Access Table

Table 4-18. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

4.4 PRU_ICSS_XBAR_INTR Registers

Table 4-19. PRU_ICSS_XBAR_INTR Registers Base Address Table

Offset	Length	Acronym	PRU_ICSS_XBAR_INTR Physical Address
0h	32	ICSSM_XBAR_INTR_PID	52E0 3000h
4h	16	ICSSM_XBAR_INTR_MUXCNTL	52E0 3004h

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4.4.1 ICSSM_XBAR_INTR_PID Registers

4.4.1.1 ICSSM_XBAR_INTR_PID Register (Offset = 0h) [reset = h]

Short Description: Identification register

Long Description:

Return to Summary Table

Table 4-20. Instance Table

Instance Name	Physical Address
ICSSM_INTR_XBAR	52E0 3000h

Access Types Legend

Table 4-21. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	scheme
29 - 28	BU	RO	2h	bu
27 - 16	FUNCTION	RO	694h	function
15 - 11	RTLVER	RO	10h	rtl version
10 - 8	MAJREV	RO	1h	major version
7 - 6	CUSTOM	RO	0h	custom id
5 - 0	MINREV	RO	0h	minor version

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4.4.2 ICSSM_XBAR_INTR_MUXCNTL Registers

4.4.2.1 ICSSM_XBAR_INTR_MUXCNTL Register (Offset = 4h) [reset = h]

Short Description: Interrupt mux control register

Long Description:

Return to Summary Table

Table 4-22. Instance Table

Instance Name	Physical Address
ICSSM_INTR_XBAR	52E0 3004h

Access Types Legend

Table 4-23. MUXCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
16	INT_ENABLE	RW	0h	interrupt output enable for interrupt N
	RESERVED	NONE		Reserved
5 - 0	ENABLE	RW	0h	Mux control for interrupt N

4.4.3 Access Table

Table 4-24. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

4.5 PRU-ICSS Registers

4.5.1 PRU_ICSS_CFG Registers

PRU_ICSS_CFG Registers lists the memory-mapped registers for the PRU-ICSS subsystem. All register offset addresses not listed in PRU_ICSS_CFG Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-25. PRU_ICSS_CFG Instances

Instance	Base Address
PRU_ICSS_CFG	4802 6000h

Table 4-26. PRU_ICSS_CFG Registers

Offset	Acronym	Register Name	PRU_ICSS_CFG Physical Address
0h	PRU_ICSS_REVID	Revision Register	4802 6000h
4h	RESERVED		4802 6004h
8h	PRU_ICSS_GPCFG0	General Purpose Configuration 0 Register	4802 6008h
Ch	PRU_ICSS_GPCFG1	General Purpose Configuration 1 Register	4802 600Ch
10h	PRU_ICSS_CGR	Clock Gating Register	4802 6010h
14h	RESERVED		4802 6014h
28h	PRU_ICSS_PMAO	PRU Master Address Offset Register	4802 6028h
2Ch	PRU_ICSS_MII_RT	MII_RT Event Enable Register	4802 602Ch
30h	PRU_ICSS_IEPCLK	IEP Clock Source Register defines the source of the IEP clock.	4802 6030h
34h	PRU_ICSS_SPP	Scratch Pad Priority and Configuration Register	4802 6034h
40h	PRU_ICSS_PIN_MX	Pin Mux Select Register	4802 6040h

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4.5.1.1 PRU_ICSS_REVID Register (Offset = 0h) [reset = 47000A02h]

PRU_ICSS_REVID is shown in Figure 4-1 and described in Table 4-28.

The Revision Register contains the ID and revision information.

Table 4-27. PRU_ICSS_REVID Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 6000h

Figure 4-1. PRU_ICSS_REVID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															
R-6B080203 h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-28. PRU_ICSS_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REVISION	R	6B080203h	TI internal data. Identifies revision of peripheral.

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4.5.1.2 PRU_ICSS_GPCFG0 Register (Offset = 8h) [reset = 0h]

PRU_ICSS_GPCFG0 is shown in Figure 4-2 and described in Table 4-30.

The General Purpose Configuration 0 Register defines the GPI/O configuration for PRU0.

Table 4-29. PRU_ICSS_GPCFG0 Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 6008h

Figure 4-2. PRU_ICSS_GPCFG0 Register

31	30	29	28	27	26	25	24
RESERVED		PR0_PRU0_GP_MUX_SEL				PRU0_GPO_SH_SEL	PRU0_GPO_DIV1
R-0h		R/W-0h				R-0h	R/W-0h
23	22	21	20	19	18	17	16
PRU0_GPO_DIV1				PRU0_GPO_DIV0			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
PRU0_GPO_DIV0	PRU0_GPO_MODE	PRU0_GPI_SB	PRU0_GPI_DIV1				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
PRU0_GPI_DIV0					PRU0_GPI_CLK_MODE	PRU0_GPI_MODE	
R/W-0h					R/W-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-30. PRU_ICSS_GPCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-26	PR0_PRU0_GP_MUX_SEL	R/W	0h	Controls the PRU-ICSS wrap mux selection. 0h: GP selected 1h: ENDAT (Peripheral Interface) 2h: MII mode 3h: SD mode 4h: Reserved
25	PRU0_GPO_SH_SEL	R	0h	Defines which shadow register is currently getting used for GPO shifting. 0h: gpo_sh0 is selected 1h: gpo_sh1 is selected
24-20	PRU0_GPO_DIV1	R/W	0h	Divisor value (divide by PRU0_GPO_DIV1 + 1). 0h: Div 1.0 1h: Div 1.5 2h: Div 2.0 .. 1Eh: Div 16.0 1Fh: Reserved

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Table 4-30. PRU_ICSS_GPCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-15	PRU0_GPO_DIV0	R/W	0h	Divisor value (divide by PRU0_GPO_DIV0 + 1). 0h: Div 1.0 1h: Div 1.5 2h: Div 2.0 .. 1Eh: Div 16.0 1Fh: Reserved
14	PRU0_GPO_MODE	R/W	0h	PRU GPO (R30) modes: 0h: Direct output mode 1h: Serial output mode
13	PRU0_GPI_SB	R/W	0h	Start Bit event for 28-bit shift mode. PRU0_GPI_SB (pru0_r31_status[29]) is set when first capture of a 1 on pru0_r31_status[0]. Read 0h: Start Bit event has not occurred. Read 1h: Start Bit event occurred. Write 0h: No Effect. Write 1h: Will clear PRU0_GPI_SB and clear the whole shift register.
12-8	PRU0_GPI_DIV1	R/W	0h	Divisor value (divide by PRU0_GPI_DIV1 + 1). 0h: Div 1.0 1h: Div 1.5 2h: Div 2.0 .. 1Eh: Div 16.0 1Fh: Reserved
7-3	PRU0_GPI_DIV0	R/W	0h	Divisor value (divide by PRU0_GPI_DIV0 + 1). 0h: Div 1.0 1h: Div 1.5 2h: Div 2.0 .. 1Eh: Div 16.0 1Fh: Reserved
2	PRU0_GPI_CLK_MODE	R/W	0h	Parallel 16-bit capture mode clock edge. 0h: Use the positive edge of pru0_r31_status[16] 1h: Use the negative edge of pru0_r31_status[16]
1-0	PRU0_GPI_MODE	R/W	0h	PRU GPI (R31) modes: 0h: Direct input mode 1h: 16-bit parallel capture mode 2h: 28-bit shift mode 3h: MII_RT mode

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4.5.1.3 PRU_ICSS_GPCFG1 Register (Offset = Ch) [reset = 0h]

PRU_ICSS_GPCFG1 is shown in Figure 4-3 and described in Table 4-32.

The General Purpose Configuration 1 Register defines the GPI/O configuration for PRU1.

Table 4-31. PRU_ICSS_GPCFG1 Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 600Ch

Figure 4-3. PRU_ICSS_GPCFG1 Register

31	30	29	28	27	26	25	24
RESERVED		PR0_PRU1_GP_MUX_SEL				PRU1_GPO_SH_SEL	PRU1_GPO_DIV1
R-0h		R/W-0h				R-0h	R/W-0h
23	22	21	20	19	18	17	16
PRU1_GPO_DIV1				PRU1_GPO_DIV0			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
PRU1_GPO_DIV0	PRU1_GPO_MODE	PRU1_GPI_SB	PRU1_GPI_DIV1				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				
7	6	5	4	3	2	1	0
PRU1_GPI_DIV0					PRU1_GPI_CLK_MODE	PRU1_GPI_MODE	
R/W-0h					R/W-0h	R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-32. PRU_ICSS_GPCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-26	PR0_PRU1_GP_MUX_SEL	R/W	0h	Controls the PRU-ICSS wrap mux selection. 0h: GP selected 1h: ENDAT (Peripheral Interface) 2h: MII mode 3h: SD mode 4h: Reserved
25	PRU1_GPO_SH_SEL	R	0h	Defines which shadow register is currently getting used for GPO shifting. 0h = gpo_sh0 is selected 1h = gpo_sh1 is selected
24-20	PRU1_GPO_DIV1	R/W	0h	Divisor value (divide by PRU1_GPO_DIV1 + 1). 0h: Div 1.0 1h: Div 1.5 2h: Div 2.0 .. 1Eh: Div 16.0 1Fh: Reserved

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Table 4-32. PRU_ICSS_GPCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-15	PRU1_GPO_DIV0	R/W	0h	Divisor value (divide by PRU1_GPO_DIV0 + 1). 0h: Div 1.0 1h: Div 1.5 2h: Div 2.0 .. 1Eh: Div 16.0 1Fh: Reserved
14	PRU1_GPO_MODE	R/W	0h	PRU GPO (R30) modes: 0h: Direct output mode 1h: Serial output mode
13	PRU1_GPI_SB	R/W	0h	28-bit shift mode Start Bit event. PRU1_GPI_SB (pru1_r31_status[29]) is set when first capture of a 1 on pru1_r31_status[0]. Read 0: Start Bit event has not occurred. Read 1: Start Bit event occurred. Write 0: No Effect. Write 1: Will clear PRU1_GPI_SB and clear the whole shift register.
12-8	PRU1_GPI_DIV1	R/W	0h	Divisor value (divide by PRU1_GPI_DIV1 + 1). 0h: Div 1.0 1h: Div 1.5 2h: Div 2.0 .. 1Eh: Div 16.0 1Fh: Reserved
7-3	PRU1_GPI_DIV0	R/W	0h	Divisor value (divide by PRU1_GPI_DIV0 + 1). 0h: Div 1.0 1h: Div 1.5 2h: Div 2.0 .. 1Eh: Div 16.0 1Fh: Reserved
2	PRU1_GPI_CLK_MODE	R/W	0h	Parallel 16-bit capture mode clock edge. 0h: Use the positive edge of pru1_r31_status[16] 1h: Use the negative edge of pru1_r31_status[16]
1-0	PRU1_GPI_MODE	R/W	0h	PRU GPI (R31) modes: 0h: Direct input mode 1h: 16-bit parallel capture mode 2h: 28-bit shift mode 3h: MII_RT mode

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4.5.1.4 PRU_ICSS_CGR Register (Offset = 10h) [reset = 00024924h]

PRU_ICSS_CGR is shown in Figure 4-4 and described in Table 4-34.

The Clock Gating Register controls the state of Clock Management of the different modules. Software should not clear PRU_ICSS_CLK_EN until PRU_ICSS_CLK_STOP_ACK is 1h.

Table 4-33. PRU_ICSS_CGR Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 6010h

Figure 4-4. PRU_ICSS_CGR Register

31	30	29	28	27	26	25	24
ICSS_STOP_ACK	ICSS_STOP_REQ	RESERVED					
R/W-0h	R-0h	R-0h					
23	22	21	20	19	18	17	16
RESERVED						IEP_CLK_EN	IEP_CLK_STOP_ACK
R-0h						R/W-1h	R-0h
15	14	13	12	11	10	9	8
IEP_CLK_STOP_REQ	ECAP_CLK_EN	ECAP_CLK_STOP_ACK	ECAP_CLK_STOP_REQ	UART_CLK_EN	UART_CLK_STOP_ACK	UART_CLK_STOP_REQ	PRU_ICSS_INTC_CLK_EN
R/W-0h	R/W-1h	R-0h	R/W-0h	R/W-1h	R-0h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
PRU_ICSS_INTC_CLK_STOP_ACK	PRU_ICSS_INTC_CLK_STOP_REQ	PRU1_CLK_EN	PRU1_CLK_STOP_ACK	PRU1_CLK_STOP_REQ	PRU0_CLK_EN	PRU0_CLK_STOP_ACK	PRU0_CLK_STOP_REQ
R-0h	R/W-0h	R/W-1h	R-0h	R/W-0h	R/W-1h	R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-34. PRU_ICSS_CGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ICSS_STOP_ACK	R/W	0h	Acknowledgement that ICSS clock can be stopped. 0h: Not Ready to Gate Clock 1h: Ready to Gate Clock
30	ICSS_STOP_REQ	R	0h	ICSS request to stop clock. 0h: No Gate Clock Request 1h: Gate Clock Request
29-18	RESERVED	R	0h	Reserved
17	IEP_CLK_EN	R/W	1h	IEP clock enable. 0h: Disable Clock 1h: Enable Clock
16	IEP_CLK_STOP_ACK	R	0h	Acknowledgement that IEP clock can be stopped. 0h: Not Ready to Gate Clock 1h: Ready to Gate Clock
15	IEP_CLK_STOP_REQ	R/W	0h	IEP request to stop clock. 0h: Do not request to stop Clock 1h: Request to stop Clock
14	ECAP_CLK_EN	R/W	1h	ECAP clock enable. 0h: Disable Clock 1h: Enable Clock

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Table 4-34. PRU_ICSS_CGR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	ECAP_CLK_STOP_ACK	R	0h	Acknowledgement that ECAP clock can be stopped. 0h: Not Ready to Gate Clock 1h: Ready to Gate Clock
12	ECAP_CLK_STOP_REQ	R/W	0h	ECAP request to stop clock. 0h: Do not request to stop Clock 1h: Request to stop Clock
11	UART_CLK_EN	R/W	1h	UART clock enable. 0h: Disable Clock 1h: Enable Clock
10	UART_CLK_STOP_ACK	R	0h	Acknowledgement that UART clock can be stopped. 0h: Not Ready to Gate Clock 1h: Ready to Gate Clock
9	UART_CLK_STOP_REQ	R/W	0h	UART request to stop clock. 0h: Do not request to stop Clock 1h: Request to stop Clock
8	PRU_ICSS_INTC_CLK_EN	R/W	1h	PRU_ICSS_INTC clock enable. 0h: Disable Clock 1h: Enable Clock
7	PRU_ICSS_INTC_CLK_STOP_ACK	R	0h	Acknowledgement that PRU_ICSS_INTC clock can be stopped. 0h: Not Ready to Gate Clock 1h: Ready to Gate Clock
6	PRU_ICSS_INTC_CLK_STOP_REQ	R/W	0h	PRU_ICSS_INTC request to stop clock. 0h: Do not request to stop Clock 1h: Request to stop Clock
5	PRU1_CLK_EN	R/W	1h	PRU1 clock enable. 0h: Disable Clock 1h: Enable Clock
4	PRU1_CLK_STOP_ACK	R	0h	Acknowledgement that PRU1 clock can be stopped. 0h: Not Ready to Gate Clock 1h: Ready to Gate Clock
3	PRU1_CLK_STOP_REQ	R/W	0h	PRU1 request to stop clock. 0h: Do not request to stop Clock 1h: Request to stop Clock
2	PRU0_CLK_EN	R/W	1h	PRU0 clock enable. 0h: Disable Clock 1h: Enable Clock
1	PRU0_CLK_STOP_ACK	R	0h	Acknowledgement that PRU0 clock can be stopped. 0h: Not Ready to Gate Clock 1h: Ready to Gate Clock
0	PRU0_CLK_STOP_REQ	R/W	0h	PRU0 request to stop clock. 0h: Do not request to stop Clock 1h: Request to stop Clock

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4.5.1.5 PRU_ICSS_PMAO Register (Offset = 28h) [reset = 0h]

PRU_ICSS_PMAO is shown in Table 4-35 and described in Table 4-36.

The PRU Master Address Offset Register enables for the PRU Master Port Address to have an offset of minus 0008_0000h. This enables the PRU to access External Host address space starting at 0000_0000h.

Table 4-35. PRU_ICSS_PMAO Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 6028h

Figure 4-5. PRU_ICSS_PMAO Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						PMAO_PRU1	PMAO_PRU0
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-36. PRU_ICSS_PMAO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	PMAO_PRU1	R/W	0h	PRU1 Master Port Address Offset Enable. 0h: Disable address offset. 1h: Enable address offset of -0008_0000h.
0	PMAO_PRU0	R/W	0h	PRU0 Master Port Address Offset Enable. 0h: Disable address offset. 1h: Enable address offset of -0008_0000h.

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4.5.1.6 PRU_ICSS_MII_RT Register (Offset = 2Ch) [reset = 1h]

PRU_ICSS_MII_RT is shown in Figure 4-6 and described in Table 4-38.

The MII_RT Event Enable Register enables MII_RT mode events to the PRU-ICSS_INTC.

Table 4-37. PRU_ICSS_MII_RT Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 602Ch

Figure 4-6. PRU_ICSS_MII_RT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							MII_RT_EVENT_EN
R-0h							R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-38. PRU_ICSS_MII_RT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MII_RT_EVENT_EN	R/W	1h	Enables the MII_RT Events to the PRU-ICSS_INTC. 0h: Disabled (use external events). 1h: Enabled (use MII_RT events).

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4.5.1.7 PRU_ICSS_IEPCLK Register (Offset = 30h) [reset = 0h]

PRU_ICSS_IEPCLK is shown in Figure 4-7 and described in Table 4-40.

The IEP Clock Source Register defines the source of the IEP clock.

Table 4-39. PRU_ICSS_IEPCLK Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 6030h

Figure 4-7. PRU_ICSS_IEPCLK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							OCP_EN
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-40. PRU_ICSS_IEPCLK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	OCP_EN	R/W	0h	IEP clock source. 0h: ICSS_IEP_CLK is the source 1h: ICSS_VCLK_CLK is the source. While this is selected no transactions should be active. It can only be cleared by a hardware reset.

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4.5.1.8 PRU_ICSS_SPP Register (Offset = 34h) [reset = 0h]

PRU_ICSS_SPP is shown in Figure 4-8 and described in Table 4-42.

The Scratch Pad Priority and Configuration Register defines the access priority assigned to the PRU cores and configures the scratch pad XFR shift functionality.

Table 4-41. PRU_ICSS_SPP Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 6034h

Figure 4-8. PRU_ICSS_SPP Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						XFR_SHIFT_EN	PRU1_PAD_HP_EN
R-0h						R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-42. PRU_ICSS_SPP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	XFR_SHIFT_EN	R/W	0h	Enables XIN XOUT shift functionality. When enabled, R0[4-0] (internal to PRU) defines the 32-bit offset for XIN and XOUT operations with the scratch pad. 0h: Disabled. 1h: Enabled.
0	PRU1_PAD_HP_EN	R/W	0h	Defines which PRU wins write cycle arbitration to a common scratch pad bank. The PRU which has higher priority will always perform the write cycle with no wait states. The lower PRU will get stalled wait states until higher PRU is not performing write cycles. If the lower priority PRU writes to the same byte has the higher priority PRU, then the lower priority PRU will over write the bytes. 0h: PRU0 has highest priority. 1h: PRU1 has highest priority.

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4.5.1.9 PRU_ICSS_PIN_MX Register (Offset = 40h) [reset = 0h]

PRU_ICSS_PIN_MX is shown in Figure 4-9 and described in Table 4-44.

The Pin Mux Select Register defines the state of the PRU-ICSS internal pinmuxing.

Table 4-43. PRU_ICSS_PIN_MX Instances

Instance	Physical Address
PRU_ICSS_CFG	4802 6040h

Figure 4-9. PRU_ICSS_PIN_MX Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				PWM3_REMAP_EN		PWM0_REMAP_EN	
R-0h				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-44. PRU_ICSS_PIN_MX Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved. Always write 0.
11-10	PWM3_REMAP_EN	R/W	0h	Remaps the eHRPWM3_SYNCI to a PRU-ICSS Host Interrupt. This bit field is only controlled by PRU-ICSS_0. If enabled, PRU-ICSS Host Interrupt 7 controls eHRPWM3_SYNCI. See for more details about eHRPWM3_SYNCI signal. 0h: Disabled 1h: PRU-ICSS_0 Host Interrupt 7 controls eHRPWM3_SYNCI 2h: PRU-ICSS_1 Host Interrupt 7 controls eHRPWM3_SYNCI 3h: Reserved
9-8	PWM0_REMAP_EN	R/W	0h	Remaps the eHRPWM0_SYNCI to a PRU-ICSS Host Interrupt. This bit field is only controlled by PRU-ICSS_0. If enabled, PRU-ICSS Host Interrupt 6 controls eHRPWM0_SYNCI. See for more details about eHRPWM0_SYNCI signal. 0h: Disabled 1h: PRU-ICSS_0 Host Interrupt 6 controls eHRPWM0_SYNCI 2h: PRU-ICSS_1 Host Interrupt 6 controls eHRPWM0_SYNCI 3h: Reserved
7-0	RESERVED	R	0h	Reserved.

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4.5.2 PRU_ICSS_ECC_CFG Registers

PRU_ICSS_ECC_CFG Registers lists the memory-mapped registers for the PRU_ICSS_ECC_CFG. All register offset addresses not listed in PRU_ICSS_ECC_CFG Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-45. PRU_ICSS_ECC_CFG Instances

Module Name	Base Address
PRU_ICSS_ECC_CFG	5802 7000h

Table 4-46. PRU_ICSS_ECC_CFG Registers

Offset	Acronym	Register Name	PRU_ICSS_ECC_CFG Physical Address
0h	ECC_REVISION	The Revision Register contains the ID and revision information for the ECC Aggregator module. It does not support byte access.	4802 7000h
8h	ECC_VECTOR	ECC RAM ID to select the ECC RAM to control or read status.	4802 7008h
Ch	ECC_MISC_STATUS	Miscellaneous status register.	4802 700Ch
10h	ECC_WRAPPER_REVISION	The Revision Register contains the ID and revision information for the ECC wrapper.	4802 7010h
14h	ECC_CONTROL	The Control Register controls the ECC control bits for the selected ECC RAM.	4802 7014h
18h	ECC_ERROR_CONTROL1	This register contains ECC error control bits for the selected ECC RAM.	4802 7018h
1Ch	ECC_ERROR_CONTROL2	This register contains ECC error control bits for the selected ECC RAM.	4802 701Ch
20h	ECC_ERROR_STATUS1	This register contains ECC status bits for the selected ECC RAM.	4802 7020h
24h	ECC_ERROR_STATUS2	This register contains ECC status bits for the selected ECC RAM.	4802 7024h
3Ch	ECC_EOI	This is the ECC_EOI register for the interrupt to the host.	4802 703Ch
40h to 7Ch	ECC_INT_STATUS to ECC_INT_STATUS_15	These are the raw level interrupt status bits where each bit corresponds to the pending status from an ECC RAM.	4802 7040h to 4802 707Ch
80h to BCh	ECC_INT_ENABLE_0 to ECC_INT_ENABLE_15	These are interrupt enables associated with the interrupt from each of the ECC RAMs.	4802 7080h to 4802 70BCh
C0h to FCh	ECC_INT_CLEAR_0 to ECC_INT_CLEAR_15	These are interrupt enable clear bits associated with the interrupt from each of the ECC RAMs.	4802 70C0h to 4802 70FCh

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4.5.2.1 ECC_REVISION Register (Offset = 0h) [reset = 0h]

ECC_REVISION is shown in Figure 4-10 and described in Table 4-48.

The Revision Register contains the ID and revision information for the module.

Table 4-47. ECC_REVISION Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7000h

Figure 4-10. ECC_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R - 4E8A0107h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-48. ECC_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R		TI internal data. Identifies revision of peripheral.

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4.5.2.2 ECC_VECTOR Register (Offset = 8h) [reset = 0h]

ECC_VECTOR is shown in Figure 4-11 and described in Table 4-50.

ECC RAM ID to select the ECC RAM to control or read status.

Table 4-49. ECC_VECTOR Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7008h

Figure 4-11. ECC_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							READ_DONE
R-							R-
23	22	21	20	19	18	17	16
READ_ADDRESS							
R/W-							
15	14	13	12	11	10	9	8
TRIGGER_READ	RESERVED					RAM_ID	
R/W-	R-					R/W-	
7	6	5	4	3	2	1	0
RAM_ID							
R/W-							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-50. ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	READ_DONE	R	0h	Status to indicate if read on the serial VBUS is complete.
23-16	READ_ADDRESS	R/W	0h	Read address. Can be any of the registers (10h – 24h).
15	TRIGGER_READ	R/W	0h	Write 1 to trigger a read on the serial VBUS.
14-11	RESERVED	R	0h	Reserved
10-0	RAM_ID	R/W	0h	Value written to select the corresponding ECC RAM for control or status. • 0h: 8KB Data RAM0 • 1h: 8KB Data RAM1 • 2h: 64KB RAM • 3h: 16KB IRAM0 • 4h: 16KB IRAM1 • 5h: Reserved

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4.5.2.3 ECC_MISC_STATUS Register (Offset = Ch) [reset = 0h]

ECC_MISC_STATUS is shown in Figure 4-12 and described in Table 4-52.

Miscellaneous status register.

Table 4-51. ECC_MISC_STATUS Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 700Ch

Figure 4-12. ECC_MISC_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					NUM_RAMS										
R-0h																					R-5h										

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-52. ECC_MISC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUM_RAMS	R	5h	Indicates the number of RAMs serviced by the ECC aggregator.

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4.5.2.4 ECC_WRAPPER_REVISION Register (Offset = 10h) [reset = 0h]

ECC_WRAPPER_REVISION is shown in Figure 4-13 and described in Table 4-54.

The Revision Register contains the ID and revision information for the ECC wrapper.

Table 4-53. ECC_WRAPPER_REVISION Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7010h

Figure 4-13. ECC_WRAPPER_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R -																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-54. ECC_WRAPPER_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R		TI internal data. Identifies revision of peripheral.

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4.5.2.5 ECC_CONTROL Register (Offset = 14h) [reset = 0h]

ECC_CONTROL is shown in Figure 4-14 and described in Table 4-56.

The Global Control Register controls the ECC control bits for the selected ECC RAM.

Table 4-55. ECC_CONTROL Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7014h

Figure 4-14. ECC_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-							
23	22	21	20	19	18	17	16
RESERVED							
R-							
15	14	13	12	11	10	9	8
RESERVED							
R-							
7	6	5	4	3	2	1	0
RESERVED	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	ENABLE_RMW	ECC_CHECK	ECC_ENABLE
R-	R/W-	R/W-	R/W-	R/W-	R/W-	R/W-	R/W-

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-56. ECC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved
6	ERROR_ONCE	R/W	0h	If this bit is set, the FORCE_SEC/ FORCE_DED will inject an error to the specified row only once. The FORCE_SEC bit will be cleared once a writeback happens. If writeback is not enabled, this error will be cleared the cycle following the read when the data is corrected. For double-bit errors, the FORCE_DED bit will be cleared the cycle following the double-bit error. Any subsequent reads will not force an error.
5	FORCE_N_ROW	R/W	0h	Force single/double-bit error on the next RAM read.
4	FORCE_DED	R/W	0h	Force double-bit error. Cleared the cycle following the error if ERROR_ONCE is asserted.
3	FORCE_SEC	R/W	0h	Force single-bit error. Cleared on a writeback or the cycle following the error if ERROR_ONCE is asserted.
2	ENABLE_RMW	R/W	1h	Enable read-modify-write on partial word writes.
1	ECC_CHECK	R/W	1h	Enable ECC check. ECC is completely bypassed if both ECC_ENABLE and ECC_CHECK are 0.
0	ECC_ENABLE	R/W	1h	Enable ECC generation.

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4.5.2.6 ECC_ERROR_CONTROL1 Register (Offset = 18h) [reset = 0h]

ECC_ERROR_CONTROL1 is shown in Figure 4-15 and described in Table 4-58.

This register contains ECC error control bits for the selected ECC RAM.

Table 4-57. ECC_ERROR_CONTROL1 Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7018h

Figure 4-15. ECC_ERROR_CONTROL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT1																ECC_ROW															
R/W-																R/W-															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-58. ECC_ERROR_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECC_BIT1	R/W	0h	Column/ Data bit that needs to be flipped when FORCE_SEC or FORCE_DED is set.
15-0	ECC_ROW	R/W	0h	Row address where FORCE_SEC or FORCE_DED needs to be applied. This is ignored if FORCE_N_ROW is set.

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4.5.2.7 ECC_ERROR_CONTROL2 Register (Offset = 1Ch) [reset = 0h]

ECC_ERROR_CONTROL2 is shown in Figure 4-16 and described in Table 4-60.

This register contains ECC error control bits for the selected ECC RAM.

Table 4-59. ECC_ERROR_CONTROL2 Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 701Ch

Figure 4-16. ECC_ERROR_CONTROL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ECC_BIT2															
R-																R/W-															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-60. ECC_ERROR_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	ECC_BIT2	R/W	0h	Data bit that needs to be flipped when FORCE_DED is set

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4.5.2.8 ECC_ERROR_STATUS1 Register (Offset = 20h) [reset = 0h]

ECC_ERROR_STATUS1 is shown in Figure 4-17 and described in Table 4-62.

This register contains ECC status bits for the selected ECC RAM.

Table 4-61. ECC_ERROR_STATUS1 Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7020h

Figure 4-17. ECC_ERROR_STATUS1 Register

31	30	29	28	27	26	25	24
ECC_ROW							
R-							
23	22	21	20	19	18	17	16
ECC_ROW							
R-							
15	14	13	12	11	10	9	8
RESERVED					CLR_ECC_OTHER	CLR_ECC_DED	CLR_ECC_SEC
R-					R/W1C	R/W1C	R/W1C
7	6	5	4	3	2	1	0
RESERVED					ECC_OTHER	ECC_DED	ECC_SEC
R-					R/W1S	R/W1S	R/W1S

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-62. ECC_ERROR_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECC_ROW	R	0h	Indicates the row/address where the single or double-bit error occurred.
15-11	RESERVED	R	0h	Reserved
10	CLR_ECC_OTHER	R/W1C	0h	1 indicates a successive single-bit error. Writing a 1 clears the status bit.
9	CLR_ECC_DED	R/W1C	0h	1 indicates a pending double-bit error. Writing a 1 clears the status bit.
8	CLR_ECC_SEC	R/W1C	0h	1 indicates a pending single-bit error. Writing a 1 clears the status bit.
7-3	RESERVED	R	0h	Reserved
2	ECC_OTHER	R/W1S	0h	1 indicates that successive single-bit errors have occurred while a writeback is still pending. Software can also write a 1 to set the pending status and write a '1' to the corresponding clear bit to clear the status.
1	ECC_DED	R/W1S	0h	1 indicates pending double-bit error. Since the double-bit error from the ECC logic is a pulsed interrupt, this is also a status set register. The software can also write a '1' to set the pending status and write a '1' to the corresponding clear bit to clear the status.
0	ECC_SEC	R/W1S	0h	1 indicates pending single-bit error status. Since the single-bit error from the ECC logic is a pulsed interrupt, this is also a status set register. The software can also write a '1' to set the pending status and write a '1' to the corresponding clear bit to clear the status.

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4.5.2.9 ECC_ERROR_STATUS2 Register (Offset = 24h) [reset = 0h]

ECC_ERROR_STATUS2 is shown in Figure 4-18 and described in Table 4-64.

This register contains ECC status bits for the selected ECC RAM.

Table 4-63. ECC_ERROR_STATUS2 Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7024h

Figure 4-18. ECC_ERROR_STATUS2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ECC_BIT1															
R-																R-															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-64. ECC_ERROR_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	ECC_BIT1	R	0h	Indicates the bit position in the RAM data that is in error. For eg: a value of 1 indicates that bit 1 in the data is in error. This is valid only for single bit errors (sec).

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4.5.2.10 ECC_EOI Register (Offset = 3Ch) [reset = 0h]

ECC_EOI is shown in Figure 4-19 and described in Table 4-66.

This is the ECC_EOI register for the interrupt to the host.

Table 4-65. ECC_EOI Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 703Ch

Figure 4-19. ECC_EOI Register

31	30	29	28	27	26	25	24
RESERVED							
R-							
23	22	21	20	19	18	17	16
RESERVED							
R-							
15	14	13	12	11	10	9	8
RESERVED							
R-							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-							R/W1S

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-66. ECC_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	Write to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host.

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4.5.2.11 ECC_INT_STATUS_0 to ECC_INT_STATUS_15 Register (Offset = 40h to 7Ch) [reset = 0h]

ECC_INT_STATUS_0 to ECC_INT_STATUS_15 is shown in Figure 4-20 and described in Table 4-68.

These are the raw level interrupt status bits where each bit corresponds to the pending status from an ECC RAM. The bit associations with the ECC RAMs are assigned by the ECC aggregator module. There is 1 register for upto 32 ECC RAMs. The addresses increment for every additional 32-bit register required to hold the interrupt status for all the ECC RAMs (0 to N-1).

Table 4-67. ECC_INT_STATUS_0 to ECC_INT_STATUS_15 Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7040h to 4802 707Ch

Figure 4-20. ECC_INT_STATUS_0 to ECC_INT_STATUS_15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																											SRC_INTR			
R-																											R-			

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-68. ECC_INT_STATUS_0 to ECC_INT_STATUS_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	SRC_INTR	R	0h	Level interrupt status from each ECC RAM. • 0h: Not pending status. • 1h: Pending status.

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4.5.2.12 ECC_INT_ENABLE_0 to ECC_INT_ENABLE_15 Register (Offset = 80h to BCh) [reset = 0h]

ECC_INT_ENABLE_0 to ECC_INT_ENABLE_15 is shown in Figure 4-21 and described in Table 4-70.

These are interrupt enables associated with the interrupt from each of the ECC RAMs. Writing a 1 to a bit position in the register enables the interrupt from the associated ECC RAM. There is 1 register for upto 32 ECC RAMs. The addresses increment for every additional 32-bit register required for all ECC RAMs (0 to N-1).

Table 4-69. ECC_INT_ENABLE_0 to ECC_INT_ENABLE_15 Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 7080h to 4802 70BCh

Figure 4-21. ECC_INT_ENABLE_0 to ECC_INT_ENABLE_15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														ENABLE	
R-																														R/W1S	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-70. ECC_INT_ENABLE_0 to ECC_INT_ENABLE_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	ENABLE	R/W1S	0h	Write 1 to enable interrupt from the associated ECC RAM.

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4.5.2.13 ECC_INT_CLEAR_0 to ECC_INT_CLEAR_15 Register (Offset = C0h to FCh) [reset = 0h]

ECC_INT_CLEAR_0 to ECC_INT_CLEAR_15 is shown in Figure 4-22 and described in Table 4-72.

These are interrupt enable clear bits associated with the interrupt from each of the ECC RAMs. Writing a 1 to a bit position in the register disables the interrupt from the associated ECC RAM. There is 1 register for upto 32 ECC RAMs. The addresses increment for every additional 32-bit register required for all the ECC RAMs (0 to N-1).

Table 4-71. ECC_INT_CLEAR_0 to ECC_INT_CLEAR_15 Instances

Instance	Physical Address
PRU_ICSS_ECC_CFG	4802 70C0h to 4802 70FCh

Figure 4-22. ECC_INT_CLEAR_0 to ECC_INT_CLEAR_15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																														ENABLE_CLEAR	
R-																														R/W1C	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-72. ECC_INT_CLEAR_0 to ECC_INT_CLEAR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	ENABLE_CLEAR	R/W1C	0h	Write 1 to disable interrupt from the associated ECC RAM.

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4.5.3 PRU_ICSS_PRU_CTRL Registers

PRU_ICSS_PRU_CTRL lists the memory-mapped registers for the PRU-ICSS PRU0 and PRU1 cores. All register offset addresses not listed in PRU_ICSS_PRU_CTRL should be considered as reserved locations and the register contents should not be modified.

Table 4-73. PRU-ICSS_PRU_CTRL Instances

Instance	Base Address
PRU_ICSS_PRU0_CTRL	4802 2000h
PRU_ICSS_PRU1_CTRL	4802 4000h

Table 4-74. PRU_ICSS_PRU_CTRL Registers

Offset	Acronym	Register Name	PRU_ICSS_PRU0_CTRL Physical Address	PRU_ICSS_PRU1_CTRL Physical Address
0h	PRU_CONTROL	Control register	4802 2000h	4802 4000h
4h	PRU_STATUS	Status register	4802 2004h	4802 4004h
8h	PRU_WAKEUP_EN	Wakeup enable register	4802 2008h	4802 4008h
Ch	PRU_CYCLE	Cycle count	4802 200Ch	4802 400Ch
10h	PRU_STALL	Stall count	4802 2010h	4802 4010h
20h	PRU_CTBIR0	Constant Table Block Index Register 0	4802 2020h	4802 4020h
24h	PRU_CTBIR1	Constant Table Block Index Register 1	4802 2024h	4802 4024h
28h	PRU_CTPPR0	Constant Table Programmable Pointer Register 0	4802 2028h	4802 4028h
2Ch	PRU_CTPPR1	Constant Table Programmable Pointer Register 1	4802 202Ch	4802 402Ch

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4.5.3.1 PRU_CONTROL Register (Offset = 0h) [reset = 1h]

PRU_CONTROL is shown in Figure 4-23 and described in Table 4-76.

CONTROL REGISTER

Table 4-75. PRU_CONTROL Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 2000h
PRU_ICSS_PRU1_CTRL	4802 4000h

Figure 4-23. PRU_CONTROL Register

31	30	29	28	27	26	25	24
PCOUNTER_RST_VAL							
R/W-0h							
23	22	21	20	19	18	17	16
PCOUNTER_RST_VAL							
R/W-0h							
15	14	13	12	11	10	9	8
RUNSTATE	BIG_ENDIAN	RESERVED					SINGLE_STEP
R-0h	R-0h	R-0h					R/W-0h
7	6	5	4	3	2	1	0
RESERVED				COUNTER_ENABLE	SLEEPING	ENABLE	SOFT_RST_N
R-0h				R/W-0h	R/W-0h	R/W-0h	R-1h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-76. PRU_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PCOUNTER_RST_VAL	R/W	0h	Program Counter Reset Value: This field controls the address where the PRU will start executing code from after it is taken out of reset.
15	RUNSTATE	R	0h	Run State: This bit indicates whether the PRU is currently executing an instruction or is halted. 0 = PRU is halted and host has access to the instruction RAM and debug registers regions. 1 = PRU is currently running and the host is locked out of the instruction RAM and debug registers regions. This bit is used by an external debug agent to know when the PRU has actually halted when waiting for a HALT instruction to execute, a single step to finish, or any other time when the pru_enable has been cleared.
14	BIG_ENDIAN	R	0h	
13-9	RESERVED	R	0h	Reserved
8	SINGLE_STEP	R/W	0h	Single Step Enable: This bit controls whether or not the PRU will only execute a single instruction when enabled. 0 = PRU will free run when enabled. 1 = PRU will execute a single instruction and then the pru_enable bit will be cleared. Note that this bit does not actually enable the PRU, it only sets the policy for how much code will be run after the PRU is enabled. The pru_enable bit must be explicitly asserted. It is legal to initialize both the single_step and pru_enable bits simultaneously. (Two independent writes are not required to cause the stated functionality.)
7-4	RESERVED	R	0h	Reserved

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Table 4-76. PRU_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	COUNTER_ENABLE	R/W	0h	PRU Cycle Counter Enable: Enables PRU cycle counters. 0 = Counters not enabled 1 = Counters enabled
2	SLEEPING	R/W	0h	PRU Sleep Indicator: This bit indicates whether or not the PRU is currently asleep. 0 = PRU is not asleep 1 = PRU is asleep If this bit is written to a 0, the PRU will be forced to power up from sleep mode.
1	ENABLE	R/W	0h	Processor Enable: This bit controls whether or not the PRU is allowed to fetch new instructions. 0 = PRU is disabled. 1 = PRU is enabled. If this bit is de-asserted while the PRU is currently running and has completed the initial cycle of a multi-cycle instruction (LBxO,SBxO,SCAN, etc.), the current instruction will be allowed to complete before the PRU pauses execution. Otherwise, the PRU will halt immediately. Because of the unpredictability timing sensitivity of the instruction execution loop, this bit is not a reliable indication of whether or not the PRU is currently running. The pru_state bit should be consulted for an absolute indication of the run state of the core. When the PRU is halted, its internal state remains coherent therefore this bit can be reasserted without issuing a software reset and the PRU will resume processing exactly where it left off in the instruction stream.
0	SOFT_RST_N	R/W	1h	Soft Reset: When this bit is cleared, the PRU will be reset. This bit is set back to 1 on the next cycle after it has been cleared.

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4.5.3.2 PRU_STATUS Register (Offset = 4h) [reset = 0h]

PRU_STATUS is shown in Figure 4-24 and described in Table 4-78.

STATUS REGISTER

Table 4-77. PRU_STATUS Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 2004h
PRU_ICSS_PRU1_CTRL	4802 4004h

Figure 4-24. PRU_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PCOUNTER															
R-0h																R-0h															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-78. PRU_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	PCOUNTER	R	0h	Program Counter: This field is a registered (1 cycle delayed) reflection of the PRU program counter. Note that the PC is an instruction address where each instruction is a 32 bit word. This is not a byte address and to compute the byte address just multiply the PC by 4 (PC of 2 = byte address of 8h, or PC of 8 = byte address of 20h).

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4.5.3.3 PRU_WAKEUP_EN Register (Offset = 8h) [reset = 0h]

PRU_WAKEUP_EN is shown in Figure 4-25 and described in Table 4-80.

WAKEUP ENABLE REGISTER

Table 4-79. PRU_WAKEUP_EN Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 2008h
PRU_ICSS_PRU1_CTRL	4802 4008h

Figure 4-25. PRU_WAKEUP_EN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BITWISE_ENABLES																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-80. PRU_WAKEUP_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BITWISE_ENABLES	R/W	0h	Wakeup Enables: This field is ANDed with the incoming R31 status inputs (whose bit positions were specified in the stmap parameter) to produce a vector which is unary ORed to produce the status_wakeup source for the core. Setting any bit in this vector will allow the corresponding status input to wake up the core when it is asserted high. The PRU should set this enable vector prior to executing a SLP (sleep) instruction to ensure that the desired sources can wake up the core.

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4.5.3.4 PRU_CYCLE Register (Offset = Ch) [reset = 0h]

PRU_CYCLE is shown in Figure 4-26 and described in Table 4-82.

CYCLE COUNT. This register counts the number of cycles for which the PRU has been enabled.

Table 4-81. PRU_CYCLE Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 200Ch
PRU_ICSS_PRU1_CTRL	4802 400Ch

Figure 4-26. PRU_CYCLE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CYCLECOUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-82. PRU_CYCLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CYCLECOUNT	R/W	0h	This value is incremented by 1 for every cycle during which the PRU is enabled and the counter is enabled (both bits ENABLE and COUNTENABLE set in the PRU control register). Counting halts while the PRU is disabled or counter is disabled, and resumes when re-eneabled. Counter clears the COUNTENABLE bit in the PRU control register when the count reaches FFFFFFFFh. (Count does does not wrap). The register can be read at any time. The register can be cleared when the counter or PRU is disabled. Clearing this register also clears the PRU Stall Count Register.

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4.5.3.5 PRU_STALL Register (Offset = 10h) [reset = 0h]

PRU_STALL is shown in Figure 4-27 and described in Table 4-84.

STALL COUNT. This register counts the number of cycles for which the PRU has been enabled, but unable to fetch a new instruction. It is linked to the Cycle Count Register (0Ch) such that this register reflects the stall cycles measured over the same cycles as counted by the cycle count register. Thus the value of this register is always less than or equal to cycle count.

Table 4-83. PRU_STALL Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 2010h
PRU_ICSS_PRU1_CTRL	4802 4010h

Figure 4-27. PRU_STALL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STALLCOUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-84. PRU_STALL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STALLCOUNT	R/W	0h	This value is incremented by 1 for every cycle during which the PRU is enabled and the counter is enabled (both bits ENABLE and COUNTENABLE set in the PRU control register), and the PRU was unable to fetch a new instruction for any reason.

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4.5.3.6 PRU_CTBIR0 Register (Offset = 20h) [reset = 0h]

PRU_CTBIR0 is shown in Figure 4-28 and described in Table 4-86.

CONSTANT TABLE BLOCK INDEX REGISTER 0. This register is used to set the block indices which are used to modify entries 24 and 25 in the PRU Constant Table. This register can be written by the PRU whenever it needs to change to a new base pointer for a block in the State Scratchpad RAM. This function is useful since the PRU is often processing multiple processing threads which require it to change contexts. The PRU can use this register to avoid requiring excessive amounts of code for repetitive context switching.

Table 4-85. PRU_CTBIR0 Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 2020h
PRU_ICSS_PRU1_CTRL	4802 4020h

Figure 4-28. PRU_CTBIR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								C25_BLK_INDEX							
R-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								C24_BLK_INDEX							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-86. PRU_CTBIR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	C25_BLK_INDEX	R/W	0h	PRU Constant Entry 25 Block Index: This field sets the value that will appear in bits 11:8 of entry 25 in the PRU Constant Table.
15-8	RESERVED	R	0h	Reserved
7-0	C24_BLK_INDEX	R/W	0h	PRU Constant Entry 24 Block Index: This field sets the value that will appear in bits 11:8 of entry 24 in the PRU Constant Table.

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4.5.3.7 PRU_CTBIR1 Register (Offset = 24h) [reset = 0h]

PRU_CTBIR1 is shown in Figure 4-29 and described in Table 4-88.

CONSTANT TABLE BLOCK INDEX REGISTER 1. This register is used to set the block indices which are used to modify entries 26 and 27 in the PRU Constant Table. This register can be written by the PRU whenever it needs to change to a new base pointer for a block in the State Scratchpad RAM. This function is useful since the PRU is often processing multiple processing threads which require it to change contexts. The PRU can use this register to avoid requiring excessive amounts of code for repetitive context switching.

Table 4-87. PRU_CTBIR1 Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 2024h
PRU_ICSS_PRU1_CTRL	4802 4024h

Figure 4-29. PRU_CTBIR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								C27_BLK_INDEX							
R-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								C26_BLK_INDEX							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-88. PRU_CTBIR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	C27_BLK_INDEX	R/W	0h	PRU Constant Entry 27 Block Index: This field sets the value that will appear in bits 11:8 of entry 27 in the PRU Constant Table.
15-8	RESERVED	R	0h	Reserved
7-0	C26_BLK_INDEX	R/W	0h	PRU Constant Entry 26 Block Index: This field sets the value that will appear in bits 11:8 of entry 26 in the PRU Constant Table.

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4.5.3.8 PRU_CTPPR0 Register (Offset = 28h) [reset = 0h]

PRU_CTPPR0 is shown in Figure 4-30 and described in Table 4-90.

CONSTANT TABLE PROGRAMMABLE POINTER REGISTER 0. This register allows the PRU to set up the 256-byte page index for entries 28 and 29 in the PRU Constant Table which serve as general purpose pointers which can be configured to point to any locations inside the session router address map. This register is useful when the PRU needs to frequently access certain structures inside the session router address space whose locations are not hard coded such as tables in scratchpad memory.

Table 4-89. PRU_CTPPR0 Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 2028h
PRU_ICSS_PRU1_CTRL	4802 4028h

Figure 4-30. PRU_CTPPR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C29_POINTER																C28_POINTER															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-90. PRU_CTPPR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	C29_POINTER	R/W	0h	PRU Constant Entry 29 Pointer: This field sets the value that will appear in bits 23:8 of entry 29 in the PRU Constant Table.
15-0	C28_POINTER	R/W	0h	PRU Constant Entry 28 Pointer: This field sets the value that will appear in bits 23:8 of entry 28 in the PRU Constant Table.

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4.5.3.9 PRU_CTPPR1 Register (Offset = 2Ch) [reset = 0h]

PRU_CTPPR1 is shown in Figure 4-31 and described in Table 4-92.

CONSTANT TABLE PROGRAMMABLE POINTER REGISTER 1. This register functions the same as the PRU Constant Table Programmable Pointer Register 0 but allows the PRU to control entries 30 and 31 in the PRU Constant Table.

Table 4-91. PRU_CTPPR1 Instances

Instance	Physical Address
PRU_ICSS_PRU0_CTRL	4802 202Ch
PRU_ICSS_PRU1_CTRL	4802 402Ch

Figure 4-31. PRU_CTPPR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C31_POINTER																C30_POINTER															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-92. PRU_CTPPR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	C31_POINTER	R/W	0h	PRU Constant Entry 31 Pointer: This field sets the value that will appear in bits 23:8 of entry 31 in the PRU Constant Table.
15-0	C30_POINTER	R/W	0h	PRU Constant Entry 30 Pointer: This field sets the value that will appear in bits 23:8 of entry 30 in the PRU Constant Table.

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4.5.4 PRU_ICSS_PRU_DEBUG Registers

PRU_ICSS_PRU_DEBUG Registers lists the memory-mapped registers for the PRU_ICSS_PRU_DEBUG. All register offset addresses not listed in PRU_ICSS_PRU_DEBUG Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-93. PRU-ICSS_PRU_DEBUG Instances

Instance	Base Address
PRU_ICSS_PRU_DEBUG_0	4802 2400h
PRU_ICSS_PRU_DEBUG_1	4802 4400h

Table 4-94. PRU_ICSS_PRU_DEBUG Registers

Offset	Acronym	Register Name	PRU_ICSS_PRU_DEBUG_0 Physical Address	PRU_ICSS_PRU_DEBUG_1 Physical Address
0h	PRU_ICSS_DBG_GPREG0	DEBUG PRU GENERAL PURPOSE REGISTER 0	4802 2400h	4802 4400h
4h	PRU_ICSS_DBG_GPREG1	DEBUG PRU GENERAL PURPOSE REGISTER 1	4802 2404h	4802 4404h
8h	PRU_ICSS_DBG_GPREG2	DEBUG PRU GENERAL PURPOSE REGISTER 2	4802 2408h	4802 4408h
Ch	PRU_ICSS_DBG_GPREG3	DEBUG PRU GENERAL PURPOSE REGISTER 3	4802 240Ch	4802 440Ch
10h	PRU_ICSS_DBG_GPREG4	DEBUG PRU GENERAL PURPOSE REGISTER 4	4802 2410h	4802 4410h
14h	PRU_ICSS_DBG_GPREG5	DEBUG PRU GENERAL PURPOSE REGISTER 5	4802 2414h	4802 4414h
18h	PRU_ICSS_DBG_GPREG6	DEBUG PRU GENERAL PURPOSE REGISTER 6	4802 2418h	4802 4418h
1Ch	PRU_ICSS_DBG_GPREG7	DEBUG PRU GENERAL PURPOSE REGISTER 7	4802 241Ch	4802 441Ch
20h	PRU_ICSS_DBG_GPREG8	DEBUG PRU GENERAL PURPOSE REGISTER 8	4802 2420h	4802 4420h
24h	PRU_ICSS_DBG_GPREG9	DEBUG PRU GENERAL PURPOSE REGISTER 9	4802 2424h	4802 4424h
28h	PRU_ICSS_DBG_GPREG10	DEBUG PRU GENERAL PURPOSE REGISTER 10	4802 2428h	4802 4428h
2Ch	PRU_ICSS_DBG_GPREG11	DEBUG PRU GENERAL PURPOSE REGISTER 11	4802 242Ch	4802 442Ch
30h	PRU_ICSS_DBG_GPREG12	DEBUG PRU GENERAL PURPOSE REGISTER 12	4802 2430h	4802 4430h
34h	PRU_ICSS_DBG_GPREG13	DEBUG PRU GENERAL PURPOSE REGISTER 13	4802 2434h	4802 4434h
38h	PRU_ICSS_DBG_GPREG14	DEBUG PRU GENERAL PURPOSE REGISTER 14	4802 2438h	4802 4438h
3Ch	PRU_ICSS_DBG_GPREG15	DEBUG PRU GENERAL PURPOSE REGISTER 15	4802 243Ch	4802 443Ch
40h	PRU_ICSS_DBG_GPREG16	DEBUG PRU GENERAL PURPOSE REGISTER 16	4802 2440h	4802 4440h
44h	PRU_ICSS_DBG_GPREG17	DEBUG PRU GENERAL PURPOSE REGISTER 17	4802 2444h	4802 4444h
48h	PRU_ICSS_DBG_GPREG18	DEBUG PRU GENERAL PURPOSE REGISTER 18	4802 2448h	4802 4448h
4Ch	PRU_ICSS_DBG_GPREG19	DEBUG PRU GENERAL PURPOSE REGISTER 19	4802 244Ch	4802 444Ch
50h	PRU_ICSS_DBG_GPREG20	DEBUG PRU GENERAL PURPOSE REGISTER 20	4802 2450h	4802 4450h

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Table 4-94. PRU_ICSS_PRU_DEBUG Registers (continued)

Offset	Acronym	Register Name	PRU_ICSS_PRU_DEBUG_0 Physical Address	PRU_ICSS_PRU_DEBUG_1 Physical Address
54h	PRU_ICSS_DBG_GPREG21	DEBUG PRU GENERAL PURPOSE REGISTER 21	4802 2454h	4802 4454h
58h	PRU_ICSS_DBG_GPREG22	DEBUG PRU GENERAL PURPOSE REGISTER 22	4802 2458h	4802 4458h
5Ch	PRU_ICSS_DBG_GPREG23	DEBUG PRU GENERAL PURPOSE REGISTER 23	4802 245Ch	4802 445Ch
60h	PRU_ICSS_DBG_GPREG24	DEBUG PRU GENERAL PURPOSE REGISTER 24	4802 2460h	4802 4460h
64h	PRU_ICSS_DBG_GPREG25	DEBUG PRU GENERAL PURPOSE REGISTER 25	4802 2464h	4802 4464h
68h	PRU_ICSS_DBG_GPREG26	DEBUG PRU GENERAL PURPOSE REGISTER 26	4802 2468h	4802 4468h
6Ch	PRU_ICSS_DBG_GPREG27	DEBUG PRU GENERAL PURPOSE REGISTER 27	4802 246Ch	4802 446Ch
70h	PRU_ICSS_DBG_GPREG28	DEBUG PRU GENERAL PURPOSE REGISTER 28	4802 2470h	4802 4470h
74h	PRU_ICSS_DBG_GPREG29	DEBUG PRU GENERAL PURPOSE REGISTER 29	4802 2474h	4802 4474h
78h	PRU_ICSS_DBG_GPREG30	DEBUG PRU GENERAL PURPOSE REGISTER 30	4802 2478h	4802 4478h
7Ch	PRU_ICSS_DBG_GPREG31	DEBUG PRU GENERAL PURPOSE REGISTER 31	4802 247Ch	4802 447Ch
80h	PRU_ICSS_DBG_CT_REG0	DEBUG PRU CONSTANTS TABLE ENTRY 0	4802 2480h	4802 4480h
84h	PRU_ICSS_DBG_CT_REG1	DEBUG PRU CONSTANTS TABLE ENTRY 1	4802 2484h	4802 4484h
88h	PRU_ICSS_DBG_CT_REG2	DEBUG PRU CONSTANTS TABLE ENTRY 2	4802 2488h	4802 4488h
8Ch	PRU_ICSS_DBG_CT_REG3	DEBUG PRU CONSTANTS TABLE ENTRY 3	4802 248Ch	4802 448Ch
90h	PRU_ICSS_DBG_CT_REG4	DEBUG PRU CONSTANTS TABLE ENTRY 4	4802 2490h	4802 4490h
94h	PRU_ICSS_DBG_CT_REG5	DEBUG PRU CONSTANTS TABLE ENTRY 5	4802 2494h	4802 4494h
98h	PRU_ICSS_DBG_CT_REG6	DEBUG PRU CONSTANTS TABLE ENTRY 6	4802 2498h	4802 4498h
9Ch	PRU_ICSS_DBG_CT_REG7	DEBUG PRU CONSTANTS TABLE ENTRY 7	4802 249Ch	4802 449Ch
A0h	PRU_ICSS_DBG_CT_REG8	DEBUG PRU CONSTANTS TABLE ENTRY 8	4802 24A0h	4802 44A0h
A4h	PRU_ICSS_DBG_CT_REG9	DEBUG PRU CONSTANTS TABLE ENTRY 9	4802 24A4h	4802 44A4h
A8h	PRU_ICSS_DBG_CT_REG10	DEBUG PRU CONSTANTS TABLE ENTRY 10	4802 24A8h	4802 44A8h
ACh	PRU_ICSS_DBG_CT_REG11	DEBUG PRU CONSTANTS TABLE ENTRY 11	4802 24ACh	4802 44ACh
B0h	PRU_ICSS_DBG_CT_REG12	DEBUG PRU CONSTANTS TABLE ENTRY 12	4802 24B0h	4802 44B0h
B4h	PRU_ICSS_DBG_CT_REG13	DEBUG PRU CONSTANTS TABLE ENTRY 13	4802 24B4h	4802 44B4h
B8h	PRU_ICSS_DBG_CT_REG14	DEBUG PRU CONSTANTS TABLE ENTRY 14	4802 24B8h	4802 44B8h
BCh	PRU_ICSS_DBG_CT_REG15	DEBUG PRU CONSTANTS TABLE ENTRY 15	4802 24BCh	4802 44BCh

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Table 4-94. PRU_ICSS_PRU_DEBUG Registers (continued)

Offset	Acronym	Register Name	PRU_ICSS_PRU_DEBUG_0 Physical Address	PRU_ICSS_PRU_DEBUG_1 Physical Address
C0h	PRU_ICSS_DBG_CT_REG16	DEBUG PRU CONSTANTS TABLE ENTRY 16	4802 24C0h	4802 44C0h
C4h	PRU_ICSS_DBG_CT_REG17	DEBUG PRU CONSTANTS TABLE ENTRY 17	4802 24C4h	4802 44C4h
C8h	PRU_ICSS_DBG_CT_REG18	DEBUG PRU CONSTANTS TABLE ENTRY 18	4802 24C8h	4802 44C8h
CCh	PRU_ICSS_DBG_CT_REG19	DEBUG PRU CONSTANTS TABLE ENTRY 19	4802 24CCh	4802 44CCh
D0h	PRU_ICSS_DBG_CT_REG20	DEBUG PRU CONSTANTS TABLE ENTRY 20	4802 24D0h	4802 44D0h
D4h	PRU_ICSS_DBG_CT_REG21	DEBUG PRU CONSTANTS TABLE ENTRY 21	4802 24D4h	4802 44D4h
D8h	PRU_ICSS_DBG_CT_REG22	DEBUG PRU CONSTANTS TABLE ENTRY 22	4802 24D8h	4802 44D8h
DCh	PRU_ICSS_DBG_CT_REG23	DEBUG PRU CONSTANTS TABLE ENTRY 23	4802 24DCh	4802 44DCh
E0h	PRU_ICSS_DBG_CT_REG24	DEBUG PRU CONSTANTS TABLE ENTRY 24	4802 24E0h	4802 44E0h
E4h	PRU_ICSS_DBG_CT_REG25	DEBUG PRU CONSTANTS TABLE ENTRY 25	4802 24E4h	4802 44E4h
E8h	PRU_ICSS_DBG_CT_REG26	DEBUG PRU CONSTANTS TABLE ENTRY 26	4802 24E8h	4802 44E8h
ECh	PRU_ICSS_DBG_CT_REG27	DEBUG PRU CONSTANTS TABLE ENTRY 27	4802 24ECh	4802 44ECh
F0h	PRU_ICSS_DBG_CT_REG28	DEBUG PRU CONSTANTS TABLE ENTRY 28	4802 24F0h	4802 44F0h
F4h	PRU_ICSS_DBG_CT_REG29	DEBUG PRU CONSTANTS TABLE ENTRY 29	4802 24F4h	4802 44F4h
F8h	PRU_ICSS_DBG_CT_REG30	DEBUG PRU CONSTANTS TABLE ENTRY 30	4802 24F8h	4802 44F8h
FCh	PRU_ICSS_DBG_CT_REG31	DEBUG PRU CONSTANTS TABLE ENTRY 31	4802 24FCh	4802 44FCh

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4.5.4.1 PRU_ICSS_DBG_GPREG0 Register (Offset = 0h) [reset = 0h]

PRU_ICSS_DBG_GPREG0 is shown in Figure 4-32 and described in Table 4-96.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 0. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-95. PRU_ICSS_DBG_GPREG0 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2400h
PRU_ICSS_PRU_DEBUG_1	4802 4400h

Figure 4-32. PRU_ICSS_DBG_GPREG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG0																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-96. PRU_ICSS_DBG_GPREG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG0	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.2 PRU_ICSS_DBG_GPREG1 Register (Offset = 4h) [reset = 0h]

PRU_ICSS_DBG_GPREG1 is shown in Figure 4-33 and described in Table 4-98.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 1. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-97. PRU_ICSS_DBG_GPREG1 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2404h
PRU_ICSS_PRU_DEBUG_1	4802 4404h

Figure 4-33. PRU_ICSS_DBG_GPREG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG1																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-98. PRU_ICSS_DBG_GPREG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG1	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.3 PRU_ICSS_DBG_GPREG2 Register (Offset = 8h) [reset = 0h]

PRU_ICSS_DBG_GPREG2 is shown in Figure 4-34 and described in Table 4-100.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 2. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-99. PRU_ICSS_DBG_GPREG2 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2408h
PRU_ICSS_PRU_DEBUG_1	4802 4408h

Figure 4-34. PRU_ICSS_DBG_GPREG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG2																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-100. PRU_ICSS_DBG_GPREG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG2	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.4 PRU_ICSS_DBG_GPREG3 Register (Offset = Ch) [reset = 0h]

PRU_ICSS_DBG_GPREG3 is shown in Figure 4-35 and described in Table 4-102.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 3. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-101. PRU_ICSS_DBG_GPREG3 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 240Ch
PRU_ICSS_PRU_DEBUG_1	4802 440Ch

Figure 4-35. PRU_ICSS_DBG_GPREG3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG3																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-102. PRU_ICSS_DBG_GPREG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG3	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.5 PRU_ICSS_DBG_GPREG4 Register (Offset = 10h) [reset = 0h]

PRU_ICSS_DBG_GPREG4 is shown in Figure 4-36 and described in Table 4-104.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 4. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-103. PRU_ICSS_DBG_GPREG4 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2410h
PRU_ICSS_PRU_DEBUG_1	4802 4410h

Figure 4-36. PRU_ICSS_DBG_GPREG4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG4																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-104. PRU_ICSS_DBG_GPREG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG4	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.6 PRU_ICSS_DBG_GPREG5 Register (Offset = 14h) [reset = 0h]

PRU_ICSS_DBG_GPREG5 is shown in Figure 4-37 and described in Table 4-106.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 5. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-105. PRU_ICSS_DBG_GPREG5 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2414h
PRU_ICSS_PRU_DEBUG_1	4802 4414h

Figure 4-37. PRU_ICSS_DBG_GPREG5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG5																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-106. PRU_ICSS_DBG_GPREG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG5	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.7 PRU_ICSS_DBG_GPREG6 Register (Offset = 18h) [reset = 0h]

PRU_ICSS_DBG_GPREG6 is shown in Figure 4-38 and described in Table 4-108.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 6. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-107. PRU_ICSS_DBG_GPREG6 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2418h
PRU_ICSS_PRU_DEBUG_1	4802 4418h

Figure 4-38. PRU_ICSS_DBG_GPREG6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG6																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-108. PRU_ICSS_DBG_GPREG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG6	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.8 PRU_ICSS_DBG_GPREG7 Register (Offset = 1Ch) [reset = 0h]

PRU_ICSS_DBG_GPREG7 is shown in Figure 4-39 and described in Table 4-110.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 7. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-109. PRU_ICSS_DBG_GPREG7 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 241Ch
PRU_ICSS_PRU_DEBUG_1	4802 441Ch

Figure 4-39. PRU_ICSS_DBG_GPREG7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG7																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-110. PRU_ICSS_DBG_GPREG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG7	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.9 PRU_ICSS_DBG_GPREG8 Register (Offset = 20h) [reset = 0h]

PRU_ICSS_DBG_GPREG8 is shown in Figure 4-40 and described in Table 4-112.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 8. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-111. PRU_ICSS_DBG_GPREG8 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2420h
PRU_ICSS_PRU_DEBUG_1	4802 4420h

Figure 4-40. PRU_ICSS_DBG_GPREG8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG8																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-112. PRU_ICSS_DBG_GPREG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG8	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.10 PRU_ICSS_DBG_GPREG9 Register (Offset = 24h) [reset = 0h]

PRU_ICSS_DBG_GPREG9 is shown in Figure 4-41 and described in Table 4-114.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 9. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-113. PRU_ICSS_DBG_GPREG9 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2424h
PRU_ICSS_PRU_DEBUG_1	4802 4424h

Figure 4-41. PRU_ICSS_DBG_GPREG9 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG9																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-114. PRU_ICSS_DBG_GPREG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG9	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.11 PRU_ICSS_DBG_GPREG10 Register (Offset = 28h) [reset = 0h]

PRU_ICSS_DBG_GPREG10 is shown in Figure 4-42 and described in Table 4-116.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 10. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-115. PRU_ICSS_DBG_GPREG10 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2428h
PRU_ICSS_PRU_DEBUG_1	4802 4428h

Figure 4-42. PRU_ICSS_DBG_GPREG10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG10																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-116. PRU_ICSS_DBG_GPREG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG10	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.12 PRU_ICSS_DBG_GPREG11 Register (Offset = 2Ch) [reset = 0h]

PRU_ICSS_DBG_GPREG11 is shown in Figure 4-43 and described in Table 4-118.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 11. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-117. PRU_ICSS_DBG_GPREG11 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 242Ch
PRU_ICSS_PRU_DEBUG_1	4802 442Ch

Figure 4-43. PRU_ICSS_DBG_GPREG11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG11																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-118. PRU_ICSS_DBG_GPREG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG11	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.13 PRU_ICSS_DBG_GPREG12 Register (Offset = 30h) [reset = 0h]

PRU_ICSS_DBG_GPREG12 is shown in Figure 4-44 and described in Table 4-120.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 12. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-119. PRU_ICSS_DBG_GPREG12 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2430h
PRU_ICSS_PRU_DEBUG_1	4802 4430h

Figure 4-44. PRU_ICSS_DBG_GPREG12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG12																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-120. PRU_ICSS_DBG_GPREG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG12	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.14 PRU_ICSS_DBG_GPREG13 Register (Offset = 34h) [reset = 0h]

PRU_ICSS_DBG_GPREG13 is shown in Figure 4-45 and described in Table 4-122.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 13. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-121. PRU_ICSS_DBG_GPREG13 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2434h
PRU_ICSS_PRU_DEBUG_1	4802 4434h

Figure 4-45. PRU_ICSS_DBG_GPREG13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG13																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-122. PRU_ICSS_DBG_GPREG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG13	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.15 PRU_ICSS_DBG_GPREG14 Register (Offset = 38h) [reset = 0h]

PRU_ICSS_DBG_GPREG14 is shown in Figure 4-46 and described in Table 4-124.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 14. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-123. PRU_ICSS_DBG_GPREG14 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2438h
PRU_ICSS_PRU_DEBUG_1	4802 4438h

Figure 4-46. PRU_ICSS_DBG_GPREG14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG14																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-124. PRU_ICSS_DBG_GPREG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG14	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.16 PRU_ICSS_DBG_GPREG15 Register (Offset = 3Ch) [reset = 0h]

PRU_ICSS_DBG_GRPREG15 is shown in Figure 4-47 and described in Table 4-126.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 15. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-125. PRU_ICSS_DBG_GPREG15 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 243Ch
PRU_ICSS_PRU_DEBUG_1	4802 443Ch

Figure 4-47. PRU_ICSS_DBG_GPREG15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG15																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-126. PRU_ICSS_DBG_GPREG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG15	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.17 PRU_ICSS_DBG_GPREG16 Register (Offset = 40h) [reset = 0h]

PRU_ICSS_DBG_GPREG16 is shown in Figure 4-48 and described in Table 4-128.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 16. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-127. PRU_ICSS_DBG_GPREG16 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2440h
PRU_ICSS_PRU_DEBUG_1	4802 4440h

Figure 4-48. PRU_ICSS_DBG_GPREG16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG16																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-128. PRU_ICSS_DBG_GPREG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG16	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.18 PRU_ICSS_DBG_GPREG17 Register (Offset = 44h) [reset = 0h]

PRU_ICSS_DBG_GPREG17 is shown in Figure 4-49 and described in Table 4-130.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 17. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-129. PRU_ICSS_DBG_GPREG17 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2444h
PRU_ICSS_PRU_DEBUG_1	4802 4444h

Figure 4-49. PRU_ICSS_DBG_GPREG17 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG17																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-130. PRU_ICSS_DBG_GPREG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG17	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.19 PRU_ICSS_DBG_GPREG18 Register (Offset = 48h) [reset = 0h]

PRU_ICSS_DBG_GPREG18 is shown in Figure 4-50 and described in Table 4-132.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 18. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-131. PRU_ICSS_DBG_GPREG18 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2448h
PRU_ICSS_PRU_DEBUG_1	4802 4448h

Figure 4-50. PRU_ICSS_DBG_GPREG18 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG18																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-132. PRU_ICSS_DBG_GPREG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG18	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.20 PRU_ICSS_DBG_GPREG19 Register (Offset = 4Ch) [reset = 0h]

PRU_ICSS_DBG_GPREG19 is shown in Figure 4-51 and described in Table 4-134.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 19. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-133. PRU_ICSS_DBG_GPREG19 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 244Ch
PRU_ICSS_PRU_DEBUG_1	4802 444Ch

Figure 4-51. PRU_ICSS_DBG_GPREG19 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG19																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-134. PRU_ICSS_DBG_GPREG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG19	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.21 PRU_ICSS_DBG_GPREG20 Register (Offset = 50h) [reset = 0h]

PRU_ICSS_DBG_GPREG20 is shown in Figure 4-52 and described in Table 4-136.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 20. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-135. PRU_ICSS_DBG_GPREG20 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2450h
PRU_ICSS_PRU_DEBUG_1	4802 4450h

Figure 4-52. PRU_ICSS_DBG_GPREG20 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG20																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-136. PRU_ICSS_DBG_GPREG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG20	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.22 PRU_ICSS_DBG_GPREG21 Register (Offset = 54h) [reset = 0h]

PRU_ICSS_DBG_GPREG21 is shown in Figure 4-53 and described in Table 4-138.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 21. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-137. PRU_ICSS_DBG_GPREG21 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2454h
PRU_ICSS_PRU_DEBUG_1	4802 4454h

Figure 4-53. PRU_ICSS_DBG_GPREG21 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG21																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-138. PRU_ICSS_DBG_GPREG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG21	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.23 PRU_ICSS_DBG_GPREG22 Register (Offset = 58h) [reset = 0h]

PRU_ICSS_DBG_GPREG22 is shown in Figure 4-54 and described in Table 4-140.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 22. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-139. PRU_ICSS_DBG_GPREG22 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2458h
PRU_ICSS_PRU_DEBUG_1	4802 4458h

Figure 4-54. PRU_ICSS_DBG_GPREG22 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG22																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-140. PRU_ICSS_DBG_GPREG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG22	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.24 PRU_ICSS_DBG_GPREG23 Register (Offset = 5Ch) [reset = 0h]

PRU_ICSS_DBG_GPREG23 is shown in Figure 4-55 and described in Table 4-142.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 23. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-141. PRU_ICSS_DBG_GPREG23 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 245Ch
PRU_ICSS_PRU_DEBUG_1	4802 445Ch

Figure 4-55. PRU_ICSS_DBG_GPREG23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG23																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-142. PRU_ICSS_DBG_GPREG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG23	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.25 PRU_ICSS_DBG_GPREG24 Register (Offset = 60h) [reset = 0h]

PRU_ICSS_DBG_GPREG24 is shown in Figure 4-56 and described in Table 4-144.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 24. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-143. PRU_ICSS_DBG_GPREG24 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2460h
PRU_ICSS_PRU_DEBUG_1	4802 4460h

Figure 4-56. PRU_ICSS_DBG_GPREG24 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG24																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-144. PRU_ICSS_DBG_GPREG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG24	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.26 PRU_ICSS_DBG_GPREG25 Register (Offset = 64h) [reset = 0h]

PRU_ICSS_DBG_GPREG25 is shown in Figure 4-57 and described in Table 4-146.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 25. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-145. PRU_ICSS_DBG_GPREG25 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2464h
PRU_ICSS_PRU_DEBUG_1	4802 4464h

Figure 4-57. PRU_ICSS_DBG_GPREG25 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG25																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-146. PRU_ICSS_DBG_GPREG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG25	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.27 PRU_ICSS_DBG_GPREG26 Register (Offset = 68h) [reset = 0h]

PRU_ICSS_DBG_GPREG26 is shown in Figure 4-58 and described in Table 4-148.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 26. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-147. PRU_ICSS_DBG_GPREG26 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2468h
PRU_ICSS_PRU_DEBUG_1	4802 4468h

Figure 4-58. PRU_ICSS_DBG_GPREG26 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG26																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-148. PRU_ICSS_DBG_GPREG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG26	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.28 PRU_ICSS_DBG_GPREG27 Register (Offset = 6Ch) [reset = 0h]

PRU_ICSS_DBG_GPREG27 is shown in Figure 4-59 and described in Table 4-150.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 27. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-149. PRU_ICSS_DBG_GPREG27 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 246Ch
PRU_ICSS_PRU_DEBUG_1	4802 446Ch

Figure 4-59. PRU_ICSS_DBG_GPREG27 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG27																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-150. PRU_ICSS_DBG_GPREG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG27	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.29 PRU_ICSS_DBG_GPREG28 Register (Offset = 70h) [reset = 0h]

PRU_ICSS_DBG_GPREG28 is shown in Figure 4-60 and described in Table 4-152.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 28. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-151. PRU_ICSS_DBG_GPREG28 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2470h
PRU_ICSS_PRU_DEBUG_1	4802 4470h

Figure 4-60. PRU_ICSS_DBG_GPREG28 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG28																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-152. PRU_ICSS_DBG_GPREG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG28	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.30 PRU_ICSS_DBG_GPREG29 Register (Offset = 74h) [reset = 0h]

PRU_ICSS_DBG_GPREG29 is shown in Figure 4-61 and described in Table 4-154.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 29. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-153. PRU_ICSS_DBG_GPREG29 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2474h
PRU_ICSS_PRU_DEBUG_1	4802 4474h

Figure 4-61. PRU_ICSS_DBG_GPREG29 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG29																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-154. PRU_ICSS_DBG_GPREG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG29	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.31 PRU_ICSS_DBG_GPREG30 Register (Offset = 78h) [reset = 0h]

PRU_ICSS_DBG_GPREG30 is shown in Figure 4-62 and described in Table 4-156.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 30. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-155. PRU_ICSS_DBG_GPREG30 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2478h
PRU_ICSS_PRU_DEBUG_1	4802 4478h

Figure 4-62. PRU_ICSS_DBG_GPREG30 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GP_REG30																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-156. PRU_ICSS_DBG_GPREG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GP_REG30	R/W	0h	PRU Internal GP Register n: Reading / writing this field directly inspects/modifies the corresponding internal register in the PRU internal regfile.

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4.5.4.32 PRU_ICSS_DBG_GPREG31 Register (Offset = 7Ch) [reset = 0h]

PRU_ICSS_DBG_GPREG31 is shown in Figure 4-63 and described in Table 4-158.

Return to Summary Table.

DEBUG PRU GENERAL PURPOSE REGISTER 31. This register allows an external agent to debug the PRU while it is disabled. Reading or writing to these registers will have the same effect as a read or write to these registers from an internal instruction in the PRU. For R30, this includes generation of the pulse outputs whenever the register is written.

Table 4-157. PRU_ICSS_DBG_GPREG31 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 247Ch
PRU_ICSS_PRU_DEBUG_1	4802 447Ch

Figure 4-63. PRU_ICSS_DBG_GPREG31 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPREG31																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-158. PRU_ICSS_DBG_GPREG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GPREG31	R/W	0h	

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4.5.4.33 PRU_ICSS_DBG_CT_REG0 Register (Offset = 80h) [reset = 00020000h]

PRU_ICSS_DBG_CT_REG0 is shown in Figure 4-64 and described in Table 4-160.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 0. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-159. PRU_ICSS_DBG_CT_REG0 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2480h
PRU_ICSS_PRU_DEBUG_1	4802 4480h

Figure 4-64. PRU_ICSS_DBG_CT_REG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG0																															
R-00020000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-160. PRU_ICSS_DBG_CT_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG0	R	00020000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.34 PRU_ICSS_DBG_CT_REG1 Register (Offset = 84h) [reset = 48040000h]

PRU_ICSS_DBG_CT_REG1 is shown in Figure 4-65 and described in Table 4-162.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 1. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-161. PRU_ICSS_DBG_CT_REG1 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2484h
PRU_ICSS_PRU_DEBUG_1	4802 4484h

Figure 4-65. PRU_ICSS_DBG_CT_REG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG1																															
R-48040000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-162. PRU_ICSS_DBG_CT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG1	R	48040000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.35 PRU_ICSS_DBG_CT_REG2 Register (Offset = 88h) [reset = 4802A000h]

PRU_ICSS_DBG_CT_REG2 is shown in Figure 4-66 and described in Table 4-164.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 2. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-163. PRU_ICSS_DBG_CT_REG2 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2488h
PRU_ICSS_PRU_DEBUG_1	4802 4488h

Figure 4-66. PRU_ICSS_DBG_CT_REG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG2																															
R-4802A000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-164. PRU_ICSS_DBG_CT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG2	R	4802A000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.36 PRU_ICSS_DBG_CT_REG3 Register (Offset = 8Ch) [reset = 00030000h]

PRU_ICSS_DBG_CT_REG3 is shown in Figure 4-67 and described in Table 4-166.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 3. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-165. PRU_ICSS_DBG_CT_REG3 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 248Ch
PRU_ICSS_PRU_DEBUG_1	4802 448Ch

Figure 4-67. PRU_ICSS_DBG_CT_REG3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG3																															
R-00030000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-166. PRU_ICSS_DBG_CT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG3	R	00030000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.37 PRU_ICSS_DBG_CT_REG4 Register (Offset = 90h) [reset = 00026000h]

PRU_ICSS_DBG_CT_REG4 is shown in Figure 4-68 and described in Table 4-168.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 4. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-167. PRU_ICSS_DBG_CT_REG4 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2490h
PRU_ICSS_PRU_DEBUG_1	4802 4490h

Figure 4-68. PRU_ICSS_DBG_CT_REG4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG4																															
R-00026000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-168. PRU_ICSS_DBG_CT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG4	R	00026000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.38 PRU_ICSS_DBG_CT_REG5 Register (Offset = 94h) [reset = 48060000h]

PRU_ICSS_DBG_CT_REG5 is shown in Figure 4-69 and described in Table 4-170.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 5. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-169. PRU_ICSS_DBG_CT_REG5 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2494h
PRU_ICSS_PRU_DEBUG_1	4802 4494h

Figure 4-69. PRU_ICSS_DBG_CT_REG5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG5																															
R-48060000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-170. PRU_ICSS_DBG_CT_REG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG5	R	48060000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.39 PRU_ICSS_DBG_CT_REG6 Register (Offset = 98h) [reset = 48030000h]

PRU_ICSS_DBG_CT_REG6 is shown in Figure 4-70 and described in Table 4-172.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 6. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-171. PRU_ICSS_DBG_CT_REG6 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 2498h
PRU_ICSS_PRU_DEBUG_1	4802 4498h

Figure 4-70. PRU_ICSS_DBG_CT_REG6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG6																															
R-48030000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-172. PRU_ICSS_DBG_CT_REG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG6	R	48030000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.40 PRU_ICSS_DBG_CT_REG7 Register (Offset = 9Ch) [reset = 00028000h]

PRU_ICSS_DBG_CT_REG7 is shown in Figure 4-71 and described in Table 4-174.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 7. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-173. PRU_ICSS_DBG_CT_REG7 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 249Ch
PRU_ICSS_PRU_DEBUG_1	4802 449Ch

Figure 4-71. PRU_ICSS_DBG_CT_REG7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG7																															
R-00028000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-174. PRU_ICSS_DBG_CT_REG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG7	R	00028000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.41 PRU_ICSS_DBG_CT_REG8 Register (Offset = A0h) [reset = 46000000h]

PRU_ICSS_DBG_CT_REG8 is shown in Figure 4-72 and described in Table 4-176.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 8. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-175. PRU_ICSS_DBG_CT_REG8 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24A0h
PRU_ICSS_PRU_DEBUG_1	4802 44A0h

Figure 4-72. PRU_ICSS_DBG_CT_REG8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG8																															
R-46000000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-176. PRU_ICSS_DBG_CT_REG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG8	R	46000000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.42 PRU_ICSS_DBG_CT_REG9 Register (Offset = A4h) [reset = 4A100000h]

PRU_ICSS_DBG_CT_REG9 is shown in Figure 4-73 and described in Table 4-178.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 9. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-177. PRU_ICSS_DBG_CT_REG9 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24A4h
PRU_ICSS_PRU_DEBUG_1	4802 44A4h

Figure 4-73. PRU_ICSS_DBG_CT_REG9 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG9																															
R-4A100000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-178. PRU_ICSS_DBG_CT_REG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG9	R	4A100000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.43 PRU_ICSS_DBG_CT_REG10 Register (Offset = A8h) [reset = 48318000h]

PRU_ICSS_DBG_CT_REG10 is shown in Figure 4-74 and described in Table 4-180.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 10. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-179. PRU_ICSS_DBG_CT_REG10 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24A8h
PRU_ICSS_PRU_DEBUG_1	4802 44A8h

Figure 4-74. PRU_ICSS_DBG_CT_REG10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG10																															
R-48318000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-180. PRU_ICSS_DBG_CT_REG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG10	R	48318000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.44 PRU_ICSS_DBG_CT_REG11 Register (Offset = ACh) [reset = 48022000h]

PRU_ICSS_DBG_CT_REG11 is shown in Figure 4-75 and described in Table 4-182.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 11. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-181. PRU_ICSS_DBG_CT_REG11 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24ACh
PRU_ICSS_PRU_DEBUG_1	4802 44ACh

Figure 4-75. PRU_ICSS_DBG_CT_REG11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG11																															
R-48022000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-182. PRU_ICSS_DBG_CT_REG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG11	R	48022000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.45 PRU_ICSS_DBG_CT_REG12 Register (Offset = B0h) [reset = 48024000h]

PRU_ICSS_DBG_CT_REG12 is shown in Figure 4-76 and described in Table 4-184.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 12. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-183. PRU_ICSS_DBG_CT_REG12 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24B0h
PRU_ICSS_PRU_DEBUG_1	4802 44B0h

Figure 4-76. PRU_ICSS_DBG_CT_REG12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG12																															
R-48024000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-184. PRU_ICSS_DBG_CT_REG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG12	R	48024000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.46 PRU_ICSS_DBG_CT_REG13 Register (Offset = B4h) [reset = 48310000h]

PRU_ICSS_DBG_CT_REG13 is shown in Figure 4-77 and described in Table 4-186.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 13. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-185. PRU_ICSS_DBG_CT_REG13 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24B4h
PRU_ICSS_PRU_DEBUG_1	4802 44B4h

Figure 4-77. PRU_ICSS_DBG_CT_REG13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG13																															
R-48310000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-186. PRU_ICSS_DBG_CT_REG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG13	R	48310000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.47 PRU_ICSS_DBG_CT_REG14 Register (Offset = B8h) [reset = 481CC000h]

PRU_ICSS_DBG_CT_REG14 is shown in Figure 4-78 and described in Table 4-188.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 14. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-187. PRU_ICSS_DBG_CT_REG14 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24B8h
PRU_ICSS_PRU_DEBUG_1	4802 44B8h

Figure 4-78. PRU_ICSS_DBG_CT_REG14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG14																															
R-481CC000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-188. PRU_ICSS_DBG_CT_REG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG14	R	481CC000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.48 PRU_ICSS_DBG_CT_REG15 Register (Offset = BCh) [reset = 481D0000h]

PRU_ICSS_DBG_CT_REG15 is shown in Figure 4-79 and described in Table 4-190.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 15. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-189. PRU_ICSS_DBG_CT_REG15 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24BCh
PRU_ICSS_PRU_DEBUG_1	4802 44BCh

Figure 4-79. PRU_ICSS_DBG_CT_REG15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG15																															
R-481D0000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-190. PRU_ICSS_DBG_CT_REG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG15	R	481D0000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.49 PRU_ICSS_DBG_CT_REG16 Register (Offset = C0h) [reset = 481A0000h]

PRU_ICSS_DBG_CT_REG16 is shown in Figure 4-80 and described in Table 4-192.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 16. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-191. PRU_ICSS_DBG_CT_REG16 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24C0h
PRU_ICSS_PRU_DEBUG_1	4802 44C0h

Figure 4-80. PRU_ICSS_DBG_CT_REG16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG16																															
R-481A0000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-192. PRU_ICSS_DBG_CT_REG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG16	R	481A0000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.50 PRU_ICSS_DBG_CT_REG17 Register (Offset = C4h) [reset = 4819C000h]

PRU_ICSS_DBG_CT_REG17 is shown in Figure 4-81 and described in Table 4-194.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 17. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-193. PRU_ICSS_DBG_CT_REG17 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24C4h
PRU_ICSS_PRU_DEBUG_1	4802 44C4h

Figure 4-81. PRU_ICSS_DBG_CT_REG17 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG17																															
R-4819C000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-194. PRU_ICSS_DBG_CT_REG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG17	R	4819C000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.51 PRU_ICSS_DBG_CT_REG18 Register (Offset = C8h) [reset = 48300000h]

PRU_ICSS_DBG_CT_REG18 is shown in Figure 4-82 and described in Table 4-196.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 18. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-195. PRU_ICSS_DBG_CT_REG18 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24C8h
PRU_ICSS_PRU_DEBUG_1	4802 44C8h

Figure 4-82. PRU_ICSS_DBG_CT_REG18 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG18																															
R-48300000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-196. PRU_ICSS_DBG_CT_REG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG18	R	48300000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.52 PRU_ICSS_DBG_CT_REG19 Register (Offset = CCh) [reset = 48302000h]

PRU_ICSS_DBG_CT_REG19 is shown in Figure 4-83 and described in Table 4-198.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 19. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-197. PRU_ICSS_DBG_CT_REG19 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24CCh
PRU_ICSS_PRU_DEBUG_1	4802 44CCh

Figure 4-83. PRU_ICSS_DBG_CT_REG19 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG19																															
R-48302000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-198. PRU_ICSS_DBG_CT_REG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG19	R	48302000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.53 PRU_ICSS_DBG_CT_REG20 Register (Offset = D0h) [reset = 48304000h]

PRU_ICSS_DBG_CT_REG20 is shown in Figure 4-84 and described in Table 4-200.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 20. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-199. PRU_ICSS_DBG_CT_REG20 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24D0h
PRU_ICSS_PRU_DEBUG_1	4802 44D0h

Figure 4-84. PRU_ICSS_DBG_CT_REG20 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG20																															
R-48304000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-200. PRU_ICSS_DBG_CT_REG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG20	R	48304000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.54 PRU_ICSS_DBG_CT_REG21 Register (Offset = D4h) [reset = 00032400h]

PRU_ICSS_DBG_CT_REG21 is shown in Figure 4-85 and described in Table 4-202.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 21. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-201. PRU_ICSS_DBG_CT_REG21 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24D4h
PRU_ICSS_PRU_DEBUG_1	4802 44D4h

Figure 4-85. PRU_ICSS_DBG_CT_REG21 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG21																															
R-00032400h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-202. PRU_ICSS_DBG_CT_REG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG21	R	00032400h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.55 PRU_ICSS_DBG_CT_REG22 Register (Offset = D8h) [reset = 480C8000h]

PRU_ICSS_DBG_CT_REG22 is shown in Figure 4-86 and described in Table 4-204.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 22. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-203. PRU_ICSS_DBG_CT_REG22 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24D8h
PRU_ICSS_PRU_DEBUG_1	4802 44D8h

Figure 4-86. PRU_ICSS_DBG_CT_REG22 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG22																															
R-480C8000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-204. PRU_ICSS_DBG_CT_REG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG22	R	480C8000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.56 PRU_ICSS_DBG_CT_REG23 Register (Offset = DCh) [reset = 480CA000h]

PRU_ICSS_DBG_CT_REG23 is shown in Figure 4-87 and described in Table 4-206.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 23. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-205. PRU_ICSS_DBG_CT_REG23 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24DCh
PRU_ICSS_PRU_DEBUG_1	4802 44DCh

Figure 4-87. PRU_ICSS_DBG_CT_REG23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG23																															
R-480CA000h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-206. PRU_ICSS_DBG_CT_REG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG23	R	480CA000h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table.

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4.5.4.57 PRU_ICSS_DBG_CT_REG24 Register (Offset = E0h) [reset = 0h]

PRU_ICSS_DBG_CT_REG24 is shown in Figure 4-88 and described in Table 4-208.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 24. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-207. PRU_ICSS_DBG_CT_REG24 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24E0h
PRU_ICSS_PRU_DEBUG_1	4802 44E0h

Figure 4-88. PRU_ICSS_DBG_CT_REG24 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG24																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-208. PRU_ICSS_DBG_CT_REG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG24	R	0h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table. This entry is partially programmable through the C24_BLK_INDEX in the PRU Control register. The reset value for this Constant Table Entry is 0x00000n00, n=C24_BLK_INDEX[3:0].

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4.5.4.58 PRU_ICSS_DBG_CT_REG25 Register (Offset = E4h) [reset = 0h]

PRU_ICSS_DBG_CT_REG25 is shown in Figure 4-89 and described in Table 4-210.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 25. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-209. PRU_ICSS_DBG_CT_REG25 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24E4h
PRU_ICSS_PRU_DEBUG_1	4802 44E4h

Figure 4-89. PRU_ICSS_DBG_CT_REG25 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG25																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-210. PRU_ICSS_DBG_CT_REG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG25	R	0h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table. This entry is partially programmable through the C25_BLK_INDEX in the PRU Control register. The reset value for this Constant Table Entry is 0x00002n00, n=C25_BLK_INDEX[3:0].

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4.5.4.59 PRU_ICSS_DBG_CT_REG26 Register (Offset = E8h) [reset = 0h]

PRU_ICSS_DBG_CT_REG26 is shown in Figure 4-90 and described in Table 4-212.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 26. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-211. PRU_ICSS_DBG_CT_REG26 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24E8h
PRU_ICSS_PRU_DEBUG_1	4802 44E8h

Figure 4-90. PRU_ICSS_DBG_CT_REG26 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG26																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-212. PRU_ICSS_DBG_CT_REG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG26	R	0h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table. This entry is partially programmable through the C26_BLK_INDEX in the PRU Control register. The reset value for this Constant Table Entry is 0x0002En00, n=C26_BLK_INDEX[3:0].

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4.5.4.60 PRU_ICSS_DBG_CT_REG27 Register (Offset = ECh) [reset = 0h]

PRU_ICSS_DBG_CT_REG27 is shown in Figure 4-91 and described in Table 4-214.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 27. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-213. PRU_ICSS_DBG_CT_REG27 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24ECh
PRU_ICSS_PRU_DEBUG_1	4802 44ECh

Figure 4-91. PRU_ICSS_DBG_CT_REG27 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG27																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-214. PRU_ICSS_DBG_CT_REG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG27	R	0h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table. This entry is partially programmable through the C27_BLK_INDEX in the PRU Control register. The reset value for this Constant Table Entry is 0x00032n00, n=C27_BLK_INDEX[3:0].

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4.5.4.61 PRU_ICSS_DBG_CT_REG28 Register (Offset = F0h) [reset = 0h]

PRU_ICSS_DBG_CT_REG28 is shown in Figure 4-92 and described in Table 4-216.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 28. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-215. PRU_ICSS_DBG_CT_REG28 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24F0h
PRU_ICSS_PRU_DEBUG_1	4802 44F0h

Figure 4-92. PRU_ICSS_DBG_CT_REG28 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG28																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-216. PRU_ICSS_DBG_CT_REG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG28	R	0h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table. This entry is partially programmable through the C28_POINTER in the PRU Control register. The reset value for this Constant Table Entry is 0x00nnnn00, nnnn=C28_POINTER[15:0].

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4.5.4.62 PRU_ICSS_DBG_CT_REG29 Register (Offset = F4h) [reset = 0h]

PRU_ICSS_DBG_CT_REG29 is shown in Figure 4-93 and described in Table 4-218.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 29. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-217. PRU_ICSS_DBG_CT_REG29 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24F4h
PRU_ICSS_PRU_DEBUG_1	4802 44F4h

Figure 4-93. PRU_ICSS_DBG_CT_REG29 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG29																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-218. PRU_ICSS_DBG_CT_REG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG29	R	0h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table. This entry is partially programmable through the C29_POINTER in the PRU Control register. The reset value for this Constant Table Entry is 0x49nnnn00, nnnn=C29_POINTER[15:0].

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4.5.4.63 PRU_ICSS_DBG_CT_REG30 Register (Offset = F8h) [reset = 0h]

PRU_ICSS_DBG_CT_REG30 is shown in Figure 4-94 and described in Table 4-220.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 30. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-219. PRU_ICSS_DBG_CT_REG30 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24F8h
PRU_ICSS_PRU_DEBUG_1	4802 44F8h

Figure 4-94. PRU_ICSS_DBG_CT_REG30 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG30																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-220. PRU_ICSS_DBG_CT_REG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG30	R	0h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table. This entry is partially programmable through the C30_POINTER in the PRU Control register. The reset value for this Constant Table Entry is 0x40nnnn00, nnnn=C30_POINTER[15:0].

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4.5.4.64 PRU_ICSS_DBG_CT_REG31 Register (Offset = FCh) [reset = 0h]

PRU_ICSS_DBG_CT_REG31 is shown in Figure 4-95 and described in Table 4-222.

Return to Summary Table.

DEBUG PRU CONSTANTS TABLE ENTRY 31. This register allows an external agent to debug the PRU while it is disabled. Since some of the constants table entries may actually depend on system inputs / and or the internal state of the PRU, these registers are provided to allow an external agent to easily determine the state of the constants table.

Table 4-221. PRU_ICSS_DBG_CT_REG31 Instances

Instance	Physical Address
PRU_ICSS_PRU_DEBUG_0	4802 24FCh
PRU_ICSS_PRU_DEBUG_1	4802 44FCh

Figure 4-95. PRU_ICSS_DBG_CT_REG31 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CT_REG31																															
R-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-222. PRU_ICSS_DBG_CT_REG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CT_REG31	R	0h	PRU Internal Constants Table Entry n: Reading this field directly inspects the corresponding entry in the PRU internal constants table. This entry is partially programmable through the C31_POINTER in the PRU Control register. The reset value for this Constant Table Entry is 0x80nnnn00, nnnn=C31_POINTER[15:0].

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4.5.5 PRU_ICSS Interrupt Contoller Registers

PRU_ICSS_INTC Registers lists the memory-mapped registers for the PRU-ICSS interrupt controller. All register offset addresses not listed in PRU_ICSS_INTC Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-223. PRU_ICSS_INTC Instances

Instance	Base Address
PRU_ICSS_INTC	4802 0000h

Table 4-224. PRU_ICSS_INTC Registers

Offset	Acronym	Register Name	PRU_ICSS_INTC Physical Address
0h	PRU_ICSS_INTC_REVID	Revision ID Register	4802 0000h
4h	PRU_ICSS_INTC_CR	Control Register	4802 0004h
10h	PRU_ICSS_INTC_GER	Global Host Interrupt Enable Register	4802 0010h
1Ch	PRU_ICSS_INTC_GNLR	Global Nesting Level Register	4802 001Ch
20h	PRU_ICSS_INTC_SISR	System Interrupt Status Indexed Set Register	4802 0020h
24h	PRU_ICSS_INTC_SICR	System Interrupt Status Indexed Clear Register	4802 0024h
28h	PRU_ICSS_INTC_EISR	System Interrupt Enable Indexed Set Register	4802 0028h
2Ch	PRU_ICSS_INTC_EICR	System Interrupt Enable Indexed Clear Register	4802 002Ch
34h	PRU_ICSS_INTC_HIEISR	Host Interrupt Enable Indexed Set Register	4802 0034h
38h	PRU_ICSS_INTC_HIEICR	Host Interrupt Enable Indexed Clear Register	4802 0038h
80h	PRU_ICSS_INTC_GPIR	Global Prioritized Index Register	4802 0080h
200h	PRU_ICSS_INTC_SRS0	System Interrupt Status Raw Set Register0	4802 0200h
204h	PRU_ICSS_INTC_SRS1	System Interrupt Status Raw Set Register1	4802 0204h
280h	PRU_ICSS_INTC_SECR0	System Interrupt Status Enabled Clear Register0	4802 0280h
284h	PRU_ICSS_INTC_SECR1	System Interrupt Status Enabled Clear Register1	4802 0284h
300h	PRU_ICSS_INTC_ESR0	System Interrupt Enable Set Register0	4802 0300h
304h	PRU_ICSS_INTC_ESR1	System Interrupt Enable Set Register1	4802 0304h
380h	PRU_ICSS_INTC_ECR0	System Interrupt Enable Clear Register0	4802 0380h
384h	PRU_ICSS_INTC_ECR1	System Interrupt Enable Clear Register1	4802 0384h
400h	PRU_ICSS_INTC_CMR_0	Channel Map Register_0	4802 0400h
404h	PRU_ICSS_INTC_CMR_1	Channel Map Register_1	4802 0404h
408h	PRU_ICSS_INTC_CMR_2	Channel Map Register_2	4802 0408h
40Ch	PRU_ICSS_INTC_CMR_3	Channel Map Register_3	4802 040Ch
410h	PRU_ICSS_INTC_CMR_4	Channel Map Register_4	4802 0410h
414h	PRU_ICSS_INTC_CMR_5	Channel Map Register_5	4802 0414h
418h	PRU_ICSS_INTC_CMR_6	Channel Map Register_6	4802 0418h
41Ch	PRU_ICSS_INTC_CMR_7	Channel Map Register_7	4802 041Ch
420h	PRU_ICSS_INTC_CMR_8	Channel Map Register_8	4802 0420h
424h	PRU_ICSS_INTC_CMR_9	Channel Map Register_9	4802 0424h
428h	PRU_ICSS_INTC_CMR_10	Channel Map Register_10	4802 0428h
42Ch	PRU_ICSS_INTC_CMR_11	Channel Map Register_11	4802 042Ch
430h	PRU_ICSS_INTC_CMR_12	Channel Map Register_12	4802 0430h
434h	PRU_ICSS_INTC_CMR_13	Channel Map Register_13	4802 0434h
438h	PRU_ICSS_INTC_CMR_14	Channel Map Register_14	4802 0438h
43Ch	PRU_ICSS_INTC_CMR_15	Channel Map Register_15	4802 043Ch
800h	PRU_ICSS_INTC_HMR0	Host Interrupt Map Register0	4802 0800h
804h	PRU_ICSS_INTC_HMR1	Host Interrupt Map Register1	4802 0804h
808h	PRU_ICSS_INTC_HMR2	Host Interrupt Map Register2	4802 0808h

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Table 4-224. PRU_ICSS_INTC Registers (continued)

Offset	Acronym	Register Name	PRU_ICSS_INTC Physical Address
900h	PRU_ICSS_INTC_HIPIR_0	Host Interrupt Prioritized Index Register_0	4802 0900h
904h	PRU_ICSS_INTC_HIPIR_1	Host Interrupt Prioritized Index Register_1	4802 0904h
908h	PRU_ICSS_INTC_HIPIR_2	Host Interrupt Prioritized Index Register_2	4802 0908h
90Ch	PRU_ICSS_INTC_HIPIR_3	Host Interrupt Prioritized Index Register_3	4802 090Ch
910h	PRU_ICSS_INTC_HIPIR_4	Host Interrupt Prioritized Index Register_4	4802 0910h
914h	PRU_ICSS_INTC_HIPIR_5	Host Interrupt Prioritized Index Register_5	4802 0914h
918h	PRU_ICSS_INTC_HIPIR_6	Host Interrupt Prioritized Index Register_6	4802 0918h
91Ch	PRU_ICSS_INTC_HIPIR_7	Host Interrupt Prioritized Index Register_7	4802 091Ch
920h	PRU_ICSS_INTC_HIPIR_8	Host Interrupt Prioritized Index Register_8	4802 0920h
924h	PRU_ICSS_INTC_HIPIR_9	Host Interrupt Prioritized Index Register_9	4802 0924h
D00h	PRU_ICSS_INTC_SIPR0	System Interrupt Polarity Register0	4802 0D00h
D04h	PRU_ICSS_INTC_SIPR1	System Interrupt Polarity Register1	4802 0D04h
D80h	PRU_ICSS_INTC_SITR0	System Interrupt Type Register0	4802 0D80h
D84h	PRU_ICSS_INTC_SITR1	System Interrupt Type Register1	4802 0D84h
1100h	PRU_ICSS_INTC_HINLR_0	Host Interrupt Nesting Level Register_0	4802 1100h
1104h	PRU_ICSS_INTC_HINLR_1	Host Interrupt Nesting Level Register_1	4802 1104h
1108h	PRU_ICSS_INTC_HINLR_2	Host Interrupt Nesting Level Register_2	4802 1108h
110Ch	PRU_ICSS_INTC_HINLR_3	Host Interrupt Nesting Level Register_3	4802 110Ch
1110h	PRU_ICSS_INTC_HINLR_4	Host Interrupt Nesting Level Register_4	4802 1110h
1114h	PRU_ICSS_INTC_HINLR_5	Host Interrupt Nesting Level Register_5	4802 1114h
1118h	PRU_ICSS_INTC_HINLR_6	Host Interrupt Nesting Level Register_6	4802 1118h
111Ch	PRU_ICSS_INTC_HINLR_7	Host Interrupt Nesting Level Register_7	4802 111Ch
1120h	PRU_ICSS_INTC_HINLR_8	Host Interrupt Nesting Level Register_8	4802 1120h
1124h	PRU_ICSS_INTC_HINLR_9	Host Interrupt Nesting Level Register_9	4802 1124h
1500h	PRU_ICSS_INTC_HIER	Host Interrupt Enable Registers	4802 1500h

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4.5.5.1 PRU_ICSS_INTC_REVID Register (Offset = 0h) [reset = 0h]

PRU_ICSS_INTC_REVID is shown in Figure 4-96 and described in .

Revision ID Register

Table 4-225. PRU_ICSS_INTC_REVID Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0000h

Figure 4-96. PRU_ICSS_INTC_REVID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															
R--h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-226. PRU_ICSS_INTC_REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REVISION	R	-h	IP Revision

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4.5.5.2 PRU_ICSS_INTC_CR Register (Offset = 4h) [reset = 0h]

PRU_ICSS_INTC_CR is shown in Figure 4-97 and described in Table 4-228.

The Control Register holds global control parameters and can forces a soft reset on the module.

Table 4-227. PRU_ICSS_INTC_CR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0004h

Figure 4-97. PRU_ICSS_INTC_CR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			PRIORITY_HOLD_MODE	NEST_MODE		WAKEUP_MODE	RESERVED
R-0h			R/W-0h	R/W-0h		R/W-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-228. PRU_ICSS_INTC_CR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	PRIORITY_HOLD_MODE	R/W	0h	Reserved
3-2	NEST_MODE	R/W	0h	The nesting mode. 0h: No nesting 1h: Automatic individual nesting (per host interrupt) 2h: Automatic global nesting (over all host interrupts) 3h: Manual nesting
1	WAKEUP_MODE	R/W	0h	Reserved
0	RESERVED	R	0h	Reserved

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4.5.5.3 PRU_ICSS_INTC_GER Register (Offset = 10h) [reset = 0h]

PRU_ICSS_INTC_GER is shown in Figure 4-98 and described in Table 4-230.

The Global Host Interrupt Enable Register enables all the host interrupts. Individual host interrupts are still enabled or disabled from their individual enables and are not overridden by the global enable.

Table 4-229. PRU_ICSS_INTC_GER Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0010h

Figure 4-98. PRU_ICSS_INTC_GER Register

31	30	29	28	27	26	25	24
RESERVED							
R-0000 000h							
23	22	21	20	19	18	17	16
RESERVED							
R-0000 000h							
15	14	13	12	11	10	9	8
RESERVED							
R-0000 000h							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_HINT_ANY
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-230. PRU_ICSS_INTC_GER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0000 000h	Reserved
0	ENABLE_HINT_ANY	R/W	0h	The current global enable value when read. Writes set the global enable.

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4.5.5.4 PRU_ICSS_INTC_GNLR Register (Offset = 1Ch) [reset = 100h]

PRU_ICSS_INTC_GNLR is shown in Figure 4-99 and described in Table 4-232.

The Global Nesting Level Register allows the checking and setting of the global nesting level across all host interrupts when automatic global nesting mode is set. The nesting level is the channel (and all of lower priority) that are nested out because of a current interrupt. This register is only available when nesting is configured.

Table 4-231. PRU_ICSS_INTC_GNLR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 001Ch

Figure 4-99. PRU_ICSS_INTC_GNLR Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							GLB_NEST_LEVEL
R-0h							R/W-100h
7	6	5	4	3	2	1	0
GLB_NEST_LEVEL							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -*n* = value after reset

Table 4-232. PRU_ICSS_INTC_GNLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Always read as 0. Writes of 1 override the automatic nesting and set the nesting_level to the written data.
30-9	RESERVED	R	0h	Reserved
8-0	GLB_NEST_LEVEL	R/W	100h	The current global nesting level (highest channel that is nested). Writes set the nesting level. In auto nesting mode this value is updated internally unless the auto_override bit is set.

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4.5.5.5 PRU_ICSS_INTC_SISR Register (Offset = 20h) [reset = 0h]

PRU_ICSS_INTC_SISR is shown in Figure 4-100 and described in Table 4-234.

The System Interrupt Status Indexed Set Register allows setting the status of an interrupt. The interrupt to set is the index value written. This sets the Raw Status Register bit of the given index.

Table 4-233. PRU_ICSS_INTC_SISR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0020h

Figure 4-100. PRU_ICSS_INTC_SISR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0000 00h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						STATUS_SET_INDEX									
R-0000 00h						W-0h									

LEGEND: R = Read Only; W = Write Only; *-n* = value after reset

Table 4-234. PRU_ICSS_INTC_SISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0000 00h	Reserved
9-0	STATUS_SET_INDEX	W	0h	Writes set the status of the interrupt given in the index value. Reads return 0.

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4.5.5.6 PRU_ICSS_INTC_SICR Register (Offset = 24h) [reset = 0h]

PRU_ICSS_INTC_SICR is shown in Figure 4-101 and described in Table 4-236.

The System Interrupt Status Indexed Clear Register allows clearing the status of an interrupt. The interrupt to clear is the index value written. This clears the Raw Status Register bit of the given index.

Table 4-235. PRU_ICSS_INTC_SICR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0024h

Figure 4-101. PRU_ICSS_INTC_SICR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0000 00h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						STATUS_CLR_INDEX									
R-0000 00h						W-0h									

LEGEND: R = Read Only; W = Write Only; *-n* = value after reset

Table 4-236. PRU_ICSS_INTC_SICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0000 00h	Reserved
9-0	STATUS_CLR_INDEX	W	0h	Writes clear the status of the interrupt given in the index value. Reads return 0.

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4.5.5.7 PRU_ICSS_INTC_EISR Register (Offset = 28h) [reset = 0h]

PRU_ICSS_INTC_EISR is shown in Figure 4-102 and described in Table 4-238.

The System Interrupt Enable Indexed Set Register allows enabling an interrupt. The interrupt to enable is the index value written. This sets the Enable Register bit of the given index.

Table 4-237. PRU_ICSS_INTC_EISR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0028h

Figure 4-102. PRU_ICSS_INTC_EISR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0000 00h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						ENABLE_SET_INDEX									
R-0000 00h						W-0h									

LEGEND: R = Read Only; W = Write Only; *-n* = value after reset

Table 4-238. PRU_ICSS_INTC_EISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0000 00h	Reserved
9-0	ENABLE_SET_INDEX	W	0h	Writes set the enable of the interrupt given in the index value. Reads return 0.

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4.5.5.8 PRU_ICSS_INTC_EICR Register (Offset = 2Ch) [reset = 0h]

PRU_ICSS_INTC_EICR is shown in Figure 4-103 and described in Table 4-240.

The System Interrupt Enable Indexed Clear Register allows disabling an interrupt. The interrupt to disable is the index value written. This clears the Enable Register bit of the given index.

Table 4-239. PRU_ICSS_INTC_EICR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 002Ch

Figure 4-103. PRU_ICSS_INTC_EICR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0000 00h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						ENABLE_CLR_INDEX									
R-0000 00h						W-0h									

LEGEND: R = Read Only; W = Write Only; *-n* = value after reset

Table 4-240. PRU_ICSS_INTC_EICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0000 00h	Reserved
9-0	ENABLE_CLR_INDEX	W	0h	Writes clear the enable of the interrupt given in the index value. Reads return 0.

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4.5.5.9 PRU_ICSS_INTC_HIEISR Register (Offset = 34h) [reset = 0h]

PRU_ICSS_INTC_HIEISR is shown in Figure 4-104 and described in Table 4-242.

The Host Interrupt Enable Indexed Set Register allows enabling a host interrupt output. The host interrupt to enable is the index value written. This enables the host interrupt output or triggers the output again if already enabled.

Table 4-241. PRU_ICSS_INTC_HIEISR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0034h

Figure 4-104. PRU_ICSS_INTC_HIEISR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0000 00h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						HINT_ENABLE_SET_INDEX									
R-0000 00h						R/W-0h									

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-242. PRU_ICSS_INTC_HIEISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0000 00h	Reserved
9-0	HINT_ENABLE_SET_INDEX	R/W	0h	Writes set the enable of the host interrupt given in the index value. Reads return 0.

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4.5.5.10 PRU_ICSS_INTC_HIEICR Register (Offset = 38h) [reset = 0h]

PRU_ICSS_INTC_HIEICR is shown in Figure 4-105 and described in Table 4-244.

The Host Interrupt Enable Indexed Clear Register allows disabling a host interrupt output. The host interrupt to disable is the index value written. This disables the host interrupt output.

Table 4-243. PRU_ICSS_INTC_HIEICR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0038h

Figure 4-105. PRU_ICSS_INTC_HIEICR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0000 00h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						HINT_ENABLE_CLR_INDEX									
R-0000 00h						R/W-0h									

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-244. PRU_ICSS_INTC_HIEICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0000 00h	Reserved
9-0	HINT_ENABLE_CLR_INDEX	R/W	0h	Writes clear the enable of the host interrupt given in the index value. Reads return 0.

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4.5.5.11 PRU_ICSS_INTC_GPIR Register (Offset = 80h) [reset = 80000000h]

PRU_ICSS_INTC_GPIR is shown in Figure 4-106 and described in Table 4-246.

The Global Prioritized Index Register shows the interrupt number of the highest priority interrupt pending across all the host interrupts.

Table 4-245. PRU_ICSS_INTC_GPIR Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0080h

Figure 4-106. PRU_ICSS_INTC_GPIR Register

31	30	29	28	27	26	25	24
GLB_NONE	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						GLB_PRI_INTR	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
GLB_PRI_INTR							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-246. PRU_ICSS_INTC_GPIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GLB_NONE	R	1h	No Interrupt is pending. Can be used by host to test for a negative value to see if no interrupts are pending.
30-10	RESERVED	R	0000 00h	Reserved
9-0	GLB_PRI_INTR	R	0h	The currently highest priority interrupt index pending across all the host interrupts.

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4.5.5.12 PRU_ICSS_INTC_SRSR0 Register (Offset = 200h) [reset = 0h]

PRU_ICSS_INTC_SRSR0 is shown in Figure 4-107 and described in Table 4-248.

The System Interrupt Status Raw Set Register0 show the pending enabled status of the system interrupts 0 to 31. Software can write to the Status Set Registers to set a system interrupt without a hardware trigger. There is one bit per system interrupt.

Table 4-247. PRU_ICSS_INTC_SRSR0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0200h

Figure 4-107. PRU_ICSS_INTC_SRSR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAW_STATUS_31_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-248. PRU_ICSS_INTC_SRSR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RAW_STATUS_31_0	R/W	0h	System interrupt raw status and setting of the system interrupts 0 to 31. Reads return the raw status. Write a 1 in a bit position to set the status of the system interrupt. Writing a 0 has no effect.

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4.5.5.13 PRU_ICSS_INTC_SRSR1 Register (Offset = 204h) [reset = 0h]

PRU_ICSS_INTC_SRSR1 is shown in Figure 4-108 and described in Table 4-250.

The System Interrupt Status Raw Set Register1 show the pending enabled status of the system interrupts 32 to 63. Software can write to the Status Set Registers to set a system interrupt without a hardware trigger. There is one bit per system interrupt.

Table 4-249. PRU_ICSS_INTC_SRSR1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0204h

Figure 4-108. PRU_ICSS_INTC_SRSR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAW_STATUS_63_32																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-250. PRU_ICSS_INTC_SRSR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RAW_STATUS_63_32	R/W	0h	System interrupt raw status and setting of the system interrupts 32 to 63. Reads return the raw status. Write a 1 in a bit position to set the status of the system interrupt. Writing a 0 has no effect.

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4.5.5.14 PRU_ICSS_INTC_SECR0 Register (Offset = 280h) [reset = 0h]

PRU_ICSS_INTC_SECR0 is shown in Figure 4-109 and described in Table 4-252.

The System Interrupt Status Enabled Clear Register0 show the pending enabled status of the system interrupts 0 to 31. Software can write to the Status Clear Registers to clear a system interrupt after it has been serviced. If a system interrupt status is not cleared then another host interrupt may not be triggered or another host interrupt may be triggered incorrectly. There is one bit per system interrupt.

Table 4-251. PRU_ICSS_INTC_SECR0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0280h

Figure 4-109. PRU_ICSS_INTC_SECR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENA_STATUS_31_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-252. PRU_ICSS_INTC_SECR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ENA_STATUS_31_0	R/W	0h	System interrupt enabled status and clearing of the system interrupts 0 to 31. Reads return the enabled status (before enabling with the Enable Registers). Write a 1 in a bit position to clear the status of the system interrupt. Writing a 0 has no effect.

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4.5.5.15 PRU_ICSS_INTC_SECR1 Register (Offset = 284h) [reset = 0h]

PRU_ICSS_INTC_SECR1 is shown in Figure 4-110 and described in Table 4-254.

The System Interrupt Status Enabled Clear Register1 show the pending enabled status of the system interrupts 32 to 63. Software can write to the Status Clear Registers to clear a system interrupt after it has been serviced. If a system interrupt status is not cleared then another host interrupt may not be triggered or another host interrupt may be triggered incorrectly. There is one bit per system interrupt.

Table 4-253. PRU_ICSS_INTC_SECR1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0284h

Figure 4-110. PRU_ICSS_INTC_SECR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENA_STATUS_63_32																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-254. PRU_ICSS_INTC_SECR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ENA_STATUS_63_32	R/W	0h	System interrupt enabled status and clearing of the system interrupts 32 to 63. Reads return the enabled status (before enabling with the Enable Registers). Write a 1 in a bit position to clear the status of the system interrupt. Writing a 0 has no effect.

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4.5.5.16 PRU_ICSS_INTC_ESR0 Register (Offset = 300h) [reset = 0h]

PRU_ICSS_INTC_ESR0 is shown in Figure 4-111 and described in Table 4-256.

The System Interrupt Enable Set Register0 enables system interrupts 0 to 31 to trigger outputs. System interrupts that are not enabled do not interrupt the host. There is a bit per system interrupt.

Table 4-255. PRU_ICSS_INTC_ESR0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0300h

Figure 4-111. PRU_ICSS_INTC_ESR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE_SET_31_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-256. PRU_ICSS_INTC_ESR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ENABLE_SET_31_0	R/W	0h	System interrupt enables system interrupts 0 to 31. Read returns the enable value (0 = disabled, 1 = enabled). Write a 1 in a bit position to set that enable. Writing a 0 has no effect.

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4.5.5.17 PRU_ICSS_INTC_ERS1 Register (Offset = 304h) [reset = 0h]

PRU_ICSS_INTC_ESR1 is shown in Figure 4-112 and described in Table 4-258.

The System Interrupt Enable Set Register1 enables system interrupts 32 to 63 to trigger outputs. System interrupts that are not enabled do not interrupt the host. There is a bit per system interrupt.

Table 4-257. PRU_ICSS_INTC_ERS1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0304h

Figure 4-112. PRU_ICSS_INTC_ERS1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE_SET_63_32																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-258. PRU_ICSS_INTC_ERS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ENABLE_SET_63_32	R/W	0h	System interrupt enables system interrupts 32 to 63. Read returns the enable value (0 = disabled, 1 = enabled). Write a 1 in a bit position to set that enable. Writing a 0 has no effect.

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4.5.5.18 PRU_ICSS_INTC_ECR0 Register (Offset = 380h) [reset = 0h]

PRU_ICSS_INT_ECR0 is shown in Figure 4-113 and described in Table 4-260.

The System Interrupt Enable Clear Register0 disables system interrupts 0 to 31 to map to channels. System interrupts that are not enabled do not interrupt the host. There is a bit per system interrupt.

Table 4-259. PRU_ICSS_INTC_ECR0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0380h

Figure 4-113. PRU_ICSS_INTC_ECR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE_CLR_31_0																															
W-0h																															

LEGEND: W = Write Only; *-n* = value after reset

Table 4-260. PRU_ICSS_INTC_ECR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ENABLE_CLR_31_0	W	0h	System interrupt enables system interrupts 0 to 31. Write a 1 in a bit position to clear that enable. Writing a 0 has no effect.

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4.5.5.19 PRU_ICSS_INTC_ECR1 Register (Offset = 384h) [reset = 0h]

PRU_ICSS_INTC_ECR1 is shown in Figure 4-114 and described in Table 4-262.

The System Interrupt Enable Clear Register1 disables system interrupts 32 to 63 to map to channels. System interrupts that are not enabled do not interrupt the host. There is a bit per system interrupt.

Table 4-261. PRU_ICSS_INTC_ECR1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0384h

Figure 4-114. PRU_ICSS_INTC_ECR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE_CLR_63_32																															
W-0h																															

LEGEND: W = Write Only; *-n* = value after reset

Table 4-262. PRU_ICSS_INTC_ECR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ENABLE_CLR_63_32	W	0h	System interrupt enables system interrupts 32 to 63. Write a 1 in a bit position to clear that enable. Writing a 0 has no effect.

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4.5.5.20 PRU_ICSS_INTC_CMR_0 Register (Offset = 400h) [reset = 0h]

PRU_ICSS_INTC_CMR_0 is shown in Figure 4-115 and described in Table 4-264.

The Channel Map Register0 specify the channel for the system interrupts 0 to 3. There is one register per 4 system interrupts.

Table 4-263. PRU_ICSS_INTC_CMR_0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0400h

Figure 4-115. PRU_ICSS_INTC_CMR_0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_3				RESERVED				CH_MAP_2			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_1				RESERVED				CH_MAP_0			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-264. PRU_ICSS_INTC_CMR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_3	R/W	0h	Sets the channel for the system interrupt 3
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_2	R/W	0h	Sets the channel for the system interrupt 2
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_1	R/W	0h	Sets the channel for the system interrupt 1
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_0	R/W	0h	Sets the channel for the system interrupt 0

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4.5.5.21 PRU_ICSS_INTC_CMR_1 Register (Offset = 404h) [reset = 0h]

PRU_ICSS_INTC_CMR_1 is shown in Figure 4-116 and described in Table 4-266.

The Channel Map Register1 specify the channel for the system interrupts 4 to 7. There is one register per 4 system interrupts.

Table 4-265. PRU_ICSS_INTC_CMR_1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0404h

Figure 4-116. PRU_ICSS_INTC_CMR_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_7				RESERVED				CH_MAP_6			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_5				RESERVED				CH_MAP_4			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-266. PRU_ICSS_INTC_CMR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_7	R/W	0h	Sets the channel for the system interrupt 7
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_6	R/W	0h	Sets the channel for the system interrupt 6
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_5	R/W	0h	Sets the channel for the system interrupt 5
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_4	R/W	0h	Sets the channel for the system interrupt 4

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4.5.5.22 PRU_ICSS_INTC_CMR_2 Register (Offset = 408h) [reset = 0h]

PRU_ICSS_INTC_CMR_2 is shown in Figure 4-117 and described in Table 4-268.

The Channel Map Register2 specify the channel for the system interrupts 8 to 11. There is one register per 4 system interrupts.

Table 4-267. PRU_ICSS_INTC_CMR_2 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0408h

Figure 4-117. PRU_ICSS_INTC_CMR_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_11				RESERVED				CH_MAP_10			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_9				RESERVED				CH_MAP_8			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-268. PRU_ICSS_INTC_CMR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_11	R/W	0h	Sets the channel for the system interrupt 11
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_10	R/W	0h	Sets the channel for the system interrupt 10
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_9	R/W	0h	Sets the channel for the system interrupt 9
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_8	R/W	0h	Sets the channel for the system interrupt 8

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4.5.5.23 PRU_ICSS_INTC_CMR_3 Register (Offset = 40Ch) [reset = 0h]

PRU_ICSS_INTC_CMR_3 is shown in Figure 4-118 and described in Table 4-270.

The Channel Map Register3 specify the channel for the system interrupts 12 to 15. There is one register per 4 system interrupts.

Table 4-269. PRU_ICSS_INTC_CMR_3 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 040Ch

Figure 4-118. PRU_ICSS_INTC_CMR_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_15				RESERVED				CH_MAP_14			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_13				RESERVED				CH_MAP_12			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-270. PRU_ICSS_INTC_CMR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_15	R/W	0h	Sets the channel for the system interrupt 15
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_14	R/W	0h	Sets the channel for the system interrupt 14
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_13	R/W	0h	Sets the channel for the system interrupt 13
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_12	R/W	0h	Sets the channel for the system interrupt 12

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4.5.5.24 PRU_ICSS_INTC_CMR_4 Register (Offset = 410h) [reset = 0h]

PRU_ICSS_INTC_CMR_4 is shown in Figure 4-119 and described in Table 4-272.

The Channel Map Register4 specify the channel for the system interrupts 16 to 19. There is one register per 4 system interrupts.

Table 4-271. PRU_ICSS_INTC_CMR_4 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0410h

Figure 4-119. PRU_ICSS_INTC_CMR_4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_19				RESERVED				CH_MAP_18			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_17				RESERVED				CH_MAP_16			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-272. PRU_ICSS_INTC_CMR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_19	R/W	0h	Sets the channel for the system interrupt 19
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_18	R/W	0h	Sets the channel for the system interrupt 18
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_17	R/W	0h	Sets the channel for the system interrupt 17
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_16	R/W	0h	Sets the channel for the system interrupt 16

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4.5.5.25 PRU_ICSS_INTC_CMR_5 Register (Offset = 414h) [reset = 0h]

PRU_ICSS_INTC_CMR_5 is shown in Figure 4-120 and described in Table 4-274.

The Channel Map Register5 specify the channel for the system interrupts 20 to 23. There is one register per 4 system interrupts.

Table 4-273. PRU_ICSS_INTC_CMR_5 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0414h

Figure 4-120. PRU_ICSS_INTC_CMR_5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_23				RESERVED				CH_MAP_22			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_21				RESERVED				CH_MAP_20			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-274. PRU_ICSS_INTC_CMR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_23	R/W	0h	Sets the channel for the system interrupt 23
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_22	R/W	0h	Sets the channel for the system interrupt 22
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_21	R/W	0h	Sets the channel for the system interrupt 21
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_20	R/W	0h	Sets the channel for the system interrupt 20

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4.5.5.26 PRU_ICSS_INTC_CMR_6 Register (Offset = 418h) [reset = 0h]

PRU_ICSS_INTC_CMR_6 is shown in Figure 4-121 and described in Table 4-276.

The Channel Map Register6 specify the channel for the system interrupts 24 to 27. There is one register per 4 system interrupts.

Table 4-275. PRU_ICSS_INTC_CMR_6 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0418h

Figure 4-121. PRU_ICSS_INTC_CMR_6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_27				RESERVED				CH_MAP_26			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_25				RESERVED				CH_MAP_24			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-276. PRU_ICSS_INTC_CMR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_27	R/W	0h	Sets the channel for the system interrupt 27
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_26	R/W	0h	Sets the channel for the system interrupt 26
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_25	R/W	0h	Sets the channel for the system interrupt 25
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_24	R/W	0h	Sets the channel for the system interrupt 24

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4.5.5.27 PRU_ICSS_INTC_CMR_7 Register (Offset = 41Ch) [reset = 0h]

PRU_ICSS_INTC_CMR_7 is shown in Figure 4-122 and described in Table 4-278.

The Channel Map Register7 specify the channel for the system interrupts 28 to 31. There is one register per 4 system interrupts.

Table 4-277. PRU_ICSS_INTC_CMR_7 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 041Ch

Figure 4-122. PRU_ICSS_INTC_CMR_7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_31				RESERVED				CH_MAP_30			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_29				RESERVED				CH_MAP_28			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-278. PRU_ICSS_INTC_CMR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_31	R/W	0h	Sets the channel for the system interrupt 31
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_30	R/W	0h	Sets the channel for the system interrupt 30
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_29	R/W	0h	Sets the channel for the system interrupt 29
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_28	R/W	0h	Sets the channel for the system interrupt 28

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4.5.5.28 PRU_ICSS_INTC_CMR_8 Register (Offset = 420h) [reset = 0h]

PRU_ICSS_INTC_CMR_8 is shown in Figure 4-123 and described in Table 4-280.

The Channel Map Register8 specify the channel for the system interrupts 32 to 35. There is one register per 4 system interrupts.

Table 4-279. PRU_ICSS_INTC_CMR_8 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0420h

Figure 4-123. PRU_ICSS_INTC_CMR_8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_35				RESERVED				CH_MAP_34			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_33				RESERVED				CH_MAP_32			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-280. PRU_ICSS_INTC_CMR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_35	R/W	0h	Sets the channel for the system interrupt 35
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_34	R/W	0h	Sets the channel for the system interrupt 34
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_33	R/W	0h	Sets the channel for the system interrupt 33
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_32	R/W	0h	Sets the channel for the system interrupt 32

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4.5.5.29 PRU_ICSS_INTC_CMR_9 Register (Offset = 424h) [reset = 0h]

PRU_ICSS_INTC_CMR_9 is shown in Figure 4-124 and described in Table 4-282.

The Channel Map Register9 specify the channel for the system interrupts 36 to 39. There is one register per 4 system interrupts.

Table 4-281. PRU_ICSS_INTC_CMR_9 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0424h

Figure 4-124. PRU_ICSS_INTC_CMR_9 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_39				RESERVED				CH_MAP_38			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_37				RESERVED				CH_MAP_36			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-282. PRU_ICSS_INTC_CMR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_39	R/W	0h	Sets the channel for the system interrupt 39
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_38	R/W	0h	Sets the channel for the system interrupt 38
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_37	R/W	0h	Sets the channel for the system interrupt 37
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_36	R/W	0h	Sets the channel for the system interrupt 36

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4.5.5.30 PRU_ICSS_INTC_CMR_10 Register (Offset = 428h) [reset = 0h]

PRU_ICSS_INTC_CMR_10 is shown in Figure 4-125 and described in Table 4-284.

The Channel Map Register10 specify the channel for the system interrupts 40 to 43. There is one register per 4 system interrupts.

Table 4-283. PRU_ICSS_INTC_CMR_10 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0428h

Figure 4-125. PRU_ICSS_INTC_CMR_10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_43				RESERVED				CH_MAP_42			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_41				RESERVED				CH_MAP_40			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-284. PRU_ICSS_INTC_CMR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_43	R/W	0h	Sets the channel for the system interrupt 43
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_42	R/W	0h	Sets the channel for the system interrupt 42
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_41	R/W	0h	Sets the channel for the system interrupt 41
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_40	R/W	0h	Sets the channel for the system interrupt 40

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4.5.5.31 PRU_ICSS_INTC_CMR_11 Register (Offset = 42Ch) [reset = 0h]

PRU_ICSS_INTC_CMR_11 is shown in Figure 4-126 and described in Table 4-286.

The Channel Map Register11 specify the channel for the system interrupts 44 to 47. There is one register per 4 system interrupts.

Table 4-285. PRU_ICSS_INTC_CMR_11 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 042Ch

Figure 4-126. PRU_ICSS_INTC_CMR_11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_47				RESERVED				CH_MAP_46			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_45				RESERVED				CH_MAP_44			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-286. PRU_ICSS_INTC_CMR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_47	R/W	0h	Sets the channel for the system interrupt 47
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_46	R/W	0h	Sets the channel for the system interrupt 46
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_45	R/W	0h	Sets the channel for the system interrupt 45
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_44	R/W	0h	Sets the channel for the system interrupt 44

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4.5.5.32 PRU_ICSS_INTC_CMR_12 Register (Offset = 430h) [reset = 0h]

PRU_ICSS_INTC_CMR_12 is shown in Figure 4-127 and described in Table 4-288.

The Channel Map Register12 specify the channel for the system interrupts 48 to 51. There is one register per 4 system interrupts.

Table 4-287. PRU_ICSS_INTC_CMR_12 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0430h

Figure 4-127. PRU_ICSS_INTC_CMR_12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_51				RESERVED				CH_MAP_50			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_49				RESERVED				CH_MAP_48			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-288. PRU_ICSS_INTC_CMR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_51	R/W	0h	Sets the channel for the system interrupt 51
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_50	R/W	0h	Sets the channel for the system interrupt 50
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_49	R/W	0h	Sets the channel for the system interrupt 49
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_48	R/W	0h	Sets the channel for the system interrupt 48

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4.5.5.33 PRU_ICSS_INTC_CMR_13 Register (Offset = 434h) [reset = 0h]

PRU_ICSS_INTC_CMR_13 is shown in Figure 4-128 and described in Table 4-290.

The Channel Map Register13 specify the channel for the system interrupts 52 to 55. There is one register per 4 system interrupts.

Table 4-289. PRU_ICSS_INTC_CMR_13 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0434h

Figure 4-128. PRU_ICSS_INTC_CMR_13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_55				RESERVED				CH_MAP_54			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_53				RESERVED				CH_MAP_52			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-290. PRU_ICSS_INTC_CMR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_55	R/W	0h	Sets the channel for the system interrupt 55
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_54	R/W	0h	Sets the channel for the system interrupt 54
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_53	R/W	0h	Sets the channel for the system interrupt 53
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_52	R/W	0h	Sets the channel for the system interrupt 52

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4.5.5.34 PRU_ICSS_INTC_CMR_14 Register (Offset = 438h) [reset = 0h]

PRU_ICSS_INTC_CMR_14 is shown in Figure 4-129 and described in Table 4-292.

The Channel Map Register14 specify the channel for the system interrupts 56 to 59. There is one register per 4 system interrupts.

Table 4-291. PRU_ICSS_INTC_CMR_14 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0438h

Figure 4-129. PRU_ICSS_INTC_CMR_14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_59				RESERVED				CH_MAP_58			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_57				RESERVED				CH_MAP_56			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-292. PRU_ICSS_INTC_CMR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_59	R/W	0h	Sets the channel for the system interrupt 59
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_58	R/W	0h	Sets the channel for the system interrupt 58
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_57	R/W	0h	Sets the channel for the system interrupt 57
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_56	R/W	0h	Sets the channel for the system interrupt 56

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4.5.5.35 PRU_ICSS_INTC_CMR_15 Register (Offset = 43Ch) [reset = 0h]

PRU_ICSS_INTC_CMR_15 is shown in Figure 4-130 and described in Table 4-294.

The Channel Map Register15 specify the channel for the system interrupts 60 to 63. There is one register per 4 system interrupts.

Table 4-293. PRU_ICSS_INTC_CMR_15 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 043Ch

Figure 4-130. PRU_ICSS_INTC_CMR_15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				CH_MAP_63				RESERVED				CH_MAP_62			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				CH_MAP_61				RESERVED				CH_MAP_60			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-294. PRU_ICSS_INTC_CMR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	CH_MAP_63	R/W	0h	Sets the channel for the system interrupt 63
23-20	RESERVED	R	0h	Reserved
19-16	CH_MAP_62	R/W	0h	Sets the channel for the system interrupt 62
15-12	RESERVED	R	0h	Reserved
11-8	CH_MAP_61	R/W	0h	Sets the channel for the system interrupt 61
7-4	RESERVED	R	0h	Reserved
3-0	CH_MAP_60	R/W	0h	Sets the channel for the system interrupt 60

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4.5.5.36 PRU_ICSS_INTC_HMR0 Register (Offset = 800h) [reset = 0h]

PRU_ICSS_INTC_HMR0 is shown in Figure 4-131 and described in Table 4-296.

The Host Interrupt Map Register0 define the host interrupt for channels 0 to 3. There is one register per 4 channels. Channels with forced host interrupt mappings will have their fields read-only.

Table 4-295. PRU_ICSS_INTC_HMR0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0800h

Figure 4-131. PRU_ICSS_INTC_HMR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				HINT_MAP_3				RESERVED				HINT_MAP_2			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HINT_MAP_1				RESERVED				HINT_MAP_0			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-296. PRU_ICSS_INTC_HMR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	HINT_MAP_3	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 3
23-20	RESERVED	R	0h	Reserved
19-16	HINT_MAP_2	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 2
15-12	RESERVED	R	0h	Reserved
11-8	HINT_MAP_1	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 1
7-4	RESERVED	R	0h	Reserved
3-0	HINT_MAP_0	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 0

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4.5.5.37 PRU_ICSS_INTC_HMR1 Register (Offset = 804h) [reset = 0h]

PRU_ICSS_INTC_HMR1 is shown in Figure 4-132 and described in Table 4-298.

The Host Interrupt Map Register1 define the host interrupt for channels 4 to 7. There is one register per 4 channels. Channels with forced host interrupt mappings will have their fields read-only.

Table 4-297. PRU_ICSS_INTC_HMR1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0804h

Figure 4-132. PRU_ICSS_INTC_HMR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				HINT_MAP_7				RESERVED				HINT_MAP_6			
R-0h				R/W-0h				R-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HINT_MAP_5				RESERVED				HINT_MAP_4			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-298. PRU_ICSS_INTC_HMR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27-24	HINT_MAP_7	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 7
23-20	RESERVED	R	0h	Reserved
19-16	HINT_MAP_6	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 6
15-12	RESERVED	R	0h	Reserved
11-8	HINT_MAP_5	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 5
7-4	RESERVED	R	0h	Reserved
3-0	HINT_MAP_4	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 4

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4.5.5.38 PRU_ICSS_INTC_HMR2 Register (Offset = 808h) [reset = 0h]

PRU_ICSS_INTC_HMR2 is shown in Figure 4-133 and described in Table 4-300.

The Host Interrupt Map Register2 define the host interrupt for channels 8 to 9. There is one register per 4 channels. Channels with forced host interrupt mappings will have their fields read-only.

Table 4-299. PRU_ICSS_INTC_HMR2 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0808h

Figure 4-133. PRU_ICSS_INTC_HMR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				HINT_MAP_9				RESERVED				HINT_MAP_8			
R-0h				R/W-0h				R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-300. PRU_ICSS_INTC_HMR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	HINT_MAP_9	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 9
7-4	RESERVED	R	0h	Reserved
3-0	HINT_MAP_8	R/W	0h	HOST INTERRUPT MAP FOR CHANNEL 8

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4.5.5.39 PRU_ICSS_INTC_HIPIR_0 Register (Offset = 900h) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR is shown in Figure 4-134 and described in Table 4-302.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-301. PRU_ICSS_INTC_HIPIR_0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0900h

Figure 4-134. PRU_ICSS_INTC_HIPIR_0 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-302. PRU_ICSS_INTC_HIPIR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

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4.5.5.40 PRU_ICSS_INTC_HIPIR_1 Register (Offset = 904h) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR_1 is shown in Figure 4-135 and described in Table 4-304.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-303. PRU_ICSS_INTC_HIPIR_1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0904h

Figure 4-135. PRU_ICSS_INTC_HIPIR_1 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-304. PRU_ICSS_INTC_HIPIR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

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4.5.5.41 PRU_ICSS_INTC_HIPIR_2 Register (Offset = 908h) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR_2 is shown in Figure 4-136 and described in Table 4-306.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-305. PRU_ICSS_INTC_HIPIR_2 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0908h

Figure 4-136. PRU_ICSS_INTC_HIPIR_2 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-306. PRU_ICSS_INTC_HIPIR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

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4.5.5.42 PRU_ICSS_INTC_HIPIR_3 Register (Offset = 90Ch) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR_3 is shown in Figure 4-137 and described in Table 4-308.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-307. PRU_ICSS_INTC_HIPIR_3 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 090Ch

Figure 4-137. PRU_ICSS_INTC_HIPIR_3 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-308. PRU_ICSS_INTC_HIPIR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

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4.5.5.43 PRU_ICSS_INTC_HIPIR_4 Register (Offset = 910h) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR_4 is shown in Figure 4-138 and described in Table 4-310.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-309. PRU_ICSS_INTC_HIPIR_4 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0910h

Figure 4-138. PRU_ICSS_INTC_HIPIR_4 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-310. PRU_ICSS_INTC_HIPIR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

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4.5.5.44 PRU_ICSS_INTC_HIPIR_5 Register (Offset = 914h) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR_5 is shown in Figure 4-139 and described in Table 4-312.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-311. PRU_ICSS_INTC_HIPIR_5 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0914h

Figure 4-139. PRU_ICSS_INTC_HIPIR_5 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-312. PRU_ICSS_INTC_HIPIR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

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4.5.5.45 PRU_ICSS_INTC_HIPIR_6 Register (Offset = 918h) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR_6 is shown in Figure 4-140 and described in Table 4-314.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-313. PRU_ICSS_INTC_HIPIR_6 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0918h

Figure 4-140. PRU_ICSS_INTC_HIPIR_6 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-314. PRU_ICSS_INTC_HIPIR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

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4.5.5.46 PRU_ICSS_INTC_HIPIR_7 Register (Offset = 91Ch) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR_7 is shown in Figure 4-141 and described in Table 4-316.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-315. PRU_ICSS_INTC_HIPIR_7 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 091Ch

Figure 4-141. PRU_ICSS_INTC_HIPIR_7 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-316. PRU_ICSS_INTC_HIPIR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

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4.5.5.47 PRU_ICSS_INTC_HIPIR_8 Register (Offset = 920h) [reset = 80000000h]

PRU_ICSS_INTC_HIPIR_8 is shown in Figure 4-142 and described in Table 4-318.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-317. PRU_ICSS_INTC_HIPIR_8 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0920h

Figure 4-142. PRU_ICSS_INTC_HIPIR_8 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-318. PRU_ICSS_INTC_HIPIR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

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4.5.5.48 PRU_ICSS_INTC_HIPIR_9 Register (Offset = 924h) [reset = 80000000h]

PRU_ICS_INTC_HIPIR_9 is shown in Figure 4-143 and described in Table 4-320.

The Host Interrupt Prioritized Index Register_j (where j=0 to 9) shows the highest priority current pending interrupt for the host interrupt j. There is one register per host interrupt.

Table 4-319. PRU_ICSS_INTC_HIPIR_9 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0924h

Figure 4-143. PRU_ICSS_INTC_HIPIR_9 Register

31	30	29	28	27	26	25	24
NONE_HINT	RESERVED						
R-1h	R-0000 00h						
23	22	21	20	19	18	17	16
RESERVED							
R-0000 00h							
15	14	13	12	11	10	9	8
RESERVED						PRI_HINT	
R-0000 00h						R-0h	
7	6	5	4	3	2	1	0
PRI_HINT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 4-320. PRU_ICSS_INTC_HIPIR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NONE_HINT	R	1h	No pending interrupt.
30-10	RESERVED	R	0000 00h	Reserved
9-0	PRI_HINT	R	0h	HOST INT j PRIORITIZED INTERRUPT. Interrupt number of the highest priority pending interrupt for this host interrupt.

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4.5.5.49 PRU_ICSS_INTC_SIPR0 Register (Offset = D00h) [reset = 1h]

PRU_ICSS_INTC_SIPR0 is shown in Figure 4-144 and described in Table 4-322.

The System Interrupt Polarity Register0 define the polarity of the system interrupts 0 to 31. There is a polarity for each system interrupt. The polarity of all system interrupts is active high; always write 1 to the bits of this register.

Table 4-321. PRU_ICSS_INTC_SIPR0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0D00h

Figure 4-144. PRU_ICSS_INTC_SIPR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POLARITY_31_0																															
R/W-1h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-322. PRU_ICSS_INTC_SIPR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	POLARITY_31_0	R/W	1h	Interrupt polarity of the system interrupts 0 to 31. 0h: Active low. 1h: Active high.

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4.5.5.50 PRU_ICSS_INTC_SIPR1 Register (Offset = D04h) [reset = 1h]

PRU_ICSS_INTC_SIPR1 is shown in Figure 4-145 and described in Table 4-324.

The System Interrupt Polarity Register1 define the polarity of the system interrupts 32 to 63. There is a polarity for each system interrupt. The polarity of all system interrupts is active high; always write 1 to the bits of this register.

Table 4-323. PRU_ICSS_INTC_SIPR1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0D04h

Figure 4-145. PRU_ICSS_INTC_SIPR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POLARITY_63_32																															
R/W-1h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-324. PRU_ICSS_INTC_SIPR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	POLARITY_63_32	R/W	1h	Interrupt polarity of the system interrupts 32 to 63. 0h: Active low. 1h: Active high.

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4.5.5.51 PRU_ICSS_INTC_SITR0 Register (Offset = D80h) [reset = 0h]

PRU_ICSS_INTC_SITR0 is shown in Figure 4-146 and described in Table 4-326.

The System Interrupt Type Register0 define the type of the system interrupts 0 to 31. There is a type for each system interrupt. The type of all system interrupts is pulse; always write 0 to the bits of this register.

Table 4-325. PRU_ICSS_INTC_SITR0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0D80h

Figure 4-146. PRU_ICSS_INTC_SITR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TYPE_31_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-326. PRU_ICSS_INTC_SITR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TYPE_31_0	R/W	0h	Interrupt type of the system interrupts 0 to 31. 0h: Level or pulse interrupt. 1h: Edge interrupt (required edge detect).

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4.5.5.52 PRU_ICSS_INTC_SITR1 Register (Offset = D84h) [reset = 0h]

PRU_ICSS_INTC_SITR1 is shown in Figure 4-147 and described in Table 4-328.

The System Interrupt Type Register1 define the type of the system interrupts 32 to 63. There is a type for each system interrupt. The type of all system interrupts is pulse; always write 0 to the bits of this register.

Table 4-327. PRU_ICSS_INTC_SITR1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 0D84h

Figure 4-147. PRU_ICSS_INTC_SITR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TYPE_63_32																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-328. PRU_ICSS_INTC_SITR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TYPE_63_32	R/W	0h	Interrupt type of the system interrupts 32 to 63. 0h Level or pulse interrupt. 1h: Edge interrupt (required edge detect).

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4.5.5.53 PRU_ICSS_INTC_HINLR_0 Register (Offset = 1100h) [reset = 100h]

PRU_ICSS_INTC_HINLR_0 is shown in Figure 4-148 and described in Table 4-330.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-329. PRU_ICSS_INTC_HINLR_0 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1100h

Figure 4-148. PRU_ICSS_INTC_HINLR_0 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-330. PRU_ICSS_INTC_HINLR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

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4.5.5.54 PRU_ICSS_INTC_HINLR_1 Register (Offset = 1104h) [reset = 100h]

PRU_ICSS_INTC_HINLR_1 is shown in Figure 4-149 and described in Table 4-332.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-331. PRU_ICSS_INTC_HINLR_1 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1104h

Figure 4-149. PRU_ICSS_INTC_HINLR_1 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-332. PRU_ICSS_INTC_HINLR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

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4.5.5.55 PRU_ICSS_INTC_HINLR_2 Register (Offset = 1108h) [reset = 100h]

PRU_ICSS_INTC_HINLR_2 is shown in Figure 4-150 and described in Table 4-334.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-333. PRU_ICSS_INTC_HINLR_2 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1108h

Figure 4-150. PRU_ICSS_INTC_HINLR_2 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-334. PRU_ICSS_INTC_HINLR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

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4.5.5.56 PRU_ICSS_INTC_HINLR_3 Register (Offset = 110Ch) [reset = 100h]

PRU_ICSS_INTC_HINLR_3 is shown in Figure 4-151 and described in Table 4-336.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-335. PRU_ICSS_INTC_HINLR_3 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 110Ch

Figure 4-151. PRU_ICSS_INTC_HINLR_3 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-336. PRU_ICSS_INTC_HINLR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

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4.5.5.57 PRU_ICSS_INTC_HINLR_4 Register (Offset = 1110h) [reset = 100h]

PRU_ICSS_INTC_HINLR_4 is shown in Figure 4-152 and described in Table 4-338.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-337. PRU_ICSS_INTC_HINLR_4 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1110h

Figure 4-152. PRU_ICSS_INTC_HINLR_4 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-338. PRU_ICSS_INTC_HINLR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

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4.5.5.58 PRU_ICSS_INTC_HINLR_5 Register (Offset = 1114h) [reset = 100h]

PRU_ICSS_INTC_HINLR_5 is shown in Figure 4-153 and described in Table 4-340.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-339. PRU_ICSS_INTC_HINLR_5 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1114h

Figure 4-153. PRU_ICSS_INTC_HINLR_5 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-340. PRU_ICSS_INTC_HINLR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

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4.5.5.59 PRU_ICSS_INTC_HINLR_6 Register (Offset = 1118h) [reset = 100h]

PRU_ICSS_INTC_HINLR_6 is shown in Figure 4-154 and described in Table 4-342.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-341. PRU_ICSS_INTC_HINLR_6 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1118h

Figure 4-154. PRU_ICSS_INTC_HINLR_6 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-342. PRU_ICSS_INTC_HINLR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

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4.5.5.60 PRU_ICSS_INTC_HINLR_7 Register (Offset = 111Ch) [reset = 100h]

PRU_ICSS_INTC_HINLR_7 is shown in Figure 4-155 and described in Table 4-344.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-343. PRU_ICSS_INTC_HINLR_7 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 111Ch

Figure 4-155. PRU_ICSS_INTC_HINLR_7 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-344. PRU_ICSS_INTC_HINLR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

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4.5.5.61 PRU_ICSS_INTC_HINLR_8 Register (Offset = 1120h) [reset = 100h]

PRU_ICSS_INTC_HINLR_8 is shown in Figure 4-156 and described in Table 4-346.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-345. PRU_ICSS_INTC_HINLR_8 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1120h

Figure 4-156. PRU_ICSS_INTC_HINLR_8 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-346. PRU_ICSS_INTC_HINLR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

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4.5.5.62 PRU_ICSS_INTC_HINLR_9 Register (Offset = 1124h) [reset = 100h]

PRU_ICSS_INTC_HINLR_9 is shown in Figure 4-157 and described in Table 4-348.

The Host Interrupt Nesting Level Register_j (where j=0 to 9) display and control the nesting level for host interrupt j. The nesting level controls which channel and lower priority channels are nested. There is one register per host interrupt.

Table 4-347. PRU_ICSS_INTC_HINLR_9 Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1124h

Figure 4-157. PRU_ICSS_INTC_HINLR_9 Register

31	30	29	28	27	26	25	24
AUTO_OVERRIDE	RESERVED						
W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							NEST_HINT
R-0h							R/W-100h
7	6	5	4	3	2	1	0
NEST_HINT							
R/W-100h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; *-n* = value after reset

Table 4-348. PRU_ICSS_INTC_HINLR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUTO_OVERRIDE	W	0h	Reads return 0. Writes of a 1 override the auto updating of the nesting_level and use the write data.
30-9	RESERVED	R	0h	Reserved
8-0	NEST_HINT	R/W	100h	Reads return the current nesting level for the host interrupt. Writes set the nesting level for the host interrupt. In auto mode the value is updated internally unless the auto_override is set and then the write data is used.

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4.5.5.63 PRU_ICSS_INTC_HIER Register (Offset = 1500h) [reset = 0h]

PRU_ICSS_INTC_HIER is shown in Figure 4-158 and described in Table 4-350.

The Host Interrupt Enable Registers enable or disable individual host interrupts. These work separately from the global enables. There is one bit per host interrupt. These bits are updated when writing to the Host Interrupt Enable Index Set and Host Interrupt Enable Index Clear registers.

Table 4-349. PRU_ICSS_INTC_HIER Instances

Instance	Physical Address
PRU_ICSS_INTC	4802 1500h

Figure 4-158. PRU_ICSS_INTC_HIER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0000 00h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						ENABLE_HINT									
R-0000 00h						R/W-0h									

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-350. PRU_ICSS_INTC_HIER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0000 00h	Reserved
9-0	ENABLE_HINT	R/W	0h	The enable of the host interrupts (one per bit). 0h: Disabled 1h: Enabled

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4.5.6 PRU_ICSS_UART Registers

PRU_ICSS_UART Registers lists the memory-mapped registers for the PRU-ICSS_UART module. All register offset addresses not listed in PRU_ICSS_UART Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-351. PRU-ICSS_UART Instances

Instance	Base Address
PRU_ICSS_UART	4802 8000h

Table 4-352. PRU-ICSS_UART Registers

Offset	Acronym	Register Name	PRU_ICSS_UART Physical Address
0h	PRU_ICSS_UART_RBR_THR	Transmitter Holding Register	4802 8000h
4h	PRU_ICSS_UART_INTERRUPT_ENABLE	Interrupt Enable Register	4802 8004h
8h	PRU_ICSS_UART_INTERRUPT_IDENTIFICATION_FIFO_CONTROL	Interrupt Identification Register/ FIFO Control Register	4802 8008h
Ch	PRU_ICSS_UART_LINE_CONTROL	Line Control Register	4802 800Ch
10h	PRU_ICSS_UART_MODEM_CONTROL	Modem Control Register	4802 8010h
14h	PRU_ICSS_UART_LINE_STATUS	Line Status Register	4802 8014h
18h	PRU_ICSS_UART_MODEM_STATUS	Modem Status Register	4802 8018h
1Ch	PRU_ICSS_UART_SCRATCH	Scratch Register	4802 801Ch
20h	PRU_ICSS_UART_DIVISOR_LSB	Divisor Latch (LSB)	4802 8020h
24h	PRU_ICSS_UART_UART_DIVISOR_MSB	Divisor Latch (MSB)	4802 8024h
28h	PRU_ICSS_UART_PERIPHERAL_ID	Peripheral ID Register	4802 8028h
2Ch	RESERVED		4802 802Ch
30h	PRU_ICSS_UART_POWER_MANAGEMENT_AND_EMULATION	Power Management and Emulation Register	4802 8030h
34h	PRU_ICSS_UART_MODE_DEFINITION	Mode Definition Register	4802 8034h

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4.5.6.1 PRU_ICSS_UART_RBR_THR Register (Offset = 0h) [reset = 0h]

PRU_ICSS_UART_RBR_THR is shown in Figure 4-159 and described in Table 4-354.

Return to Summary Table.

In the non-FIFO mode, when a character is placed in Receiver buffer register and the receiver data-ready interrupt is enabled (DR = 1 in Interrupt identification register), an interrupt is generated. This interrupt is cleared when the character is read from Receiver buffer register. In the FIFO mode, the interrupt is generated when the FIFO is filled to the trigger level selected in the FIFO control register, and it is cleared when the FIFO contents drop below the trigger level.
In the non-FIFO mode, if Transmitter holding register is empty and the THR empty (THRE) interrupt is enabled (ETBEI = 1 in Interrupt enable register), an interrupt is generated. This interrupt is cleared when a character is loaded into Transmitter holding register or the Interrupt identification register is read. In the FIFO mode, the interrupt is generated when the transmitter FIFO is empty, and it is cleared when at least one byte is loaded into the FIFO or Interrupt identification register is read.

Table 4-353. PRU_ICSS_UART_RBR_THR Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8000h

Figure 4-159. PRU_ICSS_UART_RBR_THR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DATA							
R-0h																								RW-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-354. PRU_ICSS_UART_RBR_THR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DATA	RW	0h	**Read:** Read Receive Buffer Register **Write:** Write Transmitter Holding Register

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4.5.6.2 PRU_ICSS_UART_INTERRUPT_ENABLE Register (Offset = 4h) [reset = 0h]

PRU_ICSS_UART_INTERRUPT_ENABLE is shown in Figure 4-160 and described in Table 4-356.

Return to Summary Table.

The Interrupt enable register is used to individually enable or disable each type of interrupt request that can be generated by the UART. Each interrupt request that is enabled in Interrupt enable register is forwarded to the CPU.

Table 4-355. PRU_ICSS_UART_INTERRUPT_ENABLE Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8004h

Figure 4-160. PRU_ICSS_UART_INTERRUPT_ENABLE Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				EDSSI	ELSI	ETBEI	ERBI
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-356. PRU_ICSS_UART_INTERRUPT_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	EDSSI	R/W	0h	Enable Modem Status Interrupt
2	ELSI	R/W	0h	Receiver line status interrupt enable. 0h: Receiver line status interrupt is disabled. 1h: Receiver line status interrupt is enabled.
1	ETBEI	R/W	0h	Transmitter holding register empty interrupt enable. 0h: Transmitter holding register empty interrupt is disabled. 1h: Transmitter holding register empty interrupt is enabled.
0	ERBI	R/W	0h	Receiver data available interrupt and character timeout indication interrupt enable. 0h: Receiver data available interrupt and character timeout indication interrupt is disabled. 1h: Receiver data available interrupt and character timeout indication interrupt is enabled.

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4.5.6.3 PRU_ICSS_UART_INTERRUPT_IDENTIFICATION_FIFO_CONTROL Register (Offset = 8h) [reset = 1h]

PRU_ICSS_UART_INTERRUPT_IDENTIFICATION_FIFO_CONTROL is shown in Figure 4-161 and described in Table 4-358.

Return to Summary Table.

The Interrupt identification register is a read-only register at the same address as the FIFO control register, which is a write-only register. When an interrupt is generated and enabled in the Interrupt enable register, Interrupt identification register indicates that an interrupt is pending in the IPEND bit and encodes the type of interrupt in the INTID bits. Reading Interrupt identification register clears any THR empty (THRE) interrupts that are pending. The FIFOEN bit in Interrupt identification register can be checked to determine whether the UART is in the FIFO mode or the non-FIFO mode.
Use FIFO control register to enable and clear the FIFOs and to select the receiver FIFO trigger level. The FIFOEN bit in FIFO control register must be set to 1 before other FIFO control register bits are written to or the FIFO control register bits are not programmed.

Table 4-357. PRU_ICSS_UART_INTERRUPT_IDENTIFICATION_FIFO_CONTROL Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8008h

Figure 4-161. PRU_ICSS_UART_INTERRUPT_IDENTIFICATION_FIFO_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
FIFOEN_RXFIFTL		RESERVED		INTID			IPEND_FIFOEN
RW-0h		R-0h		RW-0h			RW-1h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-358. PRU_ICSS_UART_INTERRUPT_IDENTIFICATION_FIFO_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved

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Table 4-358. PRU_ICSS_UART_INTERRUPT_IDENTIFICATION_FIFO_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	FIFOEN_RXFIFTL	RW	0h	**Read:** FIFOs enabled. 0h: Non-FIFO mode 1h-2h: Reserved 3h: FIFOs are enabled. FIFOEN bit in the FIFO control register (FCR) is set to 1.
				Write: Receiver FIFO trigger level. RXFIFTL sets the trigger level for the receiver FIFO. When the trigger level is reached, a receiver data-ready interrupt is generated (if the interrupt request is enabled). Once the FIFO drops below the trigger level, the interrupt is cleared. 0h: 1 byte 1h: 4 bytes 2h: 8 bytes 3h: 14 bytes
5-4	RESERVED	R	0h	Reserved
3-1	INTID	RW	0h	**Read:** Interrupt type. See . 0h: Reserved 1h: Transmitter holding register empty (priority 3) 2h: Receiver data available (priority 2) 3h: Receiver line status (priority 1, highest) 4h-5h: Reserved 6h: Character timeout indication (priority 2) 7h: Reserved
				Write: **Bit 3: DMAMODE1:** DMA MODE1 enable if FIFOs are enabled. Always write 1 to DMAMODE1. After a hardware reset, change DMAMODE1 from 0 to 1. DMAMODE1 = 1 is a requirement for proper communication between the UART and the EDMA controller. 0h: DMA MODE1 is disabled. 1h: DMA MODE1 is enabled. **Bit 2: TXCLR:** Transmitter FIFO clear. Write a 1 to TXCLR to clear the bit. 0h: No effect. 1h: Clears transmitter FIFO and resets the transmitter FIFO counter. The shift register is not cleared. **Bit 1: RXCLR:** Receiver FIFO clear. Write a 1 to RXCLR to clear the bit. 0h: No effect. 1h: Clears receiver FIFO and resets the receiver FIFO counter. The shift register is not cleared.
0	IPEND_FIFOEN	RW	1h	**Read:** Interrupt pending. When any UART interrupt is generated and is enabled in IER, IPEND is forced to 0. IPEND remains 0 until all pending interrupts are cleared or until a hardware reset occurs. If no interrupts are enabled, IPEND is never forced to 0. 0h: Interrupts pending. 1h: No interrupts pending.
				Write: Transmitter and receiver FIFOs mode enable. FIFOEN must be set before other FCR bits are written to or the FCR bits are not programmed. Clearing this bit clears the FIFO counters. 0h: Non-FIFO mode. The transmitter and receiver FIFOs are disabled, and the FIFO pointers are cleared. 1h: FIFO mode. The transmitter and receiver FIFOs are enabled.

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4.5.6.4 PRU_ICSS_UART_LINE_CONTROL Register (Offset = Ch) [reset = 0h]

PRU_ICSS_UART_LINE_CONTROL is shown in Figure 4-162 and described in Table 4-360.

Return to Summary Table.

The system programmer controls the format of the asynchronous data communication exchange by using Line control register. In addition, the programmer can retrieve, inspect, and modify the content of line control register; this eliminates the need for separate storage of the line characteristics in system memory.

Table 4-359. PRU_ICSS_UART_LINE_CONTROL Instances

Instance	Physical Address
PRU_ICSS_UART	4802 800Ch

Figure 4-162. PRU_ICSS_UART_LINE_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
DLAB	BC	SP	EPS	PEN	STB	WLS1	WLS0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-360. PRU_ICSS_UART_LINE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	DLAB	R/W	0h	Divisor latch access bit. The divisor latch registers (DLL and DLH) can be accessed at dedicated addresses or at addresses shared by RBR, THR, and IER. Using the shared addresses requires toggling DLAB to change which registers are selected. If you use the dedicated addresses, you can keep DLAB = 0. 0h: Allows access to the receiver buffer register (RBR), the transmitter holding register (THR), and the interrupt enable register (IER) selected. At the address shared by RBR, THR, and DLL, the CPU can read from RBR and write to THR. At the address shared by IER and DLH, the CPU can read from and write to IER. 1h: Allows access to the divisor latches of the baud generator during a read or write operation (DLL and DLH). At the address shared by RBR, THR, and DLL, the CPU can read from and write to DLL. At the address shared by IER and DLH, the CPU can read from and write to DLH.
6	BC	R/W	0h	Break Control. 0h: Break condition is disabled. 1h: Break condition is transmitted to the receiving UART. A break condition is a condition where the UARTn_TXD signal is forced to the spacing (cleared) state.

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Table 4-360. PRU_ICSS_UART_LINE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SP	R/W	0h	Stick parity. The SP bit works in conjunction with the EPS and PEN bits. The relationship between the SP, EPS, and PEN bits is summarized in . 0h: Stick parity is disabled. 1h: Stick parity is enabled. • When odd parity is selected (EPS = 0), the PARITY bit is transmitted and checked as set. • When even parity is selected (EPS = 1), the PARITY bit is transmitted and checked as cleared.
4	EPS	R/W	0h	Even parity select. Selects the parity when parity is enabled (PEN = 1). The EPS bit works in conjunction with the SP and PEN bits. The relationship between the SP, EPS, and PEN bits is summarized in . 0h: Odd parity is selected (an odd number of logic 1s is transmitted or checked in the data and PARITY bits). 1h: Even parity is selected (an even number of logic 1s is transmitted or checked in the data and PARITY bits).
3	PEN	R/W	0h	Parity enable. The PEN bit works in conjunction with the SP and EPS bits. The relationship between the SP, EPS, and PEN bits is summarized in . 0h: No PARITY bit is transmitted or checked. 1h: Parity bit is generated in transmitted data and is checked in received data between the last data word bit and the first STOP bit.
2	STB	R/W	0h	Number of STOP bits generated. STB specifies 1, 1.5, or 2 STOP bits in each transmitted character. When STB = 1, the WLS bit determines the number of STOP bits. The receiver clocks only the first STOP bit, regardless of the number of STOP bits selected. The number of STOP bits generated is summarized in . 0h: 1 STOP bit is generated. 1h: WLS bit determines the number of STOP bits: • When WLS = 0, 1.5 STOP bits are generated. • When WLS = 1h, 2h, or 3h, 2 STOP bits are generated.
1-0	WLS	R/W	0h	Word length select. Number of bits in each transmitted or received serial character. When STB = 1, the WLS bit determines the number of STOP bits. 0h: 5 bits 1h: 6 bits 2h: 7 bits 3h: 8 bits

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4.5.6.5 PRU_ICSS_UART_MODEM_CONTROL Register (Offset = 10h) [reset = 0h]

PRU_ICSS_UART_MODEM_CONTROL is shown in Figure 4-163 and described in Table 4-362.

Return to Summary Table.

The Modem control register provides the ability to enable/disable the autoflow functions, and enable/disable the loopback function for diagnostic purposes.

Table 4-361. PRU_ICSS_UART_MODEM_CONTROL Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8010h

Figure 4-163. PRU_ICSS_UART_MODEM_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		AFE	LOOP	OUT2	OUT1	RTS	RESERVED
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-362. PRU_ICSS_UART_MODEM_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	AFE	R/W	0h	Autoflow control enable. Autoflow control allows the $\overline{\text{UARTn\_RTS}}$ and $\overline{\text{UARTn\_CTS}}$ signals to provide handshaking between UARTs during data transfer. When AFE = 1, the RTS bit determines the autoflow control enabled. Note that all UARTs do not support this feature, see your device-specific data manual for supported features. If this feature is not available, this bit is reserved in this device and should be cleared to 0. 0h: Autoflow control is disabled. 1h:Autoflow control is enabled: • When RTS = 0, $\overline{\text{UARTn\_CTS}}$ is only enabled. • When RTS = 1, $\overline{\text{UARTn\_RTS}}$ and $\overline{\text{UARTn\_CTS}}$ are enabled.
4	LOOP	R/W	0h	Loop back mode enable. LOOP is used for the diagnostic testing using the loop back feature. 0h: Loop back mode is disabled. 1h: Loop back mode is enabled. When LOOP is set, the following occur: • The UARTn_TXD signal is set high. • The UARTn_RXD pin is disconnected. • The output of the transmitter shift register (TSR) is lopped back in to the receiver shift register (RSR) input.

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Table 4-362. PRU_ICSS_UART_MODEM_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OUT2	R/W	0h	OUT2 Control Bit
2	OUT1	R/W	0h	OUT1 Control Bit
1	RTS	R/W	0h	RTS control. When AFE = 1, the RTS bit determines the autoflow control enabled. Note that all UARTs do not support this feature, see your device-specific data manual for supported features. If this feature is not available, this bit is reserved in this device and should be cleared to 0. 0h: $\overline{\text{UARTn\_RTS}}$ is disabled, $\overline{\text{UARTn\_CTS}}$ is only enabled. 1h: $\overline{\text{UARTn\_RTS}}$ and $\overline{\text{UARTn\_CTS}}$ are enabled.
0	RESERVED	R	0h	Reserved

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4.5.6.6 PRU_ICSS_UART_LINE_STATUS Register (Offset = 14h) [reset = 60h]

PRU_ICSS_UART_LINE_STATUS is shown in Figure 4-164 and described in Table 4-364.

Return to Summary Table.

The Line status register provides information to the CPU concerning the status of data transfers. Line status register is intended for read operations only; do not write to this register. Bits 1 through 4 record the error conditions that produce a receiver line status interrupt.

Table 4-363. PRU_ICSS_UART_LINE_STATUS Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8014h

Figure 4-164. PRU_ICSS_UART_LINE_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RXFIFOE	TEMT	THRE	BI	FE	PE	OE	DR
R-0h	R-1h	R-1h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-364. PRU_ICSS_UART_LINE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	RXFIFOE	R	0h	Receiver FIFO error. **In non-FIFO mode:** 0h: There has been no error, or RXFIFOE was cleared because the CPU read the erroneous character from the receiver buffer register (RBR). 1h: There is a parity error, framing error, or break indicator in the receiver buffer register (RBR). **In FIFO mode:** 0h: There has been no error, or RXFIFOE was cleared because the CPU read the erroneous character from the receiver FIFO and there are no more errors in the receiver FIFO. 1h: At least one parity error, framing error, or break indicator in the receiver FIFO.

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Table 4-364. PRU_ICSS_UART_LINE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TEMT	R	1h	Transmitter empty (TEMT) indicator. **In non-FIFO mode:** 0h: Either the transmitter holding register (THR) or the transmitter shift register (TSR) contains a data character. 1h: Both the transmitter holding register (THR) and the transmitter shift register (TSR) are empty.
				In FIFO mode: 0h: Either the transmitter FIFO or the transmitter shift register (TSR) contains a data character. 1h: Both the transmitter FIFO and the transmitter shift register (TSR) are empty.
5	THRE	R	1h	Transmitter holding register empty (THRE) indicator. If the THRE bit is set and the corresponding interrupt enable bit is set (ETBEI = 1 in IER), an interrupt request is generated. **In non-FIFO mode:** 0h: Transmitter holding register (THR) is not empty. THR has been loaded by the CPU. 1h: Transmitter holding register (THR) is empty (ready to accept a new character). The content of THR has been transferred to the transmitter shift register (TSR).
				In FIFO mode: 0h: Transmitter FIFO is not empty. At least one character has been written to the transmitter FIFO. You can write to the transmitter FIFO if it is not full. 1h: Transmitter FIFO is empty. The last character in the FIFO has been transferred to the transmitter shift register (TSR).
4	BI	R	0h	Break indicator. The BI bit is set whenever the receive data input (UARTn_RXD) was held low for longer than a full-word transmission time. A full-word transmission time is defined as the total time to transmit the START, data, PARITY, and STOP bits. If the BI bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated. **In non-FIFO mode:** 0h: No break has been detected, or the BI bit was cleared because the CPU read the erroneous character from the receiver buffer register (RBR). 1h: A break has been detected with the character in the receiver buffer register (RBR).
				In FIFO mode: 0h: No break has been detected, or the BI bit was cleared because the CPU read the erroneous character from the receiver FIFO and the next character to be read from the FIFO has no break indicator. 1h: A break has been detected with the character at the top of the receiver FIFO.

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Table 4-364. PRU_ICSS_UART_LINE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	FE	R	0h	Framing error (FE) indicator. A framing error occurs when the received character does not have a valid STOP bit. In response to a framing error, the UART sets the FE bit and waits until the signal on the RX pin goes high. Once the RX signal goes high, the receiver is ready to detect a new START bit and receive new data. If the FE bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated. **In non-FIFO mode:** 0h: No framing error has been detected, or the FE bit was cleared because the CPU read the erroneous data from the receiver buffer register (RBR). 1h: A framing error has been detected with the character in the receiver buffer register (RBR).
				In FIFO mode: 0h: No framing error has been detected, or the FE bit was cleared because the CPU read the erroneous data from the receiver FIFO and the next character to be read from the FIFO has no framing error. 1h: A framing error has been detected with the character at the top of the receiver FIFO.
2	PE	R	0h	Parity error (PE) indicator. A parity error occurs when the parity of the received character does not match the parity selected with the EPS bit in the line control register (LCR). If the PE bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated. **In non-FIFO mode:** 0h: No parity error has been detected, or the PE bit was cleared because the CPU read the erroneous data from the receiver buffer register (RBR). 1h: A parity error has been detected with the character in the receiver buffer register (RBR).
				In FIFO mode: 0h: No parity error has been detected, or the PE bit was cleared because the CPU read the erroneous data from the receiver FIFO and the next character to be read from the FIFO has no parity error. 1h: A parity error has been detected with the character at the top of the receiver FIFO.

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Table 4-364. PRU_ICSS_UART_LINE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OE	R	0h	Overrun error (OE) indicator. An overrun error in the non-FIFO mode is different from an overrun error in the FIFO mode. If the OE bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated. **In non-FIFO mode:** 0h: No overrun error has been detected, or the OE bit was cleared because the CPU read the content of the line status register (LSR). 1h: Overrun error has been detected. Before the character in the receiver buffer register (RBR) could be read, it was overwritten by the next character arriving in RBR.
				In FIFO mode: 0h: No overrun error has been detected, or the OE bit was cleared because the CPU read the content of the line status register (LSR). 1h: Overrun error has been detected. If data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An overrun error is indicated to the CPU as soon as it happens. The new character overwrites the character in the shift register, but it is not transferred to the FIFO.
0	DR	R	0h	Data-ready (DR) indicator for the receiver. If the DR bit is set and the corresponding interrupt enable bit is set (ERBI = 1 in IER), an interrupt request is generated. **In non-FIFO mode:** 0h: Data is not ready, or the DR bit was cleared because the character was read from the receiver buffer register (RBR). 1h: Data is ready. A complete incoming character has been received and transferred into the receiver buffer register (RBR).
				In FIFO mode: 0h: Data is not ready, or the DR bit was cleared because all of the characters in the receiver FIFO have been read. 1h: Data is ready. There is at least one unread character in the receiver FIFO. If the FIFO is empty, the DR bit is set as soon as a complete incoming character has been received and transferred into the FIFO. The DR bit remains set until the FIFO is empty again.

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4.5.6.7 PRU_ICSS_UART_MODEM_STATUS Register (Offset = 18h) [reset = 0h]

PRU_ICSS_UART_MODEM_STATUS is shown in Figure 4-165 and described in Table 4-366.

Return to Summary Table.

The Modem status register provides information to the CPU concerning the status of modem control signals. Modem status register is intended for read operations only; do not write to this register.

Table 4-365. PRU_ICSS_UART_MODEM_STATUS Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8018h

Figure 4-165. PRU_ICSS_UART_MODEM_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CD	RI	DSR	CTS	DCD	TERI	DDSR	DCTS
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-366. PRU_ICSS_UART_MODEM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	CD	R	0h	Complement of the Carrier Detect input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 3 (OUT2)..
6	RI	R	0h	Complement of the Ring Indicator input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 2 (OUT1).
5	DSR	R	0h	Complement of the Data Set Ready input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 0 (DTR).
4	CTS	R	0h	Complement of the Clear To Send input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 1 (RTS).
3	DCD	R	0h	Change in DCD indicator bit. DCD indicates that the DCD input has changed state since the last time it was read by the CPU. When DCD is set and the modem status interrupt is enabled, a modem status interrupt is generated.
2	TERI	R	0h	Trailing edge of RI (TERI) indicator bit. TERI indicates that the RI input has changed from a low to a high. When TERI is set and the modem status interrupt is enabled, a modem status interrupt is generated.

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Table 4-366. PRU_ICSS_UART_MODEM_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DDSR	R	0h	Change in DSR indicator bit. DDSR indicates that the DSR input has changed state since the last time it was read by the CPU. When DDSR is set and the modem status interrupt is enabled, a modem status interrupt is generated.
0	DCTS	R	0h	Change in CTS indicator bit. DCTS indicates that the CTS input has changed state since the last time it was read by the CPU. When DCTS is set (autoflow control is not enabled and the modem status interrupt is enabled), a modem status interrupt is generated. When autoflow control is enabled, no interrupt is generated.

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4.5.6.8 PRU_ICSS_UART_SCRATCH Register (Offset = 1Ch) [reset = 0h]

PRU_ICSS_UART_SCRATCH is shown in Figure 4-166 and described in Table 4-368.

Return to Summary Table.

The Scratch Pad register is intended for programmer's use as a scratch pad. It temporarily holds the programmer's data without affecting UART operation.

Table 4-367. PRU_ICSS_UART_SCRATCH Instances

Instance	Physical Address
PRU_ICSS_UART	4802 801Ch

Figure 4-166. PRU_ICSS_UART_SCRATCH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DATA							
R-0h																								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-368. PRU_ICSS_UART_SCRATCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DATA	R/W	0h	These bits are intended for the programmer's use as a scratch pad in the sense that it temporarily holds the programmer's data without affecting any other UART operation.

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4.5.6.9 PRU_ICSS_UART_DIVISOR_LSB Register (Offset = 20h) [reset = 0h]

PRU_ICSS_UART_DIVISOR_LSB is shown in Figure 4-167 and described in Table 4-370.

Return to Summary Table.

Two 8-bit register fields (DLL and DLH), called divisor latches, store the 16-bit divisor for generation of the baud clock in the baud generator. DLH holds the most-significant bits of the divisor, and DLL holds the least-significant bits of the divisor. These divisor latches must be loaded during initialization of the UART in order to ensure desired operation of the baud generator. Writing to the divisor latches results in two wait states being inserted during the write access while the baud generator is loaded with the new value.

Table 4-369. PRU_ICSS_UART_DIVISOR_LSB Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8020h

Figure 4-167. PRU_ICSS_UART_DIVISOR_LSB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DLL							
R-0h																								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-370. PRU_ICSS_UART_DIVISOR_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DLL	R/W	0h	The 8 least-significant bits (LSBs) of the 16-bit divisor for generation of the baud clock in the baud rate generator.

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4.5.6.10 PRU_ICSS_UART_DIVISOR_MSB Register (Offset = 24h) [reset = 0h]

PRU_ICSS_UART_DIVISOR_MSB is shown in Figure 4-168 and described in Table 4-372.

Return to Summary Table.

Two 8-bit register fields (DLL and DLH), called divisor latches, store the 16-bit divisor for generation of the baud clock in the baud generator. DLH holds the most-significant bits of the divisor, and DLL holds the least-significant bits of the divisor. These divisor latches must be loaded during initialization of the UART in order to ensure desired operation of the baud generator. Writing to the divisor latches results in two wait states being inserted during the write access while the baud generator is loaded with the new value.

Table 4-371. PRU_ICSS_UART_DIVISOR_MSB_ Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8024h

Figure 4-168. PRU_ICSS_UART_DIVISOR_MSB_ Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DLH							
R-0h																								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-372. PRU_ICSS_UART_DIVISOR_MSB_ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	DLH	R/W	0h	The 8 most-significant bits (MSBs) of the 16-bit divisor for generation of the baud clock in the baud rate generator.

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4.5.6.11 PRU_ICSS_UART_PERIPHERAL_ID Register (Offset = 28h) [reset = 44141102h]

PRU_ICSS_UART_PERIPHERAL_ID is shown in Figure 4-169 and described in Table 4-374.

Return to Summary Table.

Peripheral Identification register.

Table 4-373. PRU_ICSS_UART_PERIPHERAL_ID Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8028h

Figure 4-169. PRU_ICSS_UART_PERIPHERAL_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PID																															
R-44141102h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-374. PRU_ICSS_UART_PERIPHERAL_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PID	R	44141102h	

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4.5.6.12 PRU_ICSS_UART_POWER_MANAGEMENT_AND_EMULATION Register (Offset = 30h) [reset = 0h]

PRU_ICSS_UART_POWER_MANAGEMENT_AND_EMULATION is shown in Figure 4-170 and described in Table 4-376.

Return to Summary Table.

Power and emulation management register.

Table 4-375. PRU_ICSS_UART_POWER_MANAGEMENT_AND_EMULATION Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8030h

Figure 4-170. PRU_ICSS_UART_POWER_MANAGEMENT_AND_EMULATION Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	UTRST	URRST	RESERVED				
R/W-0h	R/W-0h	R/W-0h	R-0h				
7	6	5	4	3	2	1	0
RESERVED							FREE
R-0h							R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-376. PRU_ICSS_UART_POWER_MANAGEMENT_AND_EMULATION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	RESERVED	R/W	0h	Reserved. This bit must always be written with a 0.
14	UTRST	R/W	0h	UART transmitter reset. Resets and enables the transmitter. 0h: Transmitter is disabled and in reset state. 1h: Transmitter is enabled.
13	URRST	R/W	0h	UART receiver reset. Resets and enables the receiver. 0h: Receiver is disabled and in reset state. 1h: Receiver is enabled.
12-1	RESERVED	R	0h	Reserved
0	FREE	R/W	0h	Free-running enable mode bit. This bit determines the emulation mode functionality of the UART. When halted, the UART can handle register read/write requests, but does not generate any transmission/reception, interrupts or events. 0h: If a transmission is not in progress, the UART halts immediately. If a transmission is in progress, the UART halts after completion of the one-word transmission. 1h: Free-running mode is enabled; UART continues to run normally.

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4.5.6.13 PRU_ICSS_UART_MODE_DEFINITION Register (Offset = 34h) [reset = 0h]

PRU_ICSS_UART_MODE_DEFINITION is shown in Figure 4-171 and described in Table 4-378.

Return to Summary Table.

The Mode definition register determines the over-sampling mode for the UART.

Table 4-377. PRU_ICSS_UART_MODE_DEFINITION Instances

Instance	Physical Address
PRU_ICSS_UART	4802 8034h

Figure 4-171. PRU_ICSS_UART_MODE_DEFINITION Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							OSM_SEL
R-0h							R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-378. PRU_ICSS_UART_MODE_DEFINITION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	OSM_SEL	R/W	0h	Over-Sampling Mode Select. 0h: 16× over-sampling. 1h: 13× over-sampling.

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4.5.7 PRU_ICSS_ECAP Registers

PRU_ICSS_ECAP Registers lists the memory-mapped registers for the PRU_ICSS_eCAP0 module. All register offset addresses not listed in PRU_ICSS_ECAP Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-379. PRU_ICSS_ECAP Instances

Instance	Base Address
PRU_ICSS_ECAP	4803 0000h

Table 4-380. PRU_ICSS_ECAP Registers

Offset	Acronym	Register Name	PRU_ICSS_ECAP Physical Address	Section
0h	PRU_ICSS_ECAP_TSCNT	Time Stamp Counter Register	4803 0000h	
4h	PRU_ICSS_ECAP_CNTPHS	Counter Phase Control Register	4803 0004h	
8h	PRU_ICSS_ECAP_CAP1	Capture-1 Register	4803 0008h	
Ch	PRU_ICSS_ECAP_CAP2	Capture-2 Register	4803 000Ch	
10h	PRU_ICSS_ECAP_CAP3	Capture-3 Register	4803 0010h	
14h	PRU_ICSS_ECAP_CAP4	Capture-4 Register	4803 0014h	
28h	PRU_ICSS_ECAP_ECCTL1	ECAP Control Register1	4803 0028h	
2Ah	PRU_ICSS_ECAP_ECCTL2	ECAP Control Register 2	4803 002Ah	
2Ch	PRU_ICSS_ECAP_ECEINT	ECAP Interrupt Enable Register	4803 002Ch	
2Eh	PRU_ICSS_ECAP_ECFLG	ECAP Interrupt Flag Register	4803 002Eh	
30h	PRU_ICSS_ECAP_ECCLR	ECAP Interrupt Clear Register	4803 0030h	
34h	PRU_ICSS_ECAP_ECFRC	ECAP Interrupt Forcing Register	4803 0034h	
5Ch	PRU_ICSS_ECAP_PID	ECAP Revision ID	4803 005Ch	

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4.5.7.1 PRU_ICSS_ECAP_TSCNT Register (Offset = 0h) [reset = 0h]

PRU_ICSS_ECAP_TSCNT is shown in Figure 4-172 and described in Table 4-382.

Return to Summary Table.

Time Stamp Counter Register

Table 4-381. PRU_ICSS_ECAP_TSCNT Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 0000h

Figure 4-172. PRU_ICSS_ECAP_TSCNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSCNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-382. PRU_ICSS_ECAP_TSCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TSCNT	R/W	0h	Active 32 bit-counter register that is used as the capture time-base

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4.5.7.2 PRU_ICSS_ECAP_CNTPHS Register (Offset = 4h) [reset = 0h]

PRU_ICSS_ECAP_CNTPHS is shown in Figure 4-173 and described in Table 4-384.

Return to Summary Table.

Counter Phase Control Register

Table 4-383. PRU_ICSS_ECAP_CNTPHS Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 0004h

Figure 4-173. PRU_ICSS_ECAP_CNTPHS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNTPHS																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-384. PRU_ICSS_ECAP_CNTPHS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CNTPHS	R/W	0h	Counter phase value register that can be programmed for phase lag/lead. This register shadows TSCNT and is loaded into PRU_ICSS_ECAP_TSCNT upon either a SYNCI event or S/W force via a control bit. Used to achieve phase control synchronization with respect to other eCAP and EPWM time-bases.

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4.5.7.3 PRU_ICSS_ECAP_CAP1 Register (Offset = 8h) [reset = 0h]

PRU_ICSS_ECAP_CAP1 is shown in Figure 4-174 and described in Table 4-386.

Return to Summary Table.

Capture-1 Register

Table 4-385. PRU_ICSS_ECAP_CAP1 Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 0008h

Figure 4-174. PRU_ICSS_ECAP_CAP1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP1																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-386. PRU_ICSS_ECAP_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP1	R/W	0h	This register can be loaded (written) by the following. (a) Time-Stamp (that is, counter value) during a capture event. (b) Software may be useful for test purposes. (c) APRD active register when used in APWM mode.

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4.5.7.4 PRU_ICSS_ECAP_CAP2 Register (Offset = Ch) [reset = 0h]

PRU_ICSS_ECAP_CAP2 is shown in Figure 4-175 and described in Table 4-388.

Return to Summary Table.

Capture-2 Register

Table 4-387. PRU_ICSS_ECAP_CAP2 Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 000Ch

Figure 4-175. PRU_ICSS_ECAP_CAP2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP2																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-388. PRU_ICSS_ECAP_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP2	R/W	0h	This register can be loaded (written) by the following. (a) Time-Stamp (that is, counter value) during a capture event. (b) Software may be useful for test purposes. (c) APRD active register when used in APWM mode.

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4.5.7.5 PRU_ICSS_ECAP_CAP3 Register (Offset = 10h) [reset = 0h]

PRU_ICSS_ECAP_CAP3 is shown in Figure 4-176 and described in Table 4-390.

Return to Summary Table.

Capture-3 Register

Table 4-389. PRU_ICSS_ECAP_CAP3 Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 0010h

Figure 4-176. PRU_ICSS_ECAP_CAP3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP3																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-390. PRU_ICSS_ECAP_CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP3	R/W	0h	In CMP mode, this is a time-stamp capture register. In APWM mode, this is the period shadow (APRD) register. User software updates the PWM period value through this register. In this mode, CAP3 shadows CAP1.

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4.5.7.6 PRU_ICSS_ECAP_CAP4 Register (Offset = 14h) [reset = 0h]

PRU_ICSS_ECAP_CAP4 is shown in Figure 4-177 and described in Table 4-392.

Return to Summary Table.

Capture-4 Register

Table 4-391. PRU_ICSS_ECAP_CAP4 Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 0014h

Figure 4-177. PRU_ICSS_ECAP_CAP4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAP4																															
R/W-0h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-392. PRU_ICSS_ECAP_CAP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAP4	R/W	0h	In CMP mode, this is a time-stamp capture register. In APWM mode, this is the compare shadow (ACMP) register. User software updates the PWM compare value through this register. In this mode, CAP4 shadows CAP2.

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4.5.7.7 PRU_ICSS_ECAP_ECCTL1 Register (Offset = 28h) [reset = 0h]

PRU_ICSS_ECAP_ECCTL1 is shown in Figure 4-178 and described in Table 4-394.

Return to Summary Table.

ECAP Control Register1

Table 4-393. PRU_ICSS_ECAP_ECCTL1 Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 0028h

Figure 4-178. PRU_ICSS_ECAP_ECCTL1 Register

15	14	13	12	11	10	9	8
FREE_SOFT		EVTFLTPS					CAPLDEN
R/W-0h		R/W-0h					R/W-0h
7	6	5	4	3	2	1	0
CTRRST4	CAP4POL	CTRRST3	CAP3POL	CTRRST2	CAP2POL	CTRRST1	CAP1POL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-394. PRU_ICSS_ECAP_ECCTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	FREE_SOFT	R/W	0h	Emulation Control 0h: TSCNT counter stops immediately on emulation suspend. 1h: TSCNT counter runs until = 0. 2h: TSCNT counter is unaffected by emulation suspend (Run Free). 3h: TSCNT counter is unaffected by emulation suspend (Run Free).
13-9	EVTFLTPS	R/W	0h	Event Filter prescale select: 0h: Divide by 1 (i.e,. no prescale, by-pass the prescaler) 1h: Divide by 2 2h: Divide by 4 3h: Divide by 6 4h: Divide by 8 5h: Divide by 10 1Eh: Divide by 60 1Fh: Divide by 62
8	CAPLDEN	R/W	0h	Enable Loading of PRU_ICSS_ECAP_CAP1 to PRU_ICSS_ECAP_CAP4 registers on a capture event 0h: Disable PRU_ICSS_ECAP_CAP1-PRU_ICSS_ECAP_CAP4 register loads at capture event time. 1h: Enable PRU_ICSS_ECAP_CAP1-PRU_ICSS_ECAP_CAP4 register loads at capture event time.
7	CTRRST4	R/W	0h	Counter Reset on Capture Event 4 0h: Do not reset counter on Capture Event 4 (absolute time stamp operation) 1h: Reset counter after Capture Event 4 time-stamp has been captured (used in difference mode operation)
6	CAP4POL	R/W	0h	Capture Event 4 Polarity select 0h: Capture Event 4 triggered on a rising edge (RE) 1h: Capture Event 4 triggered on a falling edge (FE)

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Table 4-394. PRU_ICSS_ECAP_ECCTL1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CTRRST3	R/W	0h	Counter Reset on Capture Event 3 0h: Do not reset counter on Capture Event 3 (absolute time stamp) 1h: Reset counter after Event 3 time-stamp has been captured (used in difference mode operation)
4	CAP3POL	R/W	0h	Capture Event 3 Polarity select 0h: Capture Event 3 triggered on a rising edge (RE) 1h: Capture Event 3 triggered on a falling edge (FE)
3	CTRRST2	R/W	0h	Counter Reset on Capture Event 2 0h: Do not reset counter on Capture Event 2 (absolute time stamp) 1h: Reset counter after Event 2 time-stamp has been captured (used in difference mode operation)
2	CAP2POL	R/W	0h	Capture Event 2 Polarity select 0h: Capture Event 2 triggered on a rising edge (RE) 1h: Capture Event 2 triggered on a falling edge (FE)
1	CTRRST1	R/W	0h	Counter Reset on Capture Event 1 0h: Do not reset counter on Capture Event 1 (absolute time stamp) 1h: Reset counter after Event 1 time-stamp has been captured (used in difference mode operation)
0	CAP1POL	R/W	0h	Capture Event 1 Polarity select 0h: Capture Event 1 triggered on a rising edge (RE) 1h: Capture Event 1 triggered on a falling edge (FE)

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4.5.7.8 PRU_ICSS_ECAP_ECCTL2 Register (Offset = 2Ah) [reset = 6h]

PRU_ICSS_ECAP_ECCTL2 is shown in Figure 4-179 and described in Table 4-396.

Return to Summary Table.

ECAP Control Register 2

Table 4-395. PRU_ICSS_ECAP_ECCTL2 Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 002Ah

Figure 4-179. PRU_ICSS_ECAP_ECCTL2 Register

15	14	13	12	11	10	9	8
RESERVED					APWMPOL	CAPAPWM	SWSYNC
R-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SYNCO_SEL		SYNCI_EN	TSCNTSTP	REARMRESET	STOPVALUE		CONTONESHT
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-3h		R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-396. PRU_ICSS_ECAP_ECCTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0h	Reserved
10	APWMPOL	R/W	0h	APWM output polarity select. This is applicable only in APWM operating mode 0h: Output is active high (Compare value defines high time) 1h: Output is active low (Compare value defines low time)
9	CAPAPWM	R/W	0h	CAP/APWM operating mode select 0h: ECAP module operates in capture mode. This mode forces the following configuration. (a) Inhibits TSCNT resets via CTR = PRD event. (b) Inhibits shadow loads on PRU_ICSS_ECAP_CAP1 and PRU_ICSS_ECAP_CAP2 registers. (c) Permits user to enable PRU_ICSS_ECAP_CAP1-PRU_ICSS_ECAP_CAP4 register load. (d) ECAP input/APWM output pin operates as a capture input. 1h: ECAP module operates in APWM mode. This mode forces the following configuration. (a) Resets TSCNT on CTR = PRD event (period boundary). (b) Permits shadow loading on PRU_ICSS_ECAP_CAP1 and PRU_ICSS_ECAP_CAP2 registers. (c) Disables loading of time-stamps into PRU_ICSS_ECAP_CAP1 - PRU_ICSS_ECAP_CAP4 registers. (d) ECAP input/APWM ouput pin operates as a APWM output.

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Table 4-396. PRU_ICSS_ECAP_ECCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SWSYNC	R/W	0h	Software-forced Counter (TSCNT) Synchronizing. This provides a convenient software method to synchronize some or all ECAP time bases. In APWM mode, the synchronizing can also be done via the CTR = PRD event. Note: Selection CTR = PRD is meaningful only in APWM mode. However, you can choose it in CAP mode if you find doing so useful. 0h: Writing a zero has no effect. Reading always returns a zero 1h: Writing a one forces a TSCNT shadow load of current ECAP module and any ECAP modules down-stream providing the SYNCO_SEL bits are 1'b00. After writing a 1, this bit returns to a zero.
7-6	SYNCO_SEL	R/W	0h	Sync-Out Select 0h: Select sync-in event to be the sync-out signal (pass through) 1h: Select CTR = PRD event to be the sync-out signal 2h: Disable sync out signal 3h: Disable sync out signal
5	SYNCI_EN	R/W	0h	Counter (TSCNT) Sync-In select mode 0h: Disable sync-in option 1h: Enable counter (TSCNT) to be loaded from PRU_ICSS_ECAP_CNTPHS register upon either a SYNCI signal or a S/W force event.
4	TSCNTSTP	R/W	0h	Time Stamp (TSCNT) Counter Stop (freeze) Control 0h: TSCNT stopped 1h: TSCNT free-running
3	REARMRESET	R/W	0h	One-Shot Re-Arming Control, that is, wait for stop trigger. Note: The re-arm function is valid in one shot or continuous mode. 0h: Has no effect (reading always returns a 0) 1h: Arms the one-shot sequence as follows: 1) Resets the Mod4 counter to zero. 2) Unfreezes the Mod4 counter. 3) Enables capture register loads.

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Table 4-396. PRU_ICSS_ECAP_ECCTL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-1	STOPVALUE	R/W	3h	Stop value for one-shot mode. This is the number (between 1 and 4) of captures allowed to occur before the CAP (1 through 4) registers are frozen, that is, capture sequence is stopped. Wrap value for continuous mode. This is the number (between 1 and 4) of the capture register in which the circular buffer wraps around and starts again. Notes: STOPVALUE is compared to Mod4 counter and, when equal, the following two actions occur. (1) Mod4 counter is stopped (frozen). (2) Capture register loads are inhibited. In one-shot mode, further interrupt events are blocked until re-armed. 0h: Stop after Capture Event 1 in one-shot mode. Wrap after Capture Event 1 in continuous mode. 1h: Stop after Capture Event 2 in one-shot mode. Wrap after Capture Event 2 in continuous mode. 2h: Stop after Capture Event 3 in one-shot mode. Wrap after Capture Event 3 in continuous mode. 3h: Stop after Capture Event 4 in one-shot mode. Wrap after Capture Event 4 in continuous mode.
0	CONTONESHT	R/W	0h	Continuous or one-shot mode control (applicable only in capture mode) 0h: Operate in continuous mode 1h: Operate in one-shot mode

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4.5.7.9 PRU_ICSS_ECAP_ECEINT Register (Offset = 2Ch) [reset = 0h]

PRU_ICSS_ECAP_ECEINT is shown in Figure 4-180 and described in Table 4-398.

Return to Summary Table.

ECAP Interrupt Enable Register

Table 4-397. PRU_ICSS_ECAP_ECEINT Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 002Ch

Figure 4-180. PRU_ICSS_ECAP_ECEINT Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CMPEQ	PRDEQ	CNTOVF	CEVT4	CEVT3	CEVT2	CEVT1	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-398. PRU_ICSS_ECAP_ECEINT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CMPEQ	R/W	0h	Counter Equal **Compare** Interrupt Enable. 0h: Disable Compare Equal as an Interrupt source. 1h: Enable Compare Equal as an Interrupt source.
6	PRDEQ	R/W	0h	Counter Equal **Period** Interrupt Enable. 0h: Disable Period Equal as an Interrupt source. 1h: Enable Period Equal as an Interrupt source.
5	CNTOVF	R/W	0h	Counter Overflow Interrupt Enable. 0h: Disable counter Overflow as an Interrupt source. 1h: Enable counter Overflow as an Interrupt source.
4	CEVT4	R/W	0h	Capture Event 4 Interrupt Enable. 0h: Disable Capture Event 4 as an Interrupt source. 1h: Enable Capture Event 4 as an Interrupt source.
3	CEVT3	R/W	0h	Capture Event 3 Interrupt Enable. 0h: Disable Capture Event 3 as an Interrupt source. 1h: Enable Capture Event 3 as an Interrupt source.
2	CEVT2	R/W	0h	Capture Event 2 Interrupt Enable. 0h: Disable Capture Event 2 as an Interrupt source. 1h: Enable Capture Event 2 as an Interrupt source.

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Table 4-398. PRU_ICSS_ECAP_ECEINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CEVT1	R/W	0h	Capture Event 1 Interrupt Enable . 0h: Disable Capture Event 1 as an Interrupt source. 1h: Enable Capture Event 1 as an Interrupt source.
0	RESERVED	R	0h	Reserved

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4.5.7.10 PRU_ICSS_ECAP_ECFLG Register (Offset = 2Eh) [reset = 0h]

PRU_ICSS_ECAP_ECFLG is shown in Figure 4-181 and described in Table 4-400.

Return to Summary Table.

ECAP Interrupt Flag Register

Table 4-399. PRU_ICSS_ECAP_ECFLG Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 002Eh

Figure 4-181. PRU_ICSS_ECAP_ECFLG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CMPEQ	PRDEQ	CNTOVF	CEVT4	CEVT3	CEVT2	CEVT1	INT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-400. PRU_ICSS_ECAP_ECFLG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CMPEQ	R	0h	Compare Equal Compare Status Flag. This flag is only active in APWM mode. 0h: Indicates no event occurred 1h: Indicates the counter (TSCNT) reached the compare register value (ACMP)
6	PRDEQ	R	0h	Counter Equal Period Status Flag. This flag is only active in APWM mode. 0h: Indicates no event occurred 1h: Indicates the counter (TSCNT) reached the period register value (APRD) and was reset.
5	CNTOVF	R	0h	Counter Overflow Status Flag. This flag is active in CAP and APWM mode. 0h: Indicates no event occurred. 1h: Indicates the counter (TSCNT) has made the transition from FFFFFFFFh to 00000000h
4	CEVT4	R	0h	Capture Event 4 Status Flag This flag is only active in CAP mode. 0h: Indicates no event occurred 1h: Indicates the fourth event occurred at ECAPn pin
3	CEVT3	R	0h	Capture Event 3 Status Flag. This flag is active only in CAP mode. 0h: Indicates no event occurred. 1h: Indicates the third event occurred at ECAPn pin.

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Table 4-400. PRU_ICSS_ECAP_ECFLG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CEVT2	R	0h	Capture Event 2 Status Flag. This flag is only active in CAP mode. 0h: Indicates no event occurred. 1h: Indicates the second event occurred at ECAPn pin.
1	CEVT1	R	0h	Capture Event 1 Status Flag. This flag is only active in CAP mode. 0h: Indicates no event occurred. 1h: Indicates the first event occurred at ECAPn pin.
0	INT	R	0h	Global Interrupt Status Flag 0h: Indicates no interrupt generated. 1h: Indicates that an interrupt was generated.

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4.5.7.11 PRU_ICSS_ECAP_ECCLR Register (Offset = 30h) [reset = 0h]

PRU_ICSS_ECAP_ECCLR is shown in Figure 4-182 and described in Table 4-402.

Return to Summary Table.

ECAP Interrupt Clear Register

Table 4-401. PRU_ICSS_ECAP_ECCLR Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 0030h

Figure 4-182. PRU_ICSS_ECAP_ECCLR Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CMPEQ	PRDEQ	CNTOVF	CEVT4	CEVT3	CEVT2	CEVT1	INT
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-402. PRU_ICSS_ECAP_ECCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CMPEQ	R/W	0h	Counter Equal Compare Status Flag 0h: Writing a 0 has no effect. Always reads back a 0 1h: Writing a 1 clears the CTR=CMP flag condition
6	PRDEQ	R/W	0h	Counter Equal Period Status Flag 0h: Writing a 0 has no effect. Always reads back a 0 1h: Writing a 1 clears the CTR=PRD flag condition
5	CNTOVF	R/W	0h	Counter Overflow Status Flag 0h: Writing a 0 has no effect. Always reads back a 0 1h: Writing a 1 clears the CNTOVF flag condition
4	CEVT4	R/W	0h	Capture Event 4 Status Flag 0h: Writing a 0 has no effect. Always reads back a 0. 1h: Writing a 1 clears the CEVT3 flag condition.
3	CEVT3	R/W	0h	Capture Event 3 Status Flag 0h: Writing a 0 has no effect. Always reads back a 0. 1h: Writing a 1 clears the CEVT3 flag condition.
2	CEVT2	R/W	0h	Capture Event 2 Status Flag 0h: Writing a 0 has no effect. Always reads back a 0. 1h: Writing a 1 clears the CEVT2 flag condition.

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Table 4-402. PRU_ICSS_ECAP_ECCLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CEVT1	R/W	0h	Capture Event 1 Status Flag 0h: Writing a 0 has no effect. Always reads back a 0. 1h: Writing a 1 clears the CEVT1 flag condition.
0	INT	R/W	0h	Global Interrupt Clear Flag 0h: Writing a 0 has no effect. Always reads back a 0. 1h: Writing a 1 clears the INT flag and enable further interrupts to be generated if any of the event flags are set to 1.

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4.5.7.12 PRU_ICSS_ECAP_ECFRC Register (Offset = 34h) [reset = 0h]

PRU_ICSS_ECAP_ECFRC is shown in Figure 4-183 and described in Table 4-404.

Return to Summary Table.

ECAP Interrupt Forcing Register

Table 4-403. PRU_ICSS_ECAP_ECFRC Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 0034h

Figure 4-183. PRU_ICSS_ECAP_ECFRC Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CMPEQ	PRDEQ	CNTOVF	CEVT4	CEVT3	CEVT2	CEVT1	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-404. PRU_ICSS_ECAP_ECFRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0h	Reserved
7	CMPEQ	R/W	0h	Force Counter Equal Compare Interrupt 0h: No effect. Always reads back a 0. 1h: Writing a 1 sets the CTR=CMP flag bit.
6	PRDEQ	R/W	0h	Force Counter Equal Period Interrupt 0h: No effect. Always reads back a 0. 1h: Writing a 1 sets the CTR=PRD flag bit.
5	CNTOVF	R/W	0h	Force Counter Overflow 0h: No effect. Always reads back a 0. 1h: Writing a 1 to this bit sets the CNTOVF flag bit.
4	CEVT4	R/W	0h	Force Capture Event 4 0h: No effect. Always reads back a 0. 1h: Writing a 1 sets the CEVT4 flag bit
3	CEVT3	R/W	0h	Force Capture Event 3 0h: No effect. Always reads back a 0. 1h: Writing a 1 sets the CEVT3 flag bit
2	CEVT2	R/W	0h	Force Capture Event 2 0h: No effect. Always reads back a 0. 1h: Writing a 1 sets the CEVT2 flag bit.

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Table 4-404. PRU_ICSS_ECAP_ECFRC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CEVT1	R/W	0h	Always reads back a 0. Force Capture Event 1 0h: No effect. 1h: Writing a 1 sets the CEVT1 flag bit.
0	RESERVED	R	0h	Reserved

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4.5.7.13 PRU_ICSS_ECAP_PID Register (Offset = 5Ch) [reset = -h]

PRU_ICSS_ECAP_PID is shown in Figure 4-184 and described in Table 4-406.

Return to Summary Table.

ECAP Revision ID

Table 4-405. PRU_ICSS_ECAP_PID Instances

Instance	Physical Address
PRU_ICSS_ECAP	4803 005Ch

Figure 4-184. PRU_ICSS_ECAP_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															
R--h																															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-406. PRU_ICSS_ECAP_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REVISION	R	-h	IP Revision

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4.5.8 PRU_ICSS_MII_RT Registers

PRU_ICSS_MII_RT Registers lists the memory-mapped registers for the PRU_ICSS MII_RT module. All register offset addresses not listed in PRU_ICSS_MII_RT Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-407. PRU_ICSS MII RT Instances

Instance	Base Address
PRU_ICSS_MII_RT	4803 2000h

Table 4-408. PRU_ICSS MII RT Registers

Offset	Acronym	Register Name	PRU_ICSS_MII_RT Physical Address
0h	PRU_ICSS_MII_RT_RXCFG0	MII RXCFG 0 Register	4803 2000h
4h	PRU_ICSS_MII_RT_RXCFG1	MII RXCFG 1 Register	4803 2004h
10h	PRU_ICSS_MII_RT_TXCFG0	MII TXCFG 0 Register	4803 2010h
14h	PRU_ICSS_MII_RT_TXCFG1	MII TXCFG 1 Register	4803 2014h
20h	PRU_ICSS_MII_RT_TX_CRC0	MII TXCRC 0 Register	4803 2020h
24h	PRU_ICSS_MII_RT_TX_CRC1	MII TXCRC 1 Register	4803 2024h
30h	PRU_ICSS_MII_RT_TX_IPG0	MII TXIPG 0 Register	4803 2030h
34h	PRU_ICSS_MII_RT_TX_IPG1	MII TXIPG 1 Register	4803 2034h
38h	PRU_ICSS_MII_RT_PRS0	MII PORT STATUS 0 Register	4803 2038h
3Ch	PRU_ICSS_MII_RT_PRS1	MII PORT STATUS 1 Register	4803 203Ch
40h	PRU_ICSS_MII_RT_RX_FRMS0	MII RXFRMS 0 Register	4803 2040h
44h	PRU_ICSS_MII_RT_RX_FRMS1	MII RXFRMS 1 Register	4803 2044h
48h	PRU_ICSS_MII_RT_RX_PCNT0	MII RXPCNT 0 Register	4803 2048h
4Ch	PRU_ICSS_MII_RT_RX_PCNT1	MII RXPCNT 1 Register	4803 204Ch
50h	PRU_ICSS_MII_RT_RX_ERR0	MII RXERR 0 Register	4803 2050h
54h	PRU_ICSS_MII_RT_RX_ERR1	MII RXERR 1 Register	4803 2054h
60h	PRU_ICSS_MII_RT_RXFLV0	MII RX FIFO Level 0 Register	4803 2060h
64h	PRU_ICSS_MII_RT_RXFLV1	MII RX FIFO Level 1 Register	4803 2064h
68h	PRU_ICSS_MII_RT_TXFLV0	MII TX FIFO Level 0 Register	4803 2068h
6Ch	PRU_ICSS_MII_RT_TXFLV1	MII TX FIFO Level 1 Register	4803 206Ch

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4.5.8.1 PRU_ICSS_MII_RT_RXCFG0 Register (Offset = 0h) [reset = 0h]

PRU_ICSS_MII_RT_RXCFG0 is shown in Figure 4-185 and described in Table 4-410.

MII RXCFG 0 REGISTER
This register contains the PRU0 RXCFG configuration variables (RXCFG0) for the RX path.
PRU_ICSS_MII_RT_RXCFG0 is attached to PRU0.
PRU_ICSS_MII_RT_RXCFG0 controls which RX port is attached to PRU0.

Table 4-409. PRU_ICSS_MII_RT_RXCFG0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2000h

Figure 4-185. PRU_ICSS_MII_RT_RXCFG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						RX_L2_EOF_SCLR_DIS	RX_ERR_RAW
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RX_SFD_RAW	RX_AUTO_FWD_PRE	RX_BYTE_SWAP	RX_L2_EN	RX_MUX_SEL	RX_CUT_PREAMBLE	RX_DATA_RDY_MODE_DIS	RX_ENABLE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-410. PRU_ICSS_MII_RT_RXCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9	RX_L2_EOF_SCLR_DIS	R/W	0h	0h: RX_EOF flag in R31 and RXL2 is self cleared by hardware when RXL2 is enabled 1h: RX_EOF flag in R31 and RXL2 is not self cleared by hardware when RXL2 is enabled. To clear this flag, RX_EOF_CLR must be set.
8	RX_ERR_RAW	R/W	0h	0h: Error Raw Mode Disabled. RX_ERR is qualified with RX_DV, meaning RX_DV = 1 before RX_ERR action/event is generated. 1h: Error Raw Mode Enabled. RX_ERR is not qualified with RX_DV, meaning RX_ERR action/event is generated even if RX_DV = 0.
7	RX_SFD_RAW	R/W	0h	0h: SFD Raw Mode Disabled. RX_SFD requires a pattern of 5D. 1h: SFD Raw Mode Enable. The first byte of any pattern after RX_DV assertion will trigger RX_SFD event. The first nibble of the frame (RX_DV = 1) will be in the RX FIFO.

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Table 4-410. PRU_ICSS_MII_RT_RXCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RX_AUTO_FWD_PRE	R/W	0h	Enables auto-forward of received preamble. When enabled, this will forward the preamble nibbles including the SFD to the TX L1 FIFO that is attached to the PRU. First data byte seen by PRU R31 and/or RX L2 is destination address (DA). **Note: Odd number of preamble nibbles is supported in this mode. For example, 0x55D Note that new RX should only occur after the current TX completes** 0h: Disable 1h: Enable, it must disable RX_CUT_PREAMBLE and TX_AUTO_PREAMBLE
5	RX_BYTE_SWAP	R/W	0h	Defines the order of Byte0/1 placement for RX R31 and RX L2. **Note: that if TX_AUTO_SEQUENCE enabled, this bit cannot get enable since TX_BYTE_SWAP on swaps the PRU output. This bit must be selected/updated when the port is disabled or there is no traffic.** 0h: R31 [15:8]/RXL2 [15:8] = Byte1{Nibble3,Nibble2} R31[7:0]/RXL2 [7:0] = Byte0{Nibble1,Nibble0} 1h: R31 [15:8]/RXL2 [15:8] = Byte0{Nibble1,Nibble0} R31[7:0]/RXL2 [7:0] = Byte1{Nibble3,Nibble2} Nibble0 is the first nibble received.
4	RX_L2_EN	R/W	0h	Enables RX L2 buffer. 0h: Disable (RX L2 can function as generic scratch pad) 1h: Enable
3	RX_MUX_SEL	R/W	0h	Selects receive data source. Typically, the setting for this will not be identical for the two MII receive configuration registers. 0h: MII RX Data from Port 0 (default for PRU_ICSS_MII_RT_RXCFG0) 1h: MII RX Data from Port 1 (default for PRU_ICSS_MII_RT_RXCFG1)
2	RX_CUT_PREAMBLE	R/W	0h	Removes received preamble. 0h: All data from Ethernet PHY are passed on to PRU register. This assumes Ethernet PHY which does not shorten the preamble. 1h: MII interface suppresses preamble and sync frame delimiter. First data byte seen by PRU register is destination address.
1	RX_DATA_RDY_MODE_DIS	R/W	0h	0h: R31, Bit 16 is configured for DATA_RDY mode. 1h: R31, Bit 16 is configured for TX_EOF mode.
0	RX_ENABLE	R/W	0h	Enables the receive traffic currently selected by RX_MUX_SELECT. 0h: Disable 1h: Enable

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4.5.8.2 PRU_ICSS_MII_RT_RXCFG1 Register (Offset = 4h) [reset = 8h]

PRU_ICSS_MII_RT_RXCFG1 is shown in Figure 4-186 and described in Table 4-412.

MII RXCFG 1 REGISTER
This register contains the PRU1 RXCFG configuration variables (PRU_ICSS_MII_RT_RXCFG1) for the RX path.
PRU_ICSS_MII_RT_RXCFG1 is attached to PRU1.
PRU_ICSS_MII_RT_RXCFG1 controls which RX port is attached to PRU1.

Table 4-411. PRU_ICSS_MII_RT_RXCFG1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2004h

Figure 4-186. PRU_ICSS_MII_RT_RXCFG1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						RX_L2_EOF_SCLR_DIS	RX_ERR_RAW
R-0h						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RX_SFD_RAW	RX_AUTO_FWD_PRE	RX_BYTE_SWAP	RX_L2_EN	RX_MUX_SEL	RX_CUT_PREAMBLE	RX_DATA_RDY_MODE_DIS	RX_ENABLE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-412. PRU_ICSS_MII_RT_RXCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9	RX_L2_EOF_SCLR_DIS	R/W	0h	0h: RX_EOF flag in R31 and RXL2 is self cleared by hardware when RXL2 is enabled 1h: RX_EOF flag in R31 and RXL2 is not self cleared by hardware when RXL2 is enabled. To clear this flag, RX_EOF_CLR must be set.
8	RX_ERR_RAW	R/W	0h	0h: Error Raw Mode Disabled. RX_ERR is qualified with RX_DV, meaning RX_DV = 1 before RX_ERR action/event is generated. 1h: Error Raw Mode Enabled. RX_ERR is not qualified with RX_DV, meaning RX_ERR action/event is generated even if RX_DV = 0.
7	RX_SFD_RAW	R/W	0h	0h: SFD Raw Mode Disabled. RX_SFD requires a pattern of 5D. 1h: SFD Raw Mode Enable. The first byte of any pattern after RX_DV assertion will trigger RX_SFD event. The first nibble of the frame (RX_DV = 1) will be in the RX FIFO.

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Table 4-412. PRU_ICSS_MII_RT_RXCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RX_AUTO_FWD_PRE	R/W	0h	Enables auto-forward of received preamble. When enabled, this will forward the preamble nibbles including the SFD to the TX L1 FIFO that is attached to the PRU. First data byte seen by PRU R31 and/or RX L2 is destination address (DA). **Note: Odd number of preamble nibbles is supported in this mode. For example, 0x55D Note that new RX should only occur after the current TX completes** 0h: Disable 1h: Enable, it must disable RX_CUT_PREAMBLE and TX_AUTO_PREAMBLE
5	RX_BYTE_SWAP	R/W	0h	Defines the order of Byte0/1 placement for RX R31 and RX L2. **Note: that if TX_AUTO_SEQUENCE enabled, this bit cannot get enable since TX_BYTE_SWAP on swaps the PRU output. This bit must be selected/updated when the port is disabled or there is no traffic.** 0h: R31 [15:8]/RXL2 [15:8] = Byte1{Nibble3,Nibble2} R31[7:0]/RXL2 [7:0] = Byte0{Nibble1,Nibble0} 1h: R31 [15:8]/RXL2 [15:8] = Byte0{Nibble1,Nibble0} R31[7:0]/RXL2 [7:0] = Byte1{Nibble3,Nibble2} Nibble0 is the first nibble received.
4	RX_L2_EN	R/W	0h	Enables RX L2 buffer. 0h: Disable (RX L2 can function as generic scratch pad) 1h: Enable
3	RX_MUX_SEL	R/W	1h	Selects receive data source. Typically, the setting for this will not be identical for the two MII receive configuration registers. 0h: MII RX Data from Port 0 (default for PRU_ICSS_MII_RT_RXCFG0) 1h: MII RX Data from Port 1 (default for PRU_ICSS_MII_RT_RXCFG1)
2	RX_CUT_PREAMBLE	R/W	0h	Removes received preamble. 0h: All data from Ethernet PHY are passed on to PRU register. This assumes Ethernet PHY which does not shorten the preamble. 1h: MII interface suppresses preamble and sync frame delimiter. First data byte seen by PRU register is destination address.
1	RX_DATA_RDY_MODE_DIS	R/W	0h	0h: R31, Bit 16 is configured for DATA_RDY mode. 1h: R31, Bit 16 is configured for TX_EOF mode.
0	RX_ENABLE	R/W	0h	Enables the receive traffic currently selected by RX_MUX_SELECT. 0h: Disable 1h: Enable

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4.5.8.3 PRU_ICSS_MII_RT_TXCFG0 Register (Offset = 10h) [reset = 00400100h]

PRU_ICSS_MII_RT_TXCFG0 is shown in Figure 4-187 and described in Table 4-414.

MII TXCFG 0 REGISTER
This register contains the configuration variables for the transmit path on the MII interface port 0.
PRU_ICSS_MII_RT_TXCFG0 is attached to Port TX0.
PRU_ICSS_MII_RT_TXCFG0 controls which PRU is selected for TX0

Table 4-413. PRU_ICSS_MII_RT_TXCFG0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2010h

Figure 4-187. PRU_ICSS_MII_RT_TXCFG0 Register

31	30	29	28	27	26	25	24
RESERVED		TX_CLK_DELAY		RESERVED		TX_START_DELAY	
R-0h		R/W-0h		R-0h		R/W-40h	
23	22	21	20	19	18	17	16
TX_START_DELAY							
R/W-40h							
15	14	13	12	11	10	9	8
RESERVED				TX_32_MODE_EN	PRE_TX_AUTO_ESC_ERR	PRE_TX_AUTO_SEQUENCE	TX_MUX_SEL
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-1h
7	6	5	4	3	2	1	0
RESERVED				TX_BYTE_SWAP	TX_EN_MODE	TX_AUTO_PREAMBLE	TX_ENABLE
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-414. PRU_ICSS_MII_RT_TXCFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-28	TX_CLK_DELAY	R/W	0h	In order to guarantee the MII_RT IO timing values published in the device data manual, the ICSS_i_VCLK_CLK (where i = 0 or 1) clock must be configured for 200MHz and TX_CLK_DELAY must be set to 6h.
27-26	RESERVED	R	0h	Reserved

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Table 4-414. PRU_ICSS_MII_RT_TXCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-16	TX_START_DELAY	R/W	40h	Defines the minimum time interval (delay) between receiving the RXDV for the current frame and the start of the transmit interface sending data to the MII interface. Delay value is in units of MII_RT clock cycles, which uses the ICSS_i_VCLK_CLK (default is 200MHz, or 5ns). Default TX_START_DELAY value is 320ns, which is optimized for minimum latency at 16 bit processing. Counter is started with RX_DV signal going active. Transmit interface stops sending data when no more data is written into transmit interface by PRU along with TX_EOF marker bit set. If the TX FIFO has data when the delay expires, then TX will start sending data. But if the TX FIFO is empty, it will not start until the TX FIFO is not empty. It is possible to overflow the TX FIFO with the max delay setting when auto-forwarding is enabled since the time delay is larger than the amount of data it needs to store. As long as TX L1 FIFO overflows, software will need to issue a TX_RESET to reset the TX FIFO. The total delay is 96-byte times (size of TX FIFO), but you need to allow delays for synchronization. Do to this fact, the maximum delay should be 80ns less when auto forwarding is enabled. Therefore, 0x3F0 is the maximum in this configuration.
15-12	RESERVED	R	0h	Reserved
11	TX_32_MODE_EN	R/W	0h	0h: Disable 32-bit Data Push mode. 1h: Enable 32-bit, 16-bit, and 8-bit Data Push mode with TX_MASK disabled. In this mode, the internal PRU R30 byte write strobes are used and not the R31 CMD TX_PUSH mode. Any update to R30 will trigger an TX PUSH. See .
10	RESERVED	R	0h	Reserved
9	TX_AUTO_SEQUENCE	R/W	0h	Enables transmit auto-sequence. Note the transmit data source is determined by TX_MUX_SEL setting. 0h: Disable 1h: Enable, transmit state machine based on events on receiver path that is connected to the respective transmitter. Also, the masking logic is disabled and only the MII data is used.
8	TX_MUX_SEL	R/W	1h	Selects transmit data source. The default/reset setting for TX Port 0 is 1. This setting permits MII TX Port 0 to receive data from PRU1 and the MII TX Port 1 which is connected to PRU0 by default. 0h: Data from PRU0 (default for PRU_ICSS_MII_RT_TXCFG1) 1h: Data from PRU1 (default for PRU_ICSS_MII_RT_TXCFG0)
7-4	RESERVED	R	0h	Reserved

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Table 4-414. PRU_ICSS_MII_RT_TXCFG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TX_BYTE_SWAP	R/W	0h	Defines the order of Byte0/1 placement for TX R30. This bit must be selected/updated when the port is disabled or there is no traffic. **0h: If** PRU_ICSS_MII_RT_TXCFG0**/1 [TX_32_MODE_EN] = 0,** R30[15:8] = Byte1{Nibble3,Nibble2} R30[7:0] = Byte0{Nibble1,Nibble0} R30[31:24] = TX_MASK[15:8] R30[23:16] = TX_MASK[7:0] **If** PRU_ICSS_MII_RT_TXCFG0**/1 [TX_32_MODE_EN] = 1,** R30[31:24] = Byte3{Nibble7,Nibble6} R30[23:16] = Byte2{Nibble5,Nibble4} R30[15:8] = Byte1{Nibble3,Nibble2} R30[7:0] = Byte0{Nibble1,Nibble0} **1h: If** PRU_ICSS_MII_RT_TXCFG0**/1 [TX_32_MODE_EN] = 0,** R30[15:8] = Byte0{Nibble1,Nibble0} R30[7:0] = Byte1{Nibble3,Nibble2} R30[31:24] = TX_MASK[7:0] R30[23:16] = TX_MASK[15:8] **If** PRU_ICSS_MII_RT_TXCFG0**/1 [TX_32_MODE_EN] = 1,** (ONLY SUPPORT 32bit push) R30[31:24] = Byte0{Nibble1,Nibble0} R30[23:16] = Byte1{Nibble3,Nibble2} R30[15:8] = Byte2{Nibble5,Nibble4} R30[7:0] = Byte3{Nibble7,Nibble6 **Note Nibble0 is the first nibble received.**
2	TX_EN_MODE	R/W	0h	Enables transmit self clear on TX_EOF event. **Note that iep.cmp[3] must be set before transmission will start for TX0, and iep_cmp[4] for TX1. This is a new dependency, in addition to TX L1 FIFO not empty and TX_START_DELAY expiration, to start transmission.** 0h: Disable 1h: Enable, TX_ENABLE will be clear for a TX_EOF event by itself.
1	TX_AUTO_PREAMBLE	R/W	0h	Transmit data auto-preamble. 0h: PRU will provide full preamble 1h: TX FIFO will insert pre-amble automatically **Note: the TX FIFO does not get preloaded with the preamble until the first write occurs. This can cause the latency to be larger the min latency.**
0	TX_ENABLE	R/W	0h	Enables transmit traffic on TX PORT. If TX_EN_MODE is set, then TX_ENABLE will self clear during a TX_EOF event. Note Software can use this to pre-fill the TX FIFO and then start the TX frame during non-ECS operations. 0h: TX PORT is disabled/stopped immediately 1h: TX PORT is enabled and the frame will start once the IPG counter expired and TX Start Delay counter has expired

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4.5.8.4 PRU_ICSS_MII_RT_TXCFG1 Register (Offset = 14h) [reset = 00400000h]

PRU_ICSS_MII_RT_TXCFG1 is shown in Figure 4-188 and described in Table 4-416.

MII TXCFG 1 REGISTER
This register contains the configuration variables for the transmit path on the MII interface port 1.
PRU_ICSS_MII_RT_TXCFG1 is attached to Port TX1.
PRU_ICSS_MII_RT_TXCFG1 controls which PRU is selected for TX1

Table 4-415. PRU_ICSS_MII_RT_TXCFG1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2014h

Figure 4-188. PRU_ICSS_MII_RT_TXCFG1 Register

31	30	29	28	27	26	25	24
RESERVED		TX_CLK_DELAY		RESERVED		TX_START_DELAY	
R-0h		R/W-0h		R-0h		R/W-40h	
23	22	21	20	19	18	17	16
TX_START_DELAY							
R/W-40h							
15	14	13	12	11	10	9	8
RESERVED				TX_32_MODE_EN	PRE_TX_AUTO_ESC_ERR	PRE_TX_AUTO_SEQUENCE	TX_MUX_SEL
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED				TX_BYTE_SWAP	TX_EN_MODE	TX_AUTO_PREAMBLE	TX_ENABLE
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-416. PRU_ICSS_MII_RT_TXCFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-28	TX_CLK_DELAY	R/W	0h	In order to guarantee the MII_RT IO timing values published in the device data manual, the ICSS_i_VCLK_CLK (where i = 0 or 1) clock must be configured for 200MHz and TX_CLK_DELAY must be set to 6h.
27-26	RESERVED	R	0h	Reserved

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Table 4-416. PRU_ICSS_MII_RT_TXCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-16	TX_START_DELAY	R/W	40h	Defines the minimum time interval (delay) between receiving the RXDV for the current frame and the start of the transmit interface sending data to the MII interface. Delay value is in units of MII_RT clock cycles, which uses the ICSS_i_VCLK_CLK, where i = 0 or 1 (default is 200MHz, or 5ns). Default TX_START_DELAY value is 320ns, which is optimized for minimum latency at 16 bit processing. Counter is started with RX_DV signal going active. Transmit interface stops sending data when no more data is written into transmit interface by PRU along with TX_EOF marker bit set. If the TX FIFO has data when the delay expires, then TX will start sending data. But if the TX FIFO is empty, it will not start until the TX FIFO is not empty. It is possible to overflow the TX FIFO with the max delay setting when auto-forwarding is enabled since the time delay is larger than the amount of data it needs to store. As long as TX L1 FIFO overflows, software will need to issue a TX_RESET to reset the TX FIFO. The total delay is 96-byte times (size of TX FIFO), but you need to allow delays for synchronization. Do to this fact, the maximum delay should be 80ns less when auto forwarding is enabled. Therefore, 0x3F0 is the maximum in this configuration.
15-12	RESERVED	R	0h	Reserved
11	TX_32_MODE_EN	R/W	0h	0h: Disable 32-bit Data Push mode. 1h: Enable 32-bit, 16-bit, and 8-bit Data Push mode with TX_MASK disabled. In this mode, the internal PRU R30 byte write strobes are used and not the R31 CMD TX_PUSH mode. Any update to R30 will trigger an TX PUSH.
10	RESERVED	R	0h	Reserved
9	TX_AUTO_SEQUENCE	R/W	0h	Enables transmit auto-sequence. Note the transmit data source is determined by TX_MUX_SEL setting. 0h: Disable 1h: Enable, transmit state machine based on events on receiver path that is connected to the respective transmitter. Also, the masking logic is disabled and only the MII data is used.
8	TX_MUX_SEL	R/W	0h	Selects transmit data source. The default/reset setting for TX Port 0 is 1. This setting permits MII TX Port 0 to receive data from PRU1 and the MII TX Port 1 which is connected to PRU0 by default. 0h: Data from PRU0 (default for PRU_ICSS_MII_RT_TXCFG1) 1h: Data from PRU1 (default for PRU_ICSS_MII_RT_TXCFG0)
7-4	RESERVED	R	0h	Reserved

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Table 4-416. PRU_ICSS_MII_RT_TXCFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TX_BYTE_SWAP	R/W	0h	Defines the order of Byte0/1 placement for TX R30. This bit must be selected/updated when the port is disabled or there is no traffic. 0h: If PRU_ICSS_MII_RT_TXCFG0/1 [TX_32_MODE_EN] = 0, R30[15:8] = Byte1{Nibble3,Nibble2} R30[7:0] = Byte0{Nibble1,Nibble0} R30[31:24] = TX_MASK[15:8] R30[23:16] = TX_MASK[7:0] If PRU_ICSS_MII_RT_TXCFG0/1 [TX_32_MODE_EN] = 1, R30[31:24] = Byte3{Nibble7,Nibble6} R30[23:16] = Byte2{Nibble5,Nibble4} R30[15:8] = Byte1{Nibble3,Nibble2} R30[7:0] = Byte0{Nibble1,Nibble0} 1h: If PRU_ICSS_MII_RT_TXCFG0/1 [TX_32_MODE_EN] = 0, R30[15:8] = Byte0{Nibble1,Nibble0} R30[7:0] = Byte1{Nibble3,Nibble2} R30[31:24] = TX_MASK[7:0] R30[23:16] = TX_MASK[15:8] If PRU_ICSS_MII_RT_TXCFG0/1 [TX_32_MODE_EN] = 1, (ONLY SUPPORT 32bit push) R30[31:24] = Byte0{Nibble1,Nibble0} R30[23:16] = Byte1{Nibble3,Nibble2} R30[15:8] = Byte2{Nibble5,Nibble4} R30[7:0] = Byte3{Nibble7,Nibble6 **Note Nibble0 is the first nibble received.**
2	TX_EN_MODE	R/W	0h	Enables transmit self clear on TX_EOF event. **Note that iep.cmp[3] must be set before transmission will start for TX0, and iep_cmp[4] for TX1. This is a new dependency, in addition to TX L1 FIFO not empty and TX_START_DELAY expiration, to start transmission.** 0h: Disable 1h: Enable, TX_ENABLE will be clear for a TX_EOF event by itself.
1	TX_AUTO_PREAMBLE	R/W	0h	Transmit data auto-preamble. 0h: PRU will provide full preamble 1h: TX FIFO will insert pre-amble automatically **Note: the TX FIFO does not get preloaded with the preamble until the first write occurs. This can cause the latency to be larger the min latency.**
0	TX_ENABLE	R/W	0h	Enables transmit traffic on TX PORT. If TX_EN_MODE is set, then TX_ENABLE will self clear during a TX_EOF event. Note Software can use this to pre-fill the TX FIFO and then start the TX frame during non-ECS operations. 0h: TX PORT is disabled/stopped immediately 1h: TX PORT is enabled and the frame will start once the IPG counter expired and TX Start Delay counter has expired

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4.5.8.5 PRU_ICSS_MII_RT_TX_CRC0 Register (Offset = 20h) [reset = 0h]

PRU_ICSS_MII_RT_TX_CRC0 is shown in Figure 4-189 and described in Table 4-418.

MII TXCRC 0 REGISTER
It contains CRC32 which PRU0 reads

Table 4-417. PRU_ICSS_MII_RT_TX_CRC0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2020h

Figure 4-189. PRU_ICSS_MII_RT_TX_CRC0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_CRC																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-418. PRU_ICSS_MII_RT_TX_CRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_CRC	R	0h	FCS (CRC32) data can be read by PRU for diagnostics. It is only valid after 6 clocks after a TX_CRC_HIGH command is given.

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4.5.8.6 PRU_ICSS_MII_RT_TX_CRC1 Register (Offset = 24h) [reset = 0h]

PRU_ICSS_MII_RT_TX_CRC1 is shown in Figure 4-190 and described in Table 4-420.

MII TXCRC 1 REGISTER
It contains CRC32 which PRU1 reads

Table 4-419. PRU_ICSS_MII_RT_TX_CRC1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2024h

Figure 4-190. PRU_ICSS_MII_RT_TX_CRC1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_CRC																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-420. PRU_ICSS_MII_RT_TX_CRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TX_CRC	R	0h	FCS (CRC32) data can be read by PRU for diagnostics. It is only valid after 6 clocks after a TX_CRC_HIGH command is given.

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4.5.8.7 PRU_ICSS_MII_RT_TX_IPG0 Register (Offset = 30h) [reset = 28h]

PRU_ICSS_MII_RT_TX_IPG0 is shown in Figure 4-191 and described in Table 4-422.

MII TXIPG 0 REGISTER

Table 4-421. PRU_ICSS_MII_RT_TX_IPG0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2030h

Figure 4-191. PRU_ICSS_MII_RT_TX_IPG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						TX_IPG									
R-0h																						R/W-28h									

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-422. PRU_ICSS_MII_RT_TX_IPG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	TX_IPG	R/W	28h	Defines the minimum of transmit Inter Packet Gap (IPG) which is the number of ICSS_i_VCLK_CLK (where i = 0 or 1) cycles between the de-assertion of TX_EN and the assertion of TX_EN. The start of the TX will get delayed when the incoming packet IPG is less than defined minimum value. In general, software should program in increments of 8, 40ns to insure the extra delays takes effect.

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4.5.8.8 PRU_ICSS_MII_RT_TX_IPG1 Register (Offset = 34h) [reset = 28h]

PRU_ICSS_MII_RT_TX_IPG1 is shown in Figure 4-192 and described in Table 4-424.

MII TXIPG 1 REGISTER

Table 4-423. PRU_ICSS_MII_RT_TX_IPG1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2034h

Figure 4-192. PRU_ICSS_MII_RT_TX_IPG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						TX_IPG									
R-0h																						R/W-28h									

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-424. PRU_ICSS_MII_RT_TX_IPG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	TX_IPG	R/W	28h	Defines the minimum of transmit Inter Packet Gap (IPG) which is the number of ICSS_i_VCLK_CLK (where i = 0 or 1) cycles between the de-assertion of TX_EN and the assertion of TX_EN. The start of the TX will get delayed when the incoming packet IPG is less than defined minimum value. In general, software should program in increments of 8, 40ns to insure the extra delays takes effect.

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4.5.8.9 PRU_ICSS_MII_RT_PRS0 Register (Offset = 38h) [reset = 0h]

PRU_ICSS_MII_RT_PRS0 is shown in Figure 4-193 and described in Table 4-426.

MII PORT STATUS 0 REGISTER

Table 4-425. PRU_ICSS_MII_RT_PRS0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2038h

Figure 4-193. PRU_ICSS_MII_RT_PRS0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						MII_CRS	MII_COL
R-0h						R-0h	R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 4-426. PRU_ICSS_MII_RT_PRS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	MII_CRS	R	0h	Read the current state of pr1_mii0_crs
0	MII_COL	R	0h	Read the current state of pr1_mii0_col

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4.5.8.10 PRU_ICSS_MII_RT_PRS1 Register (Offset = 3Ch) [reset = 0h]

PRU_ICSS_MII_RT_PRS1 is shown in Figure 4-194 and described in Table 4-428.

MII PORT STATUS 1 REGISTER

Table 4-427. PRU_ICSS_MII_RT_PRS1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 203Ch

Figure 4-194. PRU_ICSS_MII_RT_PRS1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						MII_CRS	MII_COL
R-0h						R-0h	R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 4-428. PRU_ICSS_MII_RT_PRS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	MII_CRS	R	0h	Read the current state of pr1_mii1_crs
0	MII_COL	R	0h	Read the current state of pr1_mii1_col

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4.5.8.11 PRU_ICSS_MII_RT_RX_FRMS0 Register (Offset = 40h) [reset = 05F1003Fh]

PRU_ICSS_MII_RT_RX_FRMS0 is shown in Figure 4-195 and described in Table 4-430.

MII RXFRMS 0 REGISTER

Table 4-429. PRU_ICSS_MII_RT_RX_FRMS0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2040h

Figure 4-195. PRU_ICSS_MII_RT_RX_FRMS0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MAX_FRM																RX_MIN_FRM															
R/W-5F1h																R/W-3Fh															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-430. PRU_ICSS_MII_RT_RX_FRMS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_MAX_FRM	R/W	5F1h	Defines the maximum received frame count. If the total byte count of received frame is more than defined value, RX_MAX_FRM_ERR will get set. 0h = 1 byte after SFD and including CRC N= N+1 bytes after SFD and including CRC. Note if the incoming frame is truncated at the marker, RX_CRC and RX_NIBBLE_ODD will not get asserted.
15-0	RX_MIN_FRM	R/W	3Fh	Defines the minimum received frame count. If the total byte count of received frame is less than defined value, RX_MIN_FRM_ERR will get set. 0h = 1 byte after SFD and including CRC N=N+1 bytes after SFD and including CRC

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4.5.8.12 PRU_ICSS_MII_RT_RX_FRMS1 Register (Offset = 44h) [reset = 05F1003Fh]

PRU_ICSS_MII_RT_RX_FRMS1 is shown in Figure 4-196 and described in Table 4-432.

MII RXFRMS 1 REGISTER

Table 4-431. PRU_ICSS_MII_RT_RX_FRMS1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2044h

Figure 4-196. PRU_ICSS_MII_RT_RX_FRMS1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MAX_FRM																RX_MIN_FRM															
R/W-5F1h																R/W-3Fh															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-432. PRU_ICSS_MII_RT_RX_FRMS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_MAX_FRM	R/W	5F1h	Defines the maximum received frame count. If the total byte count of the received frame is more than defined value, RX_MAX_FRM_ERR will get set. 0h = 1 byte after SFD and including CRC N= N+1 bytes after SFD and including CRC Note if the incoming frame is truncated at the marker, RX_CRC and RX_NIBBLE_ODD will not get asserted.
15-0	RX_MIN_FRM	R/W	3Fh	Defines the minimum received frame count. If the total byte count of received frame is less than defined value, RX_MIN_FRM_ERR will get set. 0h = 1 byte after SFD and including CRC N=N+1 bytes after SFD and including CRC

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4.5.8.13 PRU_ICSS_MII_RT_RX_PCNT0 Register (Offset = 48h) [reset = E1h]

PRU_ICSS_MII_RT_RX_PCNT0 is shown in Figure 4-197 and described in Table 4-434.

MII RXPCNT 0 REGISTER

Table 4-433. PRU_ICSS_MII_RT_RX_PCNT0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2048h

Figure 4-197. PRU_ICSS_MII_RT_RX_PCNT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_MAX_PCNT				RX_MIN_PCNT			
R-0h								R/W-Eh				R/W-1h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-434. PRU_ICSS_MII_RT_RX_PCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-4	RX_MAX_PCNT	R/W	Eh	Defines the maximum number of nibbles until the start of frame delimiter (SFD) event occurred (i.e. matches 0xD5). RX_MAX_PRE_COUNT_ERR will be set if the preamble counts more than the value of RX_MAX_PCNT. If the SFD does not occur within 16 nibbles, the error will assert and the incoming frame will be truncated. 0h: Disabled 1h: Reserved 2h: 4th nibble needs to have built 0xD5 Eh: 16th nibble needs to have built 0xD5 **Note the 16th nibble is transmitted.** **Note for firmware enabling preamble error detection, it is recommended to keep RX_MAX_PCNT disabled (0x0). Otherwise, hardware can truncate a valid frame with too long of a preamble.**
3-0	RX_MIN_PCNT	R/W	1h	Defines the minimum number of nibbles until the start of frame delimiter (SFD) event occurred, which is matched the value 0xD5. RX_MIN_PRE_COUNT_ERR will be set if the preamble counts less than the value of RX_MIN_PCNT. 0h: Disabled 1h: 1 0x5 before 0xD5 2h: 2 0x5 before 0xD5 N min of N 0x5 before 0xD5 **Note it does not need to be "0x5"**

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4.5.8.14 PRU_ICSS_MII_RT_RX_PCNT1 Register (Offset = 4Ch) [reset = E1h]

PRU_ICSS_MII_RT_RX_PCNT1 is shown in Figure 4-198 and described in Table 4-436.

MII RXPCNT 1 REGISTER

Table 4-435. PRU_ICSS_MII_RT_RX_PCNT1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 204Ch

Figure 4-198. PRU_ICSS_MII_RT_RX_PCNT1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_MAX_PCNT				RX_MIN_PCNT			
R-0h								R/W-Eh				R/W-1h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-436. PRU_ICSS_MII_RT_RX_PCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-4	RX_MAX_PCNT	R/W	Eh	Defines the maximum number of nibbles until the start of frame delimiter (SFD) event occurred (i.e. matches 0xD5). RX_MAX_PRE_COUNT_ERR will be set if the preamble counts more than the value of RX_MAX_PCNT. If the SFD does not occur within 16 nibbles, the error will assert and the incoming frame will be truncated. 0h: Disabled 1h: Reserved 2h: 4th nibble needs to have built 0xD5 Eh: 16th nibble needs to have built 0xD5 **Note the 16th nibble is transmitted** Note for firmware enabling preamble error detection, it is recommended to keep RX_MAX_PCNT disabled (0x0). Otherwise, hardware can truncate a valid frame with too long of a preamble.
3-0	RX_MIN_PCNT	R/W	1h	Defines the minimum number of nibbles until the start of frame delimiter (SFD) event occurred, which is matched the value 0xD5. RX_MIN_PRE_COUNT_ERR will be set if the preamble counts less than the value of RX_MIN_PCNT. 0h Disabled 1h: 1 0x5 before 0xD5 2h: 2 0x5 before 0xD5 N: N 0x5 before 0xD5 **Note it does not need to be "0x5"**

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4.5.8.15 PRU_ICSS_MII_RT_RX_ERR0 Register (Offset = 50h) [reset = 0h]

PRU_ICSS_MII_RT_RX_ERR0 is shown in Figure 4-199 and described in Table 4-438.

MII RXERR 0 REGISTER

Table 4-437. PRU_ICSS_MII_RT_RX_ERR0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2050h

Figure 4-199. PRU_ICSS_MII_RT_RX_ERR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				RX_MAX_FRM_ERR	RX_MIN_FRM_ERR	RX_MAX_PCNT_ERR	RX_MIN_PCNT_ERR
R-0h				RWr1Clr-0h	RWr1Clr-0h	RWr1Clr-0h	RWr1Clr-0h

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-438. PRU_ICSS_MII_RT_RX_ERR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	RX_MAX_FRM_ERR	RWr1Clr	0h	Error status of received frame is more than the value of RX_MAX_FRM. 0h: No error occurred 1h: Error occurred Write 1 to Clear
2	RX_MIN_FRM_ERR	RWr1Clr	0h	Error status of received frame is less than the value of RX_MIN_FRM. 0h: No error occurred 1h: Error occurred Write 1 to Clear
1	RX_MAX_PCNT_ERR	RWr1Clr	0h	Error status of received preamble nibble is more than the value of RX_MAX_PCNT. 0h: No error occurred 1h: Error occurred Write 1 to Clear
0	RX_MIN_PCNT_ERR	RWr1Clr	0h	Error status of received preamble nibble is less than the value of RX_MIN_PCNT. 0h: No error occurred 1h: Error occurred Write 1 to Clear

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4.5.8.16 PRU_ICSS_MII_RT_RX_ERR1 Register (Offset = 54h) [reset = 0h]

PRU_ICSS_MII_RT_RX_ERR1 is shown in Figure 4-200 and described in Table 4-440.

MII RXERR 1 REGISTER

Table 4-439. PRU_ICSS_MII_RT_RX_ERR1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2054h

Figure 4-200. PRU_ICSS_MII_RT_RX_ERR1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				RX_MAX_FRM_ERR	RX_MIN_FRM_ERR	RX_MAX_PCNT_ERR	RX_MIN_PCNT_ERR
R-0h				RWr1Clr-0h	RWr1Clr-0h	RWr1Clr-0h	RWr1Clr-0h

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-440. PRU_ICSS_MII_RT_RX_ERR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	RX_MAX_FRM_ERR	RWr1Clr	0h	Error status of received frame is more than the value of RX_MAX_FRM_CNT. 0h: No error occurred 1h: Error occurred Write 1 to Clear
2	RX_MIN_FRM_ERR	RWr1Clr	0h	Error status of received frame is less than the value of RX_MIN_FRM_CNT. 0h: No error occurred 1h: Error occurred Write 1 to Clear
1	RX_MAX_PCNT_ERR	RWr1Clr	0h	Error status of received preamble nibble is more than the value of RX_MAX_PCNT. 0h: No error occurred 1h: Error occurred Write 1 to Clear
0	RX_MIN_PCNT_ERR	RWr1Clr	0h	Error status of received preamble nibble is less than the value of RX_MIN_PCNT. 0h: No error occurred 1h: Error occurred Write 1 to Clear

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4.5.8.17 PRU_ICSS_MII_RT_RXFLV0 Register (Offset = 60h) [reset = 0h]

PRU_ICSS_MII_RT_RXFLV0 is shown in Figure 4-201 and described in Table 4-442.

MII PRU_ICSS_MII_RT_RXFLV0 REGISTER
This register defines the number of valid bytes in the RX FIFO MII interface port 0.
PRU_ICSS_MII_RT_RXFLV0 is attached to Port RX0.
PRU_ICSS_MII_RT_RXFLV0 controls which PRU is selected for RX0

Table 4-441. PRU_ICSS_MII_RT_RXFLV0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2060h

Figure 4-201. PRU_ICSS_MII_RT_RXFLV0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_FIFO_LEVEL							
R-0h								RWr1Clr-0h							

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-442. PRU_ICSS_MII_RT_RXFLV0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	RX_FIFO_LEVEL	RWr1Clr	0h	Define the number of valid bytes in the RX FIFO. 0h: Empty 1h: 1 Byte/ 2 Nibbles 2h: 2 Byte/ 4 Nibbles .... 32h: 32 Bytes/ 64 Nibbles

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4.5.8.18 PRU_ICSS_MII_RT_RXFLV1 Register (Offset = 64h) [reset = 0h]

PRU_ICSS_MII_RT_RXFLV1 is shown in Figure 4-202 and described in Table 4-444.

MII PRU_ICSS_MII_RT_RXFLV1 REGISTER
This register defines the number of valid bytes in the RX FIFO MII interface port 1.
PRU_ICSS_MII_RT_RXFLV1 is attached to Port RX1.
PRU_ICSS_MII_RT_RXFLV1 controls which PRU is selected for RX1

Table 4-443. PRU_ICSS_MII_RT_RXFLV1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2064h

Figure 4-202. PRU_ICSS_MII_RT_RXFLV1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_FIFO_LEVEL							
R-0h								RWr1Clr-0h							

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-444. PRU_ICSS_MII_RT_RXFLV1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	RX_FIFO_LEVEL	RWr1Clr	0h	Define the number of valid bytes in the RX FIFO. 0h: Empty 1h: 1 Byte/ 2 Nibbles 2h: 2 Byte/ 4 Nibbles .... 32h: 32 Bytes/ 64 Nibbles

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4.5.8.19 PRU_ICSS_MII_RT_TXFLV0 Register (Offset = 68h) [reset = 0h]

PRU_ICSS_MII_RT_TXFLV0 is shown in Figure 4-203 and described in Table 4-446.

MII PRU_ICSS_MII_RT_TXFLV0 REGISTER
This register defines the number of valid bytes in the TX FIFO MII interface port 0.
PRU_ICSS_MII_RT_TXFLV0 is attached to Port TX0.
PRU_ICSS_MII_RT_TXFLV0 controls which PRU is selected for TX0.

Table 4-445. PRU_ICSS_MII_RT_TXFLV0 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 2068h

Figure 4-203. PRU_ICSS_MII_RT_TXFLV0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TX_FIFO_LEVEL							
R-0h								RWr1Clr-0h							

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-446. PRU_ICSS_MII_RT_TXFLV0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	TX_FIFO_LEVEL	RWr1Clr	0h	Define the number of valid nibbles in the TX FIFO. 0h: Empty 1h: 1 Nibble 2h: 1 Byte/ 2 Nibbles .... 128h: 64 Bytes/ 128 Nibbles .... 192h: 96 Bytes/ 192 Nibbles

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4.5.8.20 PRU_ICSS_MII_RT_TXFLV1 Register (Offset = 6Ch) [reset = 0h]

PRU_ICSS_MII_RT_TXFLV1 is shown in Figure 4-204 and described in Table 4-448.

MII PRU_ICSS_MII_RT_TXFLV1 REGISTER
This register defines the number of valid bytes in the TX FIFO MII interface port 1.
PRU_ICSS_MII_RT_TXFLV1 is attached to Port TX1.
PRU_ICSS_MII_RT_TXFLV1 controls which PRU is selected for TX1.

Table 4-447. PRU_ICSS_MII_RT_TXFLV1 Instances

Instance	Physical Address
PRU_ICSS_MII_RT	4803 206Ch

Figure 4-204. PRU_ICSS_MII_RT_TXFLV1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TX_FIFO_LEVEL							
R-0h								RWr1Clr-0h							

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-448. PRU_ICSS_MII_RT_TXFLV1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	TX_FIFO_LEVEL	RWr1Clr	0h	Define the number of valid nibbles in the TX FIFO. 0h: Empty 1h: 1 Nibble 2h: 1 Byte/ 2 Nibble .... 128h: 64 Bytes/ 128 Nibbles .... 192h: 96 Bytes/ 192 Nibbles

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4.5.9 PRU_ICSS_MII_MDIO Registers

PRU_ICSS_MII_MDIO Registers lists the memory-mapped registers for the PRU_ICSS MII MDIO. All register offset addresses not listed in PRU_ICSS_MII_MDIO Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-449. PRU_ICSS MII MDIO Instances

Instance	Base Address
PRU_ICSS_MII_MDIO	4803 2400h

Table 4-450. PRU_ICSS MII MDIO Registers

Offset	Acronym	Register Name	PRU_ICSS_MII_MDIO Physical Address
0h	PRU_ICSS_MII_MDIO_VER	MDIO MODULE VERSION REGISTER	4803 2400h
4h	PRU_ICSS_MII_MDIO_CONTROL	MDIO MODULE CONTROL REGISTER	4803 2404h
8h	PRU_ICSS_MII_MDIO_ALIV	PHY ACKNOWLEDGE STATUS REGISTER	4803 2408h
Ch	PRU_ICSS_MII_MDIO_LINK	PHY LINK STATUS REGISTER	4803 240Ch
10h	PRU_ICSS_MII_MDIO_LINKINTRAW	LINK STATUS CHANGE INTERRUPT REGISTER (RAW VALUE)	4803 2410h
14h	PRU_ICSS_MII_MDIO_LINKINTMASKED	LINK STATUS CHANGE INTERRUPT REGISTER (MASKED VALUE)	4803 2414h
20h	PRU_ICSS_MII_MDIO_USERINTRAW	USER COMMAND COMPLETE INTERRUPT REGISTER (RAW VALUE)	4803 2420h
24h	PRU_ICSS_MII_MDIO_USERINTMASKED	USER COMMAND COMPLETE INTERRUPT REGISTER (MASKED VALUE)	4803 2424h
28h	PRU_ICSS_MII_MDIO_USERINTMASKSET	USER INTERRUPT MASK SET REGISTER	4803 2428h
2Ch	PRU_ICSS_MII_MDIO_USERINTMASKCLR	USER INTERRUPT MASK CLEAR REGISTER	4803 242Ch
80h	PRU_ICSS_MII_MDIO_USERACCESS0	USER ACCESS REGISTER0	4803 2480h
84h	PRU_ICSS_MII_MDIO_USERPHYSEL0	USER PHY SELECT REGISTER0	4803 2484h
88h	PRU_ICSS_MII_MDIO_USERACCESS1	USER ACCESS REGISTER1	4803 2488h
8Ch	PRU_ICSS_MII_MDIO_USERPHYSEL1	USER PHY SELECT REGISTER1	4803 248Ch

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4.5.9.1 PRU_ICSS_MII_MDIO_VER Register (Offset = 0h) [reset = -h]

PRU_ICSS_MII_MDIO_VER is shown in Figure 4-205 and described in Table 4-452.

MDIO MODULE VERSION REGISTER

Table 4-451. PRU_ICSS_MII_MDIO_VER Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2400h

Figure 4-205. PRU_ICSS_MII_MDIO_VER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															
R--h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-452. PRU_ICSS_MII_MDIO_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REVISION	R	-h	IP Revision.

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4.5.9.2 PRU_ICSS_MII_MDIO_CONTROL Register (Offset = 4h) [reset = 810000FFh]

PRU_ICSS_MII_MDIO_CONTROL is shown in Figure 4-206 and described in Table 4-454.

MDIO MODULE CONTROL REGISTER

Table 4-453. PRU_ICSS_MII_MDIO_CONTROL Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2404h

Figure 4-206. PRU_ICSS_MII_MDIO_CONTROL Register

31	30	29	28	27	26	25	24
IDLE	ENABLE	RESERVED	HIGHEST_USER_CHANNEL				
R-1h	R/W-0h	R-0h	R-1h				
23	22	21	20	19	18	17	16
RESERVED			PREAMBLE	FAULT	FAULT_DETECT_ENABLE	INT_TEST_ENABLE	RESERVED
R-0h			R/W-0h	RWr1Clr-0h	R/W-0h	R/W-0h	R-0h
15	14	13	12	11	10	9	8
CLKDIV							
R/W-FFh							
7	6	5	4	3	2	1	0
CLKDIV							
R/W-FFh							

LEGEND: R = Read Only; R/W = Read/Write; RWr1Clr = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 4-454. PRU_ICSS_MII_MDIO_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	MDIO state machine IDLE. Set to 1 when the state machine is in the idle state.
30	ENABLE	R/W	0h	Enable control. Writing a 1 to this bit enables the MDIO state machine, writing a 0 disables it. If the MDIO state machine is active at the time it is disabled, it will complete the current operation before halting and setting the idle bit. If using byte access, the enable bit has to be the last bit written in this register.
29	RESERVED	R	0h	Reserved
28-24	HIGHEST_USER_CHANNEL	R	1h	Highest user channel. This field specifies the highest useraccess channel that is available in the module and is currently set to 1. This implies that **MDIOUserAccess1** is the highest available user access channel.
23-21	RESERVED	R	0h	Reserved
20	PREAMBLE	R/W	0h	Preamble disable. Writing a 1 to this bit disables this device from sending MDIO frame preambles.
19	FAULT	RWr1Clr	0h	Fault indicator. This bit is set to 1 if the MDIO pins fail to read back what the device is driving onto them. This indicates a physical layer fault and the module state machine is reset. Writing a 1 to it clears this bit.
18	FAULT_DETECT_ENABLE	R/W	0h	Fault detect enable. This bit has to be set to 1 to enable the physical layer fault detection.

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Table 4-454. PRU_ICSS_MII_MDIO_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	INT_TEST_ENABLE	R/W	0h	Interrupt test enable. This bit can be set to 1 to enable the host to set the userint and linkint bits for test purposes.
16	RESERVED	R	0h	Reserved
15-0	CLKDIV	R/W	FFh	Clock Divider. This field specifies the division ratio between CLK and the frequency of MDCLK. MDCLK is disabled when clkdiv is set to 0. MDCLK frequency = clk frequency/(clkdiv+1).

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4.5.9.3 PRU_ICSS_MII_MDIO_ALIVE Register (Offset = 8h) [reset = 0h]

PRU_ICSS_MII_MDIO_ALIVE is shown in Figure 4-207 and described in Table 4-456.

PHY ACKNOWLEDGE STATUS REGISTER

Table 4-455. PRU_ICSS_MII_MDIO_ALIVE Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2408h

Figure 4-207. PRU_ICSS_MII_MDIO_ALIVE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALIVE																															
RWr1Clr-0h																															

LEGEND: RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-456. PRU_ICSS_MII_MDIO_ALIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ALIVE	RWr1Clr	0h	MDIO Alive bitfield. Each of the 32 bits of this register is set if the most recent access to the PHY with address corresponding to the register bit number was acknowledged by the PHY, the bit is reset if the PHY fails to acknowledge the access. Both the user and polling accesses to a PHY will cause the corresponding alive bit to be updated. The alive bits are only meant to be used to give an indication of the presence or not of a PHY with the corresponding address. Writing a 1 to any bit will clear it, writing a 0 has no effect.

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4.5.9.4 PRU_ICSS_MII_MDIO_LINK Register (Offset = Ch) [reset = 0h]

PRU_ICSS_MII_MDIO_LINK is shown in Figure 4-208 and described in Table 4-458.

PHY LINK STATUS REGISTER

Table 4-457. PRU_ICSS_MII_MDIO_LINK Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 240Ch

Figure 4-208. PRU_ICSS_MII_MDIO_LINK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LINK																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-458. PRU_ICSS_MII_MDIO_LINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LINK	R	0h	MDIO Link state. This register is updated after a read of the Generic Status Register of a PHY. The bit is set if the PHY with the corresponding address has link and the PHY acknowledges the read transaction. The bit is reset if the PHY indicates it does not have link or fails to acknowledge the read transaction. Writes to the register have no effect. In addition, the status of the two PHYs specified in the **MDIOUserPhySel** registers can be determined using the **MLINK** input pins. This is determined by the **linksel** bit in the **MDIOUserPhySel** register.

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4.5.9.5 PRU_ICSS_MII_MDIO_LINKINTRAW Register (Offset = 10h) [reset = 0h]

PRU_ICSS_MII_MDIO_LINKINTRAW is shown in Figure 4-209 and described in Table 4-460.

LINK STATUS CHANGE INTERRUPT REGISTER (RAW VALUE)

Table 4-459. PRU_ICSS_MII_MDIO_LINKINTRAW Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2410h

Figure 4-209. PRU_ICSS_MII_MDIO_LINKINTRAW Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						LINKINTRAW	
R-0h						RWr1Clr-0h	

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-460. PRU_ICSS_MII_MDIO_LINKINTRAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LINKINTRAW	RWr1Clr	0h	MDIO link change event, raw value. When asserted 1 , a bit indicates that there was an **MDIO link** change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the **MDIOUserPhySel** register. **linkintraw[0] and linkintraw[1]** correspond to **MDIOUserPhySel0 and MDIOUserPhysel1**, respectively. Writing a 1 will clear the event and writing 0 has no effect.**If the int_test bit in the MDIOControl register is set, the host may set the linkintraw bits to a 1 .**This mode may be used for test purposes.

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4.5.9.6 PRU_ICSS_MII_MDIO_LINKINTMASKED Register (Offset = 14h) [reset = 0h]

PRU_ICSS_MII_MDIO_LINKINTMASKED is shown in Figure 4-210 and described in Table 4-462.

LINK STATUS CHANGE INTERRUPT REGISTER (MASKED VALUE)

Table 4-461. PRU_ICSS_MII_MDIO_LINKINTMASKED Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2414h

Figure 4-210. PRU_ICSS_MII_MDIO_LINKINTMASKED Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						LINKINTMASKED	
R-0h						RWr1Clr-0h	

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-462. PRU_ICSS_MII_MDIO_LINKINTMASKED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LINKINTMASKED	RWr1Clr	0h	MDIO link change interrupt, masked value. When asserted 1 , a bit indicates that there was an MDIO link change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the MDIOUserPhySel register and the corresponding linkint_enable bit was set. linkintmasked[0] and linkintmasked[1] correspond to MDIOUserPhySel0 and MDIOUserPhysel1, respectively. Writing a 1 will clear the interrupt and writing 0 has no effect. If the int_test bit in the MDIOControl register is set, the host may set the linkint bits to a 1 . This mode may be used for test purposes.

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4.5.9.7 PRU_ICSS_MII_MDIO_USERINTRAW Register (Offset = 20h) [reset = 0h]

PRU_ICSS_MII_MDIO_USERINTRAW is shown in Figure 4-211 and described in Table 4-464.

USER COMMAND COMPLETE INTERRUPT REGISTER (RAW VALUE)

Table 4-463. PRU_ICSS_MII_MDIO_USERINTRAW Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2420h

Figure 4-211. PRU_ICSS_MII_MDIO_USERINTRAW Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTRAW	
R-0h						RWr1Clr-0h	

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-464. PRU_ICSS_MII_MDIO_USERINTRAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	USERINTRAW	RWr1Clr	0h	Raw value of MDIO user command complete event for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted 1 , a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed. Writing a 1 will clear the event and writing 0 has no effect. . If the int_test bit in the MDIOControl register is set, the host may set the userintraw bits to a 1 . This mode may be used for test purposes.

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4.5.9.8 PRU_ICSS_MII_MDIO_USERINTMASKED Register (Offset = 24h) [reset = 0h]

PRU_ICSS_MII_MDIO_USERINTMASKED is shown in Figure 4-212 and described in Table 4-466.

USER COMMAND COMPLETE INTERRUPT REGISTER (MASKED VALUE)

Table 4-465. PRU_ICSS_MII_MDIO_USERINTMASKED Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2424h

Figure 4-212. PRU_ICSS_MII_MDIO_USERINTMASKED Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKED	
R-0h						RWr1Clr-0h	

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-466. PRU_ICSS_MII_MDIO_USERINTMASKED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	USERINTMASKED	RWr1Clr	0h	Masked value of MDIO user command complete interrupt for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted 1 , a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed and the corresponding userintmaskset bit is set to 1 . . Writing a 1 will clear the interrupt and writing 0 has no effect. . If the int_test bit in the MDIOControl register is set, the host may set the userintmasked bits to a 1 . This mode may be used for test purposes.

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4.5.9.9 PRU_ICSS_MII_MDIO_USERINTMASKSET Register (Offset = 28h) [reset = 0h]

PRU_ICSS_MII_MDIO_USERINTMASKSET is shown in Figure 4-213 and described in Table 4-468.

USER INTERRUPT MASK SET REGISTER

Table 4-467. PRU_ICSS_MII_MDIO_USERINTMASKSET Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2428h

Figure 4-213. PRU_ICSS_MII_MDIO_USERINTMASKSET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKEDSET	
R-0h						R/W1S-0h	

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 4-468. PRU_ICSS_MII_MDIO_USERINTMASKSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	USERINTMASKEDSET	R/W1S	0h	MDIO user interrupt mask set for userintmasked[1:0], respectively. Writing a bit to 1 will enable MDIO user command complete interrupts for that particular MDIOUserAccess register. MDIO user interrupt for a particular MDIOUserAccess register is disabled if the corresponding bit is 0 . Writing a 0 to this register has no effect.

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4.5.9.10 PRU_ICSS_MII_MDIO_USERINTMASKCLR Register (Offset = 2Ch) [reset = 0h]

PRU_ICSS_MII_MDIO_USERINTMASKCLR is shown in Figure 4-214 and described in Table 4-470.

USER INTERRUPT MASK CLEAR REGISTER

Table 4-469. PRU_ICSS_MII_MDIO_USERINTMASKCLR Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 242Ch

Figure 4-214. PRU_ICSS_MII_MDIO_USERINTMASKCLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						USERINTMASKEDCLR	
R-0h						RWr1Clr-0h	

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-470. PRU_ICSS_MII_MDIO_USERINTMASKCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	USERINTMASKEDCLR	RWr1Clr	0h	MDIO user command complete interrupt mask clear for userintmasked[1:0], respectively. Writing a bit to 1 will disable further user command complete interrupts for that particular MDIOUserAccess register. Writing a 0 to this register has no effect.

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4.5.9.11 PRU_ICSS_MII_MDIO_USERACCESS0 Register (Offset = 80h) [reset = 0h]

PRU_ICSS_MII_MDIO_USERACCESS0 is shown in Figure 4-215 and described in Table 4-472.

USER ACCESS REGISTER0

Table 4-471. PRU_ICSS_MII_MDIO_USERACCESS0 Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2480h

Figure 4-215. PRU_ICSS_MII_MDIO_USERACCESS0 Register

31	30	29	28	27	26	25	24
GO	WRITE	ACK	RESERVED			REGADR	
R/W1S-0h	R/W-0h	R/W-0h	R-0h			R/W-0h	
23	22	21	20	19	18	17	16
REGADR			PHYADR				
R/W-0h			R/W-0h				
15	14	13	12	11	10	9	8
DATA							
R/W-0h							
7	6	5	4	3	2	1	0
DATA							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 4-472. PRU_ICSS_MII_MDIO_USERACCESS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GO	R/W1S	0h	Go. Writing a 1 to this bit causes the MDIO state machine to perform an MDIO access when it is convenient for it to do so, this is not an instantaneous process. Writing a 0 to this bit has no effect. This bit is write able only if the MDIO state machine is enabled. This bit will self clear when the requested access has been completed. Any writes to the MDIOUserAccess0 register are blocked when the go bit is 1 . If byte access is being used, the go bit should be written last.
30	WRITE	R/W	0h	Write enable. Setting this bit to a 1 causes the MDIO transaction to be a register write, otherwise it is a register read.
29	ACK	R/W	0h	Acknowledge. This bit is set if the PHY acknowledged the read transaction.
28-26	RESERVED	R	0h	Reserved
25-21	REGADR	R/W	0h	Register address. This field specifies the PHY register to be accessed for this transaction.
20-16	PHYADR	R/W	0h	PHY address. This field specifies the PHY to be accessed for this transaction.
15-0	DATA	R/W	0h	User data. The data value read from or to be written to the specified PHY register.

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4.5.9.12 PRU_ICSS_MII_MDIO_USERPHYSEL0 Register (Offset = 84h) [reset = 0h]

PRU_ICSS_MII_MDIO_USERPHYSEL0 is shown in Figure 4-216 and described in Table 4-474.

USER PHY SELECT REGISTER0

Table 4-473. PRU_ICSS_MII_MDIO_USERPHYSEL0 Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2484h

Figure 4-216. PRU_ICSS_MII_MDIO_USERPHYSEL0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
LINKSEL	LINKINT_ENABLE	RESERVED	PHYADR_MON				
R/W-0h	R/W-0h	R-0h	R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-474. PRU_ICSS_MII_MDIO_USERPHYSEL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	LINKSEL	R/W	0h	Link status determination select. Set to 1 to determine link status using the MLINK pin. Default value is 0 which implies that the link status is determined by the MDIO state machine.
6	LINKINT_ENABLE	R/W	0h	Link change interrupt enable. Set to 1 to enable link change status interrupts for PHY address specified in phyadr_mon. Link change interrupts are disabled if this bit is set to 0 .
5	RESERVED	R	0h	Reserved
4-0	PHYADR_MON	R/W	0h	PHY address whose link status is to be monitored.

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4.5.9.13 PRU_ICSS_MII_MDIO_USERACCESS1 Register (Offset = 88h) [reset = 0h]

PRU_ICSS_MII_MDIO_USERACCESS1 is shown in Figure 4-217 and described in Table 4-476.

USER ACCESS REGISTER1

Table 4-475. PRU_ICSS_MII_MDIO_USERACCESS1 Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 2488h

Figure 4-217. PRU_ICSS_MII_MDIO_USERACCESS1 Register

31	30	29	28	27	26	25	24
GO	WRITE	ACK	RESERVED			REGADR	
R/W-0h	R/W-0h	R/W-0h	R-0h			R/W-0h	
23	22	21	20	19	18	17	16
REGADR			PHYADR				
R/W-0h			R/W-0h				
15	14	13	12	11	10	9	8
DATA							
R/W-0h							
7	6	5	4	3	2	1	0
DATA							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-476. PRU_ICSS_MII_MDIO_USERACCESS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GO	R/W	0h	Go. Writing a 1 to this bit causes the MDIO state machine to perform an MDIO access when it is convenient for it to do so, this is not an instantaneous process. Writing a 0 to this bit has no effect. This bit is write able only if the MDIO state machine is enabled. This bit will self clear when the requested access has been completed. Any writes to the MDIOUserAccess0 register are blocked when the go bit is 1 . If byte access is being used, the go bit should be written last.
30	WRITE	R/W	0h	Write enable. Setting this bit to a 1 causes the MDIO transaction to be a register write, otherwise it is a register read.
29	ACK	R/W	0h	Acknowledge. This bit is set if the PHY acknowledged the read transaction.
28-26	RESERVED	R	0h	Reserved
25-21	REGADR	R/W	0h	Register address. This field specifies the PHY register to be accessed for this transaction.
20-16	PHYADR	R/W	0h	PHY address. This field specifies the PHY to be accessed for this transaction.
15-0	DATA	R/W	0h	User data. The data value read from or to be written to the specified PHY register.

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4.5.9.14 PRU_ICSS_MII_MDIO_USERPHYSEL1 Register (Offset = 8Ch) [reset = 0h]

PRU_ICSS_MII_MDIO_USERPHYSEL1 is shown in Figure 4-218 and described in Table 4-478.

USER PHY SELECT REGISTER1

Table 4-477. PRU_ICSS_MII_MDIO_USERPHYSEL1 Instances

Instance	Physical Address
PRU_ICSS_MII_MDIO	4803 248Ch

Figure 4-218. PRU_ICSS_MII_MDIO_USERPHYSEL1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
LINKSEL	LINKINT_ENABLE	RESERVED	PHYADR_MON				
R/W-0h	R/W-0h	R-0h	R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-478. PRU_ICSS_MII_MDIO_USERPHYSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	LINKSEL	R/W	0h	Link status determination select. Set to 1 to determine link status using the MLINK pin. Default value is 0 which implies that the link status is determined by the MDIO state machine.
6	LINKINT_ENABLE	R/W	0h	Link change interrupt enable. Set to 1 to enable link change status interrupts for PHY address specified in phyadr_mon. Link change interrupts are disabled if this bit is set to 0 .
5	RESERVED	R	0h	Reserved
4-0	PHYADR_MON	R/W	0h	PHY address whose link status is to be monitored.

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4.5.10 PRU_ICSS_IEP Registers

PRU_ICSS_IEP Registers lists the memory-mapped registers for the PRU_ICSS_IEP module. All register offset addresses not listed in PRU_ICSS_IEP Registers should be considered as reserved locations and the register contents should not be modified.

Table 4-479. PRU_ICSS_IEP Instances

Instance	Base Address
PRU_ICSS_IEP	4802 E000h

Table 4-480. PRU_ICSS_IEP Registers

Offset	Acronym	Register Name	PRU_ICSS_IEP Physical Address
0h	PRU_ICSS_IEP_GLOBAL_CFG	GLOBAL CFG	4802 E000h
4h	PRU_ICSS_IEP_STATUS	STATUS	4802 E004h
8h	PRU_ICSS_IEP_COMPENSATION	COMPENSATION	4802 E008h
Ch	PRU_ICSS_IEP_SLOW_COMPENSATION	SLOW COMPENSATION	4802 E00Ch
10h	PRU_ICSS_IEP_LOW_COUNTER	64 bit count value low	4802 E010h
14h	PRU_ICSS_IEP_HIGH_COUNTER	64 bit count value high	4802 E014h
18h	PRU_ICSS_IEP_CAPTURE_CFG	CAPTURE CFG	4802 E018h
1Ch	PRU_ICSS_IEP_CAPTURE_STATUS	CAPTURE STATUS	4802 E01Ch
20h	PRU_ICSS_IEP_CAPTURE_RISE00	CAPTURE RISE0 low	4802 E020h
24h	PRU_ICSS_IEP_CAPTURE_RISE10	CAPTURE RISE0 high	4802 E024h
28h	PRU_ICSS_IEP_CAPTURE_RISE01	CAPTURE RISE1 low	4802 E028h
2Ch	PRU_ICSS_IEP_CAPTURE_RISE11	CAPTURE RISE1 high	4802 E02Ch
30h	PRU_ICSS_IEP_CAPTURE_RISE02	CAPTURE RISE2 low	4802 E030h
34h	PRU_ICSS_IEP_CAPTURE_RISE12	CAPTURE RISE2 high	4802 E034h
38h	PRU_ICSS_IEP_CAPTURE_RISE03	CAPTURE RISE3 low	4802 E038h
3Ch	PRU_ICSS_IEP_CAPTURE_RISE13	CAPTURE RISE3 high	4802 E03Ch
40h	PRU_ICSS_IEP_CAPTURE_RISE04	CAPTURE RISE4 low	4802 E040h
44h	PRU_ICSS_IEP_CAPTURE_RISE14	CAPTURE RISE4 high	4802 E044h
48h	PRU_ICSS_IEP_CAPTURE_RISE05	CAPTURE RISE5 low	4802 E048h
4Ch	PRU_ICSS_IEP_CAPTURE_RISE15	CAPTURE RISE5 high	4802 E04Ch
50h	PRU_ICSS_IEP_CAPTURE_RISE06	CAPTURE RISE6 low	4802 E050h
54h	PRU_ICSS_IEP_CAPTURE_RISE16	CAPTURE RISE6 high	4802 E054h
58h	PRU_ICSS_IEP_CAPTURE_FALL06	CAPTURE FALL6 low	4802 E058h
5Ch	PRU_ICSS_IEP_CAPTURE_FALL16	CAPTURE FALL6 high	4802 E05Ch
60h	PRU_ICSS_IEP_CAPTURE_RISE07	CAPTURE RISE7 low	4802 E060h
64h	PRU_ICSS_IEP_CAPTURE_RISE17	CAPTURE RISE7 high	4802 E064h
68h	PRU_ICSS_IEP_CAPTURE_FALL07	CAPTURE FALL7 low	4802 E068h
6Ch	PRU_ICSS_IEP_CAPTURE_FALL17	CAPTURE FALL7 high	4802 E06Ch
70h	PRU_ICSS_IEP_COMPARE_CFG	COMPARE CFG	4802 E070h
74h	PRU_ICSS_IEP_COMPARE_STATUS	COMPARE STATUS	4802 E074h
78h	PRU_ICSS_IEP_COMPARE00	COMPARE0 low	4802 E078h
7Ch	PRU_ICSS_IEP_COMPARE10	COMPARE0 high	4802 E07Ch
80h	PRU_ICSS_IEP_COMPARE01	COMPARE1 low	4802 E080h
84h	PRU_ICSS_IEP_COMPARE11	COMPARE1 high	4802 E084h
88h	PRU_ICSS_IEP_COMPARE02	COMPARE2 low	4802 E088h
8Ch	PRU_ICSS_IEP_COMPARE12	COMPARE2 high	4802 E08Ch
90h	PRU_ICSS_IEP_COMPARE03	COMPARE3 low	4802 E090h
94h	PRU_ICSS_IEP_COMPARE13	COMPARE3 high	4802 E094h

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Table 4-480. PRU_ICSS_IEP Registers (continued)

Offset	Acronym	Register Name	PRU_ICSS_IEP Physical Address
98h	PRU_ICSS_IEP_COMPARE04	COMPARE4 low	4802 E098h
9Ch	PRU_ICSS_IEP_COMPARE14	COMPARE4 high	4802 E09Ch
A0h	PRU_ICSS_IEP_COMPARE05	COMPARE5 low	4802 E0A0h
A4h	PRU_ICSS_IEP_COMPARE15	COMPARE5 high	4802 E0A4h
A8h	PRU_ICSS_IEP_COMPARE06	COMPARE6 low	4802 E0A8h
ACh	PRU_ICSS_IEP_COMPARE16	COMPARE6 high	4802 E0ACh
B0h	PRU_ICSS_IEP_COMPARE07	COMPARE7 low	4802 E0B0h
B4h	PRU_ICSS_IEP_COMPARE17	COMPARE7 high	4802 E0B4h
B8h	PRU_ICSS_IEP_RXIPG0	Status for the RX port which is attached to PRU0	4802 E0B8h
BCh	PRU_ICSS_IEP_RXIPG1	Status for the RX port which is attached to PRU1	4802 E0BCh
C0h	PRU_ICSS_IEP_COMPARE08	COMPARE8 low	4802 E0C0h
C4h	PRU_ICSS_IEP_COMPARE18	COMPARE8 high	4802 E0C4h
C8h	PRU_ICSS_IEP_COMPARE09	COMPARE9 low	4802 E0C8h
CCh	PRU_ICSS_IEP_COMPARE19	COMPARE9 high	4802 E0CCh
D0h	PRU_ICSS_IEP_COMPARE010	COMPARE10 low	4802 E0D0h
D4h	PRU_ICSS_IEP_COMPARE110	COMPARE10 high	4802 E0D4h
D8h	PRU_ICSS_IEP_COMPARE011	COMPARE11 low	4802 E0D8h
DCh	PRU_ICSS_IEP_COMPARE111	COMPARE11 high	4802 E0DCh
E0h	PRU_ICSS_IEP_COMPARE012	COMPARE12 low	4802 E0E0h
E4h	PRU_ICSS_IEP_COMPARE112	COMPARE12 high	4802 E0E4h
E8h	PRU_ICSS_IEP_COMPARE013	COMPARE13 low	4802 E0E8h
ECh	PRU_ICSS_IEP_COMPARE113	COMPARE13 high	4802 E0ECh
F0h	PRU_ICSS_IEP_COMPARE014	COMPARE14 low	4802 E0F0h
F4h	PRU_ICSS_IEP_COMPARE114	COMPARE14 high	4802 E0F4h
F8h	PRU_ICSS_IEP_COMPARE015	COMPARE15 low	4802 E0F8h
FCh	PRU_ICSS_IEP_COMPARE115	COMPARE15 high	4802 E0FCh
100h	PRU_ICSS_IEP_LOW_COUNTER_RESET_VALUE	Reset value of the Master Counter (lower 32-bits)	4802 E100h
104h	PRU_ICSS_IEP_HIGH_COUNTER_RESET_VALUE	Reset value of the Master Counter (upper 32-bits)	4802 E104h
108h	PRU_ICSS_IEP_PWM	PWM Sync Out	4802 E108h
180h	PRU_ICSS_IEP_SYNC_CTRL	SYNC GENERATION CONTROL	4802 E180h
184h	PRU_ICSS_IEP_SYNC_FIRST_STAT	SYNC GENERATION FIRST EVENT STATUS	4802 E184h
188h	PRU_ICSS_IEP_SYNC0_STAT	SYNC0 STATUS	4802 E188h
18Ch	PRU_ICSS_IEP_SYNC1_STAT	SYNC1 STATUS	4802 E18Ch
190h	PRU_ICSS_IEP_SYNC_PWIDTH	SYNC PULSE WIDTH CONFIGURE	4802 E190h
194h	PRU_ICSS_IEP_SYNC0_PERIOD	SYNC0 PERIOD CONFIGURE	4802 E194h
198h	PRU_ICSS_IEP_SYNC1_DELAY	SYNC1 DELAY	4802 E198h
19Ch	PRU_ICSS_IEP_SYNC_START	SYNC START CONFIGURE	4802 E19Ch
200h	PRU_ICSS_IEP_WD_PREDIV	WATCHDOG PRE-DIVIDER	4802 E200h
204h	PRU_ICSS_IEP_PDI_WD_TIM	PDI WATCHDOG TIMER CONFIGURE	4802 E204h
208h	PRU_ICSS_IEP_PD_WD_TIM	PD WATCHDOG TIMER CONFIGURE	4802 E208h
20Ch	PRU_ICSS_IEP_WD_STATUS	WATCHDOG STATUS	4802 E20Ch
210h	PRU_ICSS_IEP_WD_EXP_CNT	WATCHDOG TIMER EXPIRATION COUNTER	4802 E210h

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Table 4-480. PRU_ICSS_IEP Registers (continued)

Offset	Acronym	Register Name	PRU_ICSS_IEP Physical Address
214h	PRU_ICSS_IEP_IEP_WD_CTRL	WATCHDOG CONTROL	4802 E214h
300h	PRU_ICSS_IEP_DIGIO_CTRL	DIGIO Control	4802 E300h
304h	PRU_ICSS_IEP_DIGIO_STATUS	DIGIO Status	4802 E304h
308h	PRU_ICSS_IEP_DIGIO_DATA_IN	DIGIO Data Input	4802 E308h
30Ch	PRU_ICSS_IEP_DIGIO_DATA_IN_RAW	DIGIO Data Input. Direct Sample.	4802 E30Ch
310h	PRU_ICSS_IEP_DIGIO_DATA_OUT	DIGIO Data Output	4802 E310h
314h	PRU_ICSS_IEP_DIGIO_DATA_OUT_EN	DIGIO Data Input which controls tri-state of pr<k>_edio_data_out_en[3:0]	4802 E314h
318h	PRU_ICSS_IEP_DIGIO_EXP	DIGIO, Defines which RX_EOF is used	4802 E318h

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4.5.10.1 PRU_ICSS_IEP_GLOBAL_CFG Register (Offset = 0h) [reset = 550h]

PRU_ICSS_IEP_GLOBAL_CFG is shown in Figure 4-219 and described in Table 4-482.

GLOBAL CFG

Table 4-481. PRU_ICSS_IEP_GLOBAL_CFG Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E000h

Figure 4-219. PRU_ICSS_IEP_GLOBAL_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				CMP_INC			
R-0h				R/W-5h			
15	14	13	12	11	10	9	8
CMP_INC							
R/W-5h							
7	6	5	4	3	2	1	0
DEFAULT_INC				RESERVED			CNT_ENABLE
R/W-5h				R-0h			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-482. PRU_ICSS_IEP_GLOBAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-8	CMP_INC	R/W	5h	Defines the increment value when compensation is active
7-4	DEFAULT_INC	R/W	5h	Defines the default increment value
3-1	RESERVED	R	0h	Reserved
0	CNT_ENABLE	R/W	0h	Counter enable. 0h: Disables the counter. The counter maintains the current count. 1h: Enables the counter.

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4.5.10.2 PRU_ICSS_IEP_STATUS Register (Offset = 4h) [reset = 0h]

PRU_ICSS_IEP_STATUS is shown in Figure 4-220 and described in Table 4-484.

STATUS

Table 4-483. PRU_ICSS_IEP_STATUS Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E004h

Figure 4-220. PRU_ICSS_IEP_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CNT_OVF
R-0h							RWr1Clr-0h

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-484. PRU_ICSS_IEP_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CNT_OVF	RWr1Clr	0h	Counter overflow status. 0h: No overflow 1h: Overflow occurred

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4.5.10.3 PRU_ICSS_IEP_COMPENSATION Register (Offset = 8h) [reset = 0h]

PRU_ICSS_IEP_COMPENSATION is shown in Figure 4-221 and described in Table 4-486.

COMPENSATION

Table 4-485. PRU_ICSS_IEP_COMPENSATION Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E008h

Figure 4-221. PRU_ICSS_IEP_COMPENSATION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COMPEN_CNT																							
R-0h								R/W-0h																							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-486. PRU_ICSS_IEP_COMPENSATION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-0	COMPEN_CNT	R/W	0h	Compensation counter. Read returns the current COMPEN_CNT value. 0h: Compensation is disabled and counter will increment by DEFAULT_INC. Nh: Compensation is enabled until COMPEN_CNT decrements to 0. The COMPEN_CNT value decrements on every IEP_CLK cycle. When COMPEN_CNT is greater than 0, then count value increments by CMP_INC. **Note** NOTE: SLOW_COMPEN_CNT MUST be set to zero IF COMPEN_CNT is not zero.

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4.5.10.4 PRU_ICSS_IEP_SLOW_COMPENSATION Register (Offset = Ch) [reset = 0h]

PRU_ICSS_IEP_SLOW_COMPENSATION is shown in Figure 4-222 and described in Table 4-488.

SLOW COMPENSATION

Table 4-487. PRU_ICSS_IEP_SLOW_COMPENSATION Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E00Ch

Figure 4-222. PRU_ICSS_IEP_SLOW_COMPENSATION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOW_COMPEN_CNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-488. PRU_ICSS_IEP_SLOW_COMPENSATION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SLOW_COMPEN_CNT	R/W	0h	Slow compensation counter. Write 0h: Slow compensation is disabled and counter will increment by DEFAULT_INC. Write Nh: Compensation is enabled for 1 count for every SLOW_COMPEN_CNT cycle, this is free running and continuous until software clears the MMR. For example, SLOW_COMPEN_CNT = 16, every 16 clock cycles the compensation value is used for 1 count. Note: COMPEN_CNT MUST be set to zero IF SLOW_COMPEN_CNT is not zero. Software can read the number of cycles left until the compensation event. For example, software writes SLOW_COMPEN_CNT = 100h and reads SLOW_COMPEN_CNT = 7h. This means in 6 more IEP_CLK cycles before the counter reaches 1h for the compensation event. If software writes SLOW_COMPEN_CNT = 8000h before compensation event, then the counter will reset to 8000h.

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4.5.10.5 PRU_ICSS_IEP_LOW_COUNTER Register (Offset = 10h) [reset = 0h]

PRU_ICSS_IEP_LOW_COUNTER is shown in Figure 4-223 and described in Table 4-490.

64 bit count value low

Table 4-489. PRU_ICSS_IEP_LOW_COUNTER Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E010h

Figure 4-223. PRU_ICSS_IEP_LOW_COUNTER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-490. PRU_ICSS_IEP_LOW_COUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	64 bit count value (lower 32-bits). Increments by (DEFAULT_INC or CMP_INC) on every positive edge of ICSS_IEP_CLK (200MHz) or ICSS_VCLK_CLK.

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4.5.10.6 PRU_ICSS_IEP_HIGH_COUNTER Register (Offset = 14h) [reset = 0h]

PRU_ICSS_HIGH_COUNTER is shown in Figure 4-224 and described in Table 4-492.

64 bit count value high

Table 4-491. PRU_ICSS_IEP_HIGH_COUNTER Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E014h

Figure 4-224. PRU_ICSS_IEP_HIGH_COUNTER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-492. PRU_ICSS_IEP_HIGH_COUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	64 bit count value (upper 32-bits). Increments by (DEFAULT_INC or CMP_INC) on every positive edge of ICSS_IEP_CLK (200MHz) or ICSS_VCLK_CLK.

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4.5.10.7 PRU_ICSS_IEP_CAPTURE_CFG Register (Offset = 18h) [reset = 0001FC00h]

PRU_ICSS_IEP_CAPTURE_CFG is shown in Figure 4-225 and described in Table 4-494.

CAPTURE CFG

Table 4-493. PRU_ICSS_IEP_CAPTURE_CFG Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E018h

Figure 4-225. PRU_ICSS_IEP_CAPTURE_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						CAP_ASYNC_EN	
R-0h						R/W-7Fh	
15	14	13	12	11	10	9	8
CAP_ASYNC_EN						CAP7F_1ST_EVENT_EN	CAP7R_1ST_EVENT_EN
R/W-7Fh						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
CAP6F_1ST_EVENT_EN	CAP6R_1ST_EVENT_EN	CAP_1ST_EVENT_EN					
R/W-0h	R/W-0h	R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-494. PRU_ICSS_IEP_CAPTURE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17-10	CAP_ASYNC_EN	R/W	7Fh	Synchronization of the capture inputs to the ICSS_IEP_CLK/ ICSS_VCLK_CLK enable. Note if input capture signal is asynchronous to ICSS_IEP_CLK, enabling synchronization will cause the capture contents to be invalid. CAP_ASYNC_EN[n] maps to CAPR[n]. 0h: Disable synchronization 1h: Enable synchronization
9	CAP7F_1ST_EVENT_EN	R/W	0h	Capture 1st Event Enable for CAP7F. 0h: Continues mode. The capture status is not set when events occur. 1h: First Event mode. The capture status is set when the first event occurs and must be cleared before new data will fill buffer. Time value is captured when first event occurs and held until time is read.
8	CAP7R_1ST_EVENT_EN	R/W	0h	Capture 1st Event Enable for CAP7R. 0h: Continues mode. The capture status is not set when events occur. 1h: First Event mode. The capture status is set when the first event occurs and must be cleared before new data will fill buffer. Time value is captured when first event occurs and held until time is read.

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Table 4-494. PRU_ICSS_IEP_CAPTURE_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CAP6F_1ST_EVENT_EN	R/W	0h	Capture 1st Event Enable for CAP6F. 0h: Continues mode. The capture status is not set when events occur. 1h: First Event mode. The capture status is set when the first event occurs and must be cleared before new data will fill buffer. Time value is captured when first event occurs and held until time is read.
6	CAP6R_1ST_EVENT_EN	R/W	0h	Capture 1st Event Enable for CAP6R. 0h: Continues mode. The capture status is not set when events occur. 1h: First Event mode. The capture status is set when the first event occurs and must be cleared before new data will fill buffer. Time value is captured when first event occurs and held until time is read.
5-0	CAP_1ST_EVENT_EN	R/W	0h	Capture 1st Event Enable for registers. CAP_1ST_EVENT_EN[n] maps to CAPR[n]. 0h: Continues mode. The capture status is not set when events occur. 1h: First Event mode. The capture status is set when the first event occurs and must be cleared before new data will fill buffer. Time value is captured when first event occurs and held until time is read.

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4.5.10.8 PRU_ICSS_IEP_CAPTURE_STATUS Register (Offset = 1Ch) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_STATUS is shown in Figure 4-226 and described in Table 4-496.

CAPTURE STATUS

Table 4-495. PRU_ICSS_IEP_CAPTURE_STATUS Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E01Ch

Figure 4-226. PRU_ICSS_IEP_CAPTURE_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
CAP_RAW							
R-0h							
15	14	13	12	11	10	9	8
RESERVED					CAP_VALID	CAPF7_VALID	CAPR7_VALID
R-0h					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
CAPF6_VALID	CAPR6_VALID	CAPR_VALID					
R-0h	R-0h	R-0h					

LEGEND: R = Read Only; *-n* = value after reset

Table 4-496. PRU_ICSS_IEP_CAPTURE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	CAP_RAW	R	0h	Raw/Current status bit for each of the capture registers, where CAP_RAW[n] maps to CAPR[n]. 0h: Current state is low. 1h: Current state is high.
15-11	RESERVED	R	0h	Reserved
10	CAP_VALID	R	0h	Valid status for capture function. Reflects the ORed result from CAP_STATUS[9:0]. 0h: No Hit for any capture event, i.e., there are all 0 in CAP_STATUS[9:0]. 1h: Hit for 1 or more captures events is pending, i.e., there has at least one value equal to 1 in CAP_STATUS[9:0].
9	CAPF7_VALID	R	0h	Valid status for CAPF7 (fall). 0h: No Hit, no capture event occurred 1h: Hit, capture event occurred
8	CAPR7_VALID	R	0h	Valid status for CAPR7 (rise). 0h: No Hit, no capture event occurred 1h: Hit, capture event occurred
7	CAPF6_VALID	R	0h	Valid status for CAPF6 (fall). 0h: No Hit, no capture event occurred 1h: Hit, capture event occurred
6	CAPR6_VALID	R	0h	Valid status for CAPR6 (rise). 0h: No Hit, no capture event occurred 1h: Hit, capture event occurred

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Table 4-496. PRU_ICSS_IEP_CAPTURE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	CAPR_VALID	R	0h	Valid status bit for each compare register, where CAPR_VALID[n] maps to CAPR[n] (rise). 0h: No Hit, no capture event occurred 1h: Hit, capture event occurred

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4.5.10.9 PRU_ICSS_IEP_CAPTURE_RISE00 Register (Offset = 20h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE00 is shown in Figure 4-227 and described in Table 4-498.

CAPTURE RISE0 low

Table 4-497. PRU_ICSS_IEP_CAPTURE_RISE00 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E020h

Figure 4-227. PRU_ICSS_IEP_CAPTURE_RISE00 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-498. PRU_ICSS_IEP_CAPTURE_RISE00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

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4.5.10.10 PRU_ICSS_IEP_CAPTURE_RISE10 Register (Offset = 24h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE10 is shown in Figure 4-228 and described in Table 4-500.

CAPTURE RISE0 high

Table 4-499. PRU_ICSS_IEP_CAPTURE_RISE10 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E024h

Figure 4-228. PRU_ICSS_IEP_CAPTURE_RISE10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-500. PRU_ICSS_IEP_CAPTURE_RISE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

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4.5.10.11 PRU_ICSS_IEP_CAPTURE_RISE01 Register (Offset = 28h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE01 is shown in Figure 4-229 and described in Table 4-502.

CAPTURE RISE1 low

Table 4-501. PRU_ICSS_IEP_CAPTURE_RISE01 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E028h

Figure 4-229. PRU_ICSS_IEP_CAPTURE_RISE01 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-502. PRU_ICSS_IEP_CAPTURE_RISE01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

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4.5.10.12 PRU_ICSS_IEP_CAPTURE_RISE11 Register (Offset = 2Ch) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE11 is shown in Figure 4-230 and described in Table 4-504.

CAPTURE RISE1 high

Table 4-503. PRU_ICSS_IEP_CAPTURE_RISE11 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E02Ch

Figure 4-230. PRU_ICSS_IEP_CAPTURE_RISE11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-504. PRU_ICSS_IEP_CAPTURE_RISE11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

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4.5.10.13 PRU_ICSS_IEP_CAPTURE_RISE02 Register (Offset = 30h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE02 is shown in Figure 4-231 and described in Table 4-506.

CAPTURE RISE2 low

Table 4-505. PRU_ICSS_IEP_CAPTURE_RISE02 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E030h

Figure 4-231. PRU_ICSS_IEP_CAPTURE_RISE02 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-506. PRU_ICSS_IEP_CAPTURE_RISE02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

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4.5.10.14 PRU_ICSS_IEP_CAPTURE_RISE12 Register (Offset = 34h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE12 is shown in Figure 4-232 and described in Table 4-508.

CAPTURE RISE2 high

Table 4-507. PRU_ICSS_IEP_CAPTURE_RISE12 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E034h

Figure 4-232. PRU_ICSS_IEP_CAPTURE_RISE12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-508. PRU_ICSS_IEP_CAPTURE_RISE12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

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4.5.10.15 PRU_ICSS_IEP_CAPTURE_RISE03 Register (Offset = 38h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE03 is shown in Figure 4-233 and described in Table 4-510.

CAPTURE RISE3 low

Table 4-509. PRU_ICSS_IEP_CAPTURE_RISE03 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E038h

Figure 4-233. PRU_ICSS_IEP_CAPTURE_RISE03 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-510. PRU_ICSS_IEP_CAPTURE_RISE03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

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4.5.10.16 PRU_ICSS_IEP_CAPTURE_RISE13 Register (Offset = 3Ch) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE13 is shown in Figure 4-234 and described in Table 4-512.

CAPTURE RISE3 high

Table 4-511. PRU_ICSS_IEP_CAPTURE_RISE13 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E03Ch

Figure 4-234. PRU_ICSS_IEP_CAPTURE_RISE13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-512. PRU_ICSS_IEP_CAPTURE_RISE13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

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4.5.10.17 PRU_ICSS_IEP_CAPTURE_RISE04 Register (Offset = 40h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE04 is shown in Figure 4-235 and described in Table 4-514.

CAPTURE RISE4 low

Table 4-513. PRU_ICSS_IEP_CAPTURE_RISE04 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E040h

Figure 4-235. PRU_ICSS_IEP_CAPTURE_RISE04 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-514. PRU_ICSS_IEP_CAPTURE_RISE04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

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4.5.10.18 PRU_ICSS_IEP_CAPTURE_RISE14 Register (Offset = 44h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE14 is shown in Figure 4-236 and described in Table 4-516.

CAPTURE RISE4 high

Table 4-515. PRU_ICSS_IEP_CAPTURE_RISE14 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E044h

Figure 4-236. PRU_ICSS_IEP_CAPTURE_RISE14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-516. PRU_ICSS_IEP_CAPTURE_RISE14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

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4.5.10.19 PRU_ICSS_IEP_CAPTURE_RISE05 Register (Offset = 48h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE05 is shown in Figure 4-237 and described in Table 4-518.

CAPTURE RISE5 low

Table 4-517. PRU_ICSS_IEP_CAPTURE_RISE05 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E048h

Figure 4-237. PRU_ICSS_IEP_CAPTURE_RISE05 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-518. PRU_ICSS_IEP_CAPTURE_RISE05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (fall) event, where i = 0 to 5. Lower 32-bits.

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4.5.10.20 PRU_ICSS_IEP_CAPTURE_RISE15 Register (Offset = 4Ch) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE15 is shown in Figure 4-238 and described in Table 4-520.

CAPTURE RISE5 high

Table 4-519. PRU_ICSS_IEP_CAPTURE_RISE15 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E04Ch

Figure 4-238. PRU_ICSS_IEP_CAPTURE_RISE15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-520. PRU_ICSS_IEP_CAPTURE_RISE15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR<i> (rise) event, where i = 0 to 5. Upper 32-bits.

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4.5.10.21 PRU_ICSS_IEP_CAPTURE_RISE06 Register (Offset = 50h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE06 is shown in Figure 4-239 and described in Table 4-522.

CAPTURE RISE6 low

Table 4-521. PRU_ICSS_IEP_CAPTURE_RISE06 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E050h

Figure 4-239. PRU_ICSS_IEP_CAPTURE_RISE06 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-522. PRU_ICSS_IEP_CAPTURE_RISE06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR6 event. Lower 32-bits.

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4.5.10.22 PRU_ICSS_IEP_CAPTURE_RISE16 Register (Offset = 54h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_RISE16 is shown in and described in .

CAPTURE RISE6 high

Table 4-523. PRU_ICSS_IEP_CAPTURE_RISE16 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E054h

Figure 4-240. PRU_ICSS_IEP_CAPTURE_RISE16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-524. PRU_ICSS_IEP_CAPTURE_RISE16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR6 event. Upper 32-bits.

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4.5.10.23 PRU_ICSS_IEP_CAPTURE_FALL06 Register (Offset = 58h) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_FALL06 is shown in Figure 4-241 and described in Table 4-526.

CAPTURE FALL6 low

Table 4-525. PRU_ICSS_IEP_CAPTURE_FALL06 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E058h

Figure 4-241. PRU_ICSS_IEP_CAPTURE_FALL06 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-526. PRU_ICSS_IEP_CAPTURE_FALL06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF	R	0h	Value captured for CAPF6 (fall) event. Lower 32-bits.

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4.5.10.24 PRU_ICSS_IEP_CAPTURE_FALL16 Register (Offset = 5Ch) [reset = 0h]

PRU_ICSS_IEP_CAPTURE_FALL16 is shown in Figure 4-242 and described in Table 4-528.

CAPTURE FALL6 high

Table 4-527. PRU_ICSS_IEP_CAPTURE_FALL16 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E05Ch

Figure 4-242. PRU_ICSS_IEP_CAPTURE_FALL16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-528. PRU_ICSS_IEP_CAPTURE_FALL16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF	R	0h	Value captured for CAPF6 (fall) event. Lower 32-bits.

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4.5.10.25 PRU_ICSS_IEP_CAPTURE_RISE07 Register (Offset = 60h) [reset = 0h]

PRU_ICSS_IEP_COMPARE_RISE07 is shown in Figure 4-243 and described in Table 4-530.

CAPTURE RISE7 low

Table 4-529. PRU_ICSS_IEP_CAPTURE_RISE07 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E060h

Figure 4-243. PRU_ICSS_IEP_CAPTURE_RISE07 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-530. PRU_ICSS_IEP_CAPTURE_RISE07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR7 (rise) event. Lower 32-bits.

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4.5.10.26 PRU_ICSS_IEP_CAPTURE_RISE17 Register (Offset = 64h) [reset = 0h]

PRU_ICSS_IEP_COMPARE_RISE17 is shown in Figure 4-244 and described in Table 4-532.

CAPTURE RISE7 high

Table 4-531. PRU_ICSS_IEP_CAPTURE_RISE17 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E064h

Figure 4-244. PRU_ICSS_IEP_CAPTURE_RISE17 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPR																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-532. PRU_ICSS_IEP_CAPTURE_RISE17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPR	R	0h	Value captured for CAPR7 (rise) event. Upper 32-bits.

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4.5.10.27 PRU_ICSS_IEP_CAPTURE_FALL07 Register (Offset = 68h) [reset = 0h]

PRU_ICSS_IEP_COMPARE_FALL07 is shown in Figure 4-245 and described in Table 4-534.

CAPTURE FALL7 low

Table 4-533. PRU_ICSS_IEP_CAPTURE_FALL07 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E068h

Figure 4-245. PRU_ICSS_IEP_CAPTURE_FALL07 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-534. PRU_ICSS_IEP_CAPTURE_FALL07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF	R	0h	Value captured for CAPF7 (fall) event. Lower 32-bits.

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4.5.10.28 PRU_ICSS_IEP_CAPTURE_FALL17 Register (Offset = 6Ch) [reset = 0h]

PRU_ICSS_IEP_COMPARE_FALL17 is shown in Figure 4-246 and described in Table 4-536.

CAPTURE FALL7 high

Table 4-535. PRU_ICSS_IEP_CAPTURE_FALL17 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E06Ch

Figure 4-246. PRU_ICSS_IEP_CAPTURE_FALL17 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPF																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-536. PRU_ICSS_IEP_CAPTURE_FALL17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CAPF	R	0h	Value captured for CAPF7 (fall) event. Upper 32-bits.

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4.5.10.29 PRU_ICSS_IEP_COMPARE_CFG Register (Offset = 70h) [reset = 0h]

PRU_ICSS_IEP_COMPARE_CFG is shown in Figure 4-247 and described in Table 4-538.

COMPARE CFG

Table 4-537. PRU_ICSS_IEP_COMPARE_CFG Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E070h

Figure 4-247. PRU_ICSS_IEP_COMPARE_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							CMP_EN
R-0h							R/W-0h
15	14	13	12	11	10	9	8
CMP_EN							
R/W-0h							
7	6	5	4	3	2	1	0
CMP_EN							CMP0_RST_CNT_EN
R/W-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-538. PRU_ICSS_IEP_COMPARE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16-1	CMP_EN	R/W	0h	Enable bits for each of the compare registers CMP_EN =0 : Disables CMPj/k Event CMP_EN=1: Enables CMPj/k Event CMP_EN[0] (bit 1 of register) maps to CMP0 event
0	CMP0_RST_CNT_EN	R/W	0h	Enable the reset of the counter 0h: Disable 1h: Enable the reset of the counter if a CMP0 event occurs

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4.5.10.30 PRU_ICSS_IEP_COMPARE_STATUS Register (Offset = 74h) [reset = 0h]

PRU_ICSS_IEP_COMPARE_STATUS is shown in Figure 4-248 and described in Table 4-540.

COMPARE STATUS

Table 4-539. PRU_ICSS_IEP_COMPARE_STATUS Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E074h

Figure 4-248. PRU_ICSS_IEP_COMPARE_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CMP_HIT															
R-0h																RWr1Clr-0h															

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-540. PRU_ICSS_IEP_COMPARE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	CMP_HIT	RWr1Clr	0h	Status bit for each of the compare registers. "Match" indicates the current counter is greater than or equal to the compare value. Note it is the firmware's responsibility to handle the IEP overflow. CMP_HITj/k = 0: No match has occured CMP_HITj/k = 1: A match occured. The associated hardware event signal will assert and remain high until the status is cleared.

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4.5.10.31 PRU_ICSS_IEP_COMPARE00 Register (Offset = 78h) [reset = 0h]

PRU_ICSS_IEP_COMPARE00 is shown in Figure 4-249 and described in Table 4-542.

COMPARE0 low

Table 4-541. PRU_ICSS_IEP_COMPARE00 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E078h

Figure 4-249. PRU_ICSS_IEP_COMPARE00 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-542. PRU_ICSS_IEP_COMPARE00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 0 low value

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4.5.10.32 PRU_ICSS_IEP_COMPARE10 Register (Offset = 7Ch) [reset = 0h]

PRU_ICSS_IEP_COMPARE10 is shown in Figure 4-250 and described in Table 4-544.

COMPARE0 high

Table 4-543. PRU_ICSS_IEP_COMPARE10 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E07Ch

Figure 4-250. PRU_ICSS_IEP_COMPARE10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-544. PRU_ICSS_IEP_COMPARE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 0 high value

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4.5.10.33 PRU_ICSS_IEP_COMPARE01 Register (Offset = 80h) [reset = 0h]

PRU_ICSS_IEP_COMPARE01 is shown in Figure 4-251 and described in Table 4-546.

COMPARE1 low

Table 4-545. PRU_ICSS_IEP_COMPARE01 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E080h

Figure 4-251. PRU_ICSS_IEP_COMPARE01 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-546. PRU_ICSS_IEP_COMPARE01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 1 low value

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4.5.10.34 PRU_ICSS_IEP_COMPARE11 Register (Offset = 84h) [reset = 0h]

PRU_ICSS_IEP_COMPARE11 is shown in Figure 4-252 and described in Table 4-548.

COMPARE1 high

Table 4-547. PRU_ICSS_IEP_COMPARE11 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E084h

Figure 4-252. PRU_ICSS_IEP_COMPARE11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-548. PRU_ICSS_IEP_COMPARE11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 1 high value

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4.5.10.35 PRU_ICSS_IEP_COMPARE02 Register (Offset = 88h) [reset = 0h]

PRU_ICSS_IEP_COMPARE02 is shown in Figure 4-253 and described in Table 4-550.

COMPARE2 low

Table 4-549. PRU_ICSS_IEP_COMPARE02 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E088h

Figure 4-253. PRU_ICSS_IEP_COMPARE02 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-550. PRU_ICSS_IEP_COMPARE02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 2 low value

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4.5.10.36 PRU_ICSS_IEP_COMPARE12 Register (Offset = 8Ch) [reset = 0h]

PRU_ICSS_IEP_COMPARE12 is shown in Figure 4-254 and described in Table 4-552.

COMPARE2 high

Table 4-551. PRU_ICSS_IEP_COMPARE12 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E08Ch

Figure 4-254. PRU_ICSS_IEP_COMPARE12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-552. PRU_ICSS_IEP_COMPARE12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 2 high value

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4.5.10.37 PRU_ICSS_IEP_COMPARE03 Register (Offset = 90h) [reset = 0h]

PRU_ICSS_IEP_COMPARE03 is shown in Figure 4-255 and described in Table 4-554.

COMPARE3 low

Table 4-553. PRU_ICSS_IEP_COMPARE03 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E090h

Figure 4-255. PRU_ICSS_IEP_COMPARE03 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-554. PRU_ICSS_IEP_COMPARE03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 3 low value

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4.5.10.38 PRU_ICSS_IEP_COMPARE13 Register (Offset = 94h) [reset = 0h]

PRU_ICSS_IEP_COMPARE13 is shown in Figure 4-256 and described in Table 4-556.

COMPARE3 high

Table 4-555. PRU_ICSS_IEP_COMPARE13 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E094h

Figure 4-256. PRU_ICSS_IEP_COMPARE13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-556. PRU_ICSS_IEP_COMPARE13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 3 high value

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4.5.10.39 PRU_ICSS_IEP_COMPARE04 Register (Offset = 98h) [reset = 0h]

PRU_ICSS_IEP_COMPARE04 is shown in Figure 4-257 and described in Table 4-558.

COMPARE4 low

Table 4-557. PRU_ICSS_IEP_COMPARE04 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E098h

Figure 4-257. PRU_ICSS_IEP_COMPARE04 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-558. PRU_ICSS_IEP_COMPARE04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 4 low value

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4.5.10.40 PRU_ICSS_IEP_COMPARE14 Register (Offset = 9Ch) [reset = 0h]

PRU_ICSS_IEP_COMPARE14 is shown in Figure 4-258 and described in Table 4-560.

COMPARE4 high

Table 4-559. PRU_ICSS_IEP_COMPARE14 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E09Ch

Figure 4-258. PRU_ICSS_IEP_COMPARE14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-560. PRU_ICSS_IEP_COMPARE14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 4 high value

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4.5.10.41 PRU_ICSS_IEP_COMPARE05 Register (Offset = A0h) [reset = 0h]

PRU_ICSS_IEP_COMPARE05 is shown in Figure 4-259 and described in Table 4-562.

COMPARE5 low

Table 4-561. PRU_ICSS_IEP_COMPARE05 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0A0h

Figure 4-259. PRU_ICSS_IEP_COMPARE05 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-562. PRU_ICSS_IEP_COMPARE05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 5 low value

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4.5.10.42 PRU_ICSS_IEP_COMPARE15 Register (Offset = A4h) [reset = 0h]

PRU_ICSS_IEP_COMPARE15 is shown in Figure 4-260 and described in Table 4-564.

COMPARE5 high

Table 4-563. PRU_ICSS_IEP_COMPARE15 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0A4h

Figure 4-260. PRU_ICSS_IEP_COMPARE15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-564. PRU_ICSS_IEP_COMPARE15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 5 high value

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4.5.10.43 PRU_ICSS_IEP_COMPARE06 Register (Offset = A8h) [reset = 0h]

PRU_ICSS_IEP_COMPARE06 is shown in Figure 4-261 and described in Table 4-566.

COMPARE6 low

Table 4-565. PRU_ICSS_IEP_COMPARE06 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0A8h

Figure 4-261. PRU_ICSS_IEP_COMPARE06 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-566. PRU_ICSS_IEP_COMPARE06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 6 low value

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4.5.10.44 PRU_ICSS_IEP_COMPARE16 Register (Offset = ACh) [reset = 0h]

PRU_ICSS_IEP_COMPARE16 is shown in Figure 4-262 and described in Table 4-568.

COMPARE6 high

Table 4-567. PRU_ICSS_IEP_COMPARE16 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0ACh

Figure 4-262. PRU_ICSS_IEP_COMPARE16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-568. PRU_ICSS_IEP_COMPARE16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 6 high value

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4.5.10.45 PRU_ICSS_IEP_COMPARE07 Register (Offset = B0h) [reset = 0h]

PRU_ICSS_IEP_COMPARE07 is shown in Figure 4-263 and described in Table 4-570.

COMPARE7 low

Table 4-569. PRU_ICSS_IEP_COMPARE07 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0B0h

Figure 4-263. PRU_ICSS_IEP_COMPARE07 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-570. PRU_ICSS_IEP_COMPARE07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 7 low value

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4.5.10.46 PRU_ICSS_IEP_COMPARE17 Register (Offset = B4h) [reset = 0h]

PRU_ICSS_IEP_COMPARE17 is shown in Figure 4-264 and described in Table 4-572.

COMPARE7 high

Table 4-571. PRU_ICSS_IEP_COMPARE17 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0B4h

Figure 4-264. PRU_ICSS_IEP_COMPARE17 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-572. PRU_ICSS_IEP_COMPARE17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 7 high value

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4.5.10.47 PRU_ICSS_IEP_RXIPG0 Register (Offset = B8h) [reset = FFFF0000h]

PRU_ICSS_IEP_RXIPG0 is shown in Figure 4-265 and described in Table 4-574.

This register can be used to determine the last RX IPG and the smallest RX IPG. RXIPG0 is the status for the RX port which is attached to PRU0.

Table 4-573. PRU_ICSS_IEP_RXIPG0 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0B8h

Figure 4-265. PRU_ICSS_IEP_RXIPG0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MIN_IPG																RX_IPG															
R/W-FFFFh																R-0h															

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-574. PRU_ICSS_IEP_RXIPG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_MIN_IPG	R/W	FFFFh	Defines the minimum number of ICSS_IEP_CLK/ICCS_VCLK_CLK cycles that is RX_DV is sampled low. It stores the smallest RX_IPG duration. It can be read at any time and gets updated after RX_IPG is updated, if RX_MIN_IPG is greater than RX_IPG.
15-0	RX_IPG	R	0h	Records the current number of ICSS_IEP_CLK/ICSS_VCLK_CLK cycles RX_DV is sampled low. Value is updated after RX_DV transitions from low to high. It will saturate at FFFFh.

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4.5.10.48 PRU_ICSS_IEP_RXIPG1 Register (Offset = BCh) [reset = FFFF0000h]

PRU_ICSS_IEP_RXIPG1 is shown in Figure 4-266 and described in Table 4-576.

This register can be used to determine the last RX IPG and the smallest RX IPG. RXIPG1 is the status for the RX port which is attached to PRU1

Table 4-575. PRU_ICSS_IEP_RXIPG1 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0BCh

Figure 4-266. PRU_ICSS_IEP_RXIPG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_MIN_IPG																RX_IPG															
R/W-FFFFh																R-0h															

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-576. PRU_ICSS_IEP_RXIPG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RX_MIN_IPG	R/W	FFFFh	Defines the minimum number of ICSS_IEP_CLK/ICSS_VCLK_CLK cycles that is RX_DV is sampled low. It stores the smallest RX_IPG duration. It can be read at any time and gets updated after RX_IPG is updated, if RX_MIN_IPG is greater than RX_IPG.
15-0	RX_IPG	R	0h	Records the current number of ICSS_IEP_CLK/ICSS_VCLK_CLK cycles RX_DV is sampled low. Value is updated after RX_DV transitions from low to high. It will saturate at FFFFh.

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4.5.10.49 PRU_ICSS_IEP_COMPARE08 Register (Offset = C0h) [reset = 0h]

PRU_ICSS_IEP_COMPARE08 is shown in Figure 4-267 and described in Table 4-578.

COMPARE8 low

Table 4-577. PRU_ICSS_IEP_COMPARE08 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0C0h

Figure 4-267. PRU_ICSS_IEP_COMPARE08 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-578. PRU_ICSS_IEP_COMPARE08 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 8 low value

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4.5.10.50 PRU_ICSS_IEP_COMPARE18 Register (Offset = C4h) [reset = 0h]

PRU_ICSS_IEP_COMPARE18 is shown in Figure 4-268 and described in Table 4-580.

COMPARE8 high

Table 4-579. PRU_ICSS_IEP_COMPARE18 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0C4h

Figure 4-268. PRU_ICSS_IEP_COMPARE18 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-580. PRU_ICSS_IEP_COMPARE18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Reset value (upper 32-bits). This register enables SW to define the reset state of the Master Counter, which can be reset by the following events (if enabled): CMP0 event; eHRPWM0_SYNCO event; eHRPWM3_SYNCO event. The RESET_VAL should be in increments of the DEFAULT_INC (default state is 5). For example, 0000_000Ah.

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4.5.10.51 PRU_ICSS_IEP_COMPARE09 Register (Offset = C8h) [reset = 0h]

PRU_ICSS_IEP_COMPARE09 is shown in Figure 4-269 and described in Table 4-582.

COMPARE9 low

Table 4-581. PRU_ICSS_IEP_COMPARE09 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0C8h

Figure 4-269. PRU_ICSS_IEP_COMPARE09 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-582. PRU_ICSS_IEP_COMPARE09 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 9 low value

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4.5.10.52 PRU_ICSS_IEP_COMPARE19 Register (Offset = CCh) [reset = 0h]

PRU_ICSS_IEP_COMPARE19 is shown in Figure 4-270 and described in Table 4-584.

COMPARE9 high

Table 4-583. PRU_ICSS_IEP_COMPARE19 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0CCh

Figure 4-270. PRU_ICSS_IEP_COMPARE19 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-584. PRU_ICSS_IEP_COMPARE19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 9 high value

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4.5.10.53 PRU_ICSS_IEP_COMPARE010 Register (Offset = D0h) [reset = 0h]

PRU_ICSS_IEP_COMPARE010 is shown in Figure 4-271 and described in Table 4-586.

COMPARE10 low

Table 4-585. PRU_ICSS_IEP_COMPARE010 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0D0h

Figure 4-271. PRU_ICSS_IEP_COMPARE010 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-586. PRU_ICSS_IEP_COMPARE010 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 10 low value

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4.5.10.54 PRU_ICSS_IEP_COMPARE110 Register (Offset = D4h) [reset = 0h]

PRU_ICSS_IEP_COMPARE110 is shown in Figure 4-272 and described in Table 4-588.

COMPARE10 high

Table 4-587. PRU_ICSS_IEP_COMPARE110 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0D4h

Figure 4-272. PRU_ICSS_IEP_COMPARE110 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-588. PRU_ICSS_IEP_COMPARE110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 10 high value

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4.5.10.55 PRU_ICSS_IEP_COMPARE011 Register (Offset = D8h) [reset = 0h]

PRU_ICSS_IEP_COMPARE011 is shown in Figure 4-273 and described in Table 4-590.

COMPARE11 low

Table 4-589. PRU_ICSS_IEP_COMPARE011 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0D8h

Figure 4-273. PRU_ICSS_IEP_COMPARE011 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-590. PRU_ICSS_IEP_COMPARE011 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 11 low value

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4.5.10.56 PRU_ICSS_IEP_COMPARE111 Register (Offset = DCh) [reset = 0h]

PRU_ICSS_IEP_COMPARE111 is shown in Figure 4-274 and described in Table 4-592.

COMPARE11 high

Table 4-591. PRU_ICSS_IEP_COMPARE111 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0DCh

Figure 4-274. PRU_ICSS_IEP_COMPARE111 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-592. PRU_ICSS_IEP_COMPARE111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 11 high value

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4.5.10.57 PRU_ICSS_IEP_COMPARE012 Register (Offset = E0h) [reset = 0h]

PRU_ICSS_IEP_COMPARE012 is shown in Figure 4-275 and described in Table 4-594.

COMPARE12 low

Table 4-593. PRU_ICSS_IEP_COMPARE012 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0E0h

Figure 4-275. PRU_ICSS_IEP_COMPARE012 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-594. PRU_ICSS_IEP_COMPARE012 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 12 low value

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4.5.10.58 PRU_ICSS_IEP_COMPARE112 Register (Offset = E4h) [reset = 0h]

PRU_ICSS_IEP_COMPARE112 is shown in Figure 4-276 and described in Table 4-596.

COMPARE12 high

Table 4-595. PRU_ICSS_IEP_COMPARE112 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0E4h

Figure 4-276. PRU_ICSS_IEP_COMPARE112 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-596. PRU_ICSS_IEP_COMPARE112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 12 high value

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4.5.10.59 PRU_ICSS_IEP_COMPARE013 Register (Offset = E8h) [reset = 0h]

PRU_ICSS_IEP_COMPARE013 is shown in Figure 4-277 and described in Table 4-598.

COMPARE13 low

Table 4-597. PRU_ICSS_IEP_COMPARE013 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0E8h

Figure 4-277. PRU_ICSS_IEP_COMPARE013 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-598. PRU_ICSS_IEP_COMPARE013 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 13 low value

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4.5.10.60 PRU_ICSS_IEP_COMPARE113 Register (Offset = ECh) [reset = 0h]

PRU_ICSS_IEP_COMPARE113 is shown in Figure 4-278 and described in Table 4-600.

COMPARE13 high

Table 4-599. PRU_ICSS_IEP_COMPARE113 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0ECh

Figure 4-278. PRU_ICSS_IEP_COMPARE113 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-600. PRU_ICSS_IEP_COMPARE113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 13 high value

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4.5.10.61 PRU_ICSS_IEP_COMPARE014 Register (Offset = F0h) [reset = 0h]

PRU_ICSS_IEP_COMPARE014 is shown in Figure 4-279 and described in Table 4-602.

COMPARE14 low

Table 4-601. PRU_ICSS_IEP_COMPARE014 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0F0h

Figure 4-279. PRU_ICSS_IEP_COMPARE014 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-602. PRU_ICSS_IEP_COMPARE014 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 14 low value

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4.5.10.62 PRU_ICSS_IEP_COMPARE114 Register (Offset = F4h) [reset = 0h]

PRU_ICSS_IEP_COMPARE114 is shown in Figure 4-280 and described in Table 4-604.

COMPARE14 high

Table 4-603. PRU_ICSS_IEP_COMPARE114 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0F4h

Figure 4-280. PRU_ICSS_IEP_COMPARE114 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-604. PRU_ICSS_IEP_COMPARE114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 14 high value

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4.5.10.63 PRU_ICSS_IEP_COMPARE015 Register (Offset = F8h) [reset = 0h]

PRU_ICSS_IEP_COMPARE015 is shown in Figure 4-281 and described in Table 4-606.

COMPARE15 low

Table 4-605. PRU_ICSS_IEP_COMPARE015 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0F8h

Figure 4-281. PRU_ICSS_IEP_COMPARE015 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-606. PRU_ICSS_IEP_COMPARE015 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 15 low value

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4.5.10.64 PRU_ICSS_IEP_COMPARE115 Register (Offset = FCh) [reset = 0h]

PRU_ICSS_IEP_COMPARE115 is shown in Figure 4-282 and described in Table 4-608.

COMPARE15 high

Table 4-607. PRU_ICSS_IEP_COMPARE115 Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E0FCh

Figure 4-282. PRU_ICSS_IEP_COMPARE115 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMP																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-608. PRU_ICSS_IEP_COMPARE115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CMP	R/W	0h	Compare 15 high value

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4.5.10.65 PRU_ICSS_IEP_LOW_COUNTER_RESET_VALUE Register (Offset = 100h) [reset = 0h]

PRU_ICSS_IEP_LOW_COUNTER_RESET_VALUE is shown in Figure 4-283 and described in Table 4-610.

Reset value of the Master Counter (lower 32-bits).

Table 4-609. PRU_ICSS_IEP_LOW_COUNTER_RESET_VALUE Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E100h

Figure 4-283. PRU_ICSS_IEP_LOW_COUNTER_RESET_VALUE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-610. PRU_ICSS_IEP_LOW_COUNTER_RESET_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESET_VAL	R/W	0h	Reset value (lower 32-bits). This register enables SW to define the reset state of the Master Counter, which can be reset by the following events (if enabled): CMP0 event; eHRPWM0_SYNCO event; eHRPWM3_SYNCO event. The RESET_VAL should be in increments of the DEFAULT_INC (default state is 5). For example, 0000_000Ah.

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4.5.10.66 PRU_ICSS_IEP_HIGH_COUNTER_RESET_VALUE Register (Offset = 104h) [reset = 0h]

PRU_ICSS_IEP_HIGH_COUNTER_RESET is shown in Figure 4-284 and described in Table 4-612.

Reset value of the Master Counter (upper 32-bits).

Table 4-611. PRU_ICSS_IEP_HIGH_COUNTER_RESET_VALUE Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E104h

Figure 4-284. PRU_ICSS_IEP_HIGH_COUNTER_RESET_VALUE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-612. PRU_ICSS_IEP_HIGH_COUNTER_RESET_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESET_VAL	R/W	0h	This enables SW to define the reset state of the Master counter when it gets reset do to the following 3 possible events if enabled: CMP0 event; eHRPWM0_SYNCO event; eHRPWM3_SYNCO event. It should be in increments of the DEFAULT_INC, default state is 5 For example, 0000_000Ah

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4.5.10.67 PRU_ICSS_IEP_PWM Register (Offset = 108h) [reset = 0h]

PRU_ICSS_IEP_PWM is shown in Figure 4-285 and described in Table 4-614.

PWM Sync Out

Table 4-613. PRU_ICSS_IEP_PWM Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E108h

Figure 4-285. PRU_ICSS_IEP_PWM Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PWM3_HIT	PWM3_RST_CNT_EN	PWM0_HIT	PWM0_RST_CNT_EN
R-0h				RW1Clr-0h	R/W-0h	RW1Clr-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; RW1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-614. PRU_ICSS_IEP_PWM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PWM3_HIT	RW1Clr	0h	The raw status bit of eHRPWM3_SYNCO event. 0h: No eHRPWM3_SYNCO event 1h: eHRPWM3_SYNCO event occurred Write 1h to Clear.
2	PWM3_RST_CNT_EN	R/W	0h	Enable the reset of the counter by a eHRPWM3_SYNCO event. 0h: Disable 1h: Enable the reset of the counter if a eHRPWM3_SYNCO event occurs
1	PWM0_HIT	RW1Clr	0h	The raw status bit of eHRPWM0_SYNCO event. 0h: No eHRPWM0_SYNCO event 1h: eHRPWM0_SYNCO event occurred Write 1 to Clear.
0	PWM0_RST_CNT_EN	R/W	0h	Enable the reset of the counter by a eHRPWM0_SYNCO event. 0h: Disable 1h: Enable the reset of the counter if a eHRPWM0_SYNCO event occurs

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4.5.10.68 PRU_ICSS_IEP_SYNC_CTRL Register (Offset = 180h) [reset = 0h]

PRU_ICSS_IEP_SYNC_CTRL is shown in Figure 4-286 and described in Table 4-616.

SYNC GENERATION CONTROL

Table 4-615. PRU_ICSS_IEP_SYNC_CTRL Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E180h

Figure 4-286. PRU_ICSS_IEP_SYNC_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							SYNC1_IND_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
SYNC1_CYCLIC_EN	SYNC1_ACK_EN	SYNC0_CYCLIC_EN	SYNC0_ACK_EN	RESERVED	SYNC1_EN	SYNC0_EN	SYNC_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-616. PRU_ICSS_IEP_SYNC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	SYNC1_IND_EN	R/W	0h	SYNC1 independent mode enable. Independent mode means the SYNC1 signal can be different from SYNC0. 0h: Dependent mode 1h: Independent mode
7	SYNC1_CYCLIC_EN	R/W	0h	SYNC1 single shot or cyclic/auto generation mode enable 0h: Disable, single shot mode 1h: Enable, cyclic generation mode
6	SYNC1_ACK_EN	R/W	0h	SYNC1 acknowledgement mode enable 0h: Disable, SYNC1 will go low after pulse width is met. 1h: Enable, SYNC1 will remain asserted until receiving software acknowledges by reading PRU_ICSS_IEP_SYNC1_STAT which clears on read.
5	SYNC0_CYCLIC_EN	R/W	0h	SYNC0 single shot or cyclic/auto generation mode enable 0h: Disable, single shot mode 1h: Enable, cyclic generation mode
4	SYNC0_ACK_EN	R/W	0h	SYNC0 acknowledgement mode enable 0h: Disable, SYNC0 will go low after pulse width is met. 1h: Enable, SYNC0 will remain asserted until receiving software acknowledges by reading PRU_ICSS_IEP_SYNC0_STAT which clears on read.
3	RESERVED	R	0h	Reserved

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Table 4-616. PRU_ICSS_IEP_SYNC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SYNC1_EN	R/W	0h	SYNC1 generation enable 0h: Disable SYNC1 generation. If SYNC1 is low, it will stop immediately. If SYNC1 is high, it will stop after SYNC1 goes low 1h: Enable SYNC1 generation
1	SYNC0_EN	R/W	0h	SYNC0 generation enable 0h: Disable SYNC0 generation. If SYNC0 is low, it will stop immediately If SYNC0 is high, it will stop after SYNC0 goes low 1h: Enable SYNC0 generation
0	SYNC_EN	R/W	0h	SYNC generation enable 0h: Disable the generation and clocking of SYNC0 and SYNC1 logic. If SYNC0 AND SYNC1 is low, it will stop immediately. If SYNC0 OR SYNC1 is high, it will stop after SYCN0 AND SYNC1 goes low. Note that you might get 1 extra high pulse if this is disabled during a high pulse of one and the 2nd pulse goes high before the last pulse low if you do not de-assert sync0_en and sync1_en at the same time. SW should always de-assert both sync1_en and sync0_en at the same time as sync_en is de-asserted 1h: Enables SYNC0 and SYNC1 generation

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4.5.10.69 PRU_ICSS_IEP_SYNC_FIRST_STAT Register (Offset = 184h) [reset = 0h]

PRU_ICSS_IEP_SYNC_FIRST_STAT is shown in Figure 4-287 and described in Table 4-618.

SYNC GENERATION FIRST EVENT STATUS

Table 4-617. PRU_ICSS_IEP_SYNC_FIRST_STAT Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E184h

Figure 4-287. PRU_ICSS_IEP_SYNC_FIRST_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						FIRST_SYNC1	FIRST_SYNC0
R-0h						R-0h	R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 4-618. PRU_ICSS_IEP_SYNC_FIRST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	FIRST_SYNC1	R	0h	SYNC1 First Event status 0h: SYNC1 first event has NOT occurred 1h: SYNC1 first event has occurred. This bits is cleared when sync1_en = 0
0	FIRST_SYNC0	R	0h	SYNC0 First Event status 0h: SYNC0 first event has not occurred 1h: SYNC0 first event has occurred. This bits is cleared when sync0_en = 0

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4.5.10.70 PRU_ICSS_IEP_SYNC0_STAT Register (Offset = 188h) [reset = 0h]

PRU_ICSS_IEP_SYNC0_STAT is shown in Figure 4-288 and described in Table 4-620.

SYNC0 STATUS

Table 4-619. PRU_ICSS_IEP_SYNC0_STAT Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E188h

Figure 4-288. PRU_ICSS_IEP_SYNC0_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							SYNC0_PEND
R-0h							RWr1Clr-0h

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-620. PRU_ICSS_IEP_SYNC0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SYNC0_PEND	RWr1Clr	0h	SYNC0 pending state 0h: SYNC0 is not pending 1h: SYNC0 is pending or has occurred when SYNC0_ACK_EN = 0 (Disable). Write "1" to clear

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4.5.10.71 PRU_ICSS_IEP_SYNC1_STAT Register (Offset = 18Ch) [reset = 0h]

PRU_ICSS_IEP_SYNC1_STAT is shown in Figure 4-289 and described in Table 4-622.

SYNC1 STATUS

Table 4-621. PRU_ICSS_IEP_SYNC1_STAT Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E18Ch

Figure 4-289. PRU_ICSS_IEP_SYNC1_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							SYNC1_PEND
R-0h							RWr1Clr-0h

LEGEND: R = Read Only; RWr1Clr = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 4-622. PRU_ICSS_IEP_SYNC1_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SYNC1_PEND	RWr1Clr	0h	SYNC1 pending state 0h: SYNC1 is not pending 1h: SYNC1 is pending or has occurred when SYNC1_ACK_EN = 0 (Disable). Write "1" to Clear

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4.5.10.72 PRU_ICSS_IEP_SYNC_PWIDTH Register (Offset = 190h) [reset = 0h]

PRU_ICSS_IEP_SYNC_PWIDTH is shown in Figure 4-290 and described in Table 4-624.

SYNC PULSE WIDTH CONFIGURE

Table 4-623. PRU_ICSS_IEP_SYNC_PWIDTH Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E190h

Figure 4-290. PRU_ICSS_IEP_SYNC_PWIDTH Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC_HPW																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-624. PRU_ICSS_IEP_SYNC_PWIDTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNC_HPW	R/W	0h	Defines the number of clock cycles SYNC0/1 will be high. Note if SYNC0/1 is disabled during pulse width time (that is, SYNC_CTRL[SYNC0_EN | SYNC1_EN | SYNC_EN] = 0), the ongoing pulse will be terminated. 0h: 1 clock cycle. 1h: 2 clock cycles. Nh: N+1 clock cycles.

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4.5.10.73 PRU_ICSS_IEP_SYNC0_PERIOD Register (Offset = 194h) [reset = 1h]

PRU_ICSS_IEP_SYNC0_PERIOD is shown in Figure 4-291 and described in Table 4-626.

SYNC0 PERIOD CONFIGURE

Table 4-625. PRU_ICSS_IEP_SYNC0_PERIOD Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E194h

Figure 4-291. PRU_ICSS_IEP_SYNC0_PERIOD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC0_PERIOD																															
R/W-1h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-626. PRU_ICSS_IEP_SYNC0_PERIOD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNC0_PERIOD	R/W	1h	Defines the period between the rising edges of SYNC0. 0h: Reserved 1h: 2 clk cycles period N: N+1 clk cycles period

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4.5.10.74 PRU_ICSS_IEP_SYNC1_DELAY Register (Offset = 198h) [reset = 0h]

PRU_ICSS_IEP_SYNC1_DELAY is shown in Figure 4-292 and described in Table 4-628.

SYNC1 DELAY

Table 4-627. PRU_ICSS_IEP_SYNC1_DELAY Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E198h

Figure 4-292. PRU_ICSS_IEP_SYNC1_DELAY Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC1_DELAY																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-628. PRU_ICSS_IEP_SYNC1_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNC1_DELAY	R/W	0h	When SYNC1_IND_EN = 0, defines number of clock cycles from the start of SYNC0 to the start of SYNC1. Note this is the delay before the start of SYNC1. 0h: No delay. 1h: 1 clock cycle delay. Nh: N clock cycles delay. When SYNC1_IND_EN = 1, defines the period between the rising edges of SYNC1. 0h: Reserved. 1h: 2 clock cycles period. Nh: N+1 clock cycles period.

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4.5.10.75 PRU_ICSS_IEP_SYNC_START Register (Offset = 19Ch) [reset = 0h]

PRU_ICSS_IEP_SYNC_START is shown in Figure 4-293 and described in Table 4-630.

SYNC START CONFIGURE

Table 4-629. PRU_ICSS_IEP_SYNC_START Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E19Ch

Figure 4-293. PRU_ICSS_IEP_SYNC_START Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNC_START																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-630. PRU_ICSS_IEP_SYNC_START Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SYNC_START	R/W	0h	Defines the start time after the activation event. 0h: 1 clock cycle delay. Nh: N+1 clock cycles delay.

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4.5.10.76 PRU_ICSS_IEP_WD_PREDIV Register (Offset = 200h) [reset = 4E20h]

PRU_ICSS_IEP_WD_PREDIV is shown in Figure 4-294 and described in Table 4-632.

WATCHDOG PRE-DIVIDER

Table 4-631. PRU_ICSS_IEP_WD_PREDIV Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E200h

Figure 4-294. PRU_ICSS_IEP_WD_PREDIV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PRE_DIV															
R-0h																R/W-4E20h															

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-632. PRU_ICSS_IEP_WD_PREDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	PRE_DIV	R/W	4E20h	Defines the number of ICSS_IEP_CLK cycles per WD clock event. Note that the WD clock is a free-running clock. The value 0x4e20 (or 20000) generates a rate of 100 us if ICSS_IEP_CLK is 200 MHz. seconds/(WD event) = (clock cycles per WD event)/(clock cycles per second) = 20000/(200 x [10]^6) = 100us

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4.5.10.77 PRU_ICSS_IEP_PDI_WD_TIM Register (Offset = 204h) [reset = 3E8h]

PRU_ICSS_IEP_PDI_WD_TIM is shown in Figure 4-295 and described in Table 4-634.

PDI WATCHDOG TIMER CONFIGURE

Table 4-633. PRU_ICSS_IEP_PDI_WD_TIM Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E204h

Figure 4-295. PRU_ICSS_IEP_PDI_WD_TIM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PDI_WD_TIME															
R-0h																R/W-3E8h															

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-634. PRU_ICSS_IEP_PDI_WD_TIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	PDI_WD_TIME	R/W	3E8h	Defines the number of WD ticks (or increments) for PDI WD, that is, the number of WD increments. If PRU_ICSS_IEP_WD_PREDIV[15-0] PRE_DIV is set to 100us, then the value 0x03e8 (or 1000) provides a rate of 100ms. Read returns the current count. Counter is reset by software write to register or when Digital Data In capture occurs. WD is disabled if WD time is set to 0x0. Note when an expiration event occurs, the expiration counter (PDI_EXP_CNT) increments and status (PDI_WD_STAT) clears.

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4.5.10.78 PRU_ICSS_IEP_PD_WD_TIM Register (Offset = 208h) [reset = 3E8h]

PRU_ICSS_IEP_PD_WD_TIM is shown in Figure 4-296 and described in Table 4-636.

PD WATCHDOG TIMER CONFIGURE

Table 4-635. PRU_ICSS_IEP_PD_WD_TIM Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E208h

Figure 4-296. PRU_ICSS_IEP_PD_WD_TIM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PD_WD_TIME															
R-0h																R/W-3E8h															

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-636. PRU_ICSS_IEP_PD_WD_TIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	PD_WD_TIME	R/W	3E8h	Defines the number of WD ticks (or increments) for PD WD, that is, the number of WD increments. If PRU_ICSS_IEP_WD_PREDIV[15-0] PRE_DIV is set to 100us, then 0x03e8 (or 1000) provides a rate of 100ms. Read returns the current count. Counter is reset by software write to register or every write access to Sync Managers with WD trigger enable bit set. WD is disabled if WD time is set to 0x0. Expiration actions: Increment expiration counter, clear status. Digital Data out forced to zero if pr[k]_edio_oe_ext = 1 and PRU_ICSS_IEP_DIGIO_EXP[0] SW_DATA_OUT_UPDATE = 0.

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4.5.10.79 PRU_ICSS_IEP_WD_STATUS Register (Offset = 20Ch) [reset = 00010001h]

PRU_ICSS_IEP_WD_STATUS is shown in Figure 4-297 and described in Table 4-638.

WATCHDOG STATUS

Table 4-637. PRU_ICSS_IEP_WD_STATUS Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E20Ch

Figure 4-297. PRU_ICSS_IEP_WD_STATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							PDI_WD_STAT
R-0h							R-1h
15	14	13	12	11	10	9	8
Galileo BCM 047:RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PD_WD_STAT
R-0h							R-1h

LEGEND: R = Read Only; *-n* = value after reset

Table 4-638. PRU_ICSS_IEP_WD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	PDI_WD_STAT	R	1h	WD PDI status. 0h: Expired (PDI_WD_EXP event generated) 1h: Active or disabled
15-1	RESERVED	R	0h	Reserved
0	PD_WD_STAT	R	1h	WD PD status (triggered by Sync Mangers status). 0h: Expired (PD_WD_EXP event generated) 1h: Active or disabled

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4.5.10.80 PRU_ICSS_IEP_WD_EXP_CNT Register (Offset = 210h) [reset = 0h]

PRU_ICSS_IEP_WD_EXP_CNT is shown in Figure 4-298 and described in Table 4-640.

WATCHDOG TIMER EXPIRATION COUNTER

Table 4-639. PRU_ICSS_IEP_WD_EXP_CNT Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E210h

Figure 4-298. PRU_ICSS_IEP_WD_EXP_CNT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PD_EXP_CNT								PDI_EXP_CNT							
RWrClr-0h								RWrClr-0h							

LEGEND: R = Read Only; RWrClr = Read/Cleared upon Write; *-n* = value after reset

Table 4-640. PRU_ICSS_IEP_WD_EXP_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-8	PD_EXP_CNT	RWrClr	0h	WD PD expiration counter. Counter increments on every PD time out and stops at FFh.
7-0	PDI_EXP_CNT	RWrClr	0h	WD PDI expiration counter. Counter increments on every PDI time out and stops at FFh.

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4.5.10.81 PRU_ICSS_IEP_WD_CTRL Register (Offset = 214h) [reset = 0h]

PRU_ICSS_IEP_WD_CTRL is shown in Figure 4-299 and described in Table 4-642.

WATCHDOG CONTROL

Table 4-641. PRU_ICSS_IEP_WD_CTRL Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E214h

Figure 4-299. PRU_ICSS_IEP_WD_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							PDI_WD_EN
R-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PD_WD_EN
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-642. PRU_ICSS_IEP_WD_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	PDI_WD_EN	R/W	0h	Watchdog PDI 0h: Disable 1h: Enable
15-1	RESERVED	R	0h	Reserved
0	PD_WD_EN	R/W	0h	Watchdog PD 0h: Disable 1h: Enable

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4.5.10.82 PRU_ICSS_IEP_DIGIO_CTRL Register (Offset = 300h) [reset = 4h]

PRU_ICSS_IEP_DIGIO_CTRL is shown in Figure 4-300 and described in Table 4-644.

DIGITAL INPUT OUTPUT CONTROL

Table 4-643. PRU_ICSS_IEP_DIGIO_CTRL Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E300h

Figure 4-300. PRU_ICSS_IEP_DIGIO_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
OUT_MODE		IN_MODE		WD_MODE	BIDI_MODE	OUTVALID_MODE	OUTVALID_POL
R/W-0h		R/W-0h		R/W-0h	R-1h	R/W-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-644. PRU_ICSS_IEP_DIGIO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-6	OUT_MODE	R/W	0h	Defines events that triggers data out to be updated. Note if OUTVALID_MODE is set, then data out is forced to zero if a WD PD expiration occurs (PD_WD_EXP) from the WD block and pr<k>_edio_oe_ext = 1. 0h: PRU0/1_RX_EOF 1h: Reserved 2h: DC SYNC0 event 3h: DC SYNC1 event
5-4	IN_MODE	R/W	0h	Defines event that triggers data in to be sampled 0h: PRU0/1_RX_SOF 1h: Rising edge of external PR<k>_EDC_LATCH0_IN signal 2h: DC rising edge of SYNC0 event 3h: DC rising edge of SYNC1 event
3	WD_MODE	R/W	0h	Defines Watchdog behavior 0h: Outputs are reset immediately after watchdog expires 1h: Outputs are reset with next output event that follows watchdog expiration

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Table 4-644. PRU_ICSS_IEP_DIGIO_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	BIDI_MODE	R	1h	Defines the digital input/output direction. NOTE THAT DUE TO INTEGRATION, ACTUAL MODE IS UNIDIRECTIONAL IN THIS DEVICE. 0h: Unidirectional mode: digital input/output direction of pins configured individually 1h: Bidirectional mode: all I/O pins are bidirectional and direction configuration is ignored
1	OUTVALID_MODE	R/W	0h	Defines the outvalid mode behavior. 0h: Output event signaling 1h: Output data is updated if watchdog is triggered. Output data is forced to zero if PD_WD_EXP from the WD block and pr1_edio_oe_ext = 1
0	OUTVALID_POL	R	0h	Defines OUTVALID polarity 0h: Active High 1h: Active Low

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4.5.10.83 PRU_ICSS_IEP_DIGIO_STATUS Register (Offset = 304h) [reset = 0h]

PRU_ICSS_IEP_DIGIO_STATUS is shown in Figure 4-301 and described in Table 4-646.

DIGITAL INPUT OUTPUT STATUS

Table 4-645. PRU_ICSS_IEP_DIGIO_STATUS Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E304h

Figure 4-301. PRU_ICSS_IEP_DIGIO_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIGIO_STAT																															
R-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-646. PRU_ICSS_IEP_DIGIO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DIGIO_STAT	R	0h	Reserved

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4.5.10.84 PRU_ICSS_IEP_DIGIO_DATA_IN Register (Offset = 308h) [reset = -h]

PRU_ICSS_IEP_DIGIO_DATA_IN is shown in Figure 4-302 and described in Table 4-648.

DIGITAL DATA INPUT

Table 4-647. PRU_ICSS_IEP_DIGIO_DATA_IN Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E308h

Figure 4-302. PRU_ICSS_IEP_DIGIO_DATA_IN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_IN																															
R--h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-648. PRU_ICSS_IEP_DIGIO_DATA_IN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_IN	R	-h	Data input. Digital inputs can be configured to be sampled in four ways. 1h: Digital inputs are sampled at the start of each frame. The SOF signal can be used externally to update the input data, because the SOF is signaled before input data is sampled. 2h: The sample time can be controlled externally by using them PR<k>_EDC_LATCH0_IN signal. 3h: Digital inputs are sampled at SYNC0 events. 4h: Digital inputs are sampled at SYNC1 events. These can be configured by [5-4] IN_MODE bit field in the PRU_ICSS_IEP_DIGIO_CTRL register.

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4.5.10.85 PRU_ICSS_IEP_DIGIO_DATA_IN_RAW Register (Offset = 30Ch) [reset = -h]

PRU_ICSS_IEP_DIGIO_DATA_IN_RAW is shown in Figure 4-303 and described in Table 4-650.

DIGITAL DATA INPUT DIRECT SAMPLE

Table 4-649. PRU_ICSS_IEP_DIGIO_DATA_IN_RAW Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E30Ch

Figure 4-303. PRU_ICSS_IEP_DIGIO_DATA_IN_RAW Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_IN_RAW																															
R--h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 4-650. PRU_ICSS_IEP_DIGIO_DATA_IN_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_IN_RAW	R	-h	Data input which direct sample of PR<k>_EDIO_DATA[0:31]. Only PR<k>_EDIO_DATA[0:3] are exported to device pins in this device.

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4.5.10.86 PRU_ICSS_IEP_DIGIO_DATA_OUT Register (Offset = 310h) [reset = 0h]

PRU_ICSS_IEP_DIGIO_DATA_OUT is shown in Figure 4-304 and described in Table 4-652.

DIGITAL DATA OUTPUT

Table 4-651. PRU_ICSS_IEP_DIGIO_DATA_OUT Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E310h

Figure 4-304. PRU_ICSS_IEP_DIGIO_DATA_OUT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_OUT																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-652. PRU_ICSS_IEP_DIGIO_DATA_OUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_OUT	R/W	0h	Data output. Digital outputs can be configured to be updated in four ways. 1h: Digital outputs are updated at the end of each frame (EOF mode). 2h: Digital outputs are updated with SYNC0 events 3h: Digital outputs are updated SYNC1 events. 4h: Digital outputs are updated at the end of a frame which triggered the Process Data Watchdog. Digital Outputs are only updated if the frame was correct (WD_TRIG mode). These can be configured by [7-6] OUT_MODE bit field in the PRU_ICSS_IEP_DIGIO_CTRL.

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4.5.10.87 PRU_ICSS_IEP_DIGIO_DATA_OUT_EN Register (Offset = 314h) [reset = 0h]

PRU_ICSS_IEP_DIGIO_DATA_OUT_EN is shown in Figure 4-305 and described in Table 4-654.

DIGITAL DATA OUT ENABLE

Table 4-653. PRU_ICSS_IEP_DIGIO_DATA_OUT_EN Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E314h

Figure 4-305. PRU_ICSS_IEP_DIGIO_DATA_OUT_EN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA_OUT_EN																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 4-654. PRU_ICSS_IEP_DIGIO_DATA_OUT_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA_OUT_EN	R/W	0h	Data input which controls tri-state of PR<k>_EDIO_DATA[0:3] 0h: Driver enabled. 1h: Sets outputs to HiZ.

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4.5.10.88 PRU_ICSS_IEP_DIGIO_EXP Register (Offset = 318h) [reset = 20h]

PRU_ICSS_IEP_DIGIO_EXP is shown in Figure 4-306 and described in Table 4-656.

DIGIO EXPANSION REGISTER

Table 4-655. PRU_ICSS_IEP_DIGIO_EXP Instances

Instance	Physical Address
PRU_ICSS_IEP	4802 E318h

Figure 4-306. PRU_ICSS_IEP_DIGIO_EXP Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		EOF_SEL	SOF_SEL	SOF_DLY			
R-0h		R/W-0h	R/W-0h	R/W-0h			
7	6	5	4	3	2	1	0
OUTVALID_DLY				RESERVED	SW_OUTVALID	OUTVALID_OVR_EN	SW_DATA_OUT_UPDATE
R/W-2h				R-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 4-656. PRU_ICSS_IEP_DIGIO_EXP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13	EOF_SEL	R/W	0h	Defines which RX_EOF is used for PR<k>_EDIO_DATA_IN[0:3] capture 0h: PRU0_RX_EOF 1h: PRU1_RX_EOF
12	SOF_SEL	R/W	0h	Defines which RX_SOF is used for PR<k>_EDIO_DATA_IN[0:3] capture 0h: PRU0_RX_SOF 1h: PRU1_RX_SOF
11-8	SOF_DLY	R/W	0h	Define the number of iep_clk (ICSS_IEP_CLK) cycle delay of SOF PR<k>_EDIO_DATA_IN[0:3] capture
7-4	OUTVALID_DLY	R/W	2h	Define the number of iep_clk (ICSS_IEP_CLK) cycle delay on assertion of PR<k>_EDIO_OUTVALID. Min is 2 clock cycles. Max is 16 clock cycles
3	RESERVED	R	0h	Reserved
2	SW_OUTVALID	R/W	0h	PR<k>_EDIO_OUTVALID = SW_OUTVALID, only if OUTVALID_OVR_EN is set.
1	OUTVALID_OVR_EN	R/W	0h	Software override enable 0h: Disable override 1h: Enable override

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Table 4-656. PRU_ICSS_IEP_DIGIO_EXP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SW_DATA_OUT_UPDATE	R/W	0h	Defines the value of pr<k>_edio_data_out when OUTVALID_OVR_EN = 1. Read 0: Start bit event has not occurred Read 1: Start bit event occurred Write 0: No effect Write 1: Causes an update of pr<k>_edio_data_out by software data out

4.6 CCMR Registers

Table 4-657. MSS_R5SS[0:1]_CCMR Registers Base Address Table

Offset	Length	Acronym	MSS_R5SS0_CCMR Physical Address	MSS_R5SS1_CCMR Physical Address
0h	32	CCMR_CCMSR1	5321 0000h	5321 1000h
4h	32	CCMR_CCMKEYR1	5321 0004h	5321 1004h
8h	32	CCMR_CCMSR2	5321 0008h	5321 1008h
Ch	32	CCMR_CCMKEYR2	5321 000Ch	5321 100Ch
10h	32	CCMR_CCMSR3	5321 0010h	5321 1010h
14h	32	CCMR_CCMKEYR3	5321 0014h	5321 1014h
18h	32	CCMR_CCMPOLCNTRL	5321 0018h	5321 1018h

4.6.1 CCMR Instance Count Note

Note

n = 0 to 1 for the CCMR registers defined below.

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4.6.2 MSS_R5SSn_CCMR_CCMSR1 Registers

4.6.2.1 R5SSn_CCMR_CCMSR1 Register (Offset = 0h) [reset = h]

Short Description: CPU Compare Status Register

Long Description:

Return to Summary Table

Table 4-658. Instance Table

Instance Name	Physical Address
R5SS0_CCMR	5321 0000h
R5SS1_CCMR	5321 1000h

Access Types Legend

Table 4-659. CCMSR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	NU2	RW	0h	Reserved
16	CMPE1	RW	0h	Compare Error0 = CPU signals are identical1= CPU signal compare mismatchWrites '1' to clear this bit
15 - 9	NU1	RW	0h	Reserved
8	STC1	RW	0h	Self Test Complete0 = self test on-going if self test mode asserted1 = self test is completeWrites have no effect
7 - 2	NU0	RW	0h	Reserved
1	STET1	RW	0h	Self Test Error Type0 = self test failed during Compare Match test1 = self test failed during Compare mismatch testWrites have no effect
0	STE1	RO	0h	Self Test Error0 = self test passed1 = self test failedWrites have no effect

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4.6.3 MSS_R5SSn_CCMR_CCMKEYR1 Registers

4.6.3.1 R5SSn_CCMR_CCMKEYR1 Register (Offset = 4h) [reset = h]

Short Description: CPU Compare Key Register

Long Description:

Return to Summary Table

Table 4-660. Instance Table

Instance Name	Physical Address
R5SS0_CCMR	5321 0004h
R5SS1_CCMR	5321 1004h

Access Types Legend

Table 4-661. CCMKEYR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU3	RW	0h	Reserved
3 - 0	MKEY1	RW	0h	Mode Key0000 = lock step mode0110 = self test mode1001 = error forcing mode1111 = self test error forcing mode

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4.6.4 MSS_R5SSn_CCMR_CCMSR2 Registers

4.6.4.1 R5SSn_CCMR_CCMSR2 Register (Offset = 8h) [reset = h]

Short Description: VIM Compare Status Register

Long Description:

Return to Summary Table

Table 4-662. Instance Table

Instance Name	Physical Address
R5SS0_CCMR	5321 0008h
R5SS1_CCMR	5321 1008h

Access Types Legend

Table 4-663. CCMSR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	NU6	RW	0h	Reserved
16	CMPE2	RW	0h	Compare Error0 = VIM signals are identical1= VIM signal compare mismatchWrites '1' to clear this bit
15 - 9	NU5	RW	0h	Reserved
8	STC2	RW	0h	Self Test Complete0 = self test on-going if self test mode asserted1 = self test is completeWrites have no effect
7 - 2	NU4	RW	0h	Reserved
1	STET2	RW	0h	Self Test Error Type0 = self test failed during Compare Match test1 = self test failed during Compare mismatch testWrites have no effect
0	STE2	RW	0h	Self Test Error0 = self test passed1 = self test failedWrites have no effect

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4.6.5 MSS_R5SSn_CCMR_CCMKEYR2 Registers

4.6.5.1 R5SSn_CCMR_CCMKEYR2 Register (Offset = Ch) [reset = h]

Short Description: VIM Compare Key Register

Long Description:

Return to Summary Table

Table 4-664. Instance Table

Instance Name	Physical Address
R5SS0_CCMR	5321 000Ch
R5SS1_CCMR	5321 100Ch

Access Types Legend

Table 4-665. CCMKEYR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU7	RW	0h	Reserved
3 - 0	MKEY2	RW	0h	Mode Key0000 = lock step mode0110 = self test mode1001 = error forcing mode1111 = self test error forcing mode

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4.6.6 MSS_R5SSn_CCMR_CCMSR3 Registers

4.6.6.1 R5SSn_CCMR_CCMSR3 Register (Offset = 10h) [reset = h]

Short Description: Inactivity Monitor Status Register

Long Description:

Return to Summary Table

Table 4-666. Instance Table

Instance Name	Physical Address
R5SS0_CCMR	5321 0010h
R5SS1_CCMR	5321 1010h

Access Types Legend

Table 4-667. CCMSR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	NU10	RW	0h	Reserved
16	CMPE3	RW	0h	Compare Error0 = Inactivity monitor signals are identical1= Inactivity monitor signal compare mismatchWrites '1' to clear this bit
15 - 9	NU9	RW	0h	Reserved
8	STC3	RW	0h	Self Test Complete0 = self test on-going if self test mode asserted1 = self test is completeWrites have no effect
7 - 2	NU8	RW	0h	Reserved
1	STET3	RW	0h	Self Test Error Type0 = self test failed during Compare Match test1 = self test failed during Compare mismatch testWrites have no effect
0	STE3	RO	0h	Self Test Error0 = self test passed1 = self test failedWrites have no effect

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4.6.7 MSS_R5SSn_CCMR_CCMKEYR3 Registers

4.6.7.1 R5SSn_CCMR_CCMKEYR3 Register (Offset = 14h) [reset = h]

Short Description: Inactivity Monitor Key Register

Long Description:

Return to Summary Table

Table 4-668. Instance Table

Instance Name	Physical Address
R5SS0_CCMR	5321 0014h
R5SS1_CCMR	5321 1014h

Access Types Legend

Table 4-669. CCMKEYR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU11	RW	0h	Reserved
3 - 0	MKEY3	RW	0h	Mode Key0000 = lock step mode0110 = self test mode1001 = error forcing mode1111 = self test error forcing mode

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4.6.8 MSS_R5SSn_CCMR_CCMPOLCNTRL Registers

4.6.8.1 R5SSn_CCMR_CCMPOLCNTRL Register (Offset = 18h) [reset = h]

Short Description: CPU Compare Polarity Control Register

Long Description:

Return to Summary Table

Table 4-670. Instance Table

Instance Name	Physical Address
R5SS0_CCMR	5321 0018h
R5SS1_CCMR	5321 1018h

Access Types Legend

Table 4-671. CCMPOLCNTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU12	RW	0h	Reserved
7 - 0	POL_INV	RO	0h	This value is used to invert the 8 XOR of the CPU1 to create compare fail in functional active compare mode. User and privilege mode read = Returns current value of the POL INVPrivilege mode write = Update the values of POL INV

4.6.9 Access Table

Table 4-672. Access Type Codes

Access Type	Code	Description
RW	RW	Read / Write
RO	RO	Read

4.7 PBIST Registers

Table 4-673. TOP_PBIST Registers Base Address Table

Offset	Length	Acronym	TOP_PBIST Physical Address
100h	16	PBIST_A0	5330 0100h
104h	16	PBIST_A1	5330 0104h
108h	32	PBIST_A2	5330 0108h
10Ch	16	PBIST_A3	5330 010Ch
110h	8	PBIST_L0	5330 0110h
114h	8	PBIST_L1	5330 0114h
118h	32	PBIST_L2	5330 0118h
11Ch	32	PBIST_L3	5330 011Ch
120h	32	PBIST_DD10	5330 0120h
124h	8	PBIST_DE10	5330 0124h
130h	0	PBIST_CA0	5330 0130h
134h	8	PBIST_CA1	5330 0134h
138h	0	PBIST_CA2	5330 0138h
13Ch	0	PBIST_CA3	5330 013Ch
140h	8	PBIST_CL0	5330 0140h
144h	8	PBIST_CL1	5330 0144h
148h	16	PBIST_CL2	5330 0148h
14Ch	32	PBIST_CL3	5330 014Ch
150h	32	PBIST_CI0	5330 0150h

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Table 4-673. TOP_PBIST Registers Base Address Table (continued)

Offset	Length	Acronym	TOP_PBIST Physical Address
154h	8	PBIST_CI1	5330 0154h
158h	32	PBIST_CI2	5330 0158h
15Ch	32	PBIST_CI3	5330 015Ch
160h	32	PBIST_RAMT	5330 0160h

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4.7.1 TOP_PBIST_A0 Registers

4.7.1.1 PBIST_A0 Register (Offset = 100h) [reset = h]

Short Description: Variable Address Register0

Long Description:

Return to Summary Table

Table 4-674. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0100h

Access Types Legend

Table 4-675. PBIST_A0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	PBIST_CI2	RW	0h	TI Internal Register.Reserved for HW RnD

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4.7.2 TOP_PBIST_A1 Registers

4.7.2.1 PBIST_A1 Register (Offset = 104h) [reset = h]

Short Description: Variable Address Register1

Long Description:

Return to Summary Table

Table 4-676. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0104h

Access Types Legend

Table 4-677. PBIST_A1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	PBIST_CI3	RW	0h	TI Internal Register.Reserved for HW RnD

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4.7.3 TOP_PBIST_A2 Registers

4.7.3.1 PBIST_A2 Register (Offset = 108h) [reset = h]

Short Description: Variable Address Register2

Long Description:

Return to Summary Table

Table 4-678. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0108h

Access Types Legend

Table 4-679. PBIST_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RGS	RW	0h	TI Internal Register.Reserved for HW RnD These registers do not have a default value after reset.
23 - 16	RDS	RW	0h	TI Internal Register.Reserved for HW RnD These registers do not have a default value after reset.
15 - 8	DWR	RW	0h	TI Internal Register.Reserved for HW RnD These registers do not have a default value after reset.
7 - 0	RAM	RW	0h	TI Internal Register.Reserved for HW RnD These registers do not have a default value after reset.

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4.7.4 TOP_PBIST_A3 Registers

4.7.4.1 PBIST_A3 Register (Offset = 10Ch) [reset = h]

Short Description: Variable Address Register3

Long Description:

Return to Summary Table

Table 4-680. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 010Ch

Access Types Legend

Table 4-681. PBIST_A3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 8	DLR1	RW	Ah	Datalogger Register[8] : Reserevd[9] : Default Testing Mode. When in this mode, ROM-based testing is kicked off. If the intention is to perform go/no-go testing via config, write to both this bit and bit [2] ofthe Datalogger Register simultaneously[15:10] : Reserevd
7 - 0	DLR0	RW	3E8h	Datalogger Register[1:0] : Reserved[2] : ROM-based testing mode. Setting this bit to 1 enables the PBIST controller to execute test algorithms that arestored in the PBIST ROM[3] : Do not change this bit from its default value of 1[4] : Config access mode. Setting this bit allows the host processor to configure the PBIST controller registers[7:5] : Reserved

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4.7.5 TOP_PBIST_L0 Registers

4.7.5.1 PBIST_L0 Register (Offset = 110h) [reset = h]

Short Description: Variable Loop Count Register L0

Long Description:

Return to Summary Table

Table 4-682. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0110h

Access Types Legend

Table 4-683. PBIST_L0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	PBIST_CMS	RW	0h	TI Internal Register.Reserved for HW RnD These registers do not have a default value after reset.

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4.7.6 TOP_PBIST_L1 Registers

4.7.6.1 PBIST_L1 Register (Offset = 114h) [reset = h]

Short Description: Variable Loop Count Register L1

Long Description:

Return to Summary Table

Table 4-684. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0114h

Access Types Legend

Table 4-685. PBIST_L1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	PBIST_PC	RW	0h	TI Internal Register.Reserved for HW RnD

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4.7.7 TOP_PBIST_L2 Registers

4.7.7.1 PBIST_L2 Register (Offset = 118h) [reset = h]

Short Description: Variable Loop Count Register L2

Long Description:

Return to Summary Table

Table 4-686. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0118h

Access Types Legend

Table 4-687. PBIST_L2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	SCR3	RW	10F05Eh	TI Internal Register.Reserved for HW RnD
23 - 16	SCR2	RW	F69B4h	TI Internal Register.Reserved for HW RnD
15 - 8	SCR1	RW	1ADBAh	TI Internal Register.Reserved for HW RnD
7 - 0	SCR0	RW	2710h	TI Internal Register.Reserved for HW RnD

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4.7.8 TOP_PBIST_L3 Registers

4.7.8.1 PBIST_L3 Register (Offset = 11Ch) [reset = h]

Short Description: Variable Loop Count Register L3

Long Description:

Return to Summary Table

Table 4-688. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 011Ch

Access Types Legend

Table 4-689. PBIST_L3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	SCR7	RW	A98AC6h	TI Internal Register.Reserved for HW RnD
23 - 16	SCR6	RW	A8041Ch	TI Internal Register.Reserved for HW RnD
15 - 8	SCR5	RW	9A4822h	TI Internal Register.Reserved for HW RnD
7 - 0	SCR4	RW	98C178h	TI Internal Register.Reserved for HW RnD

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4.7.9 TOP_PBIST_DD10 Registers

4.7.9.1 PBIST_DD10 Register (Offset = 120h) [reset = h]

Short Description: DD0 Data Register 16 (D0)

Long Description:

Return to Summary Table

Table 4-690. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0120h

Access Types Legend

Table 4-691. PBIST_DD10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	CS3	RW	0h	TI Internal Register.Reserved for HW RnD
23 - 16	CS2	RW	0h	TI Internal Register.Reserved for HW RnD
15 - 8	CS1	RW	0h	TI Internal Register.Reserved for HW RnD
7 - 0	CS0	RW	0h	TI Internal Register.Reserved for HW RnD

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4.7.10 TOP_PBIST_DE10 Registers

4.7.10.1 PBIST_DE10 Register (Offset = 124h) [reset = h]

Short Description: DE0 Data Register 16 (D0)

Long Description:

Return to Summary Table

Table 4-692. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0124h

Access Types Legend

Table 4-693. PBIST_DE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 0	PBIST_FDLY	RW	F4628h	TI Internal Register.Reserved for HW RnD

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4.7.11 TOP_PBIST_CA0 Registers

4.7.11.1 PBIST_CA0 Register (Offset = 130h) [reset = h]

Short Description: Constant Address Register0

Long Description:

Return to Summary Table

Table 4-694. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0130h

Access Types Legend

Table 4-695. PBIST_CA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
0	PBIST_PACT	RW	0h	Pbist Active/ROM Clock Enable Register[0]: This bit must be set to turn on internal PBIST clocks. Setting this bit asserts an internal signal that is usedas the clock gate enable. As long as this bit is 0, any access to PBIST will not go through, and PBIST willremain in an almost zero-power mode.Value 0 = Disable internal PBIST clocksValue 1 = Enable internal PBIST clocks

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4.7.12 TOP_PBIST_CA1 Registers

4.7.12.1 PBIST_CA1 Register (Offset = 134h) [reset = h]

Short Description: Constant Address Register1

Long Description:

Return to Summary Table

Table 4-696. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0134h

Access Types Legend

Table 4-697. PBIST_CA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	PBIST_ID	RW	1h	PBIST ID.This is a unique ID assigned to each PBIST controller in a device with multiple PBIST controllers. The value of this register does not affect the functionality of the CPU interface.

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4.7.13 TOP_PBIST_CA2 Registers

4.7.13.1 PBIST_CA2 Register (Offset = 138h) [reset = h]

Short Description: Constant Address Register2

Long Description:

Return to Summary Table

Table 4-698. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0138h

Access Types Legend

Table 4-699. PBIST_CA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
0	PBIST_FSFR0	RO	0h	Fail Status Fail Register- Port 0 This register indicates if a failure occurred during a memory self-test.Value 0 = No failure occurredValue 1 = Indicates a failure

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4.7.14 TOP_PBIST_CA3 Registers

4.7.14.1 PBIST_CA3 Register (Offset = 13Ch) [reset = h]

Short Description: Constant Address Register3

Long Description:

Return to Summary Table

Table 4-700. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 013Ch

Access Types Legend

Table 4-701. PBIST_CA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
0	PBIST_FSFR1	RO	0h	Fail Status Fail Register- Port 1 This register indicates if a failure occurred during a memory self-test.Value 0 = No failure occurredValue 1 = Indicates a failure

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4.7.15 TOP_PBIST_CL0 Registers

4.7.15.1 PBIST_CL0 Register (Offset = 140h) [reset = h]

Short Description: Constant Loop Count Register0

Long Description:

Return to Summary Table

Table 4-702. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0140h

Access Types Legend

Table 4-703. PBIST_CL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	PBIST_FSRCR0	RO	0h	Fail Status Count - Port 0 These registers keep count of the number of failures observed during the memory self-test. The PBISTcontroller stops executing the memory self-test whenever a failure occurs in any memory instance for anyof the test algorithms. The value in gets incremented by one whenever a failure occurs

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4.7.16 TOP_PBIST_CL2 Registers

4.7.16.1 PBIST_CL2 Register (Offset = 148h) [reset = h]

Short Description: Constant Loop Count Register2

Long Description:

Return to Summary Table

Table 4-704. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0148h

Access Types Legend

Table 4-705. PBIST_CL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	PBIST_FSRA1	RO	0h	TI Internal Register.Reserved for HW RnD

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4.7.17 TOP_PBIST_CL3 Registers

4.7.17.1 PBIST_CL3 Register (Offset = 14Ch) [reset = h]

Short Description: Constant Loop Count Register3

Long Description:

Return to Summary Table

Table 4-706. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 014Ch

Access Types Legend

Table 4-707. PBIST_CL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PBIST_FSRDL0	RO	7F7E1FB90 6A8A772B2 8676F312h	TI Internal Register.Reserved for HW RnD

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4.7.18 TOP_PBIST_CI0 Registers

4.7.18.1 PBIST_CI0 Register (Offset = 150h) [reset = h]

Short Description: Constant Increment Register0

Long Description:

Return to Summary Table

Table 4-708. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0150h

Access Types Legend

Table 4-709. PBIST_CI0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PBIST_FSRDL1	RO	7F7E1FB90 6A8A772B2 8676F312h	TI Internal Register.Reserved for HW RnD

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4.7.19 TOP_PBIST_CL1 Registers

4.7.19.1 PBIST_CL1 Register (Offset = 144h) [reset = h]

Short Description: Constant Loop Count Register1

Long Description:

Return to Summary Table

Table 4-710. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0144h

Access Types Legend

Table 4-711. PBIST_CL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	PBIST_FSRCR1	RO	0h	Fail Status Count - Port 1These registers keep count of the number of failures observed during the memory self-test. The PBISTcontroller stops executing the memory self-test whenever a failure occurs in any memory instance for anyof the test algorithms. The value in gets incremented by one whenever a failure occurs

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4.7.20 TOP_PBIST_CI1 Registers

4.7.20.1 PBIST_CI1 Register (Offset = 154h) [reset = h]

Short Description: Constant Increment Register1

Long Description:

Return to Summary Table

Table 4-712. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0154h

Access Types Legend

Table 4-713. PBIST_CI1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1 - 0	PBIST_ROM	RW	Bh	Rom Mask .This two-bit register sets appropriate ROM access modes for the PBIST controller.Value 0h = No information is used from ROMValue 1h = Only RAM Group information from ROMVaule 2h = Only Algorithm information from ROMValue 3h = Both Algorithm and RAM information from ROM. This option should be selected for application self-test.

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4.7.21 TOP_PBIST_CI2 Registers

4.7.21.1 PBIST_CI2 Register (Offset = 158h) [reset = h]

Short Description: Constant Increment Register2

Long Description:

Return to Summary Table

Table 4-714. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0158h

Access Types Legend

Table 4-715. PBIST_CI2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	ALGO3	RW	A98AC7h	This register is used to indicate the algorithm(s) to be used for the memory self-test routine. Each bit corresponds to a specific algorithm.Writing a value 1 to the particular bit, enables the corresponding algorithm.Writing a value 0 to the particular bit, disables the corresponding algorithm.
23 - 16	ALGO2	RW	A98AC7h	This register is used to indicate the algorithm(s) to be used for the memory self-test routine. Each bit corresponds to a specific algorithm.Writing a value 1 to the particular bit, enables the corresponding algorithm.Writing a value 0 to the particular bit, disables the corresponding algorithm.
15 - 8	ALGO1	RW	A98AC7h	This register is used to indicate the algorithm(s) to be used for the memory self-test routine. Each bit corresponds to a specific algorithm.Writing a value 1 to the particular bit, enables the corresponding algorithm.Writing a value 0 to the particular bit, disables the corresponding algorithm.
7 - 0	ALGO0	RW	A98AC7h	This register is used to indicate the algorithm(s) to be used for the memory self-test routine. Each bit corresponds to a specific algorithm.Writing a value 1 to the particular bit, enables the corresponding algorithm.Writing a value 0 to the particular bit, disables the corresponding algorithm.

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4.7.22 TOP_PBIST_CI3 Registers

4.7.22.1 PBIST_CI3 Register (Offset = 15Ch) [reset = h]

Short Description: Constant Increment Register3

Long Description:

Return to Summary Table

Table 4-716. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 015Ch

Access Types Legend

Table 4-717. PBIST_CI3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RINFOL3	RW	A98AC7h	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
23 - 16	RINFOL2	RW	A98AC7h	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
15 - 8	RINFOL1	RW	A98AC7h	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
7 - 0	RINFOL0	RW	A98AC7h	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.

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4.7.23 TOP_PBIST_RAMT Registers

4.7.23.1 PBIST_RAMT Register (Offset = 160h) [reset = h]

Short Description: RAM Configuration (RAMT -RAM)

Long Description:

Return to Summary Table

Table 4-718. Instance Table

Instance Name	Physical Address
TOP_PBIST	5330 0160h

Access Types Legend

Table 4-719. PBIST_RAMT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RINFOU3	RW	A98AC7h	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
23 - 16	RINFOU2	RW	A98AC7h	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
15 - 8	RINFOU1	RW	A98AC7h	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.
7 - 0	RINFOU0	RW	A98AC7h	This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithmto be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group.

4.7.24 Access Table

Table 4-720. Access Type Codes

Access Type	Code	Description
RW	RW	Read / Write
RO	RO	Read

4.8 STC Registers

Table 4-721. R5SS[0:1]_STC Registers Base Address Table

Offset	Length	Acronym	R5SS0_STC Physical Address	R5SS1_STC Physical Address
0h	32	SCT_STCGCR0	5350 0000h	5351 0000h
4h	32	SCT_STCGCR1	5350 0004h	5351 0004h
8h	32	SCT_STCTPR	5350 0008h	5351 0008h
Ch	32	SCT_STC_CADDR	5350 000Ch	5351 000Ch
10h	32	SCT_STCCICR	5350 0010h	5351 0010h
14h	32	SCT_STCGSTAT	5350 0014h	5351 0014h

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Table 4-721. R5SS[0:1]_STC Registers Base Address Table (continued)

Offset	Length	Acronym	R5SS0_STC Physical Address	R5SS1_STC Physical Address
18h	32	SCT_STCFSTAT	5350 0018h	5351 0018h
1Ch	32	SCT_STCSCSCR	5350 001Ch	5351 001Ch
20h	32	SCT_STC_CADDR2	5350 0020h	5351 0020h
24h	32	SCT_STC_CLKDIV	5350 0024h	5351 0024h
28h	32	SCT_STC_SEGPLR	5350 0028h	5351 0028h
2Ch	32	SCT_SEG0_START_ADDR	5350 002Ch	5351 002Ch
30h	32	SCT_SEG1_START_ADDR	5350 0030h	5351 0030h
34h	32	SCT_SEG2_START_ADDR	5350 0034h	5351 0034h
38h	32	SCT_SEG3_START_ADDR	5350 0038h	5351 0038h
3Ch	32	SCT_CORE1_CURMISR_0	5350 003Ch	5351 003Ch
40h	32	SCT_CORE1_CURMISR_1	5350 0040h	5351 0040h
44h	32	SCT_CORE1_CURMISR_2	5350 0044h	5351 0044h
48h	32	SCT_CORE1_CURMISR_3	5350 0048h	5351 0048h
4Ch	32	SCT_CORE1_CURMISR_4	5350 004Ch	5351 004Ch
50h	32	SCT_CORE1_CURMISR_5	5350 0050h	5351 0050h
54h	32	SCT_CORE1_CURMISR_6	5350 0054h	5351 0054h
58h	32	SCT_CORE1_CURMISR_7	5350 0058h	5351 0058h
5Ch	32	SCT_CORE1_CURMISR_8	5350 005Ch	5351 005Ch
60h	32	SCT_CORE1_CURMISR_9	5350 0060h	5351 0060h
64h	32	SCT_CORE1_CURMISR_10	5350 0064h	5351 0064h
68h	32	SCT_CORE1_CURMISR_11	5350 0068h	5351 0068h
6Ch	32	SCT_CORE1_CURMISR_12	5350 006Ch	5351 006Ch
70h	32	SCT_CORE1_CURMISR_13	5350 0070h	5351 0070h
74h	32	SCT_CORE1_CURMISR_14	5350 0074h	5351 0074h
78h	32	SCT_CORE1_CURMISR_15	5350 0078h	5351 0078h
7Ch	32	SCT_CORE1_CURMISR_16	5350 007Ch	5351 007Ch
80h	32	SCT_CORE1_CURMISR_17	5350 0080h	5351 0080h
84h	32	SCT_CORE1_CURMISR_18	5350 0084h	5351 0084h
88h	32	SCT_CORE1_CURMISR_19	5350 0088h	5351 0088h
8Ch	32	SCT_CORE1_CURMISR_20	5350 008Ch	5351 008Ch
90h	32	SCT_CORE1_CURMISR_21	5350 0090h	5351 0090h
94h	32	SCT_CORE1_CURMISR_22	5350 0094h	5351 0094h
98h	32	SCT_CORE1_CURMISR_23	5350 0098h	5351 0098h
9Ch	32	SCT_CORE1_CURMISR_24	5350 009Ch	5351 009Ch
A0h	32	SCT_CORE1_CURMISR_25	5350 00A0h	5351 00A0h
A4h	32	SCT_CORE1_CURMISR_26	5350 00A4h	5351 00A4h
A8h	32	SCT_CORE1_CURMISR_27	5350 00A8h	5351 00A8h
ACh	32	SCT_CORE2_CURMISR_0	5350 00ACh	5351 00ACh
B0h	32	SCT_CORE2_CURMISR_1	5350 00B0h	5351 00B0h
B4h	32	SCT_CORE2_CURMISR_2	5350 00B4h	5351 00B4h
B8h	32	SCT_CORE2_CURMISR_3	5350 00B8h	5351 00B8h
BCh	32	SCT_CORE2_CURMISR_4	5350 00BCh	5351 00BCh
C0h	32	SCT_CORE2_CURMISR_5	5350 00C0h	5351 00C0h
C4h	32	SCT_CORE2_CURMISR_6	5350 00C4h	5351 00C4h
C8h	32	SCT_CORE2_CURMISR_7	5350 00C8h	5351 00C8h
CCh	32	SCT_CORE2_CURMISR_8	5350 00CCh	5351 00CCh
D0h	32	SCT_CORE2_CURMISR_9	5350 00D0h	5351 00D0h

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Table 4-721. R5SS[0:1]_STC Registers Base Address Table (continued)

Offset	Length	Acronym	R5SS0_STC Physical Address	R5SS1_STC Physical Address
D4h	32	SCT_CORE2_CURMISR_10	5350 00D4h	5351 00D4h
D8h	32	SCT_CORE2_CURMISR_11	5350 00D8h	5351 00D8h
DCh	32	SCT_CORE2_CURMISR_12	5350 00DCh	5351 00DCh
E0h	32	SCT_CORE2_CURMISR_13	5350 00E0h	5351 00E0h
E4h	32	SCT_CORE2_CURMISR_14	5350 00E4h	5351 00E4h
E8h	32	SCT_CORE2_CURMISR_15	5350 00E8h	5351 00E8h
ECh	32	SCT_CORE2_CURMISR_16	5350 00ECh	5351 00ECh
F0h	32	SCT_CORE2_CURMISR_17	5350 00F0h	5351 00F0h
F4h	32	SCT_CORE2_CURMISR_18	5350 00F4h	5351 00F4h
F8h	32	SCT_CORE2_CURMISR_19	5350 00F8h	5351 00F8h
FCh	32	SCT_CORE2_CURMISR_20	5350 00FCh	5351 00FCh
100h	32	SCT_CORE2_CURMISR_21	5350 0100h	5351 0100h
104h	32	SCT_CORE2_CURMISR_22	5350 0104h	5351 0104h
108h	32	SCT_CORE2_CURMISR_23	5350 0108h	5351 0108h
10Ch	32	SCT_CORE2_CURMISR_24	5350 010Ch	5351 010Ch
110h	32	SCT_CORE2_CURMISR_25	5350 0110h	5351 0110h
114h	32	SCT_CORE2_CURMISR_26	5350 0114h	5351 0114h
118h	32	SCT_CORE2_CURMISR_27	5350 0118h	5351 0118h

4.8.1 SCT Instance Count Note

Note

n = 0 to 1 for the SCT registers defined below.

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4.8.2 R5SSn_STC_STCGCR0 Registers

4.8.2.1 R5SS0_STCGCR0 Register (Offset = 0h) [reset = h]

Short Description: Self test Global control Reg0. *NOT BYTE ACCESSIBLE

Long Description:

Return to Summary Table

Table 4-722. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0000h
R5SS1_STC	5351 0000h

Access Types Legend

Table 4-723. STCGCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	INTCOUNT_B16	RW	1h	Number of intervals of the self test run (RWP - Read, Priviledge Mode Write only)Count of intervals that need to be covered for a specific selftest run.The selftest controller sends out ?complete? indication once it runs all of the intervals programmed in this field.INTCOUNT_B16=0 is an invalid configuration for a selftest.
15 - 11	NU0	RO	0h	Reserved bits
10 - 8	CAP_IDLE_CYCLE	RW	1h	Idle cycles before and after capture clock (RWP - Read, Priviledge Mode Write only)Idle Cycles before and after capture clock. This value is used to insert that many idle cycles in the Capture phase. Programmable idle cycles allow implementation flexibility on SCAN_EN signal at chip level based on the size of the UUT and timing requirements.
7 - 5	SCANEN_HIGH_CAP_IDLE_CYCLE	RW	1h	Idle cycles before and after capture clock (RWP - Read, Priviledge Mode Write only). *NOT BYTE ACCESSIBLEIdle Cycles between scan_en going high to func_clk_en generation and scan_en going high to misr_log_en generation. This value is used to insert that many idle cycles in the shift clock (scan_en going high to func_clk_en generation) and misr_log_clk (scan_en going high to misr_log_en generation) generation. Programmable idle cycles allow implementation flexibility on SCAN_EN signal at chip level based on the size of the UUT and timing requirements.
4 - 2	NU1	RO	0h	Reserved bits
1 - 0	RS_CNT_B1	RW	0h	Restart/Continue or preload (RWP - Read, Priviledge Mode Write only)This bit specifies the selftest controller whether to continue the run from next interval onwards, restart from ROM address 0 or preload from a prescribed interval. This bit gets reset after the completion of selftest run.00 = Continue NSTC run from previous interval01 = Restart NSTC run from ROM address 01X = Start from segment number specified in STC_SEGPLR register

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4.8.3 R5SSn_STC_STCGCR1 Registers

4.8.3.1 R5SS0_STCGCR1 Register (Offset = 4h) [reset = h]

Short Description: Self test Global control Reg1

Long Description:

Return to Summary Table

Table 4-724. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0004h
R5SS1_STC	5351 0004h

Access Types Legend

Table 4-725. STCGCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 12	NU2	RO	0h	Reserved bits
11 - 8	SEG0_CORE_SEL	RW	0h	Selects the Segment0 CORE for self test (RWP - Read, Priviledge Mode Write only)Select the Segment0 CORE for Self -Test0001 = Select CORE for selftestOther = CORE not selected.
7	NU3	RO	0h	Reserved bits
6	CODEC_SPREAD_MODE	RW	0h	Codec Spread Mode control signal (RWP - Read, Priviledge Mode Write only)This bit is used to configure the codec in spread / X-OR mode.1 = Spread mode0 = XOR mode
5	LP_SCAN_MODE	RW	1h	LP scan mode (RWP - Read, Priviledge Mode Write only)This bit is used to decide the scan configuration:1 = Operates in Low Power Scan Mode. 0 = Operates in Normal Scan Mode.
4	ROM_ACCESS_INV	RW	0h	Rom access inversion mode (RWP - Read, Priviledge Mode Write only)- NOT SUPPORTED
3 - 0	ST_ENA_B4	RW	65h	Self test enable key (RWP - Read, Priviledge Mode Write only)1010 = Self test run enabled All values other than 1010 = Self test run disabled

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4.8.4 R5SSn_STC_STCTPR Registers

4.8.4.1 R5SS0_STCTPR Register (Offset = 8h) [reset = h]

Short Description: Time out counter preload register

Long Description:

Return to Summary Table

Table 4-726. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0008h
R5SS1_STC	5351 0008h

Access Types Legend

Table 4-727. STCTPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TO_PRELOAD	RW	8C3DEFB1 EDB984FE2 AC71C71C7 h	Self test time out preload (RWP - Read, Priviledge Mode Write only)This register contains the total number of STC clock cycles it will take before a self-test timeout error will be triggered after the initiation of the self-test run. This is a fail safe feature to avoid system hang-up situation on account of any run away self test issues. This register should be loaded with a meaningful count value for this feature to be effective.This register value (preload count value) gets loaded into the self test timeout down counter whenever a self test run is initiated (ST_ENA is enabled). and gets disabled on completion of a self test run.

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4.8.5 R5SSn_STC_STC_CADDR Registers

4.8.5.1 R5SS0_STC_CADDR Register (Offset = Ch) [reset = h]

Short Description: Current Address register for CORE1

Long Description:

Return to Summary Table

Table 4-728. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 000Ch
R5SS1_STC	5351 000Ch

Access Types Legend

Table 4-729. STC_CADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ADDR	RO	0h	Current ROM Address for CORE1This register reflects the current ROM address (for micro code load) accessed during selftest for CORE1 in of case segment0 and all the remaining segmentsn where n = 1 to 3).

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4.8.6 R5SSn_STC_STCCICR Registers

4.8.6.1 R5SS0_STCCICR Register (Offset = 10h) [reset = h]

Short Description: Current Interval count register

Long Description:

Return to Summary Table

Table 4-730. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0010h
R5SS1_STC	5351 0010h

Access Types Legend

Table 4-731. STCCICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CORE2_ICOUNT	RO	0h	Specifies the last interval number for CORE2This specifies the Last executed Interval number for CORE2 of Segment0 if self test is being executed for secondary core as well. This field is applicable only for Segment 0.
15 - 0	CORE1_ICOUNT	RO	0h	Specifies the last interval number for CORE1This specifies the Last executed Interval number of a self-test run.

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4.8.7 R5SSn_STC_STCGSTAT Registers

4.8.7.1 R5SS0_STCGSTAT Register (Offset = 14h) [reset = h]

Short Description: Global Status Register

Long Description:

Return to Summary Table

Table 4-732. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0014h
R5SS1_STC	5351 0014h

Access Types Legend

Table 4-733. STCGSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 12	NU4	RO	0h	Reserved bits
11 - 8	ST_ACTIVE	RO	65h	Tells whether self test is currently active or not.1010 = Self test is activeOthers = SelfTest is not activeOnce the self-test completes and ST_ENA_B4 key is cleared, this field will reflect the inactive value.
7 - 2	NU5	RO	0h	Reserved bits
1	TEST_FAIL	RO	0h	Test_fail flag (RCP - Read, Clear on Writing in Priviledge Mode)0 = Self test run has not failed1 = SelfTest run has failed. Write Clear.
0	TEST_DONE	RO	0h	Test_done_flag (RCP - Read, Clear on Writing in Priviledge Mode)0 = Not completed1 = SelfTest run Completed

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4.8.8 R5SSn_STC_STCFSTAT Registers

4.8.8.1 R5SS0_STCFSTAT Register (Offset = 18h) [reset = h]

Short Description: Fail Status Register

Long Description:

Return to Summary Table

Table 4-734. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0018h
R5SS1_STC	5351 0018h

Access Types Legend

Table 4-735. STCFSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 5	NU6	RO	0h	Reserved bits
4 - 3	FSEG_ID	RO	0h	Failed Segment ID (RCP - Read, Clear on Writing in Priviledge Mode)This field captures the Segment number for which any of the failures like TO_ER_B1, CPU1_FAIL_B1 and CPU2_FAIL_B1 occur.00 = Failure on Segment 001 = Failure on Segment 110 = Failure on Segment 211 = Failure on Segment 3
2	TO_ER_B1	RO	0h	Tells whether self test failed because of time out error (RCP - Read, Clear on Writing in Priviledge Mode)0 = No time out error occurred1 = SelfTest run failed due to a timeout error
1	CPU2_FAIL_B1	RO	0h	Tells whether MISR mismatch happenned in CORE2 when in Segment0 mode (RCP - Read, Clear on Writing in Priviledge Mode)0 = No MISR mismatch for CORE21 = Self test run failed due to MISR mismatch for CORE2
0	CPU1_FAIL_B1	RO	0h	Tells whether MISR mismatch happenned in CORE1 (RCP - Read, Clear on Writing in Priviledge Mode)Applicable to all segments.0 = No MISR mismatch for CORE11 = Self test run failed due to MISR mismatch for CORE1

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4.8.9 R5SSn_STC_STCSCSCR Registers

4.8.9.1 R5SS0_STCSCSCR Register (Offset = 1Ch) [reset = h]

Short Description: Signature compare Self Check Register

Long Description:

Return to Summary Table

Table 4-736. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 001Ch
R5SS1_STC	5351 001Ch

Access Types Legend

Table 4-737. STCSCSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 5	NU7	RO	0h	Reserved bits
4	FAULT_INS_B1	RW	0h	Fault Insertion bit (RWP - Read, Priviledge Mode Write only)0 = No fault insertion.1 = Inserts fault in the logic unedr test which will make signature compare fail. This feature is used as diagnostic check of the STC IP.
3 - 0	SELF_CHECK_KEY_B4	RW	65h	Signature compare logic self check key enable/disable (RWP - Read, Priviledge Mode Write only)1010 = Signature compare logic Self Check is enabledAll values other than 1010 = Signature compare logic Self Check is disabled

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4.8.10 R5SSn_STC_STC_CADDR2 Registers

4.8.10.1 R5SS0_STC_CADDR2 Register (Offset = 20h) [reset = h]

Short Description: Current Address register for CORE2

Long Description:

Return to Summary Table

Table 4-738. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0020h
R5SS1_STC	5351 0020h

Access Types Legend

Table 4-739. STC_CADDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ADDR	RO	0h	Current ROM Address for CORE2This register reflects the current ROM address(for micro code load) accessed during selftest for CORE2 in of case segment0.

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4.8.11 R5SSn_STC_STC_CLKDIV Registers

4.8.11.1 R5SS0_STC_CLKDIV Register (Offset = 24h) [reset = h]

Short Description: Clock Divider Register

Long Description:

Return to Summary Table

Table 4-740. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0024h
R5SS1_STC	5351 0024h

Access Types Legend

Table 4-741. STC_CLKDIV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 27	NU8	RO	0h	Reserved bits
26 - 24	CLKDIV0	RW	0h	Clock division for Seg0 (RWP - Read, Priviledge Mode Write only)*NOT SUPPORTEDX = Division ratio is X+1 for Segment 0
23 - 19	NU9	RO	0h	Reserved bits
18 - 16	CLKDIV1	RW	0h	Clock division for Seg1 (RWP - Read, Priviledge Mode Write only)*NOT SUPPORTEDX = Division ratio is X+1 for Segment 1
15 - 11	NU10	RO	0h	Reserved bits
10 - 8	CLKDIV2	RW	0h	Clock division for Seg2 (RWP - Read, Priviledge Mode Write only)*NOT SUPPORTEDX = Division ratio is X+1 for Segment 2
7 - 3	NU11	RO	0h	Reserved bits
2 - 0	CLKDIV3	RW	0h	Clock division for Seg3 (RWP - Read, Priviledge Mode Write only)*NOT SUPPORTEDX = Division ratio is X+1 for Segment 3

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4.8.12 R5SSn_STC_STC_SEGPLR Registers

4.8.12.1 R5SS0_STC_SEGPLR Register (Offset = 28h) [reset = h]

Short Description: Segment 1st interval Preload Register

Long Description:

Return to Summary Table

Table 4-742. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0028h
R5SS1_STC	5351 0028h

Access Types Legend

Table 4-743. STC_SEGPLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU12	RO	0h	Reserved bits
1 - 0	SEGID_PLOAD	RW	0h	Segment number for which preload is to be started (RWP - Read, Priviledge Mode Write only)This specifies the segment for which the address of its First interval will be pre-loaded into the NSTC ROM address counter. The 1st address of each segment are defined in SEGx_START_ADDR register.The address of the 1st interval of the selected segment is loaded into the NSTC ROM address counter when the RS_CNT_B1 bits of STC_GCR0 are set to 1X00 = Preload the address of the 1st interval of segment 0.01 = Preload the address of the 1st interval of segment 1.10 = Preload the address of the 1st interval of segment 2.11 = Preload the address of the 1st interval of segment 3.

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4.8.13 R5SSn_STC_SEG0_START_ADDR Registers

4.8.13.1 R5SSn_STC_SEG0_START_ADDR Register (Offset = 2Ch) [reset = h]

Short Description: ROM Start address for Segment0

Long Description:

Return to Summary Table

Table 4-744. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 002Ch
R5SS1_STC	5351 002Ch

Access Types Legend

Table 4-745. SEG0_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU13	RO	0h	Reserved bits
19 - 0	SEG_START_ADDR	RW	0h	Segment 0 Start Address (RWP - Read, Priviledge Mode Write only)This register holds the ROM address for the start of first interval of the segment.When STC_GCR0.RS_CNT_B1 field is set to (1x) ? PRELOAD? option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register.Valid number of bits depends on RTL paramerter ADDR

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4.8.14 R5SSn_STC_SEG1_START_ADDR Registers

4.8.14.1 R5SSn_STC_SEG1_START_ADDR Register (Offset = 30h) [reset = h]

Short Description: ROM Start address for Segment1

Long Description:

Return to Summary Table

Table 4-746. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0030h
R5SS1_STC	5351 0030h

Access Types Legend

Table 4-747. SEG1_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU14	RO	0h	Reserved bits
19 - 0	SEG_START_ADDR	RW	0h	Segment 1 Start Address (RWP - Read, Priviledge Mode Write only)This register holds the ROM address for the start of first interval of the segment.When STC_GCR0.RS_CNT_B1 field is set to (1x) ? PRELOAD? option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register.Valid number of bits depends on RTL paramerter ADDR.This register is present only when RTL parameter NUM_SEG = 1.

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4.8.15 R5SSn_STC_SEG2_START_ADDR Registers

4.8.15.1 R5SSn_STC_SEG2_START_ADDR Register (Offset = 34h) [reset = h]

Short Description: ROM Start address for Segment2

Long Description:

Return to Summary Table

Table 4-748. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0034h
R5SS1_STC	5351 0034h

Access Types Legend

Table 4-749. SEG2_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU15	RO	0h	Reserved bits
19 - 0	SEG_START_ADDR	RW	0h	Segment 2 Start Address (RWP - Read, Priviledge Mode Write only)This register holds the ROM address for the start of first interval of the segment.When STC_GCR0.RS_CNT_B1 field is set to (1x) ? PRELOAD? option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register.Valid number of bits depends on RTL paramerter ADDR.This register is present only when RTL parameter NUM_SEG = 2.

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4.8.16 R5SSn_STC_SEG3_START_ADDR Registers

4.8.16.1 R5SSn_STC_SEG3_START_ADDR Register (Offset = 38h) [reset = h]

Short Description: ROM Start address for Segment3

Long Description:

Return to Summary Table

Table 4-750. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0038h
R5SS1_STC	5351 0038h

Access Types Legend

Table 4-751. SEG3_START_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU16	RO	0h	Reserved bits
19 - 0	SEG_START_ADDR	RW	0h	Segment 3 Start Address (RWP - Read, Priviledge Mode Write only)This register holds the ROM address for the start of first interval of the segment.When STC_GCR0.RS_CNT_B1 field is set to (1x) ? PRELOAD? option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register.Valid number of bits depends on RTL paramerter ADDR.This register is present only when RTL parameter NUM_SEG = 3.

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4.8.17 R5SSn_STC_CORE1_CURMISR_0 Registers

4.8.17.1 R5SSn_STC_CORE1_CURMISR_0 Register (Offset = 3Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-752. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 003Ch
R5SS1_STC	5351 003Ch

Access Types Legend

Table 4-753. CORE1_CURMISR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR0	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.18 R5SSn_STC_CORE1_CURMISR_1 Registers

4.8.18.1 R5SSn_STC_CORE1_CURMISR_1 Register (Offset = 40h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-754. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0040h
R5SS1_STC	5351 0040h

Access Types Legend

Table 4-755. CORE1_CURMISR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR1	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.19 R5SSn_STC_CORE1_CURMISR_2 Registers

4.8.19.1 R5SSn_STC_CORE1_CURMISR_2 Register (Offset = 44h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-756. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0044h
R5SS1_STC	5351 0044h

Access Types Legend

Table 4-757. CORE1_CURMISR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR2	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.20 R5SSn_STC_CORE1_CURMISR_3 Registers

4.8.20.1 R5SSn_STC_CORE1_CURMISR_3 Register (Offset = 48h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-758. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0048h
R5SS1_STC	5351 0048h

Access Types Legend

Table 4-759. CORE1_CURMISR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR3	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.21 R5SSn_STC_CORE1_CURMISR_4 Registers

4.8.21.1 R5SSn_STC_CORE1_CURMISR_4 Register (Offset = 4Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-760. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 004Ch
R5SS1_STC	5351 004Ch

Access Types Legend

Table 4-761. CORE1_CURMISR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR4	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.22 R5SSn_STC_CORE1_CURMISR_5 Registers

4.8.22.1 R5SSn_STC_CORE1_CURMISR_5 Register (Offset = 50h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-762. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0050h
R5SS1_STC	5351 0050h

Access Types Legend

Table 4-763. CORE1_CURMISR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR5	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.23 R5SSn_STC_CORE1_CURMISR_6 Registers

4.8.23.1 R5SSn_STC_CORE1_CURMISR_6 Register (Offset = 54h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-764. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0054h
R5SS1_STC	5351 0054h

Access Types Legend

Table 4-765. CORE1_CURMISR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR6	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.24 R5SSn_STC_CORE1_CURMISR_7 Registers

4.8.24.1 R5SSn_STC_CORE1_CURMISR_7 Register (Offset = 58h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-766. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0058h
R5SS1_STC	5351 0058h

Access Types Legend

Table 4-767. CORE1_CURMISR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR7	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.25 R5SSn_STC_CORE1_CURMISR_8 Registers

4.8.25.1 R5SSn_STC_CORE1_CURMISR_8 Register (Offset = 5Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-768. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 005Ch
R5SS1_STC	5351 005Ch

Access Types Legend

Table 4-769. CORE1_CURMISR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR8	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.26 R5SSn_STC_CORE1_CURMISR_9 Registers

4.8.26.1 R5SSn_STC_CORE1_CURMISR_9 Register (Offset = 60h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-770. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0060h
R5SS1_STC	5351 0060h

Access Types Legend

Table 4-771. CORE1_CURMISR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR9	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.27 R5SSn_STC_CORE1_CURMISR_10 Registers

4.8.27.1 R5SSn_STC_CORE1_CURMISR_10 Register (Offset = 64h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-772. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0064h
R5SS1_STC	5351 0064h

Access Types Legend

Table 4-773. CORE1_CURMISR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR10	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.28 R5SSn_STC_CORE1_CURMISR_11 Registers

4.8.28.1 R5SSn_STC_CORE1_CURMISR_11 Register (Offset = 68h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-774. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0068h
R5SS1_STC	5351 0068h

Access Types Legend

Table 4-775. CORE1_CURMISR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR11	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.29 R5SSn_STC_CORE1_CURMISR_12 Registers

4.8.29.1 R5SSn_STC_CORE1_CURMISR_12 Register (Offset = 6Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-776. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 006Ch
R5SS1_STC	5351 006Ch

Access Types Legend

Table 4-777. CORE1_CURMISR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR12	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.30 R5SSn_STC_CORE1_CURMISR_13 Registers

4.8.30.1 R5SSn_STC_CORE1_CURMISR_13 Register (Offset = 70h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-778. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0070h
R5SS1_STC	5351 0070h

Access Types Legend

Table 4-779. CORE1_CURMISR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR13	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.31 R5SSn_STC_CORE1_CURMISR_14 Registers

4.8.31.1 R5SSn_STC_CORE1_CURMISR_14 Register (Offset = 74h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-780. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0074h
R5SS1_STC	5351 0074h

Access Types Legend

Table 4-781. CORE1_CURMISR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR14	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.32 R5SSn_STC_CORE1_CURMISR_15 Registers

4.8.32.1 R5SSn_STC_CORE1_CURMISR_15 Register (Offset = 78h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-782. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0078h
R5SS1_STC	5351 0078h

Access Types Legend

Table 4-783. CORE1_CURMISR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR15	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.33 R5SSn_STC_CORE1_CURMISR_16 Registers

4.8.33.1 R5SSn_STC_CORE1_CURMISR_16 Register (Offset = 7Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-784. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 007Ch
R5SS1_STC	5351 007Ch

Access Types Legend

Table 4-785. CORE1_CURMISR_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR16	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.34 R5SSn_STC_CORE1_CURMISR_17 Registers

4.8.34.1 R5SSn_STC_CORE1_CURMISR_17 Register (Offset = 80h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-786. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0080h
R5SS1_STC	5351 0080h

Access Types Legend

Table 4-787. CORE1_CURMISR_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR17	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.35 R5SSn_STC_CORE1_CURMISR_18 Registers

4.8.35.1 R5SSn_STC_CORE1_CURMISR_18 Register (Offset = 84h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-788. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0084h
R5SS1_STC	5351 0084h

Access Types Legend

Table 4-789. CORE1_CURMISR_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR18	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.36 R5SSn_STC_CORE1_CURMISR_19 Registers

4.8.36.1 R5SSn_STC_CORE1_CURMISR_19 Register (Offset = 88h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-790. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0088h
R5SS1_STC	5351 0088h

Access Types Legend

Table 4-791. CORE1_CURMISR_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR19	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.37 R5SSn_STC_CORE1_CURMISR_20 Registers

4.8.37.1 R5SSn_STC_CORE1_CURMISR_20 Register (Offset = 8Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-792. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 008Ch
R5SS1_STC	5351 008Ch

Access Types Legend

Table 4-793. CORE1_CURMISR_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR20	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.38 R5SSn_STC_CORE1_CURMISR_21 Registers

4.8.38.1 R5SSn_STC_CORE1_CURMISR_21 Register (Offset = 90h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-794. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0090h
R5SS1_STC	5351 0090h

Access Types Legend

Table 4-795. CORE1_CURMISR_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR21	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.39 R5SSn_STC_CORE1_CURMISR_22 Registers

4.8.39.1 R5SSn_STC_CORE1_CURMISR_22 Register (Offset = 94h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-796. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0094h
R5SS1_STC	5351 0094h

Access Types Legend

Table 4-797. CORE1_CURMISR_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR22	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.40 R5SSn_STC_CORE1_CURMISR_23 Registers

4.8.40.1 R5SSn_STC_CORE1_CURMISR_23 Register (Offset = 98h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-798. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0098h
R5SS1_STC	5351 0098h

Access Types Legend

Table 4-799. CORE1_CURMISR_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR23	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.41 R5SSn_STC_CORE1_CURMISR_24 Registers

4.8.41.1 R5SSn_STC_CORE1_CURMISR_24 Register (Offset = 9Ch) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-800. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 009Ch
R5SS1_STC	5351 009Ch

Access Types Legend

Table 4-801. CORE1_CURMISR_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR24	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.42 R5SSn_STC_CORE1_CURMISR_25 Registers

4.8.42.1 R5SSn_STC_CORE1_CURMISR_25 Register (Offset = A0h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-802. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00A0h
R5SS1_STC	5351 00A0h

Access Types Legend

Table 4-803. CORE1_CURMISR_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR25	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.43 R5SSn_STC_CORE1_CURMISR_26 Registers

4.8.43.1 R5SSn_STC_CORE1_CURMISR_26 Register (Offset = A4h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-804. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00A4h
R5SS1_STC	5351 00A4h

Access Types Legend

Table 4-805. CORE1_CURMISR_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR26	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.44 R5SSn_STC_CORE1_CURMISR_27 Registers

4.8.44.1 R5SSn_STC_CORE1_CURMISR_27 Register (Offset = A8h) [reset = h]

Short Description: Holds the MISR signature for CORE1

Long Description:

Return to Summary Table

Table 4-806. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00A8h
R5SS1_STC	5351 00A8h

Access Types Legend

Table 4-807. CORE1_CURMISR_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C1MISR27	RO	0h	MISR Signature for CORE1This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.45 R5SSn_STC_CORE2_CURMISR_0 Registers

4.8.45.1 R5SSn_STC_CORE2_CURMISR_0 Register (Offset = ACh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-808. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00ACh
R5SS1_STC	5351 00ACh

Access Types Legend

Table 4-809. CORE2_CURMISR_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR0	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.46 R5SSn_STC_CORE2_CURMISR_1 Registers

4.8.46.1 R5SSn_STC_CORE2_CURMISR_1 Register (Offset = B0h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-810. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00B0h
R5SS1_STC	5351 00B0h

Access Types Legend

Table 4-811. CORE2_CURMISR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR1	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.47 R5SSn_STC_CORE2_CURMISR_2 Registers

4.8.47.1 R5SSn_STC_CORE2_CURMISR_2 Register (Offset = B4h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-812. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00B4h
R5SS1_STC	5351 00B4h

Access Types Legend

Table 4-813. CORE2_CURMISR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR2	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.48 R5SSn_STC_CORE2_CURMISR_3 Registers

4.8.48.1 R5SSn_STC_CORE2_CURMISR_3 Register (Offset = B8h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-814. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00B8h
R5SS1_STC	5351 00B8h

Access Types Legend

Table 4-815. CORE2_CURMISR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR3	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.49 R5SSn_STC_CORE2_CURMISR_4 Registers

4.8.49.1 R5SSn_STC_CORE2_CURMISR_4 Register (Offset = BCh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-816. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00BCh
R5SS1_STC	5351 00BCh

Access Types Legend

Table 4-817. CORE2_CURMISR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR4	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.50 R5SSn_STC_CORE2_CURMISR_5 Registers

4.8.50.1 R5SSn_STC_CORE2_CURMISR_5 Register (Offset = C0h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-818. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00C0h
R5SS1_STC	5351 00C0h

Access Types Legend

Table 4-819. CORE2_CURMISR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR5	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.51 R5SSn_STC_CORE2_CURMISR_6 Registers

4.8.51.1 R5SSn_STC_CORE2_CURMISR_6 Register (Offset = C4h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-820. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00C4h
R5SS1_STC	5351 00C4h

Access Types Legend

Table 4-821. CORE2_CURMISR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR6	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.52 R5SSn_STC_CORE2_CURMISR_7 Registers

4.8.52.1 R5SSn_STC_CORE2_CURMISR_7 Register (Offset = C8h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-822. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00C8h
R5SS1_STC	5351 00C8h

Access Types Legend

Table 4-823. CORE2_CURMISR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR7	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.53 R5SSn_STC_CORE2_CURMISR_8 Registers

4.8.53.1 R5SSn_STC_CORE2_CURMISR_8 Register (Offset = CCh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-824. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00CCh
R5SS1_STC	5351 00CCh

Access Types Legend

Table 4-825. CORE2_CURMISR_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR8	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.54 R5SSn_STC_CORE2_CURMISR_9 Registers

4.8.54.1 R5SSn_STC_CORE2_CURMISR_9 Register (Offset = D0h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-826. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00D0h
R5SS1_STC	5351 00D0h

Access Types Legend

Table 4-827. CORE2_CURMISR_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR9	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.55 R5SSn_STC_CORE2_CURMISR_10 Registers

4.8.55.1 R5SSn_STC_CORE2_CURMISR_10 Register (Offset = D4h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-828. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00D4h
R5SS1_STC	5351 00D4h

Access Types Legend

Table 4-829. CORE2_CURMISR_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR10	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.56 R5SSn_STC_CORE2_CURMISR_11 Registers

4.8.56.1 R5SSn_STC_CORE2_CURMISR_11 Register (Offset = D8h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-830. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00D8h
R5SS1_STC	5351 00D8h

Access Types Legend

Table 4-831. CORE2_CURMISR_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR11	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.57 R5SSn_STC_CORE2_CURMISR_12 Registers

4.8.57.1 R5SSn_STC_CORE2_CURMISR_12 Register (Offset = DCh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-832. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00DCh
R5SS1_STC	5351 00DCh

Access Types Legend

Table 4-833. CORE2_CURMISR_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR12	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.58 R5SSn_STC_CORE2_CURMISR_13 Registers

4.8.58.1 R5SSn_STC_CORE2_CURMISR_13 Register (Offset = E0h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-834. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00E0h
R5SS1_STC	5351 00E0h

Access Types Legend

Table 4-835. CORE2_CURMISR_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR13	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.59 R5SSn_STC_CORE2_CURMISR_14 Registers

4.8.59.1 R5SSn_STC_CORE2_CURMISR_14 Register (Offset = E4h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-836. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00E4h
R5SS1_STC	5351 00E4h

Access Types Legend

Table 4-837. CORE2_CURMISR_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR14	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.60 R5SSn_STC_CORE2_CURMISR_15 Registers

4.8.60.1 R5SSn_STC_CORE2_CURMISR_15 Register (Offset = E8h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-838. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00E8h
R5SS1_STC	5351 00E8h

Access Types Legend

Table 4-839. CORE2_CURMISR_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR15	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.61 R5SSn_STC_CORE2_CURMISR_16 Registers

4.8.61.1 R5SSn_STC_CORE2_CURMISR_16 Register (Offset = ECh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-840. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00ECh
R5SS1_STC	5351 00ECh

Access Types Legend

Table 4-841. CORE2_CURMISR_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR16	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.62 R5SSn_STC_CORE2_CURMISR_17 Registers

4.8.62.1 R5SSn_STC_CORE2_CURMISR_17 Register (Offset = F0h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-842. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00F0h
R5SS1_STC	5351 00F0h

Access Types Legend

Table 4-843. CORE2_CURMISR_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR17	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.63 R5SSn_STC_CORE2_CURMISR_18 Registers

4.8.63.1 R5SSn_STC_CORE2_CURMISR_18 Register (Offset = F4h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-844. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00F4h
R5SS1_STC	5351 00F4h

Access Types Legend

Table 4-845. CORE2_CURMISR_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR18	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.64 R5SSn_STC_CORE2_CURMISR_19 Registers

4.8.64.1 R5SSn_STC_CORE2_CURMISR_19 Register (Offset = F8h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-846. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00F8h
R5SS1_STC	5351 00F8h

Access Types Legend

Table 4-847. CORE2_CURMISR_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR19	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.65 R5SSn_STC_CORE2_CURMISR_20 Registers

4.8.65.1 R5SSn_STC_CORE2_CURMISR_20 Register (Offset = FCh) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-848. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 00FCh
R5SS1_STC	5351 00FCh

Access Types Legend

Table 4-849. CORE2_CURMISR_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR20	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.66 R5SSn_STC_CORE2_CURMISR_21 Registers

4.8.66.1 R5SSn_STC_CORE2_CURMISR_21 Register (Offset = 100h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-850. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0100h
R5SS1_STC	5351 0100h

Access Types Legend

Table 4-851. CORE2_CURMISR_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR21	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.67 R5SSn_STC_CORE2_CURMISR_22 Registers

4.8.67.1 R5SSn_STC_CORE2_CURMISR_22 Register (Offset = 104h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-852. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0104h
R5SS1_STC	5351 0104h

Access Types Legend

Table 4-853. CORE2_CURMISR_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR22	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.68 R5SSn_STC_CORE2_CURMISR_23 Registers

4.8.68.1 R5SSn_STC_CORE2_CURMISR_23 Register (Offset = 108h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-854. Instance Table

R5SS0_STC	5350 0108h
R5SS1_STC	5351 0108h

Access Types Legend

Table 4-855. CORE2_CURMISR_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR23	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.69 R5SSn_STC_CORE2_CURMISR_24 Registers

4.8.69.1 R5SSn_STC_CORE2_CURMISR_24 Register (Offset = 10Ch) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-856. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 010Ch
R5SS1_STC	5351 010Ch

Access Types Legend

Table 4-857. CORE2_CURMISR_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR24	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.70 R5SSn_STC_CORE2_CURMISR_25 Registers

4.8.70.1 R5SSn_STC_CORE2_CURMISR_25 Register (Offset = 110h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-858. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0110h
R5SS1_STC	5351 0110h

Access Types Legend

Table 4-859. CORE2_CURMISR_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR25	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.71 R5SSn_STC_CORE2_CURMISR_26 Registers

4.8.71.1 R5SSn_STC_CORE2_CURMISR_26 Register (Offset = 114h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-860. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0114h
R5SS1_STC	5351 0114h

Access Types Legend

Table 4-861. CORE2_CURMISR_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR26	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

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4.8.72 R5SSn_STC_CORE2_CURMISR_27 Registers

4.8.72.1 R5SSn_STC_CORE2_CURMISR_27 Register (Offset = 118h) [reset = h]

Short Description: Holds the MISR signature for CORE2

Long Description:

Return to Summary Table

Table 4-862. Instance Table

Instance Name	Physical Address
R5SS0_STC	5350 0118h
R5SS1_STC	5351 0118h

Access Types Legend

Table 4-863. CORE2_CURMISR_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	C2MISR27	RO	0h	MISR Signature for CORE2This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed.

4.8.73 Access Table

Table 4-864. Access Type Codes

Access Type	Code	Description
RW	RW	Read / Write
RO	RO	Read

4.9 CPSW Registers

Table 4-865. MSS_CPSW Registers Base Address Table

Offset	Length	Acronym	MSS_CPSW Physical Address
0h	32	CPSW_CPSW_NUSS_IDVER_REG	5280 0000h
4h	32	CPSW_SS_SYNCE_COUNT_REG	5280 0004h
8h	8	CPSW_SS_SYNCE_MUX_REG	5280 0008h
Ch	8	CPSW_SS_CONTROL_REG	5280 000Ch
18h	32	CPSW_SS_INT_CONTROL_REG	5280 0018h
1Ch	0	CPSW_SS_STATUS_REG	5280 001Ch
20h	32	CPSW_SUBSYSTEM_CONFIG_REG	5280 0020h
30h	8	CPSW_RGMII1_STATUS_REG	5280 0030h
34h	8	CPSW_RGMII2_STATUS_REG	5280 0034h

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4.9.1 MSS_CPSW_CPSW_NUSS_IDVER_REG Registers

4.9.1.1 CPSW_NUSS_IDVER_REG Register (Offset = 0h) [reset = h]

Short Description: ID Version Register

Long Description:

Return to Summary Table

Table 4-866. Instance Table

Instance Name	Physical Address
CPSW	5280 0000h

Access Types Legend

Table 4-867. CPSW_NUSS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	IDENT	RO	6422E98E9020h	Identification value
15 - 11	RTL_VER	RO	Bh	RTL version value
10 - 8	MAJOR_VER	RO	1h	Major version value
7 - 0	MINOR_VER	RO	Bh	Minor version value

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4.9.2 MSS_CPSW_SS_SYNCE_COUNT_REG Registers

4.9.2.1 CPSW_SYNCE_COUNT_REG Register (Offset = 4h) [reset = h]

Short Description: SS SYNCE Count Register

Long Description:

Return to Summary Table

Table 4-868. Instance Table

Instance Name	Physical Address
CPSW	5280 0004h

Access Types Legend

Table 4-869. SS_SYNCE_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SYNCE_CNT	RW	0h	Sync E Count Value

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4.9.3 MSS_CPSW_SS_SYNCE_MUX_REG Registers

4.9.3.1 CPSW_SYNCE_MUX_REG Register (Offset = 8h) [reset = h]

Short Description: SS Synce Mux Register

Long Description:

Return to Summary Table

Table 4-870. Instance Table

Instance Name	Physical Address
CPSW	5280 0008h

Access Types Legend

Table 4-871. SS_SYNCE_MUX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
5 - 0	SYNCE_SEL	RW	0h	Sync E Select Value

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4.9.4 MSS_CPSW_SS_CONTROL_REG Registers

4.9.4.1 CPSW_CONTROL_REG Register (Offset = Ch) [reset = h]

Short Description: SS Control Register

Long Description:

Return to Summary Table

Table 4-872. Instance Table

Instance Name	Physical Address
CPSW	5280 000Ch

Access Types Legend

Table 4-873. SS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	EEE_PHY_ONLY	RW	0h	Energy Efficient Enable Phy Only Mode: 0=The low power indicate state includes gating off the CPPI_GCLK to the CPSW, 1=The low power indicate state does not gate the clock to the CPSW
0	EEE_EN	RW	0h	Energy Efficient Ethernet Enable: 0=EEE is disabled, 1=EEE is enabled

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4.9.5 MSS_CPSW_SS_INT_CONTROL_REG Registers

4.9.5.1 CPSW_INT_CONTROL_REG Register (Offset = 18h) [reset = h]

Short Description: SS Interrupt Control Register

Long Description:

Return to Summary Table

Table 4-874. Instance Table

Instance Name	Physical Address
CPSW	5280 0018h

Access Types Legend

Table 4-875. SS_INT_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INT_TEST	RW	0h	Interrupt Test
30	INT_SEL_VEC_EN	RW	0h	Interrupt Sel Vector Enable
	RESERVED	NONE		Reserved
21 - 16	INT_BYPASS	RW	0h	Interrupt Bypass Value
	RESERVED	NONE		Reserved
11 - 0	INT_PRESCALE	RW	0h	Interrupt Prescale Value

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4.9.6 MSS_CPSW_SS_STATUS_REG Registers

4.9.6.1 CPSW_STATUS_REG Register (Offset = 1Ch) [reset = h]

Short Description: SS Status Register

Long Description:

Return to Summary Table

Table 4-876. Instance Table

Instance Name	Physical Address
CPSW	5280 001Ch

Access Types Legend

Table 4-877. SS_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EEE_CLKSTOP_ACK	RO	0h	Energy Efficient Ethernet clockstop acknowledge from CPSW

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4.9.7 MSS_CPSW_SUBSYSTEM_CONFIG_REG Registers

4.9.7.1 CPSW_CONFIG_REG Register (Offset = 20h) [reset = h]

Short Description: Subsystem Configuration Register

Long Description:

Return to Summary Table

Table 4-878. Instance Table

Instance Name	Physical Address
CPSW	5280 0020h

Access Types Legend

Table 4-879. SUBSYSTEM_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27 - 20	XGMII	RO	0h	The Number of XGMII Ports included in the CPSW_NUSS
19	QSGMII	RO	0h	QSGMII is included in the CPSW_NUSS
18	SGMII	RO	0h	SGMII is included in the CPSW_NUSS
17	RGMII	RO	1h	RGMII is included in the CPSW_NUSS
16	RMII	RO	1h	RMII is included in the CPSW_NUSS
	RESERVED	NONE		Reserved
12 - 8	NUM_GENF	RO	Ah	The number of CPTS GENF outputs
7 - 0	NUM_PORTS	RO	Bh	The total number of ports including the host port 0

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4.9.8 MSS_CPSW_RGMII1_STATUS_REG Registers

4.9.8.1 CPSW_STATUS_REG Register (Offset = 30h) [reset = h]

Short Description: RGMII1 Status Register

Long Description:

Return to Summary Table

Table 4-880. Instance Table

Instance Name	Physical Address
CPSW	5280 0030h

Access Types Legend

Table 4-881. RGMII1_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	FULLDUPLEX	RO	0h	Rgmii1 full dulex: 0=Half-duplex, 1=Full-duplex
2 - 1	SPEED	RO	0h	Rgmii1 speed: 00=10Mbps, 01=100Mbps, 10=1000Mbps, 11=reserved
0	LINK	RO	0h	Rgmii1 link indicator: 0=Link is down, 1=Link is up

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4.9.9 MSS_CPSW_RGMII2_STATUS_REG Registers

4.9.9.1 CPSW_STATUS_REG Register (Offset = 34h) [reset = h]

Short Description: RGMII2 Status Register

Long Description:

Return to Summary Table

Table 4-882. Instance Table

Instance Name	Physical Address
CPSW	5280 0034h

Access Types Legend

Table 4-883. RGMII2_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	FULLDUPLEX	RO	0h	Rgmii2 full dulex: 0=Half-duplex, 1=Full-duplex
2 - 1	SPEED	RO	0h	Rgmii2 speed: 00=10Mbps, 01=100Mbps, 10=1000Mbps, 11=reserved
0	LINK	RO	0h	Rgmii2 link indicator: 0=Link is down, 1=Link is up

4.9.10 Access Table

Table 4-884. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
WO	WO	Write

4.10 CPSW_SS_SS Registers

Table 4-885. MSS_CPSW_SS_SS Registers Base Address Table

Offset	Length	Acronym	MSS_CPSW_SS_SS Physical Address
0h	32	CPSW_SS_SGMII_IDVER_REG	5280 0000h
0h	32	CPSW_SS_MDIO_VERSION_REG	5280 0000h
0h	32	CPSW_SS_REVISION	5280 0000h
0h	32	CPSW_SS_ID_VER_REG	5280 0000h
0h	32	CPSW_SS_USER_ACCESS_REG	5280 0000h
0h	32	CPSW_SS_PN_RESERVED_REG	5280 0000h
0h	32	CPSW_SS_PN_RESERVED_REG	5280 0000h
0h	32	CPSW_SS_FETCH_LOC	5280 0000h
0h	32	CPSW_SS_RXGOODFRAMES	5280 0000h
0h	32	CPSW_SS_IDVER_REG	5280 0000h
0h	32	CPSW_SS_MOD_VER	5280 0000h
0h	32	CPSW_SS_COMP_LOW_REG	5280 0000h
0h	32	CPSW_SS_COMP_LOW_REG	5280 0000h
4h	32	CPSW_SS_SOFT_RESET_REG	5280 0004h
4h	32	CPSW_SS_CONTROL_REG	5280 0004h
4h	32	CPSW_SS_CONTROL_REG	5280 0004h
4h	32	CPSW_SS_USER_PHY_SEL_REG	5280 0004h
4h	32	CPSW_SS_P0_CONTROL_REG	5280 0004h

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Table 4-885. MSS_CPSW_SS_SS Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_CPSW_SS_SS Physical Address
4h	32	CPSW_SS_PN_CONTROL_REG	5280 0004h
4h	32	CPSW_SS_PN_CONTROL_REG	5280 0004h
4h	32	CPSW_SS_RXBROADCASTFRAMES	5280 0004h
4h	32	CPSW_SS_CONTROL_REG	5280 0004h
4h	32	CPSW_SS_ALE_STATUS	5280 0004h
4h	32	CPSW_SS_COMP_HIGH_REG	5280 0004h
4h	32	CPSW_SS_COMP_HIGH_REG	5280 0004h
8h	32	CPSW_SS_ALIVE_REG	5280 0008h
8h	32	CPSW_SS_P0_FLOW_ID_OFFSET_REG	5280 0008h
8h	32	CPSW_SS_PN_MAX_BLKS_REG	5280 0008h
8h	32	CPSW_SS_PN_MAX_BLKS_REG	5280 0008h
8h	32	CPSW_SS_RXMULTICASTFRAMES	5280 0008h
8h	32	CPSW_SS_RFTCLK_SEL_REG	5280 0008h
8h	32	CPSW_SS_ALE_CONTROL	5280 0008h
8h	32	CPSW_SS_CONTROL_REG	5280 0008h
8h	32	CPSW_SS_CONTROL_REG	5280 0008h
Ch	32	CPSW_SS_LINK_REG	5280 000Ch
Ch	32	CPSW_SS_RXPAUSEFRAMES	5280 000Ch
Ch	32	CPSW_SS_TS_PUSH_REG	5280 000Ch
Ch	32	CPSW_SS_ALE_CTRL2	5280 000Ch
Ch	32	CPSW_SS_LENGTH_REG	5280 000Ch
Ch	32	CPSW_SS_LENGTH_REG	5280 000Ch
10h	32	CPSW_SS_CONTROL_REG	5280 0010h
10h	32	CPSW_SS_LINK_INT_RAW_REG	5280 0010h
10h	32	CPSW_SS_eoi_reg	5280 0010h
10h	32	CPSW_SS_EM_CONTROL_REG	5280 0010h
10h	32	CPSW_SS_P0_BLK_CNT_REG	5280 0010h
10h	32	CPSW_SS_PN_BLK_CNT_REG	5280 0010h
10h	32	CPSW_SS_PN_BLK_CNT_REG	5280 0010h
10h	32	CPSW_SS_RXCRCERRORS	5280 0010h
10h	32	CPSW_SS_TS_LOAD_VAL_REG	5280 0010h
10h	32	CPSW_SS_ALE_PRESCALE	5280 0010h
10h	32	CPSW_SS_PPM_LOW_REG	5280 0010h
10h	32	CPSW_SS_PPM_LOW_REG	5280 0010h
14h	32	CPSW_SS_STATUS_REG	5280 0014h
14h	32	CPSW_SS_LINK_INT_MASKED_REG	5280 0014h
14h	32	CPSW_SS_intr_vector_reg	5280 0014h
14h	32	CPSW_SS_STAT_PORT_EN_REG	5280 0014h
14h	32	CPSW_SS_P0_PORT_VLAN_REG	5280 0014h
14h	32	CPSW_SS_PN_PORT_VLAN_REG	5280 0014h
14h	32	CPSW_SS_PN_PORT_VLAN_REG	5280 0014h
14h	32	CPSW_SS_RXALIGNCODEERRORS	5280 0014h
14h	32	CPSW_SS_TS_LOAD_EN_REG	5280 0014h
14h	32	CPSW_SS_ALE_AGING_CTRL	5280 0014h
14h	32	CPSW_SS_PPM_HIGH_REG	5280 0014h
14h	32	CPSW_SS_PPM_HIGH_REG	5280 0014h
18h	32	CPSW_SS_MR_ADV_ABILITY_REG	5280 0018h

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Table 4-885. MSS_CPSW_SS_SS Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_CPSW_SS_SS Physical Address
18h	32	CPSW_SS_LINK_INT_MASK_SET_REG	5280 0018h
18h	32	CPSW_SS_PTYPE_REG	5280 0018h
18h	32	CPSW_SS_P0_TX_PRI_MAP_REG	5280 0018h
18h	32	CPSW_SS_PN_TX_PRI_MAP_REG	5280 0018h
18h	32	CPSW_SS_PN_TX_PRI_MAP_REG	5280 0018h
18h	32	CPSW_SS_RXOVERSIZEDFRAMES	5280 0018h
18h	32	CPSW_SS_TS_COMP_VAL_REG	5280 0018h
18h	32	CPSW_SS_NUDGE_REG	5280 0018h
18h	32	CPSW_SS_NUDGE_REG	5280 0018h
1Ch	32	CPSW_SS_MR_NP_TX_REG	5280 001Ch
1Ch	32	CPSW_SS_LINK_INT_MASK_CLEAR_REG	5280 001Ch
1Ch	32	CPSW_SS_SOFT_IDLE_REG	5280 001Ch
1Ch	32	CPSW_SS_P0_PRI_CTL_REG	5280 001Ch
1Ch	32	CPSW_SS_PN_PRI_CTL_REG	5280 001Ch
1Ch	32	CPSW_SS_PN_PRI_CTL_REG	5280 001Ch
1Ch	32	CPSW_SS_RXJABBERFRAMES	5280 001Ch
1Ch	32	CPSW_SS_TS_COMP_LEN_REG	5280 001Ch
1Ch	32	CPSW_SS_ALE_NXT_HDR	5280 001Ch
20h	32	CPSW_SS_MR_LP_ADV_ABILITY_REG	5280 0020h
20h	32	CPSW_SS_USER_INT_RAW_REG	5280 0020h
20h	32	CPSW_SS_THRU_RATE_REG	5280 0020h
20h	32	CPSW_SS_P0_RX_PRI_MAP_REG	5280 0020h
20h	32	CPSW_SS_PN_RX_PRI_MAP_REG	5280 0020h
20h	32	CPSW_SS_PN_RX_PRI_MAP_REG	5280 0020h
20h	32	CPSW_SS_RXUNDERSIZEDFRAMES	5280 0020h
20h	32	CPSW_SS_INTSTAT_RAW_REG	5280 0020h
20h	32	CPSW_SS_ALE_TBLCTL	5280 0020h
24h	32	CPSW_SS_MR_LP_NP_RX_REG	5280 0024h
24h	32	CPSW_SS_USER_INT_MASKED_REG	5280 0024h
24h	32	CPSW_SS_GAP_THRESH_REG	5280 0024h
24h	32	CPSW_SS_P0_RX_MAXLEN_REG	5280 0024h
24h	32	CPSW_SS_PN_RX_MAXLEN_REG	5280 0024h
24h	32	CPSW_SS_PN_RX_MAXLEN_REG	5280 0024h
24h	32	CPSW_SS_RXFRAGMENTS	5280 0024h
24h	32	CPSW_SS_INTSTAT_MASKED_REG	5280 0024h
28h	32	CPSW_SS_USER_INT_MASK_SET_REG	5280 0028h
28h	32	CPSW_SS_P0_TX_BLKS_PRI_REG	5280 0028h
28h	32	CPSW_SS_PN_TX_BLKS_PRI_REG	5280 0028h
28h	32	CPSW_SS_PN_TX_BLKS_PRI_REG	5280 0028h
28h	32	CPSW_SS_ALE_DROP	5280 0028h
28h	32	CPSW_SS_INT_ENABLE_REG	5280 0028h
2Ch	32	CPSW_SS_USER_INT_MASK_CLEAR_REG	5280 002Ch
2Ch	32	CPSW_SS_EEE_PRESCALE_REG	5280 002Ch
2Ch	32	CPSW_SS_ALE_OVERRUN_DROP	5280 002Ch
2Ch	32	CPSW_SS_TS_COMP_NUDGE_REG	5280 002Ch
30h	32	CPSW_SS_TX_CFG_REG	5280 0030h
30h	32	CPSW_SS_MANUAL_IF_REG	5280 0030h

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Table 4-885. MSS_CPSW_SS_SS Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_CPSW_SS_SS Physical Address
30h	32	CPSW_SS_TX_G_OFLOW_THRESH_SET_REG	5280 0030h
30h	32	CPSW_SS_P0_IDLE2LPI_REG	5280 0030h
30h	32	CPSW_SS_PN_IDLE2LPI_REG	5280 0030h
30h	32	CPSW_SS_PN_IDLE2LPI_REG	5280 0030h
30h	32	CPSW_SS_RXOCTETS	5280 0030h
30h	32	CPSW_SS_EVENT_POP_REG	5280 0030h
34h	32	CPSW_SS_RX_CFG_REG	5280 0034h
34h	32	CPSW_SS_POLL_REG	5280 0034h
34h	32	CPSW_SS_TX_G_OFLOW_THRESH_CLR_REG	5280 0034h
34h	32	CPSW_SS_P0_LPI2WAKE_REG	5280 0034h
34h	32	CPSW_SS_PN_LPI2WAKE_REG	5280 0034h
34h	32	CPSW_SS_PN_LPI2WAKE_REG	5280 0034h
34h	32	CPSW_SS_TXGOODFRAMES	5280 0034h
34h	32	CPSW_SS_EVENT_0_REG	5280 0034h
34h	32	CPSW_SS_ALE_TBLW2	5280 0034h
38h	32	CPSW_SS_AUX_CFG_REG	5280 0038h
38h	32	CPSW_SS_POLL_EN_REG	5280 0038h
38h	32	CPSW_SS_TX_G_BUF_THRESH_SET_L_REG	5280 0038h
38h	32	CPSW_SS_P0_EEE_STATUS_REG	5280 0038h
38h	32	CPSW_SS_PN_EEE_STATUS_REG	5280 0038h
38h	32	CPSW_SS_PN_EEE_STATUS_REG	5280 0038h
38h	32	CPSW_SS_TXBROADCASTFRAMES	5280 0038h
38h	32	CPSW_SS_EVENT_1_REG	5280 0038h
38h	32	CPSW_SS_ALE_TBLW1	5280 0038h
3Ch	32	CPSW_SS_CLAUS45_REG	5280 003Ch
3Ch	32	CPSW_SS_TX_G_BUF_THRESH_SET_H_REG	5280 003Ch
3Ch	32	CPSW_SS_TXMULTICASTFRAMES	5280 003Ch
3Ch	32	CPSW_SS_EVENT_2_REG	5280 003Ch
3Ch	32	CPSW_SS_ALE_TBLW0	5280 003Ch
40h	32	CPSW_SS_DIAG_CLEAR_REG	5280 0040h
40h	32	CPSW_SS_USER_ADDR0_REG	5280 0040h
40h	32	CPSW_SS_TX_G_BUF_THRESH_CLR_L_REG	5280 0040h
40h	32	CPSW_SS_PN_IET_CONTROL_REG	5280 0040h
40h	32	CPSW_SS_PN_IET_CONTROL_REG	5280 0040h
40h	32	CPSW_SS_TXPAUSEFRAMES	5280 0040h
40h	32	CPSW_SS_EVENT_3_REG	5280 0040h
40h	32	CPSW_SS_I0_ALE_PORTCTL0	5280 0040h
44h	32	CPSW_SS_DIAG_CONTROL_REG	5280 0044h
44h	32	CPSW_SS_USER_ADDR1_REG	5280 0044h
44h	32	CPSW_SS_TX_G_BUF_THRESH_CLR_H_REG	5280 0044h
44h	32	CPSW_SS_PN_IET_STATUS_REG	5280 0044h
44h	32	CPSW_SS_PN_IET_STATUS_REG	5280 0044h
44h	32	CPSW_SS_TXDEFERREDFRAMES	5280 0044h
44h	32	CPSW_SS_TS_LOAD_HIGH_VAL_REG	5280 0044h
48h	32	CPSW_SS_DIAG_STATUS_REG	5280 0048h
48h	32	CPSW_SS_PN_IET_VERIFY_REG	5280 0048h
48h	32	CPSW_SS_PN_IET_VERIFY_REG	5280 0048h

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Table 4-885. MSS_CPSW_SS_SS Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_CPSW_SS_SS Physical Address
48h	32	CPSW_SS_TXCOLLISIONFRAMES	5280 0048h
48h	32	CPSW_SS_TS_COMP_HIGH_VAL_REG	5280 0048h
4Ch	32	CPSW_SS_TXSINGLECOLLFRAMES	5280 004Ch
4Ch	32	CPSW_SS_TS_ADD_VAL_REG	5280 004Ch
50h	32	CPSW_SS_VLAN_LTYPE_REG	5280 0050h
50h	32	CPSW_SS_P0_FIFO_STATUS_REG	5280 0050h
50h	32	CPSW_SS_PN_FIFO_STATUS_REG	5280 0050h
50h	32	CPSW_SS_PN_FIFO_STATUS_REG	5280 0050h
50h	32	CPSW_SS_TXMULTCOLLFRAMES	5280 0050h
50h	32	CPSW_SS_TS_PPM_LOW_VAL_REG	5280 0050h
54h	32	CPSW_SS_EST_TS_DOMAIN_REG	5280 0054h
54h	32	CPSW_SS_TXEXCESSIVECOLLISIONS	5280 0054h
54h	32	CPSW_SS_TS_PPM_HIGH_VAL_REG	5280 0054h
58h	32	CPSW_SS_CUT_THRESHOLD_REG	5280 0058h
58h	32	CPSW_SS_TXLATECOLLISIONS	5280 0058h
58h	32	CPSW_SS_TS_NUDGE_VAL_REG	5280 0058h
5Ch	32	CPSW_SS_FREQUENCY_REG	5280 005Ch
5Ch	32	CPSW_SS_RXIPGERROR	5280 005Ch
60h	32	CPSW_SS_IET_HOLD_CNT_LD_VAL_REG	5280 0060h
60h	32	CPSW_SS_PN_EST_CONTROL_REG	5280 0060h
60h	32	CPSW_SS_PN_EST_CONTROL_REG	5280 0060h
60h	32	CPSW_SS_TXCARRIERSENSEERRORS	5280 0060h
64h	32	CPSW_SS_TXOCTETS	5280 0064h
68h	32	CPSW_SS_OCTETFRAMES64	5280 0068h
6Ch	32	CPSW_SS_OCTETFRAMES65T127	5280 006Ch
70h	32	CPSW_SS_OCTETFRAMES128T255	5280 0070h
74h	32	CPSW_SS_OCTETFRAMES256T511	5280 0074h
78h	32	CPSW_SS_OCTETFRAMES512T1023	5280 0078h
7Ch	32	CPSW_SS_OCTETFRAMES1024TUP	5280 007Ch
80h	32	CPSW_SS_NETOCTETS	5280 0080h
84h	32	CPSW_SS_RX_BOTTOM_OF_FIFO_DROP	5280 0084h
88h	32	CPSW_SS_PORTMASK_DROP	5280 0088h
8Ch	32	CPSW_SS_RX_TOP_OF_FIFO_DROP	5280 008Ch
90h	32	CPSW_SS_ALE_RATE_LIMIT_DROP	5280 0090h
90h	32	CPSW_SS_ALE_UVLAN_MEMBER	5280 0090h
94h	32	CPSW_SS_ALE_VID_INGRESS_DROP	5280 0094h
94h	32	CPSW_SS_ALE_UVLAN_URCAST	5280 0094h
98h	32	CPSW_SS_ALE_DA_EQ_SA_DROP	5280 0098h
98h	32	CPSW_SS_ALE_UVLAN_RMCAST	5280 0098h
9Ch	32	CPSW_SS_ALE_BLOCK_DROP	5280 009Ch
9Ch	32	CPSW_SS_ALE_UVLAN_UNTAG	5280 009Ch
A0h	32	CPSW_SS_ALE_SECURE_DROP	5280 00A0h
A4h	32	CPSW_SS_ALE_AUTH_DROP	5280 00A4h
A8h	32	CPSW_SS_ALE_UNKN_UNI	5280 00A8h
ACh	32	CPSW_SS_ALE_UNKN_UNI_BCNT	5280 00ACh
B0h	32	CPSW_SS_ALE_UNKN_MLT	5280 00B0h
B4h	32	CPSW_SS_ALE_UNKN_MLT_BCNT	5280 00B4h

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Table 4-885. MSS_CPSW_SS_SS Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_CPSW_SS_SS Physical Address
B8h	32	CPSW_SS_ALE_UNKN_BRD	5280 00B8h
B8h	32	CPSW_SS_ALE_STAT_DIAG	5280 00B8h
BCh	32	CPSW_SS_ALE_UNKN_BRD_BCNT	5280 00BCh
BCh	32	CPSW_SS_ALE_OAM_LB_CTRL	5280 00BCh
C0h	32	CPSW_SS_ALE_POL_MATCH	5280 00C0h
C4h	32	CPSW_SS_ALE_POL_MATCH_RED	5280 00C4h
C8h	32	CPSW_SS_ALE_POL_MATCH_YELLOW	5280 00C8h
CCh	32	CPSW_SS_ALE_MULT_SA_DROP	5280 00CCh
D0h	32	CPSW_SS_ALE_DUAL_VLAN_DROP	5280 00D0h
D0h	32	CPSW_SS_TS_CONFIG	5280 00D0h
D4h	32	CPSW_SS_ALE_LEN_ERROR_DROP	5280 00D4h
D8h	32	CPSW_SS_ALE_IP_NEXT_HDR_DROP	5280 00D8h
DCh	32	CPSW_SS_ALE_IPV4_FRAG_DROP	5280 00DCh
FCh	32	CPSW_SS_EGRESSOP	5280 00FCh
100h	32	CPSW_SS_enable_reg_out_pulse_0	5280 0100h
100h	32	CPSW_SS_TX_PRI0_MAXLEN_REG	5280 0100h
100h	32	CPSW_SS_POLICECFG0	5280 0100h
104h	32	CPSW_SS_TX_PRI1_MAXLEN_REG	5280 0104h
104h	32	CPSW_SS_POLICECFG1	5280 0104h
108h	32	CPSW_SS_TX_PRI2_MAXLEN_REG	5280 0108h
108h	32	CPSW_SS_POLICECFG2	5280 0108h
10Ch	32	CPSW_SS_TX_PRI3_MAXLEN_REG	5280 010Ch
10Ch	32	CPSW_SS_POLICECFG3	5280 010Ch
110h	32	CPSW_SS_TX_PRI4_MAXLEN_REG	5280 0110h
110h	32	CPSW_SS_POLICECFG4	5280 0110h
114h	32	CPSW_SS_TX_PRI5_MAXLEN_REG	5280 0114h
118h	32	CPSW_SS_TX_PRI6_MAXLEN_REG	5280 0118h
118h	32	CPSW_SS_POLICECFG6	5280 0118h
11Ch	32	CPSW_SS_TX_PRI7_MAXLEN_REG	5280 011Ch
11Ch	32	CPSW_SS_POLICECFG7	5280 011Ch
120h	32	CPSW_SS_P0_RX_DSCP_MAP_REG	5280 0120h
120h	32	CPSW_SS_PN_RX_DSCP_MAP_REG	5280 0120h
120h	32	CPSW_SS_PN_RX_DSCP_MAP_REG	5280 0120h
120h	32	CPSW_SS_POLICETBLCTL	5280 0120h
124h	32	CPSW_SS_POLICECONTROL	5280 0124h
128h	32	CPSW_SS_POLICETESTCTL	5280 0128h
12Ch	32	CPSW_SS_POLICEHSTAT	5280 012Ch
134h	32	CPSW_SS_THREADMAPDEF	5280 0134h
138h	32	CPSW_SS_THREADMAPCTL	5280 0138h
13Ch	32	CPSW_SS_THREADMAPVAL	5280 013Ch
140h	32	CPSW_SS_P0_PRI_CIR_REG	5280 0140h
140h	32	CPSW_SS_PN_PRI_CIR_REG	5280 0140h
140h	32	CPSW_SS_PN_PRI_CIR_REG	5280 0140h
140h	32	CPSW_SS_IET_RX_ASSEMBLY_ERROR_REG	5280 0140h
144h	32	CPSW_SS_IET_RX_ASSEMBLY_OK_REG	5280 0144h
148h	32	CPSW_SS_IET_RX_SMD_ERROR_REG	5280 0148h
14Ch	32	CPSW_SS_IET_RX_FRAG_REG	5280 014Ch

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Table 4-885. MSS_CPSW_SS_SS Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_CPSW_SS_SS Physical Address
150h	32	CPSW_SS_IET_TX_HOLD_REG	5280 0150h
154h	32	CPSW_SS_IET_TX_FRAG_REG	5280 0154h
160h	32	CPSW_SS_P0_PRI_EIR_REG	5280 0160h
160h	32	CPSW_SS_PN_PRI_EIR_REG	5280 0160h
160h	32	CPSW_SS_PN_PRI_EIR_REG	5280 0160h
17Ch	32	CPSW_SS_TX_MEMORY_PROTECT_ERROR	5280 017Ch
180h	32	CPSW_SS_P0_TX_D_THRESH_SET_L_REG	5280 0180h
180h	32	CPSW_SS_PN_TX_D_THRESH_SET_L_REG	5280 0180h
180h	32	CPSW_SS_PN_TX_D_THRESH_SET_L_REG	5280 0180h
180h	32	CPSW_SS_ENET_PN_TX_PRI_REG	5280 0180h
184h	32	CPSW_SS_P0_TX_D_THRESH_SET_H_REG	5280 0184h
184h	32	CPSW_SS_PN_TX_D_THRESH_SET_H_REG	5280 0184h
184h	32	CPSW_SS_PN_TX_D_THRESH_SET_H_REG	5280 0184h
188h	32	CPSW_SS_P0_TX_D_THRESH_CLR_L_REG	5280 0188h
188h	32	CPSW_SS_PN_TX_D_THRESH_CLR_L_REG	5280 0188h
188h	32	CPSW_SS_PN_TX_D_THRESH_CLR_L_REG	5280 0188h
18Ch	32	CPSW_SS_P0_TX_D_THRESH_CLR_H_REG	5280 018Ch
18Ch	32	CPSW_SS_PN_TX_D_THRESH_CLR_H_REG	5280 018Ch
18Ch	32	CPSW_SS_PN_TX_D_THRESH_CLR_H_REG	5280 018Ch
190h	32	CPSW_SS_P0_TX_G_BUF_THRESH_SET_L_REG	5280 0190h
190h	32	CPSW_SS_PN_TX_G_BUF_THRESH_SET_L_REG	5280 0190h
190h	32	CPSW_SS_PN_TX_G_BUF_THRESH_SET_L_REG	5280 0190h
194h	32	CPSW_SS_P0_TX_G_BUF_THRESH_SET_H_REG	5280 0194h
194h	32	CPSW_SS_PN_TX_G_BUF_THRESH_SET_H_REG	5280 0194h
194h	32	CPSW_SS_PN_TX_G_BUF_THRESH_SET_H_REG	5280 0194h
198h	32	CPSW_SS_P0_TX_G_BUF_THRESH_CLR_L_REG	5280 0198h
198h	32	CPSW_SS_PN_TX_G_BUF_THRESH_CLR_L_REG	5280 0198h
198h	32	CPSW_SS_PN_TX_G_BUF_THRESH_CLR_L_REG	5280 0198h
19Ch	32	CPSW_SS_P0_TX_G_BUF_THRESH_CLR_H_REG	5280 019Ch
19Ch	32	CPSW_SS_PN_TX_G_BUF_THRESH_CLR_H_REG	5280 019Ch
19Ch	32	CPSW_SS_PN_TX_G_BUF_THRESH_CLR_H_REG	5280 019Ch
1A0h	32	CPSW_SS_ENET_PN_TX_PRI_BCNT_REG	5280 01A0h
1C0h	32	CPSW_SS_ENET_PN_TX_PRI_DROP_REG	5280 01C0h
1E0h	32	CPSW_SS_ENET_PN_TX_PRI_DROP_BCNT_REG	5280 01E0h
300h	32	CPSW_SS_enable_clr_reg_out_pulse_0	5280 0300h
300h	32	CPSW_SS_P0_SRC_ID_A_REG	5280 0300h
300h	32	CPSW_SS_PN_TX_D_OFLOW_ADDVAL_L_REG	5280 0300h
300h	32	CPSW_SS_PN_TX_D_OFLOW_ADDVAL_L_REG	5280 0300h
304h	32	CPSW_SS_P0_SRC_ID_B_REG	5280 0304h
304h	32	CPSW_SS_PN_TX_D_OFLOW_ADDVAL_H_REG	5280 0304h
304h	32	CPSW_SS_PN_TX_D_OFLOW_ADDVAL_H_REG	5280 0304h
308h	32	CPSW_SS_PN_SA_L_REG	5280 0308h
308h	32	CPSW_SS_PN_SA_L_REG	5280 0308h
30Ch	32	CPSW_SS_PN_SA_H_REG	5280 030Ch
30Ch	32	CPSW_SS_PN_SA_H_REG	5280 030Ch
310h	32	CPSW_SS_PN_TS_CTL_REG	5280 0310h
310h	32	CPSW_SS_PN_TS_CTL_REG	5280 0310h

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Table 4-885. MSS_CPSW_SS_SS Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_CPSW_SS_SS Physical Address
314h	32	CPSW_SS_PN_TS_SEQ_LTYPE_REG	5280 0314h
314h	32	CPSW_SS_PN_TS_SEQ_LTYPE_REG	5280 0314h
318h	32	CPSW_SS_PN_TS_VLAN_LTYPE_REG	5280 0318h
318h	32	CPSW_SS_PN_TS_VLAN_LTYPE_REG	5280 0318h
31Ch	32	CPSW_SS_PN_TS_CTL_LTYPE2_REG	5280 031Ch
31Ch	32	CPSW_SS_PN_TS_CTL_LTYPE2_REG	5280 031Ch
320h	32	CPSW_SS_P0_HOST_BLKS_PRI_REG	5280 0320h
320h	32	CPSW_SS_PN_TS_CTL2_REG	5280 0320h
320h	32	CPSW_SS_PN_TS_CTL2_REG	5280 0320h
330h	32	CPSW_SS_PN_MAC_CONTROL_REG	5280 0330h
330h	32	CPSW_SS_PN_MAC_CONTROL_REG	5280 0330h
334h	32	CPSW_SS_PN_MAC_STATUS_REG	5280 0334h
334h	32	CPSW_SS_PN_MAC_STATUS_REG	5280 0334h
338h	32	CPSW_SS_PN_MAC_SOFT_RESET_REG	5280 0338h
338h	32	CPSW_SS_PN_MAC_SOFT_RESET_REG	5280 0338h
33Ch	32	CPSW_SS_PN_MAC_BOFFTEST_REG	5280 033Ch
33Ch	32	CPSW_SS_PN_MAC_BOFFTEST_REG	5280 033Ch
340h	32	CPSW_SS_PN_MAC_RX_PAUSETIMER_REG	5280 0340h
340h	32	CPSW_SS_PN_MAC_RX_PAUSETIMER_REG	5280 0340h
350h	32	CPSW_SS_PN_MAC_RXN_PAUSETIMER_REG	5280 0350h
350h	32	CPSW_SS_PN_MAC_RXN_PAUSETIMER_REG	5280 0350h
370h	32	CPSW_SS_PN_MAC_TX_PAUSETIMER_REG	5280 0370h
370h	32	CPSW_SS_PN_MAC_TX_PAUSETIMER_REG	5280 0370h
380h	32	CPSW_SS_PN_MAC_TXN_PAUSETIMER_REG	5280 0380h
380h	32	CPSW_SS_PN_MAC_TXN_PAUSETIMER_REG	5280 0380h
3A0h	32	CPSW_SS_PN_MAC_EMCONTROL_REG	5280 03A0h
3A0h	32	CPSW_SS_PN_MAC_EMCONTROL_REG	5280 03A0h
3A4h	32	CPSW_SS_PN_MAC_TX_GAP_REG	5280 03A4h
3A4h	32	CPSW_SS_PN_MAC_TX_GAP_REG	5280 03A4h
3A8h	32	CPSW_SS_PN_MAC_PORT_CONFIG	5280 03A8h
3A8h	32	CPSW_SS_PN_MAC_PORT_CONFIG	5280 03A8h
3ACh	32	CPSW_SS_PN_INTERVLAN_OPX_POINTER_REG	5280 03ACh
3ACh	32	CPSW_SS_PN_INTERVLAN_OPX_POINTER_REG	5280 03ACh
3B0h	32	CPSW_SS_PN_INTERVLAN_OPX_A_REG	5280 03B0h
3B0h	32	CPSW_SS_PN_INTERVLAN_OPX_A_REG	5280 03B0h
3B4h	32	CPSW_SS_PN_INTERVLAN_OPX_B_REG	5280 03B4h
3B4h	32	CPSW_SS_PN_INTERVLAN_OPX_B_REG	5280 03B4h
3B8h	32	CPSW_SS_PN_INTERVLAN_OPX_C_REG	5280 03B8h
3B8h	32	CPSW_SS_PN_INTERVLAN_OPX_C_REG	5280 03B8h
3BCh	32	CPSW_SS_PN_INTERVLAN_OPX_D_REG	5280 03BCh
3BCh	32	CPSW_SS_PN_INTERVLAN_OPX_D_REG	5280 03BCh
3C0h	32	CPSW_SS_PN_CUT_THRU_REG	5280 03C0h
3C0h	32	CPSW_SS_PN_CUT_THRU_REG	5280 03C0h
3C4h	32	CPSW_SS_PN_PORT_SPEED_REG	5280 03C4h
3C4h	32	CPSW_SS_PN_PORT_SPEED_REG	5280 03C4h
500h	32	CPSW_SS_status_reg_out_pulse_0	5280 0500h

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Table 4-885. MSS_CPSW_SS_SS Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_CPSW_SS_SS Physical Address
A80h	32	CPSW_SS_intr_vector_reg_out_pulse	5280 0A80h

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4.10.1 CPSW_SS_CPSW_SS_NUSS_IDVER_REG Registers

4.10.1.1 CPSW_SS_CPSW_SS_NUSS_IDVER_REG Register (Offset = 0h) [reset = 6ba00103h]

Short Description: ID Version Register

Long Description:

Return to Summary Table

Table 4-886. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0000h

Figure 4-307. CPSW_SS_NUSS_IDVER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IDENT															
R															
110101110100000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_VER			MINOR_VER							
R					R			R							
0					1			11							

Access Types Legend

Table 4-887. CPSW_SS_NUSS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	IDENT	R	6422E98E9020h	Identification value
15 - 11	RTL_VER	R	0h	RTL version value
10 - 8	MAJOR_VER	R	1h	Major version value
7 - 0	MINOR_VER	R	Bh	Minor version value

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4.10.2 CPSW_SS_SYNCE_COUNT_REG Registers

4.10.2.1 CPSW_SS_SYNCE_COUNT_REG Register (Offset = 4h) [reset = 0h]

Short Description: SyncE Count Register

Long Description:

Return to Summary Table

Table 4-888. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0004h

Figure 4-308. SYNCE_COUNT_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SYNCE_CNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNCE_CNT															
R/W															
0															

Access Types Legend

Table 4-889. SYNCE_COUNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SYNCE_CNT	R/W	0h	Sync E Count Value

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4.10.3 CPSW_SS_SYNCE_MUX_REG Registers

4.10.3.1 CPSW_SS_SYNCE_MUX_REG Register (Offset = 8h) [reset = 0h]

Short Description: SyncE Mux Register

Long Description:

Return to Summary Table

Table 4-890. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0008h

Figure 4-309. SYNCE_MUX_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SYNCE_SEL					
NONE										R/W					
0										0					

Access Types Legend

Table 4-891. SYNCE_MUX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
5 - 0	SYNCE_SEL	R/W	0h	Sync E Select Value

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4.10.4 CPSW_SS_CONTROL_REG Registers

4.10.4.1 CPSW_SS_CONTROL_REG Register (Offset = 8h) [reset = 0h]

Short Description: control_reg

Long Description:

Return to Summary Table

Table 4-892. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0008h

Figure 4-310. CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														POLARITY_INV	PPM_DIR
NONE														R/W	R/W
0														0	0

Access Types Legend

Table 4-893. CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	POLARITY_INV	R/W	0h	Time Stamp ESTF Generate Function Polarity Invert
0	PPM_DIR	R/W	0h	Time Stamp ESTF Generate Function PPM Direction

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4.10.5 CPSW_SS_SGMII_NON_FIBER_MODE_REG Registers

4.10.5.1 CPSW_SS_SGMII_NON_FIBER_MODE_REG Register (Offset = 10h) [reset = 3h]

Short Description: SGMII NON FIBER Mode Register

Long Description:

Return to Summary Table

Table 4-894. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0010h

Figure 4-311. SGMII_NON_FIBER_MODE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SGMII_NON_FIBER_MODE	
NONE														R/W	
0														11	

Access Types Legend

Table 4-895. SGMII_NON_FIBER_MODE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1 - 0	SGMII_NON_FIBER_MODE	R/W	Bh	This register bit goes to the CPSGMII mode input only

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4.10.6 CPSW_SS_SERDES_RESET_ISO_REG Registers

4.10.6.1 CPSW_SS_SERDES_RESET_ISO_REG Register (Offset = 14h) [reset = 0h]

Short Description: SyncE Mux Register

Long Description:

Return to Summary Table

Table 4-896. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0014h

Figure 4-312. SERDES_RESET_ISO_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SERDES_RESET_ISO	
NONE														R/W	
0														0	

Access Types Legend

Table 4-897. SERDES_RESET_ISO_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1 - 0	SERDES_RESET_ISO	R/W	0h	These bits control whether the SERDES ignores the hard reset for isolation or not

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4.10.7 CPSW_SS_SUBSSYSTEM_STATUS_REG Registers

4.10.7.1 CPSW_SS_SUBSSYSTEM_STATUS_REG Register (Offset = 1Ch) [reset = 0h]

Short Description: Subsystem Status Register

Long Description:

Return to Summary Table

Table 4-898. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 001Ch

Figure 4-313. SUBSSYSTEM_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															EEE_CLKSTOP_ACK
NONE															R
0															0

Access Types Legend

Table 4-899. SUBSSYSTEM_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
0	EEE_CLKSTOP_ACK	R	0h	Energy Efficient Ethernet clockstop acknowledge from CPSW

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4.10.8 CPSW_SS_SUBSYSTEM_CONFIG_REG Registers

4.10.8.1 CPSW_SS_SUBSYSTEM_CONFIG_REG Register (Offset = 20h) [reset = 70203h]

Short Description: Subsystem Configuration Register

Long Description:

Return to Summary Table

Table 4-900. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0020h

Figure 4-314. SUBSYSTEM_CONFIG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				XGMII								QSGMII	SGMII	RGMII	RMII
NONE				R								R	R	R	R
0				0								0	1	1	1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				NUM_GENF				NUM_PORTS							
NONE				R				R							
0				10				11							

Access Types Legend

Table 4-901. SUBSYSTEM_CONFIG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27 - 20	XGMII	R	0h	The Number of XGMII Ports included in the CPSW_SS_NUSS
19	QSGMII	R	0h	QSGMII is included in the CPSW_SS_NUSS
18	SGMII	R	1h	SGMII is included in the CPSW_SS_NUSS
17	RGMII	R	1h	RGMII is included in the CPSW_SS_NUSS
16	RMII	R	1h	RMII is included in the CPSW_SS_NUSS
	RESERVED	NONE		Reserved
12 - 8	NUM_GENF	R	Ah	The number of CPTS GENF outputs
7 - 0	NUM_PORTS	R	Bh	The total number of ports including the host port 0

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4.10.9 CPSW_SS_RGMII1_STATUS_REG Registers

4.10.9.1 CPSW_SS_RGMII1_STATUS_REG Register (Offset = 30h) [reset = 0h]

Short Description: RGMII1 Status Register

Long Description:

Return to Summary Table

Table 4-902. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0030h

Figure 4-315. RGMII1_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												FULLDUPLEX	SPEED		LINK
NONE												R	R		R
0												0	0		0

Access Types Legend

Table 4-903. RGMII1_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	FULLDUPLEX	R	0h	Rgmii1 full dulex: 0=Half-duplex, 1=Full-duplex
2 - 1	SPEED	R	0h	Rgmii1 speed: 00=10Mbps, 01=100Mbps, 10=1000Mbps, 11=reserved
0	LINK	R	0h	Rgmii1 link indicator: 0=Link is down, 1=Link is up

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4.10.10 CPSW_SS_RGMII2_STATUS_REG Registers

4.10.10.1 CPSW_SS_RGMII2_STATUS_REG Register (Offset = 34h) [reset = 0h]

Short Description: RGMII2 Status Register

Long Description:

Return to Summary Table

Table 4-904. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0034h

Figure 4-316. RGMII2_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												FULLDUPLEX	SPEED		LINK
NONE												R	R		R
0												0	0		0

Access Types Legend

Table 4-905. RGMII2_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	FULLDUPLEX	R	0h	Rgmii2 full dulex: 0=Half-duplex, 1=Full-duplex
2 - 1	SPEED	R	0h	Rgmii2 speed: 00=10Mbps, 01=100Mbps, 10=1000Mbps, 11=reserved
0	LINK	R	0h	Rgmii2 link indicator: 0=Link is down, 1=Link is up

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4.10.11 CPSW_SS_SGMII_IDVER_REG Registers

4.10.11.1 CPSW_SS_SGMII_IDVER_REG Register (Offset = 0h) [reset = 4ec21102h]

Short Description: idver_reg

Long Description:

Return to Summary Table

Table 4-906. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0000h

Figure 4-317. SGMII_IDVER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TX_IDENT															
R															
100111011000010															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_VER			MINOR_VER							
R					R			R							
10					1			10							

Access Types Legend

Table 4-907. SGMII_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	TX_IDENT	R	5B0CE93FAECAh	MODULE value
15 - 11	RTL_VER	R	Ah	RTL version value
10 - 8	MAJOR_VER	R	1h	Major version value
7 - 0	MINOR_VER	R	Ah	Minor version value

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4.10.12 CPSW_SS_SOFT_RESET_REG Registers

4.10.12.1 CPSW_SS_SOFT_RESET_REG Register (Offset = 4h) [reset = 0h]

Short Description: soft_reset_reg

Long Description:

Return to Summary Table

Table 4-908. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0004h

Figure 4-318. SOFT_RESET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														RT_SOFT_RESET	SOFT_RESET
NONE														R/W	R/W
0														0	0

Access Types Legend

Table 4-909. SOFT_RESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	RT_SOFT_RESET	R/W	0h	Transmit and receive software reset
0	SOFT_RESET	R/W	0h	Software reset

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4.10.13 CPSW_SS_STATUS_REG Registers

4.10.13.1 CPSW_SS_STATUS_REG Register (Offset = 14h) [reset = 0h]

Short Description: status_reg

Long Description:

Return to Summary Table

Table 4-910. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0014h

Figure 4-319. STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										FIB_SIG_DETECT	LOCK	MR_PAGE_RX	MR_AN_COMPLETE	AN_ERROR	LINK
NONE										R	R	R	R	R	R
0										0	0	0	0	0	0

Access Types Legend

Table 4-911. STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
5	FIB_SIG_DETECT	R	0h	Fiber signal detect
4	LOCK	R	0h	Lock
3	MR_PAGE_RX	R	0h	Next page received
2	MR_AN_COMPLETE	R	0h	Auto-negotiation complete
1	AN_ERROR	R	0h	Auto-negotiation error
0	LINK	R	0h	Link indicator

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4.10.14 CPSW_SS_MR_ADV_ABILITY_REG Registers

4.10.14.1 CPSW_SS_MR_ADV_ABILITY_REG Register (Offset = 18h) [reset = 0h]

Short Description: mr_adv_ability_reg

Long Description:

Return to Summary Table

Table 4-912. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0018h

Figure 4-320. MR_ADV_ABILITY_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR_ADV_ABILITY															
R/W															
0															

Access Types Legend

Table 4-913. MR_ADV_ABILITY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	MR_ADV_ABILITY	R/W	0h	Advertised ability

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4.10.15 CPSW_SS_MR_NP_TX_REG Registers

4.10.15.1 CPSW_SS_MR_NP_TX_REG Register (Offset = 1Ch) [reset = 0h]

Short Description: mr_np_tx_reg

Long Description:

Return to Summary Table

Table 4-914. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 001Ch

Figure 4-321. MR_NP_TX_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR_NP_TX															
R/W															
0															

Access Types Legend

Table 4-915. MR_NP_TX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	MR_NP_TX	R/W	0h	Next page transmit

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4.10.16 CPSW_SS_MR_LP_ADV_ABILITY_REG Registers

4.10.16.1 CPSW_SS_MR_LP_ADV_ABILITY_REG Register (Offset = 20h) [reset = 0h]

Short Description: mr_lp_adv_ability_reg

Long Description:

Return to Summary Table

Table 4-916. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0020h

Figure 4-322. MR_LP_ADV_ABILITY_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR_LP_ADV_ABILITY															
R															
0															

Access Types Legend

Table 4-917. MR_LP_ADV_ABILITY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	MR_LP_ADV_ABILITY	R	0h	Link partner advertised ability

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4.10.17 CPSW_SS_MR_LP_NP_RX_REG Registers

4.10.17.1 CPSW_SS_MR_LP_NP_RX_REG Register (Offset = 24h) [reset = 0h]

Short Description: mr_lp_np_rx_reg

Long Description:

Return to Summary Table

Table 4-918. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0024h

Figure 4-323. MR_LP_NP_RX_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR_LP_NP_RX															
R															
0															

Access Types Legend

Table 4-919. MR_LP_NP_RX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	MR_LP_NP_RX	R	0h	Link Partner Next Page Received

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4.10.18 CPSW_SS_TX_CFG_REG Registers

4.10.18.1 CPSW_SS_TX_CFG_REG Register (Offset = 30h) [reset = 0h]

Short Description: tx_cfg_reg

Long Description:

Return to Summary Table

Table 4-920. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0030h

Figure 4-324. TX_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TX_CFG															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_CFG															
R/W															
0															

Access Types Legend

Table 4-921. TX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TX_CFG	R/W	0h	Transmit configuration register output

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4.10.19 CPSW_SS_RX_CFG_REG Registers

4.10.19.1 CPSW_SS_RX_CFG_REG Register (Offset = 34h) [reset = 0h]

Short Description: rx_cfg_reg

Long Description:

Return to Summary Table

Table 4-922. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0034h

Figure 4-325. RX_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RX_CFG															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_CFG															
R/W															
0															

Access Types Legend

Table 4-923. RX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RX_CFG	R/W	0h	Receive configuration register output

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4.10.20 CPSW_SS_AUX_CFG_REG Registers

4.10.20.1 CPSW_SS_AUX_CFG_REG Register (Offset = 38h) [reset = 0h]

Short Description: aux_cfg_reg

Long Description:

Return to Summary Table

Table 4-924. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0038h

Figure 4-326. AUX_CFG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AUX_CFG															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUX_CFG															
R/W															
0															

Access Types Legend

Table 4-925. AUX_CFG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	AUX_CFG	R/W	0h	Auxiliary configuration register output

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4.10.21 CPSW_SS_DIAG_CLEAR_REG Registers

4.10.21.1 CPSW_SS_DIAG_CLEAR_REG Register (Offset = 40h) [reset = 0h]

Short Description: diag_clear_reg

Long Description:

Return to Summary Table

Table 4-926. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0040h

Figure 4-327. DIAG_CLEAR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															DIAG_CLEAR
NONE															R/W
0															0

Access Types Legend

Table 4-927. DIAG_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
0	DIAG_CLEAR	R/W	0h	Diagnostics clear

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4.10.22 CPSW_SS_DIAG_CONTROL_REG Registers

4.10.22.1 CPSW_SS_DIAG_CONTROL_REG Register (Offset = 44h) [reset = 0h]

Short Description: diag_control_reg

Long Description:

Return to Summary Table

Table 4-928. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0044h

Figure 4-328. DIAG_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									DIAG_SM_SEL			RESERVED		DIAG_EDGE_SEL	
NONE									R/W			NONE		R/W	
0									0			0		0	

Access Types Legend

Table 4-929. DIAG_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6 - 4	DIAG_SM_SEL	R/W	0h	Diagnostic select
	RESERVED	NONE		Reserved
1 - 0	DIAG_EDGE_SEL	R/W	0h	Diagnostics hold signals edge select

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4.10.23 CPSW_SS_DIAG_STATUS_REG Registers

4.10.23.1 CPSW_SS_DIAG_STATUS_REG Register (Offset = 48h) [reset = 0h]

Short Description: diag_status_reg

Long Description:

Return to Summary Table

Table 4-930. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0048h

Figure 4-329. DIAG_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIAG_STATUS															
R															
0															

Access Types Legend

Table 4-931. DIAG_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	DIAG_STATUS	R	0h	Diagnostics status

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4.10.24 CPSW_SS_MDIO_VERSION_REG Registers

4.10.24.1 CPSW_SS_MDIO_VERSION_REG Register (Offset = 0h) [reset = 70907h]

Short Description: version_reg

Long Description:

Return to Summary Table

Table 4-932. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0000h

Figure 4-330. MDIO_VERSION_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R		R		R											
0		0		111											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL				REVMAJ				CUSTOM		REVMIN					
R				R				R		R					
1				1				0		111					

Access Types Legend

Table 4-933. MDIO_VERSION_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	R	0h	Scheme
29 - 28	BU	R	0h	bu
27 - 16	MODULE_ID	R	6Fh	Module ID
15 - 11	REVRTL	R	1h	RTL version
10 - 8	REVMAJ	R	1h	Major version
7 - 6	CUSTOM	R	0h	Custom version
5 - 0	REVMIN	R	6Fh	Minor version

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4.10.25 CPSW_SS_ALIVE_REG Registers

4.10.25.1 CPSW_SS_ALIVE_REG Register (Offset = 8h) [reset = 0h]

Short Description: alive_reg

Long Description:

Return to Summary Table

Table 4-934. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0008h

Figure 4-331. ALIVE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ALIVE															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALIVE															
R/W															
0															

Access Types Legend

Table 4-935. ALIVE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ALIVE	R/W	0h	MDIO alive

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4.10.26 CPSW_SS_LINK_REG Registers

4.10.26.1 CPSW_SS_LINK_REG Register (Offset = Ch) [reset = 0h]

Short Description: link_reg

Long Description:

Return to Summary Table

Table 4-936. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 000Ch

Figure 4-332. LINK_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LINK															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LINK															
R															
0															

Access Types Legend

Table 4-937. LINK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	LINK	R	0h	MDIO link state

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4.10.27 CPSW_SS_LINK_INT_RAW_REG Registers

4.10.27.1 CPSW_SS_LINK_INT_RAW_REG Register (Offset = 10h) [reset = 0h]

Short Description: link_int_raw_reg

Long Description:

Return to Summary Table

Table 4-938. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0010h

Figure 4-333. LINK_INT_RAW_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														LINKINTRAW	
NONE														R/W	
0														0	

Access Types Legend

Table 4-939. LINK_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1 - 0	LINKINTRAW	R/W	0h	MDIO link change event raw value

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4.10.28 CPSW_SS_LINK_INT_MASKED_REG Registers

4.10.28.1 CPSW_SS_LINK_INT_MASKED_REG Register (Offset = 14h) [reset = 0h]

Short Description: link_int_masked_reg

Long Description:

Return to Summary Table

Table 4-940. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0014h

Figure 4-334. LINK_INT_MASKED_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														LINKINTMASKED	
NONE														R/W	
0														0	

Access Types Legend

Table 4-941. LINK_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1 - 0	LINKINTMASKED	R/W	0h	MDIO link change interrupt masked value

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4.10.29 CPSW_SS_LINK_INT_MASK_SET_REG Registers

4.10.29.1 CPSW_SS_LINK_INT_MASK_SET_REG Register (Offset = 18h) [reset = 0h]

Short Description: link_int_mask_set_reg

Long Description:

Return to Summary Table

Table 4-942. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0018h

Figure 4-335. LINK_INT_MASK_SET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															LINKINTMASKSET
NONE															R/W
0															0

Access Types Legend

Table 4-943. LINK_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
0	LINKINTMASKSET	R/W	0h	MDIO link interrupt mask set

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4.10.30 CPSW_SS_LINK_INT_MASK_CLEAR_REG Registers

4.10.30.1 CPSW_SS_LINK_INT_MASK_CLEAR_REG Register (Offset = 1Ch) [reset = 0h]

Short Description: link_int_mask_clear_reg

Long Description:

Return to Summary Table

Table 4-944. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 001Ch

Figure 4-336. LINK_INT_MASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															LINKINTMASKCLR
NONE															R/W
0															0

Access Types Legend

Table 4-945. LINK_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
0	LINKINTMASKCLR	R/W	0h	MDIO link interrupt mask clear

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4.10.31 CPSW_SS_USER_INT_RAW_REG Registers

4.10.31.1 CPSW_SS_USER_INT_RAW_REG Register (Offset = 20h) [reset = 0h]

Short Description: user_int_raw_reg

Long Description:

Return to Summary Table

Table 4-946. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0020h

Figure 4-337. USER_INT_RAW_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														USERINTRAW	
NONE														R/W	
0														0	

Access Types Legend

Table 4-947. USER_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1 - 0	USERINTRAW	R/W	0h	User interrupt raw

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4.10.32 CPSW_SS_USER_INT_MASKED_REG Registers

4.10.32.1 CPSW_SS_USER_INT_MASKED_REG Register (Offset = 24h) [reset = 0h]

Short Description: user_int_masked_reg

Long Description:

Return to Summary Table

Table 4-948. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0024h

Figure 4-338. USER_INT_MASKED_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														USERINTMASKED	
NONE														R/W	
0														0	

Access Types Legend

Table 4-949. USER_INT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1 - 0	USERINTMASKED	R/W	0h	User interrupt masked

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4.10.33 CPSW_SS_USER_INT_MASK_SET_REG Registers

4.10.33.1 CPSW_SS_USER_INT_MASK_SET_REG Register (Offset = 28h) [reset = 0h]

Short Description: user_int_mask_set_reg

Long Description:

Return to Summary Table

Table 4-950. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0028h

Figure 4-339. USER_INT_MASK_SET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														USERINTMASKSET	
NONE														R/W	
0														0	

Access Types Legend

Table 4-951. USER_INT_MASK_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1 - 0	USERINTMASKSET	R/W	0h	MDIO user interrupt mask set

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4.10.34 CPSW_SS_USER_INT_MASK_CLEAR_REG Registers

4.10.34.1 CPSW_SS_USER_INT_MASK_CLEAR_REG Register (Offset = 2Ch) [reset = 0h]

Short Description: user_int_mask_clear_reg

Long Description:

Return to Summary Table

Table 4-952. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 002Ch

Figure 4-340. USER_INT_MASK_CLEAR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														USERINTMASK CLR	
NONE														R/W	
0														0	

Access Types Legend

Table 4-953. USER_INT_MASK_CLEAR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1 - 0	USERINTMASKCLR	R/W	0h	MDIO user interrupt mask clear

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4.10.35 CPSW_SS_MANUAL_IF_REG Registers

4.10.35.1 CPSW_SS_MANUAL_IF_REG Register (Offset = 30h) [reset = 0h]

Short Description: manual_if_reg

Long Description:

Return to Summary Table

Table 4-954. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0030h

Figure 4-341. MANUAL_IF_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MDIO_MDCLK_O	MDIO_OE	MDIO_PIN
NONE													R/W	R/W	R/W
0													0	0	0

Access Types Legend

Table 4-955. MANUAL_IF_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2	MDIO_MDCLK_O	R/W	0h	MDIO Clock Output
1	MDIO_OE	R/W	0h	MDIO Output Enable
0	MDIO_PIN	R/W	0h	MDIO Pin

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4.10.36 CPSW_SS_POLL_REG Registers

4.10.36.1 CPSW_SS_POLL_REG Register (Offset = 34h) [reset = 0h]

Short Description: poll_reg

Long Description:

Return to Summary Table

Table 4-956. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0034h

Figure 4-342. POLL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MANUALMODE	STATECHANGEMODE	RESERVED													
R/W	R/W	NONE													
0	0	0													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								IPG							
NONE								R/W							
0								0							

Access Types Legend

Table 4-957. POLL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	MANUALMODE	R/W	0h	MDIO Manual Mode
30	STATECHANGEMODE	R/W	0h	MDIO State Change Mode
	RESERVED	NONE		Reserved
7 - 0	IPG	R/W	0h	MDIO IPG

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4.10.37 CPSW_SS_POLL_EN_REG Registers

4.10.37.1 CPSW_SS_POLL_EN_REG Register (Offset = 38h) [reset = ffffffffh]

Short Description: poll_reg

Long Description:

Return to Summary Table

Table 4-958. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0038h

Figure 4-343. POLL_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POLL_EN															
R/W															
11111111111111111111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POLL_EN															
R/W															
11111111111111111111111111111111															

Access Types Legend

Table 4-959. POLL_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	POLL_EN	R/W	8C3DEFB1 EDB984FE2 AC71C71C7 h	MDIO Poll Enable

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4.10.38 CPSW_SS_CLAUS45_REG Registers

4.10.38.1 CPSW_SS_CLAUS45_REG Register (Offset = 3Ch) [reset = 0h]

Short Description: poll_reg

Long Description:

Return to Summary Table

Table 4-960. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 003Ch

Figure 4-344. CLAUS45_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLAUSE45															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLAUSE45															
R/W															
0															

Access Types Legend

Table 4-961. CLAUS45_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CLAUSE45	R/W	0h	MDIO Clause 45

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4.10.39 CPSW_SS_USER_ADDR0_REG Registers

4.10.39.1 CPSW_SS_USER_ADDR0_REG Register (Offset = 40h) [reset = 0h]

Short Description: poll_reg

Long Description:

Return to Summary Table

Table 4-962. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0040h

Figure 4-345. USER_ADDR0_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USER_ADDR0															
R/W															
0															

Access Types Legend

Table 4-963. USER_ADDR0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	USER_ADDR0	R/W	0h	MDIO USER Address 0

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4.10.40 CPSW_SS_USER_ADDR1_REG Registers

4.10.40.1 CPSW_SS_USER_ADDR1_REG Register (Offset = 44h) [reset = 0h]

Short Description: poll_reg

Long Description:

Return to Summary Table

Table 4-964. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0044h

Figure 4-346. USER_ADDR1_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USER_ADDR1															
R/W															
0															

Access Types Legend

Table 4-965. USER_ADDR1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	USER_ADDR1	R/W	0h	MDIO USER Address 1

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4.10.41 CPSW_SS_REVISION Registers

4.10.41.1 CPSW_SS_REVISION Register (Offset = 0h) [reset = 6690a200h]

Short Description:

Long Description:

Return to Summary Table

Table 4-966. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0000h

Figure 4-347. REVISION Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNCTION											
R		R		R											
1		10		11010010000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTLVER				MAJREV				CUSTOM		MINREV					
R				R				R		R					
10100				10				0		0					

Access Types Legend

Table 4-967. REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	R	1h	Scheme
29 - 28	BU	R	Ah	BU
27 - 16	FUNCTION	R	2903F6B90h	Module ID
15 - 11	RTLVER	R	2774h	RTL revisions
10 - 8	MAJREV	R	Ah	Major revision
7 - 6	CUSTOM	R	0h	Custom revision
5 - 0	MINREV	R	0h	Minor revision

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4.10.42 CPSW_SS_EOI_REG Registers

4.10.42.1 CPSW_SS_EOI_REG Register (Offset = 10h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-968. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0010h

Figure 4-348. EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EOI_VECTOR							
NONE								R/W							
0								0							

Access Types Legend

Table 4-969. EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	EOI_VECTOR	R/W	0h	End of Interrupt Vector

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4.10.43 CPSW_SS_INTR_VECTOR_REG Registers

4.10.43.1 CPSW_SS_INTR_VECTOR_REG Register (Offset = 14h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-970. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0014h

Figure 4-349. INTR_VECTOR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTR_VECTOR															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTR_VECTOR															
R															
0															

Access Types Legend

Table 4-971. INTR_VECTOR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INTR_VECTOR	R	0h	Interrupt Vector Register

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4.10.44 CPSW_SS_ENABLE_REG_OUT_PULSE_0 Registers

4.10.44.1 CPSW_SS_ENABLE_REG_OUT_PULSE_0 Register (Offset = 100h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-972. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0100h

Figure 4-350. ENABLE_REG_OUT_PULSE_0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ENABLE_OUT_PULSE_EN_STAT_PENDA	ENABLE_OUT_PULSE_EN_MDIO_PENDA	ENABLE_OUT_PULSE_EN_EVNT_PENDA
NONE													R/W1TS	R/W1TS	R/W1TS
0													0	0	0

Access Types Legend

Table 4-973. ENABLE_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2	ENABLE_OUT_PULSE_EN_STAT_PENDA	R/W1TS	0h	Enable Set for out_pulse_en_stat_penda
1	ENABLE_OUT_PULSE_EN_MDIO_PENDA	R/W1TS	0h	Enable Set for out_pulse_en_mdio_penda
0	ENABLE_OUT_PULSE_EN_EVNT_PENDA	R/W1TS	0h	Enable Set for out_pulse_en_evnt_penda

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4.10.45 CPSW_SS_ENABLE_CLR_REG_OUT_PULSE_0 Registers

4.10.45.1 CPSW_SS_ENABLE_CLR_REG_OUT_PULSE_0 Register (Offset = 300h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-974. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0300h

Figure 4-351. ENABLE_CLR_REG_OUT_PULSE_0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ENABLE_OUT_PULSE_EN_STAT_PENDA_CLR	ENABLE_OUT_PULSE_EN_MDIO_PENDA_CLR	ENABLE_OUT_PULSE_EN_EVNT_PENDA_CLR
NONE													R/W1TC	R/W1TC	R/W1TC
0													0	0	0

Access Types Legend

Table 4-975. ENABLE_CLR_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2	ENABLE_OUT_PULSE_EN_STAT_PENDA_CLR	R/W1TC	0h	Enable Clear for out_pulse_en_stat_penda
1	ENABLE_OUT_PULSE_EN_MDIO_PENDA_CLR	R/W1TC	0h	Enable Clear for out_pulse_en_mdio_penda
0	ENABLE_OUT_PULSE_EN_EVNT_PENDA_CLR	R/W1TC	0h	Enable Clear for out_pulse_en_evnt_penda

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4.10.46 CPSW_SS_STATUS_REG_OUT_PULSE_0 Registers

4.10.46.1 CPSW_SS_STATUS_REG_OUT_PULSE_0 Register (Offset = 500h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-976. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0500h

Figure 4-352. STATUS_REG_OUT_PULSE_0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													STATUS_OUT_PULSE_STAT_PENDA	STATUS_OUT_PULSE_MDIO_PENDA	STATUS_OUT_PULSE_EVNT_PENDA
NONE													R	R	R
0													0	0	0

Access Types Legend

Table 4-977. STATUS_REG_OUT_PULSE_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2	STATUS_OUT_PULSE_STAT_PENDA	R	0h	Status for out_pulse_en_stat_penda
1	STATUS_OUT_PULSE_MDIO_PENDA	R	0h	Status for out_pulse_en_mdio_penda
0	STATUS_OUT_PULSE_EVNT_PENDA	R	0h	Status for out_pulse_en_evnt_penda

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4.10.47 CPSW_SS_INTR_VECTOR_REG_OUT_PULSE Registers

4.10.47.1 CPSW_SS_INTR_VECTOR_REG_OUT_PULSE Register (Offset = A80h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-978. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0A80h

Figure 4-353. INTR_VECTOR_REG_OUT_PULSE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INTR_VECTOR_OUT_PULSE															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTR_VECTOR_OUT_PULSE															
R															
0															

Access Types Legend

Table 4-979. INTR_VECTOR_REG_OUT_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	INTR_VECTOR_OUT_PULSE	R	0h	Interrupt Vector

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4.10.48 CPSW_SS_CPSW_SS_ID_VER_REG Registers

4.10.48.1 CPSW_SS_CPSW_SS_ID_VER_REG Register (Offset = 0h) [reset = 6ba80103h]

Short Description: idver_reg

Long Description:

Return to Summary Table

Table 4-980. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0000h

Figure 4-354. CPSW_SS_ID_VER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IDENT															
R															
110101110101000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_VER			MINOR_VER							
R					R			R							
0					1			11							

Access Types Legend

Table 4-981. CPSW_SS_ID_VER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	IDENT	R	6422E98E9408h	Identification Value
15 - 11	RTL_VER	R	0h	RTL Version Value
10 - 8	MAJOR_VER	R	1h	Major Version Value
7 - 0	MINOR_VER	R	Bh	Minor Version Value

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4.10.49 CPSW_SS_EM_CONTROL_REG Registers

4.10.49.1 CPSW_SS_EM_CONTROL_REG Register (Offset = 10h) [reset = 0h]

Short Description: em_control_reg

Long Description:

Return to Summary Table

Table 4-982. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0010h

Figure 4-355. EM_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SOFT	FREE
NONE														R/W	R/W
0														0	0

Access Types Legend

Table 4-983. EM_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

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4.10.50 CPSW_SS_STAT_PORT_EN_REG Registers

4.10.50.1 CPSW_SS_STAT_PORT_EN_REG Register (Offset = 14h) [reset = 0h]

Short Description: stat_port_en_reg

Long Description:

Return to Summary Table

Table 4-984. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0014h

Figure 4-356. STAT_PORT_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							P8_STAT_EN	P7_STAT_EN	P6_STAT_EN	P5_STAT_EN	P4_STAT_EN	P3_STAT_EN	P2_STAT_EN	P1_STAT_EN	P0_STAT_EN
NONE							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0							0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-985. STAT_PORT_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
8	P8_STAT_EN	R/W	0h	Port 8 Statistics Enable
7	P7_STAT_EN	R/W	0h	Port 7 Statistics Enable
6	P6_STAT_EN	R/W	0h	Port 6 Statistics Enable
5	P5_STAT_EN	R/W	0h	Port 5 Statistics Enable
4	P4_STAT_EN	R/W	0h	Port 4 Statistics Enable
3	P3_STAT_EN	R/W	0h	Port 3 Statistics Enable
2	P2_STAT_EN	R/W	0h	Port 2 Statistics Enable
1	P1_STAT_EN	R/W	0h	Port 1 Statistics Enable
0	P0_STAT_EN	R/W	0h	Port 0 Statistics Enable

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4.10.51 CPSW_SS_PTYPE_REG Registers

4.10.51.1 CPSW_SS_PTYPE_REG Register (Offset = 18h) [reset = 0h]

Short Description: ptype_reg

Long Description:

Return to Summary Table

Table 4-986. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0018h

Figure 4-357. PTYPE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															P8_PTYPE_ESC
NONE															R/W
0															0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P7_PTYPE_ESC	P6_PTYPE_ESC	P5_PTYPE_ESC	P4_PTYPE_ESC	P3_PTYPE_ESC	P2_PTYPE_ESC	P1_PTYPE_ESC	P0_PTYPE_ESC	RESERVED			ESC_PRI_LD_VAL				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	NONE			R/W				
0	0	0	0	0	0	0	0	0			0				

Access Types Legend

Table 4-987. PTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
16	P8_PTYPE_ESC	R/W	0h	Port 8 Priority Type Escalate
15	P7_PTYPE_ESC	R/W	0h	Port 7 Priority Type Escalate
14	P6_PTYPE_ESC	R/W	0h	Port 6 Priority Type Escalate
13	P5_PTYPE_ESC	R/W	0h	Port 5 Priority Type Escalate
12	P4_PTYPE_ESC	R/W	0h	Port 4 Priority Type Escalate
11	P3_PTYPE_ESC	R/W	0h	Port 3 Priority Type Escalate
10	P2_PTYPE_ESC	R/W	0h	Port 2 Priority Type Escalate
9	P1_PTYPE_ESC	R/W	0h	Port 1 Priority Type Escalate
8	P0_PTYPE_ESC	R/W	0h	Port 0 Priority Type Escalate
	RESERVED	NONE		Reserved
4 - 0	ESC_PRI_LD_VAL	R/W	0h	Escalate Priority Load Value

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4.10.52 CPSW_SS_SOFT_IDLE_REG Registers

4.10.52.1 CPSW_SS_SOFT_IDLE_REG Register (Offset = 1Ch) [reset = 0h]

Short Description: soft_idle_reg

Long Description:

Return to Summary Table

Table 4-988. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 001Ch

Figure 4-358. SOFT_IDLE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															SOFT_IDLE
NONE															R/W
0															0

Access Types Legend

Table 4-989. SOFT_IDLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
0	SOFT_IDLE	R/W	0h	Software Idle

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4.10.53 CPSW_SS_THRU_RATE_REG Registers

4.10.53.1 CPSW_SS_THRU_RATE_REG Register (Offset = 20h) [reset = 3001h]

Short Description: thru_rate_reg

Long Description:

Return to Summary Table

Table 4-990. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0020h

Figure 4-359. THRU_RATE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SL_RX_THRU_RATE				RESERVED								P0_RX_THRU_RATE			
R/W				NONE								R/W			
11				0								1			

Access Types Legend

Table 4-991. THRU_RATE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 12	SL_RX_THRU_RATE	R/W	Bh	Switch FIFO receive through rate
	RESERVED	NONE		Reserved
3 - 0	P0_RX_THRU_RATE	R/W	1h	CPPI FIFO receive through rate

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4.10.54 CPSW_SS_GAP_THRESH_REG Registers

4.10.54.1 CPSW_SS_GAP_THRESH_REG Register (Offset = 24h) [reset = bh]

Short Description: gap_thresh_reg

Long Description:

Return to Summary Table

Table 4-992. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0024h

Figure 4-360. GAP_THRESH_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											GAP_THRESH				
NONE											R/W				
0											1011				

Access Types Legend

Table 4-993. GAP_THRESH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	GAP_THRESH	R/W	3F3h	Short Gap Threshold

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4.10.55 CPSW_SS_EEE_PRESCALE_REG Registers

4.10.55.1 CPSW_SS_EEE_PRESCALE_REG Register (Offset = 2Ch) [reset = 0h]

Short Description: eee_prescale_reg

Long Description:

Return to Summary Table

Table 4-994. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 002Ch

Figure 4-361. EEE_PRESCALE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				EEE_PRESCALE											
NONE				R/W											
0				0											

Access Types Legend

Table 4-995. EEE_PRESCALE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 0	EEE_PRESCALE	R/W	0h	Energy Efficient Ethernet Pre-scale count load value

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4.10.56 CPSW_SS_TX_G_OFLOW_THRESH_SET_REG Registers

4.10.56.1 CPSW_SS_TX_G_OFLOW_THRESH_SET_REG Register (Offset = 30h) [reset = ffffffffh]

Short Description: tx_g_oflow_thresh_set_reg

Long Description:

Return to Summary Table

Table 4-996. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0030h

Figure 4-362. TX_G_OFLOW_THRESH_SET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI7				PRI6				PRI5				PRI4			
R/W				R/W				R/W				R/W			
1111				1111				1111				1111			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI3				PRI2				PRI1				PRI0			
R/W				R/W				R/W				R/W			
1111				1111				1111				1111			

Access Types Legend

Table 4-997. TX_G_OFLOW_THRESH_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 28	PRI7	R/W	457h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 7
27 - 24	PRI6	R/W	457h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 6
23 - 20	PRI5	R/W	457h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 5
19 - 16	PRI4	R/W	457h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 4
15 - 12	PRI3	R/W	457h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 3
11 - 8	PRI2	R/W	457h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 2
7 - 4	PRI1	R/W	457h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 1
3 - 0	PRI0	R/W	457h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 0

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4.10.57 CPSW_SS_TX_G_OFLOW_THRESH_CLR_REG Registers

4.10.57.1 CPSW_SS_TX_G_OFLOW_THRESH_CLR_REG Register (Offset = 34h) [reset = 0h]

Short Description: tx_g_oflow_thresh_clr_reg

Long Description:

Return to Summary Table

Table 4-998. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0034h

Figure 4-363. TX_G_OFLOW_THRESH_CLR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI7				PRI6				PRI5				PRI4			
R/W				R/W				R/W				R/W			
0				0				0				0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI3				PRI2				PRI1				PRI0			
R/W				R/W				R/W				R/W			
0				0				0				0			

Access Types Legend

Table 4-999. TX_G_OFLOW_THRESH_CLR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 28	PRI7	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 7
27 - 24	PRI6	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 6
23 - 20	PRI5	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 5
19 - 16	PRI4	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 4
15 - 12	PRI3	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 3
11 - 8	PRI2	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 2
7 - 4	PRI1	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 1
3 - 0	PRI0	R/W	0h	Priority Based Flow Control Global Outflow Usage Threshold for Pri 0

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4.10.58 CPSW_SS_TX_G_BUF_THRESH_SET_L_REG Registers

4.10.58.1 CPSW_SS_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 38h) [reset = ffffffffh]

Short Description: tx_g_buf_thresh_set_l_reg

Long Description:

Return to Summary Table

Table 4-1000. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0038h

Figure 4-364. TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI3								PRI2							
R/W								R/W							
11111111								11111111							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI1								PRI0							
R/W								R/W							
11111111								11111111							

Access Types Legend

Table 4-1001. TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	PRI3	R/W	A98AC7h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 3
23 - 16	PRI2	R/W	A98AC7h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 2
15 - 8	PRI1	R/W	A98AC7h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 1
7 - 0	PRI0	R/W	A98AC7h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 0

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4.10.59 CPSW_SS_TX_G_BUF_THRESH_SET_H_REG Registers

4.10.59.1 CPSW_SS_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 3Ch) [reset = ffffffffh]

Short Description: tx_g_buf_thresh_set_h_reg

Long Description:

Return to Summary Table

Table 4-1002. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 003Ch

Figure 4-365. TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI7								PRI6							
R/W								R/W							
11111111								11111111							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI5								PRI4							
R/W								R/W							
11111111								11111111							

Access Types Legend

Table 4-1003. TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	PRI7	R/W	A98AC7h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 7
23 - 16	PRI6	R/W	A98AC7h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 6
15 - 8	PRI5	R/W	A98AC7h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 5
7 - 0	PRI4	R/W	A98AC7h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 4

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4.10.60 CPSW_SS_TX_G_BUF_THRESH_CLR_L_REG Registers

4.10.60.1 CPSW_SS_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 40h) [reset = 0h]

Short Description: tx_g_buf_thresh_clr_l_reg

Long Description:

Return to Summary Table

Table 4-1004. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0040h

Figure 4-366. TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI3								PRI2							
R/W								R/W							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI1								PRI0							
R/W								R/W							
0								0							

Access Types Legend

Table 4-1005. TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	PRI3	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 3
23 - 16	PRI2	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 2
15 - 8	PRI1	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 1
7 - 0	PRI0	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 0

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4.10.61 CPSW_SS_TX_G_BUF_THRESH_CLR_H_REG Registers

4.10.61.1 CPSW_SS_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 44h) [reset = 0h]

Short Description: tx_g_buf_thresh_clr_h_reg

Long Description:

Return to Summary Table

Table 4-1006. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0044h

Figure 4-367. TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI7								PRI6							
R/W								R/W							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI5								PRI4							
R/W								R/W							
0								0							

Access Types Legend

Table 4-1007. TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	PRI7	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 7
23 - 16	PRI6	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 6
15 - 8	PRI5	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 5
7 - 0	PRI4	R/W	0h	Priority Based Flow Control Global Buffer Usage Threshold for Priority 4

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4.10.62 CPSW_SS_VLAN_LTYPE_REG Registers

4.10.62.1 CPSW_SS_VLAN_LTYPE_REG Register (Offset = 50h) [reset = 88a88100h]

Short Description: vlan_ltype_reg

Long Description:

Return to Summary Table

Table 4-1008. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0050h

Figure 4-368. VLAN_LTYPE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VLAN_LTYPE_OUTER															
R/W															
1000100010101000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VLAN_LTYPE_INNER															
R/W															
1000000100000000															

Access Types Legend

Table 4-1009. VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	VLAN_LTYPE_OUTER	R/W	38D95EDD78908h	Outer VLAN LType
15 - 0	VLAN_LTYPE_INNER	R/W	38D7EAABC6100h	Inner VLAN LType

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4.10.63 CPSW_SS_EST_TS_DOMAIN_REG Registers

4.10.63.1 CPSW_SS_EST_TS_DOMAIN_REG Register (Offset = 54h) [reset = 0h]

Short Description: est_ts_domain_reg

Long Description:

Return to Summary Table

Table 4-1010. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0054h

Figure 4-369. EST_TS_DOMAIN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EST_TS_DOMAIN							
NONE								R/W							
0								0							

Access Types Legend

Table 4-1011. EST_TS_DOMAIN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	EST_TS_DOMAIN	R/W	0h	Enhanced Scheduled Traffic Host Event Domain

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4.10.64 CPSW_SS_CUT_THRESHOLD_REG Registers

4.10.64.1 CPSW_SS_CUT_THRESHOLD_REG Register (Offset = 58h) [reset = 0h]

Short Description: cut_threshold_reg

Long Description:

Return to Summary Table

Table 4-1012. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0058h

Figure 4-370. CUT_THRESHOLD_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CUT_THRESH			
NONE												R/W			
0												0			

Access Types Legend

Table 4-1013. CUT_THRESHOLD_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	CUT_THRESH	R/W	0h	Cut-thru Threshold

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4.10.65 CPSW_SS_FREQUENCY_REG Registers

4.10.65.1 CPSW_SS_FREQUENCY_REG Register (Offset = 5Ch) [reset = 0h]

Short Description: cut_threshold_reg

Long Description:

Return to Summary Table

Table 4-1014. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 005Ch

Figure 4-371. FREQUENCY_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						CUT_THRESH									
NONE						R/W									
0						0									

Access Types Legend

Table 4-1015. FREQUENCY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	CUT_THRESH	R/W	0h	CPSW CPPI_CLK Frequency in Mhz

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4.10.66 CPSW_SS_IET_HOLD_CNT_LD_VAL_REG Registers

4.10.66.1 CPSW_SS_IET_HOLD_CNT_LD_VAL_REG Register (Offset = 60h) [reset = 64h]

Short Description: iet_hold_cnt_ld_val_reg

Long Description:

Return to Summary Table

Table 4-1016. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0060h

Figure 4-372. IET_HOLD_CNT_LD_VAL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								IET_HOLD_CNT_LD_VAL							
NONE								R/W							
0								1100100							

Access Types Legend

Table 4-1017. IET_HOLD_CNT_LD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	IET_HOLD_CNT_LD_VAL	R/W	10C944h	IET_HOLD_CNT_LD_VAL

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4.10.67 CPSW_SS_TX_PRI0_MAXLEN_REG Registers

4.10.67.1 CPSW_SS_TX_PRI0_MAXLEN_REG Register (Offset = 100h) [reset = 7e8h]

Short Description: tx_pri0_maxlen_reg

Long Description:

Return to Summary Table

Table 4-1018. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0100h

Figure 4-373. TX_PRI0_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_PRI0_MAXLEN													
NONE		R/W													
0		11111101000													

Access Types Legend

Table 4-1019. TX_PRI0_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
13 - 0	TX_PRI0_MAXLEN	R/W	29645F248h	Transmit Priority 0 Maximum Length

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4.10.68 CPSW_SS_TX_PRI1_MAXLEN_REG Registers

4.10.68.1 CPSW_SS_TX_PRI1_MAXLEN_REG Register (Offset = 104h) [reset = 7e8h]

Short Description: tx_pri1_maxlen_reg

Long Description:

Return to Summary Table

Table 4-1020. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0104h

Figure 4-374. TX_PRI1_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_PRI1_MAXLEN													
NONE		R/W													
0		11111101000													

Access Types Legend

Table 4-1021. TX_PRI1_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
13 - 0	TX_PRI1_MAXLEN	R/W	29645F248h	Transmit Priority 1 Maximum Length

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4.10.69 CPSW_SS_TX_PRI2_MAXLEN_REG Registers

4.10.69.1 CPSW_SS_TX_PRI2_MAXLEN_REG Register (Offset = 108h) [reset = 7e8h]

Short Description: tx_pri2_maxlen_reg

Long Description:

Return to Summary Table

Table 4-1022. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0108h

Figure 4-375. TX_PRI2_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_PRI2_MAXLEN													
NONE		R/W													
0		11111101000													

Access Types Legend

Table 4-1023. TX_PRI2_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
13 - 0	TX_PRI2_MAXLEN	R/W	29645F248h	Transmit Priority 2 Maximum Length

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4.10.70 CPSW_SS_TX_PRI3_MAXLEN_REG Registers

4.10.70.1 CPSW_SS_TX_PRI3_MAXLEN_REG Register (Offset = 10Ch) [reset = 7e8h]

Short Description: tx_pri3_maxlen_reg

Long Description:

Return to Summary Table

Table 4-1024. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 010Ch

Figure 4-376. TX_PRI3_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_PRI3_MAXLEN													
NONE		R/W													
0		11111101000													

Access Types Legend

Table 4-1025. TX_PRI3_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
13 - 0	TX_PRI3_MAXLEN	R/W	29645F248h	Transmit Priority 3 Maximum Length

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4.10.71 CPSW_SS_TX_PRI4_MAXLEN_REG Registers

4.10.71.1 CPSW_SS_TX_PRI4_MAXLEN_REG Register (Offset = 110h) [reset = 7e8h]

Short Description: tx_pri4_maxlen_reg

Long Description:

Return to Summary Table

Table 4-1026. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0110h

Figure 4-377. TX_PRI4_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_PRI4_MAXLEN													
NONE		R/W													
0		11111101000													

Access Types Legend

Table 4-1027. TX_PRI4_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
13 - 0	TX_PRI4_MAXLEN	R/W	29645F248h	Transmit Priority 4 Maximum Length

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4.10.72 CPSW_SS_TX_PRI5_MAXLEN_REG Registers

4.10.72.1 CPSW_SS_TX_PRI5_MAXLEN_REG Register (Offset = 114h) [reset = 7e8h]

Short Description: tx_pri5_maxlen_reg

Long Description:

Return to Summary Table

Table 4-1028. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0114h

Figure 4-378. TX_PRI5_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_PRI5_MAXLEN													
NONE		R/W													
0		11111101000													

Access Types Legend

Table 4-1029. TX_PRI5_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
13 - 0	TX_PRI5_MAXLEN	R/W	29645F248h	Transmit Priority 5 Maximum Length

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4.10.73 CPSW_SS_TX_PRI6_MAXLEN_REG Registers

4.10.73.1 CPSW_SS_TX_PRI6_MAXLEN_REG Register (Offset = 118h) [reset = 7e8h]

Short Description: tx_pri6_maxlen_reg

Long Description:

Return to Summary Table

Table 4-1030. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0118h

Figure 4-379. TX_PRI6_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_PRI6_MAXLEN													
NONE		R/W													
0		11111101000													

Access Types Legend

Table 4-1031. TX_PRI6_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
13 - 0	TX_PRI6_MAXLEN	R/W	29645F248h	Transmit Priority 6 Maximum Length

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4.10.74 CPSW_SS_TX_PRI7_MAXLEN_REG Registers

4.10.74.1 CPSW_SS_TX_PRI7_MAXLEN_REG Register (Offset = 11Ch) [reset = 7e8h]

Short Description: tx_pri7_maxlen_reg

Long Description:

Return to Summary Table

Table 4-1032. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 011Ch

Figure 4-380. TX_PRI7_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TX_PRI7_MAXLEN													
NONE		R/W													
0		11111101000													

Access Types Legend

Table 4-1033. TX_PRI7_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
13 - 0	TX_PRI7_MAXLEN	R/W	29645F248h	Transmit Priority 7 Maximum Length

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4.10.75 CPSW_SS_USER_ACCESS_REG Registers

4.10.75.1 CPSW_SS_USER_ACCESS_REG Register (Offset = 0h) [reset = 0h]

Short Description: user_access_reg

Long Description:

Return to Summary Table

Table 4-1034. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0000h

Figure 4-381. USER_ACCESS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GO	WRITE	ACK	RESERVED			REGADR					PHYADR				
R/W	R/W	R/W	NONE			R/W					R/W				
0	0	0	0			0					0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															
R/W															
0															

Access Types Legend

Table 4-1035. USER_ACCESS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GO	R/W	0h	Go
30	WRITE	R/W	0h	Write
29	ACK	R/W	0h	Acknowledge
	RESERVED	NONE		Reserved
25 - 21	REGADR	R/W	0h	Register address
20 - 16	PHYADR	R/W	0h	PHY address
15 - 0	DATA	R/W	0h	User data

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4.10.76 CPSW_SS_USER_PHY_SEL_REG Registers

4.10.76.1 CPSW_SS_USER_PHY_SEL_REG Register (Offset = 4h) [reset = 0h]

Short Description: user_phy_sel_reg

Long Description:

Return to Summary Table

Table 4-1036. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0004h

Figure 4-382. USER_PHY_SEL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LINKSEL	LINKINT_ENABLE	RESERVED	PHYADR_MON				
NONE								R/W	R/W	NONE	R/W				
0								0	0	0	0				

Access Types Legend

Table 4-1037. USER_PHY_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7	LINKSEL	R/W	0h	Link status determination select
6	LINKINT_ENABLE	R/W	0h	Link change interrupt enable
	RESERVED	NONE		Reserved
4 - 0	PHYADR_MON	R/W	0h	PHY address whose link status is monitored

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4.10.77 CPSW_SS_P0_CONTROL_REG Registers

4.10.77.1 CPSW_SS_P0_CONTROL_REG Register (Offset = 4h) [reset = 0h]

Short Description: p0_control_reg

Long Description:

Return to Summary Table

Table 4-1038. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0004h

Figure 4-383. P0_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												CUT_THRU_MODE_ETH	RX_REMAP_DSCP_V6	RX_REMAP_DSCP_V4	RX_REMAP_VLAN
NONE												R/W	R/W	R/W	R/W
0												0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_ECC_ERR_EN	TX_ECC_ERR_EN	RESERVED											DSCP_IPV6_EN	DSCP_IPV4_EN	RX_CHECKSUM_EN
R/W	R/W	NONE											R/W	R/W	R/W
0	0	0											0	0	0

Access Types Legend

Table 4-1039. P0_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19	CUT_THRU_MODE_ETH	R/W	0h	Port 0 Cut-Thru Mode Ethernet
18	RX_REMAP_DSCP_V6	R/W	0h	Port 0 Remap DSCP_V6 Enable
17	RX_REMAP_DSCP_V4	R/W	0h	Port 0 Remap DSCP_V4 Enable
16	RX_REMAP_VLAN	R/W	0h	Port 0 Remap VLAN Enable
15	RX_ECC_ERR_EN	R/W	0h	Port 0 Receive ECC Error Enable
14	TX_ECC_ERR_EN	R/W	0h	Port 0 Transmit ECC Error Enable
	RESERVED	NONE		Reserved
2	DSCP_IPV6_EN	R/W	0h	Port 0 IPv6 DSCP enable
1	DSCP_IPV4_EN	R/W	0h	Port 0 IPv4 DSCP enable
0	RX_CHECKSUM_EN	R/W	0h	Port 0 Receive Checksum Enable

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4.10.78 CPSW_SS_P0_FLOW_ID_OFFSET_REG Registers

4.10.78.1 CPSW_SS_P0_FLOW_ID_OFFSET_REG Register (Offset = 8h) [reset = 0h]

Short Description: p0_flow_id_offset_reg

Long Description:

Return to Summary Table

Table 4-1040. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0008h

Figure 4-384. P0_FLOW_ID_OFFSET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		VALUE													
NONE		R/W													
0		0													

Access Types Legend

Table 4-1041. P0_FLOW_ID_OFFSET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
13 - 0	VALUE	R/W	0h	This value is added to the thread/Flow_ID in CPPI transmit PSI Info Word 0

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4.10.79 CPSW_SS_P0_BLK_CNT_REG Registers

4.10.79.1 CPSW_SS_P0_BLK_CNT_REG Register (Offset = 10h) [reset = 1h]

Short Description: p0_blk_cnt_reg

Long Description:

Return to Summary Table

Table 4-1042. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0010h

Figure 4-385. P0_BLK_CNT_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			TX_BLK_CNT					RESERVED		RX_BLK_CNT					
NONE			R					NONE		R					
0			0					0		1					

Access Types Legend

Table 4-1043. P0_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
12 - 8	TX_BLK_CNT	R	0h	Port 0 Transmit Block Count Usage
	RESERVED	NONE		Reserved
5 - 0	RX_BLK_CNT	R	1h	Port 0 Receive Block Count Usage

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4.10.80 CPSW_SS_P0_PORT_VLAN_REG Registers

4.10.80.1 CPSW_SS_P0_PORT_VLAN_REG Register (Offset = 14h) [reset = 0h]

Short Description: p0_port_vlan_reg

Long Description:

Return to Summary Table

Table 4-1044. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0014h

Figure 4-386. P0_PORT_VLAN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT_PRI			PORT_CFI	PORT_VID											
R/W			R/W	R/W											
0			0	0											

Access Types Legend

Table 4-1045. P0_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11 - 0	PORT_VID	R/W	0h	Port VLAN ID

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4.10.81 CPSW_SS_P0_TX_PRI_MAP_REG Registers

4.10.81.1 CPSW_SS_P0_TX_PRI_MAP_REG Register (Offset = 18h) [reset = 76543210h]

Short Description: p0_tx_pri_map_reg

Long Description:

Return to Summary Table

Table 4-1046. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0018h

Figure 4-387. P0_TX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PRI7		RESERVED		PRI6		RESERVED		PRI5		RESERVED		PRI4	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		111		0		110		0		101		0		100	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PRI3		RESERVED		PRI2		RESERVED		PRI1		RESERVED		PRI0	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		11		0		10		0		1		0		0	

Access Types Legend

Table 4-1047. P0_TX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
30 - 28	PRI7	R/W	6Fh	Priority 7
	RESERVED	NONE		Reserved
26 - 24	PRI6	R/W	6Eh	Priority 6
	RESERVED	NONE		Reserved
22 - 20	PRI5	R/W	65h	Priority 5
	RESERVED	NONE		Reserved
18 - 16	PRI4	R/W	64h	Priority 4
	RESERVED	NONE		Reserved
14 - 12	PRI3	R/W	Bh	Priority 3
	RESERVED	NONE		Reserved
10 - 8	PRI2	R/W	Ah	Priority 2
	RESERVED	NONE		Reserved
6 - 4	PRI1	R/W	1h	Priority 1
	RESERVED	NONE		Reserved
2 - 0	PRI0	R/W	0h	Priority 0

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4.10.82 CPSW_SS_P0_PRI_CTL_REG Registers

4.10.82.1 CPSW_SS_P0_PRI_CTL_REG Register (Offset = 1Ch) [reset = 0h]

Short Description: p0_pri_ctl_reg

Long Description:

Return to Summary Table

Table 4-1048. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 001Ch

Figure 4-388. P0_PRI_CTL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								RX_FLOW_PRI							
NONE								R/W							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							RX_PTYPE	RESERVED							
NONE							R/W	NONE							
0							0	0							

Access Types Legend

Table 4-1049. P0_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
23 - 16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority)
	RESERVED	NONE		Reserved
8	RX_PTYPE	R/W	0h	Receive Priority Type
	RESERVED	NONE		Reserved

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4.10.83 CPSW_SS_P0_RX_PRI_MAP_REG Registers

4.10.83.1 CPSW_SS_P0_RX_PRI_MAP_REG Register (Offset = 20h) [reset = 76543210h]

Short Description: p0_rx_pri_map_reg

Long Description:

Return to Summary Table

Table 4-1050. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0020h

Figure 4-389. P0_RX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PRI7		RESERVED		PRI6		RESERVED		PRI5		RESERVED		PRI4	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		111		0		110		0		101		0		100	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PRI3		RESERVED		PRI2		RESERVED		PRI1		RESERVED		PRI0	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		11		0		10		0		1		0		0	

Access Types Legend

Table 4-1051. P0_RX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
30 - 28	PRI7	R/W	6Fh	Priority 7
	RESERVED	NONE		Reserved
26 - 24	PRI6	R/W	6Eh	Priority 6
	RESERVED	NONE		Reserved
22 - 20	PRI5	R/W	65h	Priority 5
	RESERVED	NONE		Reserved
18 - 16	PRI4	R/W	64h	Priority 4
	RESERVED	NONE		Reserved
14 - 12	PRI3	R/W	Bh	Priority 3
	RESERVED	NONE		Reserved
10 - 8	PRI2	R/W	Ah	Priority 2
	RESERVED	NONE		Reserved
6 - 4	PRI1	R/W	1h	Priority 1
	RESERVED	NONE		Reserved
2 - 0	PRI0	R/W	0h	Priority 0

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4.10.84 CPSW_SS_P0_RX_MAXLEN_REG Registers

4.10.84.1 CPSW_SS_P0_RX_MAXLEN_REG Register (Offset = 24h) [reset = 5eeh]

Short Description: p0_rx_maxlen_reg

Long Description:

Return to Summary Table

Table 4-1052. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0024h

Figure 4-390. P0_RX_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX_MAXLEN													
NONE		R/W													
0		10111101110													

Access Types Legend

Table 4-1053. P0_RX_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
13 - 0	RX_MAXLEN	R/W	25AAB28B6h	Rx Maximum Frame Length

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4.10.85 CPSW_SS_P0_TX_BLKS_PRI_REG Registers

4.10.85.1 CPSW_SS_P0_TX_BLKS_PRI_REG Register (Offset = 28h) [reset = 1245678h]

Short Description: p0_tx_blks_pri_reg

Long Description:

Return to Summary Table

Table 4-1054. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0028h

Figure 4-391. P0_TX_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI7				PRI6				PRI5				PRI4			
R/W				R/W				R/W				R/W			
0				1				10				100			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI3				PRI2				PRI1				PRI0			
R/W				R/W				R/W				R/W			
101				110				111				1000			

Access Types Legend

Table 4-1055. P0_TX_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 28	PRI7	R/W	0h	Priority 7 Port Transmit Blocks
27 - 24	PRI6	R/W	1h	Priority 6 Port Transmit Blocks
23 - 20	PRI5	R/W	Ah	Priority 5 Port Transmit Blocks
19 - 16	PRI4	R/W	64h	Priority 4 Port Transmit Blocks
15 - 12	PRI3	R/W	65h	Priority 3 Port Transmit Blocks
11 - 8	PRI2	R/W	6Eh	Priority 2 Port Transmit Blocks
7 - 4	PRI1	R/W	6Fh	Priority 1 Port Transmit Blocks
3 - 0	PRI0	R/W	3E8h	Priority 0 Port Transmit Blocks

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4.10.86 CPSW_SS_P0_IDLE2LPI_REG Registers

4.10.86.1 CPSW_SS_P0_IDLE2LPI_REG Register (Offset = 30h) [reset = 0h]

Short Description: p0_idle2lpi_reg

Long Description:

Return to Summary Table

Table 4-1056. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0030h

Figure 4-392. P0_IDLE2LPI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								COUNT							
NONE								R/W							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1057. P0_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
23 - 0	COUNT	R/W	0h	Port 0 EEE Idle to LPI counter load value

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4.10.87 CPSW_SS_P0_LPI2WAKE_REG Registers

4.10.87.1 CPSW_SS_P0_LPI2WAKE_REG Register (Offset = 34h) [reset = 0h]

Short Description: p0_lpi2wake_reg

Long Description:

Return to Summary Table

Table 4-1058. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0034h

Figure 4-393. P0_LPI2WAKE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								COUNT							
NONE								R/W							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1059. P0_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
23 - 0	COUNT	R/W	0h	Port 0 EEE LPI to wake counter load value

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4.10.88 CPSW_SS_P0_EEE_STATUS_REG Registers

4.10.88.1 CPSW_SS_P0_EEE_STATUS_REG Register (Offset = 38h) [reset = 60h]

Short Description: p0_eee_status_reg

Long Description:

Return to Summary Table

Table 4-1060. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0038h

Figure 4-394. P0_EEE_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
NONE									R	R	R	R	R	R	R
0									1	1	0	0	0	0	0

Access Types Legend

Table 4-1061. P0_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TX_FIFO_EMPTY	R	1h	CPPI port 0 transmit FIFO (switch egress) is empty - contains no packets
5	RX_FIFO_EMPTY	R	1h	CPPI port 0 receive FIFO (switch ingress) is empty - contains no packets
4	TX_FIFO_HOLD	R	0h	CPPI port 0 transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time
3	TX_WAKE	R	0h	CPPI port 0 transmit wakeup - asserted in the transmit LPI2WAKE count time
2	TX_LPI	R	0h	CPPI port 0 transmit LPI state - asserted when the port 0 transmit is in the LPI state
1	RX_LPI	R	0h	CPPI port 0 receive LPI state - asserted when the port 0 receive is in the LPI state
0	WAIT_IDLE2LPI	R	0h	CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time

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4.10.89 CPSW_SS_P0_FIFO_STATUS_REG Registers

4.10.89.1 CPSW_SS_P0_FIFO_STATUS_REG Register (Offset = 50h) [reset = 0h]

Short Description: p0_fifo_status_reg

Long Description:

Return to Summary Table

Table 4-1062. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0050h

Figure 4-395. P0_FIFO_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TX_PRI_ACTIVE							
NONE								R							
0								0							

Access Types Legend

Table 4-1063. P0_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	TX_PRI_ACTIVE	R	0h	Port 0 FIFO Status

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4.10.90 CPSW_SS_P0_RX_DSCP_MAP_REG Registers

4.10.90.1 CPSW_SS_P0_RX_DSCP_MAP_REG Register (Offset = 120h) [reset = 0h]

Short Description: p0_rx_dscp_map_reg

Long Description:

Return to Summary Table

Table 4-1064. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0120h

Figure 4-396. P0_RX_DSCP_MAP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PRI7		RESERVED		PRI6		RESERVED		PRI5		RESERVED		PRI4	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		0		0		0		0		0		0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PRI3		RESERVED		PRI2		RESERVED		PRI1		RESERVED		PRI0	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		0		0		0		0		0		0		0	

Access Types Legend

Table 4-1065. P0_RX_DSCP_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
30 - 28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
	RESERVED	NONE		Reserved
26 - 24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
	RESERVED	NONE		Reserved
22 - 20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
	RESERVED	NONE		Reserved
18 - 16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
	RESERVED	NONE		Reserved
14 - 12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
	RESERVED	NONE		Reserved
10 - 8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
	RESERVED	NONE		Reserved
6 - 4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority
	RESERVED	NONE		Reserved
2 - 0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

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4.10.91 CPSW_SS_P0_PRI_CIR_REG Registers

4.10.91.1 CPSW_SS_P0_PRI_CIR_REG Register (Offset = 140h) [reset = 0h]

Short Description: p0_pri_cir_reg

Long Description:

Return to Summary Table

Table 4-1066. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0140h

Figure 4-397. P0_PRI_CIR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI_CIR											
NONE				R/W											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI_CIR															
R/W															
0															

Access Types Legend

Table 4-1067. P0_PRI_CIR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27 - 0	PRI_CIR	R/W	0h	Priority N CIR

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4.10.92 CPSW_SS_P0_PRI_EIR_REG Registers

4.10.92.1 CPSW_SS_P0_PRI_EIR_REG Register (Offset = 160h) [reset = 0h]

Short Description: p0_pri_eir_reg

Long Description:

Return to Summary Table

Table 4-1068. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0160h

Figure 4-398. P0_PRI_EIR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI_EIR											
NONE				R/W											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI_EIR															
R/W															
0															

Access Types Legend

Table 4-1069. P0_PRI_EIR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27 - 0	PRI_EIR	R/W	0h	Priority N EIR

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4.10.93 CPSW_SS_P0_TX_D_THRESH_SET_L_REG Registers

4.10.93.1 CPSW_SS_P0_TX_D_THRESH_SET_L_REG Register (Offset = 180h) [reset = 1f1f1f1fh]

Short Description: p0_tx_d_thresh_set_l_reg

Long Description:

Return to Summary Table

Table 4-1070. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0180h

Figure 4-399. P0_TX_D_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
0			11111					0			11111				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
0			11111					0			11111				

Access Types Legend

Table 4-1071. P0_TX_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI3	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 3
	RESERVED	NONE		Reserved
20 - 16	PRI2	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 2
	RESERVED	NONE		Reserved
12 - 8	PRI1	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 1
	RESERVED	NONE		Reserved
4 - 0	PRI0	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 0

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4.10.94 CPSW_SS_P0_TX_D_THRESH_SET_H_REG Registers

4.10.94.1 CPSW_SS_P0_TX_D_THRESH_SET_H_REG Register (Offset = 184h) [reset = 1f1f1f1fh]

Short Description: p0_tx_d_thresh_set_h_reg

Long Description:

Return to Summary Table

Table 4-1072. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0184h

Figure 4-400. P0_TX_D_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
0			11111					0			11111				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
0			11111					0			11111				

Access Types Legend

Table 4-1073. P0_TX_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI7	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 7
	RESERVED	NONE		Reserved
20 - 16	PRI6	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 6
	RESERVED	NONE		Reserved
12 - 8	PRI5	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 5
	RESERVED	NONE		Reserved
4 - 0	PRI4	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 4

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4.10.95 CPSW_SS_P0_TX_D_THRESH_CLR_L_REG Registers

4.10.95.1 CPSW_SS_P0_TX_D_THRESH_CLR_L_REG Register (Offset = 188h) [reset = 0h]

Short Description: p0_tx_d_thresh_clr_l_reg

Long Description:

Return to Summary Table

Table 4-1074. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0188h

Figure 4-401. P0_TX_D_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
0			0					0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
0			0					0			0				

Access Types Legend

Table 4-1075. P0_TX_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
	RESERVED	NONE		Reserved
20 - 16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
	RESERVED	NONE		Reserved
12 - 8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
	RESERVED	NONE		Reserved
4 - 0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

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4.10.96 CPSW_SS_P0_TX_D_THRESH_CLR_H_REG Registers

4.10.96.1 CPSW_SS_P0_TX_D_THRESH_CLR_H_REG Register (Offset = 18Ch) [reset = 0h]

Short Description: p0_tx_d_thresh_clr_h_reg

Long Description:

Return to Summary Table

Table 4-1076. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 018Ch

Figure 4-402. P0_TX_D_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
0			0					0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
0			0					0			0				

Access Types Legend

Table 4-1077. P0_TX_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
	RESERVED	NONE		Reserved
20 - 16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
	RESERVED	NONE		Reserved
12 - 8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
	RESERVED	NONE		Reserved
4 - 0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

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4.10.97 CPSW_SS_P0_TX_G_BUF_THRESH_SET_L_REG Registers

4.10.97.1 CPSW_SS_P0_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 190h) [reset = 1f1f1f1fh]

Short Description: p0_tx_g_buf_thresh_set_l_reg

Long Description:

Return to Summary Table

Table 4-1078. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0190h

Figure 4-403. P0_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
0			11111					0			11111				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
0			11111					0			11111				

Access Types Legend

Table 4-1079. P0_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI3	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 3
	RESERVED	NONE		Reserved
20 - 16	PRI2	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 2
	RESERVED	NONE		Reserved
12 - 8	PRI1	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 1
	RESERVED	NONE		Reserved
4 - 0	PRI0	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 0

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4.10.98 CPSW_SS_P0_TX_G_BUF_THRESH_SET_H_REG Registers

4.10.98.1 CPSW_SS_P0_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 194h) [reset = 1f1f1f1fh]

Short Description: p0_tx_g_buf_thresh_set_h_reg

Long Description:

Return to Summary Table

Table 4-1080. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0194h

Figure 4-404. P0_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
0			11111					0			11111				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
0			11111					0			11111				

Access Types Legend

Table 4-1081. P0_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI7	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 7
	RESERVED	NONE		Reserved
20 - 16	PRI6	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 6
	RESERVED	NONE		Reserved
12 - 8	PRI5	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 5
	RESERVED	NONE		Reserved
4 - 0	PRI4	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 4

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4.10.99 CPSW_SS_P0_TX_G_BUF_THRESH_CLR_L_REG Registers

4.10.99.1 CPSW_SS_P0_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 198h) [reset = 0h]

Short Description: p0_tx_g_buf_thresh_clr_l_reg

Long Description:

Return to Summary Table

Table 4-1082. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0198h

Figure 4-405. P0_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
0			0					0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
0			0					0			0				

Access Types Legend

Table 4-1083. P0_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
	RESERVED	NONE		Reserved
20 - 16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
	RESERVED	NONE		Reserved
12 - 8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
	RESERVED	NONE		Reserved
4 - 0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

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4.10.100 CPSW_SS_P0_TX_G_BUF_THRESH_CLR_H_REG Registers

4.10.100.1 CPSW_SS_P0_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 19Ch) [reset = 0h]

Short Description: p0_tx_g_buf_thresh_clr_h_reg

Long Description:

Return to Summary Table

Table 4-1084. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 019Ch

Figure 4-406. P0_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
0			0					0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
0			0					0			0				

Access Types Legend

Table 4-1085. P0_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
	RESERVED	NONE		Reserved
20 - 16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
	RESERVED	NONE		Reserved
12 - 8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
	RESERVED	NONE		Reserved
4 - 0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

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4.10.101 CPSW_SS_P0_SRC_ID_A_REG Registers

4.10.101.1 CPSW_SS_P0_SRC_ID_A_REG Register (Offset = 300h) [reset = 4030201h]

Short Description: p0_src_id_a_reg

Long Description:

Return to Summary Table

Table 4-1086. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0300h

Figure 4-407. P0_SRC_ID_A_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PORT4								PORT3							
R/W								R/W							
100								11							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT2								PORT1							
R/W								R/W							
10								1							

Access Types Legend

Table 4-1087. P0_SRC_ID_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	PORT4	R/W	64h	Port 4 CPPI Info Word0 Source ID Value
23 - 16	PORT3	R/W	Bh	Port 3 CPPI Info Word0 Source ID Value
15 - 8	PORT2	R/W	Ah	Port 2 CPPI Info Word0 Source ID Value
7 - 0	PORT1	R/W	1h	Port 1 CPPI Info Word0 Source ID Value

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4.10.102 CPSW_SS_P0_SRC_ID_B_REG Registers

4.10.102.1 CPSW_SS_P0_SRC_ID_B_REG Register (Offset = 304h) [reset = 8070605h]

Short Description: p0_src_id_b_reg

Long Description:

Return to Summary Table

Table 4-1088. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0304h

Figure 4-408. P0_SRC_ID_B_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PORT8								PORT7							
R/W								R/W							
1000								111							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT6								PORT5							
R/W								R/W							
110								101							

Access Types Legend

Table 4-1089. P0_SRC_ID_B_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	PORT8	R/W	3E8h	Port 8 CPPI Info Word0 Source ID Value
23 - 16	PORT7	R/W	6Fh	Port 7 CPPI Info Word0 Source ID Value
15 - 8	PORT6	R/W	6Eh	Port 6 CPPI Info Word0 Source ID Value
7 - 0	PORT5	R/W	65h	Port 5 CPPI Info Word0 Source ID Value

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4.10.103 CPSW_SS_P0_HOST_BLKS_PRI_REG Registers

4.10.103.1 CPSW_SS_P0_HOST_BLKS_PRI_REG Register (Offset = 320h) [reset = 0h]

Short Description: p0_host_blks_pri_reg

Long Description:

Return to Summary Table

Table 4-1090. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0320h

Figure 4-409. P0_HOST_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI7				PRI6				PRI5				PRI4			
R/W				R/W				R/W				R/W			
0				0				0				0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI3				PRI2				PRI1				PRI0			
R/W				R/W				R/W				R/W			
0				0				0				0			

Access Types Legend

Table 4-1091. P0_HOST_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 28	PRI7	R/W	0h	Priority 7 Host Blocks
27 - 24	PRI6	R/W	0h	Priority 6 Host Blocks
23 - 20	PRI5	R/W	0h	Priority 5 Host Blocks
19 - 16	PRI4	R/W	0h	Priority 4 Host Blocks
15 - 12	PRI3	R/W	0h	Priority 3 Host Blocks
11 - 8	PRI2	R/W	0h	Priority 2 Host Blocks
7 - 4	PRI1	R/W	0h	Priority 1 Host Blocks
3 - 0	PRI0	R/W	0h	Priority 0 Host Blocks

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4.10.104 CPSW_SS_PN_RESERVED_REG Registers

4.10.104.1 CPSW_SS_PN_RESERVED_REG Register (Offset = 0h) [reset = 0h]

Short Description: pn_reserved_reg

Long Description:

Return to Summary Table

Table 4-1092. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0000h

Figure 4-410. PN_RESERVED_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R															
0															

Access Types Legend

Table 4-1093. PN_RESERVED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED	R		Reserved register for memory map alignment

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4.10.105 CPSW_SS_PN_CONTROL_REG Registers

4.10.105.1 CPSW_SS_PN_CONTROL_REG Register (Offset = 4h) [reset = 0h]

Short Description: pn_control_reg

Long Description:

Return to Summary Table

Table 4-1094. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0004h

Figure 4-411. PN_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														EST_PORT_EN	IET_PORT_EN
NONE														R/W	R/W
0														0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_ECC_ERR_EN	TX_ECC_ERR_EN	TX_CUT_IET_HOLD_DIS	TX_LPI_CLKSTOP_EN	RESERVED									DSCP_IPV6_EN	DSCP_IPV4_EN	RESERVED
R/W	R/W	R/W	R/W	NONE									R/W	R/W	NONE
0	0	0	0	0									0	0	0

Access Types Legend

Table 4-1095. PN_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	EST_PORT_EN	R/W	0h	EST Port Enable
16	IET_PORT_EN	R/W	0h	IET Port Enable
15	RX_ECC_ERR_EN	R/W	0h	Port 0 Receive ECC Error Enable
14	TX_ECC_ERR_EN	R/W	0h	Port 0 Transmit ECC Error Enable
13	TX_CUT_IET_HOLD_DIS	R/W	0h	Cut-Thru IET Prempt Hold Disable
12	TX_LPI_CLKSTOP_EN	R/W	0h	Transmit LPI clockstop enable
	RESERVED	NONE		Reserved
2	DSCP_IPV6_EN	R/W	0h	IPv6 DSCP enable
1	DSCP_IPV4_EN	R/W	0h	IPv4 DSCP enable
	RESERVED	NONE		Reserved

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4.10.106 CPSW_SS_PN_MAX_BLKS_REG Registers

4.10.106.1 CPSW_SS_PN_MAX_BLKS_REG Register (Offset = 8h) [reset = 1004h]

Short Description: pn_max_blks_reg

Long Description:

Return to Summary Table

Table 4-1096. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0008h

Figure 4-412. PN_MAX_BLKS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_MAX_BLKS								RX_MAX_BLKS							
R/W								R/W							
10000								100							

Access Types Legend

Table 4-1097. PN_MAX_BLKS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 8	TX_MAX_BLKS	R/W	2710h	Transmit FIFO maximum blocks
7 - 0	RX_MAX_BLKS	R/W	64h	Receive FIFO maximum blocks

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4.10.107 CPSW_SS_PN_BLK_CNT_REG Registers

4.10.107.1 CPSW_SS_PN_BLK_CNT_REG Register (Offset = 10h) [reset = 1h]

Short Description: pn_blk_cnt_reg

Long Description:

Return to Summary Table

Table 4-1098. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0010h

Figure 4-413. PN_BLK_CNT_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										RX_BLK_CNT_P					
NONE										R					
0										0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			TX_BLK_CNT					RESERVED		RX_BLK_CNT_E					
NONE			R					NONE		R					
0			0					0		1					

Access Types Legend

Table 4-1099. PN_BLK_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
21 - 16	RX_BLK_CNT_P	R	0h	Receive Prempt Queue Block Count Usage
	RESERVED	NONE		Reserved
12 - 8	TX_BLK_CNT	R	0h	Transmit Block Count Usage
	RESERVED	NONE		Reserved
5 - 0	RX_BLK_CNT_E	R	1h	Receive Block Count Usage

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4.10.108 CPSW_SS_PN_PORT_VLAN_REG Registers

4.10.108.1 CPSW_SS_PN_PORT_VLAN_REG Register (Offset = 14h) [reset = 0h]

Short Description: pn_port_vlan_reg

Long Description:

Return to Summary Table

Table 4-1100. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0014h

Figure 4-414. PN_PORT_VLAN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT_PRI			PORT_CFI	PORT_VID											
R/W			R/W	R/W											
0			0	0											

Access Types Legend

Table 4-1101. PN_PORT_VLAN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 13	PORT_PRI	R/W	0h	Port VLAN Priority
12	PORT_CFI	R/W	0h	Port CFI bit
11 - 0	PORT_VID	R/W	0h	Port VLAN ID

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4.10.109 CPSW_SS_PN_TX_PRI_MAP_REG Registers

4.10.109.1 CPSW_SS_PN_TX_PRI_MAP_REG Register (Offset = 18h) [reset = 76543210h]

Short Description: pn_tx_pri_map_reg

Long Description:

Return to Summary Table

Table 4-1102. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0018h

Figure 4-415. PN_TX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PRI7		RESERVED		PRI6		RESERVED		PRI5		RESERVED		PRI4	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		111		0		110		0		101		0		100	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PRI3		RESERVED		PRI2		RESERVED		PRI1		RESERVED		PRI0	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		11		0		10		0		1		0		0	

Access Types Legend

Table 4-1103. PN_TX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
30 - 28	PRI7	R/W	6Fh	Priority 7
	RESERVED	NONE		Reserved
26 - 24	PRI6	R/W	6Eh	Priority 6
	RESERVED	NONE		Reserved
22 - 20	PRI5	R/W	65h	Priority 5
	RESERVED	NONE		Reserved
18 - 16	PRI4	R/W	64h	Priority 4
	RESERVED	NONE		Reserved
14 - 12	PRI3	R/W	Bh	Priority 3
	RESERVED	NONE		Reserved
10 - 8	PRI2	R/W	Ah	Priority 2
	RESERVED	NONE		Reserved
6 - 4	PRI1	R/W	1h	Priority 1
	RESERVED	NONE		Reserved
2 - 0	PRI0	R/W	0h	Priority 0

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4.10.110 CPSW_SS_PN_PRI_CTL_REG Registers

4.10.110.1 CPSW_SS_PN_PRI_CTL_REG Register (Offset = 1Ch) [reset = 9000h]

Short Description: pn_pri_ctl_reg

Long Description:

Return to Summary Table

Table 4-1104. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 001Ch

Figure 4-416. PN_PRI_CTL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TX_FLOW_PRI								RX_FLOW_PRI							
R/W								R/W							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_HOST_BLKS_REM				RESERVED											
R/W				NONE											
1001				0											

Access Types Legend

Table 4-1105. PN_PRI_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	TX_FLOW_PRI	R/W	0h	Transmit Priority Based Flow Control Enable (per priority)
23 - 16	RX_FLOW_PRI	R/W	0h	Receive Priority Based Flow Control Enable (per priority)
15 - 12	TX_HOST_BLKS_REM	R/W	3E9h	Transmit FIFO Blocks that must be free before a non rate-limited CPPI Port 0 receive thread can begin sending a packet
	RESERVED	NONE		Reserved

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4.10.111 CPSW_SS_PN_RX_PRI_MAP_REG Registers

4.10.111.1 CPSW_SS_PN_RX_PRI_MAP_REG Register (Offset = 20h) [reset = 76543210h]

Short Description: pn_rx_pri_map_reg

Long Description:

Return to Summary Table

Table 4-1106. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0020h

Figure 4-417. PN_RX_PRI_MAP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PRI7		RESERVED		PRI6		RESERVED		PRI5		RESERVED		PRI4	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		111		0		110		0		101		0		100	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PRI3		RESERVED		PRI2		RESERVED		PRI1		RESERVED		PRI0	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		11		0		10		0		1		0		0	

Access Types Legend

Table 4-1107. PN_RX_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
30 - 28	PRI7	R/W	6Fh	Priority 7
	RESERVED	NONE		Reserved
26 - 24	PRI6	R/W	6Eh	Priority 6
	RESERVED	NONE		Reserved
22 - 20	PRI5	R/W	65h	Priority 5
	RESERVED	NONE		Reserved
18 - 16	PRI4	R/W	64h	Priority 4
	RESERVED	NONE		Reserved
14 - 12	PRI3	R/W	Bh	Priority 3
	RESERVED	NONE		Reserved
10 - 8	PRI2	R/W	Ah	Priority 2
	RESERVED	NONE		Reserved
6 - 4	PRI1	R/W	1h	Priority 1
	RESERVED	NONE		Reserved
2 - 0	PRI0	R/W	0h	Priority 0

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4.10.112 CPSW_SS_PN_RX_MAXLEN_REG Registers

4.10.112.1 CPSW_SS_PN_RX_MAXLEN_REG Register (Offset = 24h) [reset = 5eeh]

Short Description: pn_rx_maxlen_reg

Long Description:

Return to Summary Table

Table 4-1108. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0024h

Figure 4-418. PN_RX_MAXLEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX_MAXLEN													
NONE		R/W													
0		10111101110													

Access Types Legend

Table 4-1109. PN_RX_MAXLEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
13 - 0	RX_MAXLEN	R/W	25AAB28B6h	Rx Maximum Frame Length

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4.10.113 CPSW_SS_PN_TX_BLKS_PRI_REG Registers

4.10.113.1 CPSW_SS_PN_TX_BLKS_PRI_REG Register (Offset = 28h) [reset = 1245678h]

Short Description: pn_tx_blks_pri_reg

Long Description:

Return to Summary Table

Table 4-1110. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0028h

Figure 4-419. PN_TX_BLKS_PRI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI7				PRI6				PRI5				PRI4			
R/W				R/W				R/W				R/W			
0				1				10				100			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI3				PRI2				PRI1				PRI0			
R/W				R/W				R/W				R/W			
101				110				111				1000			

Access Types Legend

Table 4-1111. PN_TX_BLKS_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 28	PRI7	R/W	0h	Priority 7 Port Transmit Blocks
27 - 24	PRI6	R/W	1h	Priority 6 Port Transmit Blocks
23 - 20	PRI5	R/W	Ah	Priority 5 Port Transmit Blocks
19 - 16	PRI4	R/W	64h	Priority 4 Port Transmit Blocks
15 - 12	PRI3	R/W	65h	Priority 3 Port Transmit Blocks
11 - 8	PRI2	R/W	6Eh	Priority 2 Port Transmit Blocks
7 - 4	PRI1	R/W	6Fh	Priority 1 Port Transmit Blocks
3 - 0	PRI0	R/W	3E8h	Priority 0 Port Transmit Blocks

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4.10.114 CPSW_SS_PN_IDLE2LPI_REG Registers

4.10.114.1 CPSW_SS_PN_IDLE2LPI_REG Register (Offset = 30h) [reset = 0h]

Short Description: pn_idle2lpi_reg

Long Description:

Return to Summary Table

Table 4-1112. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0030h

Figure 4-420. PN_IDLE2LPI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								COUNT							
NONE								R/W							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1113. PN_IDLE2LPI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
23 - 0	COUNT	R/W	0h	EEE Idle to LPI counter load value

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4.10.115 CPSW_SS_PN_LPI2WAKE_REG Registers

4.10.115.1 CPSW_SS_PN_LPI2WAKE_REG Register (Offset = 34h) [reset = 0h]

Short Description: pn_lpi2wake_reg

Long Description:

Return to Summary Table

Table 4-1114. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0034h

Figure 4-421. PN_LPI2WAKE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								COUNT							
NONE								R/W							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1115. PN_LPI2WAKE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
23 - 0	COUNT	R/W	0h	EEE LPI to wake counter load value

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4.10.116 CPSW_SS_PN_EEE_STATUS_REG Registers

4.10.116.1 CPSW_SS_PN_EEE_STATUS_REG Register (Offset = 38h) [reset = 62h]

Short Description: pn_eee_status_reg

Long Description:

Return to Summary Table

Table 4-1116. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0038h

Figure 4-422. PN_EEE_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									TX_FIFO_EMPTY	RX_FIFO_EMPTY	TX_FIFO_HOLD	TX_WAKE	TX_LPI	RX_LPI	WAIT_IDLE2LPI
NONE									R	R	R	R	R	R	R
0									1	1	0	0	0	1	0

Access Types Legend

Table 4-1117. PN_EEE_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TX_FIFO_EMPTY	R	1h	Transmit FIFO (switch egress) is empty - contains no packets
5	RX_FIFO_EMPTY	R	1h	Receive FIFO (switch ingress) is empty - contains no packets
4	TX_FIFO_HOLD	R	0h	Transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time
3	TX_WAKE	R	0h	Transmit wakeup - asserted in the transmit LPI2WAKE count time
2	TX_LPI	R	0h	Transmit LPI state - asserted when the port 0 transmit is in the LPI state
1	RX_LPI	R	1h	Receive LPI state - asserted when the port 0 receive is in the LPI state
0	WAIT_IDLE2LPI	R	0h	CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time

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4.10.117 CPSW_SS_PN_IET_CONTROL_REG Registers

4.10.117.1 CPSW_SS_PN_IET_CONTROL_REG Register (Offset = 40h) [reset = 8h]

Short Description: pn_iet_control_reg

Long Description:

Return to Summary Table

Table 4-1118. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0040h

Figure 4-423. PN_IET_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MAC_PREMPT							
NONE								R/W							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					MAC_ADDFRAGSIZE			RESERVED				MAC_LINKFAIL	MAC_DISABLEVERIFY	MAC_HOLD	MAC_PENABLE
NONE					R/W			NONE				R/W	R/W	R/W	R/W
0					0			0				1	0	0	0

Access Types Legend

Table 4-1119. PN_IET_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
23 - 16	MAC_PREMPT	R/W	0h	IET MAC Fragment Size
	RESERVED	NONE		Reserved
10 - 8	MAC_ADDFRAGSIZE	R/W	0h	IET MAC Fragment Size
	RESERVED	NONE		Reserved
3	MAC_LINKFAIL	R/W	1h	IET MAC LINK Fail Reset
2	MAC_DISABLEVERIFY	R/W	0h	IET MAC Disable Verify
1	MAC_HOLD	R/W	0h	IET MAC HOLD
0	MAC_PENABLE	R/W	0h	IET MAC Penable

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4.10.118 CPSW_SS_PN_IET_STATUS_REG Registers

4.10.118.1 CPSW_SS_PN_IET_STATUS_REG Register (Offset = 44h) [reset = 0h]

Short Description: pn_iet_status_reg

Long Description:

Return to Summary Table

Table 4-1120. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0044h

Figure 4-424. PN_IET_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												MAC_VERIFY_ERR	MAC_RESPOND_ERR	MAC_VERIFY_FAIL	MAC_VERIFIED
NONE												R	R	R	R
0												0	0	0	0

Access Types Legend

Table 4-1121. PN_IET_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	MAC_VERIFY_ERR	R	0h	IET MAC VERIFY ERROR
2	MAC_RESPOND_ERR	R	0h	IET MAC RESPONSE ERROR
1	MAC_VERIFY_FAIL	R	0h	IET MAC VERIFY FAIL
0	MAC_VERIFIED	R	0h	IET MAC VERIFIED

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4.10.119 CPSW_SS_PN_IET_VERIFY_REG Registers

4.10.119.1 CPSW_SS_PN_IET_VERIFY_REG Register (Offset = 48h) [reset = 1312d0h]

Short Description: pn_iet_verify_reg

Long Description:

Return to Summary Table

Table 4-1122. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0048h

Figure 4-425. PN_IET_VERIFY_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								MAC_VERIFY_CNT							
NONE								R/W							
0								10011000100101101000							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC_VERIFY_CNT															
R/W															
10011000100101101000															

Access Types Legend

Table 4-1123. PN_IET_VERIFY_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
23 - 0	MAC_VERIFY_CNT	R/W	56D4E2B81 4142D9D0h	IET MAC VERIFY COUNT

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4.10.120 CPSW_SS_PN_FIFO_STATUS_REG Registers

4.10.120.1 CPSW_SS_PN_FIFO_STATUS_REG Register (Offset = 50h) [reset = ff00h]

Short Description: pn_fifo_status_reg

Long Description:

Return to Summary Table

Table 4-1124. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0050h

Figure 4-426. PN_FIFO_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED													EST_BUFACT	EST_ADD_ERR	EST_CNT_ERR
NONE													R	R	R
0													0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_E_MAC_ALLOW								TX_PRI_ACTIVE							
R								R							
11111111								0							

Access Types Legend

Table 4-1125. PN_FIFO_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
18	EST_BUFACT	R	0h	Transmit FIFO EST Buffer Active
17	EST_ADD_ERR	R	0h	Transmit FIFO EST Address Error
16	EST_CNT_ERR	R	0h	Transmit FIFO EST Count Error
15 - 8	TX_E_MAC_ALLOW	R	A98AC7h	Transmit FIFO Express Queue Priority Allow
7 - 0	TX_PRI_ACTIVE	R	0h	Transmit FIFO Priority Active

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4.10.121 CPSW_SS_PN_EST_CONTROL_REG Registers

4.10.121.1 CPSW_SS_PN_EST_CONTROL_REG Register (Offset = 60h) [reset = 0h]

Short Description: pn_est_control_reg

Long Description:

Return to Summary Table

Table 4-1126. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0060h

Figure 4-427. PN_EST_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								EST_FILL_MARGIN							
NONE								R/W							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EST_PREMPT_COMP							EST_FILL_EN	EST_TS_PRI			EST_TS_ONEPRI	EST_TS_FIRST	EST_TS_EN	EST_BUFSEL	EST_ONEBUF
R/W							R/W	R/W			R/W	R/W	R/W	R/W	R/W
0							0	0			0	0	0	0	0

Access Types Legend

Table 4-1127. PN_EST_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
25 - 16	EST_FILL_MARGIN	R/W	0h	Transmit FIFO EST Fill Margin
15 - 9	EST_PREMPT_COMP	R/W	0h	Transmit FIFO EST Prempt Comparison Value to Clear wire
8	EST_FILL_EN	R/W	0h	Transmit FIFO EST Fill Enable
7 - 5	EST_TS_PRI	R/W	0h	Transmit FIFO EST TimeStamp Priority
4	EST_TS_ONEPRI	R/W	0h	Transmit FIFO EST TimeStamp One Priority
3	EST_TS_FIRST	R/W	0h	Transmit FIFO EST TimeStamp First Express Packet
2	EST_TS_EN	R/W	0h	Transmit FIFO EST TimeStamp Enable
1	EST_BUFSEL	R/W	0h	Transmit FIFO EST Buffer Select
0	EST_ONEBUF	R/W	0h	Transmit FIFO EST One Buffer

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4.10.122 CPSW_SS_PN_RX_DSCP_MAP_REG Registers

4.10.122.1 CPSW_SS_PN_RX_DSCP_MAP_REG Register (Offset = 120h) [reset = 0h]

Short Description: pn_rx_dscp_map_reg

Long Description:

Return to Summary Table

Table 4-1128. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0120h

Figure 4-428. PN_RX_DSCP_MAP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PRI7		RESERVED		PRI6		RESERVED		PRI5		RESERVED		PRI4	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		0		0		0		0		0		0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PRI3		RESERVED		PRI2		RESERVED		PRI1		RESERVED		PRI0	
NONE		R/W		NONE		R/W		NONE		R/W		NONE		R/W	
0		0		0		0		0		0		0		0	

Access Types Legend

Table 4-1129. PN_RX_DSCP_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
30 - 28	PRI7	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+7 is mapped to this received priority
	RESERVED	NONE		Reserved
26 - 24	PRI6	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+6 is mapped to this received priority
	RESERVED	NONE		Reserved
22 - 20	PRI5	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+5 is mapped to this received priority
	RESERVED	NONE		Reserved
18 - 16	PRI4	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+4 is mapped to this received priority
	RESERVED	NONE		Reserved
14 - 12	PRI3	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+3 is mapped to this received priority
	RESERVED	NONE		Reserved
10 - 8	PRI2	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+2 is mapped to this received priority
	RESERVED	NONE		Reserved
6 - 4	PRI1	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+1 is mapped to this received priority
	RESERVED	NONE		Reserved
2 - 0	PRI0	R/W	0h	A DSCP IPV4/V6 packet TOS of N*8+0 is mapped to this received priority

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4.10.123 CPSW_SS_PN_PRI_CIR_REG Registers

4.10.123.1 CPSW_SS_PN_PRI_CIR_REG Register (Offset = 140h) [reset = 0h]

Short Description: pn_pri_send_reg

Long Description:

Return to Summary Table

Table 4-1130. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0140h

Figure 4-429. PN_PRI_CIR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI_CIR											
NONE				R/W											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI_CIR															
R/W															
0															

Access Types Legend

Table 4-1131. PN_PRI_CIR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27 - 0	PRI_CIR	R/W	0h	Priority N committed information rate

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4.10.124 CPSW_SS_PN_PRI_EIR_REG Registers

4.10.124.1 CPSW_SS_PN_PRI_EIR_REG Register (Offset = 160h) [reset = 0h]

Short Description: pn_pri_idle_reg

Long Description:

Return to Summary Table

Table 4-1132. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0160h

Figure 4-430. PN_PRI_EIR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PRI_EIR											
NONE				R/W											
0				0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI_EIR															
R/W															
0															

Access Types Legend

Table 4-1133. PN_PRI_EIR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27 - 0	PRI_EIR	R/W	0h	Priority N Excess Information Rate count

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4.10.125 CPSW_SS_PN_TX_D_THRESH_SET_L_REG Registers

4.10.125.1 CPSW_SS_PN_TX_D_THRESH_SET_L_REG Register (Offset = 180h) [reset = 1f1f1f1fh]

Short Description: pn_tx_d_thresh_set_l_reg

Long Description:

Return to Summary Table

Table 4-1134. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0180h

Figure 4-431. PN_TX_D_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
0			11111					0			11111				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
0			11111					0			11111				

Access Types Legend

Table 4-1135. PN_TX_D_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI3	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 3
	RESERVED	NONE		Reserved
20 - 16	PRI2	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 2
	RESERVED	NONE		Reserved
12 - 8	PRI1	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 1
	RESERVED	NONE		Reserved
4 - 0	PRI0	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 0

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4.10.126 CPSW_SS_PN_TX_D_THRESH_SET_H_REG Registers

4.10.126.1 CPSW_SS_PN_TX_D_THRESH_SET_H_REG Register (Offset = 184h) [reset = 1f1f1f1fh]

Short Description: pn_tx_d_thresh_set_h_reg

Long Description:

Return to Summary Table

Table 4-1136. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0184h

Figure 4-432. PN_TX_D_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
0			11111					0			11111				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
0			11111					0			11111				

Access Types Legend

Table 4-1137. PN_TX_D_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI7	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 7
	RESERVED	NONE		Reserved
20 - 16	PRI6	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 6
	RESERVED	NONE		Reserved
12 - 8	PRI5	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 5
	RESERVED	NONE		Reserved
4 - 0	PRI4	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 4

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4.10.127 CPSW_SS_PN_TX_D_THRESH_CLR_L_REG Registers

4.10.127.1 CPSW_SS_PN_TX_D_THRESH_CLR_L_REG Register (Offset = 188h) [reset = 0h]

Short Description: pn_tx_d_thresh_clr_l_reg

Long Description:

Return to Summary Table

Table 4-1138. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0188h

Figure 4-433. PN_TX_D_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
0			0					0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
0			0					0			0				

Access Types Legend

Table 4-1139. PN_TX_D_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
	RESERVED	NONE		Reserved
20 - 16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
	RESERVED	NONE		Reserved
12 - 8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
	RESERVED	NONE		Reserved
4 - 0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

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4.10.128 CPSW_SS_PN_TX_D_THRESH_CLR_H_REG Registers

4.10.128.1 CPSW_SS_PN_TX_D_THRESH_CLR_H_REG Register (Offset = 18Ch) [reset = 0h]

Short Description: pn_tx_d_thresh_clr_h_reg

Long Description:

Return to Summary Table

Table 4-1140. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 018Ch

Figure 4-434. PN_TX_D_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
0			0					0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
0			0					0			0				

Access Types Legend

Table 4-1141. PN_TX_D_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
	RESERVED	NONE		Reserved
20 - 16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
	RESERVED	NONE		Reserved
12 - 8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
	RESERVED	NONE		Reserved
4 - 0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

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4.10.129 CPSW_SS_PN_TX_G_BUF_THRESH_SET_L_REG Registers

4.10.129.1 CPSW_SS_PN_TX_G_BUF_THRESH_SET_L_REG Register (Offset = 190h) [reset = 1f1f1f1fh]

Short Description: pn_tx_g_buf_thresh_set_l_reg

Long Description:

Return to Summary Table

Table 4-1142. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0190h

Figure 4-435. PN_TX_G_BUF_THRESH_SET_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
0			11111					0			11111				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
0			11111					0			11111				

Access Types Legend

Table 4-1143. PN_TX_G_BUF_THRESH_SET_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI3	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 3
	RESERVED	NONE		Reserved
20 - 16	PRI2	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 2
	RESERVED	NONE		Reserved
12 - 8	PRI1	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 1
	RESERVED	NONE		Reserved
4 - 0	PRI0	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 0

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4.10.130 CPSW_SS_PN_TX_G_BUF_THRESH_SET_H_REG Registers

4.10.130.1 CPSW_SS_PN_TX_G_BUF_THRESH_SET_H_REG Register (Offset = 194h) [reset = 1f1f1f1fh]

Short Description: pn_tx_g_buf_thresh_set_h_reg

Long Description:

Return to Summary Table

Table 4-1144. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0194h

Figure 4-436. PN_TX_G_BUF_THRESH_SET_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
0			11111					0			11111				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
0			11111					0			11111				

Access Types Legend

Table 4-1145. PN_TX_G_BUF_THRESH_SET_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI7	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 7
	RESERVED	NONE		Reserved
20 - 16	PRI6	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 6
	RESERVED	NONE		Reserved
12 - 8	PRI5	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 5
	RESERVED	NONE		Reserved
4 - 0	PRI4	R/W	2B67h	Port Priority Based Flow Control Threshold Set Value for Priority 4

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4.10.131 CPSW_SS_PN_TX_G_BUF_THRESH_CLR_L_REG Registers

4.10.131.1 CPSW_SS_PN_TX_G_BUF_THRESH_CLR_L_REG Register (Offset = 198h) [reset = 0h]

Short Description: pn_tx_g_buf_thresh_clr_l_reg

Long Description:

Return to Summary Table

Table 4-1146. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0198h

Figure 4-437. PN_TX_G_BUF_THRESH_CLR_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
0			0					0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
0			0					0			0				

Access Types Legend

Table 4-1147. PN_TX_G_BUF_THRESH_CLR_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI3	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 3
	RESERVED	NONE		Reserved
20 - 16	PRI2	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 2
	RESERVED	NONE		Reserved
12 - 8	PRI1	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 1
	RESERVED	NONE		Reserved
4 - 0	PRI0	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 0

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4.10.132 CPSW_SS_PN_TX_G_BUF_THRESH_CLR_H_REG Registers

4.10.132.1 CPSW_SS_PN_TX_G_BUF_THRESH_CLR_H_REG Register (Offset = 19Ch) [reset = 0h]

Short Description: pn_tx_g_buf_thresh_clr_h_reg

Long Description:

Return to Summary Table

Table 4-1148. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 019Ch

Figure 4-438. PN_TX_G_BUF_THRESH_CLR_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
0			0					0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
0			0					0			0				

Access Types Legend

Table 4-1149. PN_TX_G_BUF_THRESH_CLR_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI7	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 7
	RESERVED	NONE		Reserved
20 - 16	PRI6	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 6
	RESERVED	NONE		Reserved
12 - 8	PRI5	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 5
	RESERVED	NONE		Reserved
4 - 0	PRI4	R/W	0h	Port Priority Based Flow Control Threshold Clear Value for Priority 4

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4.10.133 CPSW_SS_PN_TX_D_OFLOW_ADDVAL_L_REG Registers

4.10.133.1 CPSW_SS_PN_TX_D_OFLOW_ADDVAL_L_REG Register (Offset = 300h) [reset = 0h]

Short Description: pn_tx_d_oflow_addval_l_reg

Long Description:

Return to Summary Table

Table 4-1150. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0300h

Figure 4-439. PN_TX_D_OFLOW_ADDVAL_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI3					RESERVED			PRI2				
NONE			R/W					NONE			R/W				
0			0					0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI1					RESERVED			PRI0				
NONE			R/W					NONE			R/W				
0			0					0			0				

Access Types Legend

Table 4-1151. PN_TX_D_OFLOW_ADDVAL_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI3	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 3
	RESERVED	NONE		Reserved
20 - 16	PRI2	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 2
	RESERVED	NONE		Reserved
12 - 8	PRI1	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 1
	RESERVED	NONE		Reserved
4 - 0	PRI0	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 0

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4.10.134 CPSW_SS_PN_TX_D_OFLOW_ADDVAL_H_REG Registers

4.10.134.1 CPSW_SS_PN_TX_D_OFLOW_ADDVAL_H_REG Register (Offset = 304h) [reset = 0h]

Short Description: pn_tx_d_oflow_addval_h_reg

Long Description:

Return to Summary Table

Table 4-1152. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0304h

Figure 4-440. PN_TX_D_OFLOW_ADDVAL_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PRI7					RESERVED			PRI6				
NONE			R/W					NONE			R/W				
0			0					0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			PRI5					RESERVED			PRI4				
NONE			R/W					NONE			R/W				
0			0					0			0				

Access Types Legend

Table 4-1153. PN_TX_D_OFLOW_ADDVAL_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
28 - 24	PRI7	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 7
	RESERVED	NONE		Reserved
20 - 16	PRI6	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 6
	RESERVED	NONE		Reserved
12 - 8	PRI5	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 5
	RESERVED	NONE		Reserved
4 - 0	PRI4	R/W	0h	Port PFC Destination Based Out Flow Add Value for Priority 4

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4.10.135 CPSW_SS_PN_SA_L_REG Registers

4.10.135.1 CPSW_SS_PN_SA_L_REG Register (Offset = 308h) [reset = 0h]

Short Description: pn_sa_l_reg

Long Description:

Return to Summary Table

Table 4-1154. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0308h

Figure 4-441. PN_SA_L_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACSRCADDR_7_0								MACSRCADDR_15_8							
R/W								R/W							
0								0							

Access Types Legend

Table 4-1155. PN_SA_L_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 8	MACSRCADDR_7_0	R/W	0h	Source Address Lower 8 bits
7 - 0	MACSRCADDR_15_8	R/W	0h	Source Address bits 15:8

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4.10.136 CPSW_SS_PN_SA_H_REG Registers

4.10.136.1 CPSW_SS_PN_SA_H_REG Register (Offset = 30Ch) [reset = 0h]

Short Description: pn_sa_h_reg

Long Description:

Return to Summary Table

Table 4-1156. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 030Ch

Figure 4-442. PN_SA_H_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACSRCADDR_23_16								MACSRCADDR_31_24							
R/W								R/W							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACSRCADDR_39_32								MACSRCADDR_47_40							
R/W								R/W							
0								0							

Access Types Legend

Table 4-1157. PN_SA_H_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	MACSRCADDR_23_16	R/W	0h	Source Address bits 23:16
23 - 16	MACSRCADDR_31_24	R/W	0h	Source Address bits 31:24
15 - 8	MACSRCADDR_39_32	R/W	0h	Source Address bits 39:32
7 - 0	MACSRCADDR_47_40	R/W	0h	Source Address bits 47:40

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4.10.137 CPSW_SS_PN_TS_CTL_REG Registers

4.10.137.1 CPSW_SS_PN_TS_CTL_REG Register (Offset = 310h) [reset = 0h]

Short Description: pn_ts_ctl_reg

Long Description:

Return to Summary Table

Table 4-1158. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0310h

Figure 4-443. PN_TS_CTL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_MSG_TYPE_EN															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TS_TX_HOST_TS_EN	TS_TX_ANNEX_E_EN	TS_RX_ANNEX_E_EN	TS_LTYPE2_EN	TS_TX_ANNEX_D_EN	TS_TX_VLAN_LTYPE2_EN	TS_TX_VLAN_LTYPE1_EN	TS_TX_ANNEX_F_EN	TS_RX_ANNEX_D_EN	TS_RX_VLAN_LTYPE2_EN	TS_RX_VLAN_LTYPE1_EN	TS_RX_ANNEX_F_EN
NONE				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0				0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1159. PN_TS_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	TS_MSG_TYPE_EN	R/W	0h	Time Sync Message Type Enable
	RESERVED	NONE		Reserved
11	TS_TX_HOST_TS_EN	R/W	0h	Time Sync Transmit Host Time Stamp Enable
10	TS_TX_ANNEX_E_EN	R/W	0h	Time Synce Transmit Annex E Enable
9	TS_RX_ANNEX_E_EN	R/W	0h	Time Synce Receive Annex E Enable
8	TS_LTYPE2_EN	R/W	0h	Time Sync LTYPE 2 enable transmit and receive
7	TS_TX_ANNEX_D_EN	R/W	0h	Time Synce Transmit Annex D Enable
6	TS_TX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 2 enable
5	TS_TX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Transmit VLAN LTYPE 1 enable
4	TS_TX_ANNEX_F_EN	R/W	0h	Time Synce Transmit Annex F Enable
3	TS_RX_ANNEX_D_EN	R/W	0h	Time Synce Receive Annex D Enable
2	TS_RX_VLAN_LTYPE2_EN	R/W	0h	Time Sync Receive VLAN LTYPE 2 enable
1	TS_RX_VLAN_LTYPE1_EN	R/W	0h	Time Sync Receive VLAN LTYPE 1 enable
0	TS_RX_ANNEX_F_EN	R/W	0h	Time Synce Receive Annex F Enable

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4.10.138 CPSW_SS_PN_TS_SEQ_LTYPE_REG Registers

4.10.138.1 CPSW_SS_PN_TS_SEQ_LTYPE_REG Register (Offset = 314h) [reset = 1e0000h]

Short Description: pn_ts_seq_ltype_reg

Long Description:

Return to Summary Table

Table 4-1160. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0314h

Figure 4-444. PN_TS_SEQ_LTYPE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										TS_SEQ_ID_OFFSET					
NONE										R/W					
0										11110					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LTYPE1															
R/W															
0															

Access Types Legend

Table 4-1161. PN_TS_SEQ_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
21 - 16	TS_SEQ_ID_OFFSET	R/W	2B66h	Time Sync Sequence ID Offset
15 - 0	TS_LTYPE1	R/W	0h	Time Sync LTYPE1

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4.10.139 CPSW_SS_PN_TS_VLAN_LTYPE_REG Registers

4.10.139.1 CPSW_SS_PN_TS_VLAN_LTYPE_REG Register (Offset = 318h) [reset = 0h]

Short Description: pn_ts_vlan_ltype_reg

Long Description:

Return to Summary Table

Table 4-1162. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0318h

Figure 4-445. PN_TS_VLAN_LTYPE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_VLAN_LTYPE2															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_VLAN_LTYPE1															
R/W															
0															

Access Types Legend

Table 4-1163. PN_TS_VLAN_LTYPE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	TS_VLAN_LTYPE2	R/W	0h	Time Sync VLAN LTYPE2
15 - 0	TS_VLAN_LTYPE1	R/W	0h	Time Sync VLAN LTYPE1

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4.10.140 CPSW_SS_PN_TS_CTL_LTYPE2_REG Registers

4.10.140.1 CPSW_SS_PN_TS_CTL_LTYPE2_REG Register (Offset = 31Ch) [reset = 0h]

Short Description: pn_ts_ctl_ltype2_reg

Long Description:

Return to Summary Table

Table 4-1164. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 031Ch

Figure 4-446. PN_TS_CTL_LTYPE2_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							TS_UNI_EN	TS_TTL_NONZERO	TS_320	TS_319	TS_132	TS_131	TS_130	TS_129	TS_107
NONE							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0							0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LTYPE2															
R/W															
0															

Access Types Legend

Table 4-1165. PN_TS_CTL_LTYPE2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
24	TS_UNI_EN	R/W	0h	Time Sync Unicast Enable
23	TS_TTL_NONZERO	R/W	0h	Time Sync Time to Live Non-zero Enable
22	TS_320	R/W	0h	Time Sync Destination IP Address 320 Enable
21	TS_319	R/W	0h	Time Sync Destination IP Address 319 Enable
20	TS_132	R/W	0h	Time Sync Destination IP Address 132 Enable
19	TS_131	R/W	0h	Time Sync Destination IP Address 131 Enable
18	TS_130	R/W	0h	Time Sync Destination IP Address 130 Enable
17	TS_129	R/W	0h	Time Sync Destination IP Address 129 Enable
16	TS_107	R/W	0h	Time Sync Destination IP Address 107 Enable
15 - 0	TS_LTYPE2	R/W	0h	Time Sync LTYPE2

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4.10.141 CPSW_SS_PN_TS_CTL2_REG Registers

4.10.141.1 CPSW_SS_PN_TS_CTL2_REG Register (Offset = 320h) [reset = 40000h]

Short Description: pn_ts_ctl2_reg

Long Description:

Return to Summary Table

Table 4-1166. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0320h

Figure 4-447. PN_TS_CTL2_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										TS_DOMAIN_OFFSET					
NONE										R/W					
0										100					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_MCAST_TYPE_EN															
R/W															
0															

Access Types Legend

Table 4-1167. PN_TS_CTL2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
21 - 16	TS_DOMAIN_OFFSET	R/W	64h	Time Sync Domain Offset
15 - 0	TS_MCAST_TYPE_EN	R/W	0h	Time Sync Multicast Destination Address Type Enable

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4.10.142 CPSW_SS_PN_MAC_CONTROL_REG Registers

4.10.142.1 CPSW_SS_PN_MAC_CONTROL_REG Register (Offset = 330h) [reset = 0h]

Short Description: pn_mac_control_reg

Long Description:

Return to Summary Table

Table 4-1168. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0330h

Figure 4-448. PN_MAC_CONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							RX_CMF_EN	RX_CSF_EN	RX_CEF_EN	TX_SHORT_GAP_LIM_EN	EXT_TX_FLOW_EN	EXT_RX_FLOW_EN	EXT_EN	GIG_FORCE	IFCTL_B
NONE							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0							0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFCTL_A	RESERVED		CRC_TYPE	CMD_IDLE	TX_SHORT_GAP_ENABLE	RESERVED		GIG	TX_PACE	GMII_EN	TX_FLOW_EN	RX_FLOW_EN	MTEST	LOOPBACK	FULLDUPLEX
R/W	NONE		R/W	R/W	R/W	NONE		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0		0	0	0	0		0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1169. PN_MAC_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
24	RX_CMF_EN	R/W	0h	RX Copy MAC Control Frames Enable
23	RX_CSF_EN	R/W	0h	RX Copy Short Frames Enable
22	RX_CEF_EN	R/W	0h	RX Copy Error Frames Enable
21	TX_SHORT_GAP_LIM_EN	R/W	0h	Transmit Short Gap Limit Enable
20	EXT_TX_FLOW_EN	R/W	0h	External Transmit Flow Control Enable
19	EXT_RX_FLOW_EN	R/W	0h	External Receive Flow Control Enable
18	EXT_EN	R/W	0h	External Enable
17	GIG_FORCE	R/W	0h	Gigabit Mode Force
16	IFCTL_B	R/W	0h	Interface Control B
15	IFCTL_A	R/W	0h	Interface Control A
	RESERVED	NONE		Reserved
12	CRC_TYPE	R/W	0h	Port CRC Type
11	CMD_IDLE	R/W	0h	Command Idle
10	TX_SHORT_GAP_ENABLE	R/W	0h	Transmit Short Gap Enable
	RESERVED	NONE		Reserved
7	GIG	R/W	0h	Gigabit Mode
6	TX_PACE	R/W	0h	Transmit Pacing Enable
5	GMII_EN	R/W	0h	GMII Enable

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Table 4-1169. PN_MAC_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	TX_FLOW_EN	R/W	0h	Transmit Flow Control Enable
3	RX_FLOW_EN	R/W	0h	Receive Flow Control Enable
2	MTEST	R/W	0h	Manufacturing Test Mode
1	LOOPBACK	R/W	0h	Loop Back Mode
0	FULLDUPLEX	R/W	0h	Full Duplex mode

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4.10.143 CPSW_SS_PN_MAC_STATUS_REG Registers

4.10.143.1 CPSW_SS_PN_MAC_STATUS_REG Register (Offset = 334h) [reset = f0000000h]

Short Description: pn_mac_status_reg

Long Description:

Return to Summary Table

Table 4-1170. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0334h

Figure 4-449. PN_MAC_STATUS_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IDLE	E_IDLE	P_IDLE	MAC_TX_IDLE	TORF	TORF_PRI			TX_PFC_FLOW_ACT							
R	R	R	R	R	R			R							
1	1	1	1	0	0			0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_PFC_FLOW_ACT								RESERVED	EXT_RX_FLOW_EN	EXT_TX_FLOW_EN	EXT_GIG	EXT_FULLDUPLEX	RESERVED	RX_FLOW_ACT	TX_FLOW_ACT
R								NONE	R	R	R	R	NONE	R	R
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1171. PN_MAC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IDLE	R	1h	cpxmac_sl IDLE
30	E_IDLE	R	1h	Express cpxmac_sl IDLE
29	P_IDLE	R	1h	Prempt cpxmac_sl IDLE
28	MAC_TX_IDLE	R	1h	Prempt and Express cpxmac_sl Transmit IDLE
27	TORF	R	0h	Top of receive FIFO flow control trigger occurred. This bit is write one to clear.
26 - 24	TORF_PRI	R	0h	The lowest priority that caused top of receive FIFO flow control trigger since the last write to clear. This field is write 0x7 to clear.
23 - 16	TX_PFC_FLOW_ACT	R	0h	Transmit Priority Based Flow Control Active (priority 7 down to 0)
15 - 8	RX_PFC_FLOW_ACT	R	0h	Receive Priority Based Flow Control Active (priority 7 down to 0)
	RESERVED	NONE		Reserved
6	EXT_RX_FLOW_EN	R	0h	External Transmit Flow Control Enable
5	EXT_TX_FLOW_EN	R	0h	External Receive Flow Control Enable
4	EXT_GIG	R	0h	External GIG mode
3	EXT_FULLDUPLEX	R	0h	External Fullduplex
	RESERVED	NONE		Reserved
1	RX_FLOW_ACT	R	0h	Receive Flow Control Active
0	TX_FLOW_ACT	R	0h	Transmit Flow Control Active

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4.10.144 CPSW_SS_PN_MAC_SOFT_RESET_REG Registers

4.10.144.1 CPSW_SS_PN_MAC_SOFT_RESET_REG Register (Offset = 338h) [reset = 0h]

Short Description: pn_mac_soft_reset_reg

Long Description:

Return to Summary Table

Table 4-1172. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0338h

Figure 4-450. PN_MAC_SOFT_RESET_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															SOFT_RESET
NONE															R/W
0															0

Access Types Legend

Table 4-1173. PN_MAC_SOFT_RESET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
0	SOFT_RESET	R/W	0h	Software reset

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4.10.145 CPSW_SS_PN_MAC_BOFFTEST_REG Registers

4.10.145.1 CPSW_SS_PN_MAC_BOFFTEST_REG Register (Offset = 33Ch) [reset = 0h]

Short Description: pn_mac_bofftest_reg

Long Description:

Return to Summary Table

Table 4-1174. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 033Ch

Figure 4-451. PN_MAC_BOFFTEST_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED	PACEVAL					RNDNUM									
NONE	R/W					R/W									
0	0					0									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COLL_COUNT				RESERVED		TX_BACKOFF									
R				NONE		R									
0				0		0									

Access Types Legend

Table 4-1175. PN_MAC_BOFFTEST_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
30 - 26	PACEVAL	R/W	0h	Pacing Register Current Value
25 - 16	RNDNUM	R/W	0h	Backoff Random Number Generator
15 - 12	COLL_COUNT	R	0h	Collision Count
	RESERVED	NONE		Reserved
9 - 0	TX_BACKOFF	R	0h	Backoff Count

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4.10.146 CPSW_SS_PN_MAC_RX_PAUSETIMER_REG Registers

4.10.146.1 CPSW_SS_PN_MAC_RX_PAUSETIMER_REG Register (Offset = 340h) [reset = 0h]

Short Description: pn_mac_rx_pausetimer_reg

Long Description:

Return to Summary Table

Table 4-1176. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0340h

Figure 4-452. PN_MAC_RX_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_PAUSETIMER															
R/W															
0															

Access Types Legend

Table 4-1177. PN_MAC_RX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	RX_PAUSETIMER	R/W	0h	RX Pause Timer Value

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4.10.147 CPSW_SS_PN_MAC_RXN_PAUSETIMER_REG Registers

4.10.147.1 CPSW_SS_PN_MAC_RXN_PAUSETIMER_REG Register (Offset = 350h) [reset = 0h]

Short Description: pn_mac_rxn_pausetimer_reg

Long Description:

Return to Summary Table

Table 4-1178. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0350h

Figure 4-453. PN_MAC_RXN_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_PAUSETIMER															
R/W															
0															

Access Types Legend

Table 4-1179. PN_MAC_RXN_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	RX_PAUSETIMER	R/W	0h	RX Pause Timer Value

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4.10.148 CPSW_SS_PN_MAC_TX_PAUSETIMER_REG Registers

4.10.148.1 CPSW_SS_PN_MAC_TX_PAUSETIMER_REG Register (Offset = 370h) [reset = 0h]

Short Description: pn_mac_tx_pausetimer_reg

Long Description:

Return to Summary Table

Table 4-1180. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0370h

Figure 4-454. PN_MAC_TX_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_PAUSETIMER															
R/W															
0															

Access Types Legend

Table 4-1181. PN_MAC_TX_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	TX_PAUSETIMER	R/W	0h	TX Pause Timer Value

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4.10.149 CPSW_SS_PN_MAC_TXN_PAUSETIMER_REG Registers

4.10.149.1 CPSW_SS_PN_MAC_TXN_PAUSETIMER_REG Register (Offset = 380h) [reset = 0h]

Short Description: pn_mac_txn_pausetimer_reg

Long Description:

Return to Summary Table

Table 4-1182. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0380h

Figure 4-455. PN_MAC_TXN_PAUSETIMER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_PAUSETIMER															
R/W															
0															

Access Types Legend

Table 4-1183. PN_MAC_TXN_PAUSETIMER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	TX_PAUSETIMER	R/W	0h	TX Pause Timer Value

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4.10.150 CPSW_SS_PN_MAC_EMCONTROL_REG Registers

4.10.150.1 CPSW_SS_PN_MAC_EMCONTROL_REG Register (Offset = 3A0h) [reset = 0h]

Short Description: pn_mac_emcontrol_reg

Long Description:

Return to Summary Table

Table 4-1184. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 03A0h

Figure 4-456. PN_MAC_EMCONTROL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SOFT	FREE
NONE														R/W	R/W
0														0	0

Access Types Legend

Table 4-1185. PN_MAC_EMCONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	SOFT	R/W	0h	Emulation Soft Bit
0	FREE	R/W	0h	Emulation Free Bit

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4.10.151 CPSW_SS_PN_MAC_TX_GAP_REG Registers

4.10.151.1 CPSW_SS_PN_MAC_TX_GAP_REG Register (Offset = 3A4h) [reset = ch]

Short Description: pn_mac_tx_gap_reg

Long Description:

Return to Summary Table

Table 4-1186. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 03A4h

Figure 4-457. PN_MAC_TX_GAP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX_GAP															
R/W															
1100															

Access Types Legend

Table 4-1187. PN_MAC_TX_GAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	TX_GAP	R/W	44Ch	Transmit Inter-Packet Gap

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4.10.152 CPSW_SS_PN_MAC_PORT_CONFIG Registers

4.10.152.1 CPSW_SS_PN_MAC_PORT_CONFIG Register (Offset = 3A8h) [reset = 204h]

Short Description: Port Configuration

Long Description:

Return to Summary Table

Table 4-1188. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 03A8h

Figure 4-458. PN_MAC_PORT_CONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						IET	XGMII	INTERVLAN_ROUTES							
NONE						R	R	R							
0						1	0	100							

Access Types Legend

Table 4-1189. PN_MAC_PORT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	IET	R	1h	IET support
8	XGMII	R	0h	XGMII support
7 - 0	INTERVLAN_ROUTES	R	64h	The number of InterVLAN routes

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4.10.153 CPSW_SS_PN_INTERVLAN_OPX_POINTER_REG Registers

4.10.153.1 CPSW_SS_PN_INTERVLAN_OPX_POINTER_REG Register (Offset = 3ACh) [reset = 0h]

Short Description: pn_opx_pointer_reg

Long Description:

Return to Summary Table

Table 4-1190. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 03ACh

Figure 4-459. PN_INTERVLAN_OPX_POINTER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														POINTER	
NONE														R/W	
0														0	

Access Types Legend

Table 4-1191. PN_INTERVLAN_OPX_POINTER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	POINTER	R/W	0h	InterVLAN location pointer: This field points to the InterVLAN location that will be read/written by accesses to Enet_Pn_InterVLANx_A/B.

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4.10.154 CPSW_SS_PN_INTERVLAN_OPX_A_REG Registers

4.10.154.1 CPSW_SS_PN_INTERVLAN_OPX_A_REG Register (Offset = 3B0h) [reset = 0h]

Short Description: pn_opx_a_reg

Long Description:

Return to Summary Table

Table 4-1192. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 03B0h

Figure 4-460. PN_INTERVLAN_OPX_A_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DA_23_16								DA_31_24							
R/W								R/W							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA_39_32								DA_47_40							
R/W								R/W							
0								0							

Access Types Legend

Table 4-1193. PN_INTERVLAN_OPX_A_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	DA_23_16	R/W	0h	Destination Address bits 23:16
23 - 16	DA_31_24	R/W	0h	Destination Address bits 31:24
15 - 8	DA_39_32	R/W	0h	Destination Address bits 39:32
7 - 0	DA_47_40	R/W	0h	Destination Address bits 47:40

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4.10.155 CPSW_SS_PN_INTERVLAN_OPX_B_REG Registers

4.10.155.1 CPSW_SS_PN_INTERVLAN_OPX_B_REG Register (Offset = 3B4h) [reset = 0h]

Short Description: pn_opx_b_reg

Long Description:

Return to Summary Table

Table 4-1194. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 03B4h

Figure 4-461. PN_INTERVLAN_OPX_B_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SA_39_32								SA_47_40							
R/W								R/W							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA_7_0								DA_15_8							
R/W								R/W							
0								0							

Access Types Legend

Table 4-1195. PN_INTERVLAN_OPX_B_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	SA_39_32	R/W	0h	Source Address bits 39:32
23 - 16	SA_47_40	R/W	0h	Source Address bits 47:40
15 - 8	DA_7_0	R/W	0h	Destination Address bits 7:0
7 - 0	DA_15_8	R/W	0h	Destination Address bits 15:8

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4.10.156 CPSW_SS_PN_INTERVLAN_OPX_C_REG Registers

4.10.156.1 CPSW_SS_PN_INTERVLAN_OPX_C_REG Register (Offset = 3B8h) [reset = 0h]

Short Description: pn_opx_c_reg

Long Description:

Return to Summary Table

Table 4-1196. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 03B8h

Figure 4-462. PN_INTERVLAN_OPX_C_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SA_7_0								SA_15_8							
R/W								R/W							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SA_23_16								SA_31_24							
R/W								R/W							
0								0							

Access Types Legend

Table 4-1197. PN_INTERVLAN_OPX_C_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	SA_7_0	R/W	0h	Source Address bits 7:0
23 - 16	SA_15_8	R/W	0h	Source Address bits 15:8
15 - 8	SA_23_16	R/W	0h	Source Address bits 23:16
7 - 0	SA_31_24	R/W	0h	Source Address bits 31:24

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4.10.157 CPSW_SS_PN_INTERVLAN_OPX_D_REG Registers

4.10.157.1 CPSW_SS_PN_INTERVLAN_OPX_D_REG Register (Offset = 3BCh) [reset = 0h]

Short Description: pn_opx_d_reg

Long Description:

Return to Summary Table

Table 4-1198. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 03BCh

Figure 4-463. PN_INTERVLAN_OPX_D_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DECREMENT_TTL	DEST_FORCE_UNTAGGED_EGRESS	REPLACE_DA_SA	REPLACE_VID	VID											
R/W	R/W	R/W	R/W	R/W											
0	0	0	0	0											

Access Types Legend

Table 4-1199. PN_INTERVLAN_OPX_D_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15	DECREMENT_TTL	R/W	0h	Decrement Time To Live: When set, the Time To Live (TTL) field in the header is decremented.
14	DEST_FORCE_UNTAGGED_EGRESS	R/W	0h	Destination VLAN Force Untagged Egress: When set, this bit indicates that the VLAN should be removed on egress for the routed packet.
13	REPLACE_DA_SA	R/W	0h	Replace Destination Address and Source Address: When set this bit indicates that the routed packet destination address should be replaced by da[47:0] and the source address should be replaced by sa[47:0].
12	REPLACE_VID	R/W	0h	Replace VLAN ID: When set this bit indicates that the VLAN ID should be replaced for the routed packet.
11 - 0	VID	R/W	0h	VLAN ID

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4.10.158 CPSW_SS_PN_CUT_THRU_REG Registers

4.10.158.1 CPSW_SS_PN_CUT_THRU_REG Register (Offset = 3C0h) [reset = 0h]

Short Description: pn_cut_thru_reg

Long Description:

Return to Summary Table

Table 4-1200. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 03C0h

Figure 4-464. PN_CUT_THRU_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_PRI_CUT_THRU_EN								TX_PRI_CUT_THRU_EN							
R/W								R/W							
0								0							

Access Types Legend

Table 4-1201. PN_CUT_THRU_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 8	RX_PRI_CUT_THRU_EN	R/W	0h	Receive Cut Thru Priority Enable
7 - 0	TX_PRI_CUT_THRU_EN	R/W	0h	Transmit Cut Thru Priority Enable

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4.10.159 CPSW_SS_PN_PORT_SPEED_REG Registers

4.10.159.1 CPSW_SS_PN_PORT_SPEED_REG Register (Offset = 3C4h) [reset = 0h]

Short Description: pn_port_speed_reg

Long Description:

Return to Summary Table

Table 4-1202. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 03C4h

Figure 4-465. PN_PORT_SPEED_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											PORT_SPEED_CHANGED	RESERVED			
NONE											R	NONE			
0											0	0			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT_AUTO_SPEED				RESERVED			PORT_SPEED_AUTO_EN	RESERVED				PORT_SPEED_MANUAL			
R				NONE			R/W	NONE				R/W			
0				0			0	0				0			

Access Types Legend

Table 4-1203. PN_PORT_SPEED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
20	PORT_SPEED_CHANGED	R	0h	Port Speed Changed
	RESERVED	NONE		Reserved
15 - 12	PORT_AUTO_SPEED	R	0h	Detected Auto Speed
	RESERVED	NONE		Reserved
8	PORT_SPEED_AUTO_EN	R/W	0h	Automatic Port Speed Enable
	RESERVED	NONE		Reserved
3 - 0	PORT_SPEED_MANUAL	R/W	0h	Manual Port Speed

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4.10.160 CPSW_SS_FETCH_LOC Registers

4.10.160.1 CPSW_SS_FETCH_LOC Register (Offset = 0h) [reset = 0h]

Short Description: Revision Register

Long Description:

Return to Summary Table

Table 4-1204. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0000h

Figure 4-466. FETCH_LOC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										LOC					
NONE										R/W					
0										0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOC															
R/W															
0															

Access Types Legend

Table 4-1205. FETCH_LOC Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
21 - 0	LOC	R/W	0h	RAM Location

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4.10.161 CPSW_SS_RXGOODFRAMES Registers

4.10.161.1 CPSW_SS_RXGOODFRAMES Register (Offset = 0h) [reset = 0h]

Short Description: RxGoodFrames

Long Description:

Return to Summary Table

Table 4-1206. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0000h

Figure 4-467. RXGOODFRAMES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1207. RXGOODFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of good frames received

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4.10.162 CPSW_SS_RXBROADCASTFRAMES Registers

4.10.162.1 CPSW_SS_RXBROADCASTFRAMES Register (Offset = 4h) [reset = 0h]

Short Description: RxBroadcastFrames

Long Description:

Return to Summary Table

Table 4-1208. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0004h

Figure 4-468. RXBROADCASTFRAMES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1209. RXBROADCASTFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of good broadcast frames received

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4.10.163 CPSW_SS_RXMULTICASTFRAMES Registers

4.10.163.1 CPSW_SS_RXMULTICASTFRAMES Register (Offset = 8h) [reset = 0h]

Short Description: RxMulticastFrames

Long Description:

Return to Summary Table

Table 4-1210. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0008h

Figure 4-469. RXMULTICASTFRAMES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1211. RXMULTICASTFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of good multicast frames received

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4.10.164 CPSW_SS_RXPAUSEFRAMES Registers

4.10.164.1 CPSW_SS_RXPAUSEFRAMES Register (Offset = Ch) [reset = 0h]

Short Description: RxPauseFrames

Long Description:

Return to Summary Table

Table 4-1212. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 000Ch

Figure 4-470. RXPAUSEFRAMES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1213. RXPAUSEFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of pause frames received

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4.10.165 CPSW_SS_RXCRCERRORS Registers

4.10.165.1 CPSW_SS_RXCRCERRORS Register (Offset = 10h) [reset = 0h]

Short Description: RxCRCErrors

Long Description:

Return to Summary Table

Table 4-1214. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0010h

Figure 4-471. RXCRCERRORS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1215. RXCRCERRORS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of CRC errors frames received

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4.10.166 CPSW_SS_RXALIGNCODEERRORS Registers

4.10.166.1 CPSW_SS_RXALIGNCODEERRORS Register (Offset = 14h) [reset = 0h]

Short Description: RxAlignCodeErrors

Long Description:

Return to Summary Table

Table 4-1216. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0014h

Figure 4-472. RXALIGNCODEERRORS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1217. RXALIGNCODEERRORS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of alignment/code errors received

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4.10.167 CPSW_SS_RXOVERSIZEDFRAMES Registers

4.10.167.1 CPSW_SS_RXOVERSIZEDFRAMES Register (Offset = 18h) [reset = 0h]

Short Description: RxOversizedFrames

Long Description:

Return to Summary Table

Table 4-1218. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0018h

Figure 4-473. RXOVERSIZEDFRAMES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1219. RXOVERSIZEDFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of oversized frames received

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4.10.168 CPSW_SS_RXJABBERFRAMES Registers

4.10.168.1 CPSW_SS_RXJABBERFRAMES Register (Offset = 1Ch) [reset = 0h]

Short Description: RxJabberFrames

Long Description:

Return to Summary Table

Table 4-1220. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 001Ch

Figure 4-474. RXJABBERFRAMES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1221. RXJABBERFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of jabber frames received

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4.10.169 CPSW_SS_RXUNDERSIZEDFRAMES Registers

4.10.169.1 CPSW_SS_RXUNDERSIZEDFRAMES Register (Offset = 20h) [reset = 0h]

Short Description: RxUndersizedFrames

Long Description:

Return to Summary Table

Table 4-1222. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0020h

Figure 4-475. RXUNDERSIZEDFRAMES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1223. RXUNDERSIZEDFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of undersized frames received

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4.10.170 CPSW_SS_RXFRAGMENTS Registers

4.10.170.1 CPSW_SS_RXFRAGMENTS Register (Offset = 24h) [reset = 0h]

Short Description: RxFragments

Long Description:

Return to Summary Table

Table 4-1224. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0024h

Figure 4-476. RXFRAGMENTS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1225. RXFRAGMENTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of fragmented frames received

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4.10.171 CPSW_SS_ALE_DROP Registers

4.10.171.1 CPSW_SS_ALE_DROP Register (Offset = 28h) [reset = 0h]

Short Description: ALE_Drop

Long Description:

Return to Summary Table

Table 4-1226. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0028h

Figure 4-477. ALE_DROP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1227. ALE_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of frames dropped by the ALE

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4.10.172 CPSW_SS_ALE_OVERRUN_DROP Registers

4.10.172.1 CPSW_SS_ALE_OVERRUN_DROP Register (Offset = 2Ch) [reset = 0h]

Short Description: ALE_Overrun_Drop

Long Description:

Return to Summary Table

Table 4-1228. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 002Ch

Figure 4-478. ALE_OVERRUN_DROP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1229. ALE_OVERRUN_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of overrun frames dropped by the ALE

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4.10.173 CPSW_SS_RXOCTETS Registers

4.10.173.1 CPSW_SS_RXOCTETS Register (Offset = 30h) [reset = 0h]

Short Description: RxOctets

Long Description:

Return to Summary Table

Table 4-1230. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0030h

Figure 4-479. RXOCTETS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1231. RXOCTETS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of received bytes in good frames

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4.10.174 CPSW_SS_TXGOODFRAMES Registers

4.10.174.1 CPSW_SS_TXGOODFRAMES Register (Offset = 34h) [reset = 0h]

Short Description: TxGoodFrames

Long Description:

Return to Summary Table

Table 4-1232. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0034h

Figure 4-480. TXGOODFRAMES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1233. TXGOODFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of good frames transmitted

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4.10.175 CPSW_SS_TXBROADCASTFRAMES Registers

4.10.175.1 CPSW_SS_TXBROADCASTFRAMES Register (Offset = 38h) [reset = 0h]

Short Description: TxBroadcastFrames

Long Description:

Return to Summary Table

Table 4-1234. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0038h

Figure 4-481. TXBROADCASTFRAMES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1235. TXBROADCASTFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of good broadcast frames transmitted

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4.10.176 CPSW_SS_TXMULTICASTFRAMES Registers

4.10.176.1 CPSW_SS_TXMULTICASTFRAMES Register (Offset = 3Ch) [reset = 0h]

Short Description: TxMulticastFrames

Long Description:

Return to Summary Table

Table 4-1236. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 003Ch

Figure 4-482. TXMULTICASTFRAMES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1237. TXMULTICASTFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of good multicast frames transmitted

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4.10.177 CPSW_SS_TXPAUSEFRAMES Registers

4.10.177.1 CPSW_SS_TXPAUSEFRAMES Register (Offset = 40h) [reset = 0h]

Short Description: TxPauseFrames

Long Description:

Return to Summary Table

Table 4-1238. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0040h

Figure 4-483. TXPAUSEFRAMES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1239. TXPAUSEFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of pause frames transmitted

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4.10.178 CPSW_SS_TXDEFERREDFRAMES Registers

4.10.178.1 CPSW_SS_TXDEFERREDFRAMES Register (Offset = 44h) [reset = 0h]

Short Description: TxDeferredFrames

Long Description:

Return to Summary Table

Table 4-1240. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0044h

Figure 4-484. TXDEFERREDFRAMES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1241. TXDEFERREDFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of deferred frames transmitted

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4.10.179 CPSW_SS_TXCOLLISIONFRAMES Registers

4.10.179.1 CPSW_SS_TXCOLLISIONFRAMES Register (Offset = 48h) [reset = 0h]

Short Description: TxCollisionFrames

Long Description:

Return to Summary Table

Table 4-1242. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0048h

Figure 4-485. TXCOLLISIONFRAMES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1243. TXCOLLISIONFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of transmitted frames experiencing a collision

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4.10.180 CPSW_SS_TXSINGLECOLLFRAMES Registers

4.10.180.1 CPSW_SS_TXSINGLECOLLFRAMES Register (Offset = 4Ch) [reset = 0h]

Short Description: TxSingleCollFrames

Long Description:

Return to Summary Table

Table 4-1244. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 004Ch

Figure 4-486. TXSINGLECOLLFRAMES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1245. TXSINGLECOLLFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of transmitted frames experiencing a single collision

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4.10.181 CPSW_SS_TXMULTCOLLFRAMES Registers

4.10.181.1 CPSW_SS_TXMULTCOLLFRAMES Register (Offset = 50h) [reset = 0h]

Short Description: TxMultCollFrames

Long Description:

Return to Summary Table

Table 4-1246. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0050h

Figure 4-487. TXMULTCOLLFRAMES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1247. TXMULTCOLLFRAMES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of transmitted frames experiencing multiple collisions

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4.10.182 CPSW_SS_TXEXCESSIVECOLLISIONS Registers

4.10.182.1 CPSW_SS_TXEXCESSIVECOLLISIONS Register (Offset = 54h) [reset = 0h]

Short Description: TxExcessiveCollisions

Long Description:

Return to Summary Table

Table 4-1248. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0054h

Figure 4-488. TXEXCESSIVECOLLISIONS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1249. TXEXCESSIVECOLLISIONS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of transmitted frames abandoned due to excessive collisions

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4.10.183 CPSW_SS_TXLATECOLLISIONS Registers

4.10.183.1 CPSW_SS_TXLATECOLLISIONS Register (Offset = 58h) [reset = 0h]

Short Description: TxLateCollisions

Long Description:

Return to Summary Table

Table 4-1250. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0058h

Figure 4-489. TXLATECOLLISIONS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1251. TXLATECOLLISIONS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of transmitted frames abandoned due to a late collision

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4.10.184 CPSW_SS_RXIPGERROR Registers

4.10.184.1 CPSW_SS_RXIPGERROR Register (Offset = 5Ch) [reset = 0h]

Short Description: RxIPGError

Long Description:

Return to Summary Table

Table 4-1252. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 005Ch

Figure 4-490. RXIPGERROR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1253. RXIPGERROR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of receive inter-packet gap errors (10G only)

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4.10.185 CPSW_SS_TXCARRIERSENSEERRORS Registers

4.10.185.1 CPSW_SS_TXCARRIERSENSEERRORS Register (Offset = 60h) [reset = 0h]

Short Description: TxCarrierSenseErrors

Long Description:

Return to Summary Table

Table 4-1254. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0060h

Figure 4-491. TXCARRIERSENSEERRORS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1255. TXCARRIERSENSEERRORS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of transmitted frames that experienced a carrier loss

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4.10.186 CPSW_SS_TXOCTETS Registers

4.10.186.1 CPSW_SS_TXOCTETS Register (Offset = 64h) [reset = 0h]

Short Description: TxOctets

Long Description:

Return to Summary Table

Table 4-1256. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0064h

Figure 4-492. TXOCTETS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1257. TXOCTETS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of bytes in all good frames transmitted

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4.10.187 CPSW_SS_OCTETFRAMES64 Registers

4.10.187.1 CPSW_SS_OCTETFRAMES64 Register (Offset = 68h) [reset = 0h]

Short Description: OctetFrames64

Long Description:

Return to Summary Table

Table 4-1258. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0068h

Figure 4-493. OCTETFRAMES64 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1259. OCTETFRAMES64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of 64-byte frames received and transmitted

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4.10.188 CPSW_SS_OCTETFRAMES65T127 Registers

4.10.188.1 CPSW_SS_OCTETFRAMES65T127 Register (Offset = 6Ch) [reset = 0h]

Short Description: OctetFrames65t127

Long Description:

Return to Summary Table

Table 4-1260. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 006Ch

Figure 4-494. OCTETFRAMES65T127 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1261. OCTETFRAMES65T127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of frames of size 65 to 127 bytes received and transmitted

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4.10.189 CPSW_SS_OCTETFRAMES128T255 Registers

4.10.189.1 CPSW_SS_OCTETFRAMES128T255 Register (Offset = 70h) [reset = 0h]

Short Description: OctetFrames128t255

Long Description:

Return to Summary Table

Table 4-1262. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0070h

Figure 4-495. OCTETFRAMES128T255 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1263. OCTETFRAMES128T255 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of frames of size 128 to 255 bytes received and transmitted

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4.10.190 CPSW_SS_OCTETFRAMES256T511 Registers

4.10.190.1 CPSW_SS_OCTETFRAMES256T511 Register (Offset = 74h) [reset = 0h]

Short Description: OctetFrames256t511

Long Description:

Return to Summary Table

Table 4-1264. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0074h

Figure 4-496. OCTETFRAMES256T511 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1265. OCTETFRAMES256T511 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of frames of size 256 to 511 bytes received and transmitted

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4.10.191 CPSW_SS_OCTETFRAMES512T1023 Registers

4.10.191.1 CPSW_SS_OCTETFRAMES512T1023 Register (Offset = 78h) [reset = 0h]

Short Description: OctetFrames512t1023

Long Description:

Return to Summary Table

Table 4-1266. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0078h

Figure 4-497. OCTETFRAMES512T1023 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1267. OCTETFRAMES512T1023 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of frames of size 512 to 1023 bytes received and transmitted

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4.10.192 CPSW_SS_OCTETFRAMES1024TUP Registers

4.10.192.1 CPSW_SS_OCTETFRAMES1024TUP Register (Offset = 7Ch) [reset = 0h]

Short Description: OctetFrames1024tUP

Long Description:

Return to Summary Table

Table 4-1268. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 007Ch

Figure 4-498. OCTETFRAMES1024TUP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1269. OCTETFRAMES1024TUP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of frames of size 1024 to rx_maxlen bytes received and 1024 bytes or greater transmitted

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4.10.193 CPSW_SS_NETOCTETS Registers

4.10.193.1 CPSW_SS_NETOCTETS Register (Offset = 80h) [reset = 0h]

Short Description: NetOctets

Long Description:

Return to Summary Table

Table 4-1270. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0080h

Figure 4-499. NETOCTETS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1271. NETOCTETS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of bytes received and transmitted

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4.10.194 CPSW_SS_RX_BOTTOM_OF_FIFO_DROP Registers

4.10.194.1 CPSW_SS_RX_BOTTOM_OF_FIFO_DROP Register (Offset = 84h) [reset = 0h]

Short Description: Rx_Bottom_of_FIFO_Drop

Long Description:

Return to Summary Table

Table 4-1272. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0084h

Figure 4-500. RX_BOTTOM_OF_FIFO_DROP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1273. RX_BOTTOM_OF_FIFO_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Receive Bottom of FIFO Drop

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4.10.195 CPSW_SS_PORTMASK_DROP Registers

4.10.195.1 CPSW_SS_PORTMASK_DROP Register (Offset = 88h) [reset = 0h]

Short Description: Portmask_Drop

Long Description:

Return to Summary Table

Table 4-1274. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0088h

Figure 4-501. PORTMASK_DROP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1275. PORTMASK_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of dropped frames received due to portmask

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4.10.196 CPSW_SS_RX_TOP_OF_FIFO_DROP Registers

4.10.196.1 CPSW_SS_RX_TOP_OF_FIFO_DROP Register (Offset = 8Ch) [reset = 0h]

Short Description: Rx_Top_of_FIFO_Drop

Long Description:

Return to Summary Table

Table 4-1276. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 008Ch

Figure 4-502. RX_TOP_OF_FIFO_DROP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1277. RX_TOP_OF_FIFO_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Receive Top of FIFO Drop

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4.10.197 CPSW_SS_ALE_RATE_LIMIT_DROP Registers

4.10.197.1 CPSW_SS_ALE_RATE_LIMIT_DROP Register (Offset = 90h) [reset = 0h]

Short Description: ALE_Rate_Limit_Drop

Long Description:

Return to Summary Table

Table 4-1278. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0090h

Figure 4-503. ALE_RATE_LIMIT_DROP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1279. ALE_RATE_LIMIT_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of dropped frames due to ALE Rate Limiting

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4.10.198 CPSW_SS_ALE_VID_INGRESS_DROP Registers

4.10.198.1 CPSW_SS_ALE_VID_INGRESS_DROP Register (Offset = 94h) [reset = 0h]

Short Description: ALE_VID_Ingress_Drop

Long Description:

Return to Summary Table

Table 4-1280. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0094h

Figure 4-504. ALE_VID_INGRESS_DROP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1281. ALE_VID_INGRESS_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of dropped frames due to ALE VID Ingress

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4.10.199 CPSW_SS_ALE_DA_EQ_SA_DROP Registers

4.10.199.1 CPSW_SS_ALE_DA_EQ_SA_DROP Register (Offset = 98h) [reset = 0h]

Short Description: ALE_DA_EQ_SA_Drop

Long Description:

Return to Summary Table

Table 4-1282. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0098h

Figure 4-505. ALE_DA_EQ_SA_DROP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1283. ALE_DA_EQ_SA_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of dropped frames due to DA=SA

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4.10.200 CPSW_SS_ALE_BLOCK_DROP Registers

4.10.200.1 CPSW_SS_ALE_BLOCK_DROP Register (Offset = 9Ch) [reset = 0h]

Short Description: ALE_Block_Drop

Long Description:

Return to Summary Table

Table 4-1284. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 009Ch

Figure 4-506. ALE_BLOCK_DROP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1285. ALE_BLOCK_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of dropped frames due to ALE Block Mode

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4.10.201 CPSW_SS_ALE_SECURE_DROP Registers

4.10.201.1 CPSW_SS_ALE_SECURE_DROP Register (Offset = A0h) [reset = 0h]

Short Description: ALE_Secure_Drop

Long Description:

Return to Summary Table

Table 4-1286. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00A0h

Figure 4-507. ALE_SECURE_DROP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1287. ALE_SECURE_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of dropped frames due to ALE Secure Mode

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4.10.202 CPSW_SS_ALE_AUTH_DROP Registers

4.10.202.1 CPSW_SS_ALE_AUTH_DROP Register (Offset = A4h) [reset = 0h]

Short Description: ALE_Auth_Drop

Long Description:

Return to Summary Table

Table 4-1288. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00A4h

Figure 4-508. ALE_AUTH_DROP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1289. ALE_AUTH_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	Total number of dropped frames due to ALE Authentication

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4.10.203 CPSW_SS_ALE_UNKN_UNI Registers

4.10.203.1 CPSW_SS_ALE_UNKN_UNI Register (Offset = A8h) [reset = 0h]

Short Description: ALE_Unkn_Uni

Long Description:

Return to Summary Table

Table 4-1290. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00A8h

Figure 4-509. ALE_UNKN_UNI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1291. ALE_UNKN_UNI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	ALE Receive Unknown Unicast

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4.10.204 CPSW_SS_ALE_UNKN_UNI_BCNT Registers

4.10.204.1 CPSW_SS_ALE_UNKN_UNI_BCNT Register (Offset = ACh) [reset = 0h]

Short Description: ALE_Unkn_Uni_Bcnt

Long Description:

Return to Summary Table

Table 4-1292. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00ACh

Figure 4-510. ALE_UNKN_UNI_BCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1293. ALE_UNKN_UNI_BCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	ALE Receive Unknown Unicast Bytecount

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4.10.205 CPSW_SS_ALE_UNKN_MLT Registers

4.10.205.1 CPSW_SS_ALE_UNKN_MLT Register (Offset = B0h) [reset = 0h]

Short Description: ALE_Unkn_Mlt

Long Description:

Return to Summary Table

Table 4-1294. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00B0h

Figure 4-511. ALE_UNKN_MLT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1295. ALE_UNKN_MLT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	ALE Receive Unknown Multicast

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4.10.206 CPSW_SS_ALE_UNKN_MLT_BCNT Registers

4.10.206.1 CPSW_SS_ALE_UNKN_MLT_BCNT Register (Offset = B4h) [reset = 0h]

Short Description: ALE_Unkn_Mlt_Bcnt

Long Description:

Return to Summary Table

Table 4-1296. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00B4h

Figure 4-512. ALE_UNKN_MLT_BCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1297. ALE_UNKN_MLT_BCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	ALE Receive Unknown Multicast Bytecount

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4.10.207 CPSW_SS_ALE_UNKN_BRD Registers

4.10.207.1 CPSW_SS_ALE_UNKN_BRD Register (Offset = B8h) [reset = 0h]

Short Description: ALE_Unkn_Brd

Long Description:

Return to Summary Table

Table 4-1298. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00B8h

Figure 4-513. ALE_UNKN_BRD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1299. ALE_UNKN_BRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	ALE Receive Unknown Broadcast

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4.10.208 CPSW_SS_ALE_UNKN_BRD_BCNT Registers

4.10.208.1 CPSW_SS_ALE_UNKN_BRD_BCNT Register (Offset = BCh) [reset = 0h]

Short Description: ALE_Unkn_Brd_Bcnt

Long Description:

Return to Summary Table

Table 4-1300. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00BCh

Figure 4-514. ALE_UNKN_BRD_BCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1301. ALE_UNKN_BRD_BCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	ALE Receive Unknown Broadcast Bytecount

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4.10.209 CPSW_SS_ALE_POL_MATCH Registers

4.10.209.1 CPSW_SS_ALE_POL_MATCH Register (Offset = C0h) [reset = 0h]

Short Description: ALE_Pol_Match

Long Description:

Return to Summary Table

Table 4-1302. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00C0h

Figure 4-515. ALE_POL_MATCH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1303. ALE_POL_MATCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	ALE Policer Matched

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4.10.210 CPSW_SS_ALE_POL_MATCH_RED Registers

4.10.210.1 CPSW_SS_ALE_POL_MATCH_RED Register (Offset = C4h) [reset = 0h]

Short Description: ALE_Pol_Match_Red

Long Description:

Return to Summary Table

Table 4-1304. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00C4h

Figure 4-516. ALE_POL_MATCH_RED Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1305. ALE_POL_MATCH_RED Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	ALE Policer Matched and Condition Red

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4.10.211 CPSW_SS_ALE_POL_MATCH_YELLOW Registers

4.10.211.1 CPSW_SS_ALE_POL_MATCH_YELLOW Register (Offset = C8h) [reset = 0h]

Short Description: ALE_Pol_Match_Yellow

Long Description:

Return to Summary Table

Table 4-1306. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00C8h

Figure 4-517. ALE_POL_MATCH_YELLOW Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1307. ALE_POL_MATCH_YELLOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	ALE Policer Matched and Condition Yellow

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4.10.212 CPSW_SS_ALE_MULT_SA_DROP Registers

4.10.212.1 CPSW_SS_ALE_MULT_SA_DROP Register (Offset = CCh) [reset = 0h]

Short Description: ALE_MULT_SA_DROP

Long Description:

Return to Summary Table

Table 4-1308. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00CCh

Figure 4-518. ALE_MULT_SA_DROP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1309. ALE_MULT_SA_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	ALE Multicast Source Address drop

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4.10.213 CPSW_SS_ALE_DUAL_VLAN_DROP Registers

4.10.213.1 CPSW_SS_ALE_DUAL_VLAN_DROP Register (Offset = D0h) [reset = 0h]

Short Description: ALE_DUAL_VLAN_DROP

Long Description:

Return to Summary Table

Table 4-1310. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00D0h

Figure 4-519. ALE_DUAL_VLAN_DROP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1311. ALE_DUAL_VLAN_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	ALE Dual VLAN drop

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4.10.214 CPSW_SS_ALE_LEN_ERROR_DROP Registers

4.10.214.1 CPSW_SS_ALE_LEN_ERROR_DROP Register (Offset = D4h) [reset = 0h]

Short Description: ALE_LEN_ERROR_DROP

Long Description:

Return to Summary Table

Table 4-1312. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00D4h

Figure 4-520. ALE_LEN_ERROR_DROP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1313. ALE_LEN_ERROR_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	ALE Length Error drop

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4.10.215 CPSW_SS_ALE_IP_NEXT_HDR_DROP Registers

4.10.215.1 CPSW_SS_ALE_IP_NEXT_HDR_DROP Register (Offset = D8h) [reset = 0h]

Short Description: ALE_IP_NEXT_HDR_DROP

Long Description:

Return to Summary Table

Table 4-1314. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00D8h

Figure 4-521. ALE_IP_NEXT_HDR_DROP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1315. ALE_IP_NEXT_HDR_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	ALE Next Header drop

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4.10.216 CPSW_SS_ALE_IPV4_FRAG_DROP Registers

4.10.216.1 CPSW_SS_ALE_IPV4_FRAG_DROP Register (Offset = DCh) [reset = 0h]

Short Description: ALE_IPV4_FRAG_DROP

Long Description:

Return to Summary Table

Table 4-1316. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00DCh

Figure 4-522. ALE_IPV4_FRAG_DROP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COUNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT															
R/W															
0															

Access Types Legend

Table 4-1317. ALE_IPV4_FRAG_DROP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COUNT	R/W	0h	ALE IPV4 Fragment drop

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4.10.217 CPSW_SS_IET_RX_ASSEMBLY_ERROR_REG Registers

4.10.217.1 CPSW_SS_IET_RX_ASSEMBLY_ERROR_REG Register (Offset = 140h) [reset = 0h]

Short Description: iet_rx_assembly_error

Long Description:

Return to Summary Table

Table 4-1318. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0140h

Figure 4-523. IET_RX_ASSEMBLY_ERROR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IET_RX_ASSEMBLY_ERROR															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_RX_ASSEMBLY_ERROR															
R/W															
0															

Access Types Legend

Table 4-1319. IET_RX_ASSEMBLY_ERROR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	IET_RX_ASSEMBLY_ERROR	R/W	0h	IET Receive Assembly Error

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4.10.218 CPSW_SS_IET_RX_ASSEMBLY_OK_REG Registers

4.10.218.1 CPSW_SS_IET_RX_ASSEMBLY_OK_REG Register (Offset = 144h) [reset = 0h]

Short Description: iet_rx_assembly_ok

Long Description:

Return to Summary Table

Table 4-1320. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0144h

Figure 4-524. IET_RX_ASSEMBLY_OK_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IET_RX_ASSEMBLY_OK															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_RX_ASSEMBLY_OK															
R/W															
0															

Access Types Legend

Table 4-1321. IET_RX_ASSEMBLY_OK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	IET_RX_ASSEMBLY_OK	R/W	0h	IET Receive Assembly Ok

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4.10.219 CPSW_SS_IET_RX_SMD_ERROR_REG Registers

4.10.219.1 CPSW_SS_IET_RX_SMD_ERROR_REG Register (Offset = 148h) [reset = 0h]

Short Description: iet_rx_smd_error

Long Description:

Return to Summary Table

Table 4-1322. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0148h

Figure 4-525. IET_RX_SMD_ERROR_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IET_RX_SMD_ERROR															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_RX_SMD_ERROR															
R/W															
0															

Access Types Legend

Table 4-1323. IET_RX_SMD_ERROR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	IET_RX_SMD_ERROR	R/W	0h	IET Receive Smd Error

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4.10.220 CPSW_SS_IET_RX_FRAG_REG Registers

4.10.220.1 CPSW_SS_IET_RX_FRAG_REG Register (Offset = 14Ch) [reset = 0h]

Short Description: iet_rx_frag

Long Description:

Return to Summary Table

Table 4-1324. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 014Ch

Figure 4-526. IET_RX_FRAG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IET_RX_FRAG															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_RX_FRAG															
R/W															
0															

Access Types Legend

Table 4-1325. IET_RX_FRAG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	IET_RX_FRAG	R/W	0h	IET Receive Frag

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4.10.221 CPSW_SS_IET_TX_HOLD_REG Registers

4.10.221.1 CPSW_SS_IET_TX_HOLD_REG Register (Offset = 150h) [reset = 0h]

Short Description: iet_tx_hold

Long Description:

Return to Summary Table

Table 4-1326. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0150h

Figure 4-527. IET_TX_HOLD_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IET_TX_HOLD															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_TX_HOLD															
R/W															
0															

Access Types Legend

Table 4-1327. IET_TX_HOLD_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	IET_TX_HOLD	R/W	0h	IET Transmit Hold

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4.10.222 CPSW_SS_IET_TX_FRAG_REG Registers

4.10.222.1 CPSW_SS_IET_TX_FRAG_REG Register (Offset = 154h) [reset = 0h]

Short Description: iet_tx_frag

Long Description:

Return to Summary Table

Table 4-1328. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0154h

Figure 4-528. IET_TX_FRAG_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IET_TX_FRAG															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IET_TX_FRAG															
R/W															
0															

Access Types Legend

Table 4-1329. IET_TX_FRAG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	IET_TX_FRAG	R/W	0h	IET Transmit Frag

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4.10.223 CPSW_SS_TX_MEMORY_PROTECT_ERROR Registers

4.10.223.1 CPSW_SS_TX_MEMORY_PROTECT_ERROR Register (Offset = 17Ch) [reset = 0h]

Short Description: Tx_Memory_Protect_Error

Long Description:

Return to Summary Table

Table 4-1330. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 017Ch

Figure 4-529. TX_MEMORY_PROTECT_ERROR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNT							
NONE								R/W							
0								0							

Access Types Legend

Table 4-1331. TX_MEMORY_PROTECT_ERROR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	COUNT	R/W	0h	Transmit Memory Protect CRC Error

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4.10.224 CPSW_SS_ENET_PN_TX_PRI_REG Registers

4.10.224.1 CPSW_SS_ENET_PN_TX_PRI_REG Register (Offset = 180h) [reset = 0h]

Short Description: enet_pn_tx_pri

Long Description:

Return to Summary Table

Table 4-1332. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0180h

Figure 4-530. ENET_PN_TX_PRI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PN_TX_PRIN															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PN_TX_PRIN															
R/W															
0															

Access Types Legend

Table 4-1333. ENET_PN_TX_PRI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PN_TX_PRIN	R/W	0h	ENET TX Priority Packet Count

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4.10.225 CPSW_SS_ENET_PN_TX_PRI_BCNT_REG Registers

4.10.225.1 CPSW_SS_ENET_PN_TX_PRI_BCNT_REG Register (Offset = 1A0h) [reset = 0h]

Short Description: enet_pn_tx_pri_bcnt

Long Description:

Return to Summary Table

Table 4-1334. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 01A0h

Figure 4-531. ENET_PN_TX_PRI_BCNT_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PN_TX_PRIN_BCNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PN_TX_PRIN_BCNT															
R/W															
0															

Access Types Legend

Table 4-1335. ENET_PN_TX_PRI_BCNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PN_TX_PRIN_BCNT	R/W	0h	ENET Port n PRIORITY N Packet Byte Count

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4.10.226 CPSW_SS_ENET_PN_TX_PRI_DROP_REG Registers

4.10.226.1 CPSW_SS_ENET_PN_TX_PRI_DROP_REG Register (Offset = 1C0h) [reset = 0h]

Short Description: enet_pn_tx_pri_drop

Long Description:

Return to Summary Table

Table 4-1336. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 01C0h

Figure 4-532. ENET_PN_TX_PRI_DROP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PN_TX_PRIN_DROP															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PN_TX_PRIN_DROP															
R/W															
0															

Access Types Legend

Table 4-1337. ENET_PN_TX_PRI_DROP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PN_TX_PRIN_DROP	R/W	0h	ENET Port n PRIORITY N Packet Drop Count

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4.10.227 CPSW_SS_ENET_PN_TX_PRI_DROP_BCNT_REG Registers

4.10.227.1 CPSW_SS_ENET_PN_TX_PRI_DROP_BCNT_REG Register (Offset = 1E0h) [reset = 0h]

Short Description: enet_pn_tx_pri_drop_bcnt

Long Description:

Return to Summary Table

Table 4-1338. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 01E0h

Figure 4-533. ENET_PN_TX_PRI_DROP_BCNT_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PN_TX_PRIN_DROP_BCNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PN_TX_PRIN_DROP_BCNT															
R/W															
0															

Access Types Legend

Table 4-1339. ENET_PN_TX_PRI_DROP_BCNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PN_TX_PRIN_DROP_BCNT	R/W	0h	ENET Port n PRIORITY N Packet Drop Byte Count

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4.10.228 CPSW_SS_IDVER_REG Registers

4.10.228.1 CPSW_SS_CPTS_IDVER_REG Register (Offset = 0h) [reset = 4e8a010ch]

Short Description: idver_reg

Long Description:

Return to Summary Table

Table 4-1340. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0000h

Figure 4-534. IDVER_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TX_IDENT															
R															
100111010001010															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_VER			MINOR_VER							
R					R			R							
0					1			1100							

Access Types Legend

Table 4-1341. CPTS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	TX_IDENT	R	5B0CE9307072h	Identification value
15 - 11	RTL_VER	R	0h	RTL version value
10 - 8	MAJOR_VER	R	1h	Major version value
7 - 0	MINOR_VER	R	44Ch	Minor version value

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4.10.229 CPSW_SS_RFTCLK_SEL_REG Registers

4.10.229.1 CPSW_SS_RFTCLK_SEL_REG Register (Offset = 8h) [reset = 0h]

Short Description: rftclk_sel_reg

Long Description:

Return to Summary Table

Table 4-1342. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0008h

Figure 4-535. RFTCLK_SEL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											RFTCLK_SEL				
NONE											R/W				
0											0				

Access Types Legend

Table 4-1343. RFTCLK_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	RFTCLK_SEL	R/W	0h	Reference clock select

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4.10.230 CPSW_SS_TS_PUSH_REG Registers

4.10.230.1 CPSW_SS_TS_PUSH_REG Register (Offset = Ch) [reset = 0h]

Short Description: ts_push_reg

Long Description:

Return to Summary Table

Table 4-1344. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 000Ch

Figure 4-536. TS_PUSH_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															TS_PUSH
NONE															W
0															0

Access Types Legend

Table 4-1345. TS_PUSH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
0	TS_PUSH	W	0h	Time stamp event push

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4.10.231 CPSW_SS_TS_LOAD_VAL_REG Registers

4.10.231.1 CPSW_SS_TS_LOAD_LOW_VAL_REG Register (Offset = 10h) [reset = 0h]

Short Description: ts_load_low_val_reg

Long Description:

Return to Summary Table

Table 4-1346. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0010h

Figure 4-537. TS_LOAD_VAL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_LOAD_VAL															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LOAD_VAL															
R/W															
0															

Access Types Legend

Table 4-1347. TS_LOAD_LOW_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TS_LOAD_VAL	R/W	0h	Time stamp load low value

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4.10.232 CPSW_SS_TS_LOAD_EN_REG Registers

4.10.232.1 CPSW_SS_TS_LOAD_EN_REG Register (Offset = 14h) [reset = 0h]

Short Description: ts_load_en_reg

Long Description:

Return to Summary Table

Table 4-1348. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0014h

Figure 4-538. TS_LOAD_EN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															TS_LOAD_EN
NONE															W
0															0

Access Types Legend

Table 4-1349. TS_LOAD_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
0	TS_LOAD_EN	W	0h	Time stamp load enable

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4.10.233 CPSW_SS_TS_COMP_VAL_REG Registers

4.10.233.1 CPSW_SS_TS_COMP_LOW_VAL_REG Register (Offset = 18h) [reset = 0h]

Short Description: ts_comp_low_val_reg

Long Description:

Return to Summary Table

Table 4-1350. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0018h

Figure 4-539. TS_COMP_VAL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_COMP_VAL															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_VAL															
R/W															
0															

Access Types Legend

Table 4-1351. TS_COMP_LOW_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TS_COMP_VAL	R/W	0h	Time stamp comparison low value

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4.10.234 CPSW_SS_TS_COMP_LEN_REG Registers

4.10.234.1 CPSW_SS_TS_COMP_LEN_REG Register (Offset = 1Ch) [reset = 0h]

Short Description: ts_comp_len_reg

Long Description:

Return to Summary Table

Table 4-1352. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 001Ch

Figure 4-540. TS_COMP_LEN_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_COMP_LENGTH															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_LENGTH															
R/W															
0															

Access Types Legend

Table 4-1353. TS_COMP_LEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TS_COMP_LENGTH	R/W	0h	Time stamp comparison length

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4.10.235 CPSW_SS_INTSTAT_RAW_REG Registers

4.10.235.1 CPSW_SS_INTSTAT_RAW_REG Register (Offset = 20h) [reset = 0h]

Short Description: intstat_raw_reg

Long Description:

Return to Summary Table

Table 4-1354. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0020h

Figure 4-541. INTSTAT_RAW_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															TS_PEND_RAW
NONE															R/W
0															0

Access Types Legend

Table 4-1355. INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
0	TS_PEND_RAW	R/W	0h	TS_PEND_RAW int read (before enable)

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4.10.236 CPSW_SS_INTSTAT_MASKED_REG Registers

4.10.236.1 CPSW_SS_INTSTAT_MASKED_REG Register (Offset = 24h) [reset = 0h]

Short Description: intstat_masked_reg

Long Description:

Return to Summary Table

Table 4-1356. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0024h

Figure 4-542. INTSTAT_MASKED_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															TS_PEND
NONE															R
0															0

Access Types Legend

Table 4-1357. INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
0	TS_PEND	R	0h	TS_PEND masked interrupt read (after enable)

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4.10.237 CPSW_SS_INT_ENABLE_REG Registers

4.10.237.1 CPSW_SS_INT_ENABLE_REG Register (Offset = 28h) [reset = 0h]

Short Description: int_enable_reg

Long Description:

Return to Summary Table

Table 4-1358. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0028h

Figure 4-543. INT_ENABLE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															TS_PEND_EN
NONE															R/W
0															0

Access Types Legend

Table 4-1359. INT_ENABLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
0	TS_PEND_EN	R/W	0h	TS_PEND masked interrupt enable

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4.10.238 CPSW_SS_TS_COMP_NUDGE_REG Registers

4.10.238.1 CPSW_SS_TS_COMP_NUDGE_REG Register (Offset = 2Ch) [reset = 0h]

Short Description: ts_comp_nudge_reg

Long Description:

Return to Summary Table

Table 4-1360. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 002Ch

Figure 4-544. TS_COMP_NUDGE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								NUDGE							
NONE								R/W							
0								0							

Access Types Legend

Table 4-1361. TS_COMP_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	NUDGE	R/W	0h	This 2s complement number is added to the ts_comp_length value to increase or decrease the TS_COMP length by the nudge amount

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4.10.239 CPSW_SS_EVENT_POP_REG Registers

4.10.239.1 CPSW_SS_EVENT_POP_REG Register (Offset = 30h) [reset = 0h]

Short Description: event_pop_reg

Long Description:

Return to Summary Table

Table 4-1362. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0030h

Figure 4-545. EVENT_POP_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															EVENT_POP
NONE															W
0															0

Access Types Legend

Table 4-1363. EVENT_POP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
0	EVENT_POP	W	0h	Event pop

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4.10.240 CPSW_SS_EVENT_0_REG Registers

4.10.240.1 CPSW_SS_EVENT_0_REG Register (Offset = 34h) [reset = 0h]

Short Description: event_0_reg

Long Description:

Return to Summary Table

Table 4-1364. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0034h

Figure 4-546. EVENT_0_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIME_STAMP															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME_STAMP															
R															
0															

Access Types Legend

Table 4-1365. EVENT_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TIME_STAMP	R	0h	Time Stamp

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4.10.241 CPSW_SS_EVENT_1_REG Registers

4.10.241.1 CPSW_SS_EVENT_1_REG Register (Offset = 38h) [reset = 0h]

Short Description: event_1_reg

Long Description:

Return to Summary Table

Table 4-1366. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0038h

Figure 4-547. EVENT_1_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PREMPT_QUEUE	PORT_NUMBER					EVENT_TYPE				MESSAGE_TYPE			
NONE		R	R					R				R			
0		0	0					0				0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEQUENCE_ID															
R															
0															

Access Types Legend

Table 4-1367. EVENT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29	PREMPT_QUEUE	R	0h	Prempt QUEUE
28 - 24	PORT_NUMBER	R	0h	Port number
23 - 20	EVENT_TYPE	R	0h	Event type
19 - 16	MESSAGE_TYPE	R	0h	Message type
15 - 0	SEQUENCE_ID	R	0h	Sequence ID

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4.10.242 CPSW_SS_EVENT_2_REG Registers

4.10.242.1 CPSW_SS_EVENT_2_REG Register (Offset = 3Ch) [reset = 0h]

Short Description: event_2_reg

Long Description:

Return to Summary Table

Table 4-1368. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 003Ch

Figure 4-548. EVENT_2_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DOMAIN							
NONE								R							
0								0							

Access Types Legend

Table 4-1369. EVENT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	DOMAIN	R	0h	Domain

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4.10.243 CPSW_SS_EVENT_3_REG Registers

4.10.243.1 CPSW_SS_EVENT_3_REG Register (Offset = 40h) [reset = 0h]

Short Description: event_3_reg

Long Description:

Return to Summary Table

Table 4-1370. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0040h

Figure 4-549. EVENT_3_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIME_STAMP															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME_STAMP															
R															
0															

Access Types Legend

Table 4-1371. EVENT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TIME_STAMP	R	0h	Time Stamp

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4.10.244 CPSW_SS_TS_LOAD_HIGH_VAL_REG Registers

4.10.244.1 CPSW_SS_TS_LOAD_HIGH_VAL_REG Register (Offset = 44h) [reset = 0h]

Short Description: ts_load_high_val_reg

Long Description:

Return to Summary Table

Table 4-1372. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0044h

Figure 4-550. TS_LOAD_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_LOAD_VAL															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LOAD_VAL															
R/W															
0															

Access Types Legend

Table 4-1373. TS_LOAD_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TS_LOAD_VAL	R/W	0h	Time stamp load high value

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4.10.245 CPSW_SS_TS_COMP_HIGH_VAL_REG Registers

4.10.245.1 CPSW_SS_TS_COMP_HIGH_VAL_REG Register (Offset = 48h) [reset = 0h]

Short Description: ts_comp_high_val_reg

Long Description:

Return to Summary Table

Table 4-1374. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0048h

Figure 4-551. TS_COMP_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_COMP_HIGH_VAL															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_HIGH_VAL															
R/W															
0															

Access Types Legend

Table 4-1375. TS_COMP_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TS_COMP_HIGH_VAL	R/W	0h	Time stamp comparison high value

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4.10.246 CPSW_SS_TS_ADD_VAL_REG Registers

4.10.246.1 CPSW_SS_TS_ADD_VAL_REG Register (Offset = 4Ch) [reset = 0h]

Short Description: ts_add_val

Long Description:

Return to Summary Table

Table 4-1376. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 004Ch

Figure 4-552. TS_ADD_VAL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														ADD_VAL	
NONE														R/W	
0														0	

Access Types Legend

Table 4-1377. TS_ADD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	ADD_VAL	R/W	0h	Add Value

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4.10.247 CPSW_SS_TS_PPM_LOW_VAL_REG Registers

4.10.247.1 CPSW_SS_TS_PPM_LOW_VAL_REG Register (Offset = 50h) [reset = 0h]

Short Description: ts_ppm_low_val_reg

Long Description:

Return to Summary Table

Table 4-1378. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0050h

Figure 4-553. TS_PPM_LOW_VAL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TS_PPM_LOW_VAL															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_PPM_LOW_VAL															
R/W															
0															

Access Types Legend

Table 4-1379. TS_PPM_LOW_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TS_PPM_LOW_VAL	R/W	0h	Time stamp PPM Low value

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4.10.248 CPSW_SS_TS_PPM_HIGH_VAL_REG Registers

4.10.248.1 CPSW_SS_TS_PPM_HIGH_VAL_REG Register (Offset = 54h) [reset = 0h]

Short Description: ts_ppm_high_val_reg

Long Description:

Return to Summary Table

Table 4-1380. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0054h

Figure 4-554. TS_PPM_HIGH_VAL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TS_PPM_HIGH_VAL									
NONE						R/W									
0						0									

Access Types Legend

Table 4-1381. TS_PPM_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	TS_PPM_HIGH_VAL	R/W	0h	Time stamp PPM High value

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4.10.249 CPSW_SS_TS_NUDGE_VAL_REG Registers

4.10.249.1 CPSW_SS_TS_NUDGE_VAL_REG Register (Offset = 58h) [reset = 0h]

Short Description: ts_nudge_val_reg

Long Description:

Return to Summary Table

Table 4-1382. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0058h

Figure 4-555. TS_NUDGE_VAL_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TS_NUDGE_VAL							
NONE								R/W							
0								0							

Access Types Legend

Table 4-1383. TS_NUDGE_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	TS_NUDGE_VAL	R/W	0h	Time stamp Nudge value

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4.10.250 CPSW_SS_TS_CONFIG Registers

4.10.250.1 CPSW_SS_TS_CONFIG Register (Offset = D0h) [reset = 2002h]

Short Description: ts_config

Long Description:

Return to Summary Table

Table 4-1384. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00D0h

Figure 4-556. TS_CONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EVNT_FIFO_DEPTH								NUM_GENF							
R								R							
100000								10							

Access Types Legend

Table 4-1385. TS_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 8	EVNT_FIFO_DEPTH	R	186A0h	The Event FIFO Depth
7 - 0	NUM_GENF	R	Ah	The number of CPTS GENF outputs

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4.10.251 CPSW_SS_MOD_VER Registers

4.10.251.1 CPSW_SS_MOD_VER Register (Offset = 0h) [reset = 294104h]

Short Description: Module and Version

Long Description:

Return to Summary Table

Table 4-1386. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0000h

Figure 4-557. MOD_VER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODULE_ID															
R															
101001															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VERSION					MAJOR_REVISION			CUSTOM_REVISION		MINOR_REVISION					
R					R			R		R					
1000					1			0		100					

Access Types Legend

Table 4-1387. MOD_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	MODULE_ID	R	18A89h	ALE_3g512ie module ID.
15 - 11	RTL_VERSION	R	3E8h	RTL Version.
10 - 8	MAJOR_REVISION	R	1h	Major Revision.
7 - 6	CUSTOM_REVISION	R	0h	Custom Revision.
5 - 0	MINOR_REVISION	R	64h	Minor Revision.

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4.10.252 CPSW_SS_ALE_STATUS Registers

4.10.252.1 CPSW_SS_ALE_STATUS Register (Offset = 4h) [reset = 80000400h]

Short Description: ALE Status

Long Description:

Return to Summary Table

Table 4-1388. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0004h

Figure 4-558. ALE_STATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UREGANDREGMSK12	UREGANDREGMSK08	RESERVED													
R	R	NONE													
1	0	0													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POLCNTDIV8								RAMDEPTH128	RAMDEPTH32	RESERVED	KLUENTRIES				
R								R	R	NONE	R				
100								0	0	0	0				

Access Types Legend

Table 4-1389. ALE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UREGANDREGMSK12	R	1h	When set, the unregistered multicast field is a mask versus an index on 12 bit boundary in the ALE table.
30	UREGANDREGMSK08	R	0h	When set, the unregistered multicast field is a mask versus an index on 8 bit boundary in the ALE table.
	RESERVED	NONE		Reserved
15 - 8	POLCNTDIV8	R	64h	This is the number of policer engines the ALE implements divided by 8. A value of 4 indicates 32 policer engines total.
7	RAMDEPTH128	R	0h	The number of ALE entries per slice of the table when this is set it indicates the depth is 128 if both ramdepth128 and ramdepth32 are zero the depth is 64.
6	RAMDEPTH32	R	0h	The number of ALE entries per slice of the table when this is set it indicates the depth is 32 if both ramdepth128 and ramdepth32 are zero the depth is 64.
	RESERVED	NONE		Reserved
4 - 0	KLUENTRIES	R	0h	This is the number of table entries total divided by 1024. A value of 1 indicates 1024 table entries. A value of 8 indicates 8192 table entries.

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4.10.253 CPSW_SS_ALE_CONTROL Registers

4.10.253.1 CPSW_SS_ALE_CONTROL Register (Offset = 8h) [reset = 0h]

Short Description: ALE Control

Long Description:

Return to Summary Table

Table 4-1390. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0008h

Figure 4-559. ALE_CONTROL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ENABLE_ALE	CLEAR_TABLE	AGE_OUT_NOW	RESERVED			MIRROR_DP		UPD_BW_CTRL			RESERVED			MIRROR_TOP	
R/W	R/W	R/W	NONE			R/W		R/W			NONE			R/W	
0	0	0	0			0		0			0			0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UPD_STATIC	LRN_HOST_DST	UVLAN_NO_LEARN	MIRROR_MEN	MIRROR_DEN	MIRROR_SEN	RESERVED	EN_HOST_UNI_FLOOD	LEARN_NO_VLANID	ENABLE_VID0_MODE	ENABLE_OUI_DENY	ENABLE_BYPASS	BCAST_MCAST_CTL	ALE_VLAN_AWARE	ENABLE_AUTH_MODE	ENABLE_RATE_LIMIT
R/W	R/W	R/W	R/W	R/W	R/W	NONE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1391. ALE_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE_ALE	R/W	0h	Enable ALE 0 - Drop all packets 1 - Enable ALE packet processing
30	CLEAR_TABLE	R/W	0h	Clear ALE address table - Setting this bit causes the ALE hardware to write all table bit values to zero. Software must perform a clear table operation as part of the ALE setup/configuration process. Setting this bit causes all ALE accesses to be held up for 64 clocks while the clear is performed. Access to all ALE registers will be blocked (wait states) until the 64 clocks have completed. This bit cannot be read as one because the read is blocked until the clear table is completed at which time this bit is cleared to zero.
29	AGE_OUT_NOW	R/W	0h	Age Out Address Table Now - Setting this bit causes the ALE hardware to remove (free up) any ageable table entry that does not have a set touch bit. This bit is cleared when the age out process has completed. This bit may be read. The age out process takes four times the number of table entries clock cycles (4096 cycles for 1K addresses) best case (no ale packet processing during ageout) and sixty five times the number of table entries clock cycles (66560 cycles for 1K addresses) absolute worst case.
	RESERVED	NONE		Reserved
25 - 24	MIRROR_DP	R/W	0h	Mirror Destination Port - This field defines the port to which destination traffic destined will be duplicated. That is all traffic that is forwarded to this port will also be mirrored to the ~imirror_top port.

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Table 4-1391. ALE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23 - 21	UPD_BW_CTRL	R/W	0h	The ~iupd_bw_ctrl field allows for up to 8 times the rate in which adds, updates, touches, writes, and aging updates can occur. At frequencies of 350Mhz, the table update rate should be at it lowest or 5 Million updates per second. When operating the switch core at frequencies or above, the ~iupd_bw_ctrl can be programmed more aggressive. If the ~iupd_bw_ctrl is set but the frequency of the switch subsystem is below the associated value, ALE will drop packets due to insufficient time to complete lookup under high traffic loads. 0 - 350Mhz, 5M 1 - 359Mhz, 11M 2 - 367Mhz, 16M 3 - 375Mhz, 22M 4 - 384Mhz, 28M 5 - 392Mhz, 34M 6 - 400Mhz, 39M 7 - 409Mhz, 45M
	RESERVED	NONE		Reserved
17 - 16	MIRROR_TOP	R/W	0h	Mirror To Port - This field defines the destination port for the mirror traffic. If the traffic is received or transmitted on the mirror destination port it will not be duplicated. Traffic defined as mirror traffic only may be dropped by the switch due to congestion.
15	UPD_STATIC	R/W	0h	Update Static Entries - A static Entry is an entry that is not agable. When clear this bit will prevent any static entry (agable bit clear) from being updated due to port change. When set it allows static entries (agable bit clear) to update the source port if required. This bit should normally be '0' for most switch configurations.
14	LRN_HOST_DST	R/W	0h	Learn Host Destination - This field is set to only learn unicast packet source addresses that are destined to the host port. This bit is only valid for 3 port switches and allows the ALE table to only contain addresses the host port is concerned about. This bit is affectively disabled when ~ien_host_uni_flood is set since any unknown unicast is also sent to the host port for extended bridging operations.
13	UVLAN_NO_LEARN	R/W	0h	Unknown VLAN No Learn - This field when set will prevent source addresses of unknown VLAN IDs from being automatically added into the look up table if learning is enabled.
12	MIRROR_MEN	R/W	0h	Mirror Match Entry Enable - This field enables the match mirror option. When this bit is set any traffic whose destination, source, VLAN or OUI matches the ~imirror_midx entry index will have that traffic also sent to the ~imirror_top port.
11	MIRROR_DEN	R/W	0h	Mirror Destination Port Enable - This field enables the destination port mirror option. When this bit is set any traffic destined for the ~imirror_dp port will have its transmit traffic also sent to the ~imirror_top port.
10	MIRROR_SEN	R/W	0h	Mirror Source Port Enable - This field enables the source port mirror option. When this bit is set any port with the ~ipX_mirror_sp set in the ALE Port Control registers set will have its received traffic also sent to the ~imirror_top port.
	RESERVED	NONE		Reserved
8	EN_HOST_UNI_FLOOD	R/W	0h	Unknown unicast packets flood to host 0 - unknown unicast packets are not sent to the host 1 - unknown unicast packets flood to host port as well as other ports
7	LEARN_NO_VLANID	R/W	0h	Learn No VID - 0 - VID is learned with the source address 1 - VID is not learned with the source address (source address is not tied to VID). Determines the entry type.
6	ENABLE_VID0_MODE	R/W	0h	Enable VLAN ID = 0 Mode 0 - Process the priority tagged packet with VID = PORT_VLAN[11:0]. 1 - Process the priority tagged packet with VID = 0.
5	ENABLE_OUI_DENY	R/W	0h	Enable OUI Deny Mode - When set, any packet with a non-matching OUI source address will be dropped to the host unless the packet destination address matches a supervisory destination address table entry. When cleared, any packet source address matching an OUI address table entry will be dropped to the host unless the destination address matches with a supervisory destination address table entry.
4	ENABLE_BYPASS	R/W	0h	ALE Bypass - When set, packets received on non-host ports are sent to the host. It is expected that packets from the host are directed to the particular port. 0 - no bypass 1 - bypass the ALE

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Table 4-1391. ALE_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	BCAST_MCAST_CTL	R/W	0h	Rate Limit Transmit mode 0 - Broadcast and multicast rate limit counters are received port based 1 - Broadcast and multicast rate limit counters are transmit port based
2	ALE_VLAN_AWARE	R/W	0h	ALE VLAN Aware - Determines how traffic is forwarded using VLAN rules. 0 - Simple switch rules, packets forwarded to all ports for unknown destinations. 1 - VLAN Aware rules, packets forwarded based on VLAN members
1	ENABLE_AUTH_MODE	R/W	0h	Enable MAC Authorization Mode - Mac authorization mode requires that all table entries be made by the host software. There is no auto learning of addresses in authorization mode and the packet will be dropped if the source address is not found (and the destination address is not a multicast address with the super table entry bit set). 0 - The ALE is not in MAC authorization mode 1 - The ALE is in MAC authorization mode
0	ENABLE_RATE_LIMIT	R/W	0h	Enable Broadcast and Multicast Rate Limit 0 - Broadcast/Multicast rates not limited 1 - Broadcast/Multicast packet reception limited to the port control register rate limit fields.

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4.10.254 CPSW_SS_ALE_CTRL2 Registers

4.10.254.1 CPSW_SS_ALE_CTRL2 Register (Offset = Ch) [reset = 0h]

Short Description: ALE Control 2

Long Description:

Return to Summary Table

Table 4-1392. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 000Ch

Figure 4-560. ALE_CTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRK_EN_DST	TRK_EN_SRC	TRK_EN_PRI	RESERVED	TRK_EN_IVLAN	RESERVED	TRK_EN_SIP	TRK_EN_DIP	DROP_BADLEN	NODROP_SRCMCST	DEFNOFRAG	DEFLMTNXTHDR	RESERVED	TRK_BASE		
R/W	R/W	R/W	NONE	R/W	NONE	R/W	R/W	R/W	R/W	R/W	R/W	NONE	R/W		
0	0	0	0	0	0	0	0	0	0	0	0	0	0		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MIRROR_MIDX							
NONE								R/W							
0								0							

Access Types Legend

Table 4-1393. ALE_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TRK_EN_DST	R/W	0h	Trunk Enable Destination Address - This field enables the destination MAC address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
30	TRK_EN_SRC	R/W	0h	Trunk Enable Source Address - This field enables the source MAC address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
29	TRK_EN_PRI	R/W	0h	Trunk Enable Priority - This field enables the VLAN Priority bits to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. In the event that DSCP mapping is enabled and there is no VLAN the DSCP priority will be used. For all other non IP frames without VLAN the port default priority is used.
	RESERVED	NONE		Reserved
27	TRK_EN_IVLAN	R/W	0h	Trunk Enable Inner VLAN - This field enables the inner VLAN ID value (C-VLANID) to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination.
	RESERVED	NONE		Reserved
25	TRK_EN_SIP	R/W	0h	Trunk Enable Source IP Address - This field enables the source IP address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.
24	TRK_EN_DIP	R/W	0h	Trunk Enable Destination IP Address - This field enables the destination IP address to be used with the hash function G(X) = 1 + X + X^3 and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.
23	DROP_BADLEN	R/W	0h	Drop Bad Length will drop any packet that the 802.3 length field is larger than the packet. Ethertypes 0-1500 are 802.3 lengths, all others are Ether types.

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Table 4-1393. ALE_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	NODROP_SRCMCST	R/W	0h	No Drop Source Multicast will disable the dropping of any source address with the multicast bit set.
21	DEFNOFRAG	R/W	0h	Default No Frag field will cause an IPv4 fragmented packet to be dropped if a VLAN entry is not found.
20	DEFLMTNXTHDR	R/W	0h	Default limit next header field will cause an IPv4 protocol or IPv6 next header packet to be dropped if a VLAN entry is not found and the protocol or next header does not match the ~iALE_NXT_HDR register values.
	RESERVED	NONE		Reserved
18 - 16	TRK_BASE	R/W	0h	Trunk Base - This field is the hash formula starting value. Changing this value will cause the packet distribution on trunk ports to be changed. If all the ~itrk_en_dst, ~itrk_en_src, ~itrk_en_pri and ~itrk_en_vlan are '0', this value is used as the distribution index. That is a '0' will select the 1st bit of an 'N' link trunk, a '1' will select the second, etc. Below is the distribution across the trunk links. The first number in the ~iitalic sequence indicates the traffic is sent to the lowest numbered port of a trunk group. For example if you have a 3 port trunk, the hash result 0 will go to the base port (0), hash result 1 will go to the highest port of the trunk group (2), hash result 2 will go to the middle port (1), etc. 1 - ~i00000000 2 - ~i01010101 3 - ~i02102102 4 - ~i03210321
	RESERVED	NONE		Reserved
8 - 0	MIRROR_MIDX	R/W	0h	Mirror Index - This field is the ALE lookup table entry index that when a match occurs will cause this traffic to be mirrored to the ~imirror_top port. That is any VLAN, ONU or address with or withou VLAN can be selected for traffic mirroring.

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4.10.255 CPSW_SS_ALE_PRESCALE Registers

4.10.255.1 CPSW_SS_ALE_PRESCALE Register (Offset = 10h) [reset = 0h]

Short Description: ALE Prescale

Long Description:

Return to Summary Table

Table 4-1394. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0010h

Figure 4-561. ALE_PRESCALE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												ALE_PRESCALE			
NONE												R/W			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALE_PRESCALE															
R/W															
0															

Access Types Legend

Table 4-1395. ALE_PRESCALE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	ALE_PRESCALE	R/W	0h	ALE Prescale - The input clock is divided by this value for use in the multicast/broadcast rate limiters. The minimum operating value is 0x10. The prescaler is off when the value is zero.

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4.10.256 CPSW_SS_ALE_AGING_CTRL Registers

4.10.256.1 CPSW_SS_ALE_AGING_CTRL Register (Offset = 14h) [reset = 0h]

Short Description: ALE Aging Control

Long Description:

Return to Summary Table

Table 4-1396. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0014h

Figure 4-562. ALE_AGING_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRESCALE_2_DISABLE	PRESCALE_1_DISABLE	RESERVED						ALE_AGING_TIMER							
R/W	R/W	NONE						R/W							
0	0	0						0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALE_AGING_TIMER															
R/W															
0															

Access Types Legend

Table 4-1397. ALE_AGING_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRESCALE_2_DISABLE	R/W	0h	ALE Prescaler 2 Disable - When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes.
30	PRESCALE_1_DISABLE	R/W	0h	ALE Prescaler 1 Disable - When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes.
	RESERVED	NONE		Reserved
23 - 0	ALE_AGING_TIMER	R/W	0h	ALE Aging Timer - This field specifies the number of clock cycles times 1,000,000 between aging operations.

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4.10.257 CPSW_SS_ALE_NXT_HDR Registers

4.10.257.1 CPSW_SS_ALE_NXT_HDR Register (Offset = 1Ch) [reset = 0h]

Short Description: ALE Next Header

Long Description:

Return to Summary Table

Table 4-1398. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 001Ch

Figure 4-563. ALE_NXT_HDR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IP_NXT_HDR3								IP_NXT_HDR2							
R/W								R/W							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP_NXT_HDR1								IP_NXT_HDR0							
R/W								R/W							
0								0							

Access Types Legend

Table 4-1399. ALE_NXT_HDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	IP_NXT_HDR3	R/W	0h	The ~iip_nxt_hdr3 is the forth protocol or next header compared when enabled.
23 - 16	IP_NXT_HDR2	R/W	0h	The ~iip_nxt_hdr2 is the third protocol or next header compared when enabled.
15 - 8	IP_NXT_HDR1	R/W	0h	The ~iip_nxt_hdr1 is the second protocol or next header compared when enabled.
7 - 0	IP_NXT_HDR0	R/W	0h	The ~iip_nxt_hdr0 is the first protocol or next header compared when enabled.

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4.10.258 CPSW_SS_ALE_TBLCTL Registers

4.10.258.1 CPSW_SS_ALE_TBLCTL Register (Offset = 20h) [reset = 0h]

Short Description: ALE Table Control

Long Description:

Return to Summary Table

Table 4-1400. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0020h

Figure 4-564. ALE_TBLCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TABLE WR	RESERVED														
R/W	NONE														
0	0														
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TABLEIDX							
NONE								R/W							
0								0							

Access Types Legend

Table 4-1401. ALE_TBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TABLEWR	R/W	0h	Table Write - This bit is used to write the table words to the lookup table. 0 - Table Read Operation is performed. The contents of the ~b TABLEIDX entry will be read into the ~b ALE_TBLWx registers 1 - Table write operation is performed. This will take the current contents from the ~b ALE_TBLWx registers and write them to the table at the specified ~b TABLEIDX.
	RESERVED	NONE		Reserved
8 - 0	TABLEIDX	R/W	0h	The table index is used to determine which lookup table entry is read or written.

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4.10.259 CPSW_SS_ALE_TBLW2 Registers

4.10.259.1 CPSW_SS_ALE_TBLW2 Register (Offset = 34h) [reset = 0h]

Short Description: ALE LUT Table word 2

Long Description:

Return to Summary Table

Table 4-1402. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0034h

Figure 4-565. ALE_TBLW2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									TABLEWRD2						
NONE									R/W						
0									0						

Access Types Legend

Table 4-1403. ALE_TBLW2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6 - 0	TABLEWRD2	R/W	0h	Table Entry bits [71:64]

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4.10.260 CPSW_SS_ALE_TBLW1 Registers

4.10.260.1 CPSW_SS_ALE_TBLW1 Register (Offset = 38h) [reset = 0h]

Short Description: ALE LUT Table word 1

Long Description:

Return to Summary Table

Table 4-1404. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0038h

Figure 4-566. ALE_TBLW1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TABLEWRD1															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLEWRD1															
R/W															
0															

Access Types Legend

Table 4-1405. ALE_TBLW1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TABLEWRD1	R/W	0h	Table Entry bits [63:32]

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4.10.261 CPSW_SS_ALE_TBLW0 Registers

4.10.261.1 CPSW_SS_ALE_TBLW0 Register (Offset = 3Ch) [reset = 0h]

Short Description: ALE LUT Table word 0

Long Description:

Return to Summary Table

Table 4-1406. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 003Ch

Figure 4-567. ALE_TBLW0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TABLEWRD0															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TABLEWRD0															
R/W															
0															

Access Types Legend

Table 4-1407. ALE_TBLW0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TABLEWRD0	R/W	0h	Table Entry bits [31:0]

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4.10.262 CPSW_SS_I0_ALE_PORTCTL0 Registers

4.10.262.1 CPSW_SS_I0_ALE_PORTCTL0 Register (Offset = 40h) [reset = 0h]

Short Description: ALE Port Control X

Long Description:

Return to Summary Table

Table 4-1408. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0040h

Figure 4-568. I0_ALE_PORTCTL0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I0_REG_P0_BCAST_LIMIT								I0_REG_P0_MCAST_LIMIT							
R/W								R/W							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I0_REG_P0_DROP_DOUBLE_VLAN	I0_REG_P0_DROP_DUAL_VLAN	I0_REG_P0_MACONLY_CAF	I0_REG_P0_DIS_PAUTHMOD	I0_REG_P0_MACONLY	I0_REG_P0_TRUNKEN	I0_REG_P0_TRUNKNUM		I0_REG_P0_MIRROR_SP	RESERVED	I0_REG_P0_NO_SA_UPDATE	I0_REG_P0_NO_LEARN	I0_REG_P0_VID_INGRESS_CHECK	I0_REG_P0_DROP_UN_TAGGED	I0_REG_P0_PORTSTATE	
R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W	NONE	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0		0	0	0	0	0	0	0	

Access Types Legend

Table 4-1409. I0_ALE_PORTCTL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	I0_REG_P0_BCAST_LIMIT	R/W	0h	Broadcast Packet Rate Limit - Each prescale pulse loads this field into the port broadcast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Broadcast rate limiting is enabled by a non-zero value in this field.
23 - 16	I0_REG_P0_MCAST_LIMIT	R/W	0h	Multicast Packet Rate Limit - Each prescale pulse loads this field into the port multicast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse. Multicast rate limiting is enabled by a non-zero value in this field.The ~imcast_limit is the number of Multicast packets that will be forwaded per ~iale_prescale time.
15	I0_REG_P0_DROP_DOUBLE_VLAN	R/W	0h	Drop Double VLAN - When set cause any received packet with double VLANs to be dropped. That is if there are two ctag or two stag fields in the packet it will be dropped.
14	I0_REG_P0_DROP_DUAL_VLAN	R/W	0h	Drop Dual VLAN - When set will cause any received packet with dual VLAN stag followed by ctag to be dropped.
13	I0_REG_P0_MACONLY_CAF	R/W	0h	Mac Only Copy All Frames - When set a Mac Only port will transfer all received good frames to the host. When clear a Mac Only port will transfer packets to the host based on ALE destination address lookup operation (which operates more like an Ethernet Mac). A Mac Only port is a port with ~imaconly set.

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Table 4-1409. I0_ALE_PORTCTL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	I0_REG_P0_DIS_PAUTH MOD	R/W	0h	Disable Port authorization - When set will allow unknown addresses to arrive on a switch in authorization mode. It is intended for device to device network connection on ports which do not require MACSEC encryption.
11	I0_REG_P0_MACONLY	R/W	0h	MAC Only - When set enables this port be treated like a MAC port for the host. All traffic received is only sent to the host. The host must direct traffic to this port as the lookup engine will not send traffic to the ports with the ~ip0_maconly bit set and the ~ip0_no_learn also set. If ~ip0_maconly bit is set and the ~ip0_no_learn is not set, the host can send non-directed packets that can be sent to the destination of a MacOnly port. It is also possible that The host can broadcast to all ports including MacOnly ports in this mode.
10	I0_REG_P0_TRUNKEN	R/W	0h	Trunk Enable - This field is used to enable a port into a trunk. Any port can be used as a trunk port, any two or more ports with the ~ip0_trunken its set and having the same ~ip0_trunknum will be placed in the same trunk. There is no requirement for trunk ports to be adjacent. If all ports are enabled in the same trunk, no traffic can flow as traffic received within a trunk is never trasnmitted out the same trunk. If only a single port is a member of a trunk, it looks like a normal port with exception of entries in the look up table will be noted as a trunk entry.
9 - 8	I0_REG_P0_TRUNKNUM	R/W	0h	Trunk Number - This field is used as the trunk number when the ~ip0_trunken is also set. Ports with the same trunk number that have the ~ip0_trunken also set will have traffic distributed within the trunk based on the result of the hash function descrived above.
7	I0_REG_P0_MIRROR_SP	R/W	0h	Mirror Source Port - This field enables the source port mirror option. When this bit is set any traffic received on the port with the reg_p0_mirror_sp bit set will have its received traffic also sent to the ~imirror_top port.
	RESERVED	NONE		Reserved
5	I0_REG_P0_NO_SA_UP DATE	R/W	0h	No Source Address Update - When set will not update the source addresses for this port.
4	I0_REG_P0_NO_LEARN	R/W	0h	No Learn - When set will not learn the source addresses for this port.
3	I0_REG_P0_VID_INGRE SS_CHECK	R/W	0h	VLAN Ingress Check - When set if a packet received is not a member of the VLAN, the packet will be dropped.
2	I0_REG_P0_DROP_UN_ TAGGED	R/W	0h	If Drop Untagged - When set will drop packets without a VLAN tag.
1 - 0	I0_REG_P0_PORTSTATE	R/W	0h	Port State - Defins the current port state used for lookup operations. 0 - Disabled 1 - Blocked 2 - Learning 3 - Forwarding

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4.10.263 CPSW_SS_ALE_UVLAN_MEMBER Registers

4.10.263.1 CPSW_SS_ALE_UVLAN_MEMBER Register (Offset = 90h) [reset = 0h]

Short Description: ALE Unknown VLAN Member Mask Register

Long Description:

Return to Summary Table

Table 4-1410. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0090h

Figure 4-569. ALE_UVLAN_MEMBER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													UVLAN_MEMBER_LIST		
NONE													R/W		
0													0		

Access Types Legend

Table 4-1411. ALE_UVLAN_MEMBER Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	UVLAN_MEMBER_LIST	R/W	0h	Unknown VLAN Member List - Each bit represents the port member status for unknown VLANs.

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4.10.264 CPSW_SS_ALE_UVLAN_URCAST Registers

4.10.264.1 CPSW_SS_ALE_UVLAN_URCAST Register (Offset = 94h) [reset = 0h]

Short Description: ALE Unknown VLAN Unregistered Multicast Flood Mask Register

Long Description:

Return to Summary Table

Table 4-1412. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0094h

Figure 4-570. ALE_UVLAN_URCAST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													UVLAN_UNREG_MCAST_FLOOD_MASK		
NONE													R/W		
0													0		

Access Types Legend

Table 4-1413. ALE_UVLAN_URCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	UVLAN_UNREG_MCAST_FLOOD_MASK	R/W	0h	Unknown VLAN Unregister Multicast Flood Mask - Each bit represents the port to which unregistered multicast are sent for unregistered VLANs.

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4.10.265 CPSW_SS_ALE_UVLAN_RMCAST Registers

4.10.265.1 CPSW_SS_ALE_UVLAN_RMCAST Register (Offset = 98h) [reset = 0h]

Short Description: ALE Unknown VLAN Registered Multicast Flood Mask Register

Long Description:

Return to Summary Table

Table 4-1414. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0098h

Figure 4-571. ALE_UVLAN_RMCAST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													UVLAN_REG_MCAST_FLOOD_MASK		
NONE													R/W		
0													0		

Access Types Legend

Table 4-1415. ALE_UVLAN_RMCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	UVLAN_REG_MCAST_FLOOD_MASK	R/W	0h	Unknown VLAN Register Multicast Flood Mask - Each bit represents the port to which registered multicast are sent for unregistered VLANs. This field is ANDed with the registered multicast mask to determine the destinations for unregistered VLANs.

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4.10.266 CPSW_SS_ALE_UVLAN_UNTAG Registers

4.10.266.1 CPSW_SS_ALE_UVLAN_UNTAG Register (Offset = 9Ch) [reset = 0h]

Short Description: ALE Unknown VLAN force Untagged Egress Mask Register

Long Description:

Return to Summary Table

Table 4-1416. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 009Ch

Figure 4-572. ALE_UVLAN_UNTAG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													UVLAN_FORCE_UNTAGGED_EGRESS		
NONE													R/W		
0													0		

Access Types Legend

Table 4-1417. ALE_UVLAN_UNTAG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	UVLAN_FORCE_UNTAGGED_EGRESS	R/W	0h	Unknown VLAN Force Untagged Egress Mask - Each bit represents the port where the VLAN will be removed for unregistered VLANs.

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4.10.267 CPSW_SS_ALE_STAT_DIAG Registers

4.10.267.1 CPSW_SS_ALE_STAT_DIAG Register (Offset = B8h) [reset = 0h]

Short Description: ALE Statistic Output Diagnostic Register

Long Description:

Return to Summary Table

Table 4-1418. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00B8h

Figure 4-573. ALE_STAT_DIAG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBCAST_DIAG	RESERVED					PORT_DIAG		RESERVED				STAT_DIAG			
R/W	NONE					R/W		NONE				R/W			
0	0					0		0				0			

Access Types Legend

Table 4-1419. ALE_STAT_DIAG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15	PBCAST_DIAG	R/W	0h	When set and the ~iport_diag is set to zero, will allow all ports to see the same stat diagnostic increment.
	RESERVED	NONE		Reserved
9 - 8	PORT_DIAG	R/W	0h	The port selected that a received packet will cause the selected error to increment
	RESERVED	NONE		Reserved
3 - 0	STAT_DIAG	R/W	0h	When non-zero will cause the selected statistic to increment on the next frame received. For the selected Port. 0: Disabled 1: Destination Equal Source Drop Stat will count 2: VLAN Ingress Check Drop Stat will count 3: Source Multicast Drop Stat will count 4: Dual VLAN Drop Stat will count 5: Ether Type length error Drop Stat will count 6: Next Hop Limit Drop Stat will count 7: IPv4 Fragment Drop Stat will count 8: Classifier Hit Stat will count 9: Classifier Red Drop Stat will count 10: Classifier Yellow Drop Stat will count 11: ALE Overflow Drop Stat will count 12: Rate Limit Drop Stat will count 13: Blocked Address Drop Stat will count 14: Secure Address Drop Stat will count 15: Authorization Drop Stat will count

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4.10.268 CPSW_SS_ALE_OAM_LB_CTRL Registers

4.10.268.1 CPSW_SS_ALE_OAM_LB_CTRL Register (Offset = BCh) [reset = 0h]

Short Description: ALE OAM Loopback Control

Long Description:

Return to Summary Table

Table 4-1420. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00BCh

Figure 4-574. ALE_OAM_LB_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															OAM_LB_CTRL
NONE															R/W
0															0

Access Types Legend

Table 4-1421. ALE_OAM_LB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	OAM_LB_CTRL	R/W	0h	The ~ioam_lb_ctrl allows any port to be put into OAM loopback, that is any packet received will be returned to the same port with an egressop of 0xFF which swaps the source and destination address. BPDUs will still flow through as normal so that OAM can be remotly requested and disabled.

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4.10.269 CPSW_SS_EGRESSOP Registers

4.10.269.1 CPSW_SS_EGRESSOP Register (Offset = FCh) [reset = 0h]

Short Description: Egress Operation

Long Description:

Return to Summary Table

Table 4-1422. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 00FCh

Figure 4-575. EGRESSOP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EGRESS_OP								EGRESS_TRK			TTL_CHECK	RESERVED			
R/W								R/W			R/W	NONE			
0								0			0	0			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DEST_PORTS		
NONE													R/W		
0													0		

Access Types Legend

Table 4-1423. EGRESSOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	EGRESS_OP	R/W	0h	The Egress Operation defines the operation performed by the CPSW Egress Packet Operations 0: NOP : 1-n: Defines which egress Operation will be performed. This allows Inter VLAN routing to be configured for high bandwidth traffic, reducing CPU load. 0xff: Swap SA and DA of packet, this is intended to allow OAM diagnostics for a link.
23 - 21	EGRESS_TRK	R/W	0h	The Egress Trunk Index is the calculated trunk index from the SA, DA or VLAN if modified to that InterVLAN routing will work on trunks as well. The DA, SA and VLAN are ignored for trunk generation on InterVLAN Routing so that this field is the index generated from the Egress Op replacements elclusive or'd together into a three bit index.
20	TTL_CHECK	R/W	0h	The TTL Check will cause any packet that fails TTL checks to not be routed to the Inter VLAN Routing sub functions. The packet will be routed to the host it was destined to.
	RESERVED	NONE		Reserved
2 - 0	DEST_PORTS	R/W	0h	The Destination Ports is a list of the ports the classified packet will be set to. If a destination is a Trunk, all the port bits for that trunck must be set.

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4.10.270 CPSW_SS_POLICECFG0 Registers

4.10.270.1 CPSW_SS_POLICECFG0 Register (Offset = 100h) [reset = 0h]

Short Description: Policing Config 0

Long Description:

Return to Summary Table

Table 4-1424. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0100h

Figure 4-576. POLICECFG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PORT_MEN	TRUNKID	RESERVED			PORT_NUM		RESERVED					PRI_MEN	PRI_VAL		
R/W	R/W	NONE			R/W		NONE					R/W	R/W		
0	0	0			0		0					0	0		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ONU_MEN	RESERVED						ONU_INDEX								
R/W	NONE						R/W								
0	0						0								

Access Types Legend

Table 4-1425. POLICECFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PORT_MEN	R/W	0h	Port Match Enable - Enabled port match for the selected policing/classifier entry
30	TRUNKID	R/W	0h	Trunk ID - When set indicates the port number is a trunk group.
	RESERVED	NONE		Reserved
26 - 25	PORT_NUM	R/W	0h	Port Number - Specifies the port address to match for the selected policing/classifier entry
	RESERVED	NONE		Reserved
19	PRI_MEN	R/W	0h	Priority Match Enable - Enables frame priority match for the selected policing/classifier entry
18 - 16	PRI_VAL	R/W	0h	Priority Value - Specifies the frame priority to match for the selected policing/classifier entry
15	ONU_MEN	R/W	0h	OUI Match Enable - Enables frame ONU address match for the selected policing/classifier entry
	RESERVED	NONE		Reserved
8 - 0	ONU_INDEX	R/W	0h	OUI Table Entry Index - Specifies the ALE ONU address lookup table index to match for the selected policing/classifier entry

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4.10.271 CPSW_SS_POLICECFG1 Registers

4.10.271.1 CPSW_SS_POLICECFG1 Register (Offset = 104h) [reset = 0h]

Short Description: Policing Config 1

Long Description:

Return to Summary Table

Table 4-1426. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0104h

Figure 4-577. POLICECFG1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DST_MEN	RESERVED						DST_INDEX								
R/W	NONE						R/W								
0	0						0								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC_MEN	RESERVED						SRC_INDEX								
R/W	NONE						R/W								
0	0						0								

Access Types Legend

Table 4-1427. POLICECFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DST_MEN	R/W	0h	Destination Address Match Enable - Enables frame L2 destination address match for the selected policing/classifier entry
	RESERVED	NONE		Reserved
24 - 16	DST_INDEX	R/W	0h	Destination Address Table Entry Index - Specifies the ALE L2 destination address lookup table index to match for the selected policing/classifier entry
15	SRC_MEN	R/W	0h	Source Address Match Enable - Enables frame L2 source address match for the selected policing/classifier entry
	RESERVED	NONE		Reserved
8 - 0	SRC_INDEX	R/W	0h	Source Address Table Entry Index - Specifies the ALE L2 source address lookup table index to match for the selected policing/classifier entry

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4.10.272 CPSW_SS_POLICECFG2 Registers

4.10.272.1 CPSW_SS_POLICECFG2 Register (Offset = 108h) [reset = 0h]

Short Description: Policing Config 2

Long Description:

Return to Summary Table

Table 4-1428. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0108h

Figure 4-578. POLICECFG2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OVLAN_MEN	RESERVED							OVLAN_INDEX							
R/W	NONE							R/W							
0	0							0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IVLAN_MEN	RESERVED							IVLAN_INDEX							
R/W	NONE							R/W							
0	0							0							

Access Types Legend

Table 4-1429. POLICECFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVLAN_MEN	R/W	0h	Outer VLAN Match Enable - Enables frame Outer VLAN address match for the selected policing/classifier entry
	RESERVED	NONE		Reserved
24 - 16	OVLAN_INDEX	R/W	0h	Outer VLAN Table Entry Index - Specifies the ALE Outer VLAN address lookup table index to match for the selected policing/ classifier entry
15	IVLAN_MEN	R/W	0h	Inner VLAN Match Enable - Enables frame Inner VLAN address match for the selected policing/classifier entry
	RESERVED	NONE		Reserved
8 - 0	IVLAN_INDEX	R/W	0h	Inner VLAN Table Entry Index - Specifies the ALE Inner VLAN address lookup table index to match for the selected policing/ classifier entry

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4.10.273 CPSW_SS_POLICECFG3 Registers

4.10.273.1 CPSW_SS_POLICECFG3 Register (Offset = 10Ch) [reset = 0h]

Short Description: Policing Config 3

Long Description:

Return to Summary Table

Table 4-1430. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 010Ch

Figure 4-579. POLICECFG3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ETHERTYPE_MEN	RESERVED						ETHERTYPE_INDEX								
R/W	NONE						R/W								
0	0						0								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IPSRC_MEN	RESERVED						IPSRC_INDEX								
R/W	NONE						R/W								
0	0						0								

Access Types Legend

Table 4-1431. POLICECFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ETHERTYPE_MEN	R/W	0h	EtherType Match Enable - Enables frame Ether Type match for the selected policing/classifier entry
	RESERVED	NONE		Reserved
24 - 16	ETHERTYPE_INDEX	R/W	0h	EtherType Table Entry Index - Specifies the ALE Ether Type lookup table index to match for the selected policing/classifier entry
15	IPSRC_MEN	R/W	0h	IP Source Address Match Enable - Enables frame IP Source address match for the selected policing/classifier entry
	RESERVED	NONE		Reserved
8 - 0	IPSRC_INDEX	R/W	0h	IP Source Address Table Entry Index - Specifies the ALE IP Source address lookup table index to match for the selected policing/classifier entry

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4.10.274 CPSW_SS_POLICECFG4 Registers

4.10.274.1 CPSW_SS_POLICECFG4 Register (Offset = 110h) [reset = 0h]

Short Description: Policing Config 4

Long Description:

Return to Summary Table

Table 4-1432. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0110h

Figure 4-580. POLICECFG4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IPDST_MEN	RESERVED						IPDST_INDEX								
R/W	NONE						R/W								
0	0						0								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1433. POLICECFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	IPDST_MEN	R/W	0h	IP Destination Address Match Enable - Enables frame IP Destination address match for the selected policing/classifier entry
	RESERVED	NONE		Reserved
24 - 16	IPDST_INDEX	R/W	0h	IP Destination Address Table Entry Index - Specifies the ALE IP Destination address lookup table index to match for the selected policing/classifier entry
	RESERVED	NONE		Reserved

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4.10.275 CPSW_SS_POLICECFG6 Registers

4.10.275.1 CPSW_SS_POLICECFG6 Register (Offset = 118h) [reset = 0h]

Short Description: Policing Config 6

Long Description:

Return to Summary Table

Table 4-1434. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0118h

Figure 4-581. POLICECFG6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PIR_IDLE_INC_VAL															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIR_IDLE_INC_VAL															
R/W															
0															

Access Types Legend

Table 4-1435. POLICECFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PIR_IDLE_INC_VAL	R/W	0h	Peak Information Rate Idle Increment Value - The number added to the PIR counter every clock cycle. If zero the PIR counter is disabled and packets will never be marked or processed as RED.

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4.10.276 CPSW_SS_POLICECFG7 Registers

4.10.276.1 CPSW_SS_POLICECFG7 Register (Offset = 11Ch) [reset = 0h]

Short Description: Policing Config 7

Long Description:

Return to Summary Table

Table 4-1436. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 011Ch

Figure 4-582. POLICECFG7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CIR_IDLE_INC_VAL															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CIR_IDLE_INC_VAL															
R/W															
0															

Access Types Legend

Table 4-1437. POLICECFG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CIR_IDLE_INC_VAL	R/W	0h	Committed Information Idle Increment Value - The number added to the CIR counter every clock cycle. If zero the CIR counter is disabled and packets will never be marked or processed as YELLOW.

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4.10.277 CPSW_SS_POLICETBLCTL Registers

4.10.277.1 CPSW_SS_POLICETBLCTL Register (Offset = 120h) [reset = 0h]

Short Description: Policing Table Control

Long Description:

Return to Summary Table

Table 4-1438. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0120h

Figure 4-583. POLICETBLCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WRITE_ENABLE	RESERVED														
R/W	NONE														
0	0														

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											POL_TBL_IDX				
NONE											R/W				
0											0				

Access Types Legend

Table 4-1439. POLICETBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRITE_ENABLE	R/W	0h	Write Enable - Setting this bit will write the POLICECFG0-7 to the ~ipol_tbl_idx selected policing/classifier entry. Clearing this bit will read the ~ipol_tbl_idx selected policing/classifier entry into the POLICECFG0-7 registers.
	RESERVED	NONE		Reserved
4 - 0	POL_TBL_IDX	R/W	0h	Policer Entry Index - This field specifies the policing/classifier entry to be read or written. When writing to this field without setting the ~iwrite_enable=1 will cause the selected policing/classifier entry to be loaded into the POLICECFG0-7 registers. When writing to this field with setting the ~iwrite_enable=1 will cause the selected policing/classifier entry to be updated from the POLICECFG0-7 registers.

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4.10.278 CPSW_SS_POLICECONTROL Registers

4.10.278.1 CPSW_SS_POLICECONTROL Register (Offset = 124h) [reset = 0h]

Short Description: Policing Control

Long Description:

Return to Summary Table

Table 4-1440. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0124h

Figure 4-584. POLICECONTROL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POLICING_EN	RESERVED	RED_DROP_EN	YELLOW_DROP_EN	RESERVED	YELLOWTHRESH			POLMCHMODE		PRIORITY_THREAD_EN	MAC_ONLY_DEF_DIS	RESERVED			
R/W	NONE	R/W	R/W	NONE	R/W			R/W		R/W	R/W	NONE			
0	0	0	0	0	0			0		0	0	0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1441. POLICECONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POLICING_EN	R/W	0h	Policing Enable - Enables the policing to color the packets, this also enables red or yellow drop capabilities.
	RESERVED	NONE		Reserved
29	RED_DROP_EN	R/W	0h	RED Drop Enable - Enables the ALE to drop the red colored packets.
28	YELLOW_DROP_EN	R/W	0h	WELLOW Drop Enable - Enables the ALE to drop yellow packets based on the ~iyellowthresh value. This field would normally not be used as to let the switch drop packets at a buffer threshold instead. In the event that the switch does not enable buffer threshold dropping, YELLOW packets can be dropped based on this feature.
	RESERVED	NONE		Reserved
26 - 24	YELLOWTHRESH	R/W	0h	Yellow Threshold - When set enables a portion of the yellow packets to be dropped based on the ~iyellow_drop_en enable. 0-100% 1=50% 2-33% 3-25% 4=20% 5-17% 6-14% 7-13%
23 - 22	POLMCHMODE	R/W	0h	Policing Match Mode - This field determines what happens to packets that fail to hit any policing/classifier entry. 0 - No Hit packets are marked GREEN 1 - No Hit packets are marked YELLOW 2 - No Hit packets are marked RED 3 - No Hit packets are marked based on policing/classifier entry=0 state.
21	PRIORITY_THREAD_EN	R/W	0h	Priority Thread Enable - This field determines if priority is OR'd to the default thread when no classifiers hit and the default thread is enabled.
20	MAC_ONLY_DEF_DIS	R/W	0h	MAC Only Default Disable - This field when set disables the default thread on MAC Only Ports. That is the default thread will be {port,priority}. If the traffic matches a classifier with a thread mapping, the classifier thread mapping still occurs.
	RESERVED	NONE		Reserved

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4.10.279 CPSW_SS_POLICETESTCTL Registers

4.10.279.1 CPSW_SS_POLICETESTCTL Register (Offset = 128h) [reset = 0h]

Short Description: Policing Test Control

Long Description:

Return to Summary Table

Table 4-1442. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0128h

Figure 4-585. POLICETESTCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POL_CLRALL_HIT	POL_CLRALL_REDHIT	POL_CLRALL_YELLOWHIT	POL_CLRSEL_ALL	RESERVED											
R/W	R/W	R/W	R/W	NONE											
0	0	0	0	0											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											POL_TEST_IDX				
NONE											R/W				
0											0				

Access Types Legend

Table 4-1443. POLICETESTCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POL_CLRALL_HIT	R/W	0h	Policer Clear - This bit clears all the policing/classifier hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit.
30	POL_CLRALL_REDHIT	R/W	0h	Policer Clear RED - This bit clears all the policing/classifier RED hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a RED condition.
29	POL_CLRALL_YELLOWHIT	R/W	0h	Policer Clear YELLOW - This bit clears all the policing/classifier YELLOW hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a YELLOW condition.
28	POL_CLRSEL_ALL	R/W	0h	Police Clear Selected - This bit clears the selected policing/classifier hit, redhit and yellowhit bits. This bit is self clearing.
	RESERVED	NONE		Reserved
4 - 0	POL_TEST_IDX	R/W	0h	Policer Test Index - This field selects which policing/classifier hit bits will be read or written.

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4.10.280 CPSW_SS_POLICEHSTAT Registers

4.10.280.1 CPSW_SS_POLICEHSTAT Register (Offset = 12Ch) [reset = 0h]

Short Description: Policing Hit Status

Long Description:

Return to Summary Table

Table 4-1444. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 012Ch

Figure 4-586. POLICEHSTAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
POL_HIT	POL_REDHIT	POL_YELLOWHIT	RESERVED												
R	R	R	NONE												
0	0	0	0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
NONE															
0															

Access Types Legend

Table 4-1445. POLICEHSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POL_HIT	R	0h	Policer Hit - This indicates that the selected policing/classifier via the ~ipol_test_idx field has been hit by a packet seen on any port that matches the policing/classifier entry match.
30	POL_REDHIT	R	0h	Policer Hit RED - This indicates that the selected policing/classifier via the ~ipol_test_idx field has been hit during a RED condition by a packet seen on any port that matches the policing/classifier entry match.
29	POL_YELLOWHIT	R	0h	Policer Hit YELLOW - This indicates that the selected policing/classifier via the ~ipol_test_idx field has been hit during a YELLOW condition by a packet seen on any port that matches the policing/classifier entry match.
	RESERVED	NONE		Reserved

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4.10.281 CPSW_SS_THREADMAPDEF Registers

4.10.281.1 CPSW_SS_THREADMAPDEF Register (Offset = 134h) [reset = 0h]

Short Description: THREAD Mapping Default Value

Long Description:

Return to Summary Table

Table 4-1446. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0134h

Figure 4-587. THREADMAPDEF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEFTHREAD_EN	RESERVED									DEFTHREADVAL					
R/W	NONE									R/W					
0	0									0					

Access Types Legend

Table 4-1447. THREADMAPDEF Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15	DEFTHREAD_EN	R/W	0h	Default Tread Enable - When set the switch will use the ~idefthreadval for the host interface thread ID if no classifier is matched. If clear the switch will generate its own thread ID based on port and priority if there is no classifier match.
	RESERVED	NONE		Reserved
5 - 0	DEFTHREADVAL	R/W	0h	Default Thread Value - This field specifies the default thread ID value.

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4.10.282 CPSW_SS_THREADMAPCTL Registers

4.10.282.1 CPSW_SS_THREADMAPCTL Register (Offset = 138h) [reset = 0h]

Short Description: THREAD Mapping Control

Long Description:

Return to Summary Table

Table 4-1448. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0138h

Figure 4-588. THREADMAPCTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											CLASSINDEX				
NONE											R/W				
0											0				

Access Types Legend

Table 4-1449. THREADMAPCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
4 - 0	CLASSINDEX	R/W	0h	Classifier Index - This is the classifier index entry that the thread enable and thread value will be read or written by the ~bTHREADMAPVAL register.

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4.10.283 CPSW_SS_THREADMAPVAL Registers

4.10.283.1 CPSW_SS_THREADMAPVAL Register (Offset = 13Ch) [reset = 0h]

Short Description: THREAD Mapping Value

Long Description:

Return to Summary Table

Table 4-1450. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 013Ch

Figure 4-589. THREADMAPVAL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
THREAD_EN	RESERVED									THREADVAL					
R/W	NONE									R/W					
0	0									0					

Access Types Legend

Table 4-1451. THREADMAPVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15	THREAD_EN	R/W	0h	Thread Enable - When set the switch will use the ~ithreadval for the selected classifier match. If clear the the thread ID will be determined by the ~bTHREADMAPDEF register settings.
	RESERVED	NONE		Reserved
5 - 0	THREADVAL	R/W	0h	Thread Value - This field is the thread ID value that is used to map a classifier hit to thread ID for host traffic.

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4.10.284 CPSW_SS_COMP_LOW_REG Registers

4.10.284.1 CPSW_SS_COMP_LOW_REG Register (Offset = 0h) [reset = 0h]

Short Description: comp_low_reg

Long Description:

Return to Summary Table

Table 4-1452. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0000h

Figure 4-590. COMP_LOW_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP_LOW															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_LOW															
R/W															
0															

Access Types Legend

Table 4-1453. COMP_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP_LOW	R/W	0h	Time Stamp ESTF Generate Function Comparison Low Value

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4.10.285 CPSW_SS_COMP_HIGH_REG Registers

4.10.285.1 CPSW_SS_COMP_HIGH_REG Register (Offset = 4h) [reset = 0h]

Short Description: comp_high_reg

Long Description:

Return to Summary Table

Table 4-1454. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0004h

Figure 4-591. COMP_HIGH_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMP_HIGH															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_HIGH															
R/W															
0															

Access Types Legend

Table 4-1455. COMP_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP_HIGH	R/W	0h	Time Stamp ESTF Generate Function Comparison High Value

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4.10.286 CPSW_SS_LENGTH_REG Registers

4.10.286.1 CPSW_SS_LENGTH_REG Register (Offset = Ch) [reset = 0h]

Short Description: length_reg

Long Description:

Return to Summary Table

Table 4-1456. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 000Ch

Figure 4-592. LENGTH_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LENGTH															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LENGTH															
R/W															
0															

Access Types Legend

Table 4-1457. LENGTH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	LENGTH	R/W	0h	Time Stamp ESTF Generate Function Length Value

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4.10.287 CPSW_SS_PPM_LOW_REG Registers

4.10.287.1 CPSW_SS_PPM_LOW_REG Register (Offset = 10h) [reset = 0h]

Short Description: ppm_low_reg

Long Description:

Return to Summary Table

Table 4-1458. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0010h

Figure 4-593. PPM_LOW_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PPM_LOW															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPM_LOW															
R/W															
0															

Access Types Legend

Table 4-1459. PPM_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PPM_LOW	R/W	0h	Time Stamp ESTF Generate Function PPM Low Value

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4.10.288 CPSW_SS_PPM_HIGH_REG Registers

4.10.288.1 CPSW_SS_PPM_HIGH_REG Register (Offset = 14h) [reset = 0h]

Short Description: ppm_high_reg

Long Description:

Return to Summary Table

Table 4-1460. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0014h

Figure 4-594. PPM_HIGH_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PPM_HIGH									
NONE						R/W									
0						0									

Access Types Legend

Table 4-1461. PPM_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	PPM_HIGH	R/W	0h	Time Stamp ESTF Generate Function PPM High Value

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4.10.289 CPSW_SS_NUDGE_REG Registers

4.10.289.1 CPSW_SS_NUDGE_REG Register (Offset = 18h) [reset = 0h]

Short Description: nudge_reg

Long Description:

Return to Summary Table

Table 4-1462. Instance Table

Instance Name	Physical Address
CPSW_SS	5280 0018h

Figure 4-595. NUDGE_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								NUDGE							
NONE								R/W							
0								0							

Access Types Legend

Table 4-1463. NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	NUDGE	R/W	0h	Time Stamp ESTF Generate Function Nudge Value

4.10.290 Access Table

Table 4-1464. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
R/W1TS	R/W1TS	Read/Write 1 To Set
R/W1TC	R/W1TC	Read/Write 1 To Clear
W	W	Write
RO	RO	Undefined
RW	RW	Undefined
WO	WO	Undefined

4.11 CPSW_ECC Registers

Table 4-1465. MSS_CPSW_ECC Registers Base Address Table

Offset	Length	Acronym	MSS_CPSW_ECC Physical Address
0h	32	CPSW_ECC_rev	5280 0000h
8h	32	CPSW_ECC_vector	5280 0008h
Ch	32	CPSW_ECC_stat	5280 000Ch
10h	32	CPSW_ECC_reserved_svbus	5280 0010h
3Ch	32	CPSW_ECC_sec_eoi_reg	5280 003Ch
40h	32	CPSW_ECC_sec_status_reg0	5280 0040h

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Table 4-1465. MSS_CPSW_ECC Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_CPSW_ECC Physical Address
80h	32	CPSW_ECC_sec_enable_set_reg0	5280 0080h
C0h	32	CPSW_ECC_sec_enable_clr_reg0	5280 00C0h
13Ch	32	CPSW_ECC_ded_eoi_reg	5280 013Ch
140h	32	CPSW_ECC_ded_status_reg0	5280 0140h
180h	32	CPSW_ECC_ded_enable_set_reg0	5280 0180h
1C0h	32	CPSW_ECC_ded_enable_clr_reg0	5280 01C0h
200h	32	CPSW_ECC_aggr_enable_set	5280 0200h
204h	32	CPSW_ECC_aggr_enable_clr	5280 0204h
208h	32	CPSW_ECC_aggr_status_set	5280 0208h
20Ch	32	CPSW_ECC_aggr_status_clr	5280 020Ch

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4.11.1 MSS_CPSW_ECC_REV Registers

4.11.1.1 CPSW_ECC_AGGR_REVISION Register (Offset = 0h) [reset = 66a02a01h]

Short Description: Aggregator Revision Register

Long Description:

Return to Summary Table

Table 4-1466. Instance Table

Instance Name	Physical Address
CPSW_ECC	5280 0000h

Figure 4-596. REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R		R		R											
1		10		11010100000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL				REVMAJ				CUSTOM		REVMIN					
R				R				R		R					
101				10				0		1					

Access Types Legend

Table 4-1467. AGGR_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	R	1h	Scheme
29 - 28	BU	R	Ah	bu
27 - 16	MODULE_ID	R	29040CB20h	Module ID
15 - 11	REVRTL	R	65h	RTL version
10 - 8	REVMAJ	R	Ah	Major version
7 - 6	CUSTOM	R	0h	Custom version
5 - 0	REVMIN	R	1h	Minor version

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4.11.2 MSS_CPSW_ECC_VECTOR Registers

4.11.2.1 CPSW_ECC_ECC_VECTOR Register (Offset = 8h) [reset = 0h]

Short Description: ECC Vector Register

Long Description:

Return to Summary Table

Table 4-1468. Instance Table

Instance Name	Physical Address
CPSW_ECC	5280 0008h

Figure 4-597. VECTOR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED							RD_SVBUS_DONE	RD_SVBUS_ADDRESS							
NONE							R/W1TC	R/W							
0							0	0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD_SVBUS	RESERVED				ECC_VECTOR										
R/W1TS	NONE				R/W										
0	0				0										

Access Types Legend

Table 4-1469. ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
24	RD_SVBUS_DONE	R/W1TC	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23 - 16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1TS	0h	Write 1 to trigger a read on the serial VBUS
	RESERVED	NONE		Reserved
10 - 0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

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4.11.3 MSS_CPSW_ECC_STAT Registers

4.11.3.1 CPSW_ECC_MISC_STATUS Register (Offset = Ch) [reset = 14h]

Short Description: Misc Status

Long Description:

Return to Summary Table

Table 4-1470. Instance Table

Instance Name	Physical Address
CPSW_ECC	5280 000Ch

Figure 4-598. STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					NUM_RAMS										
NONE					R										
0					10100										

Access Types Legend

Table 4-1471. MISC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 0	NUM_RAMS	R	2774h	Indicates the number of RAMS serviced by the ECC aggregator

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4.11.4 MSS_CPSW_ECC_RESERVED_SVBUS Registers

4.11.4.1 CPSW_ECC_RESERVED_SVBUS Register (Offset = 10h) [reset = 0h]

Short Description: Reserved Area for Serial VBUS Registers

Long Description:

Return to Summary Table

Table 4-1472. Instance Table

Instance Name	Physical Address
CPSW_ECC	5280 0010h

Figure 4-599. RESERVED_SVBUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															
R/W															
0															

Access Types Legend

Table 4-1473. RESERVED_SVBUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DATA	R/W	0h	Serial VBUS register data

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4.11.5 MSS_CPSW_ECC_SEC_EOI_REG Registers

4.11.5.1 CPSW_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-1474. Instance Table

Instance Name	Physical Address
CPSW_ECC	5280 003Ch

Figure 4-600. SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															EOI_WR
NONE															R/W1TS
0															0

Access Types Legend

Table 4-1475. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

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4.11.6 MSS_CPSW_ECC_SEC_STATUS_REG0 Registers

4.11.6.1 CPSW_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-1476. Instance Table

Instance Name	Physical Address
CPSW_ECC	5280 0040h

Figure 4-601. SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												RAMECC19_PEND	RAMECC18_PEND	RAMECC17_PEND	RAMECC16_PEND
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMECC15_PEND	RAMECC14_PEND	RAMECC13_PEND	RAMECC12_PEND	RAMECC11_PEND	RAMECC10_PEND	RAMECC9_PEND	RAMECC8_PEND	RAMECC7_PEND	RAMECC6_PEND	RAMECC5_PEND	RAMECC4_PEND	RAMECC3_PEND	RAMECC2_PEND	RAMECC1_PEND	RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1477. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19	RAMECC19_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc19_pend
18	RAMECC18_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc18_pend
17	RAMECC17_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc17_pend
16	RAMECC16_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc16_pend
15	RAMECC15_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc15_pend
14	RAMECC14_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc14_pend
13	RAMECC13_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc13_pend
12	RAMECC12_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc12_pend
11	RAMECC11_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc11_pend
10	RAMECC10_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc10_pend
9	RAMECC9_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc9_pend
8	RAMECC8_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc8_pend
7	RAMECC7_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc7_pend
6	RAMECC6_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc6_pend
5	RAMECC5_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc5_pend
4	RAMECC4_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc4_pend
3	RAMECC3_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc3_pend
2	RAMECC2_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc2_pend
1	RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc1_pend

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Table 4-1477. SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc0_pend

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4.11.7 MSS_CPSW_ECC_SEC_ENABLE_SET_REG0 Registers

4.11.7.1 CPSW_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-1478. Instance Table

Instance Name	Physical Address
CPSW_ECC	5280 0080h

Figure 4-602. SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												RAMECC19_ENABLE_SET	RAMECC18_ENABLE_SET	RAMECC17_ENABLE_SET	RAMECC16_ENABLE_SET
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMECC15_ENABLE_SET	RAMECC14_ENABLE_SET	RAMECC13_ENABLE_SET	RAMECC12_ENABLE_SET	RAMECC11_ENABLE_SET	RAMECC10_ENABLE_SET	RAMECC9_ENABLE_SET	RAMECC8_ENABLE_SET	RAMECC7_ENABLE_SET	RAMECC6_ENABLE_SET	RAMECC5_ENABLE_SET	RAMECC4_ENABLE_SET	RAMECC3_ENABLE_SET	RAMECC2_ENABLE_SET	RAMECC1_ENABLE_SET	RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1479. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19	RAMECC19_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc19_pend
18	RAMECC18_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc18_pend
17	RAMECC17_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc17_pend
16	RAMECC16_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc16_pend
15	RAMECC15_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc15_pend
14	RAMECC14_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc14_pend
13	RAMECC13_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc13_pend
12	RAMECC12_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc12_pend
11	RAMECC11_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc11_pend
10	RAMECC10_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc10_pend
9	RAMECC9_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc9_pend

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Table 4-1479. SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	RAMECC8_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc8_pend
7	RAMECC7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc7_pend
6	RAMECC6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc6_pend
5	RAMECC5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc5_pend
4	RAMECC4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc4_pend
3	RAMECC3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc3_pend
2	RAMECC2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc2_pend
1	RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc1_pend
0	RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc0_pend

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4.11.8 MSS_CPSW_ECC_SEC_ENABLE_CLR_REG0 Registers

4.11.8.1 CPSW_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-1480. Instance Table

Instance Name	Physical Address
CPSW_ECC	5280 00C0h

Figure 4-603. SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												RAMECC19_ENABLE_CLR	RAMECC18_ENABLE_CLR	RAMECC17_ENABLE_CLR	RAMECC16_ENABLE_CLR
NONE												R/W1TC	R/W1TC	R/W1TC	R/W1TC
0												0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMECC15_ENABLE_CLR	RAMECC14_ENABLE_CLR	RAMECC13_ENABLE_CLR	RAMECC12_ENABLE_CLR	RAMECC11_ENABLE_CLR	RAMECC10_ENABLE_CLR	RAMECC9_ENABLE_CLR	RAMECC8_ENABLE_CLR	RAMECC7_ENABLE_CLR	RAMECC6_ENABLE_CLR	RAMECC5_ENABLE_CLR	RAMECC4_ENABLE_CLR	RAMECC3_ENABLE_CLR	RAMECC2_ENABLE_CLR	RAMECC1_ENABLE_CLR	RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1481. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19	RAMECC19_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc19_pend
18	RAMECC18_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc18_pend
17	RAMECC17_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc17_pend
16	RAMECC16_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc16_pend
15	RAMECC15_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc15_pend
14	RAMECC14_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc14_pend
13	RAMECC13_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc13_pend
12	RAMECC12_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc12_pend
11	RAMECC11_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc11_pend
10	RAMECC10_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc10_pend

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Table 4-1481. SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc9_pend
8	RAMECC8_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc8_pend
7	RAMECC7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc7_pend
6	RAMECC6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc6_pend
5	RAMECC5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc5_pend
4	RAMECC4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc4_pend
3	RAMECC3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc3_pend
2	RAMECC2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc2_pend
1	RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc1_pend
0	RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc0_pend

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4.11.9 MSS_CPSW_ECC_DED_EOI_REG Registers

4.11.9.1 CPSW_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-1482. Instance Table

Instance Name	Physical Address
CPSW_ECC	5280 013Ch

Figure 4-604. DED_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															EOI_WR
NONE															R/W1TS
0															0

Access Types Legend

Table 4-1483. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
0	EOI_WR	R/W1TS	0h	EOI Register

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4.11.10 MSS_CPSW_ECC_DED_STATUS_REG0 Registers

4.11.10.1 CPSW_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-1484. Instance Table

Instance Name	Physical Address
CPSW_ECC	5280 0140h

Figure 4-605. DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												RAMECC19_PEND	RAMECC18_PEND	RAMECC17_PEND	RAMECC16_PEND
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMECC15_PEND	RAMECC14_PEND	RAMECC13_PEND	RAMECC12_PEND	RAMECC11_PEND	RAMECC10_PEND	RAMECC9_PEND	RAMECC8_PEND	RAMECC7_PEND	RAMECC6_PEND	RAMECC5_PEND	RAMECC4_PEND	RAMECC3_PEND	RAMECC2_PEND	RAMECC1_PEND	RAMECC_PEND
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1485. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19	RAMECC19_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc19_pend
18	RAMECC18_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc18_pend
17	RAMECC17_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc17_pend
16	RAMECC16_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc16_pend
15	RAMECC15_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc15_pend
14	RAMECC14_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc14_pend
13	RAMECC13_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc13_pend
12	RAMECC12_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc12_pend
11	RAMECC11_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc11_pend
10	RAMECC10_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc10_pend
9	RAMECC9_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc9_pend
8	RAMECC8_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc8_pend
7	RAMECC7_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc7_pend
6	RAMECC6_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc6_pend
5	RAMECC5_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc5_pend
4	RAMECC4_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc4_pend
3	RAMECC3_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc3_pend
2	RAMECC2_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc2_pend
1	RAMECC1_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc1_pend

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Table 4-1485. DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RAMECC_PEND	R/W1TS	0h	Interrupt Pending Status for ramecc0_pend

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4.11.11 MSS_CPSW_ECC_DED_ENABLE_SET_REG0 Registers

4.11.11.1 CPSW_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-1486. Instance Table

Instance Name	Physical Address
CPSW_ECC	5280 0180h

Figure 4-606. DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												RAMECC19_ENABLE_SET	RAMECC18_ENABLE_SET	RAMECC17_ENABLE_SET	RAMECC16_ENABLE_SET
NONE												R/W1TS	R/W1TS	R/W1TS	R/W1TS
0												0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMECC15_ENABLE_SET	RAMECC14_ENABLE_SET	RAMECC13_ENABLE_SET	RAMECC12_ENABLE_SET	RAMECC11_ENABLE_SET	RAMECC10_ENABLE_SET	RAMECC9_ENABLE_SET	RAMECC8_ENABLE_SET	RAMECC7_ENABLE_SET	RAMECC6_ENABLE_SET	RAMECC5_ENABLE_SET	RAMECC4_ENABLE_SET	RAMECC3_ENABLE_SET	RAMECC2_ENABLE_SET	RAMECC1_ENABLE_SET	RAMECC_ENABLE_SET
R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1487. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19	RAMECC19_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc19_pend
18	RAMECC18_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc18_pend
17	RAMECC17_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc17_pend
16	RAMECC16_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc16_pend
15	RAMECC15_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc15_pend
14	RAMECC14_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc14_pend
13	RAMECC13_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc13_pend
12	RAMECC12_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc12_pend
11	RAMECC11_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc11_pend
10	RAMECC10_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc10_pend
9	RAMECC9_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc9_pend

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Table 4-1487. DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	RAMECC8_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc8_pend
7	RAMECC7_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc7_pend
6	RAMECC6_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc6_pend
5	RAMECC5_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc5_pend
4	RAMECC4_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc4_pend
3	RAMECC3_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc3_pend
2	RAMECC2_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc2_pend
1	RAMECC1_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc1_pend
0	RAMECC_ENABLE_SET	R/W1TS	0h	Interrupt Enable Set Register for ramecc0_pend

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4.11.12 MSS_CPSW_ECC_DED_ENABLE_CLR_REG0 Registers

4.11.12.1 CPSW_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-1488. Instance Table

Instance Name	Physical Address
CPSW_ECC	5280 01C0h

Figure 4-607. DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												RAMECC19_ENABLE_CLR	RAMECC18_ENABLE_CLR	RAMECC17_ENABLE_CLR	RAMECC16_ENABLE_CLR
NONE												R/W1TC	R/W1TC	R/W1TC	R/W1TC
0												0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAMECC15_ENABLE_CLR	RAMECC14_ENABLE_CLR	RAMECC13_ENABLE_CLR	RAMECC12_ENABLE_CLR	RAMECC11_ENABLE_CLR	RAMECC10_ENABLE_CLR	RAMECC9_ENABLE_CLR	RAMECC8_ENABLE_CLR	RAMECC7_ENABLE_CLR	RAMECC6_ENABLE_CLR	RAMECC5_ENABLE_CLR	RAMECC4_ENABLE_CLR	RAMECC3_ENABLE_CLR	RAMECC2_ENABLE_CLR	RAMECC1_ENABLE_CLR	RAMECC_ENABLE_CLR
R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC	R/W1TC
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1489. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19	RAMECC19_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc19_pend
18	RAMECC18_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc18_pend
17	RAMECC17_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc17_pend
16	RAMECC16_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc16_pend
15	RAMECC15_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc15_pend
14	RAMECC14_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc14_pend
13	RAMECC13_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc13_pend
12	RAMECC12_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc12_pend
11	RAMECC11_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc11_pend
10	RAMECC10_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc10_pend

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Table 4-1489. DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RAMECC9_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc9_pend
8	RAMECC8_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc8_pend
7	RAMECC7_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc7_pend
6	RAMECC6_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc6_pend
5	RAMECC5_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc5_pend
4	RAMECC4_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc4_pend
3	RAMECC3_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc3_pend
2	RAMECC2_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc2_pend
1	RAMECC1_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc1_pend
0	RAMECC_ENABLE_CLR	R/W1TC	0h	Interrupt Enable Clear Register for ramecc0_pend

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4.11.13 MSS_CPSW_ECC_AGGR_ENABLE_SET Registers

4.11.13.1 CPSW_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

Short Description: AGGR interrupt enable set Register

Long Description:

Return to Summary Table

Table 4-1490. Instance Table

Instance Name	Physical Address
CPSW_ECC	5280 0200h

Figure 4-608. AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														TIMEOUT	PARITY
NONE														R/W1TS	R/W1TS
0														0	0

Access Types Legend

Table 4-1491. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	R/W1TS	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1TS	0h	interrupt enable set for parity errors

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4.11.14 MSS_CPSW_ECC_AGGR_ENABLE_CLR Registers

4.11.14.1 CPSW_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

Short Description: AGGR interrupt enable clear Register

Long Description:

Return to Summary Table

Table 4-1492. Instance Table

Instance Name	Physical Address
CPSW_ECC	5280 0204h

Figure 4-609. AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														TIMEOUT	PARITY
NONE														R/W1TC	R/W1TC
0														0	0

Access Types Legend

Table 4-1493. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	R/W1TC	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1TC	0h	interrupt enable clear for parity errors

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4.11.15 MSS_CPSW_ECC_AGGR_STATUS_SET Registers

4.11.15.1 CPSW_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

Short Description: AGGR interrupt status set Register

Long Description:

Return to Summary Table

Table 4-1494. Instance Table

Instance Name	Physical Address
CPSW_ECC	5280 0208h

Figure 4-610. AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TIMEOUT		PARITY	
NONE												R/WI		R/WI	
0												0		0	

Access Types Legend

Table 4-1495. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	R/WI	0h	interrupt status set for svbus timeout errors
1 - 0	PARITY	R/WI	0h	interrupt status set for parity errors

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4.11.16 MSS_CPSW_ECC_AGGR_STATUS_CLR Registers

4.11.16.1 CPSW_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

Short Description: AGGR interrupt status clear Register

Long Description:

Return to Summary Table

Table 4-1496. Instance Table

Instance Name	Physical Address
CPSW_ECC	5280 020Ch

Figure 4-611. AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TIMEOUT		PARITY	
NONE												R/WD		R/WD	
0												0		0	

Access Types Legend

Table 4-1497. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	R/WD	0h	interrupt status clear for svbus timeout errors
1 - 0	PARITY	R/WD	0h	interrupt status clear for parity errors

4.11.17 Access Table

Table 4-1498. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W1TC	R/W1TC	Read/Write 1 To Clear
R/W	R/W	Read / Write
R/W1TS	R/W1TS	Read/Write 1 To Set
R/WI	R/WI	Read/Write Increment. A write to this bit field increments the specified register bit field by the amount written.
R/WD	R/WD	Read/Write Decrement. A write to this bit field decrements the specified register bit field by the amount written.

4.12 DCC Registers

Table 4-1499. MSS_DCC[0:2] Registers Base Address Table

Offset	Length	Acronym	MSS_DCC0 Physical Address	MSS_DCC1 Physical Address	MSS_DCC2 Physical Address
0h	32	DCC_DCCGCTRL	52B0 0000h	52B0 1000h	52B0 2000h
4h	32	DCC_DCCREV	52B0 0004h	52B0 1004h	52B0 2004h

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Table 4-1499. MSS_DCC[0:2] Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_DCC0 Physical Address	MSS_DCC1 Physical Address	MSS_DCC2 Physical Address
8h	32	DCC_DCCCNTSEED0	52B0 0008h	52B0 1008h	52B0 2008h
Ch	32	DCC_DCCVALIDSEED0	52B0 000Ch	52B0 100Ch	52B0 200Ch
10h	32	DCC_DCCCNTSEED1	52B0 0010h	52B0 1010h	52B0 2010h
14h	32	DCC_DCCSTATUS	52B0 0014h	52B0 1014h	52B0 2014h
18h	32	DCC_DCCCNT0	52B0 0018h	52B0 1018h	52B0 2018h
1Ch	32	DCC_DCCVALID0	52B0 001Ch	52B0 101Ch	52B0 201Ch
20h	32	DCC_DCCCNT1	52B0 0020h	52B0 1020h	52B0 2020h
24h	32	DCC_DCCCLKSRC1	52B0 0024h	52B0 1024h	52B0 2024h
28h	32	DCC_DCCCLKSRC0	52B0 0028h	52B0 1028h	52B0 2028h
2Ch	32	DCC_DCCGCTRL2	52B0 002Ch	52B0 102Ch	52B0 202Ch
30h	32	DCC_DCCSTATUS2	52B0 0030h	52B0 1030h	52B0 2030h
34h	32	DCC_DCCERRCNT	52B0 0034h	52B0 1034h	52B0 2034h

Table 4-1500. MSS_DCC3 Registers Base Address Table

Offset	Length	Acronym	MSS_DCC3 Physical Address
0h	32	DCC_DCCGCTRL	52B0 3000h
4h	32	DCC_DCCREV	52B0 3004h
8h	32	DCC_DCCCNTSEED0	52B0 3008h
Ch	32	DCC_DCCVALIDSEED0	52B0 300Ch
10h	32	DCC_DCCCNTSEED1	52B0 3010h
14h	32	DCC_DCCSTATUS	52B0 3014h
18h	32	DCC_DCCCNT0	52B0 3018h
1Ch	32	DCC_DCCVALID0	52B0 301Ch
20h	32	DCC_DCCCNT1	52B0 3020h
24h	32	DCC_DCCCLKSRC1	52B0 3024h
28h	32	DCC_DCCCLKSRC0	52B0 3028h
2Ch	32	DCC_DCCGCTRL2	52B0 302Ch
30h	32	DCC_DCCSTATUS2	52B0 3030h
34h	32	DCC_DCCERRCNT	52B0 3034h

4.12.1 MSS_DCC Instance Count Note

Note

n = 0 to 3 for the MSS_DCC registers defined below

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4.12.2 MSS_DCCn_DCCGCTRL Registers

4.12.2.1 DCCn_DCCGCTRL Register (Offset = 0h) [reset = 5555h]

Short Description: DCC Global Control Register

Long Description:

Return to Summary Table

Table 4-1501. Instance Table

Instance Name	Physical Address
DCC0	52B0 0000h
DCC1	52B0 1000h
DCC2	52B0 2000h
DCC3	52B0 3000h

Figure 4-612. DCC_DCCGCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DONEENA				SINGLESHOT				ERRENA				DCCENA			
R/W				R/W				R/W				R/W			
101				101				101				101			

Access Types Legend

Table 4-1502. DCCGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 12	DONEENA	R/W	65h	The DONEENA bit enables/disables the done interrupt signal, but has no effect on the done status flag in DCCSTAT register. User, privilege, and debug mode (read): 0101 = the done signal is disabled others = the done signal is enabled Privilege and debug mode (write): 0101 = disable done signal generation others = enable done signal generation
11 - 8	SINGLESHOT	R/W	65h	The SINGLESHOT bit enables/disables repetitive operation of the DCC. User, privilege, and debug mode (read): 1010 = stop counting when counter0 and valid0 both reach zero 1011 = stop counting when counter1 reaches zero others = continuously repeat (until error) Privilege and debug mode (write): 1010 = stop counting when counter0 and valid0 both reach zero 1011 = stop counting when counter1 reaches zero others = continuously repeat (until error)
7 - 4	ERRENA	R/W	65h	The ERRENA bit enables/disables the error signal. User, privilege, and debug mode (read): 0101 = the error signal is disabled others = the error signal is enabled Privilege and debug mode (write): 0101 = disable error signal generation others = enable error signal generation
3 - 0	DCCENA	R/W	65h	The DCCENA bit starts and stops the operation of the dcc. User, privilege, and debug mode (read): 0101 = counters are stopped others = counters are running Privilege and debug mode (write): 0101 = stop counters and error-checking others = load the counters with their seed values and begin counting

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4.12.3 MSS_DCCn_DCCREV Registers

4.12.3.1 DCCn_DCCREV Register (Offset = 4h) [reset = 40010300h]

Short Description: DCC Revision ID

Long Description:

Return to Summary Table

Table 4-1503. Instance Table

Instance Name	Physical Address
DCC0	52B0 0004h
DCC1	52B0 1004h
DCC2	52B0 2004h
DCC3	52B0 3004h

Figure 4-613. DCC_DCCREV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RESERVED		FUNC											
R		NONE		R											
1		0		1											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL				MAJOR				CUSTOM		MINOR					
R				R				R		R					
0				11				0		0					

Access Types Legend

Table 4-1504. DCCREV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	R	1h	User, privilege, and debug mode (read): Returns 01. Privilege and debug mode (write): Writes have no effect.
	RESERVED	NONE		Reserved
27 - 16	FUNC	R	1h	Reflects software-compatability. If there is no level of software compatability, a unique func number is assigned; for compatible modules, the same number is maintained. User, privilege, and debug mode (read): 0x0 Privilege and debug mode (write): Writes have no effect.
15 - 11	RTL	R	0h	Incremented for releases due to spec changes or post-release design changes. Reset to 0 when either MAJOR or MINOR is incremented. User, privilege, and debug mode (read): 0x0 Privilege and debug mode (write): Writes have no effect.
10 - 8	MAJOR	R	Bh	Represents major changes to the module (e.g. entirely new features are added/changed). The major revision number for this module. User, privilege, and debug mode (read): 0x2 Privilege and debug mode (write): Writes have no effect.
7 - 6	CUSTOM	R	0h	Indicates a special version of the module. May not be supported by standard software. User, privilege, and debug mode (read): 0x0 Privilege and debug mode (write): Writes have no effect.
5 - 0	MINOR	R	0h	Represents minor changes to the module (e.g. enhancements to existing features). The minor revision number for this module. User, privilege, and debug mode (read): 0x4 Privilege and debug mode (write): Writes have no effect.

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4.12.4 MSS_DCCn_DCCCNTSEED0 Registers

4.12.4.1 DCCn_DCCCNTSEED0 Register (Offset = 8h) [reset = 0h]

Short Description: Count0 Seed Value Register

Long Description:

Return to Summary Table

Table 4-1505. Instance Table

Instance Name	Physical Address
DCC0	52B0 0008h
DCC1	52B0 1008h
DCC2	52B0 2008h
DCC3	52B0 3008h

Figure 4-614. DCC_DCCCNTSEED0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												COUNTSEED0			
NONE												R/W			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTSEED0															
R/W															
0															

Access Types Legend

Table 4-1506. DCCCNTSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	COUNTSEED0	R/W	0h	This field contains the seed value that gets loaded into counter 0 (clock source 0). User, privilege, and debug mode (read): Returns the current seed value for counter 0. Privilege and debug mode (write): Sets the current seed value for counter 0.

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4.12.5 MSS_DCCn_DCCVALIDSEED0 Registers

4.12.5.1 DCCn_DCCVALIDSEED0 Register (Offset = Ch) [reset = 0h]

Short Description: Valid0 Seed Value Register

Long Description:

Return to Summary Table

Table 4-1507. Instance Table

Instance Name	Physical Address
DCC0	52B0 000Ch
DCC1	52B0 100Ch
DCC2	52B0 200Ch
DCC3	52B0 300Ch

Figure 4-615. DCC_DCCVALIDSEED0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALIDSEED0															
R/W															
0															

Access Types Legend

Table 4-1508. DCCVALIDSEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	VALIDSEED0	R/W	0h	This field contains the seed value that gets loaded into the valid duration counter for clock source 0. User, privilege, and debug mode (read): Returns the current seed value for VALID0. Privilege and debug mode (write): Sets the current seed value for VALID0.

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4.12.6 MSS_DCCn_DCCCNTSEED1 Registers

4.12.6.1 DCCn_DCCCNTSEED1 Register (Offset = 10h) [reset = 0h]

Short Description: Count1 Seed Value Register

Long Description:

Return to Summary Table

Table 4-1509. Instance Table

Instance Name	Physical Address
DCC0	52B0 0010h
DCC1	52B0 1010h
DCC2	52B0 2010h
DCC3	52B0 3010h

Figure 4-616. DCC_DCCCNTSEED1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												COUNTSEED1			
NONE												R/W			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTSEED1															
R/W															
0															

Access Types Legend

Table 4-1510. DCCCNTSEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	COUNTSEED1	R/W	0h	This field contains the seed value that gets loaded into counter 1 (clock source 1). User, privilege, and debug mode (read): Returns the current seed value for counter 1. Privilege and debug mode (write): Sets the current seed value for counter 1.

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4.12.7 MSS_DCCn_DCCSTATUS Registers

4.12.7.1 DCCn_DCCSTAT Register (Offset = 14h) [reset = 0h]

Short Description: DCC Status Register

Long Description:

Return to Summary Table

Table 4-1511. Instance Table

Instance Name	Physical Address
DCC0	52B0 0014h
DCC1	52B0 1014h
DCC2	52B0 2014h
DCC3	52B0 3014h

Figure 4-617. DCC_DCCSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														DONEFLG	ERRFLG
NONE														R/W1TC	R/W1TC
0														0	0

Access Types Legend

Table 4-1512. DCCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	DONEFLG	R/W1TC	0h	Indicates when single-shot mode is complete without error. Writing a 1 to this bit clears the flag. User, privilege, and debug mode (read): 0 = single-shot mode is not done 1 = single-shot mode is done Privilege and debug mode (write): 0 = no effect 1 = clear the done flag
0	ERRFLG	R/W1TC	0h	Indicates whether or not an error has occured. Writing a 1 to this bit clears the flag. User, privilege, and debug mode (read): 0 = an error has not occurred 1 = an error has occurred Privilege and debug mode (write): 0 = no effect 1 = clear the error flag

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4.12.8 MSS_DCCn_DCCCNT0 Registers

4.12.8.1 DCCn_DCCCNT0 Register (Offset = 18h) [reset = 0h]

Short Description: Count0 Value Register

Long Description:

Return to Summary Table

Table 4-1513. Instance Table

Instance Name	Physical Address
DCC0	52B0 0018h
DCC1	52B0 1018h
DCC2	52B0 2018h
DCC3	52B0 3018h

Figure 4-618. DCC_DCCCNT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												COUNT0			
NONE												R			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT0															
R															
0															

Access Types Legend

Table 4-1514. DCCCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	COUNT0	R	0h	This field contains the current value of counter 0. User, privilege, and debug mode (read): Returns the current value for counter 0. Privilege and debug mode (write): Writes have no effect.

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4.12.9 MSS_DCCn_DCCVALID0 Registers

4.12.9.1 DCCn_DCCVALID0 Register (Offset = 1Ch) [reset = 0h]

Short Description: Valid0 Value Register

Long Description:

Return to Summary Table

Table 4-1515. Instance Table

Instance Name	Physical Address
DCC0	52B0 001Ch
DCC1	52B0 101Ch
DCC2	52B0 201Ch
DCC3	52B0 301Ch

Figure 4-619. DCC_DCCVALID0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALID0															
R															
0															

Access Types Legend

Table 4-1516. DCCVALID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 0	VALID0	R	0h	This field contains the current value of valid counter 0. User, privilege, and debug mode (read): Returns the current value for valid counter 0. Privilege and debug mode (write): writes have no effect.

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4.12.10 MSS_DCCn_DCCCNT1 Registers

4.12.10.1 DCCn_DCCCNT1 Register (Offset = 20h) [reset = 0h]

Short Description: Count1 Value Register

Long Description:

Return to Summary Table

Table 4-1517. Instance Table

Instance Name	Physical Address
DCC0	52B0 0020h
DCC1	52B0 1020h
DCC2	52B0 2020h
DCC3	52B0 3020h

Figure 4-620. DCC_DCCCNT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												COUNT1			
NONE												R			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT1															
R															
0															

Access Types Legend

Table 4-1518. DCCCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
19 - 0	COUNT1	R	0h	This field contains the current value of counter 1. User, privilege, and debug mode (read): Returns the current value for counter 1. Privilege and debug mode (write): writes have no effect.

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4.12.11 MSS_DCCn_DCCCLKSRC1 Registers

4.12.11.1 DCCn_DCCCLKSRC1 Register (Offset = 24h) [reset = 0h]

Short Description: Clock Source Selection Register 1

Long Description:

Return to Summary Table

Table 4-1519. Instance Table

Instance Name	Physical Address
DCC0	52B0 0024h
DCC1	52B0 1024h
DCC2	52B0 2024h
DCC3	52B0 3024h

Figure 4-621. DCC_DCCCLKSRC1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY				RESERVED							CLKSRC1				
R/W				NONE							R/W				
0				0							0				

Access Types Legend

Table 4-1520. DCCCLKSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 12	KEY	R/W	0h	This field enables or disables clock source selection for counter 1. User, privilege, and debug mode (read): Returns the current value of the key. Privilege and debug mode (write): Sets the key value. Key values: 1010: The CLKSRC field selects the clock source for counter 1. others: Clock source selection is disabled. The secondary oscillator (clock source 1) is selected for counter 1.
	RESERVED	NONE		Reserved
4 - 0	CLKSRC1	R/W	0h	This field specifies the clock source for counter 1, when the KEY field enables this feature. User, privilege, and debug mode (read): Returns the current value of CLKSRC. Privilege and debug mode (write): Sets the value of CLKSRC.

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4.12.12 MSS_DCCn_DCCCLKSRC0 Registers

4.12.12.1 DCCn_DCCCLKSRC0 Register (Offset = 28h) [reset = 0h]

Short Description: Clock Source Selection Register 0

Long Description:

Return to Summary Table

Table 4-1521. Instance Table

Instance Name	Physical Address
DCC0	52B0 0028h
DCC1	52B0 1028h
DCC2	52B0 2028h
DCC3	52B0 3028h

Figure 4-622. DCC_DCCCLKSRC0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY				RESERVED								CLKSRC0			
R/W				NONE								R/W			
0				0								0			

Access Types Legend

Table 4-1522. DCCCLKSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
15 - 12	KEY	R/W	0h	This field enables or disables clock source selection for counter 0. User, privilege, and debug mode (read): Returns the current value of the key. Privilege and debug mode (write): Sets the key value. Key values: 1010: The CLKSRC field selects the clock source for counter 0. others: Clock source selection is disabled. The external oscillator (XTAL) is selected for counter 0.
	RESERVED	NONE		Reserved
3 - 0	CLKSRC0	R/W	0h	This field specifies the clock source for counter 0. User, privilege, and debug mode (read): Returns the current value of CLKSRC0. Privilege and debug mode (write): Sets the value of CLKSRC0.

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4.12.13 MSS_DCCn_DCCGCTRL2 Registers

4.12.13.1 DCCn_DCCGCTRL2 Register (Offset = 2Ch) [reset = 555h]

Short Description: DCC Global Control Register 2

Long Description:

Return to Summary Table

Table 4-1523. Instance Table

Instance Name	Physical Address
DCC0	52B0 002Ch
DCC1	52B0 102Ch
DCC2	52B0 202Ch
DCC3	52B0 302Ch

Figure 4-623. DCC_DCCGCTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				FIFO_NONERR				FIFO_READ				CONT_ON_ERR			
NONE				R/W				R/W				R/W			
0				101				101				101			

Access Types Legend

Table 4-1524. DCCGCTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
11 - 8	FIFO_NONERR	R/W	65h	Enables/disables FIFO writes without the error event on completion of comparison window. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Source values: 0101: Counter values are captured to non-full FIFO only upon Error event. Others: Write counter values to non-full FIFO upon completion of comparison window regardless of error or not.
7 - 4	FIFO_READ	R/W	65h	Enables the counter read registers reflect FIFO output instead of the live counter value. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Source values: 0101: Counter value is read directly. Others: Counters FIFO output is read.
3 - 0	CONT_ON_ERR	R/W	65h	Continues to next window of comparison despite the error condition. User, privilege, and debug mode (read): Returns the current field value. Privilege and debug mode (write): Sets the value of field value. Enable values: 0101: Comparison and counter reload is stopped from advancing if error is detected. Others: Counters get reloaded with seed and continue counting despite the error condition.

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4.12.14 MSS_DCCn_DCCSTATUS2 Registers

4.12.14.1 DCCn_DCCSTATUS2 Register (Offset = 30h) [reset = 7h]

Short Description: DCC FIFO Status Register

Long Description:

Return to Summary Table

Table 4-1525. Instance Table

Instance Name	Physical Address
DCC0	52B0 0030h
DCC1	52B0 1030h
DCC2	52B0 2030h
DCC3	52B0 3030h

Figure 4-624. DCC_DCCSTATUS2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										COUNT1_FIFO_FULL	VALID0_FIFO_FULL	COUNT0_FIFO_FULL	COUNT1_FIFO_EMPTY	VALID0_FIFO_EMPTY	COUNT0_FIFO_EMPTY
NONE										R	R	R	R	R	R
0										0	0	0	1	1	1

Access Types Legend

Table 4-1526. DCCSTATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
5	COUNT1_FIFO_FULL	R	0h	Count1 FIFO Full. Indicates whether Count1 FIFO is full. User, privilege, and debug mode (read): 0: Count1 FIFO is not full 1: Count1 FIFO is full. Privilege and debug mode (write): Writes have no effect.
4	VALID0_FIFO_FULL	R	0h	Valid0 FIFO Full. Indicates whether Valid0 FIFO is full. User, privilege, and debug mode (read): 0: Valid0 FIFO is not full 1: Valid0 FIFO is full. Privilege and debug mode (write): Writes have no effect.
3	COUNT0_FIFO_FULL	R	0h	Count0 FIFO Full. Indicates whether Count0 FIFO is full. User, privilege, and debug mode (read): 0: Count0 FIFO is not full 1: Count0 FIFO is full. Privilege and debug mode (write): Writes have no effect.
2	COUNT1_FIFO_EMPTY	R	1h	Count1 FIFO Empty. Indicates whether Count1 FIFO is empty. User, privilege, and debug mode (read): 0: Count1 FIFO is not empty 1: Count1 FIFO is empty. Privilege and debug mode (write): Writes have no effect.
1	VALID0_FIFO_EMPTY	R	1h	Valid0 FIFO Empty. Indicates whether Valid0 FIFO is empty. User, privilege, and debug mode (read): 0: Valid0 FIFO is not empty 1: Valid0 FIFO is empty. Privilege and debug mode (write): Writes have no effect.
0	COUNT0_FIFO_EMPTY	R	1h	Count0 FIFO Empty. Indicates whether Count0 FIFO is empty. User, privilege, and debug mode (read): 0: Count0 FIFO is not empty 1: Count0 FIFO is empty. Privilege and debug mode (write): Writes have no effect.

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4.12.15 MSS_DCCn_DCCERRCNT Registers

4.12.15.1 DCCn_DCCERRCNT Register (Offset = 34h) [reset = 0h]

Short Description: Error Count Register

Long Description:

Return to Summary Table

Table 4-1527. Instance Table

Instance Name	Physical Address
DCC0	52B0 0034h
DCC1	52B0 1034h
DCC2	52B0 2034h
DCC3	52B0 3034h

Figure 4-625. DCC_DCCERRCNT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						ERRCNT									
NONE						R/W									
0						0									

Access Types Legend

Table 4-1528. DCCERRCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 0	ERRCNT	R/W	0h	Counts the number of errors after the last write to this register or reset. If reached terminal count the count freezes. User needs to clear it.

4.12.16 Access Table

Table 4-1529. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write
R	R	Read
R/W1TC	R/W1TC	Read/Write 1 To Clear

4.13 ECC_AGG_TOP Registers

Table 4-1530. MSS_ECC_AGG_TOP Registers Base Address Table

Offset	Length	Acronym	MSS_ECC_AGG_TOP Physical Address
0h	32	ECC_AGG_TOP_REV	5301 0000h
8h	24	ECC_AGG_TOP_VECTOR	5301 0008h
Ch	16	ECC_AGG_TOP_STAT	5301 000Ch
14h	8	ECC_AGG_TOP_CTRL	5301 0014h
18h	32	ECC_AGG_TOP_ERR_CTRL1	5301 0018h
1Ch	32	ECC_AGG_TOP_ERR_CTRL2	5301 001Ch
20h	32	ECC_AGG_TOP_ERR_STAT1	5301 0020h

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Table 4-1530. MSS_ECC_AGG_TOP Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_ECC_AGG_TOP Physical Address
24h	32	ECC_AGG_TOP_ERR_STAT2	5301 0024h
28h	16	ECC_AGG_TOP_ERR_STAT3	5301 0028h
3Ch	0	ECC_AGG_TOP_SEC_EOI_REG	5301 003Ch
40h	8	ECC_AGG_TOP_SEC_STATUS_REG0	5301 0040h
80h	8	ECC_AGG_TOP_SEC_ENABLE_SET_REG0	5301 0080h
C0h	8	ECC_AGG_TOP_SEC_ENABLE_CLR_REG0	5301 00C0h
13Ch	0	ECC_AGG_TOP_DED_EOI_REG	5301 013Ch
140h	8	ECC_AGG_TOP_DED_STATUS_REG0	5301 0140h
180h	8	ECC_AGG_TOP_DED_ENABLE_SET_REG0	5301 0180h
1C0h	8	ECC_AGG_TOP_DED_ENABLE_CLR_REG0	5301 01C0h
200h	8	ECC_AGG_TOP_AGGR_ENABLE_SET	5301 0200h
204h	8	ECC_AGG_TOP_AGGR_ENABLE_CLR	5301 0204h
208h	8	ECC_AGG_TOP_AGGR_STATUS_SET	5301 0208h
20Ch	8	ECC_AGG_TOP_AGGR_STATUS_CLR	5301 020Ch

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4.13.1 MSS_ECC_AGG_TOP_REV Registers

4.13.1.1 ECC_AGG_TOP_REV Register (Offset = 0h) [reset = h]

Short Description: Revision parameters

Long Description:

Return to Summary Table

Table 4-1531. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0000h

Access Types Legend

Table 4-1532. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	2h	bu
27 - 16	MODULE_ID	RO	6A0h	Module ID
15 - 11	REVRTL	RO	1Dh	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	0h	Minor version

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4.13.2 MSS_ECC_AGG_TOP_VECTOR Registers

4.13.2.1 ECC_AGG_TOP_VECTOR Register (Offset = 8h) [reset = h]

Short Description: ECC Vector Register

Long Description:

Return to Summary Table

Table 4-1533. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0008h

Access Types Legend

Table 4-1534. VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
24	RD_SVBUS_DONE	RW	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23 - 16	RD_SVBUS_ADDRESS	RW	0h	Read address
15	RD_SVBUS	RW	0h	Write 1 to trigger a read on the serial VBUS
	RESERVED	NONE		Reserved
10 - 0	ECC_VECTOR	RW	0h	Value written to select the corresponding ECC RAM for control or status

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4.13.3 MSS_ECC_AGG_TOP_STAT Registers

4.13.3.1 ECC_AGG_TOP_STAT Register (Offset = Ch) [reset = h]

Short Description: Misc Status

Long Description:

Return to Summary Table

Table 4-1535. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 000Ch

Access Types Legend

Table 4-1536. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 0	NUM_RAMS	RO	9h	Indicates the number of RAMS serviced by the ECC aggregator

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4.13.4 MSS_ECC_AGG_TOP_CTRL Registers

4.13.4.1 ECC_AGG_TOP_CTRL Register (Offset = 14h) [reset = h]

Short Description: ECC Control Register

Long Description:

Return to Summary Table

Table 4-1537. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0014h

Access Types Legend

Table 4-1538. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
8	CHECK_SVBUS_TIMEOUT	RW	1h	check for svbus timeout errors
7	CHECK_PARITY	RW	1h	check for parity errors
6	ERROR_ONCE	RW	0h	Force Error only once
5	FORCE_N_ROW	RW	0h	Force Error on any RAM read
4	FORCE_DED	RW	0h	Force Double Bit Error
3	FORCE_SEC	RW	0h	Force Single Bit Error
2	ENABLE_RMW	RW	1h	Enable rmw
1	ECC_CHECK	RW	1h	Enable ECC check
0	ECC_ENABLE	RW	1h	Enable ECC

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4.13.5 MSS_ECC_AGG_TOP_ERR_CTRL1 Registers

4.13.5.1 ECC_AGG_TOP_ERR_CTRL1 Register (Offset = 18h) [reset = h]

Short Description: ECC Error Control1 Register

Long Description:

Return to Summary Table

Table 4-1539. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0018h

Access Types Legend

Table 4-1540. ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RW	0h	Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

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4.13.6 MSS_ECC_AGG_TOP_ERR_CTRL2 Registers

4.13.6.1 ECC_AGG_TOP_ERR_CTRL2 Register (Offset = 1Ch) [reset = h]

Short Description: ECC Error Control2 Register

Long Description:

Return to Summary Table

Table 4-1541. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 001Ch

Access Types Legend

Table 4-1542. ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT2	RW	0h	Data bit that needs to be flipped if double bit error needs to be forced
15 - 0	ECC_BIT1	RW	0h	Data bit that needs to be flipped when force_sec is set

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4.13.7 MSS_ECC_AGG_TOP_ERR_STAT1 Registers

4.13.7.1 ECC_AGG_TOP_ERR_STAT1 Register (Offset = 20h) [reset = h]

Short Description: ECC Error Status1 Register

Long Description:

Return to Summary Table

Table 4-1543. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0020h

Access Types Legend

Table 4-1544. ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT1	RO	0h	Data bit that corresponds to the single-bit error
15	CLR_CTRL_REG_ERR	RW	0h	Clear control reg error Error Status, you must also re write the contorl ergister itself to clear this
14 - 13	CLR_PARITY_ERR	RW DECR	0h	Clear parity Error Status
12	CLR_ECC_OTHER	RW	0h	Clear other Error Status
11 - 10	CLR_ECC_DED	RW DECR	0h	Clear Double Bit Error Status
9 - 8	CLR_ECC_SEC	RW DECR	0h	Clear Single Bit Error Status
7	CTR_REG_ERR	RW	0h	control register error pending, Level interrupt
6 - 5	PARITY_ERR	RW	0h	Level parity error Error Status
4	ECC_OTHER	RW	0h	successive single-bit errors have occurred while a writeback is still pending, Level interrupt
3 - 2	ECC_DED	RW INCR	0h	Level Double Bit Error Status
1 - 0	ECC_SEC	RW INCR	0h	Level Single Bit Error Status

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4.13.8 MSS_ECC_AGG_TOP_ERR_STAT2 Registers

4.13.8.1 ECC_AGG_TOP_ERR_STAT2 Register (Offset = 24h) [reset = h]

Short Description: ECC Error Status2 Register

Long Description:

Return to Summary Table

Table 4-1545. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0024h

Access Types Legend

Table 4-1546. ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RO	0h	Row address where the single or double-bit error has occurred

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4.13.9 MSS_ECC_AGG_TOP_ERR_STAT3 Registers

4.13.9.1 ECC_AGG_TOP_ERR_STAT3 Register (Offset = 28h) [reset = h]

Short Description: ECC Error Status3 Register

Long Description:

Return to Summary Table

Table 4-1547. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0028h

Access Types Legend

Table 4-1548. ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	CLR_SVBUS_TIMEOUT_ERR	RW	0h	Clear svbus timeout Error Status
	RESERVED	NONE		Reserved
1	SVBUS_TIMEOUT_ERR	RW	0h	Level svbus timeout error Error Status
0	WB_PEND	RO	0h	delayed write back pending Status

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4.13.10 MSS_ECC_AGG_TOP_SEC_EOI_REG Registers

4.13.10.1 ECC_AGG_TOP_SEC_EOI_REG Register (Offset = 3Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-1549. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 003Ch

Access Types Legend

Table 4-1550. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

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4.13.11 MSS_ECC_AGG_TOP_SEC_STATUS_REG0 Registers

4.13.11.1 ECC_AGG_TOP_SEC_STATUS_REG0 Register (Offset = 40h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-1551. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0040h

Access Types Legend

Table 4-1552. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_PEND	RW	0h	Interrupt Pending Status for tptc_a1_pend
5	TPTC_A0_PEND	RW	0h	Interrupt Pending Status for tptc_a0_pend
4	MSS_MBOX_PEND	RW	0h	Interrupt Pending Status for mss_mbox_pend
3	MSS_L2SLV3_PEND	RW	0h	Interrupt Pending Status for mss_l2slv3_pend
2	MSS_L2SLV2_PEND	RW	0h	Interrupt Pending Status for mss_l2slv2_pend
1	MSS_L2SLV1_PEND	RW	0h	Interrupt Pending Status for mss_l2slv1_pend
0	MSS_L2SLV0_PEND	RW	0h	Interrupt Pending Status for mss_l2slv0_pend

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4.13.12 MSS_ECC_AGG_TOP_SEC_ENABLE_SET_REG0 Registers

4.13.12.1 ECC_AGG_TOP_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-1553. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0080h

Access Types Legend

Table 4-1554. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for tptc_a1_pend
5	TPTC_A0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for tptc_a0_pend
4	MSS_MBOX_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_mbox_pend
3	MSS_L2SLV3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv3_pend
2	MSS_L2SLV2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv2_pend
1	MSS_L2SLV1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv1_pend
0	MSS_L2SLV0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv0_pend

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4.13.13 MSS_ECC_AGG_TOP_SEC_ENABLE_CLR_REG0 Registers

4.13.13.1 ECC_AGG_TOP_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-1555. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 00C0h

Access Types Legend

Table 4-1556. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for tptc_a1_pend
5	TPTC_A0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for tptc_a0_pend
4	MSS_MBOX_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_mbox_pend
3	MSS_L2SLV3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv3_pend
2	MSS_L2SLV2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv2_pend
1	MSS_L2SLV1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv1_pend
0	MSS_L2SLV0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv0_pend

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4.13.14 MSS_ECC_AGG_TOP_DED_EOI_REG Registers

4.13.14.1 ECC_AGG_TOP_DED_EOI_REG Register (Offset = 13Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-1557. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 013Ch

Access Types Legend

Table 4-1558. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

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4.13.15 MSS_ECC_AGG_TOP_DED_STATUS_REG0 Registers

4.13.15.1 ECC_AGG_TOP_DED_STATUS_REG0 Register (Offset = 140h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-1559. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0140h

Access Types Legend

Table 4-1560. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_PEND	RW	0h	Interrupt Pending Status for tptc_a1_pend
5	TPTC_A0_PEND	RW	0h	Interrupt Pending Status for tptc_a0_pend
4	MSS_MBOX_PEND	RW	0h	Interrupt Pending Status for mss_mbox_pend
3	MSS_L2SLV3_PEND	RW	0h	Interrupt Pending Status for mss_l2slv3_pend
2	MSS_L2SLV2_PEND	RW	0h	Interrupt Pending Status for mss_l2slv2_pend
1	MSS_L2SLV1_PEND	RW	0h	Interrupt Pending Status for mss_l2slv1_pend
0	MSS_L2SLV0_PEND	RW	0h	Interrupt Pending Status for mss_l2slv0_pend

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4.13.16 MSS_ECC_AGG_TOP_DED_ENABLE_SET_REG0 Registers

4.13.16.1 ECC_AGG_TOP_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-1561. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0180h

Access Types Legend

Table 4-1562. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for tptc_a1_pend
5	TPTC_A0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for tptc_a0_pend
4	MSS_MBOX_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_mbox_pend
3	MSS_L2SLV3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv3_pend
2	MSS_L2SLV2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv2_pend
1	MSS_L2SLV1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv1_pend
0	MSS_L2SLV0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for mss_l2slv0_pend

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4.13.17 MSS_ECC_AGG_TOP_DED_ENABLE_CLR_REG0 Registers

4.13.17.1 ECC_AGG_TOP_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-1563. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 01C0h

Access Types Legend

Table 4-1564. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
6	TPTC_A1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for tptc_a1_pend
5	TPTC_A0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for tptc_a0_pend
4	MSS_MBOX_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_mbox_pend
3	MSS_L2SLV3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv3_pend
2	MSS_L2SLV2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv2_pend
1	MSS_L2SLV1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv1_pend
0	MSS_L2SLV0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for mss_l2slv0_pend

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4.13.18 MSS_ECC_AGG_TOP_AGGR_ENABLE_SET Registers

4.13.18.1 ECC_AGG_TOP_AGGR_ENABLE_SET Register (Offset = 200h) [reset = h]

Short Description: AGGR interrupt enable set Register

Long Description:

Return to Summary Table

Table 4-1565. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0200h

Access Types Legend

Table 4-1566. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable set for svbus timeout errors
0	PARITY	RW	0h	interrupt enable set for parity errors

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4.13.19 MSS_ECC_AGG_TOP_AGGR_ENABLE_CLR Registers

4.13.19.1 ECC_AGG_TOP_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = h]

Short Description: AGGR interrupt enable clear Register

Long Description:

Return to Summary Table

Table 4-1567. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0204h

Access Types Legend

Table 4-1568. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable clear for svbus timeout errors
0	PARITY	RW	0h	interrupt enable clear for parity errors

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4.13.20 MSS_ECC_AGG_TOP_AGGR_STATUS_SET Registers

4.13.20.1 ECC_AGG_TOP_AGGR_STATUS_SET Register (Offset = 208h) [reset = h]

Short Description: AGGR interrupt status set Register

Long Description:

Return to Summary Table

Table 4-1569. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 0208h

Access Types Legend

Table 4-1570. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW INCR	0h	interrupt status set for svbus timeout errors
1 - 0	PARITY	RW INCR	0h	interrupt status set for parity errors

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4.13.21 MSS_ECC_AGG_TOP_AGGR_STATUS_CLR Registers

4.13.21.1 ECC_AGG_TOP_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = h]

Short Description: AGGR interrupt status clear Register

Long Description:

Return to Summary Table

Table 4-1571. Instance Table

Instance Name	Physical Address
ECC_AGG_TOP	5301 020Ch

Access Types Legend

Table 4-1572. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW DECR	0h	interrupt status clear for svbus timeout errors
1 - 0	PARITY	RW DECR	0h	interrupt status clear for parity errors

4.13.22 Access Table

Table 4-1573. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
RW DECR	RW DECR	Read / Write to Decrement
RW INCR	RW INCR	Read / Write to Increment

4.14 ECC_AGGA Registers

Table 4-1574. ECC_AGG_R5SS[0:1]_CORE0 Registers Base Address Table

Offset	Length	Acronym	ECC_AGG_R5SS0_CORE0 Physical Address	ECC_AGG_R5SS1_CORE0 Physical Address
0h	32	ECC_AGGA_REV	5300 0000h	5300 4000h
8h	24	ECC_AGGA_VECTOR	5300 0008h	5300 4008h
Ch	16	ECC_AGGA_STAT	5300 000Ch	5300 400Ch
10h	32	ECC_AGGA_WRAP_REV	5300 0010h	5300 4010h
14h	8	ECC_AGGA_CTRL	5300 0014h	5300 4014h
18h	32	ECC_AGGA_ERR_CTRL1	5300 0018h	5300 4018h
1Ch	32	ECC_AGGA_ERR_CTRL2	5300 001Ch	5300 401Ch
20h	32	ECC_AGGA_ERR_STAT1	5300 0020h	5300 4020h
24h	32	ECC_AGGA_ERR_STAT2	5300 0024h	5300 4024h
28h	16	ECC_AGGA_ERR_STAT3	5300 0028h	5300 4028h
3Ch	0	ECC_AGGA_SEC_EOI_REG	5300 003Ch	5300 403Ch
40h	32	ECC_AGGA_SEC_STATUS_REG0	5300 0040h	5300 4040h
80h	32	ECC_AGGA_SEC_ENABLE_SET_REG0	5300 0080h	5300 4080h
C0h	32	ECC_AGGA_SEC_ENABLE_CLR_REG0	5300 00C0h	5300 40C0h
13Ch	0	ECC_AGGA_DED_EOI_REG	5300 013Ch	5300 413Ch
140h	32	ECC_AGGA_DED_STATUS_REG0	5300 0140h	5300 4140h
180h	32	ECC_AGGA_DED_ENABLE_SET_REG0	5300 0180h	5300 4180h

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Table 4-1574. ECC_AGG_R5SS[0:1]_CORE0 Registers Base Address Table (continued)

Offset	Length	Acronym	ECC_AGG_R5SS0_CORE0 Physical Address	ECC_AGG_R5SS1_CORE0 Physical Address
1C0h	32	ECC_AGGA_DED_ENABLE_CLR_REG0	5300 01C0h	5300 41C0h
200h	8	ECC_AGGA_AGGR_ENABLE_SET	5300 0200h	5300 4200h
204h	8	ECC_AGGA_AGGR_ENABLE_CLR	5300 0204h	5300 4204h
208h	8	ECC_AGGA_AGGR_STATUS_SET	5300 0208h	5300 4208h
20Ch	8	ECC_AGGA_AGGR_STATUS_CLR	5300 020Ch	5300 420Ch

4.14.1 ECC_AGGA Instance Count Note

Note

n = 0 to 1 for the ECC_AGGA registers defined below.

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4.14.2 MSS_ECC_AGGA_REV Registers

4.14.2.1 ECC_AGGA_R5SSn_CORE0_REV Register (Offset = 0h) [reset = h]

Short Description: Revision parameters

Long Description:

Return to Summary Table

Table 4-1575. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0000h
ECC_AGG_R5SS1_CORE0	5300 4000h

Access Types Legend

Table 4-1576. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	2h	bu
27 - 16	MODULE_ID	RO	6A0h	Module ID
15 - 11	REVRTL	RO	18h	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	0h	Minor version

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4.14.3 MSS_ECC_AGGA_VECTOR Registers

4.14.3.1 ECC_AGGA_R5SSn_CORE0_VECTOR Register (Offset = 8h) [reset = h]

Short Description: ECC Vector Register

Long Description:

Return to Summary Table

Table 4-1577. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0008h
ECC_AGG_R5SS1_CORE0	5300 4008h

Access Types Legend

Table 4-1578. VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
24	RD_SVBUS_DONE	RO	0h	Status to indicate if read on serial VBUS is complete
23 - 16	RD_SVBUS_ADDRESS	RW	0h	Read address
15	RD_SVBUS	RW	0h	Write 1 to trigger a read on the serial VBUS
	RESERVED	NONE		Reserved
10 - 0	ECC_VECTOR	RW	0h	Value written to select the corresponding ECC RAM for control or status

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4.14.4 MSS_ECC_AGGA_STAT Registers

4.14.4.1 ECC_AGGA_R5SSn_CORE0_STAT Register (Offset = Ch) [reset = h]

Short Description: Misc Status

Long Description:

Return to Summary Table

Table 4-1579. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 000Ch
ECC_AGG_R5SS1_CORE0	5300 400Ch

Access Types Legend

Table 4-1580. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 0	NUM_RAMS	RO	1Ch	Indicates the number of RAMS serviced by the ECC aggregator

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4.14.5 MSS_ECC_AGGA_WRAP_REV Registers

4.14.5.1 ECC_AGGA_R5SSn_CORE0_WRAP_REV Register (Offset = 10h) [reset = h]

Short Description: Revision parameters

Long Description:

Return to Summary Table

Table 4-1581. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0010h
ECC_AGG_R5SS1_CORE0	5300 4010h

Access Types Legend

Table 4-1582. WRAP_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	2h	bu
27 - 16	MODULE_ID	RO	6A4h	Module ID
15 - 11	REVRTL	RO	0h	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	Ah	Minor version

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4.14.6 MSS_ECC_AGGA_CTRL Registers

4.14.6.1 ECC_AGGA_R5SSn_CORE0_CTRL Register (Offset = 14h) [reset = h]

Short Description: ECC Control Register

Long Description:

Return to Summary Table

Table 4-1583. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0014h
ECC_AGG_R5SS1_CORE0	5300 4014h

Access Types Legend

Table 4-1584. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
8	CHECK_SVBUS_TIMEOUT	RW	1h	check for svbus timeout errors
7	CHECK_PARITY	RW	1h	check for parity errors
6	ERROR_ONCE	RW	0h	Force Error only once
5	FORCE_N_ROW	RW	0h	Force Error on any RAM read
4	FORCE_DED	RW	0h	Force Double Bit Error
3	FORCE_SEC	RW	0h	Force Single Bit Error
2	ENABLE_RMW	RW	1h	Enable rmw
1	ECC_CHECK	RW	1h	Enable ECC check
0	ECC_ENABLE	RW	1h	Enable ECC

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4.14.7 MSS_ECC_AGGA_ERR_CTRL1 Registers

4.14.7.1 ECC_AGGA_R5SSn_CORE0_ERR_CTRL1 Register (Offset = 18h) [reset = h]

Short Description: ECC Error Control1 Register

Long Description:

Return to Summary Table

Table 4-1585. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0018h
ECC_AGG_R5SS1_CORE0	5300 4018h

Access Types Legend

Table 4-1586. ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RW	0h	Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

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4.14.8 MSS_ECC_AGGA_ERR_CTRL2 Registers

4.14.8.1 ECC_AGGA_R5SSn_CORE0_ERR_CTRL2 Register (Offset = 1Ch) [reset = h]

Short Description: ECC Error Control2 Register

Long Description:

Return to Summary Table

Table 4-1587. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 001Ch
ECC_AGG_R5SS1_CORE0	5300 401Ch

Access Types Legend

Table 4-1588. ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT2	RW	0h	Data bit that needs to be flipped if double bit error needs to be forced
15 - 0	ECC_BIT1	RW	0h	Data bit that needs to be flipped when force_sec is set

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4.14.9 MSS_ECC_AGGA_ERR_STAT1 Registers

4.14.9.1 ECC_AGGA_R5SSn_CORE0_ERR_STAT1 Register (Offset = 20h) [reset = h]

Short Description: ECC Error Status1 Register

Long Description:

Return to Summary Table

Table 4-1589. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0020h
ECC_AGG_R5SS1_CORE0	5300 4020h

Access Types Legend

Table 4-1590. ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT1	RO	0h	Data bit that corresponds to the single-bit error
15	CLR_CTRL_REG_ERR	RW	0h	Clear control reg error Error Status, you must also re write the contorl ergister itself to clear this
14 - 13	CLR_PARITY_ERR	RW DECR	0h	Clear parity Error Status
12	CLR_ECC_OTHER	RW	0h	Clear other Error Status
11 - 10	CLR_ECC_DED	RW DECR	0h	Clear Double Bit Error Status
9 - 8	CLR_ECC_SEC	RW DECR	0h	Clear Single Bit Error Status
7	CTR_REG_ERR	RW	0h	control register error pending, Level interrupt
6 - 5	PARITY_ERR	RW	0h	Level parity error Error Status
4	ECC_OTHER	RW	0h	successive single-bit errors have occurred while a writeback is still pending, Level interrupt
3 - 2	ECC_DED	RW INCR	0h	Level Double Bit Error Status
1 - 0	ECC_SEC	RW INCR	0h	Level Single Bit Error Status

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4.14.10 MSS_ECC_AGGA_ERR_STAT2 Registers

4.14.10.1 ECC_AGGA_R5SSn_CORE0_ERR_STAT2 Register (Offset = 24h) [reset = h]

Short Description: ECC Error Status2 Register

Long Description:

Return to Summary Table

Table 4-1591. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0024h
ECC_AGG_R5SS1_CORE0	5300 4024h

Access Types Legend

Table 4-1592. ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RO	0h	Row address where the single or double-bit error has occurred

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4.14.11 MSS_ECC_AGGA_ERR_STAT3 Registers

4.14.11.1 ECC_AGGA_R5SSn_CORE0_ERR_STAT3 Register (Offset = 28h) [reset = h]

Short Description: ECC Error Status3 Register

Long Description:

Return to Summary Table

Table 4-1593. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0028h
ECC_AGG_R5SS1_CORE0	5300 4028h

Access Types Legend

Table 4-1594. ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	CLR_SVBUS_TIMEOUT_ERR	RW	0h	Clear svbus timeout Error Status
	RESERVED	NONE		Reserved
1	SVBUS_TIMEOUT_ERR	RW	0h	Level svbus timeout error Error Status
0	WB_PEND	RO	0h	delayed write back pending Status

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4.14.12 MSS_ECC_AGGA_SEC_EOI_REG Registers

4.14.12.1 ECC_AGGA_R5SSn_CORE0_SEC_EOI_REG Register (Offset = 3Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-1595. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 003Ch
ECC_AGG_R5SS1_CORE0	5300 403Ch

Access Types Legend

Table 4-1596. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

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4.14.13 MSS_ECC_AGGA_SEC_STATUS_REG0 Registers

4.14.13.1 ECC_AGGA_R5SSn_CORE0_SEC_STATUS_REG0 Register (Offset = 40h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-1597. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0040h
ECC_AGG_R5SS1_CORE0	5300 4040h

Access Types Legend

Table 4-1598. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_PEND	RW	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for b0tcm0_bank0_pend
22	ATCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	RW	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank3_pend

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Table 4-1598. SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CPU0_IDATA_BANK2_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

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4.14.14 MSS_ECC_AGGA_SEC_ENABLE_SET_REG0 Registers

4.14.14.1 ECC_AGGA_R5SSn_CORE0_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-1599. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0080h
ECC_AGG_R5SS1_CORE0	5300 4080h

Access Types Legend

Table 4-1600. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend

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Table 4-1600. SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CPU0_DTAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

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4.14.15 MSS_ECC_AGGA_SEC_ENABLE_CLR_REG0 Registers

4.14.15.1 ECC_AGGA_R5SSn_CORE0_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-1601. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 00C0h
ECC_AGG_R5SS1_CORE0	5300 40C0h

Access Types Legend

Table 4-1602. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend

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Table 4-1602. SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CPU0_DTAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

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4.14.16 MSS_ECC_AGGA_DED_EOI_REG Registers

4.14.16.1 ECC_AGGA_R5SSn_CORE0_DED_EOI_REG Register (Offset = 13Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-1603. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 013Ch
ECC_AGG_R5SS1_CORE0	5300 413Ch

Access Types Legend

Table 4-1604. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

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4.14.17 MSS_ECC_AGGA_DED_STATUS_REG0 Registers

4.14.17.1 ECC_AGGA_R5SSn_CORE0_DED_STATUS_REG0 Register (Offset = 140h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-1605. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0140h
ECC_AGG_R5SS1_CORE0	5300 4140h

Access Types Legend

Table 4-1606. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_PEND	RW	0h	Interrupt Pending Status for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for b1tcm0_bank1_pend
25	B1TCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for b1tcm0_bank0_pend
24	B0TCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for b0tcm0_bank1_pend
23	B0TCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for b0tcm0_bank0_pend
22	ATCM0_BANK1_PEND	RW	0h	Interrupt Pending Status for atcm0_bank1_pend
21	ATCM0_BANK0_PEND	RW	0h	Interrupt Pending Status for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_PEND	RW	0h	Interrupt Pending Status for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram1_pend
8	CPU0_DTAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank3_pend

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Table 4-1606. DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CPU0_IDATA_BANK2_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_PEND	RW	0h	Interrupt Pending Status for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu0_itag_ram0_pend

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4.14.18 MSS_ECC_AGGA_DED_ENABLE_SET_REG0 Registers

4.14.18.1 ECC_AGGA_R5SSn_CORE0_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-1607. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0180h
ECC_AGG_R5SS1_CORE0	5300 4180h

Access Types Legend

Table 4-1608. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram1_pend

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Table 4-1608. DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CPU0_DTAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu0_itag_ram0_pend

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4.14.19 MSS_ECC_AGGA_DED_ENABLE_CLR_REG0 Registers

4.14.19.1 ECC_AGGA_R5SSn_CORE0_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-1609. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 01C0h
ECC_AGG_R5SS1_CORE0	5300 41C0h

Access Types Legend

Table 4-1610. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU0_KS_VIM_RAMECC_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend
26	B1TCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm0_bank1_pend
25	B1TCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm0_bank0_pend
24	B0TCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm0_bank1_pend
23	B0TCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm0_bank0_pend
22	ATCM0_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm0_bank1_pend
21	ATCM0_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm0_bank0_pend
20	CPU0_DDATA_RAM7_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram7_pend
19	CPU0_DDATA_RAM6_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram6_pend
18	CPU0_DDATA_RAM5_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram5_pend
17	CPU0_DDATA_RAM4_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram4_pend
16	CPU0_DDATA_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram3_pend
15	CPU0_DDATA_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram2_pend
14	CPU0_DDATA_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram1_pend
13	CPU0_DDATA_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddata_ram0_pend
12	CPU0_DDIRTY_RAM_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_ddirty_ram_pend
11	CPU0_DTAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram3_pend
10	CPU0_DTAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram2_pend
9	CPU0_DTAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram1_pend

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Table 4-1610. DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CPU0_DTAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_dtag_ram0_pend
7	CPU0_IDATA_BANK3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank3_pend
6	CPU0_IDATA_BANK2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank2_pend
5	CPU0_IDATA_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank1_pend
4	CPU0_IDATA_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_idata_bank0_pend
3	CPU0_ITAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram3_pend
2	CPU0_ITAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram2_pend
1	CPU0_ITAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram1_pend
0	CPU0_ITAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu0_itag_ram0_pend

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4.14.20 MSS_ECC_AGGA_AGGR_ENABLE_SET Registers

4.14.20.1 ECC_AGGA_R5SSn_CORE0_AGGR_ENABLE_SET Register (Offset = 200h) [reset = h]

Short Description: AGGR interrupt enable set Register

Long Description:

Return to Summary Table

Table 4-1611. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0200h
ECC_AGG_R5SS1_CORE0	5300 4200h

Access Types Legend

Table 4-1612. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable set for svbus timeout errors
0	PARITY	RW	0h	interrupt enable set for parity errors

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4.14.21 MSS_ECC_AGGA_AGGR_ENABLE_CLR Registers

4.14.21.1 ECC_AGGA_R5SSn_CORE0_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = h]

Short Description: AGGR interrupt enable clear Register

Long Description:

Return to Summary Table

Table 4-1613. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0204h
ECC_AGG_R5SS1_CORE0	5300 4204h

Access Types Legend

Table 4-1614. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable clear for svbus timeout errors
0	PARITY	RW	0h	interrupt enable clear for parity errors

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4.14.22 MSS_ECC_AGGA_AGGR_STATUS_SET Registers

4.14.22.1 ECC_AGGA_R5SSn_CORE0_AGGR_STATUS_SET Register (Offset = 208h) [reset = h]

Short Description: AGGR interrupt status set Register

Long Description:

Return to Summary Table

Table 4-1615. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 0208h
ECC_AGG_R5SS1_CORE0	5300 4208h

Access Types Legend

Table 4-1616. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW INCR	0h	interrupt status set for svbus timeout errors
1 - 0	PARITY	RW INCR	0h	interrupt status set for parity errors

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4.14.23 MSS_ECC_AGGA_AGGR_STATUS_CLR Registers

4.14.23.1 ECC_AGGA_R5SSn_CORE0_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = h]

Short Description: AGGR interrupt status clear Register

Long Description:

Return to Summary Table

Table 4-1617. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE0	5300 020Ch
ECC_AGG_R5SS1_CORE0	5300 420Ch

Access Types Legend

Table 4-1618. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW DECR	0h	interrupt status clear for svbus timeout errors
1 - 0	PARITY	RW DECR	0h	interrupt status clear for parity errors

4.14.24 Access Table

Table 4-1619. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
RW DECR	RW DECR	Read / Write to Decrement
RW INCR	RW INCR	Read / Write to Increment

4.15 ECC_AGGB Registers

Table 4-1620. ECC_AGG_R5SS[0:1]_CORE1 Registers Base Address Table

Offset	Length	Acronym	ECC_AGG_R5SS0_CORE1 Physical Address	ECC_AGG_R5SS1_CORE1 Physical Address
0h	32	ECC_AGGB_REV	5300 3000h	5300 7000h
8h	24	ECC_AGGB_VECTOR	5300 3008h	5300 7008h
Ch	16	ECC_AGGB_STAT	5300 300Ch	5300 700Ch
10h	32	ECC_AGGB_WRAP_REV	5300 3010h	5300 7010h
14h	8	ECC_AGGB_CTRL	5300 3014h	5300 7014h
18h	32	ECC_AGGB_ERR_CTRL1	5300 3018h	5300 7018h
1Ch	32	ECC_AGGB_ERR_CTRL2	5300 301Ch	5300 701Ch
20h	32	ECC_AGGB_ERR_STAT1	5300 3020h	5300 7020h
24h	32	ECC_AGGB_ERR_STAT2	5300 3024h	5300 7024h
28h	16	ECC_AGGB_ERR_STAT3	5300 3028h	5300 7028h
3Ch	0	ECC_AGGB_SEC_EOI_REG	5300 303Ch	5300 703Ch
40h	32	ECC_AGGB_SEC_STATUS_REG0	5300 3040h	5300 7040h
80h	32	ECC_AGGB_SEC_ENABLE_SET_REG0	5300 3080h	5300 7080h
C0h	32	ECC_AGGB_SEC_ENABLE_CLR_REG0	5300 30C0h	5300 70C0h
13Ch	0	ECC_AGGB_DED_EOI_REG	5300 313Ch	5300 713Ch
140h	32	ECC_AGGB_DED_STATUS_REG0	5300 3140h	5300 7140h

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Table 4-1620. ECC_AGG_R5SS[0:1]_CORE1 Registers Base Address Table (continued)

Offset	Length	Acronym	ECC_AGG_R5SS0_CORE1 Physical Address	ECC_AGG_R5SS1_CORE1 Physical Address
180h	32	ECC_AGGB_DED_ENABLE_SET_REG0	5300 3180h	5300 7180h
1C0h	32	ECC_AGGB_DED_ENABLE_CLR_REG0	5300 31C0h	5300 71C0h
200h	8	ECC_AGGB_AGGR_ENABLE_SET	5300 3200h	5300 7200h
204h	8	ECC_AGGB_AGGR_ENABLE_CLR	5300 3204h	5300 7204h
208h	8	ECC_AGGB_AGGR_STATUS_SET	5300 3208h	5300 7208h
20Ch	8	ECC_AGGB_AGGR_STATUS_CLR	5300 320Ch	5300 720Ch

4.15.1 ECC_AGGB Instance Count Note

Note

n = 0 to 1 for the ECC_AGGB registers defined below.

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4.15.2 MSS_ECC_AGGB_REV Registers

4.15.2.1 ECC_AGGB_R5SSn_CORE1_REV Register (Offset = 0h) [reset = h]

Short Description: Revision parameters

Long Description:

Return to Summary Table

Table 4-1621. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3000h
ECC_AGG_R5SS1_CORE1	5300 7000h

Access Types Legend

Table 4-1622. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	2h	bu
27 - 16	MODULE_ID	RO	6A0h	Module ID
15 - 11	REVRTL	RO	18h	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	0h	Minor version

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4.15.3 MSS_ECC_AGGB_VECTOR Registers

4.15.3.1 ECC_AGGB_R5SSn_CORE1_VECTOR Register (Offset = 8h) [reset = h]

Short Description: ECC Vector Register

Long Description:

Return to Summary Table

Table 4-1623. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3008h
ECC_AGG_R5SS1_CORE1	5300 7008h

Access Types Legend

Table 4-1624. VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
24	RD_SVBUS_DONE	RO	0h	Status to indicate if read on serial VBUS is complete
23 - 16	RD_SVBUS_ADDRESS	RW	0h	Read address
15	RD_SVBUS	RW	0h	Write 1 to trigger a read on the serial VBUS
	RESERVED	NONE		Reserved
10 - 0	ECC_VECTOR	RW	0h	Value written to select the corresponding ECC RAM for control or status

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4.15.4 MSS_ECC_AGGB_STAT Registers

4.15.4.1 ECC_AGGB_R5SSn_CORE1_STAT Register (Offset = Ch) [reset = h]

Short Description: Misc Status

Long Description:

Return to Summary Table

Table 4-1625. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 300Ch
ECC_AGG_R5SS1_CORE1	5300 700Ch

Access Types Legend

Table 4-1626. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 0	NUM_RAMS	RO	1Ch	Indicates the number of RAMS serviced by the ECC aggregator

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4.15.5 MSS_ECC_AGGB_WRAP_REV Registers

4.15.5.1 ECC_AGGB_R5SSn_CORE1_WRAP_REV Register (Offset = 10h) [reset = h]

Short Description: Revision parameters

Long Description:

Return to Summary Table

Table 4-1627. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3010h
ECC_AGG_R5SS1_CORE1	5300 7010h

Access Types Legend

Table 4-1628. WRAP_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	2h	bu
27 - 16	MODULE_ID	RO	6A4h	Module ID
15 - 11	REVRTL	RO	0h	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	Ah	Minor version

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4.15.6 MSS_ECC_AGGB_CTRL Registers

4.15.6.1 ECC_AGGB_R5SSn_CORE1_CTRL Register (Offset = 14h) [reset = h]

Short Description: ECC Control Register

Long Description:

Return to Summary Table

Table 4-1629. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3014h
ECC_AGG_R5SS1_CORE1	5300 7014h

Access Types Legend

Table 4-1630. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
8	CHECK_SVBUS_TIMEOUT	RW	1h	check for svbus timeout errors
7	CHECK_PARITY	RW	1h	check for parity errors
6	ERROR_ONCE	RW	0h	Force Error only once
5	FORCE_N_ROW	RW	0h	Force Error on any RAM read
4	FORCE_DED	RW	0h	Force Double Bit Error
3	FORCE_SEC	RW	0h	Force Single Bit Error
2	ENABLE_RMW	RW	1h	Enable rmw
1	ECC_CHECK	RW	1h	Enable ECC check
0	ECC_ENABLE	RW	1h	Enable ECC

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4.15.7 MSS_ECC_AGGB_ERR_CTRL1 Registers

4.15.7.1 ECC_AGGB_R5SSn_CORE1_ERR_CTRL1 Register (Offset = 18h) [reset = h]

Short Description: ECC Error Control1 Register

Long Description:

Return to Summary Table

Table 4-1631. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3018h
ECC_AGG_R5SS1_CORE1	5300 7018h

Access Types Legend

Table 4-1632. ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RW	0h	Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

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4.15.8 MSS_ECC_AGGB_ERR_CTRL2 Registers

4.15.8.1 ECC_AGGB_R5SSn_CORE1_ERR_CTRL2 Register (Offset = 1Ch) [reset = h]

Short Description: ECC Error Control2 Register

Long Description:

Return to Summary Table

Table 4-1633. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 301Ch
ECC_AGG_R5SS1_CORE1	5300 701Ch

Access Types Legend

Table 4-1634. ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT2	RW	0h	Data bit that needs to be flipped if double bit error needs to be forced
15 - 0	ECC_BIT1	RW	0h	Data bit that needs to be flipped when force_sec is set

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4.15.9 MSS_ECC_AGGB_ERR_STAT1 Registers

4.15.9.1 ECC_AGGB_R5SSn_CORE1_ERR_STAT1 Register (Offset = 20h) [reset = h]

Short Description: ECC Error Status1 Register

Long Description:

Return to Summary Table

Table 4-1635. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3020h
ECC_AGG_R5SS1_CORE1	5300 7020h

Access Types Legend

Table 4-1636. ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT1	RO	0h	Data bit that corresponds to the single-bit error
15	CLR_CTRL_REG_ERR	RW	0h	Clear control reg error Error Status, you must also re write the contorl ergister itself to clear this
14 - 13	CLR_PARITY_ERR	RW DECR	0h	Clear parity Error Status
12	CLR_ECC_OTHER	RW	0h	Clear other Error Status
11 - 10	CLR_ECC_DED	RW DECR	0h	Clear Double Bit Error Status
9 - 8	CLR_ECC_SEC	RW DECR	0h	Clear Single Bit Error Status
7	CTR_REG_ERR	RW	0h	control register error pending, Level interrupt
6 - 5	PARITY_ERR	RW	0h	Level parity error Error Status
4	ECC_OTHER	RW	0h	successive single-bit errors have occurred while a writeback is still pending, Level interrupt
3 - 2	ECC_DED	RW INCR	0h	Level Double Bit Error Status
1 - 0	ECC_SEC	RW INCR	0h	Level Single Bit Error Status

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4.15.10 MSS_ECC_AGGB_ERR_STAT2 Registers

4.15.10.1 ECC_AGGB_R5SSn_CORE1_ERR_STAT2 Register (Offset = 24h) [reset = h]

Short Description: ECC Error Status2 Register

Long Description:

Return to Summary Table

Table 4-1637. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3024h
ECC_AGG_R5SS1_CORE1	5300 7024h

Access Types Legend

Table 4-1638. ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RO	0h	Row address where the single or double-bit error has occurred

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4.15.11 MSS_ECC_AGGB_ERR_STAT3 Registers

4.15.11.1 ECC_AGGB_R5SSn_CORE1_ERR_STAT3 Register (Offset = 28h) [reset = h]

Short Description: ECC Error Status3 Register

Long Description:

Return to Summary Table

Table 4-1639. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3028h
ECC_AGG_R5SS1_CORE1	5300 7028h

Access Types Legend

Table 4-1640. ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	CLR_SVBUS_TIMEOUT_ERR	RW	0h	Clear svbus timeout Error Status
	RESERVED	NONE		Reserved
1	SVBUS_TIMEOUT_ERR	RW	0h	Level svbus timeout error Error Status
0	WB_PEND	RO	0h	delayed write back pending Status

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4.15.12 MSS_ECC_AGGB_SEC_EOI_REG Registers

4.15.12.1 ECC_AGGB_R5SSn_CORE1_SEC_EOI_REG Register (Offset = 3Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-1641. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 303Ch
ECC_AGG_R5SS1_CORE1	5300 703Ch

Access Types Legend

Table 4-1642. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

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4.15.13 MSS_ECC_AGGB_SEC_STATUS_REG0 Registers

4.15.13.1 ECC_AGGB_R5SSn_CORE1_SEC_STATUS_REG0 Register (Offset = 40h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-1643. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3040h
ECC_AGG_R5SS1_CORE1	5300 7040h

Access Types Legend

Table 4-1644. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_PEND	RW	0h	Interrupt Pending Status for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for b1tcm1_bank1_pend
25	B1TCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for b1tcm1_bank0_pend
24	B0TCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for b0tcm1_bank1_pend
23	B0TCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for b0tcm1_bank0_pend
22	ATCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for atcm1_bank1_pend
21	ATCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_PEND	RW	0h	Interrupt Pending Status for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank3_pend

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Table 4-1644. SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CPU1_IDATA_BANK2_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram0_pend

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4.15.14 MSS_ECC_AGGB_SEC_ENABLE_SET_REG0 Registers

4.15.14.1 ECC_AGGB_R5SSn_CORE1_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-1645. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3080h
ECC_AGG_R5SS1_CORE1	5300 7080h

Access Types Legend

Table 4-1646. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm1_bank1_pend
25	B1TCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm1_bank0_pend
24	B0TCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm1_bank1_pend
23	B0TCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm1_bank0_pend
22	ATCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm1_bank1_pend
21	ATCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram1_pend

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Table 4-1646. SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CPU1_DTAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram0_pend

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4.15.15 MSS_ECC_AGGB_SEC_ENABLE_CLR_REG0 Registers

4.15.15.1 ECC_AGGB_R5SSn_CORE1_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-1647. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 30C0h
ECC_AGG_R5SS1_CORE1	5300 70C0h

Access Types Legend

Table 4-1648. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm1_bank1_pend
25	B1TCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm1_bank0_pend
24	B0TCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm1_bank1_pend
23	B0TCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm1_bank0_pend
22	ATCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm1_bank1_pend
21	ATCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram1_pend

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Table 4-1648. SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CPU1_DTAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram0_pend

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4.15.16 MSS_ECC_AGGB_DED_EOI_REG Registers

4.15.16.1 ECC_AGGB_R5SSn_CORE1_DED_EOI_REG Register (Offset = 13Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-1649. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 313Ch
ECC_AGG_R5SS1_CORE1	5300 713Ch

Access Types Legend

Table 4-1650. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
0	EOI_WR	RW	0h	EOI Register

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4.15.17 MSS_ECC_AGGB_DED_STATUS_REG0 Registers

4.15.17.1 ECC_AGGB_R5SSn_CORE1_DED_STATUS_REG0 Register (Offset = 140h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-1651. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3140h
ECC_AGG_R5SS1_CORE1	5300 7140h

Access Types Legend

Table 4-1652. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_PEND	RW	0h	Interrupt Pending Status for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for b1tcm1_bank1_pend
25	B1TCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for b1tcm1_bank0_pend
24	B0TCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for b0tcm1_bank1_pend
23	B0TCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for b0tcm1_bank0_pend
22	ATCM1_BANK1_PEND	RW	0h	Interrupt Pending Status for atcm1_bank1_pend
21	ATCM1_BANK0_PEND	RW	0h	Interrupt Pending Status for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_PEND	RW	0h	Interrupt Pending Status for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram1_pend
8	CPU1_DTAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank3_pend

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Table 4-1652. DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CPU1_IDATA_BANK2_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_PEND	RW	0h	Interrupt Pending Status for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_PEND	RW	0h	Interrupt Pending Status for cpu1_itag_ram0_pend

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4.15.18 MSS_ECC_AGGB_DED_ENABLE_SET_REG0 Registers

4.15.18.1 ECC_AGGB_R5SSn_CORE1_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-1653. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3180h
ECC_AGG_R5SS1_CORE1	5300 7180h

Access Types Legend

Table 4-1654. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm1_bank1_pend
25	B1TCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b1tcm1_bank0_pend
24	B0TCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm1_bank1_pend
23	B0TCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for b0tcm1_bank0_pend
22	ATCM1_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm1_bank1_pend
21	ATCM1_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram1_pend

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Table 4-1654. DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CPU1_DTAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_ENABLE_SET	RW	0h	Interrupt Enable Set Register for cpu1_itag_ram0_pend

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4.15.19 MSS_ECC_AGGB_DED_ENABLE_CLR_REG0 Registers

4.15.19.1 ECC_AGGB_R5SSn_CORE1_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-1655. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 31C0h
ECC_AGG_R5SS1_CORE1	5300 71C0h

Access Types Legend

Table 4-1656. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
27	CPU1_KS_VIM_RAMECC_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ks_vim_ramecc_pend
26	B1TCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm1_bank1_pend
25	B1TCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b1tcm1_bank0_pend
24	B0TCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm1_bank1_pend
23	B0TCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for b0tcm1_bank0_pend
22	ATCM1_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm1_bank1_pend
21	ATCM1_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for atcm1_bank0_pend
20	CPU1_DDATA_RAM7_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram7_pend
19	CPU1_DDATA_RAM6_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram6_pend
18	CPU1_DDATA_RAM5_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram5_pend
17	CPU1_DDATA_RAM4_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram4_pend
16	CPU1_DDATA_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram3_pend
15	CPU1_DDATA_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram2_pend
14	CPU1_DDATA_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram1_pend
13	CPU1_DDATA_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddata_ram0_pend
12	CPU1_DDIRTY_RAM_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_ddirty_ram_pend
11	CPU1_DTAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram3_pend
10	CPU1_DTAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram2_pend
9	CPU1_DTAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram1_pend

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Table 4-1656. DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CPU1_DTAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_dtag_ram0_pend
7	CPU1_IDATA_BANK3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank3_pend
6	CPU1_IDATA_BANK2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank2_pend
5	CPU1_IDATA_BANK1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank1_pend
4	CPU1_IDATA_BANK0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_idata_bank0_pend
3	CPU1_ITAG_RAM3_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram3_pend
2	CPU1_ITAG_RAM2_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram2_pend
1	CPU1_ITAG_RAM1_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram1_pend
0	CPU1_ITAG_RAM0_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for cpu1_itag_ram0_pend

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4.15.20 MSS_ECC_AGGB_AGGR_ENABLE_SET Registers

4.15.20.1 ECC_AGGB_R5SSn_CORE1_AGGR_ENABLE_SET Register (Offset = 200h) [reset = h]

Short Description: AGGR interrupt enable set Register

Long Description:

Return to Summary Table

Table 4-1657. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3200h
ECC_AGG_R5SS1_CORE1	5300 7200h

Access Types Legend

Table 4-1658. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable set for svbus timeout errors
0	PARITY	RW	0h	interrupt enable set for parity errors

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4.15.21 MSS_ECC_AGGB_AGGR_ENABLE_CLR Registers

4.15.21.1 ECC_AGGB_R5SSn_CORE1_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = h]

Short Description: AGGR interrupt enable clear Register

Long Description:

Return to Summary Table

Table 4-1659. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3204h
ECC_AGG_R5SS1_CORE1	5300 7204h

Access Types Legend

Table 4-1660. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TIMEOUT	RW	0h	interrupt enable clear for svbus timeout errors
0	PARITY	RW	0h	interrupt enable clear for parity errors

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4.15.22 MSS_ECC_AGGB_AGGR_STATUS_SET Registers

4.15.22.1 ECC_AGGB_R5SSn_CORE1_AGGR_STATUS_SET Register (Offset = 208h) [reset = h]

Short Description: AGGR interrupt status set Register

Long Description:

Return to Summary Table

Table 4-1661. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 3208h
ECC_AGG_R5SS1_CORE1	5300 7208h

Access Types Legend

Table 4-1662. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW INCR	0h	interrupt status set for svbus timeout errors
1 - 0	PARITY	RW INCR	0h	interrupt status set for parity errors

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4.15.23 MSS_ECC_AGGB_AGGR_STATUS_CLR Registers

4.15.23.1 ECC_AGGB_R5SSn_CORE1_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = h]

Short Description: AGGR interrupt status clear Register

Long Description:

Return to Summary Table

Table 4-1663. Instance Table

Instance Name	Physical Address
ECC_AGG_R5SS0_CORE1	5300 320Ch
ECC_AGG_R5SS1_CORE1	5300 720Ch

Access Types Legend

Table 4-1664. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 2	TIMEOUT	RW DECR	0h	interrupt status clear for svbus timeout errors
1 - 0	PARITY	RW DECR	0h	interrupt status clear for parity errors

4.15.24 Access Table

Table 4-1665. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
RW DECR	RW DECR	Read / Write to Decrement
RW INCR	RW INCR	Read / Write to Increment

4.16 MSS_GPIO Registers

Note

GPIOn_x is generic name used to describe a GPIO signal, where n represents the specific GPIO module ranging from 0 to 3 and x represents one of the input/output signals associated with the module.

For additional description information on the device GPIO, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Table 4-1666. GPIO[0:2] Registers, Base Address Table

Offset	Length	Acronym	GPIO0 Physical Address	GPIO1 Physical Address	GPIO2 Physical Address
0h	32	GPIOn_PID	5200 0000h	5200 1000h	5200 2000h
4h	8	GPIOn_PCR	5200 0004h	5200 1004h	5200 2004h
8h	32	GPI0n_BINTEN	5200 0008h	5200 1008h	5200 2008h
10h	32	GPIOn_DIR01	5200 0010h	5200 1010h	5200 2010h
14h	32	GPIOn_OUT_DATA01	5200 0014h	5200 1014h	5200 2014h
18h	32	GPIOn_SET_DATA01	5200 0018h	5200 1018h	5200 2018h
1Ch	32	GPI0n_CLR_DATA01	5200 001Ch	5200 101Ch	5200 201Ch
20h	32	GPIOn_IN_DATA01	5200 0020h	5200 1020h	5200 2020h
24h	32	GPIOn_SET_RIS_TRIG01	5200 0024h	5200 1024h	5200 2024h
28h	32	GPIOn_CLR_RIS_TRIG01	5200 0028h	5200 1028h	5200 2028h

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Table 4-1666. GPIO[0:2] Registers, Base Address Table (continued)

Offset	Length	Acronym	GPIO0 Physical Address	GPIO1 Physical Address	GPIO2 Physical Address
2Ch	32	GPIOn_SET_FAL_TRIG01	5200 002Ch	5200 102Ch	5200 202Ch
30h	32	GPIOn_CLR_FAL_TRIG01	5200 0030h	5200 1030h	5200 2030h
34h	32	GPIOn_INTSTAT01	5200 0034h	5200 1034h	5200 2034h
38h	32	GPIOn_DIR23	5200 0038h	5200 1038h	5200 2038h
3Ch	32	GPIOn_OUT_DATA23	5200 003Ch	5200 103Ch	5200 203Ch
40h	32	GPIOn_SET_DATA23	5200 0040h	5200 1040h	5200 2040h
44h	32	GPIOn_CLR_DATA23	5200 0044h	5200 1044h	5200 2044h
48h	32	GPIOn_IN_DATA23	5200 0048h	5200 1048h	5200 2048h
4Ch	32	GPIOn_SET_RIS_TRIG23	5200 004Ch	5200 104Ch	5200 204Ch
50h	32	GPIOn_CLR_RIS_TRIG23	5200 0050h	5200 1050h	5200 2050h
54h	32	GPIOn_SET_FAL_TRIG23	5200 0054h	5200 1054h	5200 2054h
58h	32	GPIOn_CLR_FAL_TRIG23	5200 0058h	5200 1058h	5200 2058h
5Ch	32	GPIOn_INTSTAT23	5200 005Ch	5200 105Ch	5200 205Ch
60h	32	GPIOn_DIR45	5200 0060h	5200 1060h	5200 2060h
64h	32	GPIOn_OUT_DATA45	5200 0064h	5200 1064h	5200 2064h
68h	32	GPIOn_SET_DATA45	5200 0068h	5200 1068h	5200 2068h
6Ch	32	GPIOn_CLR_DATA45	5200 006Ch	5200 106Ch	5200 206Ch
70h	32	GPIOn_IN_DATA45	5200 0070h	5200 1070h	5200 2070h
74h	32	GPIOn_SET_RIS_TRIG45	5200 0074h	5200 1074h	5200 2074h
78h	32	GPIOn_CLR_RIS_TRIG45	5200 0078h	5200 1078h	5200 2078h
7Ch	32	GPIOn_SET_FAL_TRIG45	5200 007Ch	5200 107Ch	5200 207Ch
80h	32	GPIOn_CLR_FAL_TRIG45	5200 0080h	5200 1080h	5200 2080h
84h	32	GPIOn_INTSTAT45	5200 0084h	5200 1084h	5200 2084h
88h	32	GPIOn_DIR67	5200 0088h	5200 1088h	5200 2088h
8Ch	32	GPIOn_OUT_DATA67	5200 008Ch	5200 108Ch	5200 208Ch
90h	32	GPIOn_SET_DATA67	5200 0090h	5200 1090h	5200 2090h
94h	32	GPIOn_CLR_DATA67	5200 0094h	5200 1094h	5200 2094h
98h	32	GPIOn_IN_DATA67	5200 0098h	5200 1098h	5200 2098h
9Ch	32	GPIOn_SET_RIS_TRIG67	5200 009Ch	5200 109Ch	5200 209Ch
A0h	32	GPIOn_CLR_RIS_TRIG67	5200 00A0h	5200 10A0h	5200 20A0h
A4h	32	GPIOn_SET_FAL_TRIG67	5200 00A4h	5200 10A4h	5200 20A4h
A8h	32	GPIOn_CLR_FAL_TRIG67	5200 00A8h	5200 10A8h	5200 20A8h
ACh	32	GPIOn_INTSTAT67	5200 00ACh	5200 10ACh	5200 20ACh
B0h	32	GPIOn_DIR8	5200 00B0h	5200 10B0h	5200 20B0h
B4h	32	GPIOn_OUT_DATA8	5200 00B4h	5200 10B4h	5200 20B4h
B8h	32	GPIOn_SET_DATA8	5200 00B8h	5200 10B8h	5200 20B8h
BCh	32	GPIOn_CLR_DATA8	5200 00BCh	5200 10BCh	5200 20BCh
C0h	32	GPIOn_IN_DATA8	5200 00C0h	5200 10C0h	5200 20C0h
C4h	16	GPIOn_SET_RIS_TRIG8	5200 00C4h	5200 10C4h	5200 20C4h
C8h	16	GPIOn_CLR_RIS_TRIG8	5200 00C8h	5200 10C8h	5200 20C8h
CCh	16	GPIOn_SET_FAL_TRIG8	5200 00CCh	5200 10CCh	5200 20CCh
D0h	16	GPIOn_CLR_FAL_TRIG8	5200 00D0h	5200 10D0h	5200 20D0h
D4h	32	GPIOn_INTSTAT8	5200 00D4h	5200 10D4h	5200 20D4h

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Table 4-1667. GPIO[3] Registers Base Address Table

Offset	Length	Acronym	GPIO3 Physical Address
0h	32	GPIOn_PID	5200 3000h
4h	8	GPIOn_PCR	5200 3004h
8h	32	GPIOn_BINTEN	5200 3008h
10h	32	GPIOn_DIR01	5200 3010h
14h	32	GPIOn_OUT_DATA01	5200 3014h
18h	32	GPIOn_SET_DATA01	5200 3018h
1Ch	32	GPIOn_CLR_DATA01	5200 301Ch
20h	32	GPIOn_IN_DATA01	5200 3020h
24h	32	GPIOn_SET_RIS_TRIG01	5200 3024h
28h	32	GPIOn_CLR_RIS_TRIG01	5200 3028h
2Ch	32	GPIOn_SET_FAL_TRIG01	5200 302Ch
30h	32	GPIOn_CLR_FAL_TRIG01	5200 3030h
34h	32	GPIOn_INTSTAT01	5200 3034h
38h	32	GPIOn_DIR23	5200 3038h
3Ch	32	GPIOn_OUT_DATA23	5200 303Ch
40h	32	GPIOn_SET_DATA23	5200 3040h
44h	32	GPIOn_CLR_DATA23	5200 3044h
48h	32	GPIOn_IN_DATA23	5200 3048h
4Ch	32	GPIOn_SET_RIS_TRIG23	5200 304Ch
50h	32	GPIOn_CLR_RIS_TRIG23	5200 3050h
54h	32	GPIOn_SET_FAL_TRIG23	5200 3054h
58h	32	GPIOn_CLR_FAL_TRIG23	5200 3058h
5Ch	32	GPIOn_INTSTAT23	5200 305Ch
60h	32	GPIOn_DIR45	5200 3060h
64h	32	GPIOn_OUT_DATA45	5200 3064h
68h	32	GPIOn_SET_DATA45	5200 3068h
6Ch	32	GPIOn_CLR_DATA45	5200 306Ch
70h	32	GPIOn_IN_DATA45	5200 3070h
74h	32	GPIOn_SET_RIS_TRIG45	5200 3074h
78h	32	GPIOn_CLR_RIS_TRIG45	5200 3078h
7Ch	32	GPIOn_SET_FAL_TRIG45	5200 307Ch
80h	32	GPIOn_CLR_FAL_TRIG45	5200 3080h
84h	32	GPIOn_INTSTAT45	5200 3084h
88h	32	GPIOn_DIR67	5200 3088h
8Ch	32	GPIOn_OUT_DATA67	5200 308Ch
90h	32	GPIOn_SET_DATA67	5200 3090h
94h	32	GPIOn_CLR_DATA67	5200 3094h
98h	32	GPIOn_IN_DATA67	5200 3098h
9Ch	32	GPIOn_SET_RIS_TRIG67	5200 309Ch
A0h	32	GPIOn_CLR_RIS_TRIG67	5200 30A0h
A4h	32	GPIOn_SET_FAL_TRIG67	5200 30A4h
A8h	32	GPIOn_CLR_FAL_TRIG67	5200 30A8h
ACh	32	GPIOn_INTSTAT67	5200 30ACh
B0h	32	GPIOn_DIR8	5200 30B0h
B4h	32	GPIOn_OUT_DATA8	5200 30B4h
B8h	32	GPIOn_SET_DATA8	5200 30B8h
BCh	32	GPIOn_CLR_DATA8	5200 30BCh

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Table 4-1667. GPIO[3] Registers Base Address Table (continued)

Offset	Length	Acronym	GPIO3 Physical Address
C0h	32	GPIOn_IN_DATA8	5200 30C0h
C4h	16	GPIOn_SET_RIS_TRIG8	5200 30C4h
C8h	16	GPIOn_CLR_RIS_TRIG8	5200 30C8h
CCh	16	GPIOn_SET_FAL_TRIG8	5200 30CCh
D0h	16	GPIOn_CLR_FAL_TRIG8	5200 30D0h
D4h	32	GPIOn_INTSTAT8	5200 30D4h

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4.16.1 GPIOn_PID Register (Offset = 0h) [reset = h]

Short Description: GPIO Peripheral ID Register

Long Description:

Return to Summary Table

Table 4-1668. Instance Table

Instance Name	Physical Address
GPIO0	5200 0000h
GPIO1	5200 1000h
GPIO2	5200 2000h
GPIO3	5200 3000h

Figure 4-626. GPIOn_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RESERVED		FUNC											
RO		RO		RO											
1		0		10010000011											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL				MAJOR				CUSTOM		MINOR					
RO				RO				RO		RO					
101				1				0		101					

Access Types Legend

Table 4-1669. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Current scheme
29 - 28	RESERVED	RO		RESERVED
27 - 16	FUNC	RO	483h	Function code assigned to TCP3
15 - 11	RTL	RO	5h	RTL Version R code
10 - 8	MAJOR	RO	1h	Major revision X code
7 - 6	CUSTOM	RO	0h	Custom version code
5 - 0	MINOR	RO	5h	Minor revision Y code

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4.16.2 GPIOn_PCR Register (Offset = 4h) [reset = h]

Short Description: Peripheral Control Register

Long Description:

Return to Summary Table

Table 4-1670. Instance Table

Instance Name	Physical Address
GPIO0	5200 0004h
GPIO1	5200 1004h
GPIO2	5200 2004h
GPIO3	5200 3004h

Figure 4-627. GPIOn_PCR Name Register

15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
NONE						RO	RO
0						0	1

Access Types Legend

Table 4-1671. PCR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	SOFT	RO	0h	Used in conjunction with FREE bit to determine the emulation suspend mode.
0	FREE	RO	1h	For GPIO, the FREE bit is fixed at 1, which means GPIO runs free in emulation suspend.

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4.16.3 GPIOn_BINTEN Register (Offset = 8h) [reset = h]

Short Description: Bit Interrupt Enable Register

Long Description:

Return to Summary Table

Table 4-1672. Instance Table

Instance Name	Physical Address
GPIO0	5200 0008h
GPIO1	5200 1008h
GPIO2	5200 2008h
GPIO3	5200 3008h

Figure 4-628. GPIOn_BINTEN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN															
RW															
0															

Access Types Legend

Table 4-1673. BINTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO		RESERVED
15 - 0	EN	RW	0h	Per bank interrupt enable. 0 = disable, 1 = enable.

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4.16.4 GPIOn_DIR01 Register (Offset = 10h) [reset = h]

Short Description: Direction Register

Long Description:

Return to Summary Table

Table 4-1674. Instance Table

Instance Name	Physical Address
GPIO0	5200 0010h
GPIO1	5200 1010h
GPIO2	5200 2010h
GPIO3	5200 3010h

Figure 4-629. GPIOn_DIR01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIR1															
RW															
1111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR0															
RW															
1111111111111111															

Access Types Legend

Table 4-1675. DIR01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DIR1	RW	FFFFh	Direction of GPIO bank 1 bits, 0 = output, 1 = input.
15 - 0	DIR0	RW	FFFFh	Direction of GPIO bank 0 bits, 0 = output, 1 = input.

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4.16.5 GPIOn_OUT_DATA01 Register (Offset = 14h) [reset = h]

Short Description: Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1676. Instance Table

Instance Name	Physical Address
GPIO0	5200 0014h
GPIO1	5200 1014h
GPIO2	5200 2014h
GPIO3	5200 3014h

Figure 4-630. GPIOn_OUT_DATA01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUT1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT0															
RW															
0															

Access Types Legend

Table 4-1677. OUT_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	OUT1	RW	0h	Output drive state of GPIO bank 1 bits, does not affect operation when it is configured as input. Reading it returns the output drive state.
15 - 0	OUT0	RW	0h	Output drive state of GPIO bank 0 bits, does not affect operation when it is configured as input. Reading it returns the output drive state.

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4.16.6 GPIOn_SET_DATA01 Register (Offset = 18h) [reset = h]

Short Description: Set Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1678. Instance Table

Instance Name	Physical Address
GPIO0	5200 0018h
GPIO1	5200 1018h
GPIO2	5200 2018h
GPIO3	5200 3018h

Figure 4-631. GPIOn_SET_DATA01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SET1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET0															
RW															
0															

Access Types Legend

Table 4-1679. SET_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SET1	RW	0h	Writing 1 sets the output drive state of GPIO bank 1 bits. Reading returns the output drive state.
15 - 0	SET0	RW	0h	Writing 1 sets the output drive state of GPIO bank 0 bits. Reading returns the output drive state.

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4.16.7 GPIOn_CLR_DATA01 Register (Offset = 1Ch) [reset = h]

Short Description: Clear Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1680. Instance Table

Instance Name	Physical Address
GPIO0	5200 001Ch
GPIO1	5200 101Ch
GPIO2	5200 201Ch
GPIO3	5200 301Ch

Figure 4-632. GPIOn_CLR_DATA01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLR1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR0															
RW															
0															

Access Types Legend

Table 4-1681. CLR_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLR1	RW	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.
15 - 0	CLR0	RW	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.

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4.16.8 GPIOn_IN_DATA01 Register (Offset = 20h) [reset = h]

Short Description: Bank Status Register

Long Description:

Return to Summary Table

Table 4-1682. Instance Table

Instance Name	Physical Address
GPIO0	5200 0020h
GPIO1	5200 1020h
GPIO2	5200 2020h
GPIO3	5200 3020h

Figure 4-633. GPIOn_IN_DATA01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IN1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN0															
RO															
0															

Access Types Legend

Table 4-1683. IN_DATA01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	IN1	RO	0h	Status of GPIO bank 1 bits.
15 - 0	IN0	RO	0h	Status of GPIO bank 0 bits.

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4.16.9 GPIOn_SET_RIS_TRIG01 Register (Offset = 24h) [reset = h]

Short Description: Set Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1684. Instance Table

Instance Name	Physical Address
GPIO0	5200 0024h
GPIO1	5200 1024h
GPIO2	5200 2024h
GPIO3	5200 3024h

Figure 4-634. GPIOn_SET_RIS_TRIG01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETRIS1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETRIS0															
RW															
0															

Access Types Legend

Table 4-1685. SET_RIS_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SETRIS1	RW	0h	Writing 1 enables rising edge detection for GPIO bank 1 bits.
15 - 0	SETRIS0	RW	0h	Writing 1 enables rising edge detection for GPIO bank 0 bits.

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4.16.10 GPIOn_CLR_RIS_TRIG01 Register (Offset = 28h) [reset = h]

Short Description: Clear Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1686. Instance Table

Instance Name	Physical Address
GPIO0	5200 0028h
GPIO1	5200 1028h
GPIO2	5200 2028h
GPIO3	5200 3028h

Figure 4-635. GPIOn_CLR_RIS_TRIG01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRRIS1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRRIS0															
RW															
0															

Access Types Legend

Table 4-1687. CLR_RIS_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLRRIS1	RW	0h	Writing 1 clears rising edge detection for GPIO bank 1 bits.
15 - 0	CLRRIS0	RW	0h	Writing 1 clears rising edge detection for GPIO bank 0 bits.

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4.16.11 GPIOn_SET_FAL_TRIG01 Register (Offset = 2Ch) [reset = h]

Short Description: Set Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1688. Instance Table

Instance Name	Physical Address
GPIO0	5200 002Ch
GPIO1	5200 102Ch
GPIO2	5200 202Ch
GPIO3	5200 302Ch

Figure 4-636. GPIOn_SET_FAL_TRIG01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETFAL1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETFAL0															
RW															
0															

Access Types Legend

Table 4-1689. SET_FAL_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SETFAL1	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 1 bits.
15 - 0	SETFAL0	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 0 bits.

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4.16.12 GPIOn_CLR_FAL_TRIG01 Register (Offset = 30h) [reset = h]

Short Description: Clear Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1690. Instance Table

Instance Name	Physical Address
GPIO0	5200 0030h
GPIO1	5200 1030h
GPIO2	5200 2030h
GPIO3	5200 3030h

Figure 4-637. GPIOn_CLR_FAL_TRIG01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRFAL1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRFAL0															
RW															
0															

Access Types Legend

Table 4-1691. CLR_FAL_TRIG01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLRFAL1	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 1 bits.
15 - 0	CLRFAL0	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 0 bits.

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4.16.13 GPIOn_INTSTAT01 Register (Offset = 34h) [reset = h]

Short Description: Bank Interrupt Status Register

Long Description:

Return to Summary Table

Table 4-1692. Instance Table

Instance Name	Physical Address
GPIO0	5200 0034h
GPIO1	5200 1034h
GPIO2	5200 2034h
GPIO3	5200 3034h

Figure 4-638. GPIOn_INTSTAT01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STAT1															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT0															
RW															
0															

Access Types Legend

Table 4-1693. INTSTAT01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	STAT1	RW	0h	Status of GPIO bank 0 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.
15 - 0	STAT0	RW	0h	Status of GPIO bank 0 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.

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4.16.14 GPIOn_DIR23 Register (Offset = 38h) [reset = h]

Short Description: Direction Register

Long Description:

Return to Summary Table

Table 4-1694. Instance Table

Instance Name	Physical Address
GPIO0	5200 0038h
GPIO1	5200 1038h
GPIO2	5200 2038h
GPIO3	5200 3038h

Figure 4-639. GPIOn_DIR23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIR3															
RW															
1111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR2															
RW															
1111111111111111															

Access Types Legend

Table 4-1695. DIR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DIR3	RW	FFFFh	Direction of GPIO bank 3 bits, 0 = output, 1 = input.
15 - 0	DIR2	RW	FFFFh	Direction of GPIO bank 2 bits, 0 = output, 1 = input.

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4.16.15 GPIOn_OUT_DATA23 Register (Offset = 3Ch) [reset = h]

Short Description: Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1696. Instance Table

Instance Name	Physical Address
GPIO0	5200 003Ch
GPIO1	5200 103Ch
GPIO2	5200 203Ch
GPIO3	5200 303Ch

Figure 4-640. GPIOn_OUT_DATA23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUT3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT2															
RW															
0															

Access Types Legend

Table 4-1697. OUT_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	OUT3	RW	0h	Output drive state of GPIO bank 3 bits, does not affect operation when configured as input. Reading it returns the output drive state.
15 - 0	OUT2	RW	0h	Output drive state of GPIO bank 2 bits, does not affect operation when configured as input. Reading it returns the output drive state.

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4.16.16 GPIOn_SET_DATA23 Register (Offset = 40h) [reset = h]

Short Description: Set Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1698. Instance Table

Instance Name	Physical Address
GPIO0	5200 0040h
GPIO1	5200 1040h
GPIO2	5200 2040h
GPIO3	5200 3040h

Figure 4-641. GPIOn_SET_DATA23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SET3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET2															
RW															
0															

Access Types Legend

Table 4-1699. SET_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SET3	RW	0h	Writing 1 sets the output drive state of GPIO bank 3 bits. Reading it returns the output drive state.
15 - 0	SET2	RW	0h	Writing 1 sets the output drive state of GPIO bank 2 bits. Reading it returns the output drive state.

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4.16.17 GPIOn_CLR_DATA23 Register (Offset = 44h) [reset = h]

Short Description: Clear Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1700. Instance Table

Instance Name	Physical Address
GPIO0	5200 0044h
GPIO1	5200 1044h
GPIO2	5200 2044h
GPIO3	5200 3044h

Figure 4-642. GPIOn_CLR_DATA23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLR3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR2															
RW															
0															

Access Types Legend

Table 4-1701. CLR_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLR3	RW	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.
15 - 0	CLR2	RW	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.

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4.16.18 GPIOn_IN_DATA23 Register (Offset = 48h) [reset = h]

Short Description: Bank Status Register

Long Description:

Return to Summary Table

Table 4-1702. Instance Table

Instance Name	Physical Address
GPIO0	5200 0048h
GPIO1	5200 1048h
GPIO2	5200 2048h
GPIO3	5200 3048h

Figure 4-643. GPIOn_IN_DATA23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IN3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN2															
RO															
0															

Access Types Legend

Table 4-1703. IN_DATA23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	IN3	RO	0h	Status of GPIO bank 3 bits.
15 - 0	IN2	RO	0h	Status of GPIO bank 2 bits.

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4.16.19 GPIOn_SET_RIS_TRIG23 Register (Offset = 4Ch) [reset = h]

Short Description: Set Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1704. Instance Table

Instance Name	Physical Address
GPIO0	5200 004Ch
GPIO1	5200 104Ch
GPIO2	5200 204Ch
GPIO3	5200 304Ch

Figure 4-644. GPIOn_SET_RIS_TRIG23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETRIS3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETRIS2															
RW															
0															

Access Types Legend

Table 4-1705. SET_RIS_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SETRIS3	RW	0h	Writing 1 enables rising edge detection for GPIO bank 3 bits.
15 - 0	SETRIS2	RW	0h	Writing 1 enables rising edge detection for GPIO bank 2 bits.

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4.16.20 GPIOn_CLR_RIS_TRIG23 Register (Offset = 50h) [reset = h]

Short Description: Clear Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1706. Instance Table

Instance Name	Physical Address
GPIO0	5200 0050h
GPIO1	5200 1050h
GPIO2	5200 2050h
GPIO3	5200 3050h

Figure 4-645. GPIOn_CLR_RIS_TRIG23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRRIS3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRRIS2															
RW															
0															

Access Types Legend

Table 4-1707. CLR_RIS_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLRRIS3	RW	0h	Writing 1 clears rising edge detection for GPIO bank 3 bits.
15 - 0	CLRRIS2	RW	0h	Writing 1 clears rising edge detection for GPIO bank 2 bits.

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4.16.21 GPIOn_SET_FAL_TRIG23 Register (Offset = 54h) [reset = h]

Short Description: Set Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1708. Instance Table

Instance Name	Physical Address
GPIO0	5200 0054h
GPIO1	5200 1054h
GPIO2	5200 2054h
GPIO3	5200 3054h

Figure 4-646. GPIOn_SET_FAL_TRIG23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETFAL3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETFAL2															
RW															
0															

Access Types Legend

Table 4-1709. SET_FAL_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SETFAL3	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 3 bits.
15 - 0	SETFAL2	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 2 bits.

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4.16.22 GPIOn_CLR_FAL_TRIG23 Register (Offset = 58h) [reset = h]

Short Description: Clear Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1710. Instance Table

Instance Name	Physical Address
GPIO0	5200 0058h
GPIO1	5200 1058h
GPIO2	5200 2058h
GPIO3	5200 3058h

Figure 4-647. GPIOn_CLR_FAL_TRIG23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRFAL3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRFAL2															
RW															
0															

Access Types Legend

Table 4-1711. CLR_FAL_TRIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLRFAL3	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 3 bits.
15 - 0	CLRFAL2	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 2 bits.

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4.16.23 GPIOn_INTSTAT23 Register (Offset = 5Ch) [reset = h]

Short Description: Bank Interrupt Status Register

Long Description:

Return to Summary Table

Table 4-1712. Instance Table

Instance Name	Physical Address
GPIO0	5200 005Ch
GPIO1	5200 105Ch
GPIO2	5200 205Ch
GPIO3	5200 305Ch

Figure 4-648. GPIOn_INTSTAT23 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STAT3															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT2															
RW															
0															

Access Types Legend

Table 4-1713. INTSTAT23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	STAT3	RW	0h	Status of GPIO bank 2 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.
15 - 0	STAT2	RW	0h	Status of GPIO bank 2 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.

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4.16.24 GPIOn_DIR45 Register (Offset = 60h) [reset = h]

Short Description: Direction Register

Long Description:

Return to Summary Table

Table 4-1714. Instance Table

Instance Name	Physical Address
GPIO0	5200 0060h
GPIO1	5200 1060h
GPIO2	5200 2060h
GPIO3	5200 3060h

Figure 4-649. GPIOn_DIR45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIR5															
RW															
1111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR4															
RW															
1111111111111111															

Access Types Legend

Table 4-1715. DIR45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DIR5	RW	FFFFh	Direction of GPIO bank 5 bits, 0 = output, 1 = input.
15 - 0	DIR4	RW	FFFFh	Direction of GPIO bank 4 bits, 0 = output, 1 = input.

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4.16.25 GPIOn_OUT_DATA45 Register (Offset = 64h) [reset = h]

Short Description: Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1716. Instance Table

Instance Name	Physical Address
GPIO0	5200 0064h
GPIO1	5200 1064h
GPIO2	5200 2064h
GPIO3	5200 3064h

Figure 4-650. GPIOn_OUT_DATA45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUT5															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT4															
RW															
0															

Access Types Legend

Table 4-1717. OUT_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	OUT5	RW	0h	Output drive state of GPIO bank 5 bits, does not affect operation when it is configured as input. Reading it returns the output drive state.
15 - 0	OUT4	RW	0h	Output drive state of GPIO bank 4 bits, does not affect operation when it is configured as input. Reading it returns the output drive state.

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4.16.26 GPIOn_SET_DATA45 Register (Offset = 68h) [reset = h]

Short Description: Set Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1718. Instance Table

Instance Name	Physical Address
GPIO0	5200 0068h
GPIO1	5200 1068h
GPIO2	5200 2068h
GPIO3	5200 3068h

Figure 4-651. GPIOn_SET_DATA45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SET5															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET4															
RW															
0															

Access Types Legend

Table 4-1719. SET_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SET5	RW	0h	Writing 1 sets the output drive state of GPIO bank 5 bits. Reading returns the output drive state.
15 - 0	SET4	RW	0h	Writing 1 sets the output drive state of GPIO bank 4 bits. Reading returns the output drive state.

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4.16.27 GPIOn_CLR_DATA45 Register (Offset = 6Ch) [reset = h]

Short Description: Clear Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1720. Instance Table

Instance Name	Physical Address
GPIO0	5200 006Ch
GPIO1	5200 106Ch
GPIO2	5200 206Ch
GPIO3	5200 306Ch

Figure 4-652. GPIOn_CLR_DATA45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLR5															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR4															
RW															
0															

Access Types Legend

Table 4-1721. CLR_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLR5	RW	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.
15 - 0	CLR4	RW	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.

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4.16.28 GPIOn_IN_DATA45 Register (Offset = 70h) [reset = h]

Short Description: Bank Status Register

Long Description:

Return to Summary Table

Table 4-1722. Instance Table

Instance Name	Physical Address
GPIO0	5200 0070h
GPIO1	5200 1070h
GPIO2	5200 2070h
GPIO3	5200 3070h

Figure 4-653. GPIOn_IN_DATA45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IN5															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN4															
RO															
0															

Access Types Legend

Table 4-1723. IN_DATA45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	IN5	RO	0h	Status of GPIO bank 5 bits.
15 - 0	IN4	RO	0h	Status of GPIO bank 4 bits.

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4.16.29 GPIOn_SET_RIS_TRIG45 Register (Offset = 74h) [reset = h]

Short Description: Set Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1724. Instance Table

Instance Name	Physical Address
GPIO0	5200 0074h
GPIO1	5200 1074h
GPIO2	5200 2074h
GPIO3	5200 3074h

Figure 4-654. GPIOn_SET_RIS_TRIG45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETRIS5															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETRIS4															
RW															
0															

Access Types Legend

Table 4-1725. SET_RIS_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SETRIS5	RW	0h	Writing 1 enables rising edge detection for GPIO bank 5 bits.
15 - 0	SETRIS4	RW	0h	Writing 1 enables rising edge detection for GPIO bank 4 bits.

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4.16.30 GPIOn_CLR_RIS_TRIG45 Register (Offset = 78h) [reset = h]

Short Description: Clear Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1726. Instance Table

Instance Name	Physical Address
GPIO0	5200 0078h
GPIO1	5200 1078h
GPIO2	5200 2078h
GPIO3	5200 3078h

Figure 4-655. GPIOn_CLR_RIS_TRIG45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRRIS5															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRRIS4															
RW															
0															

Access Types Legend

Table 4-1727. CLR_RIS_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLRRIS5	RW	0h	Writing 1 clears rising edge detection for GPIO bank 5 bits.
15 - 0	CLRRIS4	RW	0h	Writing 1 clears rising edge detection for GPIO bank 4 bits.

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4.16.31 GPIOn_SET_FAL_TRIG45 Register (Offset = 7Ch) [reset = h]

Short Description: Set Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1728. Instance Table

Instance Name	Physical Address
GPIO0	5200 007Ch
GPIO1	5200 107Ch
GPIO2	5200 207Ch
GPIO3	5200 307Ch

Figure 4-656. GPIOn_SET_FAL_TRIG45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETFAL5															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETFAL4															
RW															
0															

Access Types Legend

Table 4-1729. SET_FAL_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SETFAL5	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 5 bits.
15 - 0	SETFAL4	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 4 bits.

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4.16.32 GPIOn_CLR_FAL_TRIG45 Register (Offset = 80h) [reset = h]

Short Description: Clear Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1730. Instance Table

Instance Name	Physical Address
GPIO0	5200 0080h
GPIO1	5200 1080h
GPIO2	5200 2080h
GPIO3	5200 3080h

Figure 4-657. GPIOn_CLR_FAL_TRIG45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRFAL5															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRFAL4															
RW															
0															

Access Types Legend

Table 4-1731. CLR_FAL_TRIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLRFAL5	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 5 bits.
15 - 0	CLRFAL4	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 4 bits.

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4.16.33 GPIOn_INTSTAT45 Register (Offset = 84h) [reset = h]

Short Description: Bank Interrupt Status Register

Long Description:

Return to Summary Table

Table 4-1732. Instance Table

Instance Name	Physical Address
GPIO0	5200 0084h
GPIO1	5200 1084h
GPIO2	5200 2084h
GPIO3	5200 3084h

Figure 4-658. GPIOn_INTSTAT45 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STAT5															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT4															
RW															
0															

Access Types Legend

Table 4-1733. INTSTAT45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	STAT5	RW	0h	Status of GPIO bank 4 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.
15 - 0	STAT4	RW	0h	Status of GPIO bank 4 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.

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4.16.34 GPIOn_DIR67 Register (Offset = 88h) [reset = h]

Short Description: Direction Register

Long Description:

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Table 4-1734. Instance Table

Instance Name	Physical Address
GPIO0	5200 0088h
GPIO1	5200 1088h
GPIO2	5200 2088h
GPIO3	5200 3088h

Figure 4-659. GPIOn_DIR67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIR7															
RW															
1111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR6															
RW															
1111111111111111															

Access Types Legend

Table 4-1735. DIR67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DIR7	RW	FFFFh	Direction of GPIO bank 7 bits, 0 = output, 1 = input.
15 - 0	DIR6	RW	FFFFh	Direction of GPIO bank 6 bits, 0 = output, 1 = input.

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4.16.35 GPIOn_OUT_DATA67 Register (Offset = 8Ch) [reset = h]

Short Description: Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1736. Instance Table

Instance Name	Physical Address
GPIO0	5200 008Ch
GPIO1	5200 108Ch
GPIO2	5200 208Ch
GPIO3	5200 308Ch

Figure 4-660. GPIOn_OUT_DATA67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUT7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT6															
RW															
0															

Access Types Legend

Table 4-1737. OUT_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	OUT7	RW	0h	Output drive state of GPIO bank 7 bits, does not affect operation when it is configured as input. Reading it returns the output drive state.
15 - 0	OUT6	RW	0h	Output drive state of GPIO bank 6 bits, does not affect operation when it is configured as input. Reading it returns the output drive state.

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4.16.36 GPIOn_SET_DATA67 Register (Offset = 90h) [reset = h]

Short Description: Set Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1738. Instance Table

Instance Name	Physical Address
GPIO0	5200 0090h
GPIO1	5200 1090h
GPIO2	5200 2090h
GPIO3	5200 3090h

Figure 4-661. GPIOn_SET_DATA67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SET7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET6															
RW															
0															

Access Types Legend

Table 4-1739. SET_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SET7	RW	0h	Writing 1 sets the output drive state of GPIO bank 7 bits. Reading returns the output drive state.
15 - 0	SET6	RW	0h	Writing 1 sets the output drive state of GPIO bank 6 bits. Reading returns the output drive state.

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4.16.37 GPIOn_CLR_DATA67 Register (Offset = 94h) [reset = h]

Short Description: Clear Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1740. Instance Table

Instance Name	Physical Address
GPIO0	5200 0094h
GPIO1	5200 1094h
GPIO2	5200 2094h
GPIO3	5200 3094h

Figure 4-662. GPIOn_CLR_DATA67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLR7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR6															
RW															
0															

Access Types Legend

Table 4-1741. CLR_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLR7	RW	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.
15 - 0	CLR6	RW	0h	Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state.

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4.16.38 GPIOn_IN_DATA67 Register (Offset = 98h) [reset = h]

Short Description: Bank Status Register

Long Description:

Return to Summary Table

Table 4-1742. Instance Table

Instance Name	Physical Address
GPIO0	5200 0098h
GPIO1	5200 1098h
GPIO2	5200 2098h
GPIO3	5200 3098h

Figure 4-663. GPIOn_IN_DATA67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IN7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN6															
RO															
0															

Access Types Legend

Table 4-1743. IN_DATA67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	IN7	RO	0h	Status of GPIO bank 7 bits.
15 - 0	IN6	RO	0h	Status of GPIO bank 6 bits.

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4.16.39 GPIOn_SET_RIS_TRIG67 Register (Offset = 9Ch) [reset = h]

Short Description: Set Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1744. Instance Table

Instance Name	Physical Address
GPIO0	5200 009Ch
GPIO1	5200 109Ch
GPIO2	5200 209Ch
GPIO3	5200 309Ch

Figure 4-664. GPIOn_SET_RIS_TRIG67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETRIS7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETRIS6															
RW															
0															

Access Types Legend

Table 4-1745. SET_RIS_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SETRIS7	RW	0h	Writing 1 enables rising edge detection for GPIO bank 7 bits.
15 - 0	SETRIS6	RW	0h	Writing 1 enables rising edge detection for GPIO bank 6 bits.

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4.16.40 GPIOn_CLR_RIS_TRIG67 Register (Offset = A0h) [reset = h]

Short Description: Clear Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1746. Instance Table

Instance Name	Physical Address
GPIO0	5200 00A0h
GPIO1	5200 10A0h
GPIO2	5200 20A0h
GPIO3	5200 30A0h

Figure 4-665. GPIOn_CLR_RIS_TRIG67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRRIS7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRRIS6															
RW															
0															

Access Types Legend

Table 4-1747. CLR_RIS_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLRRIS7	RW	0h	Writing 1 clears rising edge detection for GPIO bank 7 bits.
15 - 0	CLRRIS6	RW	0h	Writing 1 clears rising edge detection for GPIO bank 6 bits.

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4.16.41 GPIOn_SET_FAL_TRIG67 Register (Offset = A4h) [reset = h]

Short Description: Set Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1748. Instance Table

Instance Name	Physical Address
GPIO0	5200 00A4h
GPIO1	5200 10A4h
GPIO2	5200 20A4h
GPIO3	5200 30A4h

Figure 4-666. GPIOn_SET_FAL_TRIG67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETFAL7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETFAL6															
RW															
0															

Access Types Legend

Table 4-1749. SET_FAL_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	SETFAL7	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 7 bits.
15 - 0	SETFAL6	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 6 bits.

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4.16.42 GPIOn_CLR_FAL_TRIG67 Register (Offset = A8h) [reset = h]

Short Description: Clear Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1750. Instance Table

Instance Name	Physical Address
GPIO0	5200 00A8h
GPIO1	5200 10A8h
GPIO2	5200 20A8h
GPIO3	5200 30A8h

Figure 4-667. GPIOn_CLR_FAL_TRIG67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRFAL7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRFAL6															
RW															
0															

Access Types Legend

Table 4-1751. CLR_FAL_TRIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	CLRFAL7	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 7 bits.
15 - 0	CLRFAL6	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 6 bits.

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4.16.43 GPIOn_INTSTAT67 Register (Offset = ACh) [reset = h]

Short Description: Bank Interrupt Status Register

Long Description:

Return to Summary Table

Table 4-1752. Instance Table

Instance Name	Physical Address
GPIO0	5200 00ACh
GPIO1	5200 10ACh
GPIO2	5200 20ACh
GPIO3	5200 30ACh

Figure 4-668. GPIOn_INTSTAT67 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
STAT7															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT6															
RW															
0															

Access Types Legend

Table 4-1753. INTSTAT67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	STAT7	RW	0h	Status of GPIO bank 6 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.
15 - 0	STAT6	RW	0h	Status of GPIO bank 6 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.

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4.16.44 GPIOn_DIR8 Register (Offset = B0h) [reset = h]

Short Description: Direction Register

Long Description:

Return to Summary Table

Table 4-1754. Instance Table

Instance Name	Physical Address
GPIO0	5200 00B0h
GPIO1	5200 10B0h
GPIO2	5200 20B0h
GPIO3	5200 30B0h

Figure 4-669. GPIOn_DIR8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
1111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIR8															
RW															
1111111111111111															

Access Types Legend

Table 4-1755. DIR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO	FFFFh	RESERVED
15 - 0	DIR8	RW	FFFFh	Direction of GPIO bank 8 bits, 0 = output, 1 = input.

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4.16.45 GPIOn_OUT_DATA8 Register (Offset = B4h) [reset = h]

Short Description: Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1756. Instance Table

Instance Name	Physical Address
GPIO0	5200 00B4h
GPIO1	5200 10B4h
GPIO2	5200 20B4h
GPIO3	5200 30B4h

Figure 4-670. GPIOn_OUT_DATA8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT8															
RW															
0															

Access Types Legend

Table 4-1757. OUT_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO		RESERVED
15 - 0	OUT8	RW	0h	Output drive state of GPIO bank 8 bits, does not affect operation when it is configured as input. Reading it returns the output drive state.

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4.16.46 GPIOn_SET_DATA8 Register (Offset = B8h) [reset = h]

Short Description: Set Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1758. Instance Table

Instance Name	Physical Address
GPIO0	5200 00B8h
GPIO1	5200 10B8h
GPIO2	5200 20B8h
GPIO3	5200 30B8h

Figure 4-671. GPIOn_SET_DATA8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SET8															
RW															
0															

Access Types Legend

Table 4-1759. SET_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO		RESERVED
15 - 0	SET8	RW	0h	Writing 1 sets the output drive state of GPIO bank 8 bits. Reading returns the output drive state.

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4.16.47 GPIOn_CLR_DATA8 Register (Offset = BCh) [reset = h]

Short Description: Clear Output Drive State Register

Long Description:

Return to Summary Table

Table 4-1760. Instance Table

Instance Name	Physical Address
GPIO0	5200 00BCh
GPIO1	5200 10BCh
GPIO2	5200 20BCh
GPIO3	5200 30BCh

Figure 4-672. GPIOn_CLR_DATA8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR8															
RW															
0															

Access Types Legend

Table 4-1761. CLR_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO		RESERVED
15 - 0	CLR8	RW	0h	Writing 1 clears the output drive state of GPIO. Reading returns the output drive state.

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4.16.48 GPIOn_IN_DATA8 Register (Offset = C0h) [reset = h]

Short Description: Bank Status Register

Long Description:

Return to Summary Table

Table 4-1762. Instance Table

Instance Name	Physical Address
GPIO0	5200 00C0h
GPIO1	5200 10C0h
GPIO2	5200 20C0h
GPIO3	5200 30C0h

Figure 4-673. GPIOn_IN_DATA8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN8															
RO															
0															

Access Types Legend

Table 4-1763. IN_DATA8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO		RESERVED
15 - 0	IN8	RO	0h	Status of GPIO bank 8 bits.

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4.16.49 GPIOn_SET_RIS_TRIG8 Register (Offset = C4h) [reset = h]

Short Description: Set Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1764. Instance Table

Instance Name	Physical Address
GPIO0	5200 00C4h
GPIO1	5200 10C4h
GPIO2	5200 20C4h
GPIO3	5200 30C4h

Figure 4-674. GPIOn_SET_RIS_TRIG8 Name Register

15	14	13	12	11	10	9	8
SETRIS8							
RW							
0							
7	6	5	4	3	2	1	0
SETRIS8							
RW							
0							

Access Types Legend

Table 4-1765. SET_RIS_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SETRIS8	RW	0h	Writing 1 enables rising edge detection for GPIO bank 8 bits.

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4.16.50 GPIOn_CLR_RIS_TRIG8 Register (Offset = C8h) [reset = h]

Short Description: Clear Rising Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1766. Instance Table

Instance Name	Physical Address
GPIO0	5200 00C8h
GPIO1	5200 10C8h
GPIO2	5200 20C8h
GPIO3	5200 30C8h

Figure 4-675. GPIOn_CLR_RIS_TRIG8 Name Register

15	14	13	12	11	10	9	8
CLRRIS8							
RW							
0							
7	6	5	4	3	2	1	0
CLRRIS8							
RW							
0							

Access Types Legend

Table 4-1767. CLR_RIS_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	CLRRIS8	RW	0h	Writing 1 clears rising edge detection for GPIO bank 8 bits.

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4.16.51 GPIOn_SET_FAL_TRIG8 Register (Offset = CCh) [reset = h]

Short Description: Set Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1768. Instance Table

Instance Name	Physical Address
GPIO0	5200 00CCh
GPIO1	5200 10CCh
GPIO2	5200 20CCh
GPIO3	5200 30CCh

Figure 4-676. GPIOn_SET_FAL_TRIG8 Name Register

15	14	13	12	11	10	9	8
SETFAL8							
RW							
0							
7	6	5	4	3	2	1	0
SETFAL8							
RW							
0							

Access Types Legend

Table 4-1769. SET_FAL_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	SETFAL8	RW	0h	Writing 1 enables falling edge detection for for GPIO bank 8 bits.

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4.16.52 GPIOn_CLR_FAL_TRIG8 Register (Offset = D0h) [reset = h]

Short Description: Clear Falling Edge Detection Register

Long Description:

Return to Summary Table

Table 4-1770. Instance Table

Instance Name	Physical Address
GPIO0	5200 00D0h
GPIO1	5200 10D0h
GPIO2	5200 20D0h
GPIO3	5200 30D0h

Figure 4-677. GPIOn_CLR_FAL_TRIG8 Name Register

15	14	13	12	11	10	9	8
CLRFAL8							
RW							
0							
7	6	5	4	3	2	1	0
CLRFAL8							
RW							
0							

Access Types Legend

Table 4-1771. CLR_FAL_TRIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	CLRFAL8	RW	0h	Writing 1 clears falling edge detection for for GPIO bank 8 bits.

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4.16.53 GPIOn_INTSTAT8 Register (Offset = D4h) [reset = h]

Short Description: Bank Interrupt Status Register

Long Description:

Return to Summary Table

Table 4-1772. Instance Table

Instance Name	Physical Address
GPIO0	5200 00D4h
GPIO1	5200 10D4h
GPIO2	5200 20D4h
GPIO3	5200 30D4h

Figure 4-678. GPIOn_INTSTAT8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STAT8															
RW															
0															

Access Types Legend

Table 4-1773. INTSTAT8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	RO		RESERVED
15 - 0	STAT8	RW	0h	Status of GPIO bank 8 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status.

4.17 I2C Registers

Table 4-1774. MSS_I2C[0:2] Registers Base Address Table

Offset	Length	Acronym	MSS_I2C0 Physical Address	MSS_I2C1 Physical Address	MSS_I2C2 Physical Address
0h	32	I2C_ICOAR	5250 0000h	5250 1000h	5250 2000h
4h	32	I2C_ICIMR	5250 0004h	5250 1004h	5250 2004h
8h	32	I2C_ICSTR	5250 0008h	5250 1008h	5250 2008h
Ch	32	I2C_ICCLKL	5250 000Ch	5250 100Ch	5250 200Ch
10h	32	I2C_ICCLKH	5250 0010h	5250 1010h	5250 2010h
14h	32	I2C_ICCNT	5250 0014h	5250 1014h	5250 2014h
18h	32	I2C_ICDRR	5250 0018h	5250 1018h	5250 2018h
1Ch	32	I2C_ICSAR	5250 001Ch	5250 101Ch	5250 201Ch
20h	32	I2C_ICDXR	5250 0020h	5250 1020h	5250 2020h
24h	32	I2C_ICMDR	5250 0024h	5250 1024h	5250 2024h
28h	32	I2C_ICIVR	5250 0028h	5250 1028h	5250 2028h
2Ch	32	I2C_ICEMDR	5250 002Ch	5250 102Ch	5250 202Ch
30h	32	I2C_ICPSC	5250 0030h	5250 1030h	5250 2030h
34h	32	I2C_ICPID1	5250 0034h	5250 1034h	5250 2034h
38h	32	I2C_ICPID2	5250 0038h	5250 1038h	5250 2038h

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Table 4-1774. MSS_I2C[0:2] Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_I2C0 Physical Address	MSS_I2C1 Physical Address	MSS_I2C2 Physical Address
3Ch	32	I2C_ICDMAC	5250 003Ch	5250 103Ch	5250 203Ch
40h	32	I2C_I2C_RESERVED1	5250 0040h	5250 1040h	5250 2040h
44h	32	I2C_I2C_RESERVED2	5250 0044h	5250 1044h	5250 2044h
48h	32	I2C_ICPFUNC	5250 0048h	5250 1048h	5250 2048h
4Ch	32	I2C_ICPDIR	5250 004Ch	5250 104Ch	5250 204Ch
50h	32	I2C_ICPDIN	5250 0050h	5250 1050h	5250 2050h
54h	32	I2C_ICPDOUT	5250 0054h	5250 1054h	5250 2054h
58h	32	I2C_ICPDSET	5250 0058h	5250 1058h	5250 2058h
5Ch	32	I2C_ICPDCLR	5250 005Ch	5250 105Ch	5250 205Ch
60h	32	I2C_ICPDRV	5250 0060h	5250 1060h	5250 2060h

Table 4-1775. MSS_I2C3 Registers Base Address Table

Offset	Length	Acronym	MSS_I2C3 Physical Address
0h	32	I2C_ICOAR	5250 3000h
4h	32	I2C_ICIMR	5250 3004h
8h	32	I2C_ICSTR	5250 3008h
Ch	32	I2C_ICCLKL	5250 300Ch
10h	32	I2C_ICCLKH	5250 3010h
14h	32	I2C_ICCNT	5250 3014h
18h	32	I2C_ICDRR	5250 3018h
1Ch	32	I2C_ICSAR	5250 301Ch
20h	32	I2C_ICDXR	5250 3020h
24h	32	I2C_ICMDR	5250 3024h
28h	32	I2C_ICIVR	5250 3028h
2Ch	32	I2C_ICEMDR	5250 302Ch
30h	32	I2C_ICPSC	5250 3030h
34h	32	I2C_ICPID1	5250 3034h
38h	32	I2C_ICPID2	5250 3038h
3Ch	32	I2C_ICDMAC	5250 303Ch
40h	32	I2C_I2C_RESERVED1	5250 3040h
44h	32	I2C_I2C_RESERVED2	5250 3044h
48h	32	I2C_ICPFUNC	5250 3048h
4Ch	32	I2C_ICPDIR	5250 304Ch
50h	32	I2C_ICPDIN	5250 3050h
54h	32	I2C_ICPDOUT	5250 3054h
58h	32	I2C_ICPDSET	5250 3058h
5Ch	32	I2C_ICPDCLR	5250 305Ch
60h	32	I2C_ICPDRV	5250 3060h

4.17.1 I2C Instance Count Note

Note

n = 0 to 3 for the I2C registers defined below.

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4.17.2 MSS_I2Cn_ICOAR Registers

4.17.2.1 I2Cn_ICOAR Register (Offset = 0h) [reset = h]

Short Description: I2C Own Address register

Long Description:

Return to Summary Table

Table 4-1776. Instance Table

Instance Name	Physical Address
I2C0	5250 0000h
I2C1	5250 1000h
I2C2	5250 2000h
I2C3	5250 3000h

Access Types Legend

Table 4-1777. ICOAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 10	NU	RW	0h	Reserved
9 - 0	A9_A0	RW	0h	Own address. Use in both 7- and 10-bit address mode. Note that usercan program the I2C own address to any value as long as it does notconflict with other components in the system.

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4.17.3 MSS_I2Cn_ICIMR Registers

4.17.3.1 I2Cn_ICIMR Register (Offset = 4h) [reset = h]

Short Description: I2C Interrupt Mask/Status register

Long Description:

Return to Summary Table

Table 4-1778. Instance Table

Instance Name	Physical Address
I2C0	5250 0004h
I2C1	5250 1004h
I2C2	5250 2004h
I2C3	5250 3004h

Access Types Legend

Table 4-1779. ICIMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	NU	RW	0h	Reserved
6	AAS	RW	0h	Address As Slave interrupt mask bit. Setting a"1" to this bit unmasks the Address As Slave interrupt. Setting a"0" to this bit masks the Address As Slave interrupt.
5	SCD	RW	0h	Stop Condition Detection mask bit. Setting a"1" to this bit unmasks the Stop Condition Detection interrupt. Setting a "0" to this bit masks the Stop Condition Detection interrupt.
4	ICXRDY	RW	0h	Transmit Data Ready interrupt mask bit. Setting a"1" to this bit unmasks the Transmit Data Ready interrupt. Setting a"0" to this bit masks the Transmit Data Ready interrupt.
3	ICRRDY	RW	0h	Receive Data Ready interrupt mask bit. Setting a"1" to this bit unmasks the Receive Data Ready interrupt. Setting a"0" to this bit masks the Receive Data Ready interrupt.
2	ARDY	RW	0h	Register access ready interrupt mask bit. Setting a"1" to this bit unmasks the Register access ready interrupt. Setting a"0" to this bit masks the Register access ready interrupt.
1	NACK	RW	0h	No Acknowledgement interrupt mask bit. Setting a"1" to this bit unmasks the No Acknowledgement interrupt. Setting a"0" to this bit masks the No Acknowledgement interrupt.
0	AL	RW	0h	Arbitration Lost interrupt mask bit. Setting a"1" to this bit unmasks the Arbitration Lost interrupt. Setting a"0" to this bit masks the Arbitration Lost interrupt.

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4.17.4 MSS_I2Cn_ICSTR Registers

4.17.4.1 I2Cn_ICSTR Register (Offset = 8h) [reset = h]

Short Description: I2C Interrupt Status register

Long Description:

Return to Summary Table

Table 4-1780. Instance Table

Instance Name	Physical Address
I2C0	5250 0008h
I2C1	5250 1008h
I2C2	5250 2008h
I2C3	5250 3008h

Access Types Legend

Table 4-1781. ICSTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 15	NU2	RW	0h	Reserved
14	SDIR	RW	0h	Slave Direction. This bit is clear to '0' indicating the I2C is a master transmitter/receiver or a slave receiver. This bit is also clear by STOP condition or START condition. It is set to '1' when the I2C slave is a transmitter. In DLB mode (which the configuration should be master-transmitter slave-receiver) this bit is clear to '0'. Writing a"1" to this bit to clear it.
13	NACKSNT	RW	0h	A No Acknowledge is sent due to NACKMOD is set to a"1". NACKSNT =0: A No Acknowledge is not sent. NACKSNT =1: A No Acknowledge is sent. Writing a"1" to this bit to clear it.
12	BB	RW	0h	Bus Busy. This bit indicates the state of the serial bus. BB=0: The bus is free. BB=1: The bus is occupied. On reception of a"start" condition the device sets BB to 1. This bit is also set if the I2C detects SCL low state. BB is clear to 0 after reception of a"stop" condition. BB is kept to"0" regardless SCL state when the I2C is in reset (IRS_=0). If the IRS_ is set to"1" during transaction between other I2C devices the BB bit is set at the first falling edge of SCL or START condition. - (RW)
11	RSFULL	RW	0h	Receive shift full. This bit indicates whether the receiver has experienced overrun. Overrun occurs when the receive shift register (ICRSR) is full and ICDRR has not been read since the ICRSR-to-ICDRR transfer. The FSM is holding for ICDRR read access. RSFULL is clear when reading the ICDRR. RSFULL is set to"1" when the I2C has recognized an overrun. The contents of ICDRR are NOT lost in this case. In repeat mode since double buffer (ICRSR and ICDRR) behaves like a single buffer RSFULL is set to"1" every time the data is received. RSFULL is clear as a result of reading the ICDRR. - (RW)
10	XSMT	RW	0h	Transmit shift empty not. This bit indicates whether the transmitter has experienced underflow. Underflow occurs when the transmit shift register (ICXSR) is empty and ICDXR has not been loaded. The FSM is holding for ICDXR write access. XSMT_ is cleared when underflow has occurred. XSMT_ is set to"1" as a result of writing to ICDXR. In repeat mode if the I2C in master transmitter mode is holding transfer with XSMT_=0 (i.e. waiting for further action) and the STT or STP bit is set XSMT_ is set to"1" by hardware.
9	AAS	RW	0h	Address As Slave. This bit is set to 1 by the device when it has recognized its own slave address or an address of all (8) zeros. The AAS bit is reset by stop condition or detection of any address byte that does not match ICOAR. - (RW)

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Table 4-1781. ICSTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	AD0	RW	0h	Address Zero Status: This bit is set to 1 by device if it detects the address of all (8) zeros (i.e. general call). The AD0 bit is reset to 0 (default value) when a"start" or"stop" condition is detected. - (RW)
7 - 6	NU1	RW	0h	Reserved
5	SCD	RW	0h	Stop Condition Detection bit SCD is set when the I2C sends or receives STOP condition. This bit is cleared by reading ICIVR (as 110) or writing '1' to itself.
4	ICXRDY	RW	0h	Transmit Data Ready interrupt flag bit. ICXRDY is set to"1" is generated when the transmitted data has been copied from ICDXR to the transmit-shift register (ICXSR). ICRXDY is clear to"0" when the ICDXR is written. This bit can also be polled by the CPU to write a new transmitted data into the ICDXR. Write '1' to this bit will set it and DXR Write will clear it.
3	ICRRDY	RW	0h	Receive Data Ready interrupt flag bit. ICRRDY is set to"1" when the received data has been copied from ICRSR into the ICDRR. ICRRDY is cleared to"0" when the ICDRR is read. This bit can also be polled by the CPU to read the received data in the ICDRR. Write '1' or DRR Read will clear it.
2	ARDY	RW	0h	Register-access-ready interrupt flag bit. ARDY is generated by the hardware if the I2C is in the master mode when the previously programmed data and command has been performed and status bit has been updated. This flag is used by the CPU to let it knows that the I2C registers are ready to be accessed again. When RM=0 ARDY is set when the internal data count is passed 0 if STP register bit has not been set. When RM=1 ARDY is set at each byte end. If the I2C is in FDF mode(FDF=1) ARDY is set just after Start condition. This bit is automatically cleared by hardware when writing data to ICDXR in transmit mode reading data from ICDRR in receive mode or setting STT or STP bit. Write '1' will clear it.
1	NACK	RW	0h	No-Acknowledgement interrupt flag bit. The No Acknowledge flag bit is set when the hardware in "master" mode detects no acknowledge has been received. This bit is NOT set by no-acknowledgement after Start byte Write '1' or Read the ICIVR (as 010) will clear it.
0	AL	RW	0h	Arbitration-Lost interrupt flag bit. The Arbitration Lost flag bit is set to 1 when the device in the "master" mode senses it has lost an arbitration when two or more transmitters start a transmission almost simultaneously or when the I2C attempts to start a transfer while BB (bus busy) is 1. When this is set to 1 due to arbitration lost the MST/STT/STP bits are clear the I2C becomes a slave. Write '1' or Read the ICIVR (as 001) will clear it.

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4.17.5 MSS_I2Cn_ICCLKL Registers

4.17.5.1 I2Cn_ICCLKL Register (Offset = Ch) [reset = h]

Short Description: I2C Clock Divider Low register

Long Description:

Return to Summary Table

Table 4-1782. Instance Table

Instance Name	Physical Address
I2C0	5250 000Ch
I2C1	5250 100Ch
I2C2	5250 200Ch
I2C3	5250 300Ch

Access Types Legend

Table 4-1783. ICCLKL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU	RW	0h	Reserved
15 - 0	ICCL15_ICCL0	RW	0h	Low time I 2 C SCL Clock Division Factor. They are used to divide down the master clock to create the SCL low time transition frequency. This register must be configured while the I2C is still in reset (IRS_=0).

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4.17.6 MSS_I2Cn_ICCLKH Registers

4.17.6.1 I2Cn_ICCLKH Register (Offset = 10h) [reset = h]

Short Description: I2C Clock Divider High register

Long Description:

Return to Summary Table

Table 4-1784. Instance Table

Instance Name	Physical Address
I2C0	5250 0010h
I2C1	5250 1010h
I2C2	5250 2010h
I2C3	5250 3010h

Access Types Legend

Table 4-1785. ICCLKH Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU	RW	0h	Reserved
15 - 0	ICCH15_ICCLH0	RW	0h	High time I 2 C SCL Clock Division Factor. They are used to divide down the master clock to create the SCL high time transition frequency. This register must be configured while the I2C is still in reset (IRS_=0).

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4.17.7 MSS_I2Cn_ICCNT Registers

4.17.7.1 I2Cn_ICCNT Register (Offset = 14h) [reset = h]

Short Description: I2C Data Count register

Long Description:

Return to Summary Table

Table 4-1786. Instance Table

Instance Name	Physical Address
I2C0	5250 0014h
I2C1	5250 1014h
I2C2	5250 2014h
I2C3	5250 3014h

Access Types Legend

Table 4-1787. ICCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU	RW	0h	Reserved
15 - 0	ICDC15_ICDC0	RW	0h	Data count. This data count register is used to generate a Stop condition if a Stop condition is specified (STP=1). . ICCNT=1 data count is 1 :: :: ICCNT=0FFFFh data count is 65535 ICCNT=0data counter is 65536 Note that ICCNT is a don"t care when RM is set to 1.

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4.17.8 MSS_I2Cn_ICDRR Registers

4.17.8.1 I2Cn_ICDRR Register (Offset = 18h) [reset = h]

Short Description: I2C Data Receive register

Long Description:

Return to Summary Table

Table 4-1788. Instance Table

Instance Name	Physical Address
I2C0	5250 0018h
I2C1	5250 1018h
I2C2	5250 2018h
I2C3	5250 3018h

Access Types Legend

Table 4-1789. ICDRR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU	RW	0h	Reserved
7 - 0	D7_D0	RW	0h	Receive data

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4.17.9 MSS_I2Cn_ICSAR Registers

4.17.9.1 I2Cn_ICSAR Register (Offset = 1Ch) [reset = h]

Short Description: I2C Slave Address register

Long Description:

Return to Summary Table

Table 4-1790. Instance Table

Instance Name	Physical Address
I2C0	5250 001Ch
I2C1	5250 101Ch
I2C2	5250 201Ch
I2C3	5250 301Ch

Access Types Legend

Table 4-1791. ICSAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 10	NU	RW	0h	Reserved
9 - 0	A9_A0	RW	0h	Slave address. Use in both 7- and 10-bit address mode.

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4.17.10 MSS_I2Cn_ICDXR Registers

4.17.10.1 I2Cn_ICDXR Register (Offset = 20h) [reset = h]

Short Description: I2C Data Transmit register

Long Description:

Return to Summary Table

Table 4-1792. Instance Table

Instance Name	Physical Address
I2C0	5250 0020h
I2C1	5250 1020h
I2C2	5250 2020h
I2C3	5250 3020h

Access Types Legend

Table 4-1793. ICDXR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU	RW	0h	Reserved
7 - 0	D7_D0	RW	0h	Transmit data

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4.17.11 MSS_I2Cn_ICMDR Registers

4.17.11.1 I2Cn_ICMDR Register (Offset = 24h) [reset = h]

Short Description: I2C Mode register

Long Description:

Return to Summary Table

Table 4-1794. Instance Table

Instance Name	Physical Address
I2C0	5250 0024h
I2C1	5250 1024h
I2C2	5250 2024h
I2C3	5250 3024h

Access Types Legend

Table 4-1795. ICMDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU2	RW	0h	Reserved
15	NACKMOD	RW	0h	No Acknowledge (NACK) mode. This bit is used to send an Acknowledge (ACK) or a No Acknowledge (NACK) to the transmitter. This bit is only applicable when the I2C is in receiver mode. In master receiver mode when the internal data count counter decrements to zero the I2C sends a NACK. The master receiver I2C finishes a transfer when it sends a NACK. The I2C ignores ICCNT when NACKMOD is '1'. The NACKMOD bit should be set before the rising edge of the last data bit (bit 8) if a NACK must be sent and this bit is cleared once a NACK has been sent. NACKMOD=0 the I2C sends an ACK to the transmitter during the acknowledge cycle. NACKMOD=1 the I2C sends a NACK to the transmitter during the acknowledge cycle.
14	FREE	RW	0h	Free Running. This bit is used to determine the state of the I2C when a breakpoint is encountered in the HLL debugger. FREE=0: (default) Stops immediately if SCL is low and keep driving SCL low whether I2C is master transmitter/receiver. If SCL is high I2C waits until SCL becomes low and then stops. If the I2C is a slave it will stop when the transmission/receiving completes. FREE=1: The I2C runs free.
13	STT	RW	0h	Start Condition (Master only mode). This bit can be set to a"1" by the CPU to generate a Start condition. In master mode when setting Start to"1" generates a Start condition. It is reset to "0" by the hardware after the Start condition has been generated. The Start/ Stop bits can be configured to generate different transfer formats. Note that the STT and STP can be used to terminate the repeat mode. ST T___STP____Conditions_____Bus Activities _1_____0_____Start_____S-A-D _0_____1_____Stop_____P _1_____1_____Start-Stop (ICCNT= n)_____S-A-D..(n)..D-P _1_____0_____Start (ICCNT= n)_____S-A-D..(n)..D
12	NU1	RW	0h	Reserved for IDLEEN (IDLE Enable on 5509). - (RW)
11	STP	RW	0h	Stop Condition (Master mode only). This bit can be set to a"1" by the CPU to generate a Stop condition. It is reset to "0" by the hardware after the Stop condition has been generated. The Stop condition is generated when ICCNT passes 0 when the I2C is in non-repeat mode(RM=0).

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Table 4-1795. ICMDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	MST	RW	0h	Master. MST=0: The I 2 C peripheral is in the"slave" mode and clock is received from the"master" device. MST=1: The I 2 C peripheral is in the"master" mode and it generates the clock. This bit is clear when the transfer completed.
9	TRX	RW	0h	Transmitter. TRX=0: The I 2 C is in the"receiver" mode and data on data line SDA is shifted into the data register ICDRR. TRX=1: The I 2 C is in the"transmitter" mode and the data in ICDXR is shifted out on data line SDA. The operating modes (not in FDF mode) are defined as follows. In FDF mode TRX must be configured even if the I2C is in slave mode because there is no address/direction byte in FDF mode. _____MST___TRX___Operating Modes _0_____x_____"slave receiver" _0_____x_____"slave transmitter" _1_____0_____"master receiver" _1_____1_____"master transmitter" _____
8	XA	RW	0h	Expanded Address. XA=0: (default) 7-bit address mode (normal address mode). XA=1: 10-bit address mode (expanded address mode) Please note that XA needs to be configured even if the I2C is in slave mode.
7	RM	RW	0h	Repeat Mode. This bit is set to a"1" by the CPU to put the I2C in the repeat mode. In this mode data is continuously transmitted out of the ICDXR until the STP bit is set to"1" regardless of ICCNT value. This bit is don"t care if the I2C is configured in slave mode. _____ __RM___STT___STP___Conditions_____Bus Activities_____Mode _0_____0_____0_____Idle_____None_____NA _0_____0_____1_____Stop_____P_____NA _0_____1_____0_____(Re)Start_____S-A-D..(n)..D____Repeat n _0_____1_____1_____(Re)Start-Stop___S-A-D..(n)..D-P__Repeat n _1_____0_____0_____Idle_____none_____NA _1_____0_____1_____Stop_____P _____NA _1_____1_____0_____(Re)Start_____S-A-D-D-D..____Continuous _1_____1_____1_____Reserved_____None_____NA _____ __
6	DLB	RW	0h	Digital Loop Back (in master transmit mode only). This bit is set to a"1" by the CPU to put the I2C in the loop back mode. In this mode data transmitted out of the ICDXR will be received in the ICDRR after ((CPU freq/I2C freq)8) CPU cycles via an internal path. The address of the ICOAR is output on SDA.
5	IRS	RW	0h	I2C Reset Not. This can be set to a"0" by the CPU to put the I2C in reset or to a"1" to take the I2C out of reset. When this bit is reset to 0 all status bits in ICSTR and ICIVR are set to default values. Note that if this bit is reset during a transfer it can cause the I2C bus hang (SDA and SCL are tri-stated).
4	STB	RW	0h	Start Byte (Master only mode). The Start Byte mode bit is set to 1 by the CPU to configure the I2C in Start byte mode the I2C sends "00000001"? regardless ICSAR value. Refer to the Philip I2C spec for more details.
3	FDF	RW	0h	Free Data Format. This bit can be set to"1" by the CPU to configure the I2C in Free Data Format mode. _____FDF___MST___TRX_____Operating mode _0_____0_____ x____Slave in non FDF mode _0_____1_____0____Master receive in non FDF mode _0_____1_____1____Master transmit in non FDF mode _1_____0_____0____Slave receiver in FDF mode _1_____0_____1____Slave transmitter in FDF mode _1_____1_____0____Master receiver in FDF mode _1_____1_____1____Master transmitter in FDF mode _____

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Table 4-1795. ICMDR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2 - 0	BC2_BC1_BC0	RW	0h	Bit Count : Bit Count 2, Bit Count 1 and Bit Count 0 define the number of bits starting from the lsb (excluding the acknowledge bit) of the next byte which are yet to be received or transmitted. BC2_BC1_BC0 Bits/byte in FDF Bits/byte w/ ACK 0 0 0 8 9 0 0 1 7 8 0 1 0 6 7 0 1 1 5 6 1 0 0 4 5 1 0 1 3 4 1 1 0 2 3 1 1 1 1 NA (reserved) NA (reserved)

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4.17.12 MSS_I2Cn_ICIVR Registers

4.17.12.1 I2Cn_ICIVR Register (Offset = 28h) [reset = h]

Short Description: I2C Interrupt Vector register

Long Description:

Return to Summary Table

Table 4-1796. Instance Table

Instance Name	Physical Address
I2C0	5250 0028h
I2C1	5250 1028h
I2C2	5250 2028h
I2C3	5250 3028h

Access Types Legend

Table 4-1797. ICIVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 12	NU2	RW	0h	Reserved.
11 - 8	TESTMD	RW	0h	Reserved for internal testing.
7 - 3	NU1	RW	0h	Reserved.
2 - 0	INTCODE	RW	0h	Interrupt code. The binary-coded-interrupt vector indicates which interrupt has occurred. Reading the ICIVR clears the interrupt code except ARDY(011) RRDY(100) and XRDY(101). Interrupt code for ARDY RRDY and XRDY is cleared when ARDY ICRRDY and ICXRDY bits in the ICSTR is cleared to default value respectively. If other interrupts are pending a new interrupt is generated. If there are more than one interrupt flag reading the ICIVR clears the highest priority interrupt code. Reading the ICIVR also clears corresponding status bit in the ICSTR except ARDY ICRRDY ICXRDY and AAS. Note that users must read (clear) the ICIVR before doing another start otherwise the ICIVR could contain incorrect (old interrupt flags) value. Interrupt Code Interrupt Occurred 000 (default) None 001 (highest priority) Arbitration Lost interrupt 010 No Acknowledgement interrupt 011 Register Access Ready interrupt 100 Receive Data Ready interrupt 101 Transmit Data Ready interrupt 110 Stop Condition Detection 111 (lowest priority) Address As Slave - (RW)

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4.17.13 MSS_I2Cn_ICEMDR Registers

4.17.13.1 I2Cn_ICEMDR Register (Offset = 2Ch) [reset = h]

Short Description: I2C Extended Mode register

Long Description:

Return to Summary Table

Table 4-1798. Instance Table

Instance Name	Physical Address
I2C0	5250 002Ch
I2C1	5250 102Ch
I2C2	5250 202Ch
I2C3	5250 302Ch

Access Types Legend

Table 4-1799. ICEMDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved. - (RW)
1	IGNACK	RW	0h	Ignore NACK mode IGNACK=0 The master transmitter will operate normally discontinue the data transfer and set the ARDY and NACK status bits when a NACK signal is received from the slave. IGNACK=1 The master transmitter will ignore a NACK received from the slave.
0	BCM	RW	0h	Backward Compatibility Mode. This bit affects the I2C interrupt behavior.

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4.17.14 MSS_I2Cn_ICPSC Registers

4.17.14.1 I2Cn_ICPSC Register (Offset = 30h) [reset = h]

Short Description: I2C Prescaler register

Long Description:

Return to Summary Table

Table 4-1800. Instance Table

Instance Name	Physical Address
I2C0	5250 0030h
I2C1	5250 1030h
I2C2	5250 2030h
I2C3	5250 3030h

Access Types Legend

Table 4-1801. ICPSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU	RW	0h	Reserved.
7 - 0	IPSC7_IPSC0	RW	0h	8-bit prescaler to divide the system clock down to 4/8/12Mhz clock and used by the I2C module. This register must be initialized while the I2C is still in reset (IRS_=0). The value takes effect on the rising edge of IRS_.

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4.17.15 MSS_I2Cn_ICPID1 Registers

4.17.15.1 I2Cn_ICPID1 Register (Offset = 34h) [reset = h]

Short Description: I2C Peripheral ID register 1

Long Description:

Return to Summary Table

Table 4-1802. Instance Table

Instance Name	Physical Address
I2C0	5250 0034h
I2C1	5250 1034h
I2C2	5250 2034h
I2C3	5250 3034h

Access Types Legend

Table 4-1803. ICPID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU	RW	0h	Reserved.
15 - 8	CLASS	RW	0h	Identifies the class of peripheral. This value should be 0x01 - (RW)
7 - 0	REVISION	RW	0h	Identifies the revision level of the I2C. This value should be incremented each time the design is revised. - (RW)

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4.17.16 MSS_I2Cn_ICPID2 Registers

4.17.16.1 I2Cn_ICPID2 Register (Offset = 38h) [reset = h]

Short Description: I2C Peripheral ID register 2

Long Description:

Return to Summary Table

Table 4-1804. Instance Table

Instance Name	Physical Address
I2C0	5250 0038h
I2C1	5250 1038h
I2C2	5250 2038h
I2C3	5250 3038h

Access Types Legend

Table 4-1805. ICPID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU	RW	0h	Reserved.
7 - 0	TYPE	RW	0h	Identifies the type of peripheral. This value should be 0x05 - (RW)

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4.17.17 MSS_I2Cn_ICDMAC Registers

4.17.17.1 I2Cn_ICDMAC Register (Offset = 3Ch) [reset = h]

Short Description: I2C DMA Control Register

Long Description:

Return to Summary Table

Table 4-1806. Instance Table

Instance Name	Physical Address
I2C0	5250 003Ch
I2C1	5250 103Ch
I2C2	5250 203Ch
I2C3	5250 303Ch

Access Types Legend

Table 4-1807. ICDMAC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved. - (RW)
1	TXDMAEN	RW	0h	Transmit DMA enable. This bit controls the receive DMA event pin to the system. When this bit is 1 the DMA event is enabled and ICTEVT_POR pin is asserted when the DMA transfer is required. When this bit is 0 the ICTEVT_POR pin is never asserted. RXDMAEN=0: DMA transmit event is disabled. RXDMAEN=1: DMA transmit event is enabled. (Default)
0	RXDMAEN	RW	0h	Receive DMA enable. This bit controls the receive DMA event pin to the system. When this bit is 1 the DMA event is enabled and ICREVT_POR pin is asserted when the DMA transfer is required. When this bit is 0 the ICREVT_POR pin is never asserted. RXDMAEN=0: DMA receive event is disabled. RXDMAEN=1: DMA receive event is enabled. (Default)

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4.17.18 MSS_I2Cn_I2C_RESERVED1 Registers

4.17.18.1 I2Cn_RESERVED1 Register (Offset = 40h) [reset = h]

Short Description: Reserved

Long Description:

Return to Summary Table

Table 4-1808. Instance Table

Instance Name	Physical Address
I2C0	5250 0040h
I2C1	5250 1040h
I2C2	5250 2040h
I2C3	5250 3040h

Access Types Legend

Table 4-1809. I2C_RESERVED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU	RW	0h	Reserved.

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4.17.19 MSS_I2Cn_I2C_RESERVED2 Registers

4.17.19.1 I2Cn_RESERVED2 Register (Offset = 44h) [reset = h]

Short Description: Reserved

Long Description:

Return to Summary Table

Table 4-1810. Instance Table

Instance Name	Physical Address
I2C0	5250 0044h
I2C1	5250 1044h
I2C2	5250 2044h
I2C3	5250 3044h

Access Types Legend

Table 4-1811. I2C_RESERVED2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU	RW	0h	Reserved.

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4.17.20 MSS_I2Cn_ICPFUNC Registers

4.17.20.1 I2Cn_ICPFUNC Register (Offset = 48h) [reset = h]

Short Description: I2C Pin Function register

Long Description:

Return to Summary Table

Table 4-1812. Instance Table

Instance Name	Physical Address
I2C0	5250 0048h
I2C1	5250 1048h
I2C2	5250 2048h
I2C3	5250 3048h

Access Types Legend

Table 4-1813. ICPFUNC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU	RW	0h	Reserved.
0	PFUNC0	RW	0h	Controls the function of the I2C SCL and SDA pins. 0 = Pins function as SCL and SDA 1 = Pins functions as GPIO Note: No hardware protection is required to disable I2C function when the PFUNC[0] and IRS_ bits are both set to one. When PFUNC[0] is"1" (GPIO mode) the sub-module which controls the I2C function receives the value"1" for SCL and SDA. IRS_ can be set to"1" regardless of PFUNC[0] and the I2C function works whenever the IRS_ bit is"1". The user is expected to hold I2C in reset via IRS_ bit when changing to/from GPIO mode via the PFUNC[0] bit.

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4.17.21 MSS_I2Cn_ICPDIR Registers

4.17.21.1 I2Cn_ICPDIR Register (Offset = 4Ch) [reset = h]

Short Description: I2C Pin Direction register

Long Description:

Return to Summary Table

Table 4-1814. Instance Table

Instance Name	Physical Address
I2C0	5250 004Ch
I2C1	5250 104Ch
I2C2	5250 204Ch
I2C3	5250 304Ch

Access Types Legend

Table 4-1815. ICPDIR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDIR1	RW	0h	Controls the direction of the I2C SDA pin when configured as GPIO. 0 = SDA pin functions as input 1 = SDA pin functions as output
0	PDIR0	RW	0h	Controls the direction of the I2C SCL pin when configured as GPIO. 0 = SCL pin functions as input 1 = SCL pin functions as output

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4.17.22 MSS_I2Cn_ICPDIN Registers

4.17.22.1 I2Cn_ICPDIN Register (Offset = 50h) [reset = h]

Short Description: I2C Pin Data In register

Long Description:

Return to Summary Table

Table 4-1816. Instance Table

Instance Name	Physical Address
I2C0	5250 0050h
I2C1	5250 1050h
I2C2	5250 2050h
I2C3	5250 3050h

Access Types Legend

Table 4-1817. ICPDIN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDIN1	RW	0h	Indicates the logic level present on the SDA pin. Reads: 0 = Logic low present at SDA pin regardless of PFUNC setting. 1 = Logic high present at SDA pin regardless of PFUNC setting. Writes: Writes have no effect. - (RW)
0	PDIN0	RW	0h	Indicates the logic level present on the SCL pin. Reads: 0 = Logic low present at SCL pin regardless of PFUNC setting. 1 = Logic high present at SCL pin regardless of PFUNC setting. Writes: Writes have no effect - (RW)

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4.17.23 MSS_I2Cn_ICPDOUT Registers

4.17.23.1 I2Cn_ICPDOUT Register (Offset = 54h) [reset = h]

Short Description: I2C Pin Data Out register

Long Description:

Return to Summary Table

Table 4-1818. Instance Table

Instance Name	Physical Address
I2C0	5250 0054h
I2C1	5250 1054h
I2C2	5250 2054h
I2C3	5250 3054h

Access Types Legend

Table 4-1819. ICPDOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDOUT1	RW	0h	Controls the level driven on the SDA pin when configured as GPIO output. Reads: Reads return register values not GPIO pin levels. Writes: 0 = SDA pin driven low 1 = SDA pin driven high. Note: If SDA is connected to an open-drain buffer at the chiplevel the I2C cannot drive SDA to high.
0	PDOUT0	RW	0h	Controls the level driven on the SCL pin when configured as GPIO output. Reads: Reads return register values not GPIO pin levels. Writes: 0 = SCL pin driven low 1 = SCL pin driven high Note: If SCL is connected to an open-drain buffer at the chiplevel the I2C cannot drive SCL to high.

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4.17.24 MSS_I2Cn_ICPDSET Registers

4.17.24.1 I2Cn_ICPDSET Register (Offset = 58h) [reset = h]

Short Description: I2C Pin Data Set register

Long Description:

Return to Summary Table

Table 4-1820. Instance Table

Instance Name	Physical Address
I2C0	5250 0058h
I2C1	5250 1058h
I2C2	5250 2058h
I2C3	5250 3058h

Access Types Legend

Table 4-1821. ICPDSET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDSET1	RW	0h	Used to set PDOUT[1] bit which corresponds to the SDA GPIO pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[1] bit is set to logic high.
0	PDSET0	RW	0h	Used to set PDOUT[0] bit which corresponds to the SCL GPIO pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[0] bit is set to logic high.

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4.17.25 MSS_I2Cn_ICPDCLR Registers

4.17.25.1 I2Cn_ICPDCLR Register (Offset = 5Ch) [reset = h]

Short Description: I2C Pin Data Clear register

Long Description:

Return to Summary Table

Table 4-1822. Instance Table

Instance Name	Physical Address
I2C0	5250 005Ch
I2C1	5250 105Ch
I2C2	5250 205Ch
I2C3	5250 305Ch

Access Types Legend

Table 4-1823. ICPDCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDCLR1	RW	0h	Used to clear PDOUT[1] bit which corresponds to the SDA pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[1] bit is cleared to logic low.
0	PDCLR0	RW	0h	Used to clear PDOUT[0] bit which corresponds to the SCL pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[0] bit is cleared to logic low.

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4.17.26 MSS_I2Cn_ICPDRV Registers

4.17.26.1 I2Cn_ICPDRV Register (Offset = 60h) [reset = h]

Short Description: I2C Pin Driver Mode Register

Long Description:

Return to Summary Table

Table 4-1824. Instance Table

Instance Name	Physical Address
I2C0	5250 0060h
I2C1	5250 1060h
I2C2	5250 2060h
I2C3	5250 3060h

Access Types Legend

Table 4-1825. ICPDRV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU	RW	0h	Reserved
1	PDRV1	RW	0h	Used to select driver mode of output buffer for SDA pin. 0 = I2C mode. 1 = GPIO mode. Note: Value of this register is reflected on the PDRV_SDA_POR port. Actual function depends on I/O buffer and chip implementation.
0	PDRV0	RW	0h	Used to select driver mode of output buffer for SCL pin. 0 = I2C mode. 1 = GPIO mode. Note: Value of this register is reflected on the PDRV_SCL_POR port. Actual function depends on I/O buffer and chip implementation.

4.17.27 Access Table

Table 4-1826. Access Type Codes

Access Type	Code	Description
RW	RW	Read / Write

4.18 L2 Registers

Table 4-1827. MSS_L2 Registers Base Address Table

Offset	Length	Acronym	MSS_L2 Physical Address
0h	32	L2_START	7000 0000h
1FFFFCh	32	L2_END	701F FFFCh

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4.18.1 MSS_L2_START Registers

4.18.1.1 L2_START Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 4-1828. Instance Table

Instance Name	Physical Address
L2OCRAM	7000 0000h

Figure 4-679. MSS_L2_START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
RW															
0															

Access Types Legend

Table 4-1829. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	L2 Memory start address

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4.18.2 MSS_L2_END Registers

4.18.2.1 L2_END Register (Offset = 1FFFFCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 4-1830. Instance Table

Instance Name	Physical Address
L2OCRAM	701F FFFCh

Figure 4-680. MSS_L2_END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
RW															
0															

Access Types Legend

Table 4-1831. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	END	RW	0h	L2 Memory end address

4.18.3 Access Table

Table 4-1832. Access Type Codes

Access Type	Code	Description
RW	RW	Read / Write

4.19 LIN Registers

Table 4-1833. MSS_LIN[0:2] Registers Base Address Table

Offset	Length	Acronym	MSS_LIN0 Physical Address	MSS_LIN1 Physical Address	MSS_LIN2 Physical Address
0h	32	LIN_SCIGCR0	5240 0000h	5240 1000h	5240 2000h
4h	32	LIN_SCIGCR1	5240 0004h	5240 1004h	5240 2004h
8h	32	LIN_SCIGCR2	5240 0008h	5240 1008h	5240 2008h
Ch	32	LIN_SCISETINT	5240 000Ch	5240 100Ch	5240 200Ch
10h	32	LIN_SCICLEARINT	5240 0010h	5240 1010h	5240 2010h
14h	32	LIN_SCISETINTLVL	5240 0014h	5240 1014h	5240 2014h
18h	32	LIN_SCICLEARINTLVL	5240 0018h	5240 1018h	5240 2018h
1Ch	32	LIN_SCIFLR	5240 001Ch	5240 101Ch	5240 201Ch
20h	32	LIN_SCIINTVECT0	5240 0020h	5240 1020h	5240 2020h
24h	32	LIN_SCIINTVECT1	5240 0024h	5240 1024h	5240 2024h
28h	32	LIN_SCIFORMAT	5240 0028h	5240 1028h	5240 2028h
2Ch	32	LIN_BRSR	5240 002Ch	5240 102Ch	5240 202Ch
30h	32	LIN_SCIED	5240 0030h	5240 1030h	5240 2030h

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Table 4-1833. MSS_LIN[0:2] Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_LIN0 Physical Address	MSS_LIN1 Physical Address	MSS_LIN2 Physical Address
34h	32	LIN_SCIRD	5240 0034h	5240 1034h	5240 2034h
38h	32	LIN_SCITD	5240 0038h	5240 1038h	5240 2038h
3Ch	32	LIN_SCIPIO0	5240 003Ch	5240 103Ch	5240 203Ch
40h	32	LIN_SCIPIO1	5240 0040h	5240 1040h	5240 2040h
44h	32	LIN_SCIPIO2	5240 0044h	5240 1044h	5240 2044h
48h	32	LIN_SCIPIO3	5240 0048h	5240 1048h	5240 2048h
4Ch	32	LIN_SCIPIO4	5240 004Ch	5240 104Ch	5240 204Ch
50h	32	LIN_SCIPIO5	5240 0050h	5240 1050h	5240 2050h
54h	32	LIN_SCIPIO6	5240 0054h	5240 1054h	5240 2054h
58h	32	LIN_SCIPIO7	5240 0058h	5240 1058h	5240 2058h
5Ch	32	LIN_SCIPIO8	5240 005Ch	5240 105Ch	5240 205Ch
60h	32	LIN_LINCOMP	5240 0060h	5240 1060h	5240 2060h
64h	32	LIN_LINRD0	5240 0064h	5240 1064h	5240 2064h
68h	32	LIN_LINRD1	5240 0068h	5240 1068h	5240 2068h
6Ch	32	LIN_LINMASK	5240 006Ch	5240 106Ch	5240 206Ch
70h	32	LIN_LINID	5240 0070h	5240 1070h	5240 2070h
74h	32	LIN_LINTD0	5240 0074h	5240 1074h	5240 2074h
78h	32	LIN_LINTD1	5240 0078h	5240 1078h	5240 2078h
7Ch	32	LIN_MBRSR	5240 007Ch	5240 107Ch	5240 207Ch
80h	32	LIN_RESERVED_1	5240 0080h	5240 1080h	5240 2080h
90h	32	LIN_IODFTCTRL	5240 0090h	5240 1090h	5240 2090h
94h	32	LIN_RESERVED_2	5240 0094h	5240 1094h	5240 2094h
E0h	32	LIN_LIN_GLB_INT_EN	5240 00E0h	5240 10E0h	5240 20E0h
E4h	32	LIN_LIN_GLB_INT_FLG	5240 00E4h	5240 10E4h	5240 20E4h
E8h	32	LIN_LIN_GLB_INT_CLR	5240 00E8h	5240 10E8h	5240 20E8h

Table 4-1834. MSS_LIN[3:4] Registers Base Address Table

Offset	Length	Acronym	MSS_LIN3 Physical Address	MSS_LIN4 Physical Address
0h	32	LIN_SCIGCR0	5240 3000h	5240 4000h
4h	32	LIN_SCIGCR1	5240 3004h	5240 4004h
8h	32	LIN_SCIGCR2	5240 3008h	5240 4008h
Ch	32	LIN_SCISETINT	5240 300Ch	5240 400Ch
10h	32	LIN_SCICLEARINT	5240 3010h	5240 4010h
14h	32	LIN_SCISETINTLVL	5240 3014h	5240 4014h
18h	32	LIN_SCICLEARINTLVL	5240 3018h	5240 4018h
1Ch	32	LIN_SCIFLR	5240 301Ch	5240 401Ch
20h	32	LIN_SCIINTVECT0	5240 3020h	5240 4020h
24h	32	LIN_SCIINTVECT1	5240 3024h	5240 4024h
28h	32	LIN_SCIFORMAT	5240 3028h	5240 4028h
2Ch	32	LIN_BRSR	5240 302Ch	5240 402Ch
30h	32	LIN_SCIED	5240 3030h	5240 4030h
34h	32	LIN_SCIRD	5240 3034h	5240 4034h
38h	32	LIN_SCITD	5240 3038h	5240 4038h
3Ch	32	LIN_SCIPIO0	5240 303Ch	5240 403Ch
40h	32	LIN_SCIPIO1	5240 3040h	5240 4040h
44h	32	LIN_SCIPIO2	5240 3044h	5240 4044h

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Table 4-1834. MSS_LIN[3:4] Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_LIN3 Physical Address	MSS_LIN4 Physical Address
48h	32	LIN_SCIPIO3	5240 3048h	5240 4048h
4Ch	32	LIN_SCIPIO4	5240 304Ch	5240 404Ch
50h	32	LIN_SCIPIO5	5240 3050h	5240 4050h
54h	32	LIN_SCIPIO6	5240 3054h	5240 4054h
58h	32	LIN_SCIPIO7	5240 3058h	5240 4058h
5Ch	32	LIN_SCIPIO8	5240 305Ch	5240 405Ch
60h	32	LIN_LINCOMP	5240 3060h	5240 4060h
64h	32	LIN_LINRD0	5240 3064h	5240 4064h
68h	32	LIN_LINRD1	5240 3068h	5240 4068h
6Ch	32	LIN_LINMASK	5240 306Ch	5240 406Ch
70h	32	LIN_LINID	5240 3070h	5240 4070h
74h	32	LIN_LINTD0	5240 3074h	5240 4074h
78h	32	LIN_LINTD1	5240 3078h	5240 4078h
7Ch	32	LIN_MBRSR	5240 307Ch	5240 407Ch
80h	32	LIN_RESERVED_1	5240 3080h	5240 4080h
90h	32	LIN_IODFTCTRL	5240 3090h	5240 4090h
94h	32	LIN_RESERVED_2	5240 3094h	5240 4094h
E0h	32	LIN_LIN_GLB_INT_EN	5240 30E0h	5240 40E0h
E4h	32	LIN_LIN_GLB_INT_FLG	5240 30E4h	5240 30E4h
E8h	32	LIN_LIN_GLB_INT_CLR	5240 30E8h	5240 40E8h

4.19.1 LIN Instance Count Note

Note

n = 0 to 4 for the LIN registers defined below

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4.19.2 MSS_LINn_SCIGCR0 Registers

4.19.2.1 LINn_SCIGCR0 Register (Offset = 0h) [reset = h]

Short Description: The SCIGCR0 register defines the module reset.

Long Description:

Return to Summary Table

Table 4-1835. Instance Table

Instance Name	Physical Address
LIN0	5240 0000h
LIN1	5240 1000h
LIN2	5240 2000h
LIN3	5240 3000h
LIN4	5240 4000h

Figure 4-681. SCIGCR0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1															RESET
RO															RW/P
0															0

Access Types Legend

Table 4-1836. SCIGCR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_2	RO	0h	Reserved
15 - 1	RESERVED_1	RO	0h	Reserved
0	RESET	RW/P	0h	This bit resets the SCI/LIN module. [[br]]This bit is effective in LIN or SCI-compatible mode.. This bit affects the reset state of the SCI/LIN module. 0 | RESET_ONSCI/LIN module is in held in reset. 1 | RESET_OFFSCI/LIN module is out of reset.

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4.19.3 MSS_LINn_SCIGCR1 Registers

4.19.3.1 LINn_SCIGCR1 Register (Offset = 4h) [reset = h]

Short Description: The SCIGCR1 register defines the frame format, protocol, and communication mode used by the SCI.

Long Description:

Return to Summary Table

Table 4-1837. Instance Table

Instance Name	Physical Address
LIN0	5240 0004h
LIN1	5240 1004h
LIN2	5240 2004h
LIN3	5240 3004h
LIN4	5240 4004h

Figure 4-682. SCIGCR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3						TXENA	RXENA	RESERVED_2						CONT	LOOPBACK
RO						RW	RW	RO						RW	RW
0						0	0	0						0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1		STOP EXTFRAME	HGEN CTRL	CTYPE	MBUF MODE	ADAPT	SLEEP	SWNRST	LINMODE	CLK_MASTER	STOP	PARITY	PARITYENA	TIMINGMODE	COMMMODE
RO		RW	RW	RW	RW	RW	RW	RW	RW/P	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1838. SCIGCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	RESERVED_3	RO	0h	Reserved
25	TXENA	RW	0h	Transmit enable.[[br]]This bit is effective in LIN and SCI modes. Data is transferred from SCITD or the TDy (with y=0, 1,...7) buffers in LIN mode to the SCITXSHF shift out register only when the TXENA bit is set.[[br]] [[br]]Note: Data written to SCITD or the transmit multi-buffer before TXENA is set is not[[br]]transmitted. If TXENA is cleared while transmission is ongoing, the data previously[[br]]written to SCITD is sent (including the checksum byte in LIN mode). 0 | TXENA_DISABLEDisable transfers from SCITD or TDy to SCITXSHF 1 | TXENA_ENABLEEnable transfers of data from SCITD or TDy to SCITXSHF

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Table 4-1838. SCIGCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	RXENA	RW	0h	Receive enable.[[br]]This bit is effective in LIN or SCI-compatible mode. RXENA allows or prevents the transfer of data from SCIRXSHF to SCIRD or the receive multibuffers.[[br]] [[br]]Note: Clearing RXENA stops received characters from being transferred into the receive buffer or multi-buffers, prevents the RX status flags (see Table 7) from being updated by receive data, and inhibits both receive and error interrupts. However, the shift register continues to assemble data regardless of the state of RXENA.[[br]] [[br]]Note: If RXENA is cleared before the time the reception of a frame is complete, the data from the frame is not transferred into the receive buffer.[[br]] [[br]]Note: If RXENA is set before the time the reception of a frame is complete, the data from the frame is transferred into the receive buffer. If RXENA is set while SCIRXSHF is in the process of assembling a frame, the status flags are not guaranteed to be accurate for that frame. To ensure that the status flagscorrectly reflect what was detected on the bus during a particular frame, RXENA should be set before the detection of that frame 0 | RXENA_SUSPENDPrevents the receiver from transferring data from the shift buffer to the receive buffer or multi-buffers 1 | RXENA_RUNAllows the receiver to transfer data from the shift buffer to the receive buffer or multi-buffers
23 - 18	RESERVED_2	RO	0h	Reserved
17	CONT	RW	0h	Continue on suspend.[[br]]This bit has an effect only when a program is being debugged with an emulator, and it determines how the SCI/LIN operates when the program is suspended. This bit affects the LIN counters. When this bit is set, the counters are not stopped during debug. When this bit is cleared, the counters are stopped during debug. 0 | CONT_SUSPENDWhen debug mode is entered, the SCI/LIN state machine is frozen. Transmissions and LIN counters are halted and resume when debug mode is exited. 1 | CONT_RUNWhen debug mode is entered, the SCI/LIN continues to operate until the current transmit and receive functions are complete.
16	LOOPBACK	RW	0h	Loopback bit.[[br]]This bit is effective in LIN or SCI-compatible mode. The self-checking option for the SCI/LIN can be selected with this bit. If the LINTX and LINRX pins are configured with SCI/LIN functionality, then the LINTX pin is internally connected to the LINRX pin. Externally, during loop back operation, the LINTX pin outputs a high value and the LINRX pin is in a high-impedance state. If this bit value is changed while the SCI/LIN is transmitting or receiving data, errors may result. 0 | LOOPBACK_DISABLELoopback mode is disabled. 1 | LOOPBACK_ENABLELoopback mode is enabled.
15 - 14	RESERVED_1	RO	0h	Reserved
13	STOPEXTFRAME	RW	0h	Stop extended frame communication.[[br]]This bit is effective in LIN mode only. This bit can be written only during extended frame communication. When the extended frame communication is stopped, this bit is cleared automatically. 0 | STOPEXTFRAME_NO_EFFECTNo effect 1 | STOPEXTFRAME_EFFECTExtended frame communication will be stopped, once current frame transmission/reception is completed.
12	HGENCTRL	RW	0h	HGEN control bit.[[br]]This bit is effective in LIN mode only. This bit controls the type of mask filtering comparison. 0 | HGENCTRL_IDBYTEID filtering using ID-Byte. [[br]]RECEIVEDID and IDBYTE fields in the LINID register are used for detecting a match (using TX/RXMASK values). Mask of 0xFF in LINMASK register will result in NO match. 1 | HGENCTRL_IDSLAVEID filtering using ID-SlaveTask byte (Recommended). [[br]]RECEIVEDID and IDSLAVETASKBYTE fields in the LINID register are used for detecting a match (using TX/RXMASK values). Mask of 0xFF in LINMASK register will result in ALWAYS match

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Table 4-1838. SCIGCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CTYPE	RW	0h	Checksum type.[[br]]This bit is effective in LIN mode only. This bit controls the type of checksum to be used: classic or enhanced. 0 | CTYPE_CLASSICClassic checksum is used. [[br]]This checksum is compatible with LIN 1.3 slave nodes. The classic checksum contains the modulo-256 sum with carry over all data bytes. Frames sent with Identifier 60 (0x3C) to 63 (0x3F) must allways use the classic checksum. 1 | CTYPE_ENHANCEDEnhanced checksum is used. [[br]]The enhanced checksum is compatible with LIN 2.0 and newer slave nodes. The enhanced checksum contains the modulo-256 sum with carry over all data bytes AND the protected Identifier.
10	MBUFMODE	RW	0h	Multibuffer mode.[[br]]This bit is effective in LIN or SCI-compatible mode. This bit controls receive/transmit buffer usage, that is, whether the RX/TX multibuffers are used or a single register, RD0/TD0, is used. 0 | MBUFMODE_DISABLEDThe multi-buffer mode is disabled. 1 | MBUFMODE_ENABLEDThe multi-buffer mode is enabled.
9	ADAPT	RW	0h	Adapt mode enable.[[br]]This mode is effective in LIN mode only. This bit has an effect during the detection of the Sync Field. There are two LIN protocol bit rate modes that could be enabled with this bit according to the Node capability file definition: automatic or select. Software and network configuration will decide which of the previous two modes. When this bit is cleared, the LIN 2.0 protocol fixed bit rate should be used. If the ADAPT bit is set, a LIN slave node detecting the baudrate will compare it to the prescalers in BRSR register and update it if they are different. The BRSR register will be updated with the new value. If this bit is not set there will be no adjustment to the BRSR register.[[br]] [[br]]This field is writable in LIN mode only. 0 | ADAPT_DISABLEAutomatic baudrate adjustment is disabled. 1 | ADAPT_ENABLEAutomatic baudrate adjustment is enabled.
8	SLEEP	RW	0h	SCI sleep.[[br]]SCI compatibility mode only. In a multiprocessor configuration, this bit controls the receive sleep function. Clearing this bit brings the SCI out of sleep mode.[[br]] [[br]]The receiver still operates when the SLEEP bit is set; however, RXRDY is updated and SCIRD is loaded with new data only when an address frame is detected. The remaining receiver status flags are updated and an error interrupt is requested if the corresponding interrupt enable bit is set, regardless of the value of the SLEEP bit. In this way, if an error is detected on the receive data line while the SCI is asleep, software can promptly deal with the error condition. The SLEEP bit is not automatically cleared when an address byte is detected.[[br]] [[br]]This field is writable in SCI mode only. 0 | SLEEP_DISABLESleep mode is disabled. 1 | SLEEP_ENABLESleep mode is enabled.
7	SWNRST	RW	0h	Software reset (active low).[[br]]This bit is effective in LIN or SCI-compatible mode. The SCI/LIN should only be configured while SWnRST = 0.[[br]] [[br]]Only the following configuration bits can be changed in runtime (i.e.,[[br]]while SWnRESET = 1):[[br]]- STOP EXT Frame (SCIGCR1[13])[[br]]- CC bit (SCIGCR2[17])[[br]]- SC bit (SCIGCR2[16]) 0 | SWNRST_RESETThe SCI/LIN is in its reset state; no data will be transmitted or received. Writing a 0 to this bit intializes the SCI/LIN state machines and operating flags. All affected logic is held in the reset state until a 1 is written to this bit. 1 | SWNRST_READYThe SCI/LIN is in its ready state; transmission and reception can occur. After this bit is set to 1, the configuration of the module should not change.
6	LINMODE	RW/P	0h	LIN mode[[br]]This bit controls the mode of operation of the module. 0 | LINMODE_DISABLELIN mode is disabled; SCI compatibility mode is enabled. 1 | LINMODE_ENABLELIN mode is enabled; SCI compatibility mode is disabled.

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Table 4-1838. SCIGCR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_MASTER	RW	0h	SCI internal clock enable or LIN Master/Slave configuration.[[br]]In the SCI mode, this bit enables the clock to the SCI module. In LIN mode, this bit determines whether a LIN node is a slave or master. 0 | CLK_MASTER_OFFSCI-compatible mode: Reserved.[[br]]LIN mode: The module is in slave mode. 1 | CLK_MASTER_ONSCI-compatible mode: Enable clock to the SCI module.[[br]]LIN mode: The node is in master mode.
4	STOP	RW	0h	SCI number of stop bits.[[br]]This bit is effective in SCI-compatible mode only.[[br]] [[br]]Note: The receiver checks for only one stop bit. However in idle-line mode, the receiver waits until the end of the second stop bit (if STOP = 1) to begin checking for an idle period. [[br]] [[br]]This field is writable in SCI mode only. 0 | STOP_ONEOne stop bit is used. 1 | STOP_TWOTwo stop bits are used.
3	PARITY	RW	0h	SCI parity odd/even selection.[[br]]This bit is effective in SCI-compatible mode only. If the PARITY ENA bit (SCIGCR1.2) is set, PARITY designates odd or even parity. The parity bit is calculated based on the data bits in each frame and the address bit (in address-bit mode). The start and stop fields in the frame are not included in the parity calculation.[[br]] [[br]]This field is writable in SCI mode only. 0 | PARITY_ODDOdd parity is used. The SCI transmits and expects to receive a value in the parity bit that makes odd the total number of bits in the frame with the value of 1. 1 | PARITY_EVENEven parity is used. The SCI transmits and expects to receive a value in the parity bit that makes even the total number of bits in the frame with the value of 1.
2	PARITYENA	RW	0h	Parity enable.[[br]]Enables or disables the parity function. 0 | PARITYENA_DISABLESCI-compatible mode: Parity disabled; no parity bit is generated during transmission or is expected during reception.[[br]]LIN mode: ID-parity verification is disabled. 1 | PARITYENA_ENABLESCI compatible mode: Parity enabled. A parity bit is generated during transmission and is expected during reception.[[br]]LIN mode: ID-parity verification is enabled.
1	TIMINGMODE	RW	0h	SCI timing mode bit.[[br]]This bit is effective in SCI-compatible mode only. It must be set to 1 when the SCI mode is used. This bit configures the SCI for asynchronous operation. 0 | TIMINGMODE_RSVDReserved. 1 | TIMINGMODE_SETMust be set to 1 when module is configured for SCI operation
0	COMMMODE	RW	0h	SCI/LIN communication mode bit.[[br]]In compatibility mode, it selects the SCI communication mode. In LIN mode it selects length control option for ID-field bits ID4 and ID5. 0 | COMMMODE_UNUSESCI-compatible mode: Idle-line mode is used. [[br]]LIN mode: ID4 and ID5 are not used for length control. 1 | COMMMODE_USESCI-compatible mode: Address-bit mode is used. [[br]]LIN mode: ID4 and ID5 are used for length control.

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4.19.4 MSS_LINn_SCIGCR2 Registers

4.19.4.1 LINn_SCIGCR2 Register (Offset = 8h) [reset = h]

Short Description: The SCIGCR2 register is used to send or compare a checksum byte during extended frames, to generate a wakeup and for low-power mode control of the LIN module.

Long Description:

Return to Summary Table

Table 4-1839. Instance Table

Instance Name	Physical Address
LIN0	5240 0008h
LIN1	5240 1008h
LIN2	5240 2008h
LIN3	5240 3008h
LIN4	5240 4008h

Figure 4-683. SCIGCR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3														CC	SC
RO														RW	RW
0														0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2							GENWU	RESERVED_1							POWERDOWN
RO							RW	RO							RW
0							0	0							0

Access Types Legend

Table 4-1840. SCIGCR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 18	RESERVED_3	RO	0h	Reserved
17	CC	RW	0h	Compare Checksum.[[br]]This mode is effective in LIN mode only. This bit is used by the receiver for extended frames to trigger a checksum compare. The user will initiate this transaction by writing a one to this bit.[[br]]In non multibuffer mode, once the CC bit is set, the checksum will be compared on the byte that is currently being received, expected to be the checkbyte.[[br]]During Multi-buffer mode, following are the scenarios associated with the CC bit :[[br]]- If CC bit is set during the reception of the data, then the byte that is received after the reception of the programmed no. of data bytes indicated by SCIFORMAT[18:16], is treated as a checksum byte.[[br]]- If CC bit is set during the IDLE period (i.e. during inter-frame space), then the next immediate byte will be treated as a checksum byte.[[br]] [[br]]A CE will immediatly be flagged if there is a checksum error. This bit is automatically cleared once the checksum is successfully compared. 0 | CC_NO_EFFECTNo effect 1 | CC_EFFECTCompare checksum on expected checkbyte

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Table 4-1840. SCIGCR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	SC	RW	0h	Send Checksum[[br]]This mode is effective in LIN mode only. This bit is used by the transmitter with extended frames to send a checkbyte. In non multibuffer mode the checkbyte will be sent after the current byte transmission. In multibuffer mode the checkbyte will be sent after the last byte count, indicated by the SCIFORMAT[18:16]). [[br]] [[br]]This field is writable in LIN mode only. 0 | SC_NO_CHECKNo checkbyte will be sent. 1 | SC_CHECKA checkbyte will be sent. This bit will automatically get cleared after the checkbyte is transmitted. The checksum will not be sent if this bit is set before transmitting the very first byte, that is, during interframe space.
15 - 9	RESERVED_2	RO	0h	Reserved
8	GENWU	RW	0h	Generate wakeup signal.[[br]]This bit controls the generation of a wakeup signal, by transmitting the TDO buffer value. This bit is cleared on reception of a valid sync break. 0 | GENWU_NO_EFFECTNo effect 1 | GENWU_EFFECTTransmit TDO for wakeup. This bit will be cleared on a SWnRST (SCIGCR1.7)
7 - 1	RESERVED_1	RO	0h	Reserved
0	POWERDOWN	RW	0h	Power down.[[br]]This bit is effective in LIN or SCI-compatible mode. When the powerdown bit is set, the SCI/LIN module attempts to enter local low-power mode. If the POWERDOWN bit is set while the receiver is actively receiving data and the wakeup interrupt is disabled, then the SCI/LIN will delay low-power mode from being entered until completion of reception. In LIN mode the user may set the POWERDOWN bit on Sleep Command reception or on idle bus detection (more than 4 seconds, i.e. 80,000 cycles at 20kHz) 0 | POWERDOWN_RUNNormal operation 1 | POWERDOWN_LOWRequest local low-power mode

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4.19.5 MSS_LINn_SCISETINT Registers

4.19.5.1 LINn_SCISETINT Register (Offset = Ch) [reset = h]

Short Description: The SCISETINT register is used to enable the various interrupts available in the LIN module.

Long Description:

Return to Summary Table

Table 4-1841. Instance Table

Instance Name	Physical Address
LIN0	5240 000Ch
LIN1	5240 100Ch
LIN2	5240 200Ch
LIN3	5240 300Ch
LIN4	5240 400Ch

Figure 4-684. SCISETINT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETBEINT	SETPBEINT	SETCEINT	SETISFEINT	SETNREINT	SETFEINT	SETOEINT	SETPEINT	RESERVED_5					SET_RX_DMA_ALL	SET_RX_DMA	SET_TX_DMA
RW	RW	RW	RW	RW	RW	RW	RW	RO					RW	RW	RW
0	0	0	0	0	0	0	0	0					0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_4		SETIDINT	RESERVED_3			SETRXINT	SETTXINT	SETTOA3WUSINT	SETTOAWUSINT	RESERVED_2	SETTIMEOUTINT	RESERVED_1		SETWAKEUPINT	SETBRKDTINT
RO		RW	RO			RW	RW	RW	RW	RO	RW	RO		RW	RW
0		0	0			0	0	0	0	0	0	0		0	0

Access Types Legend

Table 4-1842. SCISETINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SETBEINT	RW	0h	Set bit error interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when there is a bit error.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETBEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETBEINT_ENABLEInterrupt is enabled.
30	SETPBEINT	RW	0h	Set physical bus error interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when a physical bus error occurs.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETPBEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETPBEINT_ENABLEInterrupt is enabled.
29	SETCEINT	RW	0h	Set checksum-error Interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when there is a checksum error.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETCEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETCEINT_DEABLEInterrupt is enabled.
28	SETISFEINT	RW	0h	Set inconsistent-sync-field-error interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when there is an inconsistent sync field error.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETISFEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETISFEINT_ENABLEInterrupt is enabled.

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Table 4-1842. SCISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	SETNREINT	RW	0h	Set no-response-error interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when a no-response error occurs.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETNREINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETNREINT_ENABLEInterrupt is enabled.
26	SETFEINT	RW	0h	Set framing-error interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN module to generate an interrupt when a framing error occurs. 0 | SETFEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETFEINT_ENABLEInterrupt is enabled.
25	SETOEINT	RW	0h	Set overrun-error interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN module to generate an interrupt when an overrun error occurs. 0 | SETOEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETOEINT_ENABLEInterrupt is enabled.
24	SETPEINT	RW	0h	Set parity interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN module to generate an interrupt when a parity error occurs. 0 | SETPEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETPEINT_ENABLEInterrupt is enabled.
23 - 19	RESERVED_5	RO	0h	Reserved
18	SET_RX_DMA_ALL	RW	0h	Set receiver DMA for Address & Data frames.[[br]]This bit is effective in LIN or SCI-compatible mode. To enable RX DMA request for address and data frames this bit must be set. If it is cleared, RX interrupt request is generated for address frames and DMA requests are generated for data frames. 0 | SERXDMAALL_DISABLEReceiver DMA request is disabled for address frames (RX interrupt request is enabled for address frames). Writing a 0 to this bit has no effect. 1 | SERXDMAALL_ENABLEReceiver DMA request is enabled for address and data frames
17	SET_RX_DMA	RW	0h	Set receiver DMA.[[br]]This bit is effective in LIN or SCI-compatible mode. To enable DMA requests for the receiver this bit must be set. If it is cleared, interrupt requests are generated depending on SETRXINT. 0 | SERXDMA_DISABLEReceiver DMA request is disabled. Writing a 0 to this bit has no effect. 1 | SERXDMA_ENABLEReceiver DMA request is enabled.
16	SET_TX_DMA	RW	0h	Set transmit DMA.[[br]]This bit is effective in LIN or SCI-compatible mode. To enable DMA requests for the transmitter, this bit must be set. If it is cleared, interrupt requests are generated depending on SETTXINT. 0 | SETXDMA_DISABLETransmit DMA request is disabled. Writing a 0 to this bit has no effect. 1 | SETXDMA_ENABLETransmit DMA request is enabled
15 - 14	RESERVED_4	RO	0h	Reserved
13	SETIDINT	RW	0h	Set Identification interrupt.[[br]]This bit is effective in LIN mode only. This bit is set to enable interrupt once a valid matching identifier is received. 0 | SETIDINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETIDINT_ENABLEInterrupt is enabled.
12 - 10	RESERVED_3	RO	0h	Reserved
9	SETRXINT	RW	0h	Set Receiver interrupt.[[br]]Setting this bit enables the SCI/LIN to generate a receive interrupt after a frame has been completely received and the data is being transferred from SCIRXSHF to SCIRD. 0 | SETRXINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETRXINT_ENABLEInterrupt is enabled.
8	SETTXINT	RW	0h	Set Transmitter interrupt.[[br]]Setting this bit enables the SCI/LIN to generate a transmit interrupt as data is being transferred from SCITD to SCITXSHF and the TXRDY bit is being set. 0 | SETTXINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETTXINT_ENABLEInterrupt is enabled.

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Table 4-1842. SCISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	SETTOA3WUSINT	RW	0h	Set Timeout After 3 Wakeup Signals interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN to generate an interrupt when there is a timeout after 3 wakeup signals have been sent.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETTOA3WUSINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETTOA3WUSINT_ENABLEInterrupt is enabled.
6	SETTOAWUSINT	RW	0h	Set Timeout After Wakeup Signal interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN to generate an interrupt when there is a timeout after one wakeup signal has been sent.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETTOAWUSINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETTOAWUSINT_ENABLEInterrupt is enabled.
5	RESERVED_2	RO	0h	Reserved
4	SETTIMEOUTINT	RW	0h	Set timeout interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN to generate an interrupt when no LIN bus activity (bus idle) occurs for at least 4 seconds.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETTIMEOUTINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETTIMEOUTINT_ENABLEInterrupt is enabled.
3 - 2	RESERVED_1	RO	0h	Reserved
1	SETWAKEUPINT	RW	0h	Set wake-up interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN to generate a wake-up interrupt and thereby exit low-power mode. The wake-up interrupt is asserted on falling edge of the wake-up pulse. If enabled, the wake-up interrupt is asserted when local low-power mode is requested while the receiver is busy or if a low level is detected on the SCIRX pin during low-power mode. Wake-up interrupt is not asserted upon a wakeup pulse if the module is not in power down mode. 0 | SETWAKEUPINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETWAKEUPINT_ENABLEInterrupt is enabled.
0	SETBRKDTINT	RW	0h	Set break-detect interrupt.[[br]]This bit is effective in SCI-compatible mode only. Setting this bit enables the SCI/LIN to generate an interrupt if a break condition is detected on the LINRX pin.[[br]] [[br]]This field is writable in SCI mode only. 0 | SETBRKDTINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | SETBRKDTINT_ENABLEInterrupt is enabled.

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4.19.6 MSS_LINn_SCICLEARINT Registers

4.19.6.1 LINn_SCICLEARINT Register (Offset = 10h) [reset = h]

Short Description: The SCICLEARINT register is used to disable the enabled interrupts without accessing the SCISETINT register.

Long Description:

Return to Summary Table

Table 4-1843. Instance Table

Instance Name	Physical Address
LIN0	5240 0010h
LIN1	5240 1010h
LIN2	5240 2010h
LIN3	5240 3010h
LIN4	5240 4010h

Figure 4-685. SCICLEARINT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRBEINT	CLRPBEINT	CLRCEINT	CLRISFEINT	CLRNREINT	CLRFEINT	CLROEINT	CLRPEINT	RESERVED_6					RESERVED_5	SETRXDMA	CLRTXDMA
RW	RW	RW	RW	RW	RW	RW	RW	RO					RO	RW	RW
0	0	0	0	0	0	0	0	0					0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_4		CLRIDINT	RESERVED_3			CLRRXINT	CLRTXINT	CLRTOA3WUSINT	CLRTOAWUSINT	RESERVED_2	CLRTIMEOUTINT	RESERVED_1		CLRWAKEUPINT	CLRBRKDTINT
RO		RW	RO			RW	RW	RW	RW	RO	RW	RO		RW	RW
0		0	0			0	0	0	0	0	0	0		0	0

Access Types Legend

Table 4-1844. SCICLEARINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLRBEINT	RW	0h	Clear Bit Error Interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the bit error interrupt.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRBEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRBEINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
30	CLRPBEINT	RW	0h	Clear Physical Bus Error Interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the physical-bus error interrupt.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRPBEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRPBEINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
29	CLRCEINT	RW	0h	Clear checksum-error Interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the checksum-error interrupt. [[br]] [[br]]This field is writable in LIN mode only. 0 | CLRCEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRCEINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.

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Table 4-1844. SCICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	CLRISFEINT	RW	0h	Clear Inconsistent-Sync-Field-Error Interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the ISFE interrupt. [[br]] [[br]]This field is writable in LIN mode only. 0 | CLRISFEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRISFEINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
27	CLRNREINT	RW	0h	Clear No-Reponse-Error Interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the no-response error interrupt.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRNREINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRNREINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
26	CLRFEINT	RW	0h	Clear Framing-Error Interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit disables framing-error interrupt. 0 | CLRFEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRFEINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
25	CLROEINT	RW	0h	Clear Overrun-Error Interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the overrun interrupt. 0 | CLROEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLROEINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
24	CLRPEINT	RW	0h	Clear Parity Interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the parity error interrupt. 0 | CLRPEINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRPEINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
23 - 19	RESERVED_6	RO	0h	Reserved
18	RESERVED_5	RO	0h	Reserved
17	SETRXDMA	RW	0h	Clear receiver DMA.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the receive DMA request. 0 | CLRRXDMA_DISABLEReceiver DMA request is disabled. Writing a 0 to this bit has no effect. 1 | CLRRXDMA_ENABLEReceiver DMA request is enabled. Writing a 1 to this bit will disable the DMA request and clear this bit.
16	CLRTXDMA	RW	0h	Clear transmit DMA.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the transmit DMA request. 0 | CLRTXDMA_DISABLETransmit DMA request is disabled. Writing a 0 to this bit has no effect. 1 | CLRTXDMA_ENABLETransmit DMA request is enabled. Writing a 1 to this bit will disable the DMA request and clear this bit.
15 - 14	RESERVED_4	RO	0h	Reserved
13	CLRIDINT	RW	0h	Clear Identifier interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the ID interrupt. 0 | CLRIDINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRIDINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
12 - 10	RESERVED_3	RO	0h	Reserved
9	CLRRXINT	RW	0h	Clear Receiver interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the receiver interrupt. 0 | CLRRXINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRRXINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
8	CLRTXINT	RW	0h	Clear Transmitter interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the transmitter interrupt. 0 | CLRTXINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRTXINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.

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Table 4-1844. SCICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CLRTOA3WUSINT	RW	0h	Clear Timeout After 3 Wakeup Signals interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the timeout after 3 wakeup signals interrupt.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRTOA3WUSINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRTOA3WUSINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
6	CLRTOAWUSINT	RW	0h	Clear Timeout After Wakeup Signal interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the timeout after one wakeup signal interrupt.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRTOAWUSINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRTOAWUSINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
5	RESERVED_2	RO	0h	Reserved
4	CLRTIMEOUTINT	RW	0h	Clear Timeout interrupt.[[br]]This bit is effective in LIN mode only. Setting this bit disables the timeout (LIN bus idle) interrupt.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRTIMEOUTINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRTIMEOUTINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
3 - 2	RESERVED_1	RO	0h	Reserved
1	CLRWAKEUPINT	RW	0h	Clear Wake-up interrupt.[[br]]This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the wake-up interrupt. 0 | CLRWAKEUPINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRWAKEUPINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.
0	CLRBRKDTINT	RW	0h	Clear Break-detect interrupt.[[br]]This bit is effective in SCI-compatible mode only. Setting this bit disables the Break-detect interrupt.[[br]] [[br]]This field is writable in SCI mode only. 0 | CLRBRKDTINT_DISABLEInterrupt is disabled. Writing a 0 to this bit has no effect. 1 | CLRBRKDTINT_ENABLEInterrupt is enabled. Writing a 1 to this bit will disable the interrupt and clear this bit.

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4.19.7 MSS_LINn_SCISETINTLVL Registers

4.19.7.1 LINn_SCISETINTLVL Register (Offset = 14h) [reset = h]

Short Description: The SCISETINTLVL register is used to map individual interrupt sources to the INT1 interrupt line.

Long Description:

Return to Summary Table

Table 4-1845. Instance Table

Instance Name	Physical Address
LIN0	5240 0014h
LIN1	5240 1014h
LIN2	5240 2014h
LIN3	5240 3014h
LIN4	5240 4014h

Figure 4-686. SCISETINTLVL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SETBEINTLVL	SETPBEINTLVL	SETCEINTLVL	SETISFEINTLVL	SETNREINTLVL	SETFEINTLVL	SETOEINTLVL	SETPEINTLVL	RESERVED_7					RESERVED_6	RESERVED_5	
RW	RW	RW	RW	RW	RW	RW	RW	RO					RO	RO	
0	0	0	0	0	0	0	0	0					0	0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_4		SETIDINTLVL	RESERVED_3			SETRXINTOVO	SETTXINTLVL	SETTOA3WUSINTLVL	SETTOAWUSINTLVL	RESERVED_2	SETTIMEOUTINTLVL	RESERVED_1		SETWAKEUPINTLVL	SETBRKDTINTLVL
RO		RW	RO			RW	RW	RW	RW	RO	RW	RO		RW	RW
0		0	0			0	0	0	0	0	0	0		0	0

Access Types Legend

Table 4-1846. SCISETINTLVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SETBEINTLVL	RW	0h	Set Bit Error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the Bit Error interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETBEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETBEINTLVL_INT1Interrupt level mapped to INT1 line.
30	SETPBEINTLVL	RW	0h	Set Physical Bus Error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the Physical Bus Error interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETPBEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETPBEINTLVL_INT1Interrupt level mapped to INT1 line.
29	SETCEINTLVL	RW	0h	Set Checksum-error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the Checksum-error interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETCEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETCEINTLVL_INT1Interrupt level mapped to INT1 line.
28	SETISFEINTLVL	RW	0h	Set Inconsistent-Sync-Field-Error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the Inconsistent-Sync-Field-Error interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETISFEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETISFEINTLVL_INT1Interrupt level mapped to INT1 line.

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Table 4-1846. SCISETINTLVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	SETNREINTLVL	RW	0h	Set No-Reponse-Error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the No-Response-Error interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETNREINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETNREINTLVL_INT1Interrupt level mapped to INT1 line.
26	SETFEINTLVL	RW	0h	Set Framing-Error interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Framing-Error interrupt level to the INT1 line. 0 | SETFEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETFEINTLVL_INT1Interrupt level mapped to INT1 line.
25	SETOEINTLVL	RW	0h	Set Overrun-Error Interrupt Level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Overrun-Error interrupt level to the INT1 line. 0 | SETOEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETOEINTLVL_INT1Interrupt level mapped to INT1 line.
24	SETPEINTLVL	RW	0h	Set Parity Error interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Parity error interrupt level to the INT1 line. 0 | SETPEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETPEINTLVL_INT1Interrupt level mapped to INT1 line.
23 - 19	RESERVED_7	RO	0h	Reserved
18	RESERVED_6	RO	0h	Reserved
17 - 16	RESERVED_5	RO	0h	Reserved
15 - 14	RESERVED_4	RO	0h	Reserved
13	SETIDINTLVL	RW	0h	Set ID interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the ID interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETIDINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETIDINTLVL_INT1Interrupt level mapped to INT1 line.
12 - 10	RESERVED_3	RO	0h	Reserved
9	SETRXINTOVO	RW	0h	Set Receiver interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the receiver interrupt level to the INT1 line. 0 | SETRXINTOVO_INT0Interrupt level mapped to INT0 line. 1 | SETRXINTOVO_INT1Interrupt level mapped to INT1 line.
8	SETTXINTLVL	RW	0h	Set Transmitter interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the transmitter interrupt level to the INT1 line. 0 | SETTXINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETTXINTLVL_INT1Interrupt level mapped to INT1 line.
7	SETTOA3WUSINTLVL	RW	0h	Set Timeout After 3 Wakeup Signals interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the timeout after 3 wakeup signals interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETTOA3WUSINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETTOA3WUSINTLVL_INT1Interrupt level mapped to INT1 line.
6	SETTOAWUSINTLVL	RW	0h	Set Timeout After Wakeup Signal interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the the timeout after wakeup interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETTOAWUSINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETTOAWUSINTLVL_INT1Interrupt level mapped to INT1 line.
5	RESERVED_2	RO	0h	Reserved
4	SETTIMEOUTINTLVL	RW	0h	Set Timeout interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the timeout interrupt level to the INT1 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | SETTIMEOUTINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETTIMEOUTINTLVL_INT1Interrupt level mapped to INT1 line.
3 - 2	RESERVED_1	RO	0h	Reserved

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Table 4-1846. SCISETINTLVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SETWAKEUPINTLVL	RW	0h	Set Wake-up interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Wake-up interrupt level to the INT1 line. 0 | SETWAKEUPINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETWAKEUPINTLVL_INT1Interrupt level mapped to INT1 line.
0	SETBRKDTINTLVL	RW	0h	Set Break-detect interrupt level.[[br]]This bit is effective in SCI-compatible mode only. Writing to this bit maps the Break-detect interrupt level to the INT1 line.[[br]] [[br]]This field is writable in SCI mode only. 0 | SETBRKDTINTLVL_INT0Interrupt level mapped to INT0 line. 1 | SETBRKDTINTLVL_INT1Interrupt level mapped to INT1 line.

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4.19.8 MSS_LINn_SCICLEARINTLVL Registers

4.19.8.1 LINn_SCICLEARINTLVL Register (Offset = 18h) [reset = h]

Short Description: The SCICLEARINTLVL register is used to map individual interrupt sources to the INT0 line.

Long Description:

Return to Summary Table

Table 4-1847. Instance Table

Instance Name	Physical Address
LIN0	5240 0018h
LIN1	5240 1018h
LIN2	5240 2018h
LIN3	5240 3018h
LIN4	5240 4018h

Figure 4-687. SCICLEARINTLVL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRBEINTLVL	CLRPBEINTLVL	CLRCEINTLVL	CLRISFEINTLVL	CLRNREINTLVL	CLRFEINTLVL	CLROEINTLVL	CLRPEINTLVL	RESERVED_7					RESERVED_6	RESERVED_5	
RW	RW	RW	RW	RW	RW	RW	RW	RO					RO	RO	
0	0	0	0	0	0	0	0	0					0	0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_4		CLRIDINTLVL	RESERVED_3			CLRRXINTLVL	CLRTXINTLVL	CLRTOA3WUSINTLVL	CLRTOAWUSINTLVL	RESERVED_2	CLRTIMEOUTINTLVL	RESERVED_1		CLRWAKEUPINTLVL	CLRBRKDTINTLVL
RO		RW	RO			RW	RW	RW	RW	RO	RW	RO		RW	RW
0		0	0			0	0	0	0	0	0	0		0	0

Access Types Legend

Table 4-1848. SCICLEARINTLVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLRBEINTLVL	RW	0h	Clear Bit Error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the Bit Error interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRBEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRBEINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
30	CLRPBEINTLVL	RW	0h	Clear Physical Bus Error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the Physical Bus Error interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRPBEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRPBEINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
29	CLRCEINTLVL	RW	0h	Clear Checksum-error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the Checksum-error interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRCEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRCEINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.

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Table 4-1848. SCICLEARINTLVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	CLRISFEINTLVL	RW	0h	Clear Inconsistent-Sync-Field-Error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the Inconsistent-Sync-Field-Error interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRISFEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRISFEINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
27	CLRNREINTLVL	RW	0h	Clear No-Reponse-Error interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the No-Response-Error interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRNREINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRNREINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
26	CLRFEINTLVL	RW	0h	Clear Framing-Error interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Framing-Error interrupt level to the INT0 line. 0 | CLRFEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRFEINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
25	CLROEINTLVL	RW	0h	Clear Overrun-Error Interrupt Level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Overrun-Error interrupt level to the INT0 line. 0 | CLROEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLROEINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
24	CLRPEINTLVL	RW	0h	Clear Parity Error interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Parity Error interrupt level to the INT0 line. 0 | CLRPEINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRPEINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
23 - 19	RESERVED_7	RO	0h	Reserved
18	RESERVED_6	RO	0h	Reserved
17 - 16	RESERVED_5	RO	0h	Reserved
15 - 14	RESERVED_4	RO	0h	Reserved
13	CLRIDINTLVL	RW	0h	Clear ID interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the ID interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRIDINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRIDINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
12 - 10	RESERVED_3	RO	0h	Reserved
9	CLRRXINTLVL	RW	0h	Clear Receiver interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the receiver interrupt level to the INT0 line. 0 | CLRRXINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRRXINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
8	CLRTXINTLVL	RW	0h	Clear Transmitter interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the transmitter interrupt level to the INT0 line. 0 | CLRTXINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRTXINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
7	CLRTOA3WUSINTLVL	RW	0h	Clear Timeout After 3 Wakeup Signals interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the timeout after 3 wakeup signals interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRTOA3WUSINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRTOA3WUSINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.

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Table 4-1848. SCICLEARINTLVL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CLRTOAWUSINTLVL	RW	0h	Clear Timeout After Wakeup Signal interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the the timeout after wakeup interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRTOAWUSINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRTOAWUSINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
5	RESERVED_2	RO	0h	Reserved
4	CLRTIMEOUTINTLVL	RW	0h	Clear Timeout interrupt level.[[br]]This bit is effective in LIN mode only. Writing to this bit maps the timeout interrupt level to the INT0 line.[[br]] [[br]]This field is writable in LIN mode only. 0 | CLRTIMEOUTINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRTIMEOUTINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
3 - 2	RESERVED_1	RO	0h	Reserved
1	CLRWAKEUPINTLVL	RW	0h	Clear Wake-up interrupt level.[[br]]This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Wake-up interrupt level to the INT0 line. 0 | CLRWAKEUPINTLVL_INT0Interrupt level mapped to INT0 line. Writing a 0 to this bit has no effect. 1 | CLRWAKEUPINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.
0	CLRBRKDTINTLVL	RW	0h	Clear Break-detect interrupt level.[[br]]This bit is effective in SCI-compatible mode only. Writing to this bit maps the Break-detect interrupt level to the INT0 line.[[br]] [[br]]This field is writable in SCI mode only. 0 | CLRBRKDTINTLVL_INT0Interrupt level mapped to INT0 line. 1 | CLRBRKDTINTLVL_INT1Interrupt level mapped to INT1 line. Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.

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4.19.9 MSS_LINn_SCIFLR Registers

4.19.9.1 LINn_SCIFLR Register (Offset = 1Ch) [reset = h]

Short Description: The SCIFLR register indicates the current status of the various interrupt sources of the LIN module.

Long Description:

Return to Summary Table

Table 4-1849. Instance Table

Instance Name	Physical Address
LIN0	5240 001Ch
LIN1	5240 101Ch
LIN2	5240 201Ch
LIN3	5240 301Ch
LIN4	5240 401Ch

Figure 4-688. SCIFLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BE	PBE	CE	ISFE	NRE	FE	OE	PE	RESERVED_3							
RW	RW	RW	RW	RW	RW	RW	RW	RO							
0	0	0	0	0	0	0	0	0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2	IDRXFLAG	IDTXFLAG	RXWAKE	TXEMPTY	TXWAKE	RXRDY	TXRDY	TOA3WUS	TOAWUS	RESERVED_1	TIMEOUT	BUSY	IDLE	WAKEUP	BRKDT
RO	RW	RW	RO	RO	RW	RW	RO	RW	RW	RO	RW	RO	RO	RW	RW
0	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0

Access Types Legend

Table 4-1850. SCIFLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BE	RW	0h	Bit Error Flag.[[br]]This bit is effective in LIN mode only. This bit is set when there has been a bit error. This is detected by the bit monitor in the internal bit monitor. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]]- Reception of a new sync break[[br]] [[br]]This field is writable in LIN mode only. 0 | BE_NO_EFFECTNo bit error detected. 1 | BE_EFFECTBit error detected.
30	PBE	RW	0h	Physical Bus Error Flag.[[br]]This bit is effective in LIN mode only. This bit is set when there has been a physical bus error. This is detected by the bit monitor in TED. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]]- Reception of a new sync break[[br]] [[br]]Note: thie PBE will ony be flagged if no sync break can be generated. (because of a bus shortage to VBAT) or if no sync break delimeter can be generated (because of a bus shortage to GND).[[br]] [[br]]This field is writable in LIN mode only. 0 | PBE_NO_EFFECTNo physiscal bus error detected. 1 | PBE_EFFECTPhysical bus error detected.

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Table 4-1850. SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	CE	RW	0h	Checksum Error Flag. [[br]]This bit is effective in LIN mode only. This bit is set when there is checksum error detected by a receiving node. The type of checksum to be used depends on the SCIGCR1.CTYPE bit. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]]- Reception of a new sync break[[br]] [[br]]This field is writable in LIN mode only. 0 | CE_NO_EFFECTNo Checksum error detected. 1 | CE_EFFECTChecksum error detected.
28	ISFE	RW	0h	Inconsistent Sync Field Error Flag.[[br]]This bit is effective in LIN mode only. This bit is set when there has been an inconsistent Sync Field error detected by the synchronizer during header reception. See the "Header Reception and Adaptive Baudrate" section for more information. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]]- Reception of a new sync break[[br]] [[br]]This field is writable in LIN mode only. 0 | ISFE_NO_EFFECTNo Inconsistent Sync Field error detected. 1 | ISFE_EFFECTInconsistent Sync Field error detected.
27	NRE	RW	0h	No-Response Error Flag.[[br]]This bit is effective in LIN mode only. This bit is set when there is no response to a master's header completed within TFRAME_MAX. This timeout period is applied for message frames of unknown length (identifiers 0 to 61). This error is detected by the synchronizer of the module. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]]- Reception of a new sync break[[br]] [[br]]This field is writable in LIN mode only. 0 | NRE_NO_EFFECTNo No-Response error detected. 1 | NRE_EFFECTNo-Response error detected.
26	FE	RW	0h	Framing error flag.[[br]]This bit is effective in LIN or SCI-compatible mode. This bit is set when an expected stop bit is not found. In SCI compatible mode, only the first stop bit is checked. The missing stop bit indicates that synchronization with the start bit has been lost and that the character is incorrectly framed. Detection of a framing error causes the SCI to generate an error interrupt if the RXERR INT ENA bit is set. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]]- Reception of a new character (SCI-compatible mode), or frame (LIN mode)[[br]]In multibuffer mode the frame is defined in the SCIFORMAT register. 0 | FE_NO_EFFECTNo framing error detected. 1 | FE_EFFECTFraming error detected.
25	OE	RW	0h	Overrun error flag.[[br]]This bit is effective in LIN or SCI-compatible mode. This bit is set when the transfer of data from SCIRXSHF to SCIRD overwrites unread data already in SCIRD or the RDy buffers. Detection of an overrun error causes the LIN to generate an error interrupt if the SET OE INT bit is one. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit 0 | OE_NO_EFFECTNo overrun error detected. 1 | OE_EFFECTOverrun error detected.

DRAFT
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Table 4-1850. SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	PE	RW	0h	Parity error flag.[[br]]This bit is effective in LIN or SCI-compatible mode. This bit is set when a parity error is detected in the received data. In SCI address-bit mode, the parity is calculated on the data and address bit fields of the received frame. In idle-line mode, only the data is used to calculate parity. An error is generated when a character is received with a mismatch between the number of 1s and its parity bit. For more information on parity checking, see the "SCI Global Control Register (SCIGCR1)" description. If the parity function is disabled (that is, SCIGCR1.2 = 0), the PE flag is disabled and read as 0. Detection of a parity error causes the LIN to generate an error interrupt if the SET PE INT bit = 1. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Reception of a new charcter (SCI-compatible mode) orframe (LIN mode)[[br]]- Writing a 1 to this bit 0 | PE_NO_EFFECTNo parity error or parity disabled. 1 | PE_EFFECTParity error detected.
23 - 16	RESERVED_3	RO	0h	Reserved
15	RESERVED_2	RO	0h	Reserved
14	IDRXFLAG	RW	0h	Identifier On Receive Flag.[[br]]This bit is effective in LIN mode only. This flag is set once an identifier is received with an RX match and no ID-parity error. See the "Message Filtering and Validation" section for more details. When this flag is set it indicates that a new valid identifier has been received on an RX match. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Reading the LINID register[[br]]- Writing a 1 to this bit[[br]] [[br]]This field is writable in LIN mode only. 0 | IDRXFLAG_NO_EFFECTNo valid ID received. 1 | IDRXFLAG_EFFECTValid ID RX received in LINID[23:16] on RX match.
13	IDTXFLAG	RW	0h	Identifier On Transmit Flag.[[br]]This bit is effective in LIN mode only. This flag is set once an identifier is received with a TX match and no ID-parity error. See the "Message Filtering and Validation" section for more details. When this flag is set it indicates that a new valid identifier has been received on a TX match. This bit is cleared by: [[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- RESET bit (SCIGCR0.0)[[br]]- Setting SWnRESET[[br]]- System reset[[br]]- Reading the LINID register[[br]]- Writing a 1 to this bit [[br]] [[br]]This field is writable in LIN mode only. 0 | IDTXFLAG_NO_EFFECTNo valid ID received. 1 | IDTXFLAG_EFFECTValid ID received in LINID[23:16] on TX match.
12	RXWAKE	RO	0h	Receiver wakeup detect flag.[[br]]This bit is effective in SCI-compatible mode only. The SCI sets this bit to indicate that the data currently in SCIRD is an address. This bit is cleared by: [[br]]- RESET bit[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- System reset[[br]]- Receipt of a data frame[[br]] [[br]]This bit is writable in SCI mode only. Read0 | RXWAKE_NO_EFFECTThe data in SCIRD is not an address. Read1 | RXWAKE_EFFECTThe data in SCIRD is an address.[[br]]See [1] Section 3.4.4, Sleep Mode for Multiprocessor Communication, on page 16 for more information on using the RXWAKE bit with sleep mode.

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Table 4-1850. SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TXEMPTY	RO	1h	Transmitter Empty flag.[[br]]The value of this flag indicates the contents of the transmitter's buffer register(s) (SCITD/TDy) and shift register (SCITXSHF). In multibuffer mode, this flag indicates the value of the TDx registers and shift register (SCITXSHF). In non multibuffer mode, this flag indicates the value of LINTD0 (byte) and shift register (SCITXSHF). This bit is set by: [[br]]- RESET bit (SCIGCR0.0)[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- System reset. [[br]] [[br]]Note: This bit does not cause an interrupt request. Read0 | TXEMPTY_NO_EFFECTCompatible mode or LIN with no multibuffer:[[br]]Transmitter buffer or shift register (or both) are loaded with data.[[br]]In LIN mode using multibuffer mode: [[br]]Multibuffer or shift register (or all) are loaded with data. Read1 | TXEMPTY_EFFECTCompatible mode or LIN with no multibuffer: [[br]]Transmitter buffer and shift registers are both empty.[[br]]In LIN mode using multibuffer mode:[[br]]Multibuffer and shift registers are all empty.
10	TXWAKE	RW	0h	SCI transmitter wakeup method select.[[br]]This bit is effective in SCI-compatible mode only. The TXWAKE bit controls whether the data in SCITD should be sent as an address or data frame using multiprocessor communication format. This bit is set to 1 or 0 by software before a byte is written to SCITD and is cleared by the SCI when data is transferred from SCITD to SCITXSHF or by a system reset. TXWAKE is not cleared by the SWnRESET bit (SCIGCR1.7). 0 | TXWAKE_ADDR0Address-bit mode: Frame to be transmitted will be data (address bit = 0).[[br]]Idle-line mode: Frame to be transmitted will be data. 1 | TXWAKE_ADDR1Address-bit mode:[[br]]Frame to be transmitted will be an address (address bit=1).[[br]]Idle-line mode: [[br]]Following frame to be transmitted will be an address (writing a 1 to this bit followed by writing dummy data to the SCITD will result in a idle period of 11 bit periods before the next frame is transmitted).
9	RXRDY	RW	0h	Receiver ready flag. [[br]]In SCI compatibility mode, the receiver sets this bit to indicate that the SCIRD contains new data and is ready to be read by the CPU. In LIN mode, RXRDY is set once a valid frame is received in multibuffer mode, a valid frame being a message frame received with no errors. In non multibuffer mode RXRDY is set for each received byte and will be set for the last byte of the frame if there are no errors. The SCI/LIN generates a receive interrupt when RXRDY flag bit is set[[br]]if the interrupt-enable bit is set (SCISETINT.9). RXRDY is cleared by:[[br]]- RESET bit (SCIGCR0.0)[[br]]- Setting the SWnRESET[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]]- Reading SCIRD in while in SCI compatibility mode[[br]]- Reading last data byte RDy of the response in LIN mode [[br]] [[br]]Note: The RXRDY flag cannot be cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register. 0 | RXRDY_NO_EFFECTNo new data in SCIRD/RDy. 1 | RXRDY_EFFECTNew data ready to be read from SCIRD.
8	TXRDY	RO	1h	Transmitter buffer register ready flag.[[br]]When set, this bit indicates that the transmit buffer(s) register (SCITD in compatibility mode and LINTD0, LINTD1 in MBUF mode) is/are ready to get another character from a CPU write. [[br]]In SCI compatibility mode, writing data to SCITD automatically clears this bit. In LIN mode, this bit is cleared once byte 0 (TD0) is written to LINTD0. This bit is set after the data of the TX buffer are shifted into the SCITXSHF register. This event can trigger a transmit DMA event if the DMA enable bit is set. This bit is set to 1 by:[[br]]- RESET bit (SCIGCR0.0)[[br]]- Setting the SWnRESET (SCIGCR1.7)[[br]]- System reset[[br]] [[br]]Note: The TXRDY flag cannot be cleared by reading the corresponding interrupt offset in the SCIINTVECT0/1 register.[[br]] [[br]]Note: The transmit interrupt request can be eliminated until the next series of data is written into the transmit buffers LINTD0 and LINTD1, by disaLINg the corresponding interrupt via theSCICLEARINT register or by disaLINg the transmitter via the TXENA bit (SCIGCR1.25=0). Read0 | TXRDY_FULLCompatible mode: SCITD is full.[[br]]LIN mode: The multibuffers are full. Read1 | TXRDY_EMPTYCompatible mode: SCITD is ready to receive the next character.[[br]]LIN mode: The multibuffers are ready to receive the next character(s).

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Table 4-1850. SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	TOA3WUS	RW	0h	Timeout After 3 Wakeup Signals flag.[[br]]This bit is effective in LIN mode only. This flag is set if there is no Sync Break received after 3 wakeup signals and a period of 1.5 seconds have passed. Such expiration time is used before issuing another round of wakeup signals. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]] [[br]]This field is writable in LIN mode only. 0 | TOA3WUS_NO_EFFECTNo timeout after 3 wakeup signals. 1 | TOA3WUS_EFFECTTimeout after 3 wakeup signals and 1.5s time.
6	TOAWUS	RW	0h	Timeout After Wakeup Signal flag.[[br]]This bit is effective in LIN mode only. This bit is set if there is no Sync Break received after a wakeup signal has been sent. A minimum of 150 ms expiration time is used before issuing another wakeup signal. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]] [[br]]This field is writable in LIN mode only. 0 | TOAWUS_NO_EFFECTNo timeout after one wakeup signal (150 ms). 1 | TOAWUS_EFFECTTimeout after one wakeup signal.
5	RESERVED_1	RO	0h	Reserved
4	TIMEOUT	RW	0h	LIN Bus IDLE timeout flag.[[br]]This bit is effective in LIN mode only. This bit is set if there is no LIN bus activity for at least 4 seconds. LIN bus activity being a transition from recessive to dominant. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit[[br]] [[br]]This field is writable in LIN mode only. 0 | TIMEOUT_NO_EFFECTNo bus idle detected. 1 | TIMEOUT_EFFECTLIN bus idle detected.
3	BUSY	RO	0h	Bus BUSY flag.[[br]]This bit is effective in LIN mode and SCI-compatible mode. This bit indicates whether the receiver is in the process of receiving a frame. As soon as the receiver detects the beginning of a start bit, the BUSY bit is set to 1. When the reception of a frame is complete, the BUSY bit is cleared. If SET WAKEUP INT is set and power down is requested while this bit is set, the SCI/LIN automatically prevents low-power mode from being entered and generates wakeup interrupt. The BUSY bit is controlled directly by the SCI receiver but can be cleared by:[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset. Read0 | BUSY_NO_EFFECTReceiver is not currently receiving a frame. Read1 | BUSY_EFFECTReceiver is currently receiving a frame.
2	IDLE	RO	1h	SCI receiver in idle state.[[br]]This bit is effective in SCI-compatible mode only. While this bit is set, the SCI looks for an idle period to resynchronize itself with the bit stream. The receiver does not receive any data while the bit is set. The bus must be idle for 11 bit periods to clear this bit. The SCI enters this state:[[br]]- After a system reset[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- After coming out of power down[[br]] [[br]]This bit is writable in SCI mode only. Read0 | IDLE_NO_EFFECTIdle period detected, the SCI is ready to receive. Read1 | IDLE_EFFECTIdle period not detected, the SCI will not receive any data.
1	WAKEUP	RW	0h	Wake-up flag.[[br]]This bit is effective in LIN mode only. This bit is set by the SCI/LIN when receiver or transmitter activity has taken the module out of power-down mode. An interrupt is generated if the SET WAKEUP INT bit (SCISETINT.1) is set. This bit is cleared by:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register.[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- Writing a 1 to this bit.[[br]] [[br]]This field is writable in LIN mode only. 0 | WAKEUP_NO_EFFECTDo not wake up from power-down mode. 1 | WAKEUP_EFFECTWake up from power-down mode.

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Table 4-1850. SCIFLR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	BRKDT	RW	0h	SCI break-detect flag.[[br]]This bit is effective in SCI-compatible mode only. This bit is set when the SCI detects a break condition on the LINRX pin. A break condition occurs when the LINRX pin remains continuously low for at least 10 bits after a missing first stop bit, that is, after a framing error. Detection of a break condition causes the SCI to generate an error interrupt if the BRKDT INT ENA bit is set. The BRKDT bit is cleared by the following:[[br]]- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register.[[br]]- Setting the SWnRESET bit (SCIGCR1.7)[[br]]- RESET bit (SCIGCR0.0)[[br]]- System reset[[br]]- By writing a 1 to this bit.[[br]] [[br]]This bit is writable in SCI mode only. 0 | BRKDT_NO_EFFECTNo break condition detected. 1 | BRKDT_EFFECTBreak condition detected.

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4.19.10 MSS_LINn_SCIINTVECT0 Registers

4.19.10.1 LINn_SCIINTVECT0 Register (Offset = 20h) [reset = h]

Short Description: The SCIINTVECT0 register indicates the offset for the INT0 interrupt line.

Long Description:

Return to Summary Table

Table 4-1851. Instance Table

Instance Name	Physical Address
LIN0	5240 0020h
LIN1	5240 1020h
LIN2	5240 2020h
LIN3	5240 3020h
LIN4	5240 4020h

Figure 4-689. SCIINTVECT0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1											INTVECT0				
RO											RO				
0											0				

Access Types Legend

Table 4-1852. SCIINTVECT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_2	RO	0h	Reserved
15 - 5	RESERVED_1	RO	0h	Reserved
4 - 0	INTVECT0	RO	0h	Interrupt vector offset for INT0.[[br]]This register indicates the offset for interrupt line INT0. A read to this register updates its value to the next highest priority pending interrupt in SCIFLR and clears the flag corresponding to the offset that was read.[[br]] [[br]]Note: The flags for the receive (SCIFLR.9) and the transmit (SCIFLR.8) interrupts cannot be cleared by reading the corresponding offset vector in this register (see detailed description in SCIFLR register).

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4.19.11 MSS_LINn_SCIINTVECT1 Registers

4.19.11.1 LINn_SCIINTVECT1 Register (Offset = 24h) [reset = h]

Short Description: The SCIINTVECT1 register indicates the offset for the INT1 interrupt line.

Long Description:

Return to Summary Table

Table 4-1853. Instance Table

Instance Name	Physical Address
LIN0	5240 0024h
LIN1	5240 1024h
LIN2	5240 2024h
LIN3	5240 3024h
LIN4	5240 4024h

Figure 4-690. SCIINTVECT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1											INTVECT1				
RO											RO				
0											0				

Access Types Legend

Table 4-1854. SCIINTVECT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_2	RO	0h	Reserved
15 - 5	RESERVED_1	RO	0h	Reserved
4 - 0	INTVECT1	RO	0h	Interrupt vector offset for INT1.[[br]]This register indicates the offset for interrupt line INT1. A read to this register updates its value to the next highest priority pending interrupt in SCIFLR and clears the flag corresponding to the offset that was read.[[br]] [[br]]Note: The flags for the receive (SCIFLR.9) and the transmit (SCIFLR.8) interrupts cannot be cleared by reading the corresponding offset vector in this register (see detailed description in SCIFLR register).

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4.19.12 MSS_LINn_SCIFORMAT Registers

4.19.12.1 LINn_SCIFORMAT Register (Offset = 28h) [reset = h]

Short Description: The SCIFORMAT register is used to set up the character and frame lengths.

Long Description:

Return to Summary Table

Table 4-1855. Instance Table

Instance Name	Physical Address
LIN0	5240 0028h
LIN1	5240 1028h
LIN2	5240 2028h
LIN3	5240 3028h
LIN4	5240 4028h

Figure 4-691. SCIFORMAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2													LENGTH		
RO													RW		
0													0		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1													CHAR		
RO													RW		
0													0		

Access Types Legend

Table 4-1856. SCIFORMAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 19	RESERVED_2	RO	0h	Reserved
18 - 16	LENGTH	RW	0h	Frame length control bits.[[br]]In LIN mode, these bits indicate the number of bytes in the response field from 1 to 8 bytes. In buffered SCI mode, these bits indicate the number of characters. When these bits are used to indicate LIN response length (SCIGCR1[0] = 1), then when there is an ID RX match, this value should be updated with the expected length of the response. In buffered SCI mode, these bits indicate the number of characters with SCIFORMAT[2:0] bits per character. i.e. these bits indicate the transmitter/receiver format for the number of characters: 1 to 8. There can be up to eight characters with eight bits each. 0x0 | FIELD_1The response field has 1 bytes/characters. 0x1 | FIELD_2The response field has 2 bytes/characters. 0x2 | FIELD_3The response field has 3 bytes/characters. 0x3 | FIELD_4The response field has 4 bytes/characters. 0x4 | FIELD_5The response field has 5 bytes/characters. 0x5 | FIELD_6The response field has 6 bytes/characters. 0x6 | FIELD_7The response field has 7 bytes/characters. 0x7 | FIELD_8The response field has 8 bytes/characters.
15 - 3	RESERVED_1	RO	0h	Reserved

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Table 4-1856. SCIFORMAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2 - 0	CHAR	RW	0h	Character length control bits.[[br]]These bits are effective in SCI compatible mode only. These bits set the SCI character length from 1 to 8 bits.[[br]] [[br]]Note: In compatibility mode or buffered SCI mode, when data of fewer than eight bits in length is received, it is left justified in SCIRD/RDy and padded with trailing zeros. Data read from the SCIRD should be shifted by software to make the received data right justified.[[br]] [[br]]Note: Data written to the SCITD should be right justified but does not need to be padded with leading zeros.[[br]] [[br]]These bits are witable in SCI mode only. 0x0 | CHAR_1The character is 1 bits long. 0x1 | CHAR_2The character is 2 bits long. 0x2 | CHAR_3The character is 3 bits long. 0x3 | CHAR_4The character is 4 bits long. 0x4 | CHAR_5The character is 5 bits long. 0x5 | CHAR_6The character is 6 bits long. 0x6 | CHAR_7The character is 7 bits long. 0x7 | CHAR_8The character is 8 bits long.

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4.19.13 MSS_LINn_BRSR Registers

4.19.13.1 LINn_BRSR Register (Offset = 2Ch) [reset = h]

Short Description: The BRSR register is used to configure the baud rate of the LIN module.

Long Description:

Return to Summary Table

Table 4-1857. Instance Table

Instance Name	Physical Address
LIN0	5240 002Ch
LIN1	5240 102Ch
LIN2	5240 202Ch
LIN3	5240 302Ch
LIN4	5240 402Ch

Figure 4-692. BRSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1	U			M				SCI_LIN_PSH							
RO	RW			RW				RW							
0	0			0				0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCI_LIN_PSL															
RW															
0															

Access Types Legend

Table 4-1858. BRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED_1	RO	0h	Reserved
30 - 28	U	RW	0h	Superfractional Divider Selection. (U)[[br]]These bits are an additional fractional part for the baudrate specification. These bits allow a super fine tuning of the fractional baudrate with 7 more intermediate values for each of the M fractional divider values. See the Superfractional Divider section for more details.
27 - 24	M	RW	0h	SCI/LIN 4-bit Fractional Divider Selection. (M)[[br]]These bits are effective in LIN or SCI asynchronous mode. These bits are used to select a baud rate for the SCI/LIN module, and they are a fractional part for the baud rate specification. The M divider allows fine-tuning of the baud rate over the P prescaler with 15 additional intermediate values for each of the P integer values.
23 - 16	SCI_LIN_PSH	RW	0h	PRESCALER P (High Bits).[[br]]SCI/LIN 24-bit Integer Prescaler Selection.[[br]]These bits are used to select a baudrate for the SCI/LIN module. These bits are effective in LIN mode and SCI compatible mode. The SCI/LIN has an internally generated serial clock determined by the LIN module input clock and the prescalers P and M in this register. The SCI/LIN uses the 24-bit integer prescaler P value to select 1 of over 16,700,000 available baud rates. The additional 4-bit fractional prescaler M refines the baudate selection.

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Table 4-1858. BRSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15 - 0	SCI_LIN_PSL	RW	0h	PRESCALER P (Low Bits).[[br]]SCI/LIN 24-bit Integer Prescaler Selection.[[br]]These bits are used to select a baudrate for the SCI/LIN module. These bits are effective in LIN mode and SCI compatible mode. The SCI/LIN has an internally generated serial clock determined by the LIN module input clock and the prescalers P and M in this register. The SCI/LIN uses the 24-bit integer prescaler P value to select 1 of over 16,700,000 available baud rates. The additional 4-bit fractional prescaler M refines the baudate selection.

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4.19.14 MSS_LINn_SCIED Registers

4.19.14.1 LINn_SCIED Register (Offset = 30h) [reset = h]

Short Description: The SCIED register is a duplicate copy of SCIRD register that has no affect on the RXRDY flag for use with an emulator.

Long Description:

Return to Summary Table

Table 4-1859. Instance Table

Instance Name	Physical Address
LIN0	5240 0030h
LIN1	5240 1030h
LIN2	5240 2030h
LIN3	5240 3030h
LIN4	5240 4030h

Figure 4-693. SCIED Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1								ED							
RO								RO							
0								0							

Access Types Legend

Table 4-1860. SCIED Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_1	RO	0h	Reserved
7 - 0	ED	RO	0h	Receiver Emulation Data.[[br]]This bit is effective in SCI-compatible mode only. Reading SCIED(7-0) does not clear the RXRDY flag. This register should be used only by an emulator that must continually read the data buffer without affecting the RXRDY flag.

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4.19.15 MSS_LINn_SCIRD Registers

4.19.15.1 LINn_SCIRD Register (Offset = 34h) [reset = h]

Short Description: The SCIRD register is where received data is stored and can be read from.

Long Description:

Return to Summary Table

Table 4-1861. Instance Table

Instance Name	Physical Address
LIN0	5240 0034h
LIN1	5240 1034h
LIN2	5240 2034h
LIN3	5240 3034h
LIN4	5240 4034h

Figure 4-694. SCIRD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1								RD							
RO								RO							
0								0							

Access Types Legend

Table 4-1862. SCIRD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_1	RO	0h	Reserved
7 - 0	RD	RO	0h	Received Data.[[br]]This bit is effective in SCI-compatible mode only. When a frame has been completely received, the data in the frame is transferred from the receiver shift register SCIRXSHF to this register. As this transfer occurs, the RXRDY flag is set and a receive interrupt is generated if RX INT ENA (SCISETINT0.9) is set. When the data is read from SCIRD, the RXRDY flag is automatically cleared.[[br]] [[br]]When the SCI receives data that is fewer than eight bits in length, it loads the data into this register in a left justified format padded with trailing zeros. Therefore, your software should perform a logical shift on the data by the correct number of positions to make it right justified.

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4.19.16 MSS_LINn_SCITD Registers

4.19.16.1 LINn_SCITD Register (Offset = 38h) [reset = h]

Short Description: The SCITD register is where data to be transmitted is written to by application software.

Long Description:

Return to Summary Table

Table 4-1863. Instance Table

Instance Name	Physical Address
LIN0	5240 0038h
LIN1	5240 1038h
LIN2	5240 2038h
LIN3	5240 3038h
LIN4	5240 4038h

Figure 4-695. SCITD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1								TD							
RO								RW							
0								0							

Access Types Legend

Table 4-1864. SCITD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_1	RO	0h	Reserved
7 - 0	TD	RW	0h	Transmit data[[br]]This bit is effective in SCI-compatible mode only. Data to be transmitted is written to this register. The transfer of data from this register to the transmit shift register SCITXSHF sets the TXRDY flag (SCIFLR.23), which indicates that SCITD is ready to be loaded with another byte of data. Note: If TX INT ENA (SCISETINT.8) is set, this data transfer also causes an interrupt.[[br]] [[br]]Note: Data written to the SCIRD register that is fewer than eight bits long must be right justified, but it does not need to be padded with leading zeros.

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4.19.17 MSS_LINn_SCIPIO0 Registers

4.19.17.1 LINn_SCIPIO0 Register (Offset = 3Ch) [reset = h]

Short Description: The SCIPIO0 register is used to enable the LINTX and LINRX pins.

Long Description:

Return to Summary Table

Table 4-1865. Instance Table

Instance Name	Physical Address
LIN0	5240 003Ch
LIN1	5240 103Ch
LIN2	5240 203Ch
LIN3	5240 303Ch
LIN4	5240 403Ch

Figure 4-696. SCIPIO0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXFUNC	RXFUNC	RESERVED_1
RO													RW	RW	RO
0													0	0	0

Access Types Legend

Table 4-1866. SCIPIO0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXFUNC	RW	0h	Transmit pin function.[[br]]This bit is effective in LIN or SCI mode. This bit defines the function of LINTX pin. 0 | LINTX_DISABLEDLINTX pin is disabled. 1 | LINTX_ENABLEDLINTX pin is enabled.
1	RXFUNC	RW	0h	Receive pin function.[[br]]This bit is effective in LIN or SCI mode. This bit defines the function of the LINRX pin. 0 | LINRX_DISABLEDLINRX pin is disabled. 1 | LINRX_ENABLEDLINRX pin is enabled.
0	RESERVED_1	RO	0h	Reserved

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4.19.18 MSS_LINn_SCIPIO1 Registers

4.19.18.1 LINn_SCIPIO1 Register (Offset = 40h) [reset = h]

Short Description: Pin control Register 1

Long Description:

Return to Summary Table

Table 4-1867. Instance Table

Instance Name	Physical Address
LIN0	5240 0040h
LIN1	5240 1040h
LIN2	5240 2040h
LIN3	5240 3040h
LIN4	5240 4040h

Figure 4-697. SCIPIO1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXDIR	RXDIR	RESERVED_1
RO													RW	RW	RO
0													0	0	0

Access Types Legend

Table 4-1868. SCIPIO1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXDIR	RW	0h	Transmit pin direction.[[br]]This bit is effective in LIN or SCI mode. This bit determines the data direction on the LINTX pin if it is configured with general-purpose I/O functionality (TX FUNC = 0). 0: general purpose input pin. 1: general-purpose output pin
1	RXDIR	RW	0h	Receive pin direction.[[br]]This bit is effective in LIN or SCI mode. This bit determines the data direction on the LINRX pin if it is configured with general-purpose I/O functionality (RX FUNC = 0). 0: general purpose input pin. 1: general-purpose output pin
0	RESERVED_1	RO	0h	Reserved

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4.19.19 MSS_LINn_SCIPIO2 Registers

4.19.19.1 LINn_SCIPIO2 Register (Offset = 44h) [reset = h]

Short Description: The SCIPIO2 register indicates the current status of the LINTX and LINRX pins.

Long Description:

Return to Summary Table

Table 4-1869. Instance Table

Instance Name	Physical Address
LIN0	5240 0044h
LIN1	5240 1044h
LIN2	5240 2044h
LIN3	5240 3044h
LIN4	5240 4044h

Figure 4-698. SCIPIO2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXIN	RXIN	RESERVED_1
RO													RO	RO	RO
0													0	0	0

Access Types Legend

Table 4-1870. SCIPIO2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXIN	RO	0h	Transmit data in.[[br]]This bit is effective in LIN or SCI-compatible mode. This bit contains the current value on the LINTX pin.
1	RXIN	RO	0h	Receive data in.[[br]]This bit is effective in LIN or SCI-compatible mode. This bit contains the current value on the LINRX pin.
0	RESERVED_1	RO	0h	Reserved

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4.19.20 MSS_LINn_SCIPIO3 Registers

4.19.20.1 LINn_SCIPIO3 Register (Offset = 48h) [reset = h]

Short Description: Pin control Register 3

Long Description:

Return to Summary Table

Table 4-1871. Instance Table

Instance Name	Physical Address
LIN0	5240 0048h
LIN1	5240 1048h
LIN2	5240 2048h
LIN3	5240 3048h
LIN4	5240 4048h

Figure 4-699. SCIPIO3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXOUT	RXOUT	RESERVED_1
RO													RW	RW	RO
0													0	0	0

Access Types Legend

Table 4-1872. SCIPIO3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXOUT	RW	0h	Transmit pin out.[[br]]This bit is effective in LIN or SCI mode. This pin specifies the logic to be output on pin LINTX.
1	RXOUT	RW	0h	Receive pin out.[[br]]This bit is effective in LIN or SCI mode. This pin specifies the logic to be output on pin LINRX.
0	RESERVED_1	RO	0h	Reserved

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4.19.21 MSS_LINn_SCIPIO4 Registers

4.19.21.1 LINn_SCIPIO4 Register (Offset = 4Ch) [reset = h]

Short Description: Pin control Register 4

Long Description:

Return to Summary Table

Table 4-1873. Instance Table

Instance Name	Physical Address
LIN0	5240 004Ch
LIN1	5240 104Ch
LIN2	5240 204Ch
LIN3	5240 304Ch
LIN4	5240 404Ch

Figure 4-700. SCIPIO4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXSET	RXSET	RESERVED_1
RO													RW	RW	RO
0													0	0	0

Access Types Legend

Table 4-1874. SCIPIO4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXSET	RW	0h	Transmit pin set.[[br]]This bit is effective in LIN or SCI mode. This bit sets the logic to be output on pin LINTX.
1	RXSET	RW	0h	Receive pin set.[[br]]This bit is effective in LIN or SCI mode. This bit sets the logic to be output on pin LINRX.
0	RESERVED_1	RO	0h	Reserved

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4.19.22 MSS_LINn_SCIPIO5 Registers

4.19.22.1 LINn_SCIPIO5 Register (Offset = 50h) [reset = h]

Short Description: Pin control Register 5

Long Description:

Return to Summary Table

Table 4-1875. Instance Table

Instance Name	Physical Address
LIN0	5240 0050h
LIN1	5240 1050h
LIN2	5240 2050h
LIN3	5240 3050h
LIN4	5240 4050h

Figure 4-701. SCIPIO5 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXCLR	RXCLR	RESERVED_1
RO													RW	RW	RO
0													0	0	0

Access Types Legend

Table 4-1876. SCIPIO5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXCLR	RW	0h	Transmit pin clear.[[br]]This bit is effective in LIN or SCI mode. This bit clears the logic to be output on pin LINTX.
1	RXCLR	RW	0h	Receive pin clear.[[br]]This bit is effective in LIN or SCI mode. This bit clears the logic to be output on pin LINRX.
0	RESERVED_1	RO	0h	Reserved

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4.19.23 MSS_LINn_SCIPIO6 Registers

4.19.23.1 LINn_SCIPIO6 Register (Offset = 54h) [reset = h]

Short Description: Pin control Register 6

Long Description:

Return to Summary Table

Table 4-1877. Instance Table

Instance Name	Physical Address
LIN0	5240 0054h
LIN1	5240 1054h
LIN2	5240 2054h
LIN3	5240 3054h
LIN4	5240 4054h

Figure 4-702. SCIPIO6 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXPDR	RXPDR	RESERVED_1
RO													RW	RW	RO
0													0	0	0

Access Types Legend

Table 4-1878. SCIPIO6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXPDR	RW	0h	Transmit pin open drain enable.[[br]]This bit is effective in LIN or SCI mode. This bit enables open-drain capability in the output pin LINTX.
1	RXPDR	RW	0h	Receive pin open drain enable.[[br]]This bit is effective in LIN or SCI mode. This bit enables open-drain capability in the output pin LINRX.
0	RESERVED_1	RO	0h	Reserved

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4.19.24 MSS_LINn_SCIPIO7 Registers

4.19.24.1 LINn_SCIPIO7 Register (Offset = 58h) [reset = h]

Short Description: Pin control Register 7

Long Description:

Return to Summary Table

Table 4-1879. Instance Table

Instance Name	Physical Address
LIN0	5240 0058h
LIN1	5240 1058h
LIN2	5240 2058h
LIN3	5240 3058h
LIN4	5240 4058h

Figure 4-703. SCIPIO7 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXPD	RXPD	RESERVED_1
RO													RW	RW	RO
0													0	0	0

Access Types Legend

Table 4-1880. SCIPIO7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXPD	RW	0h	Transmit pin pull control disable.[[br]]This bit is effective in LIN or SCI mode. This bit disables pull control capability on the input pin LINTX.
1	RXPD	RW	0h	Receive pin pull control disable.[[br]]This bit is effective in LIN or SCI mode. This bit disables pull control capability on the input pin LINRX.
0	RESERVED_1	RO	0h	Reserved

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4.19.25 MSS_LINn_SCIPIO8 Registers

4.19.25.1 LINn_SCIPIO8 Register (Offset = 5Ch) [reset = h]

Short Description: Pin control Register 8

Long Description:

Return to Summary Table

Table 4-1881. Instance Table

Instance Name	Physical Address
LIN0	5240 005Ch
LIN1	5240 105Ch
LIN2	5240 205Ch
LIN3	5240 305Ch
LIN4	5240 405Ch

Figure 4-704. SCIPIO8 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2													TXPSL	RXPSL	RESERVED_1
RO													RW	RW	RO
0													1	1	1

Access Types Legend

Table 4-1882. SCIPIO8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 3	RESERVED_2	RO	0h	Reserved
2	TXPSL	RW	1h	TX pin pull select.[[br]]This bit is effective in LIN or SCI mode. This bit selects pull type in the input pin LINTX.
1	RXPSL	RW	1h	RX pin pull select.[[br]]This bit is effective in LIN or SCI mode. This bit selects pull type in the input pin LINRX.
0	RESERVED_1	RO	1h	Reserved

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4.19.26 MSS_LINn_LINCOMP Registers

4.19.26.1 LINn_LINCOMP Register (Offset = 60h) [reset = h]

Short Description: The LINCOMPARE register is used to configure the sync delimeter and sync break extension.

Long Description:

Return to Summary Table

Table 4-1883. Instance Table

Instance Name	Physical Address
LIN0	5240 0060h
LIN1	5240 1060h
LIN2	5240 2060h
LIN3	5240 3060h
LIN4	5240 4060h

Figure 4-705. LINCOMP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2						SDEL		RESERVED_1					SBREAK		
RO						RW/P		RO					RW/P		
0						0		0					0		

Access Types Legend

Table 4-1884. LINCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED_3	RO	0h	Reserved
15 - 10	RESERVED_2	RO	0h	Reserved
9 - 8	SDEL	RW/P	0h	2-bit Sync Delimiter compare.[[br]]These bits are effective in LIN mode only. These bits are used to configure the number of Tbit for the sync delimiter in the sync field.[[br]]The time delay calculation for the synchronization delimiter is:[[br]]TSDEL = (SDEL + 1)Tbit[[br]] [[br]]These bits are writable in LIN mode only. 0x0 | SDEL_1The sync delimiter has 1 Tbit. 0x1 | SDEL_2The sync delimiter has 2 Tbit. 0x2 | SDEL_3The sync delimiter has 3 Tbit. 0x3 | SDEL_4The sync delimiter has 4 Tbit.
7 - 3	RESERVED_1	RO	0h	Reserved
2 - 0	SBREAK	RW/P	0h	3-bit Sync Break extend.[[br]]LIN mode only. These bits are used to configure the number of Tbits for the sync break to extend the minimum 13 Tbit in the Sync Field to a maximum of 20 Tbit.[[br]]The time delay calculation for the sync break is:[[br]]TSYNBRK = 13Tbit + SBREAK x Tbit[[br]] [[br]]These bits are writable in LIN mode only. 0x0 | SBREAK_0The sync break has no additional Tbit. 0x1 | SBREAK_1The sync break has 1 additional Tbit. 0x2 | SBREAK_2The sync break has 2 additional Tbit. 0x3 | SBREAK_3The sync break has 3 additional Tbit. 0x4 | SBREAK_4The sync break has 4 additional Tbit. 0x5 | SBREAK_5The sync break has 5 additional Tbit. 0x6 | SBREAK_6The sync break has 6 additional Tbit. 0x7 | SBREAK_7The sync break has 7 additional Tbit.

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4.19.27 MSS_LINn_LINRD0 Registers

4.19.27.1 LINn_LINRD0 Register (Offset = 64h) [reset = h]

Short Description: The LINRD0 register contains the lower 4 bytes of the received LIN frame data.

Long Description:

Return to Summary Table

Table 4-1885. Instance Table

Instance Name	Physical Address
LIN0	5240 0064h
LIN1	5240 1064h
LIN2	5240 2064h
LIN3	5240 3064h
LIN4	5240 4064h

Figure 4-706. LINRD0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RD0								RD1							
RO								RO							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD2								RD3							
RO								RO							
0								0							

Access Types Legend

Table 4-1886. LINRD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RD0	RO	0h	8-bit Receive Buffer 0[[br]]Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.[[br]]A read of this byte clears the RXDY byte.[[br]]Note: RD
23 - 16	RD1	RO	0h	8-bit Receive Buffer 1.[[br]]Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
15 - 8	RD2	RO	0h	8-bit Receive Buffer 2.[[br]]Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
7 - 0	RD3	RO	0h	8-bit Receive Buffer 3.[[br]]Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.

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4.19.28 MSS_LINn_LINRD1 Registers

4.19.28.1 LINn_LINRD1 Register (Offset = 68h) [reset = h]

Short Description: The LINRD1 regsiter contains the upper 4 bytes of the received LIN frame data.

Long Description:

Return to Summary Table

Table 4-1887. Instance Table

Instance Name	Physical Address
LIN0	5240 0068h
LIN1	5240 1068h
LIN2	5240 2068h
LIN3	5240 3068h
LIN4	5240 4068h

Figure 4-707. LINRD1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RD4								RD5							
RO								RO							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD6								RD7							
RO								RO							
0								0							

Access Types Legend

Table 4-1888. LINRD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RD4	RO	0h	8-bit Receive Buffer 4 [[br]]Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
23 - 16	RD5	RO	0h	8-bit Receive Buffer 5.[[br]]Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
15 - 8	RD6	RO	0h	8-bit Receive Buffer 6.[[br]]Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.
7 - 0	RD7	RO	0h	8-bit Receive Buffer 7.[[br]]Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.

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4.19.29 MSS_LINn_LINMASK Registers

4.19.29.1 LINn_LINMASK Register (Offset = 6Ch) [reset = h]

Short Description: The LINMASK register is used to configure the masks used for filtering incoming ID messages for receive and transmit frames.

Long Description:

Return to Summary Table

Table 4-1889. Instance Table

Instance Name	Physical Address
LIN0	5240 006Ch
LIN1	5240 106Ch
LIN2	5240 206Ch
LIN3	5240 306Ch
LIN4	5240 406Ch

Figure 4-708. LINMASK Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_2								RXIDMASK							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1								TXIDMASK							
RO								RW							
0								0							

Access Types Legend

Table 4-1890. LINMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED_2	RO	0h	Reserved
23 - 16	RXIDMASK	RW	0h	Receive ID mask.[[br]]This field is effective in LIN mode only.This 8-bit mask is used for filtering an incoming ID message and compare it to the ID-byte. A compare match of the received ID witht the RX ID mask will set the ID RX flag and trigger and ID interrupt if enabled. A 0 bit in the mask indicates that bit is compared to the ID-byte. A 1 bit in the mask indicates that that bit is filtered and therefore not used in the compare.[[br]] [[br]]When HGENCTRL is set to 1, this field must be set to 0xFF.
15 - 8	RESERVED_1	RO	0h	Reserved
7 - 0	TXIDMASK	RW	0h	Transmit ID mask.[[br]]This field is effective in LIN mode only. This 8-bit mask is used for filtering an incoming ID message and compare it to the ID-byte. A compare match of the received ID with the TX ID Mask will set the ID TX flag and trigger an ID interrupt if enabled. A 0 bit in the mask indicates that bit is compared to the ID-byte. A 1 bit in the mask indicates that bit is filtered and therefore not used for the compare.[[br]] [[br]]When HGENCTRL is set to 1, this field must be set to 0xFF.

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4.19.30 MSS_LINn_LINID Registers

4.19.30.1 LINn_LINID Register (Offset = 70h) [reset = h]

Short Description: The LINID register contains the identification fields for LIN communication.[[br]]NOTE: For software compatibility with future LIN modules, the HGEN CTRL bit must be set to 1, the RX ID MASK field must be set to FFh, and the TX ID MASK field must be set to FFh.

Long Description:

Return to Summary Table

Table 4-1891. Instance Table

Instance Name	Physical Address
LIN0	5240 0070h
LIN1	5240 1070h
LIN2	5240 2070h
LIN3	5240 3070h
LIN4	5240 4070h

Figure 4-709. LINID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1								RECEIVEDID							
RO								RO							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDSLAVETASKBYTE								IDBYTE							
RW								RW							
0								0							

Access Types Legend

Table 4-1892. LINID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED_1	RO	0h	Reserved
23 - 16	RECEIVEDID	RO	0h	Received ID.[[br]]This bit is effective in LIN mode only. This byte contains the current message identifier. During header reception the received ID is copied from the SCIRXSHF register to this byte if there is no ID-parity error and there has been an RX/TX match.[[br]]Note: If a framing error (FE) is detected during ID reception, the received ID will also not be copied to the LINID register.
15 - 8	IDSLAVETASKBYTE	RW	0h	ID Slave Task byte.[[br]]This field is effective in LIN mode only. This byte contains the identifier to which the received ID of an incoming header will be compared in order to decide whether a RX response, a TX response, or no action needs to be done by the LIN node. [[br]] [[br]]These bits are writable in LIN mode only.
7 - 0	IDBYTE	RW	0h	ID byte.[[br]]This field is effective in LIN mode only. This byte is the LIN mode message ID. On a master node, a write to this register by the CPU initiates a header transmission. For a slave task, this byte is used for message filtering when HGENCTRL (SCIGCR1.12) is '0'.[[br]] [[br]]These bits are writable in LIN mode only.

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4.19.31 MSS_LINn_LINTD0 Registers

4.19.31.1 LINn_LINTD0 Register (Offset = 74h) [reset = h]

Short Description: The LINTD0 register contains the lower 4 bytes of the data to be transmitted.[[br]]NOTE: TD

Long Description:

Return to Summary Table

Table 4-1893. Instance Table

Instance Name	Physical Address
LIN0	5240 0074h
LIN1	5240 1074h
LIN2	5240 2074h
LIN3	5240 3074h
LIN4	5240 4074h

Figure 4-710. LINTD0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TD0								TD1							
RW								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TD2								TD3							
RW								RW							
0								0							

Access Types Legend

Table 4-1894. LINTD0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	TD0	RW	0h	8-bit Transmit Buffer 0.[[br]]Byte 0 to be transmitted is written into this register and then copied to SCITXSHF for transmission. Once byte 0 is written in TDO buffer, transmission will be initiated.
23 - 16	TD1	RW	0h	8-bit Transmit Buffer 3.[[br]]Byte 1 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
15 - 8	TD2	RW	0h	8-bit Transmit Buffer 2.[[br]]Byte 2 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
7 - 0	TD3	RW	0h	8-bit Transmit Buffer 3.[[br]]Byte 3 to be transmitted is written into this register and then copied to SCITXSHF for transmission.

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4.19.32 MSS_LINn_LINTD1 Registers

4.19.32.1 LINn_LINTD1 Register (Offset = 78h) [reset = h]

Short Description: The LINTD1 register contains the upper 4 bytes of the data to be transmitted.[[br]]NOTE: TD

Long Description:

Return to Summary Table

Table 4-1895. Instance Table

Instance Name	Physical Address
LIN0	5240 0078h
LIN1	5240 1078h
LIN2	5240 2078h
LIN3	5240 3078h
LIN4	5240 4078h

Figure 4-711. LINTD1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TD4								TD5							
RW								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TD6								TD7							
RW								RW							
0								0							

Access Types Legend

Table 4-1896. LINTD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	TD4	RW	0h	8-bit Transmit Buffer 4.[[br]]Byte4 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
23 - 16	TD5	RW	0h	8-bit Transmit Buffer 5.[[br]]Byte 5 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
15 - 8	TD6	RW	0h	8-bit Transmit Buffer 6.[[br]]Byte 6 to be transmitted is written into this register and then copied to SCITXSHF for transmission.
7 - 0	TD7	RW	0h	8-bit Transmit Buffer 7.[[br]]Byte 7 to be transmitted is written into this register and then copied to SCITXSHF for transmission.

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4.19.33 MSS_LINn_MBRSR Registers

4.19.33.1 LINn_MBRSR Register (Offset = 7Ch) [reset = h]

Short Description: The MBRSR register is used to configure the expected maximum baud rate of the LIN network.

Long Description:

Return to Summary Table

Table 4-1897. Instance Table

Instance Name	Physical Address
LIN0	5240 007Ch
LIN1	5240 107Ch
LIN2	5240 207Ch
LIN3	5240 307Ch
LIN4	5240 407Ch

Figure 4-712. MBRSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1			MBR												
RO			RW												
0			110110101100												

Access Types Legend

Table 4-1898. MBRSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 13	RESERVED_1	RO	0h	Reserved
12 - 0	MBR	RW	19A312CE6Ch	Maximum Baud Rate Prescaler.[[br]]This field is effective in LIN mode only. This 13-bit prescaler is used during the synchronization phase (see the "Header Reception and Adaptive Baudrate" section) of a slave module if the ADAPT bit is set. In this way, a SCI/LIN slave using an automatic or select bit rate modes detects any LIN bus legal rate automatically.[[br]] [[br]]The MBR value should be programmed to allow a maximum baud rate that is not more than 10% above the expected operating baud rate in the LIN network. Otherwise a s 0x00 data byte could mistakenly be detected as sync break. [[br]]The default value is for a 70MHz LINCLK (0xDAC).[[br]]This MBR prescaler is used by the wake-up and idle time counters for a constant expiration time relative to a 20kHz rate.

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4.19.34 MSS_LINn_IODFTCTRL Registers

4.19.34.1 LINn_IODFTCTRL Register (Offset = 90h) [reset = h]

Short Description: The IODFTCTRL register is used to emulate various error and test conditions.

Long Description:

Return to Summary Table

Table 4-1899. Instance Table

Instance Name	Physical Address
LIN0	5240 0090h
LIN1	5240 1090h
LIN2	5240 2090h
LIN3	5240 3090h
LIN4	5240 4090h

Figure 4-713. IODFTCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BERRENA	PBERRENA	CERRENA	ISFERRENA	RESERVED_4	FERRENA	PERRENA	BRKDTERRENA	RESERVED_3			PINSAMPLEMASK		TXSHIFT		
RW	RW	RW	RW	RO	RW	RW	RW	RW			RW		RW		
0	0	0	0	0	0	0	0	0			0		0		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_2				IODFTENA				RESERVED_1						LPBENA	RXPENA
RO				RW/P				RO						RW/P	RW/P
0				101				0						0	0

Access Types Legend

Table 4-1900. IODFTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BERRENA	RW	0h	Bit Errror Enable bit.[[br]]This bit is effective in LIN mode only. This bit is used to create a Bit error. When this bit is set, the bit received is ORed with 1 and passed to the Bit monitor circuitry.
30	PBERRENA	RW	0h	Physical Bus Error Enable bit.[[br]]This bit is effective in LIN mode only. This bit is used to create a Physical Bus Error. When this bit is set, the bit received during Sync Break field transmission is ORed with 1 and passed to the Bit monitor circuitry
29	CERRENA	RW	0h	Checksum Error Enable bit.[[br]]This bit is effective in LIN mode only. This bit is used to create a checksum error. When this bit is set, the polarity of the CTYPE (checksum type) in the receive checksum calculator is changed so that a checksum error is generated.
28	ISFERRENA	RW	0h	Inconsistent Sync Field Error Enable bit.[[br]]This bit is effective in LIN mode only. This bit is used to create an ISF error. When this bit is set, the bit widths in the sync field are varied so that the ISF check fails and the error flag is set.
27	RESERVED_4	RO	0h	Reserved
26	FERRENA	RW	0h	This bit is used to create a Frame Error.[[br]]This bit is effective in SCI-compatible mode only. When this bit is set, the stop bit received is ANDed with '0' and passed to the stop bit check circuitry.
25	PERRENA	RW	0h	Compatible Mode only[[br]]This bit is effective in SCI-compatible mode only. This bit is used to create a Parity Error. When this bit is set, in compatible mode, the parity bit received is toggled so that a parity error occurs.

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Table 4-1900. IODFTCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	BRKDTERRENA	RW	0h	Compatible Mode only[[br]]This bit is effective in SCI-compatible mode only. This bit is used to create BRKDT error (SCI mode only). When this bit is set, the stop bit of the frame is ANDed with '0' and passed to the RSM so that a frame error occurs. Then the RX Pin is forced to continuous low for 10 Tbits so that a BRKDT error occurs.
23 - 21	RESERVED_3	RW	0h	Reserved
20 - 19	PINSAMPLEMASK	RW	0h	Pin sample mask.[[br]]These bits define the sample number at which the TX Pin value that is being transmitted will be inverted to verify the receive pin samples correctly with the majority detection circuitry.[[br]]Note: During IODFT mode testing for the pin sample mask, the prescalar P must be programmed to be greater than 2. 0x0 | PINSAMPLEMASK_NONo Mask 0x1 | PINSAMPLEMASK_TBITInvert the TX Pin value at TBIT_CENTER 0x2 | PINSAMPLEMASK_SCLKInvert the TX Pin value at TBIT_CENTER + SCLK 0x3 | PINSAMPLEMASK_2SCLKInvert the TX Pin value at TBIT_CENTER + 2 SCLK
18 - 16	TXSHIFT	RW	0h	Transmit shift.[[br]]These bits define the delay by which the value on LINTX is delayed so that the value on LINRX is asynchronous. (Not applicable to Start Bit) 0x0 | TXSHIFT_DELAY_0No Delay 0x1 | TXSHIFT_DELAY_1Delay by 1 SCLK 0x2 | TXSHIFT_DELAY_2Delay by 2 SCLK 0x3 | TXSHIFT_DELAY_3Delay by 3 SCLK 0x4 | TXSHIFT_DELAY_4Delay by 4 SCLK 0x5 | TXSHIFT_DELAY_5Delay by 5 SCLK 0x6 | TXSHIFT_DELAY_6Delay by 6 SCLK 0x7 | TXSHIFT_DELAY_7Delay by 7 SCLK
15 - 12	RESERVED_2	RO	0h	Reserved
11 - 8	IODFTENA	RW/P	65h	IO DFT Enable Key[[br]]This field is used to enable the IODFT mode of the SCI/LIN module for testing. 0x0 | IODFTENA_DISABLE_0IODFT is disabled 0x1 | IODFTENA_DISABLE_1IODFT is disabled 0x2 | IODFTENA_DISABLE_2IODFT is disabled 0x3 | IODFTENA_DISABLE_3IODFT is disabled 0x4 | IODFTENA_DISABLE_4IODFT is disabled 0x5 | IODFTENA_DISABLE_5IODFT is disabled 0x6 | IODFTENA_DISABLE_6IODFT is disabled 0x7 | IODFTENA_DISABLE_7IODFT is disabled 0x8 | IODFTENA_DISABLE_8IODFT is disabled 0x9 | IODFTENA_DISABLE_9IODFT is disabled 0xA | IODFTENA_DISABLE_10IODFT is enabled 0xB | IODFTENA_DISABLE_11IODFT is disabled 0xC | IODFTENA_DISABLE_12IODFT is disabled 0xD | IODFTENA_DISABLE_13IODFT is disabled 0xE | IODFTENA_DISABLE_14IODFT is disabled 0xF | IODFTENA_DISABLE_15IODFT is disabled
7 - 2	RESERVED_1	RO	0h	Reserved
1	LPBENA	RW/P	0h	Module loopback enable.[[br]]In analog loopback mode the complete communication path through the I/Os can be tested, whereas in digital loopback mode the I/O buffers are excluded from this path. 0 | LPBENA_DIGITALDigital loopback is enabled. 1 | LPBENA_ANALOGAnalog loopback is enabled in module I/O DFT mode (when IODFTENA = 1010)
0	RXPENA	RW/P	0h	Module Analog loopback through receive pin enable.[[br]]This bit defines whether the I/O buffers for the transmit or the receive pin are included in the communication path in analog loopback mode only. 0 | RXPENA_TRANSMITAnalog loopback through the transmit pin is enabled. 1 | RXPENA_RECEIVEAnalog loopback through the receive pin is enabled.

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4.19.35 MSS_LINn_LIN_GLB_INT_EN Registers

4.19.35.1 LINn_GLB_INT_EN Register (Offset = E0h) [reset = h]

Short Description: The LIN_GLB_INT_EN register is used to enable the INT0 and INT1 interrupt lines to propagate to the PIE block.

Long Description:

Return to Summary Table

Table 4-1901. Instance Table

Instance Name	Physical Address
LIN0	5240 00E0h
LIN1	5240 10E0h
LIN2	5240 20E0h
LIN3	5240 30E0h
LIN4	5240 40E0h

Figure 4-714. LIN_GLB_INT_EN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1														GLBINT1_EN	GLBINT0_EN
RO														RW	RW
0														0	0

Access Types Legend

Table 4-1902. LIN_GLB_INT_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED_1	RO	0h	Reserved
1	GLBINT1_EN	RW	0h	Global Interrupt Enable for LIN INT1.[[br]]This bit determines whether the INT1 interrupt line generates an interrupt to the PIE or not 0 | GLBINT1_DISABLEDLIN INT1 line does not generate an interrupt to the PIE. 1 | GLBINT1_ENABLEDLIN INT1 line generates an interrupt to the PIE if an enabled interrupt condition occurs.
0	GLBINT0_EN	RW	0h	Global Interrupt Enable for LIN INT0.[[br]]This bit determines whether the INT0 interrupt line generates an interrupt to the PIE or not. 0 | GLBINT0_DISABLEDLIN INT0 line does not generate an interrupt to the PIE. 1 | GLBINT0_ENABLEDLIN INT0 line generates an interrupt to the PIE if an enabled interrupt condition occurs.

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4.19.36 MSS_LINn_GLB_INT_FLAG Registers

4.19.36.1 LINn_LIN_GLB_INT_FLG Register (Offset = E4h) [reset = h]

Short Description: The LIN_GLB_INT_FLG register contains the current status of the INT0 and the INT1 flags.

Long Description:

Return to Summary Table

Table 4-1903. Instance Table

Instance Name	Physical Address
LIN0	5240 00E4h
LIN1	5240 10E4h
LIN2	5240 20E4h
LIN3	5240 30E4h
LIN4	5240 40E4h

Figure 4-715. LIN_GLB_INT_FLG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1														INT1_FLG	INT0_FLG
RO														RO	RO
0														0	0

Access Types Legend

Table 4-1904. LIN_GLB_INT_FLG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED_1	RO	0h	Reserved
1	INT1_FLG	RO	0h	Global Interrupt Flag for LIN INT1.[[br]]This bit indicates if an interrupt was generated to the PIE due to an enabled interrupt on the INT1 interrupt line. Refer to the LIN Interrupt Status Register for the condition that generated the interrupt.[[br]]This bit can be cleared by writing a 1 to the corresponding bit in the LIN_GLB_INT_CLR register. Read0 | INT1_FLG_NOT_GENERATEDNo interrupt is active on the INT1 line. Read1 | INT1_FLG_GENERATEDAn interrupt was generated due to an enabled interrupt on the INT1 interrupt line.
0	INT0_FLG	RO	0h	Global Interrupt Flag for LIN INT0.[[br]]This bit indicates if an interrupt was generated to the PIE due to an enabled interrupt on the INT0 interrupt line. Refer to the LIN Interrupt Status Register for the condition that generated the interrupt.[[br]]This bit can be cleared by writing a 1 to the corresponding bit in the LIN_GLB_INT_CLR register. Read0 | INT0_FLG_NOT_GENERATEDNo interrupt is active on the INT0 line. Read1 | INT0_FLG_GENERATEDAn interrupt was generated due to an enabled interrupt on the INT0 interrupt line.

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4.19.37 MSS_LINn_GLB_INT_CLR Registers

4.19.37.1 LINn_GLB_INT_CLR Register (Offset = E8h) [reset = h]

Short Description: The LIN_GLB_INT_CLR register is used to clear the interrupt flags in the LIN_GLB_INT_FLG register.

Long Description:

Return to Summary Table

Table 4-1905. Instance Table

Instance Name	Physical Address
LIN0	5240 00E8h
LIN1	5240 10E8h
LIN2	5240 20E8h
LIN3	5240 30E8h
LIN4	5240 40E8h

Figure 4-716. LIN_GLB_INT_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_1														INT1_FLG_CLR	INT0_FLG_CLR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-1906. LIN_GLB_INT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED_1	RO	0h	Reserved
1	INT1_FLG_CLR	RW	0h	Global Interrupt flag clear for LIN INT1.[[br]]This bit is used to clear the corresponding bit in the LIN_GLB_INT_FLG register. Write 1 to clear the INT1_FLG bit. Writing 0 has no effect.
0	INT0_FLG_CLR	RW	0h	Global Interrupt flag clear for LIN INT0.[[br]]This bit is used to clear the corresponding bit in the LIN_GLB_INT_FLG register. Write 1 to clear the INT0_FLG bit. Writing 0 has no effect.

4.19.38 Access Table

Table 4-1907. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
RW/P	RW/P	Read / Write (Privilege Only)

4.20 MBOX Registers

Table 4-1908. MSS_MBOX Registers Base Address Table

Offset	Length	Acronym	MSS_MBOX Physical Address
0h	32	MBOX_START	7200 0000h

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Table 4-1908. MSS_MBOX Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_MBOX Physical Address
3FFCh	32	MBOX_END	7200 3FFCh

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4.20.1 MSS_MBOX_START Registers

4.20.1.1 MBOX_START Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 4-1909. Instance Table

Instance Name	Physical Address
MBOX_SRAM	7200 0000h

Access Types Legend

Table 4-1910. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	L2 Memory start address

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4.20.2 MSS_MBOX_END Registers

4.20.2.1 MBOX_END Register (Offset = 3FFCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 4-1911. Instance Table

Instance Name	Physical Address
MBOX_SRAM	7200 3FFCh

Access Types Legend

Table 4-1912. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	END	RW	0h	L2 Memory end address

4.20.3 Access Table

Table 4-1913. Access Type Codes

Access Type	Code	Description
RW	RW	Read / Write

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4.21 MCAN_CFG Registers

Table 4-1914. MSS_MCAN[0:2]_CFG Registers Base Address Table

Offset	Length	Acronym	MSS_MCAN0_CFG Physical Address	MSS_MCAN1_CFG Physical Address	MSS_MCAN2_CFG Physical Address
0h	32	MCAN_CFG_SS_PID	5260 8000h	5261 8000h	5262 8000h
4h	32	MCAN_CFG_SS_CTRL	5260 8004h	5261 8004h	5262 8004h
8h	32	MCAN_CFG_SS_STAT	5260 8008h	5261 8008h	5262 8008h
Ch	32	MCAN_CFG_SS_ICS	5260 800Ch	5261 800Ch	5262 800Ch
10h	32	MCAN_CFG_SS_IRS	5260 8010h	5261 8010h	5262 8010h
14h	32	MCAN_CFG_SS_IECS	5260 8014h	5261 8014h	5262 8014h
18h	32	MCAN_CFG_SS_IE	5260 8018h	5261 8018h	5262 8018h
1Ch	32	MCAN_CFG_SS_IES	5260 801Ch	5261 801Ch	5262 801Ch
20h	32	MCAN_CFG_SS_EOI	5260 8020h	5261 8020h	5262 8020h
24h	32	MCAN_CFG_SS_EXT_TS_PS	5260 8024h	5261 8024h	5262 8024h
28h	32	MCAN_CFG_SS_EXT_TS_USIC	5260 8028h	5261 8028h	5262 8028h
200h	32	MCAN_CFG_CREL	5260 8200h	5261 8200h	5262 8200h
204h	32	MCAN_CFG_ENDN	5260 8204h	5261 8204h	5262 8204h
208h	32	MCAN_CFG_CUST	5260 8208h	5261 8208h	5262 8208h
20Ch	32	MCAN_CFG_DBTP	5260 820Ch	5261 820Ch	5262 820Ch
210h	32	MCAN_CFG_TEST	5260 8210h	5261 8210h	5262 8210h
214h	32	MCAN_CFG_RWD	5260 8214h	5261 8214h	5262 8214h
218h	32	MCAN_CFG_CCCR	5260 8218h	5261 8218h	5262 8218h
21Ch	32	MCAN_CFG_NBTP	5260 821Ch	5261 821Ch	5262 821Ch
220h	32	MCAN_CFG_TSCC	5260 8220h	5261 8220h	5262 8220h
224h	32	MCAN_CFG_TSCV	5260 8224h	5261 8224h	5262 8224h
228h	32	MCAN_CFG_TOCC	5260 8228h	5261 8228h	5262 8228h
22Ch	32	MCAN_CFG_TOCV	5260 822Ch	5261 822Ch	5262 822Ch
230h	32	MCAN_CFG_RES00	5260 8230h	5261 8230h	5262 8230h
234h	32	MCAN_CFG_RES01	5260 8234h	5261 8234h	5262 8234h
238h	32	MCAN_CFG_RES02	5260 8238h	5261 8238h	5262 8238h
23Ch	32	MCAN_CFG_RES03	5260 823Ch	5261 823Ch	5262 823Ch
240h	32	MCAN_CFG_ECR	5260 8240h	5261 8240h	5262 8240h
244h	32	MCAN_CFG_PSR	5260 8244h	5261 8244h	5262 8244h
248h	32	MCAN_CFG_TDCR	5260 8248h	5261 8248h	5262 8248h
24Ch	32	MCAN_CFG_RES04	5260 824Ch	5261 824Ch	5262 824Ch
250h	32	MCAN_CFG_IR	5260 8250h	5261 8250h	5262 8250h
254h	32	MCAN_CFG_IE	5260 8254h	5261 8254h	5262 8254h
258h	32	MCAN_CFG_ILS	5260 8258h	5261 8258h	5262 8258h
25Ch	32	MCAN_CFG_ILE	5260 825Ch	5261 825Ch	5262 825Ch
260h	32	MCAN_CFG_RES05	5260 8260h	5261 8260h	5262 8260h
264h	32	MCAN_CFG_RES06	5260 8264h	5261 8264h	5262 8264h
268h	32	MCAN_CFG_RES07	5260 8268h	5261 8268h	5262 8268h
26Ch	32	MCAN_CFG_RES08	5260 826Ch	5261 826Ch	5262 826Ch
270h	32	MCAN_CFG_RES09	5260 8270h	5261 8270h	5262 8270h
274h	32	MCAN_CFG_RES10	5260 8274h	5261 8274h	5262 8274h
278h	32	MCAN_CFG_RES11	5260 8278h	5261 8278h	5262 8278h
27Ch	32	MCAN_CFG_RES12	5260 827Ch	5261 827Ch	5262 827Ch
280h	32	MCAN_CFG_GFC	5260 8280h	5261 8280h	5262 8280h

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Table 4-1914. MSS_MCAN[0:2]_CFG Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_MCAN0_CFG Physical Address	MSS_MCAN1_CFG Physical Address	MSS_MCAN2_CFG Physical Address
284h	32	MCAN_CFG_SIDFC	5260 8284h	5261 8284h	5262 8284h
288h	32	MCAN_CFG_XIDFC	5260 8288h	5261 8288h	5262 8288h
28Ch	32	MCAN_CFG_RES13	5260 828Ch	5261 828Ch	5262 828Ch
290h	32	MCAN_CFG_XIDAM	5260 8290h	5261 8290h	5262 8290h
294h	32	MCAN_CFG_HPMS	5260 8294h	5261 8294h	5262 8294h
298h	32	MCAN_CFG_NDAT1	5260 8298h	5261 8298h	5262 8298h
29Ch	32	MCAN_CFG_NDAT2	5260 829Ch	5261 829Ch	5262 829Ch
2A0h	32	MCAN_CFG_RXF0C	5260 82A0h	5261 82A0h	5262 82A0h
2A4h	32	MCAN_CFG_RXF0S	5260 82A4h	5261 82A4h	5262 82A4h
2A8h	32	MCAN_CFG_RXF0A	5260 82A8h	5261 82A8h	5262 82A8h
2ACh	32	MCAN_CFG_RXBC	5260 82ACh	5261 82ACh	5262 82ACh
2B0h	32	MCAN_CFG_RXF1C	5260 82B0h	5261 82B0h	5262 82B0h
2B4h	32	MCAN_CFG_RXF1S	5260 82B4h	5261 82B4h	5262 82B4h
2B8h	32	MCAN_CFG_RXF1A	5260 82B8h	5261 82B8h	5262 82B8h
2BCh	32	MCAN_CFG_RXESC	5260 82BCh	5261 82BCh	5262 82BCh
2C0h	32	MCAN_CFG_TXBC	5260 82C0h	5261 82C0h	5262 82C0h
2C4h	32	MCAN_CFG_TXFQS	5260 82C4h	5261 82C4h	5262 82C4h
2C8h	32	MCAN_CFG_TXESC	5260 82C8h	5261 82C8h	5262 82C8h
2CCh	32	MCAN_CFG_TXBRP	5260 82CCh	5261 82CCh	5262 82CCh
2D0h	32	MCAN_CFG_TXBAR	5260 82D0h	5261 82D0h	5262 82D0h
2D4h	32	MCAN_CFG_TXBCR	5260 82D4h	5261 82D4h	5262 82D4h
2D8h	32	MCAN_CFG_TXBTO	5260 82D8h	5261 82D8h	5262 82D8h
2DCh	32	MCAN_CFG_TXBCF	5260 82DCh	5261 82DCh	5262 82DCh
2E0h	32	MCAN_CFG_TXBTIE	5260 82E0h	5261 82E0h	5262 82E0h
2E4h	32	MCAN_CFG_TXBCIE	5260 82E4h	5261 82E4h	5262 82E4h
2E8h	32	MCAN_CFG_RES14	5260 82E8h	5261 82E8h	5262 82E8h
2ECh	32	MCAN_CFG_RES15	5260 82ECh	5261 82ECh	5262 82ECh
2F0h	32	MCAN_CFG_TXEFC	5260 82F0h	5261 82F0h	5262 82F0h
2F4h	32	MCAN_CFG_TXEFS	5260 82F4h	5261 82F4h	5262 82F4h
2F8h	32	MCAN_CFG_TXEFA	5260 82F8h	5261 82F8h	5262 82F8h
2FCh	32	MCAN_CFG_RES16	5260 82FCh	5261 82FCh	5262 82FCh

Table 4-1915. MSS_MCAN3_CFG Registers Base Address Table

Offset	Length	Acronym	MSS_MCAN3_CFG Physical Address
0h	32	MCAN_CFG_SS_PID	5263 8000h
4h	32	MCAN_CFG_SS_CTRL	5263 8004h
8h	32	MCAN_CFG_SS_STAT	5263 8008h
Ch	32	MCAN_CFG_SS_ICS	5263 800Ch
10h	32	MCAN_CFG_SS_IRS	5263 8010h
14h	32	MCAN_CFG_SS_IECS	5263 8014h
18h	32	MCAN_CFG_SS_IE	5263 8018h
1Ch	32	MCAN_CFG_SS_IES	5263 801Ch
20h	32	MCAN_CFG_SS_EOI	5263 8020h
24h	32	MCAN_CFG_SS_EXT_TS_PS	5263 8024h
28h	32	MCAN_CFG_SS_EXT_TS_USIC	5263 8028h
200h	32	MCAN_CFG_CREL	5263 8200h

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Table 4-1915. MSS_MCAN3_CFG Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_MCAN3_CFG Physical Address
204h	32	MCAN_CFG_ENDN	5263 8204h
208h	32	MCAN_CFG_CUST	5263 8208h
20Ch	32	MCAN_CFG_DBTP	5263 820Ch
210h	32	MCAN_CFG_TEST	5263 8210h
214h	32	MCAN_CFG_RWD	5263 8214h
218h	32	MCAN_CFG_CCCR	5263 8218h
21Ch	32	MCAN_CFG_NBTP	5263 821Ch
220h	32	MCAN_CFG_TSCC	5263 8220h
224h	32	MCAN_CFG_TSCV	5263 8224h
228h	32	MCAN_CFG_TOCC	5263 8228h
22Ch	32	MCAN_CFG_TOCV	5263 822Ch
230h	32	MCAN_CFG_RES00	5263 8230h
234h	32	MCAN_CFG_RES01	5263 8234h
238h	32	MCAN_CFG_RES02	5263 8238h
23Ch	32	MCAN_CFG_RES03	5263 823Ch
240h	32	MCAN_CFG_ECR	5263 8240h
244h	32	MCAN_CFG_PSR	5263 8244h
248h	32	MCAN_CFG_TDCR	5263 8248h
24Ch	32	MCAN_CFG_RES04	5263 824Ch
250h	32	MCAN_CFG_IR	5263 8250h
254h	32	MCAN_CFG_IE	5263 8254h
258h	32	MCAN_CFG_ILS	5263 8258h
25Ch	32	MCAN_CFG_ILE	5263 825Ch
260h	32	MCAN_CFG_RES05	5263 8260h
264h	32	MCAN_CFG_RES06	5263 8264h
268h	32	MCAN_CFG_RES07	5263 8268h
26Ch	32	MCAN_CFG_RES08	5263 826Ch
270h	32	MCAN_CFG_RES09	5263 8270h
274h	32	MCAN_CFG_RES10	5263 8274h
278h	32	MCAN_CFG_RES11	5263 8278h
27Ch	32	MCAN_CFG_RES12	5263 827Ch
280h	32	MCAN_CFG_GFC	5263 8280h
284h	32	MCAN_CFG_SIDFC	5263 8284h
288h	32	MCAN_CFG_XIDFC	5263 8288h
28Ch	32	MCAN_CFG_RES13	5263 828Ch
290h	32	MCAN_CFG_XIDAM	5263 8290h
294h	32	MCAN_CFG_HPMS	5263 8294h
298h	32	MCAN_CFG_NDAT1	5263 8298h
29Ch	32	MCAN_CFG_NDAT2	5263 829Ch
2A0h	32	MCAN_CFG_RXF0C	5263 82A0h
2A4h	32	MCAN_CFG_RXF0S	5263 82A4h
2A8h	32	MCAN_CFG_RXF0A	5263 82A8h
2ACh	32	MCAN_CFG_RXBC	5263 82ACh
2B0h	32	MCAN_CFG_RXF1C	5263 82B0h
2B4h	32	MCAN_CFG_RXF1S	5263 82B4h
2B8h	32	MCAN_CFG_RXF1A	5263 82B8h
2BCh	32	MCAN_CFG_RXESC	5263 82BCh

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Table 4-1915. MSS_MCAN3_CFG Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_MCAN3_CFG Physical Address
2C0h	32	MCAN_CFG_TXBC	5263 82C0h
2C4h	32	MCAN_CFG_TXFQS	5263 82C4h
2C8h	32	MCAN_CFG_TXESC	5263 82C8h
2CCh	32	MCAN_CFG_TXBRP	5263 82CCh
2D0h	32	MCAN_CFG_TXBAR	5263 82D0h
2D4h	32	MCAN_CFG_TXBCR	5263 82D4h
2D8h	32	MCAN_CFG_TXBTO	5263 82D8h
2DCh	32	MCAN_CFG_TXBCF	5263 82DCh
2E0h	32	MCAN_CFG_TXBTIE	5263 82E0h
2E4h	32	MCAN_CFG_TXBCIE	5263 82E4h
2E8h	32	MCAN_CFG_RES14	5263 82E8h
2ECh	32	MCAN_CFG_RES15	5263 82ECh
2F0h	32	MCAN_CFG_TXEFC	5263 82F0h
2F4h	32	MCAN_CFG_TXEFS	5263 82F4h
2F8h	32	MCAN_CFG_TXEFA	5263 82F8h
2FCh	32	MCAN_CFG_RES16	5263 82FCh

4.21.1 MCAN_CFG Instance Count Note

Note

n = 0 to 3 for the MCAN_CFG registers defined below.

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4.21.2 MSS_MCANn_CFG_SS_PID Registers

4.21.2.1 MCANn_CFG_SS_PID Register (Offset = 0h) [reset = h]

Short Description: SS_PID

Long Description:

Return to Summary Table

Table 4-1916. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8000h
MCAN1_CFG	5261 8000h
MCAN2_CFG	5262 8000h
MCAN3_CFG	5263 8000h

Figure 4-717. SS_PID Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		100011100000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
RO					RO			RO		RO					
1011					1			0		1					

Access Types Legend

Table 4-1917. SS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID register scheme
29 - 28	BU	RO	Ah	Business Unit: 10 = Processors
27 - 16	MODULE_ID	RO	1749204760h	Module ID
15 - 11	RTL	RO	3F3h	RTL revision. Will vary depending on release.
10 - 8	MAJOR	RO	1h	Major revision
7 - 6	CUSTOM	RO	0h	Custom
5 - 0	MINOR	RO	1h	Minor revision

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4.21.3 MSS_MCANn_CFG_SS_CTRL Registers

4.21.3.1 MCANn_CFG_SS_CTRL Register (Offset = 4h) [reset = h]

Short Description: SS_CTRL

Long Description:

Return to Summary Table

Table 4-1918. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8004h
MCAN1_CFG	5261 8004h
MCAN2_CFG	5262 8004h
MCAN3_CFG	5263 8004h

Figure 4-718. SS_CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU0															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU0									EXT_TS_CNTR_EN	AUTOWAKEUP	WAKEUPREGEN	DBGSUSP_FREE	NU		
RO									RW	RW	RW	RW	RO		
0									0	0	0	1	0		

Access Types Legend

Table 4-1919. SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	NU0	RO	0h	Reserved
6	EXT_TS_CNTR_EN	RW	0h	External TimeStamp Counter Enable
5	AUTOWAKEUP	RW	0h	Automatic Wakeup Enable
4	WAKEUPREGEN	RW	0h	Wakeup Request Enable
3	DBGSUSP_FREE	RW	1h	0-Honor Debug Suspend, 1-Disregard debug suspend
2 - 0	NU	RO	0h	Reserved

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4.21.4 MSS_MCANn_CFG_SS_STAT Registers

4.21.4.1 MCANn_CFG_SS_STAT Register (Offset = 8h) [reset = h]

Short Description: SS_STAT

Long Description:

Return to Summary Table

Table 4-1920. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8008h
MCAN1_CFG	5261 8008h
MCAN2_CFG	5262 8008h
MCAN3_CFG	5263 8008h

Figure 4-719. SS_STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU1															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU1													EN_FDOE	MMI_DONE	NU
RO													RO	RO	RO
0													1	1	0

Access Types Legend

Table 4-1921. SS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	NU1	RO	0h	Reserved
2	EN_FDOE	RO	1h	Reflects the value of mcanss_enable_fdoe configuration portx=mcanss_enable_fdoe
1	MMI_DONE	RO	1h	0:Memory Initialization is in progress, 1:Memory Intialization Done
0	NU	RO	0h	Reserved

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4.21.5 MSS_MCANn_CFG_SS_ICS Registers

4.21.5.1 MCANn_CFG_SS_ICS Register (Offset = Ch) [reset = h]

Short Description: SS_ICS

Long Description:

Return to Summary Table

Table 4-1922. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 800Ch
MCAN1_CFG	5261 800Ch
MCAN2_CFG	5262 800Ch
MCAN3_CFG	5263 800Ch

Figure 4-720. SS_ICS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU2															ICS
RO															WO
0															0

Access Types Legend

Table 4-1923. SS_ICS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU2	RO	0h	Reserved
0	ICS	WO	0h	This bit contains the External TimeStamp Counter Overflow Interrupt status. Write '1' to clear bits. (ICS - Interrupt Clear Shadow Register)

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4.21.6 MSS_MCANn_CFG_SS_IRS Registers

4.21.6.1 MCANn_CFG_SS_IRS Register (Offset = 10h) [reset = h]

Short Description: SS_IRS

Long Description:

Return to Summary Table

Table 4-1924. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8010h
MCAN1_CFG	5261 8010h
MCAN2_CFG	5262 8010h
MCAN3_CFG	5263 8010h

Figure 4-721. SS_IRS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU3															IRS
RO															RO
0															0

Access Types Legend

Table 4-1925. SS_IRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU3	RO	0h	Reserved
0	IRS	RO	0h	External TimeStamp Counter Overflow Interrupt status. Read raw interrupt status. (IRS - Interrupt Raw Status Register)

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4.21.7 MSS_MCANn_CFG_SS_IECS Registers

4.21.7.1 MCANn_CFG_SS_IECS Register (Offset = 14h) [reset = h]

Short Description: SS_IECS

Long Description:

Return to Summary Table

Table 4-1926. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8014h
MCAN1_CFG	5261 8014h
MCAN2_CFG	5262 8014h
MCAN3_CFG	5263 8014h

Figure 4-722. SS_IECS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU4															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU4															IECS
RO															WO
0															0

Access Types Legend

Table 4-1927. SS_IECS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU4	RO	0h	Reserved
0	IECS	WO	0h	External TimeStamp Counter Overflow Interrupt. Write '1' to clear bits. (IECS - Interrupt Enable Clear Shadow Register)

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4.21.8 MSS_MCANn_CFG_SS_IE Registers

4.21.8.1 MCANn_CFG_SS_IE Register (Offset = 18h) [reset = h]

Short Description: SS_IE

Long Description:

Return to Summary Table

Table 4-1928. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8018h
MCAN1_CFG	5261 8018h
MCAN2_CFG	5262 8018h
MCAN3_CFG	5263 8018h

Figure 4-723. SS_IE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU5															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU5															IE
RO															RW
0															0

Access Types Legend

Table 4-1929. SS_IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU5	RO	0h	Reserved
0	IE	RW	0h	External TimeStamp Counter Overflow Interrupt. Write '1' to set interrupt enable. Read returns interrupt enable. (IE - Interrupt Enable Register)

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4.21.9 MSS_MCANn_CFG_SS_IES Registers

4.21.9.1 MCANn_CFG_SS_IES Register (Offset = 1Ch) [reset = h]

Short Description: SS_IES

Long Description:

Return to Summary Table

Table 4-1930. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 801Ch
MCAN1_CFG	5261 801Ch
MCAN2_CFG	5262 801Ch
MCAN3_CFG	5263 801Ch

Figure 4-724. SS_IES Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6															IES
RO															RO
0															0

Access Types Legend

Table 4-1931. SS_IES Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU6	RO	0h	Reserved
0	IES	RO	0h	External TimeStamp Counter Overflow Interrupt. Read Enabled Interrupts. (IES - Interrupt Enable Status)

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4.21.10 MSS_MCANn_CFG_SS_EOI Registers

4.21.10.1 MCANn_CFG_SS_EOI Register (Offset = 20h) [reset = h]

Short Description: SS_EOI

Long Description:

Return to Summary Table

Table 4-1932. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8020h
MCAN1_CFG	5261 8020h
MCAN2_CFG	5262 8020h
MCAN3_CFG	5263 8020h

Figure 4-725. SS_EOI Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7								EOI							
RO								WO							
0								0							

Access Types Legend

Table 4-1933. SS_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU7	RO	0h	Reserved
7 - 0	EOI	WO	0h	Write with bit position of targeted interrupt. (E.g. Ext TS is bit 0).Upon write, level interrupt will clear and if unserviced interrupt counter > 1 will issue another pulse interrupt. Field values: ext_ts_eoi(0): EOI value for External TS interrupt mcan_0_eoi(1): EOI value for mcan[0] interrupt mcan_1_eoi(2): EOI value for mcan[1] interrupt(EOI - End Of Interrupt)

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4.21.11 MSS_MCANn_CFG_SS_EXT_TS_PS Registers

4.21.11.1 MCANn_CFG_SS_EXT_TS_PS Register (Offset = 24h) [reset = h]

Short Description: SS_EXT_TS_PS

Long Description:

Return to Summary Table

Table 4-1934. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8024h
MCAN1_CFG	5261 8024h
MCAN2_CFG	5262 8024h
MCAN3_CFG	5263 8024h

Figure 4-726. SS_EXT_TS_PS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8								PRESCALE							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRESCALE															
RW															
0															

Access Types Legend

Table 4-1935. SS_EXT_TS_PS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU8	RO	0h	Reserved
23 - 0	PRESCALE	RW	0h	External Timestamp Prescaler reload value.External Timestamp count rate is host clock rate divided by this valuewith one exception: a value of 0 has the same effect as 1 .

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4.21.12 MSS_MCANn_CFG_SS_EXT_TS_USIC Registers

4.21.12.1 MCANn_CFG_SS_EXT_TS_USIC Register (Offset = 28h) [reset = h]

Short Description: SS_EXT_TS_USIC

Long Description:

Return to Summary Table

Table 4-1936. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8028h
MCAN1_CFG	5261 8028h
MCAN2_CFG	5262 8028h
MCAN3_CFG	5263 8028h

Figure 4-727. SS_EXT_TS_USIC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU9															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU9											EXT_TS_INTR_CNTR				
RO											RO				
0											0				

Access Types Legend

Table 4-1937. SS_EXT_TS_USIC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 5	NU9	RO	0h	Reserved
4 - 0	EXT_TS_INTR_CNTR	RO	0h	Number of unserviced rollover interrupts. If >1 an EOI write will issue another pulse interrupt (EXT_TS_USIC - External TImeStamp Unserviced Interrupts Counter)

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4.21.13 MSS_MCANn_CFG_CREL Registers

4.21.13.1 MCANn_CFG_CREL Register (Offset = 200h) [reset = h]

Short Description: CREL

Long Description:

Return to Summary Table

Table 4-1938. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8200h
MCAN1_CFG	5261 8200h
MCAN2_CFG	5262 8200h
MCAN3_CFG	5263 8200h

Figure 4-728. CREL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REL				STEP				SUBSTEP				YEAR			
RO				RO				RO				RO			
11				10				11				1000			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MON								DAY							
RO								RO							
110								1000							

Access Types Legend

Table 4-1939. CREL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 28	REL	RO	Bh	Core Release
27 - 24	STEP	RO	Ah	Step of Core Release
23 - 20	SUBSTEP	RO	Bh	Sub-Step of Core Release
19 - 16	YEAR	RO	3E8h	Time Stamp Year
15 - 8	MON	RO	6Eh	Time Stamp Month
7 - 0	DAY	RO	3E8h	Time Stamp Day

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4.21.14 MSS_MCANn_CFG_ENDN Registers

4.21.14.1 MCANn_CFG_ENDN Register (Offset = 204h) [reset = h]

Short Description: ENDN

Long Description:

Return to Summary Table

Table 4-1940. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8204h
MCAN1_CFG	5261 8204h
MCAN2_CFG	5262 8204h
MCAN3_CFG	5263 8204h

Figure 4-729. ENDN Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ETV															
RO															
10000111011001010100001100100001															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETV															
RO															
10000111011001010100001100100001															

Access Types Legend

Table 4-1941. ENDN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ETV	RO	7E3819F3A 12CEB3649 491171A1h	Endianess test value

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4.21.15 MSS_MCANn_CFG_CUST Registers

4.21.15.1 MCANn_CFG_CUST Register (Offset = 208h) [reset = h]

Short Description: CUST

Long Description:

Return to Summary Table

Table 4-1942. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8208h
MCAN1_CFG	5261 8208h
MCAN2_CFG	5262 8208h
MCAN3_CFG	5263 8208h

Figure 4-730. CUST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CUST															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CUST															
RO															
0															

Access Types Legend

Table 4-1943. CUST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CUST	RO	0h	Custom

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4.21.16 MSS_MCANn_CFG_DBTP Registers

4.21.16.1 MCANn_CFG_DBTP Register (Offset = 20Ch) [reset = h]

Short Description: DBTP

Long Description:

Return to Summary Table

Table 4-1944. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 820Ch
MCAN1_CFG	5261 820Ch
MCAN2_CFG	5262 820Ch
MCAN3_CFG	5263 820Ch

Figure 4-731. DBTP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU13								TDC	NU12		DBRP				
RO								RW	RO		RW				
0								0	0		0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU11			DTSEG1					DTSEG2			DSJW				
RO			RW					RW			RW				
0			1010					11			11				

Access Types Legend

Table 4-1945. DBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU13	RO	0h	Reserved
23	TDC	RW	0h	Transmitter Delay Compensation
22 - 21	NU12	RO	0h	Reserved
20 - 16	DBRP	RW	0h	Data Baud Rate Prescaler
15 - 13	NU11	RO	0h	Reserved
12 - 8	DTSEG1	RW	3F2h	Data time segment before smaple point
7 - 4	DTSEG2	RW	Bh	Data time segment after sample point
3 - 0	DSJW	RW	Bh	Data resynchronization Jump Width

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4.21.17 MSS_MCANn_CFG_TEST Registers

4.21.17.1 MCANn_CFG_TEST Register (Offset = 210h) [reset = h]

Short Description: TEST

Long Description:

Return to Summary Table

Table 4-1946. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8210h
MCAN1_CFG	5261 8210h
MCAN2_CFG	5262 8210h
MCAN3_CFG	5263 8210h

Figure 4-732. TEST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU15								RX	TX		LBCK	NU14			
RO								RO	RW		RW	RO			
0								0	0		0	0			

Access Types Legend

Table 4-1947. TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	NU15	RO	0h	Reserved
7	RX	RO	0h	Receive Pin
6 - 5	TX	RW	0h	Control of Transmit Pin
4	LBCK	RW	0h	Loop Back Mode
3 - 0	NU14	RO	0h	Reserved

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4.21.18 MSS_MCANn_CFG_RWD Registers

4.21.18.1 MCANn_CFG_RWD Register (Offset = 214h) [reset = h]

Short Description: RWD

Long Description:

Return to Summary Table

Table 4-1948. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8214h
MCAN1_CFG	5261 8214h
MCAN2_CFG	5262 8214h
MCAN3_CFG	5263 8214h

Figure 4-733. RWD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDV								WDC							
RO								RW							
0								0							

Access Types Legend

Table 4-1949. RWD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU16	RO	0h	Reserved
15 - 8	WDV	RO	0h	Watchdog Value
7 - 0	WDC	RW	0h	Watchdog Counter Value

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4.21.19 MSS_MCANn_CFG_CCCR Registers

4.21.19.1 MCANn_CFG_CCCR Register (Offset = 218h) [reset = h]

Short Description: CCCR

Long Description:

Return to Summary Table

Table 4-1950. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8218h
MCAN1_CFG	5261 8218h
MCAN2_CFG	5262 8218h
MCAN3_CFG	5263 8218h

Figure 4-734. CCCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU18															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU18	TXP	EFBI	PXHD	NU17		BRSE	FDOE	TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
RW	RW	RW	RW	RO		RW	RW	RW	RW	RW	RW	RO	RW	RW	RW
0	0	0	0	0		0	0	0	0	0	0	0	0	0	1

Access Types Legend

Table 4-1951. CCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 15	NU18	RW	0h	Reserved
14	TXP	RW	0h	Transmit Pause
13	EFBI	RW	0h	Edge Filtering durign Bus Integration
12	PXHD	RW	0h	Protocol Exception Handling Disable
11 - 10	NU17	RO	0h	Reserved
9	BRSE	RW	0h	Bit Rate Switch Enable
8	FDOE	RW	0h	FD Operation Enable
7	TEST	RW	0h	Test Mode enable
6	DAR	RW	0h	Disable Automatic Regransmission
5	MON	RW	0h	Bus Monitoring Mode
4	CSR	RW	0h	Clock Stop Request
3	CSA	RO	0h	Clock Stop Acknowledge
2	ASM	RW	0h	Restriced Operation Mode
1	CCE	RW	0h	Configuration Change Enable
0	INIT	RW	1h	Initialization

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4.21.20 MSS_MCANn_CFG_NBTP Registers

4.21.20.1 MCANn_CFG_NBTP Register (Offset = 21Ch) [reset = h]

Short Description: NBTP

Long Description:

Return to Summary Table

Table 4-1952. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 821Ch
MCAN1_CFG	5261 821Ch
MCAN2_CFG	5262 821Ch
MCAN3_CFG	5263 821Ch

Figure 4-735. NBTP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NSJW								NBRP							
RW								RW							
11								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NTSEG1								NU19	NTSEG2						
RW								RO	RW						
1010								0	11						

Access Types Legend

Table 4-1953. NBTP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	NSJW	RW	Bh	Nominal Resynchronization Jump Width
24 - 16	NBRP	RW	0h	Nominal Baud Rate Prescaler
15 - 8	NTSEG1	RW	3F2h	Nominal Time segment before sample point
7	NU19	RO	0h	Reserved
6 - 0	NTSEG2	RW	Bh	Nominal Time segment after sample point

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4.21.21 MSS_MCANn_CFG_TSCC Registers

4.21.21.1 MCANn_CFG_TSCC Register (Offset = 220h) [reset = h]

Short Description: TSCC

Long Description:

Return to Summary Table

Table 4-1954. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8220h
MCAN1_CFG	5261 8220h
MCAN2_CFG	5262 8220h
MCAN3_CFG	5263 8220h

Figure 4-736. TSCC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU21												TCP			
RO												RW			
0												0			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU20														TSS	
RO														RW	
0														0	

Access Types Legend

Table 4-1955. TSCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	NU21	RO	0h	Reserved
19 - 16	TCP	RW	0h	Timestamp Counter Prescaler
15 - 2	NU20	RO	0h	Reserved
1 - 0	TSS	RW	0h	Timestamp Select

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4.21.22 MSS_MCANn_CFG_TSCV Registers

4.21.22.1 MCANn_CFG_TSCV Register (Offset = 224h) [reset = h]

Short Description: TSCV

Long Description:

Return to Summary Table

Table 4-1956. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8224h
MCAN1_CFG	5261 8224h
MCAN2_CFG	5262 8224h
MCAN3_CFG	5263 8224h

Figure 4-737. TSCV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU22															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSC															
RW															
0															

Access Types Legend

Table 4-1957. TSCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU22	RO	0h	Reserved
15 - 0	TSC	RW	0h	Timestamp Counter

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4.21.23 MSS_MCANn_CFG_TOCC Registers

4.21.23.1 MCANn_CFG_TOCC Register (Offset = 228h) [reset = h]

Short Description: TOCC

Long Description:

Return to Summary Table

Table 4-1958. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8228h
MCAN1_CFG	5261 8228h
MCAN2_CFG	5262 8228h
MCAN3_CFG	5263 8228h

Figure 4-738. TOCC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOP															
RW															
1111111111111111															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU23													TOS		ETOC
RO													RW		RW
0													0		0

Access Types Legend

Table 4-1959. TOCC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	TOP	RW	3F28CB715 71C7h	Timeout Period
15 - 3	NU23	RO	0h	Reserved
2 - 1	TOS	RW	0h	Timeout Select
0	ETOC	RW	0h	Enable Timeout Counter

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4.21.24 MSS_MCANn_CFG_TOCV Registers

4.21.24.1 MCANn_CFG_TOCV Register (Offset = 22Ch) [reset = h]

Short Description: TOCV

Long Description:

Return to Summary Table

Table 4-1960. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 822Ch
MCAN1_CFG	5261 822Ch
MCAN2_CFG	5262 822Ch
MCAN3_CFG	5263 822Ch

Figure 4-739. TOCV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU24															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOC															
RW															
1111111111111111															

Access Types Legend

Table 4-1961. TOCV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU24	RO	0h	Reserved
15 - 0	TOC	RW	3F28CB715 71C7h	Timeout Counter

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4.21.25 MSS_MCANn_CFG_RES00 Registers

4.21.25.1 MCANn_CFG_RES00 Register (Offset = 230h) [reset = h]

Short Description: RES00

Long Description:

Return to Summary Table

Table 4-1962. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8230h
MCAN1_CFG	5261 8230h
MCAN2_CFG	5262 8230h
MCAN3_CFG	5263 8230h

Figure 4-740. RES00 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES00															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES00															
RO															
0															

Access Types Legend

Table 4-1963. RES00 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES00	RO	0h	Reserved

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4.21.26 MSS_MCANn_CFG_RES01 Registers

4.21.26.1 MCANn_CFG_RES01 Register (Offset = 234h) [reset = h]

Short Description: RES01

Long Description:

Return to Summary Table

Table 4-1964. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8234h
MCAN1_CFG	5261 8234h
MCAN2_CFG	5262 8234h
MCAN3_CFG	5263 8234h

Figure 4-741. RES01 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES01															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES01															
RO															
0															

Access Types Legend

Table 4-1965. RES01 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES01	RO	0h	Reserved

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4.21.27 MSS_MCANn_CFG_RES02 Registers

4.21.27.1 MCANn_CFG_RES02 Register (Offset = 238h) [reset = h]

Short Description: RES02

Long Description:

Return to Summary Table

Table 4-1966. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8238h
MCAN1_CFG	5261 8238h
MCAN2_CFG	5262 8238h
MCAN3_CFG	5263 8238h

Figure 4-742. RES02 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES02															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES02															
RO															
0															

Access Types Legend

Table 4-1967. RES02 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES02	RO	0h	Reserved

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4.21.28 MSS_MCANn_CFG_RES03 Registers

4.21.28.1 MCANn_CFG_RES03 Register (Offset = 23Ch) [reset = h]

Short Description: RES03

Long Description:

Return to Summary Table

Table 4-1968. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 823Ch
MCAN1_CFG	5261 823Ch
MCAN2_CFG	5262 823Ch
MCAN3_CFG	5263 823Ch

Figure 4-743. RES03 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES03															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES03															
RO															
0															

Access Types Legend

Table 4-1969. RES03 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES03	RO	0h	Reserved

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4.21.29 MSS_MCANn_CFG_ECR Registers

4.21.29.1 MCANn_CFG_ECR Register (Offset = 240h) [reset = h]

Short Description: ECR

Long Description:

Return to Summary Table

Table 4-1970. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8240h
MCAN1_CFG	5261 82040h
MCAN2_CFG	5262 8240h
MCAN3_CFG	5263 8240h

Figure 4-744. ECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU25								CEL							
RO								RO							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RP	REC							TEC							
RO	RO							RO							
0	0							0							

Access Types Legend

Table 4-1971. ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU25	RO	0h	Reserved
23 - 16	CEL	RO	0h	CAN Error Logging
15	RP	RO	0h	Recieve Error Passive
14 - 8	REC	RO	0h	Recieve Error Counter
7 - 0	TEC	RO	0h	Transmit Error Counter

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4.21.30 MSS_MCANn_CFG_PSR Registers

4.21.30.1 MCANn_CFG_PSR Register (Offset = 244h) [reset = h]

Short Description: PSR

Long Description:

Return to Summary Table

Table 4-1972. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8244h
MCAN1_CFG	5261 8244h
MCAN2_CFG	5262 8244h
MCAN3_CFG	5263 8244h

Figure 4-745. PSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU27									TDCV						
RO									RO						
0									0						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU26	PXE	RFDF	RBRS	RESI	DLEC			BO	EW	EP	ACT		LEC		
RO	RO	RO	RO	RO	RO			RO	RO	RO	RO		RO		
0	0	0	0	0	111			0	0	0	0		111		

Access Types Legend

Table 4-1973. PSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 23	NU27	RO	0h	Reserved
22 - 16	TDCV	RO	0h	Transmitter Delay Compensation Value
15	NU26	RO	0h	Reserved
14	PXE	RO	0h	Protocol Exception Event
13	RFDF	RO	0h	Recieved a CAN FD Message
12	RBRS	RO	0h	BRS flag of last recieved CAN FD Message
11	RESI	RO	0h	ESI flag of last recieved CAN FD Message
10 - 8	DLEC	RO	6Fh	Data Phase Last Error Code
7	BO	RO	0h	Bus_Off status
6	EW	RO	0h	Warning Status
5	EP	RO	0h	Error Passive
4 - 3	ACT	RO	0h	Activity
2 - 0	LEC	RO	6Fh	Last Error Code

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4.21.31 MSS_MCANn_CFG_TDCR Registers

4.21.31.1 MCANn_CFG_TDCR Register (Offset = 248h) [reset = h]

Short Description: TDCR

Long Description:

Return to Summary Table

Table 4-1974. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8248h
MCAN1_CFG	5261 8248h
MCAN2_CFG	5262 8248h
MCAN3_CFG	5263 8248h

Figure 4-746. TDCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU29															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU29	TDCO							NU28	TDCF						
RO	RW							RO	RW						
0	0							0	0						

Access Types Legend

Table 4-1975. TDCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 15	NU29	RO	0h	Reserved
14 - 8	TDCO	RW	0h	Transmitter Delay Compensation Offset
7	NU28	RO	0h	Reserved
6 - 0	TDCF	RW	0h	Transmitter Delay Compensation Filter Window Length

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4.21.32 MSS_MCANn_CFG_RES04 Registers

4.21.32.1 MCANn_CFG_RES04 Register (Offset = 24Ch) [reset = h]

Short Description: RES04

Long Description:

Return to Summary Table

Table 4-1976. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 824Ch
MCAN1_CFG	5261 824Ch
MCAN2_CFG	5262 824Ch
MCAN3_CFG	5263 824Ch

Figure 4-747. RES04 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES04															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES04															
RO															
0															

Access Types Legend

Table 4-1977. RES04 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES04	RO	0h	Reserved

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4.21.33 MSS_MCANn_CFG_IR Registers

4.21.33.1 MCANn_CFG_IR Register (Offset = 250h) [reset = h]

Short Description: IR

Long Description:

Return to Summary Table

Table 4-1978. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8250h
MCAN1_CFG	5261 8250h
MCAN2_CFG	5262 8250h
MCAN3_CFG	5263 8250h

Figure 4-748. IR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU30		ARA	PED	PEA	WDI	BO	EW	EP	ELO	BEU	BEC	DRX	TOO	MRAF	TSW
RO		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM	RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1979. IR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU30	RO	0h	Reserved
29	ARA	RW	0h	Access to Reserved Address
28	PED	RW	0h	Protocol Error in data Phase
27	PEA	RW	0h	Protocol Error in Arbitration Phase
26	WDI	RW	0h	Watchdog Interrupt
25	BO	RW	0h	Bus_Off Status
24	EW	RW	0h	Warning Status
23	EP	RW	0h	Error Passive
22	ELO	RW	0h	Error Logging Overflow
21	BEU	RW	0h	Bit Error Uncorrected
20	BEC	RW	0h	Bit Error Corrected
19	DRX	RW	0h	Message stored to Dedicated Rx Buffer
18	TOO	RW	0h	Timeout Occurred
17	MRAF	RW	0h	Message RAM Access Failure
16	TSW	RW	0h	Timestamp Wraparound
15	TEFL	RW	0h	Tx Event FIFO Element Lost
14	TEFF	RW	0h	Tx Event FIFO Full
13	TEFW	RW	0h	Tx Event FIFO Watermark Reached
12	TEFN	RW	0h	Tx Event FIFO New Entry
11	TFE	RW	0h	Tx FIFO Empty
10	TCF	RW	0h	Transmission Cancellation Finished
9	TC	RW	0h	Transmission Complete

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Table 4-1979. IR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	HPM	RW	0h	High Priority Message
7	RF1L	RW	0h	Rx FIFO 1 Message Lost
6	RF1F	RW	0h	Rx FIFO 1 Full
5	RF1W	RW	0h	Rx FIFO 1 Watermark Reached
4	RF1N	RW	0h	Rx FIFO 1 New Message
3	RF0L	RW	0h	Rx FIFO 0 Message Lost
2	RF0F	RW	0h	Rx FIFO 0 Full
1	RF0W	RW	0h	Rx FIFO 0 Watermark Reached
0	RF0N	RW	0h	Rx FIFO 0 New Message

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4.21.34 MSS_MCANn_CFG_IE Registers

4.21.34.1 MCANn_CFG_IE Register (Offset = 254h) [reset = h]

Short Description: IE

Long Description:

Return to Summary Table

Table 4-1980. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8254h
MCAN1_CFG	5261 8254h
MCAN2_CFG	5262 8254h
MCAN3_CFG	5263 8254h

Figure 4-749. IE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU31		ARAE	PEDE	PEAE	WDIE	BOE	EWE	EPE	ELOE	BEUE	BECE	DRX	TOOE	MRAFE	TSWE
RO		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1981. IE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU31	RO	0h	Reserved
29	ARAE	RW	0h	Accees to Reserve Address Interrupt Enable
28	PEDE	RW	0h	Protocol Error in Data Phase Interrupt Enable
27	PEAE	RW	0h	Protocol Error in Arbitration Phase Interrupt Enable
26	WDIE	RW	0h	Watchdog Interrupt Enable
25	BOE	RW	0h	Bus_Off Status Interrupt Enable
24	EWE	RW	0h	Warning Status Interrupt Enable
23	EPE	RW	0h	Error Passive Interrupt Enable
22	ELOE	RW	0h	Error Logging Overflow Interrupt Enable
21	BEUE	RW	0h	Bit Error Uncorrected Interrupt Enable
20	BECE	RW	0h	Bit Error Corrected Interrupt Enable
19	DRX	RW	0h	Message stored to Dedicated Rx Buffer Interrupt Enable
18	TOOE	RW	0h	Timeout Occurred Interrupt Enable
17	MRAFE	RW	0h	Message RAM Access Failure Interrupt Enable
16	TSWE	RW	0h	Timestamp Wraparound Interrupt Enable
15	TEFLE	RW	0h	Tx Event FIFO Event Lost Interrupt Enable
14	TEFFE	RW	0h	Tx Event FIFO Full Interrupt Enable
13	TEFWE	RW	0h	Tx Event FIFO Watermark Reached Interrupt enable
12	TEFNE	RW	0h	Tx Event FIFO New Entry Interrupt Enable
11	TFEE	RW	0h	Tx FIFO Empty Interrupt Enable

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Table 4-1981. IE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	TCFE	RW	0h	Transmission Cancellation Finishied Interrupt Enable
9	TCE	RW	0h	Transmission Completed Interrupt Enable
8	HPME	RW	0h	High Priority message Interrupt Enable
7	RF1LE	RW	0h	rx FIFO 1 Message Lost Interrupt Enable
6	RF1FE	RW	0h	Rx FIFO 1 Full Interrupt Enable
5	RF1WE	RW	0h	Rx FIFO 1 Watermark Reached Interrupt Enable
4	RF1NE	RW	0h	Rx FIFO 1 New Message Interrupt Enable
3	RF0LE	RW	0h	Rx FIFO 0 Message Lost Interrupt Enable
2	RF0FE	RW	0h	Rx FIFO 0 Full Interrupt Enable
1	RF0WE	RW	0h	Rx FIFO 0 Watermark Reached Interrupt Enable
0	RF0NE	RW	0h	Rx FIFO 0 New Message Interrupt Enable

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4.21.35 MSS_MCANn_CFG_ILS Registers

4.21.35.1 MCANn_CFG_ILS Register (Offset = 258h) [reset = h]

Short Description: ILS

Long Description:

Return to Summary Table

Table 4-1982. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8258h
MCAN1_CFG	5261 8258h
MCAN2_CFG	5262 8258h
MCAN3_CFG	5263 8258h

Figure 4-750. ILS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU32		ARAL	PEDL	PEAL	WDIL	BOL	EWL	EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL
RO		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-1983. ILS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU32	RO	0h	Reserved
29	ARAL	RW	0h	Accees to Reserve Address Interrupt Line
28	PEDL	RW	0h	Protocol Error in Data Phase Interrupt Line
27	PEAL	RW	0h	Protocol Error in Arbitration Phase Interrupt Line
26	WDIL	RW	0h	Watchdog Interrupt Line
25	BOL	RW	0h	Bus_Off Status Interrupt Line
24	EWL	RW	0h	Warning Status Interrupt Line
23	EPL	RW	0h	Error Passive Interrupt Line
22	ELOL	RW	0h	Error Logging Overflow Interrupt Line
21	BEUL	RW	0h	Bit Error Uncorrected Interrupt Line
20	BECL	RW	0h	Bit Error Corrected Interrupt Line
19	DRXL	RW	0h	Message stored to Dedicated Rx Buffer Interrupt Line
18	TOOL	RW	0h	Timeout Occurred Interrupt Line
17	MRAFL	RW	0h	Message RAM Access Failure Interrupt Line
16	TSWL	RW	0h	Timestamp Wraparound Interrupt Line
15	TEFLL	RW	0h	Tx Event FIFO Event Lost Interrupt Line
14	TEFFL	RW	0h	Tx Event FIFO Full Interrupt Line
13	TEFWL	RW	0h	Tx Event FIFO Watermark Reached Interrupt Line
12	TEFNL	RW	0h	Tx Event FIFO New Entry Interrupt Line
11	TFEL	RW	0h	Tx FIFO Empty Interrupt Line

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Table 4-1983. ILS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	TCFL	RW	0h	Transmission Cancellation Finishied Interrupt Line
9	TCL	RW	0h	Transmission Completed Interrupt Line
8	HPML	RW	0h	High Priority message Interrupt Line
7	RF1LL	RW	0h	rx FIFO 1 Message Lost Interrupt Line
6	RF1FL	RW	0h	Rx FIFO 1 Full Interrupt Line
5	RF1WL	RW	0h	Rx FIFO 1 Watermark Reached Interrupt Line
4	RF1NL	RW	0h	Rx FIFO 1 New Message Interrupt Line
3	RF0LL	RW	0h	Rx FIFO 0 Message Lost Interrupt Line
2	RF0FL	RW	0h	Rx FIFO 0 Full Interrupt Line
1	RF0WL	RW	0h	Rx FIFO 0 Watermark Reached Interrupt Line
0	RF0NL	RW	0h	Rx FIFO 0 New Message Interrupt Line

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4.21.36 MSS_MCANn_CFG_ILE Registers

4.21.36.1 MCANn_CFG_ILE Register (Offset = 25Ch) [reset = h]

Short Description: ILE

Long Description:

Return to Summary Table

Table 4-1984. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 825Ch
MCAN1_CFG	5261 825Ch
MCAN2_CFG	5262 825Ch
MCAN3_CFG	5263 825Ch

Figure 4-751. ILE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU33															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU33														EINT1	EINT0
RO														RW	RW
0														0	0

Access Types Legend

Table 4-1985. ILE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU33	RO	0h	Reserved
1	EINT1	RW	0h	Enable Interrupt Line 1
0	EINT0	RW	0h	Enable Interrupt Line 0

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4.21.37 MSS_MCANn_CFG_RES05 Registers

4.21.37.1 MCANn_CFG_RES05 Register (Offset = 260h) [reset = h]

Short Description: RES05

Long Description:

Return to Summary Table

Table 4-1986. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8260h
MCAN1_CFG	5261 8260h
MCAN2_CFG	5262 8260h
MCAN3_CFG	5263 8260h

Figure 4-752. RES05 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES05															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES05															
RO															
0															

Access Types Legend

Table 4-1987. RES05 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES05	RO	0h	Reserved

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4.21.38 MSS_MCANn_CFG_RES06 Registers

4.21.38.1 MCANn_CFG_RES06 Register (Offset = 264h) [reset = h]

Short Description: RES06

Long Description:

Return to Summary Table

Table 4-1988. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8264h
MCAN1_CFG	5261 8264h
MCAN2_CFG	5262 8264h
MCAN3_CFG	5263 8264h

Figure 4-753. RES06 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES06															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES06															
RO															
0															

Access Types Legend

Table 4-1989. RES06 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES06	RO	0h	Reserved

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4.21.39 MSS_MCANn_CFG_RES07 Registers

4.21.39.1 MCANn_CFG_RES07 Register (Offset = 268h) [reset = h]

Short Description: RES07

Long Description:

Return to Summary Table

Table 4-1990. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8268h
MCAN1_CFG	5261 8268h
MCAN2_CFG	5262 8268h
MCAN3_CFG	5263 8268h

Figure 4-754. RES07 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES07															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES07															
RO															
0															

Access Types Legend

Table 4-1991. RES07 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES07	RO	0h	Reserved

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4.21.40 MSS_MCANn_CFG_RES08 Registers

4.21.40.1 MCANn_CFG_RES08 Register (Offset = 26Ch) [reset = h]

Short Description: RES08

Long Description:

Return to Summary Table

Table 4-1992. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 826Ch
MCAN1_CFG	5261 826Ch
MCAN2_CFG	5262 826Ch
MCAN3_CFG	5263 826Ch

Figure 4-755. RES08 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES08															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES08															
RO															
0															

Access Types Legend

Table 4-1993. RES08 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES08	RO	0h	Reserved

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4.21.41 MSS_MCANn_CFG_RES09 Registers

4.21.41.1 MCANn_CFG_RES09 Register (Offset = 270h) [reset = h]

Short Description: RES09

Long Description:

Return to Summary Table

Table 4-1994. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8270h
MCAN1_CFG	5261 8270h
MCAN2_CFG	5262 8270h
MCAN3_CFG	5263 8270h

Figure 4-756. RES09 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES09															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES09															
RO															
0															

Access Types Legend

Table 4-1995. RES09 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES09	RO	0h	Reserved

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4.21.42 MSS_MCANn_CFG_RES10 Registers

4.21.42.1 MCANn_CFG_RES10 Register (Offset = 274h) [reset = h]

Short Description: RES10

Long Description:

Return to Summary Table

Table 4-1996. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8274h
MCAN1_CFG	5261 8274h
MCAN2_CFG	5262 8274h
MCAN3_CFG	5263 8274h

Figure 4-757. RES10 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES10															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES10															
RO															
0															

Access Types Legend

Table 4-1997. RES10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES10	RO	0h	Reserved

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4.21.43 MSS_MCANn_CFG_RES11 Registers

4.21.43.1 MCANn_CFG_RES11 Register (Offset = 278h) [reset = h]

Short Description: RES11

Long Description:

Return to Summary Table

Table 4-1998. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8278h
MCAN1_CFG	5261 8278h
MCAN2_CFG	5262 8278h
MCAN3_CFG	5263 8278h

Figure 4-758. RES11 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES11															
RO															
0															

Access Types Legend

Table 4-1999. RES11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES11	RO	0h	Reserved

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4.21.44 MSS_MCANn_CFG_RES12 Registers

4.21.44.1 MCANn_CFG_RES12 Register (Offset = 27Ch) [reset = h]

Short Description: RES12

Long Description:

Return to Summary Table

Table 4-2000. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 827Ch
MCAN1_CFG	5261 827Ch
MCAN2_CFG	5262 827Ch
MCAN3_CFG	5263 827Ch

Figure 4-759. RES12 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES12															
RO															
0															

Access Types Legend

Table 4-2001. RES12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES12	RO	0h	Reserved

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4.21.45 MSS_MCANn_CFG_GFC Registers

4.21.45.1 MCANn_CFG_GFC Register (Offset = 280h) [reset = h]

Short Description: GFC

Long Description:

Return to Summary Table

Table 4-2002. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8280h
MCAN1_CFG	5261 8280h
MCAN2_CFG	5262 8280h
MCAN3_CFG	5263 8280h

Figure 4-760. GFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU34															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU34										ANFS		ANFE		RRFS	RRFE
RO										RW		RW		RW	RW
0										0		0		0	0

Access Types Legend

Table 4-2003. GFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	NU34	RO	0h	Reserved
5 - 4	ANFS	RW	0h	Accept Non-matching Frames Standard
3 - 2	ANFE	RW	0h	Accept Non-matching Frames Extended
1	RRFS	RW	0h	reject Remote Frames Standard
0	RRFE	RW	0h	reject Remote Frames Extended

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4.21.46 MSS_MCANn_CFG_SIDFC Registers

4.21.46.1 MCANn_CFG_SIDFC Register (Offset = 284h) [reset = h]

Short Description: SIDFC

Long Description:

Return to Summary Table

Table 4-2004. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8284h
MCAN1_CFG	5261 8284h
MCAN2_CFG	5262 8284h
MCAN3_CFG	5263 8284h

Figure 4-761. SIDFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU36								LSS_S							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLSSA_S														NU35	
RW														RO	
0														0	

Access Types Legend

Table 4-2005. SIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU36	RO	0h	Reserved
23 - 16	LSS_S	RW	0h	List Size Standard
15 - 2	FLSSA_S	RW	0h	Filter List Standard Start Address
1 - 0	NU35	RO	0h	Reserved

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4.21.47 MSS_MCANn_CFG_XIDFC Registers

4.21.47.1 MCANn_CFG_XIDFC Register (Offset = 288h) [reset = h]

Short Description: XIDFC

Long Description:

Return to Summary Table

Table 4-2006. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8288h
MCAN1_CFG	5261 8228h
MCAN2_CFG	5262 8228h
MCAN3_CFG	5263 8228h

Figure 4-762. XIDFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU38								LSS_X							
RO								RW							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLSSA_X														NU37	
RW														RO	
0														0	

Access Types Legend

Table 4-2007. XIDFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NU38	RO	0h	Reserved
23 - 16	LSS_X	RW	0h	List Size Standard
15 - 2	FLSSA_X	RW	0h	Filter List Standard Start Address
1 - 0	NU37	RO	0h	Reserved

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4.21.48 MSS_MCANn_CFG_RES13 Registers

4.21.48.1 MCANn_CFG_RES13 Register (Offset = 28Ch) [reset = h]

Short Description: RES13

Long Description:

Return to Summary Table

Table 4-2008. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 828Ch
MCAN1_CFG	5261 828Ch
MCAN2_CFG	5262 828Ch
MCAN3_CFG	5263 828Ch

Figure 4-763. RES13 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES13															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES13															
RO															
0															

Access Types Legend

Table 4-2009. RES13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES13	RO	0h	Reserved

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4.21.49 MSS_MCANn_CFG_XIDAM Registers

4.21.49.1 MCANn_CFG_XIDAM Register (Offset = 290h) [reset = h]

Short Description: XIDAM

Long Description:

Return to Summary Table

Table 4-2010. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8290h
MCAN1_CFG	5261 8290h
MCAN2_CFG	5262 8290h
MCAN3_CFG	5263 8290h

Figure 4-764. XIDAM Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU39			EIDM												
RO			RW												
0			11111111111111111111111111111												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EIDM															
RW															
11111111111111111111111111111															

Access Types Legend

Table 4-2011. XIDAM Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	NU39	RO	0h	Reserved
28 - 0	EIDM	RW	23E6E54C4 50CAD4F67 1C71C7h	Extended ID Mask

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4.21.50 MSS_MCANn_CFG_HPMS Registers

4.21.50.1 MCANn_CFG_HPMS Register (Offset = 294h) [reset = h]

Short Description: HPMS

Long Description:

Return to Summary Table

Table 4-2012. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8294h
MCAN1_CFG	5261 8294h
MCAN2_CFG	5262 8294h
MCAN3_CFG	5263 8294h

Figure 4-765. HPMS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU40															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLST	FIDX							MSI		BIDX					
RO	RO							RO		RO					
0	0							0		0					

Access Types Legend

Table 4-2013. HPMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU40	RO	0h	Reserved
15	FLST	RO	0h	Filter List
14 - 8	FIDX	RO	0h	Filter Index
7 - 6	MSI	RO	0h	Message Storeage Indicator
5 - 0	BIDX	RO	0h	Buffer Index

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4.21.51 MSS_MCANn_CFG_NDAT1 Registers

4.21.51.1 MCANn_CFG_NDAT1 Register (Offset = 298h) [reset = h]

Short Description: NDAT1

Long Description:

Return to Summary Table

Table 4-2014. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 8298h
MCAN1_CFG	5261 8298h
MCAN2_CFG	5262 8298h
MCAN3_CFG	5263 8298h

Figure 4-766. NDAT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND0_31															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND0_31															
RW															
0															

Access Types Legend

Table 4-2015. NDAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ND0_31	RW	0h	New Data 0-31

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4.21.52 MSS_MCANn_CFG_NDAT2 Registers

4.21.52.1 MCANn_CFG_NDAT2 Register (Offset = 29Ch) [reset = h]

Short Description: NDAT2

Long Description:

Return to Summary Table

Table 4-2016. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 829Ch
MCAN1_CFG	5261 829Ch
MCAN2_CFG	5262 829Ch
MCAN3_CFG	5263 829Ch

Figure 4-767. NDAT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND32_63															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND32_63															
RW															
0															

Access Types Legend

Table 4-2017. NDAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ND32_63	RW	0h	New Data 32-63

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4.21.53 MSS_MCANn_CFG_RXF0C Registers

4.21.53.1 MCANn_CFG_RXF0C Register (Offset = 2A0h) [reset = h]

Short Description: RXF0C

Long Description:

Return to Summary Table

Table 4-2018. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82A0h
MCAN1_CFG	5261 82A0h
MCAN2_CFG	5262 82A0h
MCAN3_CFG	5263 82A0h

Figure 4-768. RXF0C Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
F0OM	F0WM							NU42_1	F0S						
RW	RW							RO	RW						
0	0							0	0						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU42	F0SA													NU41	
RO	RW													RO	
0	0													0	

Access Types Legend

Table 4-2019. RXF0C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F0OM	RW	0h	Rx FIFO 0 Operation Mode
30 - 24	F0WM	RW	0h	Rx FIFO 0 Watermark
23	NU42_1	RO	0h	Reserved
22 - 16	F0S	RW	0h	Rx FIFO 0 Size
15	NU42	RO	0h	Reserved
14 - 2	F0SA	RW	0h	Rx FIFO 0 Start Address
1 - 0	NU41	RO	0h	Reserved

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4.21.54 MSS_MCANn_CFG_RXF0S Registers

4.21.54.1 MCANn_CFG_RXF0S Register (Offset = 2A4h) [reset = h]

Short Description: RXF0S

Long Description:

Return to Summary Table

Table 4-2020. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82A4h
MCAN1_CFG	5261 82A4h
MCAN2_CFG	5262 82A4h
MCAN3_CFG	5263 82A4h

Figure 4-769. RXF0S Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU46						RF0L	F0F	NU45		F0PI					
RO						RO	RO	RO		RO					
0						0	0	0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU44		F0GI						NU43	F0FL						
RO		RO						RO	RO						
0		0						0	0						

Access Types Legend

Table 4-2021. RXF0S Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	NU46	RO	0h	Reserved
25	RF0L	RO	0h	Rx FIFO 0 Message Lost
24	F0F	RO	0h	Rx FIFO 0 Full
23 - 22	NU45	RO	0h	Reserved
21 - 16	F0PI	RO	0h	Rx FIFO 0 Put Index
15 - 14	NU44	RO	0h	Reserved
13 - 8	F0GI	RO	0h	Rx FIFO 0 Get Index
7	NU43	RO	0h	Reserved
6 - 0	F0FL	RO	0h	Rx FIFO 0 Fill Level

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4.21.55 MSS_MCANn_CFG_RXF0A Registers

4.21.55.1 MCANn_CFG_RXF0A Register (Offset = 2A8h) [reset = h]

Short Description: RXF0A

Long Description:

Return to Summary Table

Table 4-2022. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82A8h
MCAN1_CFG	5261 82A8h
MCAN2_CFG	5262 82A8h
MCAN3_CFG	5263 82A8h

Figure 4-770. RXF0A Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU47															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU47										F0AI					
RO										RW					
0										0					

Access Types Legend

Table 4-2023. RXF0A Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	NU47	RO	0h	Reserved
5 - 0	F0AI	RW	0h	Rx FIFO 0 Acknowledge Index

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4.21.56 MSS_MCANn_CFG_RXBC Registers

4.21.56.1 MCANn_CFG_RXBC Register (Offset = 2ACh) [reset = h]

Short Description: RXBC

Long Description:

Return to Summary Table

Table 4-2024. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82ACh
MCAN1_CFG	5261 82ACh
MCAN2_CFG	5262 82ACh
MCAN3_CFG	5263 82ACh

Figure 4-771. RXBC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU49															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBSA														NU48	
RW														RO	
0														0	

Access Types Legend

Table 4-2025. RXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	NU49	RO	0h	Reserved
15 - 2	RBSA	RW	0h	Rx Buffer Start Address
1 - 0	NU48	RO	0h	Reserved

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4.21.57 MSS_MCANn_CFG_RXF1C Registers

4.21.57.1 MCANn_CFG_RXF1C Register (Offset = 2B0h) [reset = h]

Short Description: RXF1C

Long Description:

Return to Summary Table

Table 4-2026. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82B0h
MCAN1_CFG	5261 82B0h
MCAN2_CFG	5262 82B0h
MCAN3_CFG	5263 82B0h

Figure 4-772. RXF1C Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
F1OM	F1WM							NU50_1	F1S						
RW	RW							RO	RW						
0	0							0	0						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU50	F1SA													NU499	
RO	RW													RO	
0	0													0	

Access Types Legend

Table 4-2027. RXF1C Register Field Descriptions

Bit	Field	Type	Reset	Description
31	F1OM	RW	0h	Rx FIFO 0 Operation Mode
30 - 24	F1WM	RW	0h	Rx FIFO 0 Watermark
23	NU50_1	RO	0h	Reserved
22 - 16	F1S	RW	0h	Rx FIFO 0 Size
15	NU50	RO	0h	Reserved
14 - 2	F1SA	RW	0h	Rx FIFO 0 Start Address
1 - 0	NU499	RO	0h	Reserved

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4.21.58 MSS_MCANn_CFG_RXF1S Registers

4.21.58.1 MCANn_CFG_RXF1S Register (Offset = 2B4h) [reset = h]

Short Description: RXF1S

Long Description:

Return to Summary Table

Table 4-2028. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82B4h
MCAN1_CFG	5261 82B4h
MCAN2_CFG	5262 82B4h
MCAN3_CFG	5263 82B4h

Figure 4-773. RXF1S Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU54						RF1L	F1F	NU53		F1PI					
RO						RO	RO	RO		RO					
0						0	0	0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU52		F1GI						NU51	F1FL						
RO		RO						RO	RO						
0		0						0	0						

Access Types Legend

Table 4-2029. RXF1S Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	NU54	RO	0h	Reserved
25	RF1L	RO	0h	Rx FIFO 0 Message Lost
24	F1F	RO	0h	Rx FIFO 0 Full
23 - 22	NU53	RO	0h	Reserved
21 - 16	F1PI	RO	0h	Rx FIFO 0 Put Index
15 - 14	NU52	RO	0h	Reserved
13 - 8	F1GI	RO	0h	Rx FIFO 0 Get Index
7	NU51	RO	0h	Reserved
6 - 0	F1FL	RO	0h	Rx FIFO 0 Fill Level

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4.21.59 MSS_MCANn_CFG_RXF1A Registers

4.21.59.1 MCANn_CFG_RXF1A Register (Offset = 2B8h) [reset = h]

Short Description: RXF1A

Long Description:

Return to Summary Table

Table 4-2030. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82B8h
MCAN1_CFG	5261 82B8h
MCAN2_CFG	5262 82B8h
MCAN3_CFG	5263 82B8h

Figure 4-774. RXF1A Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU55															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU55										F1AI					
RO										RW					
0										0					

Access Types Legend

Table 4-2031. RXF1A Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	NU55	RO	0h	Reserved
5 - 0	F1AI	RW	0h	Rx FIFO 0 Acknowledge Index

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4.21.60 MSS_MCANn_CFG_RXESC Registers

4.21.60.1 MCANn_CFG_RXESC Register (Offset = 2BCh) [reset = h]

Short Description: RXESC

Long Description:

Return to Summary Table

Table 4-2032. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82BCh
MCAN1_CFG	5261 82BCh
MCAN2_CFG	5262 82BCh
MCAN3_CFG	5263 82BCh

Figure 4-775. RXESC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU58															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU58					RBDS			NU57	F1DS			NU56	F0DS		
RO					RW			RO	RW			RO	RW		
0					0			0	0			0	0		

Access Types Legend

Table 4-2033. RXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 11	NU58	RO	0h	Reserved
10 - 8	RBDS	RW	0h	Rx Buffer data Field Size
7	NU57	RO	0h	Reserved
6 - 4	F1DS	RW	0h	Rx FIFO 1 Data Field Size
3	NU56	RO	0h	Reserved
2 - 0	F0DS	RW	0h	Rx FIFO 0 Data Field Size

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4.21.61 MSS_MCANn_CFG_TXBC Registers

4.21.61.1 MCANn_CFG_TXBC Register (Offset = 2C0h) [reset = h]

Short Description: TXBC

Long Description:

Return to Summary Table

Table 4-2034. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82C0h
MCAN1_CFG	5261 82C0h
MCAN2_CFG	5262 82C0h
MCAN3_CFG	5263 82C0h

Figure 4-776. TXBC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU61	TFQM	TFQS						NU60		NDTB					
RO	RO	RO						RO		RO					
0	0	0						0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBSA														NU59	
RO														RO	
0														0	

Access Types Legend

Table 4-2035. TXBC Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NU61	RO	0h	Reserved
30	TFQM	RO	0h	Tx FIFO/Queue Mode
29 - 24	TFQS	RO	0h	Transmit FIFO/Queue Size
23 - 22	NU60	RO	0h	Reserved
21 - 16	NDTB	RO	0h	Number of Dedicated Transmit Buffers
15 - 2	TBSA	RO	0h	Tx Buffers Start Address
1 - 0	NU59	RO	0h	Reserved

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4.21.62 MSS_MCANn_CFG_TXFQS Registers

4.21.62.1 MCANn_CFG_TXFQS Register (Offset = 2C4h) [reset = h]

Short Description: TXFQS

Long Description:

Return to Summary Table

Table 4-2036. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82C4h
MCAN1_CFG	5261 82C4h
MCAN2_CFG	5262 82C4h
MCAN3_CFG	5263 82C4h

Figure 4-777. TXFQS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU64										TFQF	TFQPI				
RO										RO	RO				
0										0	0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU63			TFGI					NU62		TFFL					
RO			RO					RO		RO					
0			0					0		0					

Access Types Legend

Table 4-2037. TXFQS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 22	NU64	RO	0h	Reserved
21	TFQF	RO	0h	Tx FIFO/Queue Full
20 - 16	TFQPI	RO	0h	Tx FIFO/Queue Put Index
15 - 13	NU63	RO	0h	Reserved
12 - 8	TFGI	RO	0h	Tx Queue Get Index
7 - 6	NU62	RO	0h	Reserved
5 - 0	TFFL	RO	0h	Tx FIFO Free Level

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4.21.63 MSS_MCANn_CFG_TXESC Registers

4.21.63.1 MCANn_CFG_TXESC Register (Offset = 2C8h) [reset = h]

Short Description: TXESC

Long Description:

Return to Summary Table

Table 4-2038. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82C8h
MCAN1_CFG	5261 82C8h
MCAN2_CFG	5262 82C8h
MCAN3_CFG	5263 82C8h

Figure 4-778. TXESC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU65															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU65													TBDS		
RO													RW		
0													0		

Access Types Legend

Table 4-2039. TXESC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	NU65	RO	0h	Reserved
2 - 0	TBDS	RW	0h	Tx Buffer Data Field Size

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4.21.64 MSS_MCANn_CFG_TXBRP Registers

4.21.64.1 MCANn_CFG_TXBRP Register (Offset = 2CCh) [reset = h]

Short Description: TXBRP

Long Description:

Return to Summary Table

Table 4-2040. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82CCh
MCAN1_CFG	5261 82CCh
MCAN2_CFG	5262 82CCh
MCAN3_CFG	5263 82CCh

Figure 4-779. TXBRP Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRP															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRP															
RO															
0															

Access Types Legend

Table 4-2041. TXBRP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TRP	RO	0h	Transmission Request Pending

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4.21.65 MSS_MCANn_CFG_TXBAR Registers

4.21.65.1 MCANn_CFG_TXBAR Register (Offset = 2D0h) [reset = h]

Short Description: TXBAR

Long Description:

Return to Summary Table

Table 4-2042. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82D0h
MCAN1_CFG	5261 82D0h
MCAN2_CFG	5262 82D0h
MCAN3_CFG	5263 82D0h

Figure 4-780. TXBAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AR															
RW W0TOCLR															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AR															
RW W0TOCLR															
0															

Access Types Legend

Table 4-2043. TXBAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	AR	RW W0TOCLR	0h	Add request

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4.21.66 MSS_MCANn_CFG_TXBCR Registers

4.21.66.1 MCANn_CFG_TXBCR Register (Offset = 2D4h) [reset = h]

Short Description: TXBCR

Long Description:

Return to Summary Table

Table 4-2044. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82D4h
MCAN1_CFG	5261 82D4h
MCAN2_CFG	5262 82D4h
MCAN3_CFG	5263 82D4h

Figure 4-781. TXBCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CR															
RW W0TOCLR															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CR															
RW W0TOCLR															
0															

Access Types Legend

Table 4-2045. TXBCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CR	RW W0TOCLR	0h	Cancellation Request

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4.21.67 MSS_MCANn_CFG_TXBTO Registers

4.21.67.1 MCANn_CFG_TXBTO Register (Offset = 2D8h) [reset = h]

Short Description: TXBTO

Long Description:

Return to Summary Table

Table 4-2046. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82D8h
MCAN1_CFG	5261 82D8h
MCAN2_CFG	5262 82D8h
MCAN3_CFG	5263 82D8h

Figure 4-782. TXBTO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TO															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TO															
RO															
0															

Access Types Legend

Table 4-2047. TXBTO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TO	RO	0h	Transmission Occurred

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4.21.68 MSS_MCANn_CFG_TXBCF Registers

4.21.68.1 MCANn_CFG_TXBCF Register (Offset = 2DCh) [reset = h]

Short Description: TXBCF

Long Description:

Return to Summary Table

Table 4-2048. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82DCh
MCAN1_CFG	5261 82DCh
MCAN2_CFG	5262 82DCh
MCAN3_CFG	5263 82DCh

Figure 4-783. TXBCF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CF															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CF															
RO															
0															

Access Types Legend

Table 4-2049. TXBCF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CF	RO	0h	Cancellation Finished

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4.21.69 MSS_MCANn_CFG_TXBTIE Registers

4.21.69.1 MCANn_CFG_TXBTIE Register (Offset = 2E0h) [reset = h]

Short Description: TXBTIE

Long Description:

Return to Summary Table

Table 4-2050. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82E0h
MCAN1_CFG	5261 82E0h
MCAN2_CFG	5262 82E0h
MCAN3_CFG	5263 82E0h

Figure 4-784. TXBTIE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIE															
RW															
0															

Access Types Legend

Table 4-2051. TXBTIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TIE	RW	0h	Transmission Interrupt Enable

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4.21.70 MSS_MCANn_CFG_TXBCIE Registers

4.21.70.1 MCANn_CFG_TXBCIE Register (Offset = 2E4h) [reset = h]

Short Description: TXBCIE

Long Description:

Return to Summary Table

Table 4-2052. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82E4h
MCAN1_CFG	5261 82E4h
MCAN2_CFG	5262 82E4h
MCAN3_CFG	5263 82E4h

Figure 4-785. TXBCIE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CFIE															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFIE															
RW															
0															

Access Types Legend

Table 4-2053. TXBCIE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CFIE	RW	0h	Cancellation Finished Interrupt Enable

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4.21.71 MSS_MCANn_CFG_RES14 Registers

4.21.71.1 MCANn_CFG_RES14 Register (Offset = 2E8h) [reset = h]

Short Description: RES14

Long Description:

Return to Summary Table

Table 4-2054. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82E8h
MCAN1_CFG	5261 82E8h
MCAN2_CFG	5262 82E8h
MCAN3_CFG	5263 82E8h

Figure 4-786. RES14 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES14															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES14															
RO															
0															

Access Types Legend

Table 4-2055. RES14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES14	RO	0h	Reserved

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4.21.72 MSS_MCANn_CFG_RES15 Registers

4.21.72.1 MCANn_CFG_RES15 Register (Offset = 2ECh) [reset = h]

Short Description: RES15

Long Description:

Return to Summary Table

Table 4-2056. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82ECh
MCAN1_CFG	5261 82ECh
MCAN2_CFG	5262 82ECh
MCAN3_CFG	5263 82ECh

Figure 4-787. RES15 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15															
RO															
0															

Access Types Legend

Table 4-2057. RES15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES15	RO	0h	Reserved

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4.21.73 MSS_MCANn_CFG_TXEFC Registers

4.21.73.1 MCANn_CFG_TXEFC Register (Offset = 2F0h) [reset = h]

Short Description: TXEFC

Long Description:

Return to Summary Table

Table 4-2058. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82F0h
MCAN1_CFG	5261 82F0h
MCAN2_CFG	5262 82F0h
MCAN3_CFG	5263 82F0h

Figure 4-788. TXEFC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU68				EFWM				NU67		EFS					
RW				RW				RW		RW					
0				0				0		0					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EFSA														NU66	
RW														RW	
0														0	

Access Types Legend

Table 4-2059. TXEFC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	NU68	RW	0h	Reserved
29 - 24	EFWM	RW	0h	Event FIFO Watermark
23 - 22	NU67	RW	0h	Reserved
21 - 16	EFS	RW	0h	Event FIFO Size
15 - 2	EFSA	RW	0h	Event FIFO Start Address
1 - 0	NU66	RW	0h	Reserved

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4.21.74 MSS_MCANn_CFG_TXEFS Registers

4.21.74.1 MCANn_CFG_TXEFS Register (Offset = 2F4h) [reset = h]

Short Description: TXEFS

Long Description:

Return to Summary Table

Table 4-2060. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82F4h
MCAN1_CFG	5261 82Fh
MCAN2_CFG	5262 82F4h
MCAN3_CFG	5263 82F4h

Figure 4-789. TXEFS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU72						TEFL	EFF	NU71			EFPI				
RO						RO	RO	RO			RO				
0						0	0	0			0				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU70			EFGI					NU69		EFFL					
RO			RO					RO		RO					
0			0					0		0					

Access Types Legend

Table 4-2061. TXEFS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	NU72	RO	0h	Reserved
25	TEFL	RO	0h	Tx Event FIFO Element Lost
24	EFF	RO	0h	Event FIFO Full
23 - 21	NU71	RO	0h	Reserved
20 - 16	EFPI	RO	0h	Event FIFO Put Index
15 - 13	NU70	RO	0h	Reserved
12 - 8	EFGI	RO	0h	Event FIFO Get Index
7 - 6	NU69	RO	0h	Reserved
5 - 0	EFFL	RO	0h	Event FIFO FIll Level

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4.21.75 MSS_MCANn_CFG_TXEFA Registers

4.21.75.1 MCANn_CFG_TXEFA Register (Offset = 2F8h) [reset = h]

Short Description: TXEFA

Long Description:

Return to Summary Table

Table 4-2062. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82F8h
MCAN1_CFG	5261 82F8h
MCAN2_CFG	5262 82F8h
MCAN3_CFG	5263 82F8h

Figure 4-790. TXEFA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU73															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU73											EFAI				
RO											RO				
0											0				

Access Types Legend

Table 4-2063. TXEFA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 5	NU73	RO	0h	Reserved
4 - 0	EFAI	RO	0h	Event FIFO Acknowledge Index

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4.21.76 MSS_MCANn_CFG_RES16 Registers

4.21.76.1 MCANn_CFG_RES16 Register (Offset = 2FCh) [reset = h]

Short Description: RES16

Long Description:

Return to Summary Table

Table 4-2064. Instance Table

Instance Name	Physical Address
MCAN0_CFG	5260 82FCh
MCAN1_CFG	5261 82FCh
MCAN2_CFG	5262 82FCh
MCAN3_CFG	5263 82FCh

Figure 4-791. RES16 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES16															
RO															
0															

Access Types Legend

Table 4-2065. RES16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RES16	RO	0h	Reserved

4.21.77 Access Table

Table 4-2066. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
WO	WO	Write
RW W0TOCLR	RW W0TOCLR	Read / Write 0 to Clear

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4.22 MCAN_ECC Registers

Table 4-2067. MSS_MCAN[0:2]_ECC Registers Base Address Table

Offset	Length	Acronym	MSS_MCAN0_ECC Physical Address	MSS_MCAN1_ECC Physical Address	MSS_MCAN2_ECC Physical Address
0h	32	MCAN_ECC_REV	5270 0000h	5270 1000h	5270 2000h
8h	32	MCAN_ECC_VECTOR	5270 0008h	5270 1008h	5270 2008h
Ch	32	MCAN_ECC_STAT	5270 000Ch	5270 100Ch	5270 200Ch
14h	32	MCAN_ECC_CTRL	5270 0014h	5270 1014h	5270 2014h
18h	32	MCAN_ECC_ERR_CTRL1	5270 0018h	5270 1018h	5270 2018h
1Ch	32	MCAN_ECC_ERR_CTRL2	5270 001Ch	5270 101Ch	5270 201Ch
20h	32	MCAN_ECC_ERR_STAT1	5270 0020h	5270 1020h	5270 2020h
24h	32	MCAN_ECC_ERR_STAT2	5270 0024h	5270 1024h	5270 2024h
28h	32	MCAN_ECC_ERR_STAT3	5270 0028h	5270 1028h	5270 2028h
3Ch	32	MCAN_ECC_SEC_EOI_REG	5270 003Ch	5270 103Ch	5270 203Ch
40h	32	MCAN_ECC_SEC_STATUS_REG0	5270 0040h	5270 1040h	5270 2040h
80h	32	MCAN_ECC_SEC_ENABLE_SET_REG0	5270 0080h	5270 1080h	5270 2080h
C0h	32	MCAN_ECC_SEC_ENABLE_CLR_REG0	5270 00C0h	5270 10C0h	5270 20C0h
13Ch	32	MCAN_ECC_DED_EOI_REG	5270 013Ch	5270 113Ch	5270 213Ch
140h	32	MCAN_ECC_DED_STATUS_REG0	5270 0140h	5270 1140h	5270 2140h
180h	32	MCAN_ECC_DED_ENABLE_SET_REG0	5270 0180h	5270 1180h	5270 2180h
1C0h	32	MCAN_ECC_DED_ENABLE_CLR_REG0	5270 01C0h	5270 11C0h	5270 21C0h
200h	32	MCAN_ECC_AGGR_ENABLE_SET	5270 0200h	5270 1200h	5270 2200h
204h	32	MCAN_ECC_AGGR_ENABLE_CLR	5270 0204h	5270 1204h	5270 2204h
208h	32	MCAN_ECC_AGGR_STATUS_SET	5270 0208h	5270 1208h	5270 2208h
20Ch	32	MCAN_ECC_AGGR_STATUS_CLR	5270 020Ch	5270 120Ch	5270 220Ch

Table 4-2068. MSS_MCAN3_ECC Registers Base Address Table

Offset	Length	Acronym	MSS_MCAN3_ECC Physical Address
0h	32	MCAN_ECC_REV	5270 3000h
8h	32	MCAN_ECC_VECTOR	5270 3008h
Ch	32	MCAN_ECC_STAT	5270 300Ch
14h	32	MCAN_ECC_CTRL	5270 3014h
18h	32	MCAN_ECC_ERR_CTRL1	5270 3018h
1Ch	32	MCAN_ECC_ERR_CTRL2	5270 301Ch
20h	32	MCAN_ECC_ERR_STAT1	5270 3020h
24h	32	MCAN_ECC_ERR_STAT2	5270 3024h
28h	32	MCAN_ECC_ERR_STAT3	5270 3028h
3Ch	32	MCAN_ECC_SEC_EOI_REG	5270 303Ch
40h	32	MCAN_ECC_SEC_STATUS_REG0	5270 3040h
80h	32	MCAN_ECC_SEC_ENABLE_SET_REG0	5270 3080h
C0h	32	MCAN_ECC_SEC_ENABLE_CLR_REG0	5270 30C0h
13Ch	32	MCAN_ECC_DED_EOI_REG	5270 313Ch

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Table 4-2068. MSS_MCAN3_ECC Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_MCAN3_ECC Physical Address
140h	32	MCAN_ECC_DED_STATUS_REG0	5270 3140h
180h	32	MCAN_ECC_DED_ENABLE_SET_REG0	5270 3180h
1C0h	32	MCAN_ECC_DED_ENABLE_CLR_REG0	5270 31C0h
200h	32	MCAN_ECC_AGGR_ENABLE_SET	5270 3200h
204h	32	MCAN_ECC_AGGR_ENABLE_CLR	5270 3204h
208h	32	MCAN_ECC_AGGR_STATUS_SET	5270 3208h
20Ch	32	MCAN_ECC_AGGR_STATUS_CLR	5270 320Ch

4.22.1 MCAN_ECC Instance Count Note

Note

n = 0 to 3 for the MCAN_ECC registers defined below.

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4.22.2 MSS_MCANn_ECC_REV Registers

4.22.2.1 MCANn_ECC_REV Register (Offset = 0h) [reset = h]

Short Description: Aggregator Revision Register

Long Description:

Return to Summary Table

Table 4-2069. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0000h
MCAN1_ECC	5270 1000h
MCAN2_ECC	5270 2000h
MCAN3_ECC	5270 3000h

Figure 4-792. REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
RO		RO		RO											
1		10		11010100000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
RO					RO			RO		RO					
11101					10			0		0					

Access Types Legend

Table 4-2070. REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	Scheme
29 - 28	BU	RO	Ah	bu
27 - 16	MODULE_ID	RO	29040CB20h	Module ID
15 - 11	REVRTL	RO	2B5Dh	RTL version
10 - 8	REVMAJ	RO	Ah	Major version
7 - 6	CUSTOM	RO	0h	Custom version
5 - 0	REVMIN	RO	0h	Minor version

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4.22.3 MSS_MCANn_ECC_VECTOR Registers

4.22.3.1 MCANn_ECC_VECTOR Register (Offset = 8h) [reset = h]

Short Description: ECC Vector Register

Long Description:

Return to Summary Table

Table 4-2071. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0008h
MCAN1_ECC	5270 1008h
MCAN2_ECC	5270 2008h
MCAN3_ECC	5270 3008h

Figure 4-793. VECTOR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU1							RD_SVBUS_DONE	RD_SVBUS_ADDR							
RO							RW	RW							
0							0	0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD_SVBUS	NU0				ECC_VEC										
RW	RO				RW										
0	0				0										

Access Types Legend

Table 4-2072. VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	NU1	RO	0h	Reserved
24	RD_SVBUS_DONE	RW	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field.
23 - 16	RD_SVBUS_ADDR	RW	0h	Read address
15	RD_SVBUS	RW	0h	Write 1 to trigger a read on the serial VBUS. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
14 - 11	NU0	RO	0h	Reserved
10 - 0	ECC_VEC	RW	0h	Value written to select the corresponding ECC RAM for control or status

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4.22.4 MSS_MCANn_ECC_STAT Registers

4.22.4.1 MCANn_ECC_STAT Register (Offset = Ch) [reset = h]

Short Description: Misc Status

Long Description:

Return to Summary Table

Table 4-2073. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 000Ch
MCAN1_ECC	5270 100Ch
MCAN2_ECC	5270 200Ch
MCAN3_ECC	5270 300Ch

Figure 4-794. STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU2															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU2					NUM_RAMS										
RO					RO										
0					10										

Access Types Legend

Table 4-2074. STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 11	NU2	RO	0h	Reserved
10 - 0	NUM_RAMS	RO	Ah	Indicates the number of RAMS serviced by the ECC aggregator

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4.22.5 MSS_MCANn_ECC_CTRL Registers

4.22.5.1 MCANn_ECC_CTRL Register (Offset = 14h) [reset = h]

Short Description: CTRL

Long Description:

Return to Summary Table

Table 4-2075. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0014h
MCAN1_ECC	5270 1014h
MCAN2_ECC	5270 2014h
MCAN3_ECC	5270 3014h

Figure 4-795. CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU3															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU3							CHECK_TIMEOUT	CHECK_PARITY	ERROR_ONCE	FORCE_N_ROW	FORCE_DED	FORCE_SEC	EN_RMW	ECC_CHK	ECC_EN
RO							WO	WO	WO	WO	WO	WO	WO	WO	WO
0							1	1	0	0	0	0	1	1	1

Access Types Legend

Table 4-2076. CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 9	NU3	RO	0h	TI Internal : Reserved
8	CHECK_TIMEOUT	WO	1h	TI Internal : Check timeout
7	CHECK_PARITY	WO	1h	TI Internal : Check Parity
6	ERROR_ONCE	WO	0h	TI Internal : Force Error only once
5	FORCE_N_ROW	WO	0h	TI Internal : Force Error on any RAM read
4	FORCE_DED	WO	0h	TI Internal : Force Double Bit Error
3	FORCE_SEC	WO	0h	TI Internal : Force Single Bit Error
2	EN_RMW	WO	1h	TI Internal : Enable rmw
1	ECC_CHK	WO	1h	TI Internal : Enable ECC check
0	ECC_EN	WO	1h	TI Internal : Enable ECC

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4.22.6 MSS_MCANn_ECC_ERR_CTRL1 Registers

4.22.6.1 MCANn_ECC_ERR_CTRL1 Register (Offset = 18h) [reset = h]

Short Description: ERR_CTRL1

Long Description:

Return to Summary Table

Table 4-2077. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0018h
MCAN1_ECC	5270 1018h
MCAN2_ECC	5270 2018h
MCAN3_ECC	5270 3018h

Figure 4-796. ERR_CTRL1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RW															
0															

Access Types Legend

Table 4-2078. ERR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RW	0h	TI Internal : Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set

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4.22.7 MSS_MCANn_ECC_ERR_CTRL2 Registers

4.22.7.1 MCANn_ECC_ERR_CTRL2 Register (Offset = 1Ch) [reset = h]

Short Description: ERR_CTRL2

Long Description:

Return to Summary Table

Table 4-2079. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 001Ch
MCAN1_ECC	5270 101Ch
MCAN2_ECC	5270 201Ch
MCAN3_ECC	5270 301Ch

Figure 4-797. ERR_CTRL2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT2															
RW															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_BIT1															
RW															
0															

Access Types Legend

Table 4-2080. ERR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT2	RW	0h	TI Internal : Data bit that needs to be flipped if double bit error needs to be forced
15 - 0	ECC_BIT1	RW	0h	TI Internal : Data bit that needs to be flipped when force_sec is set

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4.22.8 MSS_MCANn_ECC_ERR_STAT1 Registers

4.22.8.1 MCANn_ECC_ERR_STAT1 Register (Offset = 20h) [reset = h]

Short Description: ERR_STAT1

Long Description:

Return to Summary Table

Table 4-2081. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0020h
MCAN1_ECC	5270 1020h
MCAN2_ECC	5270 2020h
MCAN3_ECC	5270 3020h

Figure 4-798. ERR_STAT1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_BIT1_STS															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLR_ECC_CTRL_REG	CLR_ECC_PAR		CLR_ECC_OTHER	CLR_ECC_DED		CLR_ECC_SEC		ECC_CTRL_REG	ECC_PAR		ECC_OTHER	ECC_DED		ECC_SEC	
WO	WO		WO	WO		WO		WO	WO		WO	WO		WO	
0	0		0	0		0		0	0		0	0		0	

Access Types Legend

Table 4-2082. ERR_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	ECC_BIT1_STS	RO	0h	TI Internal : Data bit that corresponds to the single-bit error
15	CLR_ECC_CTRL_REG	WO	0h	TI Internal : Clear Ctrl Reg Error Status. Write 1 to clear. This bit is self clearing.
14 - 13	CLR_ECC_PAR	WO	0h	TI Internal : Clear Parity Error Status. Write 1 to clear. This bit is self clearing.
12	CLR_ECC_OTHER	WO	0h	TI Internal : Clear Other Error Status. Write 1 to clear. This bit is self clearing.
11 - 10	CLR_ECC_DED	WO	0h	TI Internal : Clear Double Bit Error Status. Write 1 to clear. This bit is self clearing.
9 - 8	CLR_ECC_SEC	WO	0h	TI Internal : Clear Single Bit Error Status. Write 1 to clear. This bit is self clearing.
7	ECC_CTRL_REG	WO	0h	TI Internal : Force ctrl reg pending interrupt. Write 1 to set. This bit is self clearing.
6 - 5	ECC_PAR	WO	0h	TI Internal : Force ECC parity pending interrupt. Write 1 to set. This bit is self clearing.
4	ECC_OTHER	WO	0h	TI Internal : Force ECC other pending interrupt. Write 1 to set. This bit is self clearing.
3 - 2	ECC_DED	WO	0h	TI Internal : Force ECC DED pending interrupt. Write 1 to set. This bit is self clearing.
1 - 0	ECC_SEC	WO	0h	TI Internal : Force ECC SEC pending interrupt. Write 1 to set. This bit is self clearing.

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4.22.9 MSS_MCANn_ECC_ERR_STAT2 Registers

4.22.9.1 MCANn_ECC_ERR_STAT2 Register (Offset = 24h) [reset = h]

Short Description: ERR_STAT2

Long Description:

Return to Summary Table

Table 4-2083. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0024h
MCAN1_ECC	5270 1024h
MCAN2_ECC	5270 2024h
MCAN3_ECC	5270 3024h

Figure 4-799. ERR_STAT2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_ROW															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_ROW															
RO															
0															

Access Types Legend

Table 4-2084. ERR_STAT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	ECC_ROW	RO	0h	TI Internal : Row address where the single or double-bit error has occurred

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4.22.10 MSS_MCANn_ECC_ERR_STAT3 Registers

4.22.10.1 MCANn_ECC_ERR_STAT3 Register (Offset = 28h) [reset = h]

Short Description: ERR_STAT3

Long Description:

Return to Summary Table

Table 4-2085. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0028h
MCAN1_ECC	5270 1028h
MCAN2_ECC	5270 2028h
MCAN3_ECC	5270 3028h

Figure 4-800. ERR_STAT3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU6															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU6						CLR_TIMEOUT_PEND	NU5							TIMEOUT_PEND	NU4
RO						WO	RO							WO	RO
0						0	0							0	0

Access Types Legend

Table 4-2086. ERR_STAT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 10	NU6	RO	0h	TI Internal : Reserved
9	CLR_TIMEOUT_PEND	WO	0h	TI Internal : Clear timeout pending
8 - 2	NU5	RO	0h	TI Internal : Reserved
1	TIMEOUT_PEND	WO	0h	TI Internal : Timeout pending
0	NU4	RO	0h	TI Internal : Reserved

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4.22.11 MSS_MCANn_ECC_SEC_EOI_REG Registers

4.22.11.1 MCANn_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-2087. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 003Ch
MCAN1_ECC	5270 103Ch
MCAN2_ECC	5270 203Ch
MCAN3_ECC	5270 303Ch

Figure 4-801. SEC_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU7															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU7															SEC_EOI_WR
RO															RW
0															0

Access Types Legend

Table 4-2088. SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU7	RO	0h	Reserved
0	SEC_EOI_WR	RW	0h	EOI Register. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. This bit is self clearing, reading this bit will return 0.

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4.22.12 MSS_MCANn_ECC_SEC_STATUS_REG0 Registers

4.22.12.1 MCANn_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-2089. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0040h
MCAN1_ECC	5270 1040h
MCAN2_ECC	5270 2040h
MCAN3_ECC	5270 3040h

Figure 4-802. SEC_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU8															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU8														CTRL_EDC_VBUSS_PEND	SEC_PEND
RO														RO	RO
0														0	0

Access Types Legend

Table 4-2090. SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU8	RO	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	RO	0h	Interrupt Pending Status for ctrl_edc_vbuss_pend.
0	SEC_PEND	RO	0h	Interrupt Pending Status for msgmem_pend.

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4.22.13 MSS_MCANn_ECC_SEC_ENABLE_SET_REG0 Registers

4.22.13.1 MCANn_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-2091. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0080h
MCAN1_ECC	5270 1080h
MCAN2_ECC	5270 2080h
MCAN3_ECC	5270 3080h

Figure 4-803. SEC_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU9															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU9														CTRL_EDC_VBUSS_ENABLE_SET	SEC_EN_SET
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2092. SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU9	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	RW	0h	Interrupt Enable Set Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	SEC_EN_SET	RW	0h	Interrupt Enable Set Register for msgmem_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

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4.22.14 MSS_MCANn_ECC_SEC_ENABLE_CLR_REG0 Registers

4.22.14.1 MCANn_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-2093. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 00C0h
MCAN1_ECC	5270 10C0h
MCAN2_ECC	5270 20C0h
MCAN3_ECC	5270 30C0h

Figure 4-804. SEC_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU10															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU10														CTRL_EDC_VBUSS_ENABLE_CLR	SEC_EN_CLR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2094. SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU10	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	SEC_EN_CLR	RW	0h	Interrupt Enable Clear Register for msgmem_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

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4.22.15 MSS_MCANn_ECC_DED_EOI_REG Registers

4.22.15.1 MCANn_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-2095. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 013Ch
MCAN1_ECC	5270 113Ch
MCAN2_ECC	5270 213Ch
MCAN3_ECC	5270 313Ch

Figure 4-805. DED_EOI_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU11															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU11															DED_EOI_WR
RO															RW
0															0

Access Types Legend

Table 4-2096. DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	NU11	RO	0h	Reserved
0	DED_EOI_WR	RW	0h	EOI Register. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. This bit is self clearing, reading this bit will return 0.

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4.22.16 MSS_MCANn_ECC_DED_STATUS_REG0 Registers

4.22.16.1 MCANn_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = h]

Short Description: Interrupt Status Register 0

Long Description:

Return to Summary Table

Table 4-2097. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0140h
MCAN1_ECC	5270 1140h
MCAN2_ECC	5270 2140h
MCAN3_ECC	5270 3140h

Figure 4-806. DED_STATUS_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU12															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU12														CTRL_EDC_VBUSS_PEND	DED_PEND
RO														RO	RO
0														0	0

Access Types Legend

Table 4-2098. DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU12	RO	0h	Reserved
1	CTRL_EDC_VBUSS_PEND	RO	0h	Interrupt Pending Status for ctrl_edc_vbuss_pend.
0	DED_PEND	RO	0h	Interrupt Pending Status for msgmem_pend.

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4.22.17 MSS_MCANn_ECC_DED_ENABLE_SET_REG0 Registers

4.22.17.1 MCANn_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = h]

Short Description: Interrupt Enable Set Register 0

Long Description:

Return to Summary Table

Table 4-2099. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0180h
MCAN1_ECC	5270 1180h
MCAN2_ECC	5270 2180h
MCAN3_ECC	5270 3180h

Figure 4-807. DED_ENABLE_SET_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU13															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU13														CTRL_EDC_VBUSS_ENABLE_SET	DED_EN_SET
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2100. DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU13	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_SET	RW	0h	Interrupt Enable Set Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	DED_EN_SET	RW	0h	Interrupt Enable Set Register for msgmem_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

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4.22.18 MSS_MCANn_ECC_DED_ENABLE_CLR_REG0 Registers

4.22.18.1 MCANn_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = h]

Short Description: Interrupt Enable Clear Register 0

Long Description:

Return to Summary Table

Table 4-2101. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 01C0h
MCAN1_ECC	5270 11C0h
MCAN2_ECC	5270 21C0h
MCAN3_ECC	5270 31C0h

Figure 4-808. DED_ENABLE_CLR_REG0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU14															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU14														CTRL_EDC_VBUSS_ENABLE_CLR	DED_EN_CLR
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2102. DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU14	RO	0h	Reserved
1	CTRL_EDC_VBUSS_ENABLE_CLR	RW	0h	Interrupt Enable Clear Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	DED_EN_CLR	RW	0h	Interrupt Enable Clear Register for msgmem_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

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4.22.19 MSS_MCANn_ECC_AGGR_ENABLE_SET Registers

4.22.19.1 MCANn_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = h]

Short Description: AGGR interrupt enable set Register

Long Description:

Return to Summary Table

Table 4-2103. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0200h
MCAN1_ECC	5270 1200h
MCAN2_ECC	5270 2200h
MCAN3_ECC	5270 3200h

Figure 4-809. AGGR_ENABLE_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU15															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU15														TIMEOUT	PARITY
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2104. AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU15	RO	0h	Reserved
1	TIMEOUT	RW	0h	Interrupt Enable Set Register for svbus timeout errors. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.
0	PARITY	RW	0h	Interrupt Enable Set Register for parity errors. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.

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4.22.20 MSS_MCANn_ECC_AGGR_ENABLE_CLR Registers

4.22.20.1 MCANn_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = h]

Short Description: AGGR interrupt enable clear Register

Long Description:

Return to Summary Table

Table 4-2105. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0204h
MCAN1_ECC	5270 1204h
MCAN2_ECC	5270 2204h
MCAN3_ECC	5270 3204h

Figure 4-810. AGGR_ENABLE_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU16															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU16														TIMEOUT	PARITY
RO														RW	RW
0														0	0

Access Types Legend

Table 4-2106. AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	NU16	RO	0h	Reserved
1	TIMEOUT	RW	0h	Interrupt Enable Clear for svbus timeout errors. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.
0	PARITY	RW	0h	Interrupt Enable Clear for parity errors. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.

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4.22.21 MSS_MCANn_ECC_AGGR_STATUS_SET Registers

4.22.21.1 MCANn_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = h]

Short Description: AGGR interrupt status set Register

Long Description:

Return to Summary Table

Table 4-2107. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 0208h
MCAN1_ECC	5270 1208h
MCAN2_ECC	5270 2208h
MCAN3_ECC	5270 3208h

Figure 4-811. AGGR_STATUS_SET Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU17															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU17												TIMEOUT		PARITY	
RO												RW		RW	
0												0		0	

Access Types Legend

Table 4-2108. AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU17	RO	0h	Reserved
3 - 2	TIMEOUT	RW	0h	Interrupt status set for svbus timeout errors. A write to increment field. Writing a value to this field increment the field value by the value written. Reads do not alter the value of the field.
1 - 0	PARITY	RW	0h	Interrupt status set for parity errors. A write to increment field. Writing a value to this field increment the field value by the value written. Reads do not alter the value of the field.

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4.22.22 MSS_MCANn_ECC_AGGR_STATUS_CLR Registers

4.22.22.1 MCANn_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = h]

Short Description: AGGR interrupt status clear Register

Long Description:

Return to Summary Table

Table 4-2109. Instance Table

Instance Name	Physical Address
MCAN0_ECC	5270 020Ch
MCAN1_ECC	5270 120Ch
MCAN2_ECC	5270 220Ch
MCAN3_ECC	5270 320Ch

Figure 4-812. AGGR_STATUS_CLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NU18															
RO															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU18												TIMEOUT		PARITY	
RO												RW		RW	
0												0		0	

Access Types Legend

Table 4-2110. AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	NU18	RO	0h	Reserved
3 - 2	TIMEOUT	RW	0h	Interrupt status clear for svbus timeout errors. A write to decrement field. Writing a value to this field decrements the field value by the value written. Reads do not alter the value of the field.
1 - 0	PARITY	RW	0h	Interrupt status clear for parity errors. A write to decrement field. Writing a value to this field decrements the field value by the value written. Reads do not alter the value of the field.

4.22.23 Access Table

Table 4-2111. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
WO	WO	Write

4.23 MCAN_MSG_RAM Registers

Table 4-2112. MSS_MCAN[0:2]_MSG_RAM Registers Base Address Table

Offset	Length	Acronym	MSS_MCAN0_MSG_RAM Physical Address	MSS_MCAN1_MSG_RAM Physical Address	MSS_MCAN2_MSG_RAM Physical Address
0h	32	MCAN_MSG_RAM_RAM_REG	5260 0000h	5261 0000h	5262 0000h

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Table 4-2113. MSS_MCAN3_MSG_RAM Registers Base Address Table

Offset	Length	Acronym	MSS_MCAN3_MSG_RAM Physical Address
0h	32	MCAN_MSG_RAM_RAM_REG	5263 0000h

4.23.1 MCAN_MSG_RAM Instance Count Note

Note

n = 0 to 3 for the MCAN_MSG_RAM registers defined below.

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4.23.2 MSS_MCANn_MSG_RAM_RAM_REG Registers

4.23.2.1 MCANn_MSG_RAM_RAM_REG Register (Offset = 0h) [reset = 0h]

Short Description: RAM memory word

Long Description:

Return to Summary Table

Table 4-2114. Instance Table

Instance Name	Physical Address
MCAN0_MSG_RAM	5260 0000h
MCAN1_MSG_RAM	5261 0000h
MCAN2_MSG_RAM	5262 0000h
MCAN3_MSG_RAM	5263 0000h

Figure 4-813. MCANn_MSG_RAM_RAM_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BYTE3								BYTE2							
R/W								R/W							
0								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BYTE1								BYTE0							
R/W								R/W							
0								0							

Access Types Legend

Table 4-2115. RAM_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	BYTE3	R/W	0h	This is the MS byte
23 - 16	BYTE2	R/W	0h	This is the UM byte
15 - 8	BYTE1	R/W	0h	This is the LM byte
7 - 0	BYTE0	R/W	0h	This is the LS byte

4.23.3 Access Table

Table 4-2116. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write

4.24 MCRC Registers

Table 4-2117. MSS_MCRC0 Registers Base Address Table

Offset	Length	Acronym	MSS_MCRC0 Physical Address
0h	32	MCRC_CRC_CTRL0	3500 0000h
8h	32	MCRC_CRC_CTRL1	3500 0008h
10h	32	MCRC_CRC_CTRL2	3500 0010h
18h	32	MCRC_CRC_INTS	3500 0018h
20h	32	MCRC_CRC_INTR	3500 0020h
28h	32	MCRC_CRC_STATUS_REG	3500 0028h
30h	32	MCRC_CRC_INT_OFFSET_REG	3500 0030h
38h	32	MCRC_CRC_BUSY	3500 0038h

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Table 4-2117. MSS_MCRC0 Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_MCRC0 Physical Address
40h	32	MCRC_CRC_PCOUNT_REG1	3500 0040h
44h	32	MCRC_CRC_SCOUNT_REG1	3500 0044h
48h	32	MCRC_CRC_CURSEC_REG1	3500 0048h
4Ch	32	MCRC_CRC_WDTOPLD1	3500 004Ch
50h	32	MCRC_CRC_BCTOPLD1	3500 0050h
60h	32	MCRC_PSA_SIGREGL1	3500 0060h
64h	32	MCRC_PSA_SIGREGH1	3500 0064h
68h	32	MCRC_CRC_REGL1	3500 0068h
6Ch	32	MCRC_CRC_REGH1	3500 006Ch
70h	32	MCRC_PSA_SECSIGREGL1	3500 0070h
74h	32	MCRC_PSA_SECSIGREGH1	3500 0074h
78h	32	MCRC_RAW_DATAREGL1	3500 0078h
7Ch	32	MCRC_RAW_DATAREGH1	3500 007Ch
80h	32	MCRC_CRC_PCOUNT_REG2	3500 0080h
84h	32	MCRC_CRC_SCOUNT_REG2	3500 0084h
88h	32	MCRC_CRC_CURSEC_REG2	3500 0088h
8Ch	32	MCRC_CRC_WDTOPLD2	3500 008Ch
90h	32	MCRC_CRC_BCTOPLD2	3500 0090h
A0h	32	MCRC_PSA_SIGREGL2	3500 00A0h
A4h	32	MCRC_PSA_SIGREGH2	3500 00A4h
A8h	32	MCRC_CRC_REGL2	3500 00A8h
ACh	32	MCRC_CRC_REGH2	3500 00ACh
B0h	32	MCRC_PSA_SECSIGREGL2	3500 00B0h
B4h	32	MCRC_PSA_SECSIGREGH2	3500 00B4h
B8h	32	MCRC_RAW_DATAREGL2	3500 00B8h
BCh	32	MCRC_RAW_DATAREGH2	3500 00BCh
C0h	32	MCRC_CRC_PCOUNT_REG3	3500 00C0h
C4h	32	MCRC_CRC_SCOUNT_REG3	3500 00C4h
C8h	32	MCRC_CRC_CURSEC_REG3	3500 00C8h
CCh	32	MCRC_CRC_WDTOPLD3	3500 00CCh
D0h	32	MCRC_CRC_BCTOPLD3	3500 00D0h
E0h	32	MCRC_PSA_SIGREGL3	3500 00E0h
E4h	32	MCRC_PSA_SIGREGH3	3500 00E4h
E8h	32	MCRC_CRC_REGL3	3500 00E8h
ECh	32	MCRC_CRC_REGH3	3500 00ECh
F0h	32	MCRC_PSA_SECSIGREGL3	3500 00F0h
F4h	32	MCRC_PSA_SECSIGREGH3	3500 00F4h
F8h	32	MCRC_RAW_DATAREGL3	3500 00F8h
FCh	32	MCRC_RAW_DATAREGH3	3500 00FCh
100h	32	MCRC_CRC_PCOUNT_REG4	3500 0100h
104h	32	MCRC_CRC_SCOUNT_REG4	3500 0104h
108h	32	MCRC_CRC_CURSEC_REG4	3500 0108h
10Ch	32	MCRC_CRC_WDTOPLD4	3500 010Ch
110h	32	MCRC_CRC_BCTOPLD4	3500 0110h
120h	32	MCRC_PSA_SIGREGL4	3500 0120h
124h	32	MCRC_PSA_SIGREGH4	3500 0124h
128h	32	MCRC_CRC_REGL4	3500 0128h

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Table 4-2117. MSS_MCRC0 Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_MCRC0 Physical Address
12Ch	32	MCRC_CRC_REGH4	3500 012Ch
130h	32	MCRC_PSA_SECSIGREGL4	3500 0130h
134h	32	MCRC_PSA_SECSIGREGH4	3500 0134h
138h	32	MCRC_RAW_DATAREGL4	3500 0138h
13Ch	32	MCRC_RAW_DATAREGH4	3500 013Ch
140h	32	MCRC_MCRC_BUS_SEL	3500 0140h
144h	32	MCRC_MCRC_RESERVED	3500 0144h

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4.24.1 MSS_MCRC0_CRC_CTRL0 Registers

4.24.1.1 MCRC0_CRC_CTRL0 Register (Offset = 0h) [reset = h]

Short Description: Contains sw reset control bit to reset PSA

Long Description:

Return to Summary Table

Table 4-2118. Instance Table

Instance Name	Physical Address
MCRC0	3500 0000h

Access Types Legend

Table 4-2119. CRC_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NU12	RO	0h	Reserved
30	NU11	RO	0h	Reserved
29	NU10	RO	0h	Reserved
28 - 27	NU9	RO	0h	Reserved
26 - 25	NU8	RO	0h	Reserved
24	NU7	RO	0h	Reserved
23	NU6	RO	0h	Reserved
22	NU5	RO	0h	Reserved
21	NU4	RO	0h	Reserved
20 - 19	NU3	RO	0h	Reserved
18 - 17	NU2	RO	0h	Reserved
16	NU1	RO	0h	Reserved
15	CH2_CRC_SEL2	RW	0h	Refer "CH2_DW_SEL" field description
14	CH2_BYTE_SWAP	RW	0h	BYTE SWAP Enable across Data Size0 ? Byte Swap Disabled1 ? Byte Swap enabled.
13	CH2_BIT_SWAP	RW	0h	msb/lsb SWAPPING 0 ? msb (most significant bit First)1 ? lsb (least significant bit First)
12 - 11	CH2_CRC_SEL	RW	0h	CRC type select. {CH1_CRC_SEL2,CH1_CRC_SEL[1:0]}000 ? CRC-64001 - CRC-16010 ? CRC-32100 - VDA CAN, SAE-J1850 CRC-8101 - H2F, Autosar 4.0110 - CASTAGNOLI, iSCSI111 / 011 - E2E Profile 4
10 - 9	CH2_DW_SEL	RW	0h	CRC Data Size select.000 ? 64 bit Data Size001 - 16 bit Data Size010 ? 32 Bit Data Size
8	CH2_PSA_SWREST	RW	0h	Channel 2 PSA Software Reset. When set, the PSA SignatureRegister is reset to all zero. Software reset does not reset softwarereset bit itself. Therefore, CPU is required to clear this bit by writinga ?0?.0 = PSA Signature Register not reset1 = PSA Signature Register reset
7	CH1_CRC_SEL2	RW	0h	Refer "CH1_DW_SEL" field description
6	CH1_BYTE_SWAP	RW	0h	BYTE SWAP Enable across Data Size0 ? Byte Swap Disabled1 ? Byte Swap enabled.
5	CH1_BIT_SWAP	RW	0h	msb/lsb SWAPPING 0 ? msb (most significant bit First)1 ? lsb (least significant bit First)
4 - 3	CH1_CRC_SEL	RW	0h	CRC type select. {CH1_CRC_SEL2,CH1_CRC_SEL[1:0]}000 ? CRC-64001 - CRC-16010 ? CRC-32100 - VDA CAN, SAE-J1850 CRC-8101 - H2F, Autosar 4.0110 - CASTAGNOLI, iSCSI111 / 011 - E2E Profile 4
2 - 1	CH1_DW_SEL	RW	0h	CRC Data Size select.000 ? 64 bit Data Size001 - 16 bit Data Size010 ? 32 Bit Data Size

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Table 4-2119. CRC_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CH1_PSA_SWREST	RW	0h	Channel 1 PSA Software Reset. When set, the PSA SignatureRegister is reset to all zero. Software reset does not reset softwarereset bit itself. Therefore, CPU is required to clear this bit by writinga ?0?.0 = PSA Signature Register not reset1 = PSA Signature Register reset

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4.24.2 MSS_MCRC0_CRC_CTRL1 Registers

4.24.2.1 MCRC0_CRC_CTRL1 Register (Offset = 8h) [reset = h]

Short Description: Contains power down control bit

Long Description:

Return to Summary Table

Table 4-2120. Instance Table

Instance Name	Physical Address
MCRC0	3500 0008h

Access Types Legend

Table 4-2121. CRC_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	RESERVED1	RO	0h	Not Defined
0	PWDN	RW	0h	Power Down. When set, MCRC moduleMCRC Module is put inpower down mode.0 = MCRC is not in power down mode1 = MCRC is in power down mode

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4.24.3 MSS_MCRC0_CRC_CTRL2 Registers

4.24.3.1 MCRC0_CRC_CTRL2 Register (Offset = 10h) [reset = h]

Short Description: Contains channel mode, data trace enable control bits

Long Description:

Return to Summary Table

Table 4-2122. Instance Table

Instance Name	Physical Address
MCRC0	3500 0010h

Access Types Legend

Table 4-2123. CRC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	RESERVED5	RO	0h	Not Defined
25 - 24	NU14	RO	0h	Reserved
23 - 18	RESERVED4	RO	0h	Not Defined
17 - 16	NU13	RO	0h	Reserved
15 - 10	RESERVED3	RO	0h	Not Defined
9 - 8	CH2_MODE	RW	0h	Channel 2 Mode:0 0 = Data Capture mode. In this mode, the PSA Signature Registerdoes not compress data when it is written. Any datawritten to PSA Signature Register is simply captured byPSA Signature Register without any compression. Thismode can be used to plant seed value into the PSA register0 1 = AUTO mode1 0 = reserved1 1 = Full-CPU mode
7 - 5	RESERVED2	RO	0h	Not Defined
4	CH1_TRACEEN	RW	0h	Channel 1 Data Trace Enable. When set, the channel is put intodata trace mode. The channel snoops on the CPU VBUSM,ITCM, DTCM buses for any read transaction. Any read data onthese buses is compressed by the PSA Signature Register. Whensuspend is on, the PSA Signature Register does not compress anyread data on these buses.0 = Data Trace disable1 = Data Trace enable
3 - 2	RESERVED1	RO	0h	Not Defined
1 - 0	CH1_MODE	RW	0h	Channel 1 Mode:0 0 = Data Capture mode. In this mode, the PSA Signature Registerdoes not compress data when it is written. Any datawritten to PSA Signature Register is simply captured byPSA Signature Register without any compression. Thismode can be used to plant seed value into the PSA register0 1 = AUTO mode1 0 = reserved1 1 = Full-CPU mode

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4.24.4 MSS_MCRC0_CRC_INTS Registers

4.24.4.1 MCRC0_CRC_INTS Register (Offset = 18h) [reset = h]

Short Description: Write one to a bit to enable a interrupt

Long Description:

Return to Summary Table

Table 4-2124. Instance Table

Instance Name	Physical Address
MCRC0	3500 0018h

Access Types Legend

Table 4-2125. CRC_INTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED5	RO	0h	Not Defined
28	NU22	RO	0h	Reserved
27	NU21	RO	0h	Reserved
26	NU20	RO	0h	Reserved
25	NU19	RO	0h	Reserved
24 - 21	RESERVED4	RO	0h	Not Defined
20	NU18	RO	0h	Reserved
19	NU17	RO	0h	Reserved
18	NU16	RO	0h	Reserved
17	NU15	RO	0h	Reserved
16 - 13	RESERVED3	RO	0h	Not Defined
12	CH2_TIMEOUTENS	RW	0h	Channel 2 Timeout Interrupt Enable Bit. Writing a one to thisbit enable the timeout interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Timeout Interrupt disable1 = Timeout Interrupt enableUser and privileged mode write:0 = Has no effect1 = Timeout Interrupt enable
11	CH2_UNDERENS	RW	0h	Channel 2 Underrun Interrupt Enable Bit. Writing a one tothis bit enable the underrun interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Underrun Interrupt disable1 = Underrun Interrupt enableUser and privileged mode write:0 = Has no effect1 = Underrun Interrupt enable
10	CH2_OVERENS	RW	0h	Channel 2 Overrun Interrupt Enable Bit. Writing a one to thisbit enable the overrun interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Overrun Interrupt disable1 = Overrun Interrupt enableUser and privileged mode write:0 = Has no effect1 = Overrun Interrupt enable
9	CH2_CRCFAILENS	RW	0h	Channel 2 CRC Fail Interrupt Enable Bit. Writing a one to thisbit enable the CRC fail interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = CRC Fail Interrupt disable1 = CRC Fail Interrupt enableUser and privileged mode write:0 = Has no effect1 = CRC Fail Interrupt enable
8 - 5	RESERVED2	RO	0h	Not Defined
4	CH1_TIMEOUTENS	RW	0h	Channel 1 Timeout Interrupt Enable Bit. Writing a one to thisbit enable the timeout interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Timeout Interrupt disable1 = Timeout Interrupt enableUser and privileged mode write:0 = Has no effect1 = Timeout Interrupt enable

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Table 4-2125. CRC_INTS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CH1_UNDERENS	RW	0h	Channel 1 Underrun Interrupt Enable Bit. Writing a one tothis bit enable the underrun interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Underrun Interrupt disable1 = Underrun Interrupt enableUser and privileged mode write:0 = Has no effect1 = Underrun Interrupt enable
2	CH1_OVERENS	RW	0h	Channel 1 Overrun Interrupt Enable Bit. Writing a one to thisbit enable the overrun interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Overrun Interrupt disable1 = Overrun Interrupt enableUser and privileged mode write:0 = Has no effect1 = Overrun Interrupt enable
1	CH1_CRCFAILENS	RW	0h	Channel 1 CRC Fail Interrupt Enable Bit. Writing a one to thisbit enable the CRC fail interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = CRC Fail Interrupt disable1 = CRC Fail Interrupt enableUser and privileged mode write:0 = Has no effect1 = CRC Fail Interrupt enable
0	RESERVED1	RO	0h	Not Defined

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4.24.5 MSS_MCRC0_CRC_INTR Registers

4.24.5.1 MCRC0_CRC_INTR Register (Offset = 20h) [reset = h]

Short Description: Write one to a bit to disable a interrupt

Long Description:

Return to Summary Table

Table 4-2126. Instance Table

Instance Name	Physical Address
MCRC0	3500 0020h

Access Types Legend

Table 4-2127. CRC_INTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED5	RO	0h	Not Defined
28	NU30	RO	0h	Reserved
27	NU29	RO	0h	Reserved
26	NU28	RO	0h	Reserved
25	NU27	RO	0h	Reserved
24 - 21	RESERVED4	RO	0h	Not Defined
20	NU26	RO	0h	Reserved
19	NU25	RO	0h	Reserved
18	NU24	RO	0h	Reserved
17	NU23	RO	0h	Reserved
16 - 13	RESERVED3	RO	0h	Not Defined
12	CH2_TIMEOUTENR	RW	0h	Channel 2 Timeout Interrupt Disable Bit. Writing a one to thisbit disable the timeout interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Timeout Interrupt disable1 = Timeout Interrupt enableUser and privileged mode write:0 = Has no effect1 = Timeout Interrupt disable
11	CH2_UNDERENR	RW	0h	Channel 2 Underrun Interrupt Disable Bit. Writing a one tothis bit disable the underrun interrupt. Writing a zero has noeffect. Reading from this bit gives the status (interrupt enable/dis-able).User and privileged mode read:0 = Underrun Interrupt disable1 = Underrun Interrupt enableUser and privileged mode write:0 = Has no effect1 = Underrun Interrupt disable
10	CH2_OVERENR	RW	0h	Channel 2 Overrun Interrupt Disable Bit. Writing a one to thisbit disable the overrun interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Overrun Interrupt disable1 = Overrun Interrupt enableUser and privileged mode write:0 = Has no effect1 = Overrun Interrupt disable
9	CH2_CRCFAILENR	RW	0h	Channel 2 CRC Fail Interrupt Disable Bit. Writing a one to thisbit disable the CRC fail interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = CRC Fail Interrupt disable1 = CRC Fail Interrupt enableUser and privileged mode write:0 = Has no effect1 = CRC Fail Interrupt disable
8 - 5	RESERVED2	RO	0h	Not Defined
4	CH1_TIMEOUTENR	RW	0h	Channel 1 Timeout Interrupt Disable Bit. Writing a one to thisbit disable the timeout interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Timeout Interrupt disable1 = Timeout Interrupt enableUser and privileged mode write:0 = Has no effect1 = Timeout Interrupt disable

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Table 4-2127. CRC_INTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CH1_UNDERENR	RW	0h	Channel 1 Underrun Interrupt Disable Bit. Writing a one tothis bit disable the underrun interrupt. Writing a zero has noeffect. Reading from this bit gives the status (interrupt enable/dis-able).User and privileged mode read:0 = Underrun Interrupt disable1 = Underrun Interrupt enableUser and privileged mode write:0 = Has no effect1 = Underrun Interrupt disable
2	CH1_OVERENR	RW	0h	Channel 1 Overrun Interrupt Disable Bit. Writing a one to thisbit disable the overrun interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = Overrun Interrupt disable1 = Overrun Interrupt enableUser and privileged mode write:0 = Has no effect1 = Overrun Interrupt disable
1	CH1_CRCFAILENR	RW	0h	Channel 1 CRC Fail Interrupt Disable Bit. Writing a one to thisbit disable the CRC fail interrupt. Writing a zero has no effect.Reading from this bit gives the status (interrupt enable/disable).User and privileged mode read:0 = CRC Fail Interrupt disable1 = CRC Fail Interrupt enableUser and privileged mode write:0 = Has no effect1 = CRC Fail Interrupt disable
0	RESERVED1	RO	0h	Not Defined

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4.24.6 MSS_MCRC0_CRC_STATUS_REG Registers

4.24.6.1 MCRC0_CRC_STATUS_REG Register (Offset = 28h) [reset = h]

Short Description: Contains interrupt flags for different types of interrupt

Long Description:

Return to Summary Table

Table 4-2128. Instance Table

Instance Name	Physical Address
MCRC0	3500 0028h

Access Types Legend

Table 4-2129. CRC_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED5	RO	0h	Not Defined
28	NU38	RO	0h	Reserved
27	NU37	RO	0h	Reserved
26	NU36	RO	0h	Reserved
25	NU35	RO	0h	Reserved
24 - 21	RESERVED4	RO	0h	Not Defined
20	NU34	RO	0h	Reserved
19	NU33	RO	0h	Reserved
18	NU32	RO	0h	Reserved
17	NU31	RO	0h	Reserved
16 - 13	RESERVED3	RO	0h	Not Defined
12	CH2_TIMEOUT	RW	0h	Channel 2 CRC Timeout Status Flag. This bit is cleared bywriting a ?1? to it only. Writing ?0? has no effect. This bit is set inAUTO mode.0 = No timeout interrupt is active1 = Timeout interrupt is active
11	CH2_UNDER	RW	0h	Channel 2 CRC Underrun Status Flag. This bit is cleared bywriting a ?1? to it only. Writing ?0? has no effect. This bit is set inAUTO mode only0 = No underrun interrupt is active1 = Underrun interrupt is active
10	CH2_OVER	RW	0h	Channel 2 CRC Overrun Status Flag. This bit is cleared bywriting a ?1? to it only. Writing ?0? has no effect. This bit is set inAUTO mode0 = No overrun interrupt is active1 = Overrun interrupt is active
9	CH2_CRCFAIL	RW	0h	Channel 2 CRC Compare Fail Status Flag. This bit is clearedby writing a ?1? to it only. Writing ?0? has no effect. This bit is setin AUTO mode only.0 = No CRC compare fail interrupt is active1 = CRC compare fail interrupt is active
8 - 5	RESERVED2	RO	0h	Not Defined
4	CH1_TIMEOUT	RW	0h	Channel 1 CRC Timeout Status Flag. This bit is cleared bywriting a ?1? to it only. Writing ?0? has no effect. This bit is set inAUTO mode.0 = No timeout interrupt is active1 = Timeout interrupt is active
3	CH1_UNDER	RW	0h	Channel 1 CRC Underrun Status Flag. This bit is cleared bywriting a ?1? to it only. Writing ?0? has no effect. This bit is set inAUTO mode only0 = No underrun interrupt is active1 = Underrun interrupt is active
2	CH1_OVER	RW	0h	Channel 1 CRC Overrun Status Flag. This bit is cleared bywriting a ?1? to it only. Writing ?0? has no effect. This bit is set inAUTO mode0 = No overrun interrupt is active1 = Overrun interrupt is active
1	CH1_CRCFAIL	RW	0h	Channel 1 CRC Compare Fail Status Flag. This bit is clearedby writing a ?1? to it only. Writing ?0? has no effect. This bit is setin AUTO mode only.0 = No CRC compare fail interrupt is active1 = CRC compare fail interrupt is active

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Table 4-2129. CRC_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED1	RO	0h	Not Defined

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4.24.7 MSS_MCRC0_CRC_INT_OFFSET_REG Registers

4.24.7.1 MCRC0_CRC_INT_OFFSET_REG Register (Offset = 30h) [reset = h]

Short Description: Contains the interrupt offset vector address

Long Description:

Return to Summary Table

Table 4-2130. Instance Table

Instance Name	Physical Address
MCRC0	3500 0030h

Access Types Legend

Table 4-2131. CRC_INT_OFFSET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED1	RO	0h	Not Defined
7 - 0	OFSTREG	RW	0h	CRC Interrupt Offset. This register indicates the highest prioritypending interrupt vector address. Reading the offset register auto-matically clear the respective interrupt flag. Please referenceTable 1?3. for details.

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4.24.8 MSS_MCRC0_CRC_BUSY Registers

4.24.8.1 MCRC0_CRC_BUSY Register (Offset = 38h) [reset = h]

Short Description: Contains the busy flag for each channel

Long Description:

Return to Summary Table

Table 4-2132. Instance Table

Instance Name	Physical Address
MCRC0	3500 0038h

Access Types Legend

Table 4-2133. CRC_BUSY Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	RESERVED4	RO	0h	Not Defined
24	NU40	RO	0h	Reserved
23 - 17	RESERVED3	RO	0h	Not Defined
16	NU39	RO	0h	Reserved
15 - 9	RESERVED2	RO	0h	Not Defined
8	CH2_BUSY	RO	0h	Ch2_BUSY. During AUTO mode, the busy flag is set when thefirst data pattern of the block is compressed and remains set untilthe the last data pattern of the block is compressed. The flag iscleared when the last data pattern of the block is compressed.
7 - 1	RESERVED1	RO	0h	Not Defined
0	CH1_BUSY	RO	0h	CH1_BUSY. During AUTO mode, the busy flag is set when thefirst data pattern of the block is compressed and remains set untilthe the last data pattern of the block is compressed. The flag iscleared when the last data pattern of the block is compressed.

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4.24.9 MSS_MCRC0_CRC_PCOUNT_REG1 Registers

4.24.9.1 MCRC0_CRC_PCOUNT_REG1 Register (Offset = 40h) [reset = h]

Short Description: Channel 1 preload register for the pattern count

Long Description:

Return to Summary Table

Table 4-2134. Instance Table

Instance Name	Physical Address
MCRC0	3500 0040h

Access Types Legend

Table 4-2135. CRC_PCOUNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	RESERVED1	RO	0h	Not Defined
19 - 0	CRC_PAT_COUNT1	RW	0h	Channel 1 Pattern Counter Preload Register. This register con-tains the number of data patterns in one sector to be compressedbefore a CRC is performed.

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4.24.10 MSS_MCRC0_CRC_SCOUNT_REG1 Registers

4.24.10.1 MCRC0_CRC_SCOUNT_REG1 Register (Offset = 44h) [reset = h]

Short Description: Channel 1 preload register for the sector count

Long Description:

Return to Summary Table

Table 4-2136. Instance Table

Instance Name	Physical Address
MCRC0	3500 0044h

Access Types Legend

Table 4-2137. CRC_SCOUNT_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED1	RO	0h	Not Defined
15 - 0	CRC_SEC_COUNT1	RW	0h	Channel 1 Sector Counter Preload Register. This register con-tains the number of sectors in one block of memory.

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4.24.11 MSS_MCRC0_CRC_CURSEC_REG1 Registers

4.24.11.1 MCRC0_CRC_CURSEC_REG1 Register (Offset = 48h) [reset = h]

Short Description: Channel 1 current sector register contains the sector number which causes CRC failure

Long Description:

Return to Summary Table

Table 4-2138. Instance Table

Instance Name	Physical Address
MCRC0	3500 0048h

Access Types Legend

Table 4-2139. CRC_CURSEC_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED1	RO	0h	Not Defined
15 - 0	CRC_CURSEC1	RW	0h	Channel 1 Current Sector ID Register. In AUTO mode, thisregister contains the current sector number of which the signatureverification fails. The sector counter is a free running up counter.When a sector fails, the erroneous sector number is logged intocurrent sector ID register and the CRC fail interrupt is generatedThe sector ID register is frozen until it is read and the CRC failstatus bit is cleared by CPU. While it is frozen, it does not captureanother erroneous sector number. When this condition happens,an overrun interrupt is generated instead. Once the register is readand the CRC fail interrupt flag is cleared it can capture new erro-neous sector number.

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4.24.12 MSS_MCRC0_CRC_WDTOPLD1 Registers

4.24.12.1 MCRC0_CRC_WDTOPLD1 Register (Offset = 4Ch) [reset = h]

Short Description: Channel 1 timeout pre-load value to check if within a given time DMA initiates a block transfer

Long Description:

Return to Summary Table

Table 4-2140. Instance Table

Instance Name	Physical Address
MCRC0	3500 004Ch

Access Types Legend

Table 4-2141. CRC_WDTOPLD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED1	RO	0h	Not Defined
23 - 0	CRC_WDTOPLD1	RW	0h	Channel 1 Watchdog Timeout Counter Preload Register. Thisregister contains the number of clock cycles within which theDMA must transfer the next block of data patterns.

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4.24.13 MSS_MCRC0_CRC_BCTOPLD1 Registers

4.24.13.1 MCRC0_CRC_BCTOPLD1 Register (Offset = 50h) [reset = h]

Short Description: Channel 1 timeout pre-load value to check if one block of patterns are compressed with a given time

Long Description:

Return to Summary Table

Table 4-2142. Instance Table

Instance Name	Physical Address
MCRC0	3500 0050h

Access Types Legend

Table 4-2143. CRC_BCTOPLD1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED1	RO	0h	Not Defined
23 - 0	CRC_BCTOPLD1	RW	0h	Channel 1 Block Complete Timeout Counter Preload Regis-ter. This register contains the number of clock cycles withinwhich the CRC for an entire block needs to complete before atimeout interrupt is generated.

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4.24.14 MSS_MCRC0_PSA_SIGREGL1 Registers

4.24.14.1 MCRC0_PSA_SIGREGL1 Register (Offset = 60h) [reset = h]

Short Description: Channel 1 PSA signature low register

Long Description:

Return to Summary Table

Table 4-2144. Instance Table

Instance Name	Physical Address
MCRC0	3500 0060h

Access Types Legend

Table 4-2145. PSA_SIGREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PSASIG1_31_0	RW	0h	Channel 1 PSA Signature Low Register. This register containsthe value stored at PSASIG1[31:0] register.

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4.24.15 MSS_MCRC0_PSA_SIGREGH1 Registers

4.24.15.1 MCRC0_PSA_SIGREGH1 Register (Offset = 64h) [reset = h]

Short Description: Channel 1 PSA signature high register

Long Description:

Return to Summary Table

Table 4-2146. Instance Table

Instance Name	Physical Address
MCRC0	3500 0064h

Access Types Legend

Table 4-2147. PSA_SIGREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PSA_SIG1_63_32	RW	0h	Channel 1 PSA Signature High Register. This register containsthe value stored at PSASIG1[63:32] register.

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4.24.16 MSS_MCRC0_CRC_REGL1 Registers

4.24.16.1 MCRC0_CRC_REGL1 Register (Offset = 68h) [reset = h]

Short Description: Channel 1 CRC value low register

Long Description:

Return to Summary Table

Table 4-2148. Instance Table

Instance Name	Physical Address
MCRC0	3500 0068h

Access Types Legend

Table 4-2149. CRC_REGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CRC1_31_0	RW	0h	Channel 1 CRC Value Low Register. This register contains thecurrent known good signature value stored at CRC1[31:0] register.

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4.24.17 MSS_MCRC0_CRC_REGH1 Registers

4.24.17.1 MCRC0_CRC_REGH1 Register (Offset = 6Ch) [reset = h]

Short Description: Channel 1 CRC value high register

Long Description:

Return to Summary Table

Table 4-2150. Instance Table

Instance Name	Physical Address
MCRC0	3500 006Ch

Access Types Legend

Table 4-2151. CRC_REGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CRC1_63_32	RW	0h	Channel 1 CRC Value High Register. This register contains thecurrent known good signature value stored at CRC1[63:32] register.

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4.24.18 MSS_MCRC0_PSA_SECSIGREGL1 Registers

4.24.18.1 MCRC0_PSA_SECSIGREGL1 Register (Offset = 70h) [reset = h]

Short Description: Channel 1 PSA sector signature low regis-ter

Long Description:

Return to Summary Table

Table 4-2152. Instance Table

Instance Name	Physical Address
MCRC0	3500 0070h

Access Types Legend

Table 4-2153. PSA_SECSIGREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PSASECSIG1_31_0	RO	0h	Channel 1 PSA Sector Signature Low Register. This registercontains the value stored at PSASECSIG1[31:0] register.

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4.24.19 MSS_MCRC0_PSA_SECSIGREGH1 Registers

4.24.19.1 MCRC0_PSA_SECSIGREGH1 Register (Offset = 74h) [reset = h]

Short Description: Channel 1 PSA sector signature high regis-ter

Long Description:

Return to Summary Table

Table 4-2154. Instance Table

Instance Name	Physical Address
MCRC0	3500 0074h

Access Types Legend

Table 4-2155. PSA_SECSIGREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PSASECSIG1_63_32	RO	0h	Channel 1 PSA Sector Signature High Register. This registercontains the value stored at PSASECSIG1[63:32] register.

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4.24.20 MSS_MCRC0_RAW_DATAREGL1 Registers

4.24.20.1 MCRC0_RAW_DATAREGL1 Register (Offset = 78h) [reset = h]

Short Description: Channel 1 un-compressed raw data low register

Long Description:

Return to Summary Table

Table 4-2156. Instance Table

Instance Name	Physical Address
MCRC0	3500 0078h

Access Types Legend

Table 4-2157. RAW_DATAREGL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RAW_DATA1_31_0	RO	0h	Channel 1 Raw Data Low Register. This register contains bit31:0 of the un-compressed raw data.

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4.24.21 MSS_MCRC0_RAW_DATAREGH1 Registers

4.24.21.1 MCRC0_RAW_DATAREGH1 Register (Offset = 7Ch) [reset = h]

Short Description: Channel 1 un-compressed raw data high register

Long Description:

Return to Summary Table

Table 4-2158. Instance Table

Instance Name	Physical Address
MCRC0	3500 007Ch

Access Types Legend

Table 4-2159. RAW_DATAREGH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RAW_DATA1_63_32	RO	0h	Channel 1 Raw Data High Register. This register contains bit63:32 of the un-compressed raw data.

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4.24.22 MSS_MCRC0_CRC_PCOUNT_REG2 Registers

4.24.22.1 MCRC0_CRC_PCOUNT_REG2 Register (Offset = 80h) [reset = h]

Short Description: Channel 2 preload register for the pattern count

Long Description:

Return to Summary Table

Table 4-2160. Instance Table

Instance Name	Physical Address
MCRC0	3500 0080h

Access Types Legend

Table 4-2161. CRC_PCOUNT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	RESERVED1	RO	0h	Not Defined
19 - 0	CRC_PAT_COUNT2	RW	0h	Channel 2 Pattern Counter Preload Register. This register con-tains the number of data patterns in one sector to be compressedbefore a CRC is performed.

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4.24.23 MSS_MCRC0_CRC_SCOUNT_REG2 Registers

4.24.23.1 MCRC0_CRC_SCOUNT_REG2 Register (Offset = 84h) [reset = h]

Short Description: Channel 2 preload register for the sector count

Long Description:

Return to Summary Table

Table 4-2162. Instance Table

Instance Name	Physical Address
MCRC0	3500 0084h

Access Types Legend

Table 4-2163. CRC_SCOUNT_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED1	RO	0h	Not Defined
15 - 0	CRC_SEC_COUNT2	RW	0h	Channel 2 Sector Counter Preload Register. This register con-tains the number of sectors in one block of memory.

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4.24.24 MSS_MCRC0_CRC_CURSEC_REG2 Registers

4.24.24.1 MCRC0_CRC_CURSEC_REG2 Register (Offset = 88h) [reset = h]

Short Description: Channel 2 current sector register contains the sector number which causes CRC fail-ure

Long Description:

Return to Summary Table

Table 4-2164. Instance Table

Instance Name	Physical Address
MCRC0	3500 0088h

Access Types Legend

Table 4-2165. CRC_CURSEC_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED1	RO	0h	Not Defined
15 - 0	CRC_CURSEC2	RW	0h	Channel 2 Current Sector ID Register. In AUTO mode, thisregister contains the current sector number of which the signatureverification fails. The sector counter is a free running up counter.When a sector fails, the erroneous sector number is logged intocurrent sector ID register and the CRC fail interrupt is generatedThe sector ID register is frozen until it is read and the CRC failstatus bit is cleared by CPU. While it is frozen, it does not captureanother erroneous sector number. When this condition happens,an overrun interrupt is generated instead. Once the register is readand the CRC fail interrupt flag is cleared it can capture new erro-neous sector number.

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4.24.25 MSS_MCRC0_CRC_WDTOPLD2 Registers

4.24.25.1 MCRC0_CRC_WDTOPLD2 Register (Offset = 8Ch) [reset = h]

Short Description: Channel 2 timeout pre-load value to check if within a given time DMA initiates a block transfer

Long Description:

Return to Summary Table

Table 4-2166. Instance Table

Instance Name	Physical Address
MCRC0	3500 008Ch

Access Types Legend

Table 4-2167. CRC_WDTOPLD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED1	RO	0h	Not Defined
23 - 0	CRC_WDTOPLD2	RW	0h	Channel 2 Watchdog Timeout Counter Preload Register. Thisregister contains the number of clock cycles within which theDMA must transfer the next block of data patterns.

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4.24.26 MSS_MCRC0_CRC_BCTOPLD2 Registers

4.24.26.1 MCRC0_CRC_BCTOPLD2 Register (Offset = 90h) [reset = h]

Short Description: Channel 2 timeout pre-load value to check if one block of patterns are compressed with a given time

Long Description:

Return to Summary Table

Table 4-2168. Instance Table

Instance Name	Physical Address
MCRC0	3500 0090h

Access Types Legend

Table 4-2169. CRC_BCTOPLD2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED1	RO	0h	Not Defined
23 - 0	CRC_BCTOPLD2	RW	0h	Channel 2 Block Complete Timeout Counter Preload Regis-ter. This register contains the number of clock cycles withinwhich the CRC for an entire block needs to complete before atimeout interrupt is generated.

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4.24.27 MSS_MCRC0_PSA_SIGREGL2 Registers

4.24.27.1 MCRC0_PSA_SIGREGL2 Register (Offset = A0h) [reset = h]

Short Description: Channel 2 PSA signature low register

Long Description:

Return to Summary Table

Table 4-2170. Instance Table

Instance Name	Physical Address
MCRC0	3500 00A0h

Access Types Legend

Table 4-2171. PSA_SIGREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PSASIG2_31_0	RW	0h	Channel 2 PSA Signature Low Register. This register containsthe value stored at PSASIG2[31:0] register.

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4.24.28 MSS_MCRC0_PSA_SIGREGH2 Registers

4.24.28.1 MCRC0_PSA_SIGREGH2 Register (Offset = A4h) [reset = h]

Short Description: Channel 2 PSA signature high register

Long Description:

Return to Summary Table

Table 4-2172. Instance Table

Instance Name	Physical Address
MCRC0	3500 00A4h

Access Types Legend

Table 4-2173. PSA_SIGREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PSA_SIG2_63_32	RW	0h	Channel 2 PSA Signature High Register. This register containsthe value stored at PSASIG2[63:32] register.

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4.24.29 MSS_MCRC0_CRC_REGL2 Registers

4.24.29.1 MCRC0_CRC_REGL2 Register (Offset = A8h) [reset = h]

Short Description: Channel 2 CRC value low register

Long Description:

Return to Summary Table

Table 4-2174. Instance Table

Instance Name	Physical Address
MCRC0	3500 00A8h

Access Types Legend

Table 4-2175. CRC_REGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CRC2_31_0	RW	0h	Channel 2 CRC Value Low Register. This register contains thecurrent known good signature value stored at CRC2[31:0] register.

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4.24.30 MSS_MCRC0_CRC_REGH2 Registers

4.24.30.1 MCRC0_CRC_REGH2 Register (Offset = ACh) [reset = h]

Short Description: Channel 2 CRC value high register

Long Description:

Return to Summary Table

Table 4-2176. Instance Table

Instance Name	Physical Address
MCRC0	3500 00ACh

Access Types Legend

Table 4-2177. CRC_REGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CRC2_63_32	RW	0h	Channel 2 CRC Value High Register. This register contains thecurrent known good signature value stored at CRC2[63:32] register.

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4.24.31 MSS_MCRC0_PSA_SECSIGREGL2 Registers

4.24.31.1 MCRC0_PSA_SECSIGREGL2 Register (Offset = B0h) [reset = h]

Short Description: Channel 2 PSA sector signature low regis-ter

Long Description:

Return to Summary Table

Table 4-2178. Instance Table

Instance Name	Physical Address
MCRC0	3500 00B0h

Access Types Legend

Table 4-2179. PSA_SECSIGREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PSASECSIG2_31_0	RO	0h	Channel 2 PSA Sector Signature Low Register. This registercontains the value stored at PSASECSIG2[31:0] register.

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4.24.32 MSS_MCRC0_PSA_SECSIGREGH2 Registers

4.24.32.1 MCRC0_PSA_SECSIGREGH2 Register (Offset = B4h) [reset = h]

Short Description: Channel 2 PSA sector signature high regis-ter

Long Description:

Return to Summary Table

Table 4-2180. Instance Table

Instance Name	Physical Address
MCRC0	3500 00B4h

Access Types Legend

Table 4-2181. PSA_SECSIGREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	PSASECSIG2_63_32	RO	0h	Channel 2 PSA Sector Signature High Register. This registercontains the value stored at PSASECSIG2[63:32] register.

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4.24.33 MSS_MCRC0_RAW_DATAREGL2 Registers

4.24.33.1 MCRC0_RAW_DATAREGL2 Register (Offset = B8h) [reset = h]

Short Description: Channel 2 un-compressed raw data low register

Long Description:

Return to Summary Table

Table 4-2182. Instance Table

Instance Name	Physical Address
MCRC0	3500 00B8h

Access Types Legend

Table 4-2183. RAW_DATAREGL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RAW_DATA2_31_0	RO	0h	Channel 2 Raw Data Low Register. This register contains bit31:0 of the un-compressed raw data.

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4.24.34 MSS_MCRC0_RAW_DATAREGH2 Registers

4.24.34.1 MCRC0_RAW_DATAREGH2 Register (Offset = BCh) [reset = h]

Short Description: Channel 2 un-compressed raw data high Register

Long Description:

Return to Summary Table

Table 4-2184. Instance Table

Instance Name	Physical Address
MCRC0	3500 00BCh

Access Types Legend

Table 4-2185. RAW_DATAREGH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RAW_DATA2_63_32	RO	0h	Channel 2 Raw Data High Register. This register contains bit63:32 of the un-compressed raw data.

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4.24.35 MSS_MCRC0_CRC_PCOUNT_REG3 Registers

4.24.35.1 MCRC0_CRC_PCOUNT_REG3 Register (Offset = C0h) [reset = h]

Short Description: Channel 3 preload register for the pattern count

Long Description:

Return to Summary Table

Table 4-2186. Instance Table

Instance Name	Physical Address
MCRC0	3500 00C0h

Access Types Legend

Table 4-2187. CRC_PCOUNT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	RESERVED1	RO	0h	Not Defined
19 - 0	NU41	RO	0h	Reserved

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4.24.36 MSS_MCRC0_CRC_SCOUNT_REG3 Registers

4.24.36.1 MCRC0_CRC_SCOUNT_REG3 Register (Offset = C4h) [reset = h]

Short Description: Channel 3 preload register for the sector count

Long Description:

Return to Summary Table

Table 4-2188. Instance Table

Instance Name	Physical Address
MCRC0	3500 00C4h

Access Types Legend

Table 4-2189. CRC_SCOUNT_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED1	RO	0h	Not Defined
15 - 0	NU42	RO	0h	Reserved

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4.24.37 MSS_MCRC0_CRC_CURSEC_REG3 Registers

4.24.37.1 MCRC0_CRC_CURSEC_REG3 Register (Offset = C8h) [reset = h]

Short Description: Channel 3 current sector register contains the sector number which causes CRC fail-ure

Long Description:

Return to Summary Table

Table 4-2190. Instance Table

Instance Name	Physical Address
MCRC0	3500 00C8h

Access Types Legend

Table 4-2191. CRC_CURSEC_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED1	RO	0h	Not Defined
15 - 0	NU43	RO	0h	Reserved

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4.24.38 MSS_MCRC0_CRC_WDTOPLD3 Registers

4.24.38.1 MCRC0_CRC_WDTOPLD3 Register (Offset = CCh) [reset = h]

Short Description: Channel 3 timeout pre-load value to check if within a given time DMA initiates a block transfer

Long Description:

Return to Summary Table

Table 4-2192. Instance Table

Instance Name	Physical Address
MCRC0	3500 00CCh

Access Types Legend

Table 4-2193. CRC_WDTOPLD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED1	RO	0h	Not Defined
23 - 0	NU44	RO	0h	Reserved

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4.24.39 MSS_MCRC0_CRC_BCTOPLD3 Registers

4.24.39.1 MCRC0_CRC_BCTOPLD3 Register (Offset = D0h) [reset = h]

Short Description: Channel 3 timeout pre-load value to check if one block of patterns are compressed with a given time

Long Description:

Return to Summary Table

Table 4-2194. Instance Table

Instance Name	Physical Address
MCRC0	3500 00D0h

Access Types Legend

Table 4-2195. CRC_BCTOPLD3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED1	RO	0h	Not Defined
23 - 0	NU45	RO	0h	Reserved

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4.24.40 MSS_MCRC0_PSA_SIGREGL3 Registers

4.24.40.1 MCRC0_PSA_SIGREGL3 Register (Offset = E0h) [reset = h]

Short Description: Channel 3 PSA signature low register

Long Description:

Return to Summary Table

Table 4-2196. Instance Table

Instance Name	Physical Address
MCRC0	3500 00E0h

Access Types Legend

Table 4-2197. PSA_SIGREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU46	RO	0h	Reserved

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4.24.41 MSS_MCRC0_PSA_SIGREGH3 Registers

4.24.41.1 MCRC0_PSA_SIGREGH3 Register (Offset = E4h) [reset = h]

Short Description: Channel 3 PSA signature high register

Long Description:

Return to Summary Table

Table 4-2198. Instance Table

Instance Name	Physical Address
MCRC0	3500 00E4h

Access Types Legend

Table 4-2199. PSA_SIGREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU47	RO	0h	Reserved

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4.24.42 MSS_MCRC0_CRC_REGL3 Registers

4.24.42.1 MCRC0_CRC_REGL3 Register (Offset = E8h) [reset = h]

Short Description: Channel 3 CRC value low register

Long Description:

Return to Summary Table

Table 4-2200. Instance Table

Instance Name	Physical Address
MCRC0	3500 00E8h

Access Types Legend

Table 4-2201. CRC_REGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU48	RO	0h	Reserved

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4.24.43 MSS_MCRC0_CRC_REGH3 Registers

4.24.43.1 MCRC0_CRC_REGH3 Register (Offset = ECh) [reset = h]

Short Description: Channel 3 CRC value high register

Long Description:

Return to Summary Table

Table 4-2202. Instance Table

Instance Name	Physical Address
MCRC0	3500 00ECh

Access Types Legend

Table 4-2203. CRC_REGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU49	RO	0h	Reserved

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4.24.44 MSS_MCRC0_PSA_SECSIGREGL3 Registers

4.24.44.1 MCRC0_PSA_SECSIGREGL3 Register (Offset = F0h) [reset = h]

Short Description: Channel 3 PSA sector signature low regis-ter

Long Description:

Return to Summary Table

Table 4-2204. Instance Table

Instance Name	Physical Address
MCRC0	3500 00F0h

Access Types Legend

Table 4-2205. PSA_SECSIGREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU50	RO	0h	Reserved

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4.24.45 MSS_MCRC0_PSA_SECSIGREGH3 Registers

4.24.45.1 MCRC0_PSA_SECSIGREGH3 Register (Offset = F4h) [reset = h]

Short Description: Channel 3 PSA sector signature high regis-ter

Long Description:

Return to Summary Table

Table 4-2206. Instance Table

Instance Name	Physical Address
MCRC0	3500 00F4h

Access Types Legend

Table 4-2207. PSA_SECSIGREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU51	RO	0h	Reserved

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4.24.46 MSS_MCRC0_RAW_DATAREGL3 Registers

4.24.46.1 MCRC0_RAW_DATAREGL3 Register (Offset = F8h) [reset = h]

Short Description: Channel 3 un-compressed raw data low register

Long Description:

Return to Summary Table

Table 4-2208. Instance Table

Instance Name	Physical Address
MCRC0	3500 00F8h

Access Types Legend

Table 4-2209. RAW_DATAREGL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU52	RO	0h	Reserved

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4.24.47 MSS_MCRC0_RAW_DATAREGH3 Registers

4.24.47.1 MCRC0_RAW_DATAREGH3 Register (Offset = FCh) [reset = h]

Short Description: Channel 3 un-compressed raw data high Register

Long Description:

Return to Summary Table

Table 4-2210. Instance Table

Instance Name	Physical Address
MCRC0	3500 00FCh

Access Types Legend

Table 4-2211. RAW_DATAREGH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU53	RO	0h	Reserved

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4.24.48 MSS_MCRC0_CRC_PCOUNT_REG4 Registers

4.24.48.1 MCRC0_CRC_PCOUNT_REG4 Register (Offset = 100h) [reset = h]

Short Description: Channel 4 preload register for the pattern count

Long Description:

Return to Summary Table

Table 4-2212. Instance Table

Instance Name	Physical Address
MCRC0	3500 0100h

Access Types Legend

Table 4-2213. CRC_PCOUNT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	RESERVED1	RO	0h	Not Defined
19 - 0	NU54	RO	0h	Reserved

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4.24.49 MSS_MCRC0_CRC_SCOUNT_REG4 Registers

4.24.49.1 MCRC0_CRC_SCOUNT_REG4 Register (Offset = 104h) [reset = h]

Short Description: Channel 4 preload register for the sector count

Long Description:

Return to Summary Table

Table 4-2214. Instance Table

Instance Name	Physical Address
MCRC0	3500 0104h

Access Types Legend

Table 4-2215. CRC_SCOUNT_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED1	RO	0h	Not Defined
15 - 0	NU55	RO	0h	Reserved

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4.24.50 MSS_MCRC0_CRC_CURSEC_REG4 Registers

4.24.50.1 MCRC0_CRC_CURSEC_REG4 Register (Offset = 108h) [reset = h]

Short Description: Channel 4 current sector register contains the sector number which causes CRC fail-ure

Long Description:

Return to Summary Table

Table 4-2216. Instance Table

Instance Name	Physical Address
MCRC0	3500 0108h

Access Types Legend

Table 4-2217. CRC_CURSEC_REG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED1	RO	0h	Not Defined
15 - 0	NU56	RO	0h	Reserved

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4.24.51 MSS_MCRC0_CRC_WDTOPLD4 Registers

4.24.51.1 MCRC0_CRC_WDTOPLD4 Register (Offset = 10Ch) [reset = h]

Short Description: Channel 4 timeout pre-load value to check if within a given time DMA initiates a block transfer

Long Description:

Return to Summary Table

Table 4-2218. Instance Table

Instance Name	Physical Address
MCRC0	3500 010Ch

Access Types Legend

Table 4-2219. CRC_WDTOPLD4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED1	RO	0h	Not Defined
23 - 0	NU57	RO	0h	Reserved

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4.24.52 MSS_MCRC0_CRC_BCTOPLD4 Registers

4.24.52.1 MCRC0_CRC_BCTOPLD4 Register (Offset = 110h) [reset = h]

Short Description: Channel 4 timeout pre-load value to check if one block of patterns are compressed with a given time

Long Description:

Return to Summary Table

Table 4-2220. Instance Table

Instance Name	Physical Address
MCRC0	3500 0110h

Access Types Legend

Table 4-2221. CRC_BCTOPLD4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RESERVED1	RO	0h	Not Defined
23 - 0	NU58	RO	0h	Reserved

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4.24.53 MSS_MCRC0_PSA_SIGREGL4 Registers

4.24.53.1 MCRC0_PSA_SIGREGL4 Register (Offset = 120h) [reset = h]

Short Description: Channel 4 PSA signature low register

Long Description:

Return to Summary Table

Table 4-2222. Instance Table

Instance Name	Physical Address
MCRC0	3500 0120h

Access Types Legend

Table 4-2223. PSA_SIGREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU59	RO	0h	Reserved

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4.24.54 MSS_MCRC0_PSA_SIGREGH4 Registers

4.24.54.1 MCRC0_PSA_SIGREGH4 Register (Offset = 124h) [reset = h]

Short Description: Channel 4 PSA signature high register

Long Description:

Return to Summary Table

Table 4-2224. Instance Table

Instance Name	Physical Address
MCRC0	3500 0124h

Access Types Legend

Table 4-2225. PSA_SIGREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU60	RO	0h	Reserved

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4.24.55 MSS_MCRC0_CRC_REGL4 Registers

4.24.55.1 MCRC0_CRC_REGL4 Register (Offset = 128h) [reset = h]

Short Description: Channel 4 CRC value low register

Long Description:

Return to Summary Table

Table 4-2226. Instance Table

Instance Name	Physical Address
MCRC0	3500 0128h

Access Types Legend

Table 4-2227. CRC_REGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU61	RO	0h	Reserved

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4.24.56 MSS_MCRC0_CRC_REGH4 Registers

4.24.56.1 MCRC0_CRC_REGH4 Register (Offset = 12Ch) [reset = h]

Short Description: Channel 4 CRC value high register

Long Description:

Return to Summary Table

Table 4-2228. Instance Table

Instance Name	Physical Address
MCRC0	3500 012Ch

Access Types Legend

Table 4-2229. CRC_REGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU62	RO	0h	Reserved

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4.24.57 MSS_MCRC0_PSA_SECSIGREGL4 Registers

4.24.57.1 MCRC0_PSA_SECSIGREGL4 Register (Offset = 130h) [reset = h]

Short Description: Channel 4 PSA sector signature low regis-ter

Long Description:

Return to Summary Table

Table 4-2230. Instance Table

Instance Name	Physical Address
MCRC0	3500 0130h

Access Types Legend

Table 4-2231. PSA_SECSIGREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU63	RO	0h	Reserved

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4.24.58 MSS_MCRC0_PSA_SECSIGREGH4 Registers

4.24.58.1 MCRC0_PSA_SECSIGREGH4 Register (Offset = 134h) [reset = h]

Short Description: Channel 4 PSA sector signature high regis-ter

Long Description:

Return to Summary Table

Table 4-2232. Instance Table

Instance Name	Physical Address
MCRC0	3500 0134h

Access Types Legend

Table 4-2233. PSA_SECSIGREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU64	RO	0h	Reserved

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4.24.59 MSS_MCRC0_RAW_DATAREGL4 Registers

4.24.59.1 MCRC0_RAW_DATAREGL4 Register (Offset = 138h) [reset = h]

Short Description: Channel 4 un-compressed raw data low register

Long Description:

Return to Summary Table

Table 4-2234. Instance Table

Instance Name	Physical Address
MCRC0	3500 0138h

Access Types Legend

Table 4-2235. RAW_DATAREGL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU65	RO	0h	Reserved

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4.24.60 MSS_MCRC0_RAW_DATAREGH4 Registers

4.24.60.1 MCRC0_RAW_DATAREGH4 Register (Offset = 13Ch) [reset = h]

Short Description: Channel 4 un-compressed raw data high Register

Long Description:

Return to Summary Table

Table 4-2236. Instance Table

Instance Name	Physical Address
MCRC0	3500 013Ch

Access Types Legend

Table 4-2237. RAW_DATAREGH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU66	RO	0h	Reserved

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4.24.61 MSS_MCRC0_MCRC_BUS_SEL Registers

4.24.61.1 MCRC0_MCRC_BUS_SEL Register (Offset = 140h) [reset = h]

Short Description: Disables either or all tracing of data buses

Long Description:

Return to Summary Table

Table 4-2238. Instance Table

Instance Name	Physical Address
MCRC0	3500 0140h

Access Types Legend

Table 4-2239. MCRC_BUS_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 3	NU67	RO	0h	Reserved
2	MEN	RW	1h	MEn. Enable/disables the tracing of VBUSM 0: Tracing of VBUSM master bus has been disabled 1: Tracing of VBUSM master bus has been enabled
1	DTCMEN	RW	1h	DTCMEn. Enable/disables the tracing of data TCM0: Tracing of DTCM_ODD and DTCM_EVEN buses have been disabled1: Tracing of DTCM_ODD and DTCM_EVEN buses have been enabled
0	ITCMEN	RW	1h	ITCMEn. Enable/disables the tracing of instruction TCM 0: Tracing of ITCM bus has been disabled 1: Tracing of ITCM bus has been enabled

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4.24.62 MSS_MCRC0_MCRC_RESERVED Registers

4.24.62.1 MCRC0_MCRC_RESERVED Register (Offset = 144h) [reset = h]

Short Description: 0x144 to 0x1FF is reserved area.

Long Description:

Return to Summary Table

Table 4-2240. Instance Table

Instance Name	Physical Address
MCRC0	3500 0144h

Access Types Legend

Table 4-2241. MCRC_RESERVED Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	NU68	RO	0h	0x144 to 0x1FF is reserved area.

4.24.63 Access Table

Table 4-2242. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

4.25 QSPI Registers

Table 4-2243. MSS_QSPI0 Registers Base Address Table

Offset	Length	Acronym	MSS_QSPI0 Physical Address
0h	32	QSPI_PID	4820 0000h
4h	32	QSPI_RESERVED1	4820 0004h
8h	32	QSPI_RESERVED2	4820 0008h
Ch	32	QSPI_RESERVED3	4820 000Ch
10h	32	QSPI_SYSCONFIG	4820 0010h
14h	32	QSPI_RESERVED4	4820 0014h
18h	32	QSPI_RESERVED5	4820 0018h
1Ch	32	QSPI_RESERVED6	4820 001Ch
20h	32	QSPI_INTR_STATUS_RAW_SET	4820 0020h
24h	32	QSPI_INTR_STATUS_ENABLED_CLEAR	4820 0024h
28h	32	QSPI_INTR_ENABLE_SET	4820 0028h
2Ch	32	QSPI_INTR_ENABLE_CLEAR	4820 002Ch
30h	32	QSPI_INTC_EOI	4820 0030h
34h	32	QSPI_RESERVED7	4820 0034h
38h	32	QSPI_RESERVED8	4820 0038h
3Ch	32	QSPI_RESERVED9	4820 003Ch
40h	32	QSPI_SPI_CLOCK_CNTRL	4820 0040h
44h	32	QSPI_SPI_DC	4820 0044h
48h	32	QSPI_SPI_CMD	4820 0048h
4Ch	32	QSPI_SPI_STATUS	4820 004Ch
50h	32	QSPI_SPI_DATA	4820 0050h
54h	32	QSPI_SPI_SETUP0	4820 0054h

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Table 4-2243. MSS_QSPI0 Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_QSPI0 Physical Address
58h	32	QSPI_SPI_SETUP1	4820 0058h
5Ch	32	QSPI_SPI_SETUP2	4820 005Ch
60h	32	QSPI_SPI_SETUP3	4820 0060h
64h	32	QSPI_SPI_SWITCH	4820 0064h
68h	32	QSPI_SPI_DATA1	4820 0068h
6Ch	32	QSPI_SPI_DATA2	4820 006Ch
70h	32	QSPI_SPI_DATA3	4820 0070h

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4.25.1 MSS_QSPI0_PID Registers

4.25.1.1 QSPI0_PID Register (Offset = 0h) [reset = h]

Short Description: PID

Long Description:

Return to Summary Table

Table 4-2244. Instance Table

Instance Name	Physical Address
QSPI0	4820 0000h

Access Types Legend

Table 4-2245. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	The scheme of the register used. This indicates the PDR3.5 Method
29 - 28	RESERVED	RO		Always read as 0
27 - 16	FUNC	RO	19DE22B940h	The function of the module being used
15 - 11	RTL	RO	0h	RTL Release Version The PDR release number of this IP
10 - 8	MAJOR	RO	0h	Major Release Number
7 - 6	CUSTOM	RO	0h	Custom IP
5 - 0	MINOR	RO	0h	Minor Release Number

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4.25.2 MSS_QSPI0_RESERVED1 Registers

4.25.2.1 QSPI0_RESERVED1 Register (Offset = 4h) [reset = h]

Short Description: Reserved

Long Description:

Return to Summary Table

Table 4-2246. Instance Table

Instance Name	Physical Address
QSPI0	4820 0004h

Access Types Legend

Table 4-2247. RESERVED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_1	RO	0h	Reserved

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4.25.3 MSS_QSPI0_RESERVED2 Registers

4.25.3.1 QSPI0_RESERVED2 Register (Offset = 8h) [reset = h]

Short Description: Reserved

Long Description:

Return to Summary Table

Table 4-2248. Instance Table

Instance Name	Physical Address
QSPI0	4820 0008h

Access Types Legend

Table 4-2249. RESERVED2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_2	RO	0h	Reserved

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4.25.4 MSS_QSPI0_RESERVED3 Registers

4.25.4.1 QSPI0_RESERVED3 Register (Offset = Ch) [reset = h]

Short Description: Reserved

Long Description:

Return to Summary Table

Table 4-2250. Instance Table

Instance Name	Physical Address
QSPI0	4820 000Ch

Access Types Legend

Table 4-2251. RESERVED3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_3	RO	0h	Reserved

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4.25.5 MSS_QSPI0_SYSCONFIG Registers

4.25.5.1 QSPI0_SYSCONFIG Register (Offset = 10h) [reset = h]

Short Description: SYSCONFIG

Long Description:

Return to Summary Table

Table 4-2252. Instance Table

Instance Name	Physical Address
QSPI0	4820 0010h

Access Types Legend

Table 4-2253. SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	RESERVED3	RO	0h	Always read as 0
5 - 4	RESERVED2	RO	0h	Always read as 0
3 - 2	IDLEMODE	RW	Ah	Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state0x0 : Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, i.e. regardless of the IP module's internal requirements. Backup mode, for debug only0x1 : No-idle mode: local target never enters idle state. Backup mode, for debug only0x2 : Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wakeup events0x3 : Smart-idle wakeup-capable mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module may generate (IRQ- or DMA-request-related) wakeup events when in idle state.Mode is only relevant if the appropriate IP module "swakeup" output(s) is (are) implemented
1 - 0	RESERVED1	RO	0h	Always read as 0

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4.25.6 MSS_QSPI0_RESERVED4 Registers

4.25.6.1 QSPI0_RESERVED4 Register (Offset = 14h) [reset = h]

Short Description: Reserved

Long Description:

Return to Summary Table

Table 4-2254. Instance Table

Instance Name	Physical Address
QSPI0	4820 0014h

Access Types Legend

Table 4-2255. RESERVED4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_4	RO	0h	Reserved

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4.25.7 MSS_QSPI0_RESERVED5 Registers

4.25.7.1 QSPI0_RESERVED5 Register (Offset = 18h) [reset = h]

Short Description: Reserved

Long Description:

Return to Summary Table

Table 4-2256. Instance Table

Instance Name	Physical Address
QSPI0	4820 0018h

Access Types Legend

Table 4-2257. RESERVED5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_5	RO	0h	Reserved

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4.25.8 MSS_QSPI0_RESERVED6 Registers

4.25.8.1 QSPI0_RESERVED6 Register (Offset = 1Ch) [reset = h]

Short Description: Reserved

Long Description:

Return to Summary Table

Table 4-2258. Instance Table

Instance Name	Physical Address
QSPI0	4820 001Ch

Access Types Legend

Table 4-2259. RESERVED6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_6	RO	0h	Reserved

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4.25.9 MSS_QSPI0_INTR_STATUS_RAW_SET Registers

4.25.9.1 QSPI0_INTR_STATUS_RAW_SET Register (Offset = 20h) [reset = h]

Short Description: INTR Interrupt Status Raw/Set Register

Long Description:

Return to Summary Table

Table 4-2260. Instance Table

Instance Name	Physical Address
QSPI0	4820 0020h

Access Types Legend

Table 4-2261. INTR_STATUS_RAW_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED	RO		Always read as 0
1	WIRQ_RAW	RW	0h	Word Interrupt Status Read indicates raw status0 = inactive1 = activeWriting 1 will set statusWriting 0 has no effect
0	FIRQ_RAW	RW	0h	Frame Interrupt StatusRead indicates raw status0 = inactive1 = activeWriting 1 will set statusWriting 0 has no effect

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4.25.10 MSS_QSPI0_INTR_STATUS_ENABLED_CLEAR Registers

4.25.10.1 QSPI0_INTR_STATUS_ENABLED_CLEAR Register (Offset = 24h) [reset = h]

Short Description: INTR Interrupt Status Enabled/Clear Register

Long Description:

Return to Summary Table

Table 4-2262. Instance Table

Instance Name	Physical Address
QSPI0	4820 0024h

Access Types Legend

Table 4-2263. INTR_STATUS_ENABLED_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED	RO		Always read as 0
1	WIRQ_ENA	RW	0h	Word Interrupt Enabled StatusRead indicates enabled status0 = inactive1 = activeWriting 1 will clear interruptWriting 0 has no effect
0	FIRQ_ENA	RW	0h	Frame Interrupt Enabled StatusRead indicates enabled status0 = inactive1 = activeWriting 1 will clear interruptWriting 0 has no effect

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4.25.11 MSS_QSPI0_INTR_ENABLE_SET Registers

4.25.11.1 QSPI0_INTR_ENABLE_SET Register (Offset = 28h) [reset = h]

Short Description: INTR Interrupt Enable/Set Register

Long Description:

Return to Summary Table

Table 4-2264. Instance Table

Instance Name	Physical Address
QSPI0	4820 0028h

Access Types Legend

Table 4-2265. INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED	RO		Always read as 0
1	WIRQ_ENA_SET	RW	0h	Word Interrupt Enable/SetRead indicates interrupt enable0 = disabled1 = enabledWriting 1 will set interrupt enabledWriting 0 has no effect
0	FIRQ_ENA_SET	RW	0h	Frame Interrupt Enable/SetRead indicates interrupt enable0 = disabled1 = enabledWriting 1 will set interrupt enabledWriting 0 has no effect

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4.25.12 MSS_QSPI0_INTR_ENABLE_CLEAR Registers

4.25.12.1 QSPI0_INTR_ENABLE_CLEAR Register (Offset = 2Ch) [reset = h]

Short Description: INTR Interrupt Enable/Clear Register

Long Description:

Return to Summary Table

Table 4-2266. Instance Table

Instance Name	Physical Address
QSPI0	4820 002Ch

Access Types Legend

Table 4-2267. INTR_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED	RO		Always read as 0
1	WIRQ_ENA_CLR	RW	0h	Word Interrupt Enable/ClearRead indicates interrupt enable0 = disabled1 = enabledWriting 1 will clear interrupt enabledWriting 0 has no effect
0	FIRQ_ENA_CLR	RW	0h	Frame Interrupt Enable/ClearRead indicates interrupt enable0 = disabled1 = enabledWriting 1 will clear interrupt enabledWriting 0 has no effect

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4.25.13 MSS_QSPI0_INTC_EOI Registers

4.25.13.1 QSPI0_INTC_EOI Register (Offset = 30h) [reset = h]

Short Description: EOI Register

Long Description:

Return to Summary Table

Table 4-2268. Instance Table

Instance Name	Physical Address
QSPI0	4820 0030h

Access Types Legend

Table 4-2269. INTC_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	EOI_VECTOR	RW	0h	Number associated with the ipgenericirq for intr output. There are 1 interrupt outputsWrite 0x0 : Write to intr IP GenericAny other write value is ignored.

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4.25.14 MSS_QSPI0_RESERVED7 Registers

4.25.14.1 QSPI0_RESERVED7 Register (Offset = 34h) [reset = h]

Short Description: Reserved

Long Description:

Return to Summary Table

Table 4-2270. Instance Table

Instance Name	Physical Address
QSPI0	4820 0034h

Access Types Legend

Table 4-2271. RESERVED7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_7	RO	0h	Reserved

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4.25.15 MSS_QSPI0_RESERVED8 Registers

4.25.15.1 QSPI0_RESERVED8 Register (Offset = 38h) [reset = h]

Short Description: Reserved

Long Description:

Return to Summary Table

Table 4-2272. Instance Table

Instance Name	Physical Address
QSPI0	4820 0038h

Access Types Legend

Table 4-2273. RESERVED8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_8	RO	0h	Reserved

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4.25.16 MSS_QSPI0_RESERVED9 Registers

4.25.16.1 QSPI0_RESERVED9 Register (Offset = 3Ch) [reset = h]

Short Description: Reserved

Long Description:

Return to Summary Table

Table 4-2274. Instance Table

Instance Name	Physical Address
QSPI0	4820 003Ch

Access Types Legend

Table 4-2275. RESERVED9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED_9	RO	0h	Reserved

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4.25.17 MSS_QSPI0_SPI_CLOCK_CNTRL Registers

4.25.17.1 QSPI0_SPI_CLOCK_CNTRL Register (Offset = 40h) [reset = h]

Short Description: SPI Clock Control Register (SPICC)

Long Description:

Return to Summary Table

Table 4-2276. Instance Table

Instance Name	Physical Address
QSPI0	4820 0040h

Access Types Legend

Table 4-2277. SPI_CLOCK_CNTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CLKEN	RW	0h	Clock Enable. 0- Data clock is turned off1- Data clock is enabled
30 - 16	RESERVED	RO		Always read as 0
15 - 0	DCLK_DIV	RW	0h	Serial data clock divide by ratio

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4.25.18 MSS_QSPI0_SPI_DC Registers

4.25.18.1 QSPI0_SPI_DC Register (Offset = 44h) [reset = h]

Short Description: SPI Data Control Register (SPIDC)

Long Description:

Return to Summary Table

Table 4-2278. Instance Table

Instance Name	Physical Address
QSPI0	4820 0044h

Access Types Legend

Table 4-2279. SPI_DC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED4	RO	0h	Always read as 0
28 - 27	DD3	RW	0h	Data delay for chip select 300- Data is output on the same cycle as the CS_N goes active01- Data is output 1 DCLK cycle after the CS_N goes active 10- Data is output 2 DCLK cycles after the CS_N goes active11- Data is output 3 DCLK cycles after the CS_N goes active
26	CKPH3	RW	0h	Clock phase for chip select 3 If CKP0 = 0 0- Data shifted out on falling edge; input on rising edge 1- Data shifted out on rising edge; input on falling edgeIf CKP0 = 1 1- Data shifted out on falling edge; input on rising edge 0- Data shifted out on rising edge; input on falling edge
25	CSP3	RW	0h	Chip select polarity for chip select 30- Active low1- Active high
24	CKP3	RW	0h	Clock polarity for chip select 30- When data is not being transferred, SCK = 01- When data is not being transferred, SCK = 1
23 - 21	RESERVED3	RO	0h	Always read as 0
20 - 19	DD2	RW	0h	Data delay for chip select 200- Data is output on the same cycle as the CS_N goes active01- Data is output 1 DCLK cycle after the CS_N goes active 10- Data is output 2 DCLK cycles after the CS_N goes active11- Data is output 3 DCLK cycles after the CS_N goes active
18	CKPH2	RW	0h	Clock phase for chip select 2. If CKP0 = 0 0- Data shifted out on falling edge; input on rising edge 1- Data shifted out on rising edge; input on falling edgeIf CKP0 = 1 1- Data shifted out on falling edge; input on rising edge 0- Data shifted out on rising edge; input on falling edge
17	CSP2	RW	0h	Chip select polarity for chip select 20- Active low1- Active high
16	CKP2	RW	0h	Clock polarity for chip select 20- When data is not being transferred, SCK = 01- When data is not being transferred, SCK = 1
15 - 13	RESERVED2	RO	0h	Always read as 0
12 - 11	DD1	RW	0h	Data delay for chip select 100- Data is output on the same cycle as the CS_N goes active01- Data is output 1 DCLK cycle after the CS_N goes active 10- Data is output 2 DCLK cycles after the CS_N goes active11- Data is output 3 DCLK cycles after the CS_N goes active
10	CKPH1	RW	0h	Clock phase for chip select 1. If CKP0 = 0 0- Data shifted out on falling edge; input on rising edge 1- Data shifted out on rising edge; input on falling edgeIf CKP0 = 1 1- Data shifted out on falling edge; input on rising edge 0- Data shifted out on rising edge; input on falling edge
9	CSP1	RW	0h	Chip select polarity for chip select 10- Active low1- Active high
8	CKP1	RW	0h	Clock polarity for chip select 10- When data is not being transferred, SCK = 01- When data is not being transferred, SCK = 1

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Table 4-2279. SPI_DC Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7 - 5	RESERVED1	RO	0h	Always read as 0
4 - 3	DD0	RW	0h	Data delay for chip select 000- Data is output on the same cycle as the CS_N goes active01- Data is output 1 DCLK cycle after the CS_N goes active 10- Data is output 2 DCLK cycles after the CS_N goes active11- Data is output 3 DCLK cycles after the CS_N goes active
2	CKPH0	RW	0h	Clock phase for chip select 0. If CKP0 = 0 0- Data shifted out on falling edge; input on rising edge 1- Data shifted out on rising edge; input on falling edgeIf CKP0 = 1 1- Data shifted out on falling edge; input on rising edge 0- Data shifted out on rising edge; input on falling edge
1	CSP0	RW	0h	Chip select polarity for chip select 00- Active low1- Active high
0	CKP0	RW	0h	Clock polarity for chip select 00- When data is not being transferred, SCK = 01- When data is not being transferred, SCK = 1

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4.25.19 MSS_QSPI0_SPI_CMD Registers

4.25.19.1 QSPI0_SPI_CMD Register (Offset = 48h) [reset = h]

Short Description: SPI Command Register (SPICR)

Long Description:

Return to Summary Table

Table 4-2280. Instance Table

Instance Name	Physical Address
QSPI0	4820 0048h

Access Types Legend

Table 4-2281. SPI_CMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	RESERVED3	RO	0h	Always read as 0
29 - 28	CSNUM	RW	0h	Device select. Sets the active chip select for the transfer00- Chip Select 0 active01- Chip Select 1 active10- Chip Select 2 active11- Chip Select 3 active
27 - 26	RESERVED2	RO	0h	Always read as 0
25 - 19	WLEN	RW	0h	Word length. Sets the size of the individual transfers from 1 ? 128 bits0- 1 bit1- 2 bits?127 ? 128 bits
18 - 16	CMD	RW	0h	Transfer command000- Reserved001- 4 pin Read Single 010- 4 pin Write Single011- 4 pin Read Dual100 ? Reserved101 ? 3 pin Read Single110 ? 3 pin Write Single 111 ? 6 pin Read Quad
15	FIRQ	RW	0h	Frame count interrupt enable
14	WIRQ	RW	0h	Word count interrupt enable
13 - 12	RESERVED1	RO	0h	Always read as 0
11 - 0	FLEN	RW	0h	Frame Length0- 1 word1- 2 words?4095 ? 4096 words

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4.25.20 MSS_QSPI0_SPI_STATUS Registers

4.25.20.1 QSPI0_SPI_STATUS Register (Offset = 4Ch) [reset = h]

Short Description: SPI Status Register (SPISR)

Long Description:

Return to Summary Table

Table 4-2282. Instance Table

Instance Name	Physical Address
QSPI0	4820 004Ch

Access Types Legend

Table 4-2283. SPI_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 28	RESERVED2	RO	0h	Always read as 0
27 - 16	WDCNT	RO	0h	Word count. This field will reflect the 1-4096 words transferred
15 - 3	RESERVED1	RO	0h	Always read as 0
2	FC	RO	0h	Frame complete. This bit is set after all of the requested words have been transmitted.0- Transfer is not complete1- Transfer is completeThis bit is reset when the SPI Status Register is read
1	WC	RO	0h	Word complete. This bit is set after each word transfer is completed.0- Word transfer is not complete1- Word transfer is completeThis bit is reset when the SPI Status Register is read
0	BUSY	RO	0h	Busy bit. Active transfer in progress. This bit is only set during an active word transfer. Between words, the bit will clear to signal that it is ok to read/write the data registers.0- Idle1- Busy

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4.25.21 MSS_QSPI0_SPI_DATA Registers

4.25.21.1 QSPI0_SPI_DATA Register (Offset = 50h) [reset = h]

Short Description: SPI Data Register (SPIDR)

Long Description:

Return to Summary Table

Table 4-2284. Instance Table

Instance Name	Physical Address
QSPI0	4820 0050h

Access Types Legend

Table 4-2285. SPI_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DATA	RW	0h	Data register for read and write operations

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4.25.22 MSS_QSPI0_SPI_SETUP0 Registers

4.25.22.1 QSPI0_SPI_SETUP0 Register (Offset = 54h) [reset = h]

Short Description: Memory Mapped SPI Setup0 Register

Long Description:

Return to Summary Table

Table 4-2286. Instance Table

Instance Name	Physical Address
QSPI0	4820 0054h

Access Types Legend

Table 4-2287. SPI_SETUP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED2	RO	0h	Always read as 0
28 - 24	NUM_D_BITS	RW	0h	Number of dummy bits to use if NUM_D_BYTES = 0
23 - 16	WCMD	RW	Ah	Write Command
15 - 14	RESERVED1	RO	0h	Always read as 0
13 - 12	READ_TYPE	RW	0h	Determines if the read command is a single, dual or quad read mode command00 ? Normal read (all data input on spi_din)01 ? Dual read (odd bytes input on spi_din; even on spi_dout)10 ? Normal read (all data input on spi_din)11 ? Quad read (uses spi_qdin0/1)
11 - 10	NUM_D_BYTES	RW	0h	Number of dummy bytes to be used for fast read. 0 = use the value in NUM_D_BITS1 = use 8 bits; 2 = use 16 bits; 3 = use 24 bits
9 - 8	NUM_A_BYTES	RW	Ah	Number of address bytes to be sent. 0 = 1 byte; 1 = 2 bytes; 2 = 3 bytes; 3 = 4 bytes
7 - 0	RCMD	RW	Bh	Read Command

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4.25.23 MSS_QSPI0_SPI_SETUP1 Registers

4.25.23.1 QSPI0_SPI_SETUP1 Register (Offset = 58h) [reset = h]

Short Description: Memory Mapped SPI Setup1 Register

Long Description:

Return to Summary Table

Table 4-2288. Instance Table

Instance Name	Physical Address
QSPI0	4820 0058h

Access Types Legend

Table 4-2289. SPI_SETUP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED2	RO	0h	Always read as 0
28 - 24	NUM_D_BITS	RW	0h	Number of dummy bits to use if NUM_D_BYTES = 0
23 - 16	WCMD	RW	Ah	Write Command
15 - 14	RESERVED1	RO	0h	Always read as 0
13 - 12	READ_TYPE	RW	0h	Determines if the read command is a single, dual or quad read mode command00 ? Normal read (all data input on spi_din)01 ? Dual read (odd bytes input on spi_din; even on spi_dout)10 ? Normal read (all data input on spi_din)11 ? Quad read (uses spi_qdin0/1)
11 - 10	NUM_D_BYTES	RW	0h	Number of dummy bytes to be used for fast read. 0 = use the value in NUM_D_BITS1 = use 8 bits; 2 = use 16 bits; 3 = use 24 bits
9 - 8	NUM_A_BYTES	RW	Ah	Number of address bytes to be sent. 0 = 1 byte; 1 = 2 bytes; 2 = 3 bytes; 3 = 4 bytes
7 - 0	RCMD	RW	Bh	Read Command

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4.25.24 MSS_QSPI0_SPI_SETUP2 Registers

4.25.24.1 QSPI0_SPI_SETUP2 Register (Offset = 5Ch) [reset = h]

Short Description: Memory Mapped SPI Setup2 Register

Long Description:

Return to Summary Table

Table 4-2290. Instance Table

Instance Name	Physical Address
QSPI0	4820 005Ch

Access Types Legend

Table 4-2291. SPI_SETUP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED2	RO	0h	Always read as 0
28 - 24	NUM_D_BITS	RW	0h	Number of dummy bits to use if NUM_D_BYTES = 0
23 - 16	WCMD	RW	Ah	Write Command
15 - 14	RESERVED1	RO	0h	Always read as 0
13 - 12	READ_TYPE	RW	0h	Determines if the read command is a single, dual or quad read mode command00 ? Normal read (all data input on spi_din)01 ? Dual read (odd bytes input on spi_din; even on spi_dout)10 ? Normal read (all data input on spi_din)11 ? Quad read (uses spi_qdin0/1)
11 - 10	NUM_D_BYTES	RW	0h	Number of dummy bytes to be used for fast read. 0 = use the value in NUM_D_BITS1 = use 8 bits; 2 = use 16 bits; 3 = use 24 bits
9 - 8	NUM_A_BYTES	RW	Ah	Number of address bytes to be sent. 0 = 1 byte; 1 = 2 bytes; 2 = 3 bytes; 3 = 4 bytes
7 - 0	RCMD	RW	Bh	Read Command

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4.25.25 MSS_QSPI0_SPI_SETUP3 Registers

4.25.25.1 QSPI0_SPI_SETUP3 Register (Offset = 60h) [reset = h]

Short Description: Memory Mapped SPI Setup3 Register

Long Description:

Return to Summary Table

Table 4-2292. Instance Table

Instance Name	Physical Address
QSPI0	4820 0060h

Access Types Legend

Table 4-2293. SPI_SETUP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 29	RESERVED2	RO	0h	Always read as 0
28 - 24	NUM_D_BITS	RW	0h	Number of dummy bits to use if NUM_D_BYTES = 0
23 - 16	WCMD	RW	Ah	Write Command
15 - 14	RESERVED1	RO	0h	Always read as 0
13 - 12	READ_TYPE	RW	0h	Determines if the read command is a single, dual or quad read mode command00 ? Normal read (all data input on spi_din)01 ? Dual read (odd bytes input on spi_din; even on spi_dout)10 ? Normal read (all data input on spi_din)11 ? Quad read (uses spi_qdin0/1)
11 - 10	NUM_D_BYTES	RW	0h	Number of dummy bytes to be used for fast read. 0 = use the value in NUM_D_BITS1 = use 8 bits; 2 = use 16 bits; 3 = use 24 bits
9 - 8	NUM_A_BYTES	RW	Ah	Number of address bytes to be sent. 0 = 1 byte; 1 = 2 bytes; 2 = 3 bytes; 3 = 4 bytes
7 - 0	RCMD	RW	Bh	Read Command

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4.25.26 MSS_QSPI0_SPI_SWITCH Registers

4.25.26.1 QSPI0_SPI_SWITCH Register (Offset = 64h) [reset = h]

Short Description: Memory Mapped SPI Switch Register

Long Description:

Return to Summary Table

Table 4-2294. Instance Table

Instance Name	Physical Address
QSPI0	4820 0064h

Access Types Legend

Table 4-2295. SPI_SWITCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED	RO		Always read as 0
1	MM_INT_EN	RW	0h	Memory Mapped mode interrupt enable.0 ? Interrupts are disabled during memory mapped operations1 ? Word Count interrupt is enabled for memory mapped operations
0	MMPT_S	RW	0h	MMPT select. If 0 (default) config port has is selected to control config of core SPI module. If 1, Memory Mapped Protocol Translator is selected to control config port of core SPI module.

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4.25.27 MSS_QSPI0_SPI_DATA1 Registers

4.25.27.1 QSPI0_SPI_DATA1 Register (Offset = 68h) [reset = h]

Short Description: SPI Data Register (SPIDR1)

Long Description:

Return to Summary Table

Table 4-2296. Instance Table

Instance Name	Physical Address
QSPI0	4820 0068h

Access Types Legend

Table 4-2297. SPI_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DATA	RW	0h	Data register for read and write operations

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4.25.28 MSS_QSPI0_SPI_DATA2 Registers

4.25.28.1 QSPI0_SPI_DATA2 Register (Offset = 6Ch) [reset = h]

Short Description: SPI Data Register (SPIDR2)

Long Description:

Return to Summary Table

Table 4-2298. Instance Table

Instance Name	Physical Address
QSPI0	4820 006Ch

Access Types Legend

Table 4-2299. SPI_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DATA	RW	0h	Data register for read and write operations

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4.25.29 MSS_QSPI0_SPI_DATA3 Registers

4.25.29.1 QSPI0_SPI_DATA3 Register (Offset = 70h) [reset = h]

Short Description: SPI Data Register (SPIDR3)

Long Description:

Return to Summary Table

Table 4-2300. Instance Table

Instance Name	Physical Address
QSPI0	4820 0070h

Access Types Legend

Table 4-2301. SPI_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DATA	RW	0h	Data register for read and write operations

4.25.30 Access Table

Table 4-2302. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

4.26 RTI Registers

Table 4-2303. MSS_RTI[0:2] Registers Base Address Table

Offset	Length	Acronym	MSS_RTI0 Physical Address	MSS_RTI1 Physical Address	MSS_RTI2 Physical Address
0h	32	RTI_RTIGCTRL	5218 0000h	5218 1000h	5218 2000h
4h	32	RTI_RTITBCTRL	5218 0004h	5218 1004h	5218 2004h
8h	32	RTI_RTICAPCTRL	5218 0008h	5218 1008h	5218 2008h
Ch	32	RTI_RTICOMPCTRL	5218 000Ch	5218 100Ch	5218 200Ch
10h	32	RTI_RTIFRC0	5218 0010h	5218 1010h	5218 2010h
14h	32	RTI_RTIUC0	5218 0014h	5218 1014h	5218 2014h
18h	32	RTI_RTICPUC0	5218 0018h	5218 1018h	5218 2018h
20h	32	RTI_RTICAFRC0	5218 0020h	5218 1020h	5218 2020h
24h	32	RTI_RTICAUC0	5218 0024h	5218 1024h	5218 2024h
30h	32	RTI_RTIFRC1	5218 0030h	5218 1030h	5218 2030h
34h	32	RTI_RTIUC1	5218 0034h	5218 1034h	5218 2034h
38h	32	RTI_RTICPUC1	5218 0038h	5218 1038h	5218 2038h
40h	32	RTI_RTICAFRC1	5218 0040h	5218 1040h	5218 2040h
44h	32	RTI_RTICAUC1	5218 0044h	5218 1044h	5218 2044h
50h	32	RTI_RTICOMP0	5218 0050h	5218 1050h	5218 2050h
54h	32	RTI_RTIUDCP0	5218 0054h	5218 1054h	5218 2054h
58h	32	RTI_RTICOMP1	5218 0058h	5218 1058h	5218 2058h
5Ch	32	RTI_RTIUDCP1	5218 005Ch	5218 105Ch	5218 205Ch
60h	32	RTI_RTICOMP2	5218 0060h	5218 1060h	5218 2060h
64h	32	RTI_RTIUDCP2	5218 0064h	5218 1064h	5218 2064h
68h	32	RTI_RTICOMP3	5218 0068h	5218 1068h	5218 2068h
6Ch	32	RTI_RTIUDCP3	5218 006Ch	5218 106Ch	5218 206Ch

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Table 4-2303. MSS_RTI[0:2] Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_RTI0 Physical Address	MSS_RTI1 Physical Address	MSS_RTI2 Physical Address
70h	32	RTI_RTITBLCOMP	5218 0070h	5218 1070h	5218 2070h
74h	32	RTI_RTITBHCOMP	5218 0074h	5218 1074h	5218 2074h
80h	32	RTI_RTISETINT	5218 0080h	5218 1080h	5218 2080h
84h	32	RTI_RTICLEARINT	5218 0084h	5218 1084h	5218 2084h
88h	32	RTI_RTIINTFLAG	5218 0088h	5218 1088h	5218 2088h
90h	32	RTI_RTIDWDCTRL	5218 0090h	5218 1090h	5218 2090h
94h	32	RTI_RTIDWDPRLD	5218 0094h	5218 1094h	5218 2094h
98h	32	RTI_RTIWDSTATUS	5218 0098h	5218 1098h	5218 2098h
9Ch	32	RTI_RTIWDKEY	5218 009Ch	5218 109Ch	5218 209Ch
A0h	32	RTI_RTIDWDCNTR	5218 00A0h	5218 10A0h	5218 20A0h
A4h	32	RTI_RTIWWDRXNCTRL	5218 00A4h	5218 10A4h	5218 20A4h
A8h	32	RTI_RTIWWDSIZECTRL	5218 00A8h	5218 10A8h	5218 20A8h
ACh	32	RTI_RTIINTCLRENABLE	5218 00ACh	5218 10ACh	5218 20ACh
B0h	32	RTI_RTICOMP0CLR	5218 00B0h	5218 10B0h	5218 20B0h
B4h	32	RTI_RTICOMP1CLR	5218 00B4h	5218 10B4h	5218 20B4h
B8h	32	RTI_RTICOMP2CLR	5218 00B8h	5218 10B8h	5218 20B8h
BCh	32	RTI_RTICOMP3CLR	5218 00BCh	5218 10BCh	5218 20BCh

Table 4-2304. MSS_RTI3 Registers Base Address Table

Offset	Length	Acronym	MSS_RTI3 Physical Address
0h	32	RTI_RTIGCTRL	5218 3000h
4h	32	RTI_RTITBCTRL	5218 3004h
8h	32	RTI_RTICAPCTRL	5218 3008h
Ch	32	RTI_RTICOMPCTRL	5218 300Ch
10h	32	RTI_RTIFRC0	5218 3010h
14h	32	RTI_RTIUC0	5218 3014h
18h	32	RTI_RTICPUC0	5218 3018h
20h	32	RTI_RTICAFRC0	5218 3020h
24h	32	RTI_RTICAUC0	5218 3024h
30h	32	RTI_RTIFRC1	5218 3030h
34h	32	RTI_RTIUC1	5218 3034h
38h	32	RTI_RTICPUC1	5218 3038h
40h	32	RTI_RTICAFRC1	5218 3040h
44h	32	RTI_RTICAUC1	5218 3044h
50h	32	RTI_RTICOMP0	5218 3050h
54h	32	RTI_RTIUDCP0	5218 3054h
58h	32	RTI_RTICOMP1	5218 3058h
5Ch	32	RTI_RTIUDCP1	5218 305Ch
60h	32	RTI_RTICOMP2	5218 3060h
64h	32	RTI_RTIUDCP2	5218 3064h
68h	32	RTI_RTICOMP3	5218 3068h
6Ch	32	RTI_RTIUDCP3	5218 306Ch
70h	32	RTI_RTITBLCOMP	5218 3070h
74h	32	RTI_RTITBHCOMP	5218 3074h
80h	32	RTI_RTISETINT	5218 3080h
84h	32	RTI_RTICLEARINT	5218 3084h

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Table 4-2304. MSS_RTI3 Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_RTI3 Physical Address
88h	32	RTI_RTIINTFLAG	5218 3088h
90h	32	RTI_RTIDWDCTRL	5218 3090h
94h	32	RTI_RTIDWDPRLD	5218 3094h
98h	32	RTI_RTIWDSTATUS	5218 3098h
9Ch	32	RTI_RTIWDKEY	5218 309Ch
A0h	32	RTI_RTIDWDCNTR	5218 30A0h
A4h	32	RTI_RTIWWDRXNCTRL	5218 30A4h
A8h	32	RTI_RTIWWDSIZECTRL	5218 30A8h
ACh	32	RTI_RTIINTCLRENABLE	5218 30ACh
B0h	32	RTI_RTICOMP0CLR	5218 30B0h
B4h	32	RTI_RTICOMP1CLR	5218 30B4h
B8h	32	RTI_RTICOMP2CLR	5218 30B8h
BCh	32	RTI_RTICOMP3CLR	5218 30BCh

4.26.1 RTI Instance Count Note

Note

n = 0 to 3 for the RTI registers defined below.

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4.26.2 MSS_RTIn_RTIGCTRL Registers

4.26.2.1 RTIn_RTIGCTRL Register (Offset = 0h) [reset = h]

Short Description: Global Control Register starts / stops the counters

Long Description:

Return to Summary Table

Table 4-2305. Instance Table

Instance Name	Physical Address
RTI0	5218 0000h
RTI1	5218 1000h
RTI2	5218 2000h
RTI3	5218 3000h

Access Types Legend

Table 4-2306. RTIGCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 20	RESERVED2	RW	0h	Reserved.Reads return 0 and writes have no effect
19 - 16	NTUSEL	RW	0h	NTUSEL: Select NTU signal.These bits determine which NTU input signal is used as external timebase. There are up to four inputs supported with four valid selection combinations. Any invalid selection value written to the NTUSEL bit-field will result in a TIED LOW being used as the NTU signal. The NTU signal will also be TIED LOW in case of a single-bit flip as it will result in an invalid combination of NTUSEL.User and privilege mode (read):0000 = NTU00101 = NTU11010 = NTU21111 = NTU3other = tied to ?0? Privilege mode (write):0000 = NTU00101 = NTU11010 = NTU21111 = NTU3other = tied to ?0?
15	COS	RW	0h	COS: Continue On Suspend.This bit determines if both counters are stopped when the device goes into debug mode or if they continue counting.User and privilege mode (read):0 = counters are stopped while in debug mode1 = counters are running while in debug modePrivilege mode (write):0 = stop counters in debug mode1 = continue counting in debug mode
14 - 2	RESERVED1	RW	0h	Reserved.Reads return 0 and writes have no effect
1	CNT1EN	RW	0h	CNT1EN: Counter 1 Enable. The CNT1EN bit starts and stops the operation of counter block 1 (UC1 and FRC1).User and privilege mode (read):0 = counters are stopped1 = counters are runningPrivilege mode (write):0 = stop counters1 = start countersGives the absolute 32 bit destination address (physical).
0	CNT0EN	RW	0h	CNT0EN: Counter 0 Enable.The CNT0EN bit starts and stops the operation of counter block 0 (UC0 and FRC0).User and privilege mode (read):0 = counters are stopped1 = counters are runningPrivilege mode (write):0 = stop counters1 = start countersGives the absolute 32 bits source address (physical).

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4.26.3 MSS_RTIn_RTITBCTRL Registers

4.26.3.1 RTIn_RTITBCTRL Register (Offset = 4h) [reset = h]

Short Description: Timebase Control selection which source triggers free running counter 0

Long Description:

Return to Summary Table

Table 4-2307. Instance Table

Instance Name	Physical Address
RTI0	5218 0004h
RTI1	5218 1004h
RTI2	5218 2004h
RTI3	5218 3004h

Access Types Legend

Table 4-2308. RTITBCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED3	RW	0h	Reserved
1	INC	RW	0h	INC: Increment Free Running Counter 0.This bit determines wether the Free Running Counter 0 is automatically incremented if a failing clock on the NTUx signal is detected.User and privilege mode (read):0 = FRC0 will not be incremented1 = FRC0 will be incrementedPrivilege mode (write):0 = Do not increment FRC0 on failing external clock1 = Increment FRC0 on failing external clock
0	TBEXT	RW	0h	TBEXT: Timebase External.The Timebase External bit selects whether the Free Running Counter 0 is clocked by the internal Up Counter 0 or from the external signal NTUx. Since setting the TBEXT bit to 1 resets Up Counter 0, Free Running Counter 0 will not be incremented in this occurence. The only source which is able to increment Free Running Counter 0 is NTUx.When the Timebase Supervisor circuit detects a missing clockedge, then the TBEXT bit is reset.The selection if the external signal should be used, can only be done by software.User and privilege mode (read):0 = UC0 clocks FRC01 = NTUx clocks FRC0Privilege mode (write):0 = MUX is switched to internal UC0 clocking scheme1 = MUX is switched to external NTUx clocking scheme

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4.26.4 MSS_RTIn_RTICAPCTRL Registers

4.26.4.1 RTIn_RTICAPCTRL Register (Offset = 8h) [reset = h]

Short Description: Capture Control controls the capture source for the counters

Long Description:

Return to Summary Table

Table 4-2309. Instance Table

Instance Name	Physical Address
RTI0	5218 0008h
RTI1	5218 1008h
RTI2	5218 2008h
RTI3	5218 3008h

Access Types Legend

Table 4-2310. RTICAPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RESERVED4	RW	0h	Reserved.Reads return 0 and writes have no effect
1	CAPCNTR1	RW	0h	CAPCNTR1: Capture Counter 1.This bit determines, which external interrupt source triggers a capture event of both UC1 and FRC1.User and privilege mode (read):0 = capture event is triggered by Capture Event Source 01 = capture event is triggered by Capture Event Source 1Privilege mode (write):0 = enable capture event triggered by Capture Event Source 01 = enable capture event triggered by Capture Event Source 1
0	CAPCNTR0	RW	0h	CAPCNTR0: Capture Counter 0.This bit determines, which external interrupt source triggers a capture event of both UC0 and FRC0.User and privilege mode (read):0 = capture event is triggered by Capture Event Source 01 = capture event is triggered by Capture Event Source 1Privilege mode (write):0 = enable capture event triggered by Capture Event Source 01 = enable capture event triggered by Capture Event Source 111 indexed10 reserved01 post-increment00 constant

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4.26.5 MSS_RTIn_RTICOMPCTRL Registers

4.26.5.1 RTIn_RTICOMPCTRL Register (Offset = Ch) [reset = h]

Short Description: Compare Control controls the source for the compare registers

Long Description:

Return to Summary Table

Table 4-2311. Instance Table

Instance Name	Physical Address
RTI0	5218 000Ch
RTI1	5218 100Ch
RTI2	5218 200Ch
RTI3	5218 300Ch

Access Types Legend

Table 4-2312. RTICOMPCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 13	RESERVED8	RW	0h	Reserved.Reads return 0 and writes have no effect
12	COMP3SEL	RW	0h	COMPSEL3: Compare Select 3.This bit determines the counter with which the compare value hold in compare register 3 is compared.User and privilege mode (read):0 = value will be compared with FRC 01 = value will be compared with FRC 1Privilege mode (write):0 = enable compare with FRC 01 = enable compare with FRC 1
11 - 9	RESERVED7	RW	0h	Reserved.Reads return 0 and writes have no effect
8	COMP2SEL	RW	0h	COMPSEL2: Compare Select 2.This bit determines the counter with which the compare value hold in compare register 2 is compared.User and privilege mode (read):0 = value will be compared with FRC 01 = value will be compared with FRC 1Privilege mode (write):0 = enable compare with FRC 01 = enable compare with FRC 1
7 - 5	RESERVED6	RW	0h	Reserved.Reads return 0 and writes have no effect
4	COMP1SEL	RW	0h	COMPSEL1: Compare Select 1.This bit determines the counter with which the compare value hold in compare register 1 is compared. User and privilege mode (read):0 = value will be compared with FRC 01 = value will be compared with FRC 1Privilege mode (write):0 = enable compare with FRC 01 = enable compare with FRC 1
3 - 1	RESERVED5	RW	0h	Reserved.Reads return 0 and writes have no effect
0	COMP0SEL	RW	0h	COMPSEL0: Compare Select 0.This bit determines the counter with which the compare value hold in compare register 0 is compared.User and privilege mode (read):0 = value will be compared with FRC 01 = value will be compared with FRC 1Privilege mode (write):0 = enable compare with FRC 01 = enable compare with FRC 1

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4.26.6 MSS_RTIn_RTIFRC0 Registers

4.26.6.1 RTIn_RTIFRC0 Register (Offset = 10h) [reset = h]

Short Description: Free Running Counter 0 current value of free running counter 0

Long Description:

Return to Summary Table

Table 4-2313. Instance Table

Instance Name	Physical Address
RTI0	5218 0010h
RTI1	5218 1010h
RTI2	5218 2010h
RTI3	5218 3010h

Access Types Legend

Table 4-2314. RTIFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FRC0	RW	0h	FRC0: Free Running Counter 0.This registers holds the current value of the Free Running Counter 0 and will be updated continuously.User and privilege mode (read):current value of the counterPrivilege mode (write):The counter can be preset by writing to this register. The counter increments then from this written value upwards.Note: Presetting countersIf counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0.

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4.26.7 MSS_RTIn_RTIUC0 Registers

4.26.7.1 RTIn_RTIUC0 Register (Offset = 14h) [reset = h]

Short Description: Up Counter 0 current value of prescale counter 0

Long Description:

Return to Summary Table

Table 4-2315. Instance Table

Instance Name	Physical Address
RTI0	5218 0014h
RTI1	5218 1014h
RTI2	5218 2014h
RTI3	5218 3014h

Access Types Legend

Table 4-2316. RTIUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UC0	RW	0h	UC0: Up Counter 0.This registers holds the current value of the Up Counter 0 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 0. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 0 and Free Running Counter 0.User and privilege mode (read):value of the counter when the Free Running Counter 0 was readPrivilege mode (write):the counter can be preset by writing to this register. The counter increments then from this written value upwards.Note: Presetting countersIf counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0.Note: Preset value concernIf the preset value is bigger than the compare value stored in register RTICPUC0 then it can take a long time until a compare matches, since RTIUC0 has to count up until it overflows.

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4.26.8 MSS_RTIn_RTICPUC0 Registers

4.26.8.1 RTIn_RTICPUC0 Register (Offset = 18h) [reset = h]

Short Description: Compare Up Counter 0 compare value compared with prescale counter 0

Long Description:

Return to Summary Table

Table 4-2317. Instance Table

Instance Name	Physical Address
RTI0	5218 0018h
RTI1	5218 1018h
RTI2	5218 2018h
RTI3	5218 3018h

Access Types Legend

Table 4-2318. RTICPUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CPUC0	RW	0h	This registers holds the compare value, which is compared with the Up Counter 0. When the compare matches, Free Running counter 0 is incremented. The Up Counter is set to zero when the counter value matches the CPUC0 value. The value set in this prescales the RTI clock.If CPUC0 = 0: then, frequency = RTICLK/ (2^32)If CPUC0 ? 0: then , frequency = RTICLK/(CPUC0 + 1)User and privilege mode (read):current compare valuePrivilege mode (write when TBEXT = 0):the compare value is updatedPrivilege mode (write when TBEXT = 1):the compare value is not changed

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4.26.9 MSS_RTIn_RTICAFRC0 Registers

4.26.9.1 RTIn_RTICAFRC0 Register (Offset = 20h) [reset = h]

Short Description: Capture Free Running Counter 0 current value of free running counter 0 on external event

Long Description:

Return to Summary Table

Table 4-2319. Instance Table

Instance Name	Physical Address
RTI0	5218 0020h
RTI1	5218 1020h
RTI2	5218 2020h
RTI3	5218 3020h

Access Types Legend

Table 4-2320. RTICAFRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAFRC0	RW	0h	CAFRC0: Capture Free Running Counter 0.This registers captures the current value of the Free Running Counter 0 when a event occurs, controlled by the external capture control block.User and privilege mode (read):value of Free Running Counter 0 on a capture event

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4.26.10 MSS_RTIn_RTICAUC0 Registers

4.26.10.1 RTIn_RTICAUC0 Register (Offset = 24h) [reset = h]

Short Description: Capture Up Counter 0 current value of prescale counter 0 on external event

Long Description:

Return to Summary Table

Table 4-2321. Instance Table

Instance Name	Physical Address
RTI0	5218 0024h
RTI1	5218 1024h
RTI2	5218 2024h
RTI3	5218 3024h

Access Types Legend

Table 4-2322. RTICAUC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAUC0	RW	0h	CAUC0: Capture Up Counter 0.This registers captures the current value of the Up Counter 0 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 0 and Free Running Counter 0. So the RTICAFRC0 register has to be read first, before the RTICAUC0 register is read. This sequence ensures that the value of the RTICAUC0 register is the corresponding value to the RTICAFRC0 register, even if another capture event happens in between the two reads.User and privilege mode (read):value of Up Counter 0 on a capture event

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4.26.11 MSS_RTIn_RTIFRC1 Registers

4.26.11.1 RTIn_RTIFRC1 Register (Offset = 30h) [reset = h]

Short Description: Free Running Counter 1 current value of free running counter 1

Long Description:

Return to Summary Table

Table 4-2323. Instance Table

Instance Name	Physical Address
RTI0	5218 0030h
RTI1	5218 1030h
RTI2	5218 2030h
RTI3	5218 3030h

Access Types Legend

Table 4-2324. RTIFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	FRC1	RW	0h	FRC1: Free Running Counter 1.This registers holds the current value of the Free Running Counter 1 and will be updated continuously.User and privilege mode (read):current value of the counterPrivilege mode (write):The counter can be preset by writing to this register. The counter increments then from this written value upwards.Note: Presetting countersIf counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1.

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4.26.12 MSS_RTIn_RTIUC1 Registers

4.26.12.1 RTIn_RTIUC1 Register (Offset = 34h) [reset = h]

Short Description: Up Counter 1 current value of prescale counter 1

Long Description:

Return to Summary Table

Table 4-2325. Instance Table

Instance Name	Physical Address
RTI0	5218 0034h
RTI1	5218 1034h
RTI2	5218 2034h
RTI3	5218 3034h

Access Types Legend

Table 4-2326. RTIUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UC1	RW	0h	UC1: Up Counter 1.This registers holds the current value of the Up Counter 1 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 1. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 1 and Free Running Counter 1.User and privilege mode (read):value of the counter when the Free Running Counter 1 was readPrivilege mode (write):the counter can be preset by writing to this register. The counter increments then from this written value upwards.Note: Presetting countersIf counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1.Note: Preset value concernIf the preset value is bigger than the compare value stored in register RTICPUC1 then it can take a long time until a compare matches, since RTIUC1 has to count up until it overflows.

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4.26.13 MSS_RTIn_RTICPUC1 Registers

4.26.13.1 RTIn_RTICPUC1 Register (Offset = 38h) [reset = h]

Short Description: Compare Up Counter 1 compare value compared with prescale counter 1

Long Description:

Return to Summary Table

Table 4-2327. Instance Table

Instance Name	Physical Address
RTI0	5218 0038h
RTI1	5218 1038h
RTI2	5218 2038h
RTI3	5218 3038h

Access Types Legend

Table 4-2328. RTICPUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CPUC1	RW	0h	This registers holds the compare value, which is compared with the Up Counter 1. When the compare matches, Free Running Counter 1 is incremented. The Up Counter is set to zero when the counter value matches the CPUC1 value. The value set in this prescales the RTI clock.If CPUC1 = 0: then, frequency = RTICLK/ (2^32)If CPUC1 ? 0: then , frequency = RTICLK/(CPUC1 + 1)User and privilege mode (read):current compare valuePrivilege mode (write when TBEXT = 0):the compare value is updatedPrivilege mode (write when TBEXT = 1):the compare value is not changed

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4.26.14 MSS_RTIn_RTICAFRC1 Registers

4.26.14.1 RTIn_RTICAFRC1 Register (Offset = 40h) [reset = h]

Short Description: Capture Free Running Counter 1 current value of free running counter 1 on external event

Long Description:

Return to Summary Table

Table 4-2329. Instance Table

Instance Name	Physical Address
RTI0	5218 0040h
RTI1	5218 1040h
RTI2	5218 2040h
RTI3	5218 3040h

Access Types Legend

Table 4-2330. RTICAFRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAFRC1	RW	0h	CAFRC1: Capture Free Running Counter 1.This registers captures the current value of the Free Running Counter 1 when a event occurs, controlled by the external capture control block.User and privilege mode (read):value of Free Running Counter 1 on a capture event

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4.26.15 MSS_RTIn_RTICAUC1 Registers

4.26.15.1 RTIn_RTICAUC1 Register (Offset = 44h) [reset = h]

Short Description: Capture Up Counter 1 current value of prescale counter 1 on external event

Long Description:

Return to Summary Table

Table 4-2331. Instance Table

Instance Name	Physical Address
RTI0	5218 0044h
RTI1	5218 1044h
RTI2	5218 2044h
RTI3	5218 3044h

Access Types Legend

Table 4-2332. RTICAUC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	CAUC1	RW	0h	CAUC1: Capture Up Counter 1.This registers captures the current value of the Up Counter 1 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 1 and Free Running Counter 1. So the RTICAFRC1 register has to be read first, before the RTICAUC1 register is read. This sequence ensures that the value of the RTICAUC1 register is the corresponding value to the RTICAFRC1 register, even if another capture event happens in between the two reads.User and privilege mode (read):value of Up Counter 1 on a capture event

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4.26.16 MSS_RTIn_RTICOMP0 Registers

4.26.16.1 RTIn_RTICOMP0 Register (Offset = 50h) [reset = h]

Short Description: Compare 0 compare value to be compared with the counters

Long Description:

Return to Summary Table

Table 4-2333. Instance Table

Instance Name	Physical Address
RTI0	5218 0050h
RTI1	5218 1050h
RTI2	5218 2050h
RTI3	5218 3050h

Access Types Legend

Table 4-2334. RTICOMP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP0	RW	0h	COMP0: Compare 0.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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4.26.17 MSS_RTIn_RTIUDCP0 Registers

4.26.17.1 RTIn_RTIUDCP0 Register (Offset = 54h) [reset = h]

Short Description: Update Compare 0 value to be added to the compare register 0 value on compare match

Long Description:

Return to Summary Table

Table 4-2335. Instance Table

Instance Name	Physical Address
RTI0	5218 0054h
RTI1	5218 1054h
RTI2	5218 2054h
RTI3	5218 3054h

Access Types Legend

Table 4-2336. RTIUDCP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UDCP0	RW	0h	UDCP0: Update Compare 0 Register.This registers holds a value, which is added to the value in the compare 0 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.User and privilege mode (read):value to be added to the compare 0 register on the next compare matchPrivilege mode (write):new update value

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4.26.18 MSS_RTIn_RTICOMP1 Registers

4.26.18.1 RTIn_RTICOMP1 Register (Offset = 58h) [reset = h]

Short Description: Compare 1 compare value to be compared with the counters

Long Description:

Return to Summary Table

Table 4-2337. Instance Table

Instance Name	Physical Address
RTI0	5218 0058h
RTI1	5218 1058h
RTI2	5218 2058h
RTI3	5218 3058h

Access Types Legend

Table 4-2338. RTICOMP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP1	RW	0h	COMP1: compare1.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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4.26.19 MSS_RTIn_RTIUDCP1 Registers

4.26.19.1 RTIn_RTIUDCP1 Register (Offset = 5Ch) [reset = h]

Short Description: Update Compare 1 value to be added to the compare register 1 value on compare match

Long Description:

Return to Summary Table

Table 4-2339. Instance Table

Instance Name	Physical Address
RTI0	5218 005Ch
RTI1	5218 105Ch
RTI2	5218 205Ch
RTI3	5218 305Ch

Access Types Legend

Table 4-2340. RTIUDCP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UDCP1	RW	0h	UDCP1: Update compare1 Register.This registers holds a value, which is added to the value in the compare1 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.User and privilege mode (read):value to be added to the compare1 register on the next compare matchPrivilege mode (write):new update value

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4.26.20 MSS_RTIn_RTICOMP2 Registers

4.26.20.1 RTIn_RTICOMP2 Register (Offset = 60h) [reset = h]

Short Description: Compare 2 compare value to be compared with the counters

Long Description:

Return to Summary Table

Table 4-2341. Instance Table

Instance Name	Physical Address
RTI0	5218 0060h
RTI1	5218 1060h
RTI2	5218 2060h
RTI3	5218 3060h

Access Types Legend

Table 4-2342. RTICOMP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP2	RW	0h	COMP2: compare 2.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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4.26.21 MSS_RTIn_RTIUDCP2 Registers

4.26.21.1 RTIn_RTIUDCP2 Register (Offset = 64h) [reset = h]

Short Description: Update Compare 2 value to be added to the compare register 2 value on compare match

Long Description:

Return to Summary Table

Table 4-2343. Instance Table

Instance Name	Physical Address
RTI0	5218 0064h
RTI1	5218 1064h
RTI2	5218 2064h
RTI3	5218 3064h

Access Types Legend

Table 4-2344. RTIUDCP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UDCP2	RW	0h	UDCP2: Update compare 2 Register.This registers holds a value, which is added to the value in the compare 2 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.User and privilege mode (read):value to be added to the compare 2 register on the next compare matchPrivilege mode (write):new update value

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4.26.22 MSS_RTIn_RTICOMP3 Registers

4.26.22.1 RTIn_RTICOMP3 Register (Offset = 68h) [reset = h]

Short Description: Compare 3 compare value to be compared with the counters

Long Description:

Return to Summary Table

Table 4-2345. Instance Table

Instance Name	Physical Address
RTI0	5218 0068h
RTI1	5218 1068h
RTI2	5218 2068h
RTI3	5218 3068h

Access Types Legend

Table 4-2346. RTICOMP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP3	RW	0h	COMP3: compare 3.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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4.26.23 MSS_RTIn_RTIUDCP3 Registers

4.26.23.1 RTIn_RTIUDCP3 Register (Offset = 6Ch) [reset = h]

Short Description: Update Compare 3 value to be added to the compare register 3 value on compare match

Long Description:

Return to Summary Table

Table 4-2347. Instance Table

Instance Name	Physical Address
RTI0	5218 006Ch
RTI1	5218 106Ch
RTI2	5218 206Ch
RTI3	5218 306Ch

Access Types Legend

Table 4-2348. RTIUDCP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	UDCP3	RW	0h	UDCP3: Update compare 3 Register.This registers holds a value, which is added to the value in the compare 3 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.User and privilege mode (read):value to be added to the compare 3 register on the next compare matchPrivilege mode (write):new update value

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4.26.24 MSS_RTIn_RTITBLCOMP Registers

4.26.24.1 RTIn_RTITBLCOMP Register (Offset = 70h) [reset = h]

Short Description: Timebase Low Compare compare value to activate edge detection circuit

Long Description:

Return to Summary Table

Table 4-2349. Instance Table

Instance Name	Physical Address
RTI0	5218 0070h
RTI1	5218 1070h
RTI2	5218 2070h
RTI3	5218 3070h

Access Types Legend

Table 4-2350. RTITBLCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TBLCOMP	RW	0h	TBLCOMP: Timebase Low Compare Value.This value determines when the edge detection circuit starts monitoring the NTUx signal. It will be compared with Up Counter 0.User and privilege mode (read):current compare valuePrivilege mode (write when TBEXT = 0):the compare value is updatedPrivilege mode (write when TBEXT = 1):the compare value is not changedNote: Reset behaviorA reset does not generate a compare match.

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4.26.25 MSS_RTIn_RTITBHCOMP Registers

4.26.25.1 RTIn_RTITBHCOMP Register (Offset = 74h) [reset = h]

Short Description: Timebase High Compare compare value to deactivate edge detection circuit

Long Description:

Return to Summary Table

Table 4-2351. Instance Table

Instance Name	Physical Address
RTI0	5218 0074h
RTI1	5218 1074h
RTI2	5218 2074h
RTI3	5218 3074h

Access Types Legend

Table 4-2352. RTITBHCOMP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TBHCOMP	RW	0h	TBHCOMP: Timebase High Compare Value.This value determines when the edge detection circuit will stop monitoring the NTUx signal. It will be compared with Up Counter 0.RTITBHCOMP has to be less than RTICPUC0, since RTIUC0 will be reset when RTICPUC0 is reached.Example:The NTUx edge detection circuit should be active +/- 10 RTICLK cycles around RTICPUC0.RTICPUC0 = 0x00000050RTITBLCOMP = 0x000046RTITBHCOMP = 0x00000009User and privilege mode (read):current compare valuePrivilege mode (write when TBEXT = 0):the compare value is updatedPrivilege mode (write when TBEXT = 1):the compare value is not changedNote: Reset behaviorA reset does not generate a compare match.

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4.26.26 MSS_RTIn_RTISETINT Registers

4.26.26.1 RTIn_RTISETINT Register (Offset = 80h) [reset = h]

Short Description: Set Interrupt Enable sets interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation

Long Description:

Return to Summary Table

Table 4-2353. Instance Table

Instance Name	Physical Address
RTI0	5218 0080h
RTI1	5218 1080h
RTI2	5218 2080h
RTI3	5218 3080h

Access Types Legend

Table 4-2354. RTISETINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 19	RESERVED11	RW	0h	Reserved.Reads return 0 and writes have no effect
18	SETOVL1INT	RW	0h	SETOVL1INT: Set Free Running Counter 1 Overflow Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt
17	SETOVL0INT	RW	0h	SETOVL0INT: Set Free Running Counter 0 Overflow Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt
16	SETTBINT	RW	0h	SETTBINT: Set Timebase Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt
15 - 12	RESERVED10	RW	0h	Reserved.Reads return 0 and writes have no effect
11	SETDMA3	RW	0h	SETDMA3: Set Compare DMA Request 3.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable DMA request
10	SETDMA2	RW	0h	SETDMA2: Set Compare DMA Request 2.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable DMA request
9	SETDMA1	RW	0h	SETDMA1: Set Compare DMA Request 1.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable DMA request
8	SETDMA0	RW	0h	SETDMA0: Set Compare DMA Request 0.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable DMA request
7 - 4	RESERVED9	RW	0h	Reserved.Reads return 0 and writes have no effect
3	SETINT3	RW	0h	SETINT3: Set Compare Interrupt 3.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged
2	SETINT2	RW	0h	SETINT2: Set Compare Interrupt 2.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt

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Table 4-2354. RTISETINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	SETINT1	RW	0h	SETINT1: Set Compare Interrupt 1.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt
0	SETINT0	RW	0h	SETINT0: Set Compare Interrupt 0.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = enable interrupt

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4.26.27 MSS_RTIn_RTICLEARINT Registers

4.26.27.1 RTIn_RTICLEARINT Register (Offset = 84h) [reset = h]

Short Description: Clear Interrupt Enable clears interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation

Long Description:

Return to Summary Table

Table 4-2355. Instance Table

Instance Name	Physical Address
RTI0	5218 0084h
RTI1	5218 1084h
RTI2	5218 2084h
RTI3	5218 3084h

Access Types Legend

Table 4-2356. RTICLEARINT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 19	RESERVED14	RW	0h	Reserved.Reads return 0 and writes have no effect
18	CLEAROVL1INT	RW	0h	CLEAROVL1INT: CLEAR Free Running Counter 1 Overflow Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt
17	CLEAROVL0INT	RW	0h	CLEAROVL0INT: CLEAR Free Running Counter 0 Overflow Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt
16	CLEARTBINT	RW	0h	CLEARTBINT: CLEAR Timebase Interrupt.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt
15 - 12	RESERVED13	RW	0h	Reserved.Reads return 0 and writes have no effect
11	CLEARDMA3	RW	0h	CLEARDMA3: CLEAR Compare DMA Request 3.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable DMA request
10	CLEARDMA2	RW	0h	CLEARDMA2: CLEAR Compare DMA Request 2.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable DMA request
9	CLEARDMA1	RW	0h	CLEARDMA1: CLEAR Compare DMA Request 1.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable DMA request
8	CLEARDMA0	RW	0h	CLEARDMA0: CLEAR Compare DMA Request 0.User and privilege mode (read):0 = DMA request is disabled1 = DMA request is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable DMA request
7 - 4	RESERVED12	RW	0h	Reserved.Reads return 0 and writes have no effect
3	CLEARINT3	RW	0h	CLEARINT3: CLEAR Compare Interrupt 3.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt
2	CLEARINT2	RW	0h	CLEARINT2: CLEAR Compare Interrupt 2.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt

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Table 4-2356. RTICLEARINT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	CLEARINT1	RW	0h	CLEARINT1: CLEAR Compare Interrupt 1.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt
0	CLEARINT0	RW	0h	CLEARINT0: CLEAR Compare Interrupt 0.User and privilege mode (read):0 = interrupt is disabled1 = interrupt is enabledPrivilege mode (write):0 = leaves the corresponding bit unchanged1 = disable interrupt

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4.26.28 MSS_RTIn_RTIINTFLAG Registers

4.26.28.1 RTIn_RTIINTFLAG Register (Offset = 88h) [reset = h]

Short Description: Interrupt Flags interrupt pending bits

Long Description:

Return to Summary Table

Table 4-2357. Instance Table

Instance Name	Physical Address
RTI0	5218 0088h
RTI1	5218 1088h
RTI2	5218 2088h
RTI3	5218 3088h

Access Types Legend

Table 4-2358. RTIINTFLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 19	RESERVED16	RW	0h	Reserved.Reads return 0 and writes have no effect
18	OVL1INT	RW	0h	OVL1INT: Free Running Counter 1 Overflow Interrupt Flag.User and privilege mode (read):determines if an interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
17	OVL0INT	RW	0h	OVL0INT: Free Running Counter 0 Overflow Interrupt Flag.User and privilege mode (read):determines if an interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
16	TBINT	RW	0h	User and privilege mode (read):this flag is set when the TBEXT bit is cleared by detection of a missing external clockedge. It will not be set by clearing TBEXT by software.determines if an interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
15 - 4	RESERVED15	RW	0h	Reserved.Reads return 0 and writes have no effect
3	INT3	RW	0h	INT3: Interrupt Flag 3.User and privilege mode (read):determines if a interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
2	INT2	RW	0h	INT2: Interrupt Flag 2.User and privilege mode (read):determines if a interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
1	INT1	RW	0h	INT1: Interrupt Flag 1.User and privilege mode (read):determines if a interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0
0	INT0	RW	0h	INT0: Interrupt Flag 0.User and privilege mode (read):determines if a interrupt is pending0 = no interrupt pending1 = interrupt pendingPrivilege mode (write):0 = leaves the bit unchanged1 = set the bit to 0

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4.26.29 MSS_RTIn_RTIDWDCTRL Registers

4.26.29.1 RTIn_RTIDWDCTRL Register (Offset = 90h) [reset = h]

Short Description: Digital Watchdog Control Enables the Digital Watchdog

Long Description:

Return to Summary Table

Table 4-2359. Instance Table

Instance Name	Physical Address
RTI0	5218 0090h
RTI1	5218 1090h
RTI2	5218 2090h
RTI3	5218 3090h

Access Types Legend

Table 4-2360. RTIDWDCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DWDCTRL	RW	0h	DWDCTRL: Digital Watchdog Control.User and priviledge mode (read):0x5312ACED = DWD counter is disabled. This is the default value.0xA98559DA = DWD counter is enabledAny other value = DWD counter state is unchanged (enabled or disabled)Priviledge mode (write):0xA98559DA = DWD counter is enabledAny other value = State of DWD counter is unchanged (stays enabled or disabled)Note: One-Write Functionality of DWDCTRL RegisterThe RTIDWDCTRL register implements a one-write functionality, such that the application cannot write to this registermore than once. Writing the default value will not enable the watchdog as described above. Writing the enable value will start the watchdog counters. A write to RTIDWDCTRL will only be enabled after a system reset again.

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4.26.30 MSS_RTIn_RTIDWDPRLD Registers

4.26.30.1 RTIn_RTIDWDPRLD Register (Offset = 94h) [reset = h]

Short Description: Digital Watchdog Preload sets the experation time of the Digital Watchdog

Long Description:

Return to Summary Table

Table 4-2361. Instance Table

Instance Name	Physical Address
RTI0	5218 0094h
RTI1	5218 1094h
RTI2	5218 2094h
RTI3	5218 3094h

Access Types Legend

Table 4-2362. RTIDWDPRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 12	RESERVED17	RW	0h	Reserved.Reads return 0 and writes have no effect
11 - 0	DWDPRLD	RW	0h	DWDPRLD: Digital Watchdog Preload Value.User and priviledge mode (read):A read from this register in any CPU mode returns the current preload value.Priviledge mode (write):If the DWD is always enabled after reset is released:The DWD starts counting down from the reset value of the counter, that is, 0x002DFFFF. The application can configure the DWD preload register any time before this down counter expires.When the application services the DWD, the preload register contents are copied left-justified into the DWD down counter and it starts counting down from that value.If the DWD is implemented such that the down counter is enabled by software:The DWD preload register can be configured only when the DWD is disabled. Therefore, the application can only configure the DWD preload register before it enables the DWD down counter.The expiration time of the DWD Down Counter can be determined with following equation:texp = (RTIDWDPRLD+1) x 2 ^ 13 / RTICLK1where: RTIDWDPRLD = 0...4095

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4.26.31 MSS_RTIn_RTIWDSTATUS Registers

4.26.31.1 RTIn_RTIWDSTATUS Register (Offset = 98h) [reset = h]

Short Description: Watchdog Status reflects the status of Analog and Digital Watchdog

Long Description:

Return to Summary Table

Table 4-2363. Instance Table

Instance Name	Physical Address
RTI0	5218 0098h
RTI1	5218 1098h
RTI2	5218 2098h
RTI3	5218 3098h

Access Types Legend

Table 4-2364. RTIWDSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 6	RESERVED18	RW	0h	Reserved.Reads return 0 and writes have no effect
5	DWWD_ST	RW	0h	DWWD ST: Windowed Watchdog Status.This bit denotes whether the time-window defined by the windowed watchdog configuration has been violated, or if a wrong key or key sequence was written to service the watchdog.User and priviledge mode (read):0 = no time-window violation has occurred.1 = a time-window violation has occurred. The watchdog will generate either a system reset or a non-maskable interrupt to the CPU in this case.Priviledge mode (write):0 = leaves the current value unchanged.1 = clears the bit to 0. This will also clear all other status flags in the RTIWDSTATUS register except for the AWD ST flag. Clearing of the status flags will deassert the non-maskable interrupt generated due to violation of the DWWD.
4	ENDTIMEVIOL	RW	0h	END TIME VIOL: Windowed Watchdog End Time Violation Status.This bit denotes whether the end-time defined by the windowed watchdog configuration has been violated. This bit is effectively a copy of the DWD ST status flag.User and priviledge mode (read):0 = no end-time window violation has occurred.1 = the end-time defined by the windowed watchdog configuration has been violated.Priviledge mode (write):0 = leaves the current value unchanged.1 = clears the bit to 0.
3	STARTTIMEVIOL	RW	0h	START TIME VIOL: Windowed Watchdog Start Time Violation Status. This bit denotes whether the start-time defined by the windowed watchdog configuration has been violated. This indicates that the WWD was serviced before the service window was opened.User and priviledge mode (read):0 = no start-time window violation has occurred.1 = the start-time defined by the windowed watchdog configuration has been violated.Priviledge mode (write):0 = leaves the current value unchanged.1 = clears the bit to 0.
2	KEYST	RW	0h	KEYST: Watchdog KeyStatus.This bit denotes a reset generated by a wrong key or a wrong key-sequence written to the RTIWDKEY register.User and priviledge mode (read):0 = no wrong key or key-sequence written1 = wrong key or key-sequence written to RTIWDKEY registerPriviledge mode (write):0 = leaves the current value unchanged1 = clears the bit to 0
1	DWDST	RW	0h	DWDST: Digital Watchdog Status.This bit is effectively a copy of the END TIME VIOL status flag and is maintained for compatibility reasons.User and priviledge mode (read):0 = DWD timeout period not expired1 = DWD timeout period has expiredPriviledge mode (write):0 = leaves the current value unchanged1 = clears the bit to 0

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Table 4-2364. RTIWDSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	AWDST	RW	0h	AWDST: Analog Watchdog Status.User and priviledge mode (read):0 = AWD pin 0 ?> 1 threshold not exceeded1 = AWD pin 0 ?> 1 threshold exceededPriviledge mode (write):0 = leaves the current value unchanged1 = clears the bit to 0

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4.26.32 MSS_RTIn_RTIWDKEY Registers

4.26.32.1 RTIn_RTIWDKEY Register (Offset = 9Ch) [reset = h]

Short Description: Watchdog Key correct written key values discharge the external capacitor

Long Description:

Return to Summary Table

Table 4-2365. Instance Table

Instance Name	Physical Address
RTI0	5218 009Ch
RTI1	5218 109Ch
RTI2	5218 209Ch
RTI3	5218 309Ch

Access Types Legend

Table 4-2366. RTIWDKEY Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED19	RW	0h	Reserved.Reads return 0 and writes have no effect
15 - 0	WDKEY	RW	0h	WDKEY: Watchdog Key.User and privilege mode reads are indeterminate.Privilege mode (write):A write of 0xE51A followed by 0xA35C in two separate write operations defines the Key Sequence and discharges the watchdog capacitor. This also causes the upper 12 bits of the DWD down counter to be reloaded with the contents of the DWD preload register and the lower 13 bits to become all 1?s. Writing any other value causes a digital watchdog reset, as shown in Table 1-3.Note: Register write access time precautionThe user has to take into account that the write to the register takes 3 VCLK cycle. This needs to be considered for the AWD/DWD expiration calculation.

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4.26.33 MSS_RTIn_RTIDWDCNTR Registers

4.26.33.1 RTIn_RTIDWDCNTR Register (Offset = A0h) [reset = h]

Short Description: Digital Watchdog Down Counter current value of DWD down counter

Long Description:

Return to Summary Table

Table 4-2367. Instance Table

Instance Name	Physical Address
RTI0	5218 00A0h
RTI1	5218 10A0h
RTI2	5218 20A0h
RTI3	5218 30A0h

Access Types Legend

Table 4-2368. RTIDWDCNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	RESERVED20	RW	0h	Reserved.Reads return 0 and writes have no effect
24 - 0	DWDCNTR	RW	0h	DWDCNTR: Digital Watchdog Down Counter.The value of the DWDCNTR after a system reset is 0x002D_FFFF. When the DWD is enabled and the DWD counter starts counting down from this value with an RTICLK1 time base of 3MHz, a watchdog reset will be generated in 1 second.User and privilege mode (read):Reads return the current counter value.Privilege mode (write):Writes don?t have an effect.

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4.26.34 MSS_RTIn_RTIWWDRXNCTRL Registers

4.26.34.1 RTIn_RTIWWDRXNCTRL Register (Offset = A4h) [reset = h]

Short Description: Windowed Watchdog Reaction Control configures the windowed watchdog to either generate a non-maskable interrupt to the CPU or to generate a system reset

Long Description:

Return to Summary Table

Table 4-2369. Instance Table

Instance Name	Physical Address
RTI0	5218 00A4h
RTI1	5218 10A4h
RTI2	5218 20A4h
RTI3	5218 30A4h

Access Types Legend

Table 4-2370. RTIWWDRXNCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RESERVED21	RW	0h	Reserved.Reads return 0 and writes have no effect
3 - 0	WWDRXN	RW	0h	WWDRXN: Digital Windowed Watchdog Reaction.User and privilege mode (read), privileged mode (write):0x5 = This is the default value. The windowed watchdog will cause a reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all.0xA = The windowed watchdog will generate a non-maskable interrupt to the CPU if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all.Writing any other value will cause a system reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all.Note: Configuration of DWWD ReactionThe DWWD reaction can be selected by the application even when the DWWD counter is already enabled.If a change to the WWDRXN is made before the watchdog service window is opened, then the change in the configuration takes effect immediately.If a change to the WWDRXN is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced.

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4.26.35 MSS_RTIn_RTIWWDSIZECTRL Registers

4.26.35.1 RTIn_RTIWWDSIZECTRL Register (Offset = A8h) [reset = h]

Short Description: Windowed Watchdog Size Control configures the size of the window for the digital windowed watchdog

Long Description:

Return to Summary Table

Table 4-2371. Instance Table

Instance Name	Physical Address
RTI0	5218 00A8h
RTI1	5218 10A8h
RTI2	5218 20A8h
RTI3	5218 30A8h

Access Types Legend

Table 4-2372. RTIWWDSIZECTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	WWDSIZE	RW	0h	WWDSIZE: Digital Windowed Watchdog Window Size.User and privilege mode (read), privileged mode (write):Value written to WWDSIZE Window Size0x00000005 100% (Functionality same as the time-out digital watchdog.)0x00000050 50%0x00000500 25%0x00005000 12.5%0x00050000 6.25%0x00500000 3.125%Any other value 3.125%Note: Incorrect value being written to watchdog window size control registerIf an incorerct value is written to the WWDSIZE field, or if a system disturbance causes the WWDSIZE field to have a value other than 0x5, 0x50, 0x500, 0x5000, 0x50000, or 0x500000, then the window size will be configured to be 3.125%. This increases the chances of getting a reset due to the windowed watchdog, which enables the system to handle the cause for the incorrect configuration.Note: Configuration of DWWD Window SizeThe DWWD window size can be selected by the application even when the DWWD counter is already enabled.If a change to the WWDSIZE is made before the watchdog service window is opened, then the change in the configuration takes effect immediately.If a change to the WWDSIZE is made when the watchdog service window is already open, then

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4.26.36 MSS_RTIn_RTIINTCLRENABLE Registers

4.26.36.1 RTIn_RTIINTCLRENABLE Register (Offset = ACh) [reset = h]

Short Description: RTI Compare Interrupt Clear Enable enable the auto clear functionality for each of the compare interrupts

Long Description:

Return to Summary Table

Table 4-2373. Instance Table

Instance Name	Physical Address
RTI0	5218 00ACh
RTI1	5218 10ACh
RTI2	5218 20ACh
RTI3	5218 30ACh

Access Types Legend

Table 4-2374. RTIINTCLRENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 28	RESERVED25	RW	0h	Reserved.Reads return 0 and writes have no effect
27 - 24	INTCLRENABLE3	RW	0h	INTCLRENABLE3.Enables the auto-clear functionality on the compare 3 interrupt.User and Privileged mode (read):0x5 = Auto-clear for compare 3 interrupt is disabled.Any other value = Auto-clear for compare 3 interrupt is enabled.Privileged mode (write):0x5 = Disables the auto-clear functionality on the compare 3 interrupt.Any other value = Enables the auto-clear functionality on the compare 3 interrupt.
23 - 20	RESERVED24	RW	0h	Reserved.Reads return 0 and writes have no effect
19 - 16	INTCLRENABLE2	RW	0h	INTCLRENABLE2.Enables the auto-clear functionality on the compare 2 interrupt.User and Privileged mode (read):0x5 = Auto-clear for compare 2 interrupt is disabled.Any other value = Auto-clear for compare 2 interrupt is enabled.Privileged mode (write):0x5 = Disables the auto-clear functionality on the compare 2 interrupt.Any other value = Enables the auto-clear functionality on the compare 2 interrupt.
15 - 12	RESERVED23	RW	0h	Reserved.Reads return 0 and writes have no effect
11 - 8	INTCLRENABLE1	RW	0h	INTCLRENABLE1.Enables the auto-clear functionality on the compare 1 interrupt.User and Privileged mode (read):0x5 = Auto-clear for compare 1 interrupt is disabled.Any other value = Auto-clear for compare 1 interrupt is enabled.Privileged mode (write):0x5 = Disables the auto-clear functionality on the compare 1 interrupt.Any other value = Enables the auto-clear functionality on the compare 1 interrupt.
7 - 4	RESERVED22	RW	0h	Reserved.Reads return 0 and writes have no effect
3 - 0	INTCLRENABLE0	RW	0h	INTCLRENABLE0.Enables the auto-clear functionality on the compare 0 interrupt.User and Privileged mode (read):0x5 = Auto-clear for compare 0 interrupt is disabled.Any other value = Auto-clear for compare 0 interrupt is enabled.Privileged mode (write):0x5 = Disables the auto-clear functionality on the compare 0 interrupt.Any other value = Enables the auto-clear functionality on the compare 0 interrupt.

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4.26.37 MSS_RTIn_RTICOMP0CLR Registers

4.26.37.1 RTIn_RTICOMP0CLR Register (Offset = B0h) [reset = h]

Short Description: Compare 0 Clear compare value to be compared with the counter to clear the compare0 interrupt line

Long Description:

Return to Summary Table

Table 4-2375. Instance Table

Instance Name	Physical Address
RTI0	5218 00B0h
RTI1	5218 10B0h
RTI2	5218 20B0h
RTI3	5218 30B0h

Access Types Legend

Table 4-2376. RTICOMP0CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP0CLR	RW	0h	COMP0CLR: Compare 0 Clear.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 0 interrupt or DMA request line is cleared.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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4.26.38 MSS_RTIn_RTICOMP1CLR Registers

4.26.38.1 RTIn_RTICOMP1CLR Register (Offset = B4h) [reset = h]

Short Description: Compare 1 Clear compare value to be compared with the counter to clear the compare1 interrupt line

Long Description:

Return to Summary Table

Table 4-2377. Instance Table

Instance Name	Physical Address
RTI0	5218 00B4h
RTI1	5218 10B4h
RTI2	5218 20B4h
RTI3	5218 30B4h

Access Types Legend

Table 4-2378. RTICOMP1CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP1CLR	RW	0h	COMP1CLR: Compare 1 Clear.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 1 interrupt or DMA request line is cleared.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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4.26.39 MSS_RTIn_RTICOMP2CLR Registers

4.26.39.1 RTIn_RTICOMP2CLR Register (Offset = B8h) [reset = h]

Short Description: Compare 2 Clear compare value to be compared with the counter to clear the compare2 interrupt line

Long Description:

Return to Summary Table

Table 4-2379. Instance Table

Instance Name	Physical Address
RTI0	5218 00B8h
RTI1	5218 10B8h
RTI2	5218 20B8h
RTI3	5218 30B8h

Access Types Legend

Table 4-2380. RTICOMP2CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP2CLR	RW	0h	COMP2CLR: Compare 2 Clear.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 2 interrupt or DMA request line is cleared.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

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4.26.40 MSS_RTIn_RTICOMP3CLR Registers

4.26.40.1 RTIn_RTICOMP3CLR Register (Offset = BCh) [reset = h]

Short Description: Compare 3 Clear compare value to be compared with the counter to clear the compare3 interrupt line

Long Description:

Return to Summary Table

Table 4-2381. Instance Table

Instance Name	Physical Address
RTI0	5218 00BCh
RTI1	5218 10BCh
RTI2	5218 20BCh
RTI3	5218 30BCh

Access Types Legend

Table 4-2382. RTICOMP3CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	COMP3CLR	RW	0h	COMP3CLR: Compare 3 Clear.This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 3 interrupt or DMA request line is cleared.User and privilege mode (read):current compare valuePrivilege mode (write):update of the compare register with a new compare valueNote: Reset behaviorA reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.

4.26.41 Access Table

Table 4-2383. Access Type Codes

Access Type	Code	Description
RW	RW	Read / Write

4.27 MCSPI Registers

Table 4-2384. MSS_MCSPI[0:2] Registers Base Address Table

Offset	Length	Acronym	MSS_MCSPI0 Physical Address	MSS_MCSPI1 Physical Address	MSS_MCSPI2 Physical Address
0h	32	MCSPI_HL_REV	5220 0000h	5220 1000h	5220 2000h
4h	32	MCSPI_HL_HWINFO	5220 0004h	5220 1004h	5220 2004h
10h	32	MCSPI_HL_SYSCONFIG	5220 0010h	5220 1010h	5220 2010h
100h	32	MCSPI_REVISION	5220 0100h	5220 1100h	5220 2100h
110h	32	MCSPI_SYSCONFIG	5220 0110h	5220 1110h	5220 2110h
114h	32	MCSPI_SYSSTATUS	5220 0114h	5220 1114h	5220 2114h
118h	32	MCSPI_IRQSTATUS	5220 0118h	5220 1118h	5220 2118h
11Ch	32	MCSPI_IRQENABLE	5220 011Ch	5220 111Ch	5220 211Ch
120h	32	MCSPI_WAKEUPENABLE	5220 0120h	5220 1120h	5220 2120h
124h	32	MCSPI_SYST	5220 0124h	5220 1124h	5220 2124h
128h	32	MCSPI_MODULCTRL	5220 0128h	5220 1128h	5220 2128h
12Ch	32	MCSPI_CH0CONF	5220 012Ch	5220 112Ch	5220 212Ch
130h	32	MCSPI_CH0STAT	5220 0130h	5220 1130h	5220 2130h

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Table 4-2384. MSS_MCSPI[0:2] Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_MCSPI0 Physical Address	MSS_MCSPI1 Physical Address	MSS_MCSPI2 Physical Address
134h	32	MCSPI_CH0CTRL	5220 0134h	5220 1134h	5220 2134h
138h	32	MCSPI_TX0	5220 0138h	5220 1138h	5220 2138h
13Ch	32	MCSPI_RX0	5220 013Ch	5220 113Ch	5220 213Ch
140h	32	MCSPI_CH1CONF	5220 0140h	5220 1140h	5220 2140h
144h	32	MCSPI_CH1STAT	5220 0144h	5220 1144h	5220 2144h
148h	32	MCSPI_CH1CTRL	5220 0148h	5220 1148h	5220 2148h
14Ch	32	MCSPI_TX1	5220 014Ch	5220 114Ch	5220 214Ch
150h	32	MCSPI_RX1	5220 0150h	5220 1150h	5220 2150h
154h	32	MCSPI_CH2CONF	5220 0154h	5220 1154h	5220 2154h
158h	32	MCSPI_CH2STAT	5220 0158h	5220 1158h	5220 2158h
15Ch	32	MCSPI_CH2CTRL	5220 015Ch	5220 115Ch	5220 215Ch
160h	32	MCSPI_TX2	5220 0160h	5220 1160h	5220 2160h
164h	32	MCSPI_RX2	5220 0164h	5220 1164h	5220 2164h
168h	32	MCSPI_CH3CONF	5220 0168h	5220 1168h	5220 2168h
16Ch	32	MCSPI_CH3STAT	5220 016Ch	5220 116Ch	5220 216Ch
170h	32	MCSPI_CH3CTRL	5220 0170h	5220 1170h	5220 2170h
174h	32	MCSPI_TX3	5220 0174h	5220 1174h	5220 2174h
178h	32	MCSPI_RX3	5220 0178h	5220 1178h	5220 2178h
17Ch	32	MCSPI_XFERLEVEL	5220 017Ch	5220 117Ch	5220 217Ch
180h	32	MCSPI_DAFTX	5220 0180h	5220 1180h	5220 2180h
1A0h	32	MCSPI_DAFRX	5220 01A0h	5220 11A0h	5220 21A0h

Table 4-2385. MSS_MCSPI[3:4] Registers Base Address Table

Offset	Length	Acronym	MSS_MCSPI3 Physical Address	MSS_MCSPI4 Physical Address
0h	32	MCSPI_HL_REV	5220 3000h	5220 4000h
4h	32	MCSPI_HL_HWINFO	5220 3004h	5220 4004h
10h	32	MCSPI_HL_SYSCONFIG	5220 3010h	5220 4010h
100h	32	MCSPI_REVISION	5220 3100h	5220 4100h
110h	32	MCSPI_SYSCONFIG	5220 3110h	5220 4110h
114h	32	MCSPI_SYSSTATUS	5220 3114h	5220 4114h
118h	32	MCSPI_IRQSTATUS	5220 3118h	5220 4118h
11Ch	32	MCSPI_IRQENABLE	5220 311Ch	5220 411Ch
120h	32	MCSPI_WAKEUPENABLE	5220 3120h	5220 4120h
124h	32	MCSPI_SYST	5220 3124h	5220 4124h
128h	32	MCSPI_MODULCTRL	5220 3128h	5220 4128h
12Ch	32	MCSPI_CH0CONF	5220 312Ch	5220 412Ch
130h	32	MCSPI_CH0STAT	5220 3130h	5220 4130h
134h	32	MCSPI_CH0CTRL	5220 3134h	5220 4134h
138h	32	MCSPI_TX0	5220 3138h	5220 4138h
13Ch	32	MCSPI_RX0	5220 313Ch	5220 413Ch
140h	32	MCSPI_CH1CONF	5220 3140h	5220 4140h
144h	32	MCSPI_CH1STAT	5220 3144h	5220 4144h
148h	32	MCSPI_CH1CTRL	5220 3148h	5220 4148h
14Ch	32	MCSPI_TX1	5220 314Ch	5220 414Ch
150h	32	MCSPI_RX1	5220 3150h	5220 4150h
154h	32	MCSPI_CH2CONF	5220 3154h	5220 4154h

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Table 4-2385. MSS_MCSPI[3:4] Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_MCSPI3 Physical Address	MSS_MCSPI4 Physical Address
158h	32	MCSPI_CH2STAT	5220 3158h	5220 4158h
15Ch	32	MCSPI_CH2CTRL	5220 315Ch	5220 415Ch
160h	32	MCSPI_TX2	5220 3160h	5220 4160h
164h	32	MCSPI_RX2	5220 3164h	5220 4164h
168h	32	MCSPI_CH3CONF	5220 3168h	5220 4168h
16Ch	32	MCSPI_CH3STAT	5220 316Ch	5220 416Ch
170h	32	MCSPI_CH3CTRL	5220 3170h	5220 4170h
174h	32	MCSPI_TX3	5220 3174h	5220 4174h
178h	32	MCSPI_RX3	5220 3178h	5220 4178h
17Ch	32	MCSPI_XFERLEVEL	5220 317Ch	5220 417Ch
180h	32	MCSPI_DAFTX	5220 3180h	5220 4180h
1A0h	32	MCSPI_DAFRX	5220 31A0h	5220 41A0h

4.27.1 MCSPI Instance Count Note

Note

n = 0 to 4 for the MCSPI registers defined below.

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4.27.2 MSS_MCSPIn_HL_REV Registers

4.27.2.1 MCSPIn_HL_REV Register (Offset = 0h) [reset = 40301a0bh]

Short Description: IP Revision register

Long Description: Used by software to track features, bugs, and compatibility

Return to Summary Table

Table 4-2386. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0000h
MCSPI1	5220 1000h
MCSPI2	5220 2000h
MCSPI3	5220 3000h
MCSPI4	5220 4000h

Figure 4-814. MCSPI_HL_REV Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RSVD		FUNC											
R		R		R											
1		0		110000											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R_RTL					X_MAJOR			CUSTOM		Y_MINOR					
R					R			R		R					
11					10			0		1011					

Access Types Legend

Table 4-2387. HL_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	R	1h	Used to distinguish between old scheme and current
29 - 28	RSVD	R	0h	Reserved These bits are initialized to zero, and writes to them are ignored
27 - 16	FUNC	R	1ADB0h	Function indicates a software compatible module family If there is no level of software compatibility a new Func number [and hence REVISION] should be assigned
15 - 11	R_RTL	R	Bh	RTL Version [R], maintained by IP design owner RTL follows a numbering such as XYRZ which are explained in this table R changes ONLY when: [1] PDS uploads occur which may have been due to spec changes [2] Bug fixes occur [3] Resets to '0' when X or Y changes Design team has an internal 'Z' [customer invisible] number which increments on every drop that happens due to DV and RTL updates Z resets to 0 when R increments
10 - 8	X_MAJOR	R	Ah	Major Revision [X], maintained by IP specification owner X changes ONLY when: [1] There is a major feature addition An example would be adding Master Mode to Utopia Level2 The Func field [or Class/ Type in old PID format] will remain the same X does NOT change due to: [1] Bug fixes [2] Change in feature parameters
7 - 6	CUSTOM	R	0h	Indicates a special version for a particular device Consequence of use may avoid use of standard Chip Support Library [CSL] / Drivers

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Table 4-2387. HL_REV Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5 - 0	Y_MINOR	R	3F3h	Minor Revision [Y], maintained by IP specification owner Y changes ONLY when: [1] Features are scaled [up or down] Flexibility exists in that this feature scalability may either be represented in the Y change or a specific register in the IP that indicates which features are exactly available [2] When feature creeps from Is-Not list to Is list But this may not be the case once it sees silicon; in which case X will change Y does NOT change due to: [1] Bug fixes [2] Typos or clarifications [3] major functional/feature change/addition/ deletion Instead these changes may be reflected via R, S, X as applicable Spec owner maintains a customer-invisible number 'S' which changes due to: [1] Typos/clarifications [2] Bug documentation Note that this bug is not due to a spec change but due to implementation Nevertheless, the spec tracks the IP bugs An RTL release [say for silicon PG11] that occurs due to bug fix should document the corresponding spec number [XYS] in its release notes

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4.27.3 MSS_MCSPIn_HL_HWINFO Registers

4.27.3.1 MCSPIn_HWINFO Register (Offset = 4h) [reset = 9h]

Short Description: MCSPI hardware configuration register

Long Description: Information about the IP module's hardware configuration, that is, typically the module's HDL generics (if any). Actual field format and encoding is up to the module's designer to decide.

Note

Some of the MCSPI features described in this section may not be supported on this family of devices. For more information, see MCSPI Not Supported Features.

Return to Summary Table

Table 4-2388. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0004h
MCSPI1	5220 1004h
MCSPI2	5220 2004h
MCSPI3	5220 3004h
MCSPI4	5220 4004h

Figure 4-815. MCSPI_HL_HWINFO Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									RETMODE	FFNBYTE					USEFIFO
R									R	R					R
0									0	100					1

Access Types Legend

Table 4-2389. HL_HWINFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RSVD	R	0h	Reserved These bits are initialized to zero, and writes to them are ignored
6	RETMODE	R	0h	This bit field indicates whether the retention mode is supported using the pin PIRFFRET
5 - 1	FFNBYTE	R	64h	FIFO number of byte generic parameter This register defines the value of FFNBYTE generic parameter, only MSB bits from 8 down to 4 are taken into account
0	USEFIFO	R	1h	Use of a FIFO enable: This bit field indicates if a FIFO is integrated within controller design with its management

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4.27.4 MSS_MCSPIn_HL_SYSCONFIG Registers

4.27.4.1 MCSPIn_SYSCONFIG Register (Offset = 10h) [reset = 8h]

Short Description: Clock management configuration register

Long Description: Clock management configuration register

Return to Summary Table

Table 4-2390. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0010h
MCSPI1	5220 1010h
MCSPI2	5220 2010h
MCSPI3	5220 3010h
MCSPI4	5220 4010h

Figure 4-816. MCSPI_HL_SYSCONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												IDLEMODE		FREEEMU	SOFTRESET
R												R/W		R/W	R/W
0												10		0	0

Access Types Legend

Table 4-2391. HL_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RSVD	R	0h	Reserved
3 - 2	IDLEMODE	R/W	Ah	Configuration of the local target state management mode By definition, target can handle read/write transaction as long as it is out of IDLE state
1	FREEEMU	R/W	0h	Sensitivity to emulation [debug] suspend input signal
0	SOFTRESET	R/W	0h	Software reset [Optional]

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4.27.5 MSS_MCSPIn_REVISION Registers

4.27.5.1 MCSPIn_REVISION Register (Offset = 100h) [reset = 2bh]

Short Description: Revision number

Long Description: This register contains the revision number.

Return to Summary Table

Table 4-2392. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0100h
MCSPI1	5220 1100h
MCSPI2	5220 2100h
MCSPI3	5220 3100h
MCSPI4	5220 4100h

Figure 4-817. MCSPI_REVISION Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_13															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_13								REV							
R								R							
0								101011							

Access Types Legend

Table 4-2393. REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_13	R	0h	Reads returns 0
7 - 0	REV	R	18A93h	IP revision [7:4] Major revision [3:0] Minor revision Examples: 0x10 for 10, 0x21 for 21

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4.27.6 MSS_MCSPIn_SYSCONFIG Registers

4.27.6.1 MCSPIn_SYSCONFIG Register (Offset = 110h) [reset = 15h]

Short Description: Configuration register

Long Description: This register allows controlling various parameters of the configuration interface and is not affected by software reset.

Return to Summary Table

Table 4-2394. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0110h
MCSPI1	5220 1110h
MCSPI2	5220 2110h
MCSPI3	5220 3110h
MCSPI4	5220 4110h

Figure 4-818. MCSPI_SYSCONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_14															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_14						CLOCKACTIVITY		RESERVED_15			SIDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE
R						R/W		R			R/W		R/W	R/W	R/W
0						0		0			10		1	0	1

Access Types Legend

Table 4-2395. SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 10	RESERVED_14	R	0h	Reads returns 0
9 - 8	CLOCKACTIVITY	R/W	0h	Clocks activity during wake up mode period
7 - 5	RESERVED_15	R	0h	Reads returns 0
4 - 3	SIDLEMODE	R/W	Ah	Power management
2	ENAWAKEUP	R/W	1h	WakeUp feature control
1	SOFTRESET	R/W	0h	Software reset During reads it always returns 0
0	AUTOIDLE	R/W	1h	Internal OCP Clock gating strategy

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4.27.7 MSS_MCSPIn_SYSSTATUS Registers

4.27.7.1 MCSPIn_SYSSTATUS Register (Offset = 114h) [reset = 1h]

Short Description: Status information register

Long Description: This register provides status information about the module excluding the interrupt status information.

Return to Summary Table

Table 4-2396. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0114h
MCSPI1	5220 1114h
MCSPI2	5220 2114h
MCSPI3	5220 3114h
MCSPI4	5220 4114h

Figure 4-819. MCSPI_SYSSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															RESETDONE
N/A															R
0															1

Access Types Legend

Table 4-2397. SYSSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	RESERVED	N/A		Reserved for module specific status information Read returns 0
0	RESETDONE	R	1h	Internal Reset Monitoring

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4.27.8 MSS_MCSPIn_IRQSTATUS Registers

4.27.8.1 MCSPIn_IRQSTATUS Register (Offset = 118h) [reset = 0h]

Short Description: Interrupt status register

Long Description: The interrupt status regroups all the status of the module internal events that can generate an interrupt.

Return to Summary Table

Table 4-2398. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0118h
MCSPI1	5220 1118h
MCSPI2	5220 2118h
MCSPI3	5220 3118h
MCSPI4	5220 4118h

Figure 4-820. MCSPI_IRQSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														EOW	WKS
N/A														R/W1TS	R/W1TS
0														0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RX3_FULL	TX3_UNDERFLOW	TX3_EMPTY	RESERVED	RX2_FULL	TX2_UNDERFLOW	TX2_EMPTY	RESERVED	RX1_FULL	TX1_UNDERFLOW	TX1_EMPTY	RX0_OVERFLOW	RX0_FULL	TX0_UNDERFLOW	TX0_EMPTY
N/A	R/W1TS	R/W1TS	R/W1TS	N/A	R/W1TS	R/W1TS	R/W1TS	N/A	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS	R/W1TS
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2399. IRQSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 18	RESERVED	N/A		Reads returns 0
17	EOW	R/W1TS	0h	End of word count event when a channel is enabled using the FIFO buffer and the channel had sent the number of SPI word defined by MCSPI_XFERLEVEL[WCNT]
16	WKS	R/W1TS	0h	Wake Up event in slave mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV]
15	RESERVED	N/A		Reads returns 0
14	RX3_FULL	R/W1TS	0h	Receiver register is full or almost full Only when Channel 3 is enabled
13	TX3_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Only when Channel 3 is enabled The transmitter register is empty [not updated by Host or DMA with new data] before its time slot assignment Exception: No TX_underflow event when no data has been loaded into the transmitter register since channel has been enabled
12	TX3_EMPTY	R/W1TS	0h	Transmitter register is empty or almost empty Note: Enabling the channel automatically rises this event
11	RESERVED	N/A		Reads returns 0
10	RX2_FULL	R/W1TS	0h	Receiver register full or almost full Channel 2
9	TX2_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 2

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Table 4-2399. IRQSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	TX2_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 2
7	RESERVED	N/A		Reads returns 0
6	RX1_FULL	R/W1TS	0h	Receiver register full or almost full Channel 1
5	TX1_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 1
4	TX1_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 1
3	RX0_OVERFLOW	R/W1TS	0h	Receiver register overflow [slave mode only] Channel 0
2	RX0_FULL	R/W1TS	0h	Receiver register full or almost full Channel 0
1	TX0_UNDERFLOW	R/W1TS	0h	Transmitter register underflow Channel 0
0	TX0_EMPTY	R/W1TS	0h	Transmitter register empty or almost empty Channel 0

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4.27.9 MSS_MCSPIn_IRQENABLE Registers

4.27.9.1 MCSPIn_IRQENABLE Register (Offset = 11Ch) [reset = 0h]

Short Description: Interrupt enable register

Long Description: This register allows enabling/disabling of the module internal sources of interrupt, on an event-by-event basis.

Return to Summary Table

Table 4-2400. Instance Table

Instance Name	Physical Address
MCSPI0	5220 011Ch
MCSPI1	5220 111Ch
MCSPI2	5220 211Ch
MCSPI3	5220 311Ch
MCSPI4	5220 411Ch

Figure 4-821. MCSPI_IRQENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														EOW_ENABLE	WKE
N/A														R/W	R/W
0														0	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RX3_FULL_ENABLE	TX3_UNDERFLOW_ENABLE	TX3_EMPTY_ENABLE	RESERVED	RX2_FULL_ENABLE	TX2_UNDERFLOW_ENABLE	TX2_EMPTY_ENABLE	RESERVED	RX1_FULL_ENABLE	TX1_UNDERFLOW_ENABLE	TX1_EMPTY_ENABLE	RX0_OVERFLOW_ENABLE	RX0_FULL_ENABLE	TX0_UNDERFLOW_ENABLE	TX0_EMPTY_ENABLE
N/A	R/W	R/W	R/W	N/A	R/W	R/W	R/W	N/A	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2401. IRQENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 18	RESERVED	N/A		Reads return 0
17	EOW_ENABLE	R/W	0h	End of Word count Interrupt Enable
16	WKE	R/W	0h	Wake Up event interrupt Enable in slave mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV]
15	RESERVED	N/A		Reads returns 0
14	RX3_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 3
13	TX3_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 3
12	TX3_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch3
11	RESERVED	N/A		Reads return 0
10	RX2_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 2
9	TX2_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 2
8	TX2_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch 2
7	RESERVED	N/A		Reads return 0
6	RX1_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 1

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Table 4-2401. IRQENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TX1_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 1
4	TX1_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch 1
3	RX0_OVERFLOW_ENABLE	R/W	0h	Receiver register Overflow Interrupt Enable Ch 0
2	RX0_FULL_ENABLE	R/W	0h	Receiver register Full Interrupt Enable Ch 0
1	TX0_UNDERFLOW_ENABLE	R/W	0h	Transmitter register Underflow Interrupt Enable Ch 0
0	TX0_EMPTY_ENABLE	R/W	0h	Transmitter register Empty Interrupt Enable Ch 0

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4.27.10 MSS_MCSPIn_WAKEUPENABLE Registers

4.27.10.1 MCSPIn_WAKEUPENABLE Register (Offset = 120h) [reset = 0h]

Short Description: Wake-up enable register

Long Description: The wake-up enable register allows enabling and disabling of the module internal sources of wakeup on event-by-event basis.

Return to Summary Table

Table 4-2402. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0120h
MCSPI1	5220 1120h
MCSPI2	5220 2120h
MCSPI3	5220 3120h
MCSPI4	5220 4120h

Figure 4-822. MCSPI_WAKEUPENABLE Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_18															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_18															WKEN
R															R/W
0															0

Access Types Legend

Table 4-2403. WAKEUPENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	RESERVED_18	R	0h	Reads returns 0
0	WKEN	R/W	0h	WakeUp functionality in slave mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV]

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4.27.11 MSS_MCSPIn_SYST Registers

4.27.11.1 MCSPIn_SYST Register (Offset = 124h) [reset = 0h]

Short Description: System interconnect check in system test mode

Long Description: This register is used to check the correctness of the system interconnect either internally to peripheral bus, or externally to device I/O pads, when the module is configured in system test (SYSTEST) mode.

Return to Summary Table

Table 4-2404. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0124h
MCSPI1	5220 1124h
MCSPI2	5220 2124h
MCSPI3	5220 3124h
MCSPI4	5220 4124h

Figure 4-823. MCSPI_SYST Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SSB	SPIENDIR	SPIDATDIR1	SPIDATDIR0	WAKD	SPICLK	SPIDAT_1	SPIDAT_0	SPIEN_3	SPIEN_2	SPIEN_1	SPIEN_0
N/A				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0				0	0	0	0	0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2405. SYST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 12	RESERVED	N/A		Reads returns 0
11	SSB	R/W	0h	Set status bit
10	SPIENDIR	R/W	0h	Set the direction of the SPIEN[3:0] lines and SPICLK line
9	SPIDATDIR1	R/W	0h	Set the direction of the SPIDAT[1]
8	SPIDATDIR0	R/W	0h	Set the direction of the SPIDAT[0]
7	WAKD	R/W	0h	SWAKEUP output [signal data value of internal signal to system] The signal is driven high or low according to the value written into this register bit
6	SPICLK	R/W	0h	SPICLK line [signal data value] If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the CLKSPI line [high or low], and a write into this bit has no effect If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the CLKSPI line is driven high or low according to the value written into this register
5	SPIDAT_1	R/W	0h	SPIDAT[1] line [signal data value] If MCSPI_SYST[SPIDATDIR1] = 0 [output mode direction], the SPIDAT[1] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIDATDIR1] = 1 [input mode direction], this bit returns the value on the SPIDAT[1] line [high or low], and a write into this bit has no effect

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Table 4-2405. SYST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SPIDAT_0	R/W	0h	SPIDAT[0] line [signal data value] If MCSPI_SYST[SPIDATDIR0] = 0 [output mode direction], the SPIDAT[0] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIDATDIR0] = 1 [input mode direction], this bit returns the value on the SPIDAT[0] line [high or low], and a write into this bit has no effect
3	SPIEN_3	R/W	0h	SPIEN[3] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[3] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[3] line [high or low], and a write into this bit has no effect
2	SPIEN_2	R/W	0h	SPIEN[2] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[2] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[2] line [high or low], and a write into this bit has no effect
1	SPIEN_1	R/W	0h	SPIEN[1] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[1] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[1] line [high or low], and a write into this bit has no effect
0	SPIEN_0	R/W	0h	SPIEN[0] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIENT[0] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[0] line [high or low], and a write into this bit has no effect

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4.27.12 MSS_MCSPIn_MODULCTRL Registers

4.27.12.1 MCSPIn_MODULCTRL Register (Offset = 128h) [reset = 4h]

Short Description: MCSPI configuration register

Long Description: This register is dedicated to the configuration of the serial peripheral interface.

Return to Summary Table

Table 4-2406. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0128h
MCSPI1	5220 1128h
MCSPI2	5220 2128h
MCSPI3	5220 3128h
MCSPI4	5220 4128h

Figure 4-824. MCSPI_MODULCTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							FDAA	MOA	INITDLY			SYSTEM_TEST	MS	PIN34	SINGLE
N/A							R/W	R/W	R/W			R/W	R/W	R/W	R/W
0							0	0	0			0	1	0	0

Access Types Legend

Table 4-2407. MODULCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 9	RESERVED	N/A		Reads returns 0
8	FDAA	R/W	0h	FIFO DMA Address 256-bit aligned This register is used when a FIFO is managed by the module and DMA connected to the controller provides only 256 bit aligned address If this bit is set the enabled channel which uses the FIFO has its datas managed through MCSPI_DAFTX and MCSPI_DAFRX registers instead of MCSPI_TX[i] and MCSPI_RX[i] registers
7	MOA	R/W	0h	Multiple word ocp access: This register can only be used when a channel is enabled using a FIFO It allows the system to perform multiple SPI word access for a single 32-bit OCP word access This is possible for WL < 16
6 - 4	INITDLY	R/W	0h	Initial spi delay for first transfer: This register is an option only available in SINGLE master mode, The controller waits for a delay to transmit the first spi word after channel enabled and corresponding TX register filled This Delay is based on SPI output frequency clock, No clock output provided to the boundary and chip select is not active in 4 pin mode within this period
3	SYSTEM_TEST	R/W	0h	Enables the system test mode
2	MS	R/W	1h	Master/ Slave
1	PIN34	R/W	0h	Pin mode selection: This register is used to configure the SPI pin mode, in master or slave mode If asserted the controller only use SIMO,SOMI and SPICLK clock pin for spi transfers
0	SINGLE	R/W	0h	Single channel / Multi Channel [master mode only]

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4.27.13 MSS_MCSPIn_CH0CONF Registers

4.27.13.1 MCSPIn_CH0CONF Register (Offset = 12Ch) [reset = 60000h]

Short Description: Configuration register of channel 0

Long Description: This register is dedicated to the configuration of the channel 0.

Return to Summary Table

Table 4-2408. Instance Table

Instance Name	Physical Address
MCSPI0	5220 012Ch
MCSPI1	5220 112Ch
MCSPI2	5220 212Ch
MCSPI3	5220 312Ch
MCSPI4	5220 412Ch

Figure 4-825. MCSPI_CH0CONF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		CLKG	FFER	FFEW	TCS0		SBPOL	SBE	SPIENSLV		FORCE	TURBO	IS	DPE1	DPE0
N/A		R/W	R/W	R/W	R/W		R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W
0		0	0	0	0		0	0	0		0	0	1	1	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAR	DMAW	TRM		WL					EPOL	CLKD				POL	PHA
R/W	R/W	R/W		R/W					R/W	R/W				R/W	R/W
0	0	0		0					0	0				0	0

Access Types Legend

Table 4-2409. CH0CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	RESERVED	N/A		read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set
26 - 25	TCS0	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock
24	SBPOL	R/W	0h	Start bit polarity
23	SBE	R/W	0h	Start bit enable for SPI transfer
22 - 21	SPIENSLV	R/W	0h	Channel 0 only and slave mode only: SPI slave select signal detection Reserved bits for other cases
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel master mode only]
19	TURBO	R/W	0h	Turbo mode
18	IS	R/W	1h	Input Select
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]]
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]]

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Table 4-2409. CH0CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel
13 - 12	TRM	R/W	0h	Transmit/Receive modes
11 - 7	WL	R/W	0h	SPI word length
6	EPOL	R/W	0h	SPIEN polarity
5 - 2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Master SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0
1	POL	R/W	0h	SPICLK polarity
0	PHA	R/W	0h	SPICLK phase

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4.27.14 MSS_MCSPIn_CH0STAT Registers

4.27.14.1 MCSPIn_CH0STAT Register (Offset = 130h) [reset = 0h]

Short Description: Status register of channel 0

Long Description: This register provides status information about transmitter and receiver registers of channel

Return to Summary Table

Table 4-2410. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0130h
MCSPI1	5220 1130h
MCSPI2	5220 2130h
MCSPI3	5220 3130h
MCSPI4	5220 4130h

Figure 4-826. MCSPI_CH0STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
N/A									R	R	R	R	R	R	R
0									0	0	0	0	0	0	0

Access Types Legend

Table 4-2411. CH0STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RESERVED	N/A		Read returns 0
6	RXFFF	R	0h	Channel 0 FIFO Receive Buffer Full Status
5	RXFFE	R	0h	Channel 0 FIFO Receive Buffer Empty Status
4	TXFFF	R	0h	Channel 0 FIFO Transmit Buffer Full Status
3	TXFFE	R	0h	Channel 0 FIFO Transmit Buffer Empty Status
2	EOT	R	0h	Channel 0 End of transfer Status The definitions of beginning and end of transfer vary with master versus slave and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details
1	TXS	R	0h	Channel 0 Transmitter Register Status
0	RXS	R	0h	Channel 0 Receiver Register Status

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4.27.15 MSS_MCSPIn_CH0CTRL Registers

4.27.15.1 MCSPIn_CH0CTRL Register (Offset = 134h) [reset = 0h]

Short Description: Enable register of channel 0

Long Description: This register is dedicated to enable channel 0

Return to Summary Table

Table 4-2412. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0134h
MCSPI1	5220 1134h
MCSPI2	5220 2134h
MCSPI3	5220 3134h
MCSPI4	5220 4134h

Figure 4-827. MCSPI_CH0CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTCLK								RESERVED							EN
R/W								N/A							R/W
0								0							0

Access Types Legend

Table 4-2413. CH0CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	N/A		Read returns 0
15 - 8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio
7 - 1	RESERVED	N/A		Read returns 0
0	EN	R/W	0h	Channel Enable

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4.27.16 MSS_MCSPIn_TX0 Registers

4.27.16.1 MCSPIn_TX0 Register (Offset = 138h) [reset = 0h]

Short Description: TX register of channel 0

Long Description: This register contains a single MCSPI word for channel 0 to transmit on the serial link, whatever MCSPI word length is.

Return to Summary Table

Table 4-2414. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0138h
MCSPI1	5220 1138h
MCSPI2	5220 2138h
MCSPI3	5220 3138h
MCSPI4	5220 4138h

Figure 4-828. MCSPI_TX0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDATA															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA															
R/W															
0															

Access Types Legend

Table 4-2415. TX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TDATA	R/W	0h	Channel 0 Data to transmit

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4.27.17 MSS_MCSPIn_RX0 Registers

4.27.17.1 MCSPIn_RX0 Register (Offset = 13Ch) [reset = 0h]

Short Description: RX register of channel 0

Long Description: This register contains a single MCSPI word for channel 0 received through the serial link, whatever MCSPI word length is.

Return to Summary Table

Table 4-2416. Instance Table

Instance Name	Physical Address
MCSPI0	5220 013Ch
MCSPI1	5220 113Ch
MCSPI2	5220 213Ch
MCSPI3	5220 313Ch
MCSPI4	5220 413Ch

Figure 4-829. MCSPI_RX0 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDATA															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA															
R															
0															

Access Types Legend

Table 4-2417. RX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RDATA	R	0h	Channel 0 Received Data

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4.27.18 MSS_MCSPIn_CH1CONF Registers

4.27.18.1 MCSPIn_CH1CONF Register (Offset = 140h) [reset = 60000h]

Short Description: Configuration register of channel 1

Long Description: This register is dedicated to the configuration of the channel 1.

Return to Summary Table

Table 4-2418. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0140h
MCSPI1	5220 1140h
MCSPI2	5220 2140h
MCSPI3	5220 3140h
MCSPI4	5220 4140h

Figure 4-830. MCSPI_CH1CONF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		CLKG	FFER	FFEW	TCS1		SBPOL	SBE	RESERVED		FORCE	TURBO	IS	DPE1	DPE0
N/A		R/W	R/W	R/W	R/W		R/W	R/W	N/A		R/W	R/W	R/W	R/W	R/W
0		0	0	0	0		0	0	0		0	0	1	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAR	DMAW	TRM		WL					EPOL	CLKD				POL	PHA
R/W	R/W	R/W		R/W					R/W	R/W				R/W	R/W
0	0	0		0					0	0				0	0

Access Types Legend

Table 4-2419. CH1CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	RESERVED	N/A		read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set
26 - 25	TCS1	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock
24	SBPOL	R/W	0h	Start bit polarity
23	SBE	R/W	0h	Start bit enable for SPI transfer
22 - 21	RESERVED	N/A		read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel master mode only]
19	TURBO	R/W	0h	Turbo mode
18	IS	R/W	1h	Input Select
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]]
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]]

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Table 4-2419. CH1CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel
13 - 12	TRM	R/W	0h	Transmit/Receive modes
11 - 7	WL	R/W	0h	SPI word length
6	EPOL	R/W	0h	SPIEN polarity
5 - 2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Master SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0
1	POL	R/W	0h	SPICLK polarity
0	PHA	R/W	0h	SPICLK phase

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4.27.19 MSS_MCSPIn_CH1STAT Registers

4.27.19.1 MCSPIn_CH1STAT Register (Offset = 144h) [reset = 0h]

Short Description: Status register of channel 1

Long Description: This register provides status information about transmitter and receiver registers of channel 1.

Return to Summary Table

Table 4-2420. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0144h
MCSPI1	5220 1144h
MCSPI2	5220 2144h
MCSPI3	5220 3144h
MCSPI4	5220 4144h

Figure 4-831. MCSPI_CH1STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
N/A									R	R	R	R	R	R	R
0									0	0	0	0	0	0	0

Access Types Legend

Table 4-2421. CH1STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RESERVED	N/A		Read returns 0
6	RXFFF	R	0h	Channel 1 FIFO Receive Buffer Full Status
5	RXFFE	R	0h	Channel 1 FIFO Receive Buffer Empty Status
4	TXFFF	R	0h	Channel 1 FIFO Transmit Buffer Full Status
3	TXFFE	R	0h	Channel 1 FIFO Transmit Buffer Empty Status
2	EOT	R	0h	Channel 1 End of transfer Status The definitions of beginning and end of transfer vary with master versus slave and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details
1	TXS	R	0h	Channel 1 Transmitter Register Status
0	RXS	R	0h	Channel 1 Receiver Register Status

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4.27.20 MSS_MCSPIn_CH1CTRL Registers

4.27.20.1 MCSPIn_CH1CTRL Register (Offset = 148h) [reset = 0h]

Short Description: Enable register of channel 1

Long Description: This register is dedicated to enable channel 1.

Return to Summary Table

Table 4-2422. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0148h
MCSPI1	5220 1148h
MCSPI2	5220 2148h
MCSPI3	5220 3148h
MCSPI4	5220 4148h

Figure 4-832. MCSPI_CH1CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTCLK								RESERVED							EN
R/W								N/A							R/W
0								0							0

Access Types Legend

Table 4-2423. CH1CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	N/A		Read returns 0
15 - 8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio
7 - 1	RESERVED	N/A		Read returns 0
0	EN	R/W	0h	Channel Enable

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4.27.21 MSS_MCSPIn_TX1 Registers

4.27.21.1 MCSPIn_TX1 Register (Offset = 14Ch) [reset = 0h]

Short Description: TX register of channel 1

Long Description: This register contains a single MCSPI word for channel 1 to transmit on the serial link, whatever MCSPI word length is.

Return to Summary Table

Table 4-2424. Instance Table

Instance Name	Physical Address
MCSPI0	5220 014Ch
MCSPI1	5220 114Ch
MCSPI2	5220 214Ch
MCSPI3	5220 314Ch
MCSPI4	5220 414Ch

Figure 4-833. MCSPI_TX1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDATA															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA															
R/W															
0															

Access Types Legend

Table 4-2425. TX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TDATA	R/W	0h	Channel 1 Data to transmit

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4.27.22 MSS_MCSPIn_RX1 Registers

4.27.22.1 MCSPIn_RX1 Register (Offset = 150h) [reset = 0h]

Short Description: RX register of channel 1

Long Description: This register contains a single MCSPI word for channel 1 received through the serial link, whatever MCSPI word length is.

Return to Summary Table

Table 4-2426. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0150h
MCSPI1	5220 1150h
MCSPI2	5220 2150h
MCSPI3	5220 3150h
MCSPI4	5220 4150h

Figure 4-834. MCSPI_RX1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDATA															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA															
R															
0															

Access Types Legend

Table 4-2427. RX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RDATA	R	0h	Channel 1 Received Data

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4.27.23 MSS_MCSPIn_CH2CONF Registers

4.27.23.1 MCSPIn_CH2CONF Register (Offset = 154h) [reset = 60000h]

Short Description: Configuration register of channel 2

Long Description: This register is dedicated to the configuration of the channel 2

Return to Summary Table

Table 4-2428. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0154h
MCSPI1	5220 1154h
MCSPI2	5220 2154h
MCSPI3	5220 3154h
MCSPI4	5220 4154h

Figure 4-835. MCSPI_CH2CONF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		CLKG	FFER	FFEW	TCS2		SBPOL	SBE	RESERVED		FORCE	TURBO	IS	DPE1	DPE0
N/A		R/W	R/W	R/W	R/W		R/W	R/W	N/A		R/W	R/W	R/W	R/W	R/W
0		0	0	0	0		0	0	0		0	0	1	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAR	DMAW	TRM		WL					EPOL	CLKD				POL	PHA
R/W	R/W	R/W		R/W					R/W	R/W				R/W	R/W
0	0	0		0					0	0				0	0

Access Types Legend

Table 4-2429. CH2CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	RESERVED	N/A		read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set
26 - 25	TCS2	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock
24	SBPOL	R/W	0h	Start bit polarity
23	SBE	R/W	0h	Start bit enable for SPI transfer
22 - 21	RESERVED	N/A		read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel master mode only]
19	TURBO	R/W	0h	Turbo mode
18	IS	R/W	1h	Input Select
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]]
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]]

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Table 4-2429. CH2CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel
13 - 12	TRM	R/W	0h	Transmit/Receive modes
11 - 7	WL	R/W	0h	SPI word length
6	EPOL	R/W	0h	SPIEN polarity
5 - 2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Master SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0
1	POL	R/W	0h	SPICLK polarity
0	PHA	R/W	0h	SPICLK phase

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4.27.24 MSS_MCSPIn_CH2STAT Registers

4.27.24.1 MCSPIn_CH2STAT Register (Offset = 158h) [reset = 0h]

Short Description: Status register of channel 2

Long Description: This register provides status information about transmitter and receiver registers of channel 2.

Return to Summary Table

Table 4-2430. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0158h
MCSPI1	5220 1158h
MCSPI2	5220 2158h
MCSPI3	5220 3158h
MCSPI4	5220 4158h

Figure 4-836. MCSPI_CH2STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
N/A									R	R	R	R	R	R	R
0									0	0	0	0	0	0	0

Access Types Legend

Table 4-2431. CH2STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RESERVED	N/A		Read returns 0
6	RXFFF	R	0h	Channel 2 FIFO Receive Buffer Full Status
5	RXFFE	R	0h	Channel 2 FIFO Receive Buffer Empty Status
4	TXFFF	R	0h	Channel 2 FIFO Transmit Buffer Full Status
3	TXFFE	R	0h	Channel 2 FIFO Transmit Buffer Empty Status
2	EOT	R	0h	Channel 2 End of transfer Status The definitions of beginning and end of transfer vary with master versus slave and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details
1	TXS	R	0h	Channel 2 Transmitter Register Status
0	RXS	R	0h	Channel 2 Receiver Register Status

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4.27.25 MSS_MCSPIn_CH2CTRL Registers

4.27.25.1 MCSPIn_CH2CTRL Register (Offset = 15Ch) [reset = 0h]

Short Description: Enable register of channel 2

Long Description: This register is dedicated to enable channel 2

Return to Summary Table

Table 4-2432. Instance Table

Instance Name	Physical Address
MCSPI0	5220 015Ch
MCSPI1	5220 115Ch
MCSPI2	5220 215Ch
MCSPI3	5220 315Ch
MCSPI4	5220 415Ch

Figure 4-837. MCSPI_CH2CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTCLK								RESERVED							EN
R/W								N/A							R/W
0								0							0

Access Types Legend

Table 4-2433. CH2CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	N/A		Read returns 0
15 - 8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio
7 - 1	RESERVED	N/A		Read returns 0
0	EN	R/W	0h	Channel Enable

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4.27.26 MSS_MCSPIn_TX2 Registers

4.27.26.1 MCSPIn_TX2 Register (Offset = 160h) [reset = 0h]

Short Description: TX register of channel 2

Long Description: This register contains a single MCSPI word for channel 2 to transmit on the serial link, whatever MCSPI word length is.

Return to Summary Table

Table 4-2434. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0160h
MCSPI1	5220 1160h
MCSPI2	5220 2160h
MCSPI3	5220 3160h
MCSPI4	5220 4160h

Figure 4-838. MCSPI_TX2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDATA															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA															
R/W															
0															

Access Types Legend

Table 4-2435. TX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TDATA	R/W	0h	Channel 2 Data to transmit

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4.27.27 MSS_MCSPIn_RX2 Registers

4.27.27.1 MCSPIn_RX2 Register (Offset = 164h) [reset = 0h]

Short Description: RX register of channel 2

Long Description: This register contains a single MCSPI word for channel 2 received through the serial link, whatever MCSPI word length is.

Return to Summary Table

Table 4-2436. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0164h
MCSPI1	5220 1164h
MCSPI2	5220 2164h
MCSPI3	5220 3164h
MCSPI4	5220 4164h

Figure 4-839. MCSPI_RX2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDATA															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA															
R															
0															

Access Types Legend

Table 4-2437. RX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RDATA	R	0h	Channel 2 Received Data

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4.27.28 MSS_MCSPIn_CH3CONF Registers

4.27.28.1 MCSPIn_CH3CONF Register (Offset = 168h) [reset = 60000h]

Short Description: Configuration register of channel 3

Long Description: This register is dedicated to the configuration of the channel 3

Return to Summary Table

Table 4-2438. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0168h
MCSPI1	5220 1168h
MCSPI2	5220 2168h
MCSPI3	5220 3168h
MCSPI4	5220 4168h

Figure 4-840. MCSPI_CH3CONF Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		CLKG	FFER	FFEW	TCS3		SBPOL	SBE	RESERVED		FORCE	TURBO	IS	DPE1	DPE0
N/A		R/W	R/W	R/W	R/W		R/W	R/W	N/A		R/W	R/W	R/W	R/W	R/W
0		0	0	0	0		0	0	0		0	0	1	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAR	DMAW	TRM		WL					EPOL	CLKD				POL	PHA
R/W	R/W	R/W		R/W					R/W	R/W				R/W	R/W
0	0	0		0					0	0				0	0

Access Types Legend

Table 4-2439. CH3CONF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	RESERVED	N/A		read returns 0
29	CLKG	R/W	0h	Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096 clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values
28	FFER	R/W	0h	FIFO enabled for receive:Only one channel can have this bit field set
27	FFEW	R/W	0h	FIFO enabled for Transmit:Only one channel can have this bit field set
26 - 25	TCS3	R/W	0h	Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock
24	SBPOL	R/W	0h	Start bit polarity
23	SBE	R/W	0h	Start bit enable for SPI transfer
22 - 21	RESERVED	N/A		read returns 0
20	FORCE	R/W	0h	Manual SPIEN assertion to keep SPIEN active between SPI words [single channel master mode only]
19	TURBO	R/W	0h	Turbo mode
18	IS	R/W	1h	Input Select
17	DPE1	R/W	1h	Transmission Enable for data line 1 [SPIDATAGZEN[1]]
16	DPE0	R/W	0h	Transmission Enable for data line 0 [SPIDATAGZEN[0]]

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Table 4-2439. CH3CONF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	DMAR	R/W	0h	DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel
14	DMAW	R/W	0h	DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel
13 - 12	TRM	R/W	0h	Transmit/Receive modes
11 - 7	WL	R/W	0h	SPI word length
6	EPOL	R/W	0h	SPIEN polarity
5 - 2	CLKD	R/W	0h	Frequency divider for SPICLK [only when the module is a Master SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0
1	POL	R/W	0h	SPICLK polarity
0	PHA	R/W	0h	SPICLK phase

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4.27.29 MSS_MCSPIn_CH3STAT Registers

4.27.29.1 MCSPIn_CH3STAT Register (Offset = 16Ch) [reset = 0h]

Short Description: Status register of channel 3

Long Description: This register provides status information about transmitter and receiver registers of channel 3.

Return to Summary Table

Table 4-2440. Instance Table

Instance Name	Physical Address
MCSPI0	5220 016Ch
MCSPI1	5220 116Ch
MCSPI2	5220 216Ch
MCSPI3	5220 316Ch
MCSPI4	5220 416Ch

Figure 4-841. MCSPI_CH3STAT Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									RXFFF	RXFFE	TXFFF	TXFFE	EOT	TXS	RXS
N/A									R	R	R	R	R	R	R
0									0	0	0	0	0	0	0

Access Types Legend

Table 4-2441. CH3STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RESERVED	N/A		Read returns 0
6	RXFFF	R	0h	Channel 3 FIFO Receive Buffer Full Status
5	RXFFE	R	0h	Channel 3 FIFO Receive Buffer Empty Status
4	TXFFF	R	0h	Channel 3 FIFO Transmit Buffer Full Status
3	TXFFE	R	0h	Channel 3 FIFO Transmit Buffer Empty Status
2	EOT	R	0h	Channel 3 End of transfer Status The definitions of beginning and end of transfer vary with master versus slave and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details
1	TXS	R	0h	Channel 3 Transmitter Register Status
0	RXS	R	0h	Channel 3 Receiver Register Status

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4.27.30 MSS_MCSPIn_CH3CTRL Registers

4.27.30.1 MCSPIn_CH3CTRL Register (Offset = 170h) [reset = 0h]

Short Description: Enable register of channel 3

Long Description: This register is dedicated to enable channel 3.

Return to Summary Table

Table 4-2442. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0170h
MCSPI1	5220 1170h
MCSPI2	5220 2170h
MCSPI3	5220 3170h
MCSPI4	5220 4170h

Figure 4-842. MCSPI_CH3CTRL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
N/A															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTCLK								RESERVED							EN
R/W								N/A							R/W
0								0							0

Access Types Legend

Table 4-2443. CH3CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RESERVED	N/A		Read returns 0
15 - 8	EXTCLK	R/W	0h	Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096 clock divider ratio
7 - 1	RESERVED	N/A		Read returns 0
0	EN	R/W	0h	Channel Enable

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4.27.31 MSS_MCSPIn_TX3 Registers

4.27.31.1 MCSPIn_TX3 Register (Offset = 174h) [reset = 0h]

Short Description: TX register of channel 3

Long Description: This register contains a single MCSPI word for channel 3 to transmit on the serial link, whatever MCSPI word length is.

Return to Summary Table

Table 4-2444. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0174h
MCSPI1	5220 1174h
MCSPI2	5220 2174h
MCSPI3	5220 3174h
MCSPI4	5220 4174h

Figure 4-843. MCSPI_TX3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDATA															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDATA															
R/W															
0															

Access Types Legend

Table 4-2445. TX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	TDATA	R/W	0h	Channel 3 Data to transmit

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4.27.32 MSS_MCSPIn_RX3 Registers

4.27.32.1 MCSPIn_RX3 Register (Offset = 178h) [reset = 0h]

Short Description: RX register of channel 3

Long Description: This register contains a single MCSPI word for channel 3 received through the serial link, whatever MCSPI word length is.

Return to Summary Table

Table 4-2446. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0178h
MCSPI1	5220 1178h
MCSPI2	5220 2178h
MCSPI3	5220 3178h
MCSPI4	5220 4178h

Figure 4-844. MCSPI_RX3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDATA															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA															
R															
0															

Access Types Legend

Table 4-2447. RX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RDATA	R	0h	Channel 3 Received Data

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4.27.33 MSS_MCSPIn_XFERLEVEL Registers

4.27.33.1 MCSPIn_XFERLEVEL Register (Offset = 17Ch) [reset = 0h]

Short Description: Transfer levels when FIFO is used

Long Description: This register provides transfer levels needed while using FIFO buffer during transfer.

Return to Summary Table

Table 4-2448. Instance Table

Instance Name	Physical Address
MCSPI0	5220 017Ch
MCSPI1	5220 117Ch
MCSPI2	5220 217Ch
MCSPI3	5220 317Ch
MCSPI4	5220 417Ch

Figure 4-845. MCSPI_XFERLEVEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WCNT															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFL								AEL							
R/W								R/W							
0								0							

Access Types Legend

Table 4-2449. XFERLEVEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	WCNT	R/W	0h	Spi word counterThis register holds the programmable value of number of SPI word to be transferred on channel which is using the FIFO bufferWhen transfer had started, a read back in this register returns the current SPI word transfer index
15 - 8	AFL	R/W	0h	Buffer Almost Full This register holds the programmable almost full level value used to determine almost full buffer condition If the user wants an interrupt or a DMA read request to be issued during a receive operation when the data buffer holds at least n bytes, then the buffer MCSPI_MODULCTRL[AFL] must be set with n-1The size of this register is defined by the generic parameter FFNBYTE
7 - 0	AEL	R/W	0h	Buffer Almost EmptyThis register holds the programmable almost empty level value used to determine almost empty buffer condition If the user wants an interrupt or a DMA write request to be issued during a transmit operation when the data buffer is able to receive n bytes, then the buffer MCSPI_MODULCTRL[AEL] must be set with n-1

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4.27.34 MSS_MCSPIn_DAFTX Registers

4.27.34.1 MCSPIn_DAFTX Register (Offset = 180h) [reset = 0h]

Short Description: MCSPI words transmitted when FIFO is used

Long Description: This register contains the MCSPI words to be transmitted on the MCSPI bus when FIFO is used and DMA address is aligned on 256 bit. This register is an image of one of the MCSPI_TX registers corresponding to the channel which has its FIFO enabled.

Return to Summary Table

Table 4-2450. Instance Table

Instance Name	Physical Address
MCSPI0	5220 0180h
MCSPI1	5220 1180h
MCSPI2	5220 2180h
MCSPI3	5220 3180h
MCSPI4	5220 4180h

Figure 4-846. MCSPI_DAFTX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DAFTDATA															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAFTDATA															
R/W															
0															

Access Types Legend

Table 4-2451. DAFTX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DAFTDATA	R/W	0h	FIFO Data to transmit with DMA 256 bit aligned address This Register is only is used when MCSPI_MODULCTRL[FDAA] is set to "1" and only one of the MCSPI_CH[i]CONF[FFEW] of enabled channels is set If these conditions are not respected any access to this register return a null value

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4.27.35 MSS_MCSPIn_DAFRX Registers

4.27.35.1 MCSPIn_DAFRX Register (Offset = 1A0h) [reset = 0h]

Short Description: MCSPI words received when FIFO is used

Long Description: This register contains the MCSPI words received from the MCSPI bus when FIFO is used and DMA address is aligned on 256 bit. This register is an image of one of the MCSPI_RX registers corresponding to the channel which has its FIFO enabled.

Return to Summary Table

Table 4-2452. Instance Table

Instance Name	Physical Address
MCSPI0	5220 01A0h
MCSPI1	5220 11A0h
MCSPI2	5220 21A0h
MCSPI3	5220 31A0h
MCSPI4	5220 41A0h

Figure 4-847. MCSPI_DAFRX Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DAFRDATA															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAFRDATA															
R															
0															

Access Types Legend

Table 4-2453. DAFRX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DAFRDATA	R	0h	FIFO Data to transmit with DMA 256 bit aligned address This Register is only is used when MCSPI_MODULCTRL[FDAA] is set to "1" and only one of the MCSPI_CH[i]CONF[FFEW] of enabled channels is set If these conditions are not respected any access to this register return a null value

4.27.36 Access Table

Table 4-2454. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write
N/A	N/A	Undefined
R/W1TS	R/W1TS	Read/Write 1 To Set

4.28 SPINLOCK Registers

Table 4-2455. MSS_SPINLOCK0 Registers Base Address Table

Offset	Length	Acronym	MSS_SPINLOCK0 Physical Address
0h	32	SPINLOCK_REVISION	50E0 0000h
10h	32	SPINLOCK_SYSCONFIG	50E0 0010h

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Table 4-2455. MSS_SPINLOCK0 Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_SPINLOCK0 Physical Address
14h	32	SPINLOCK_SYSTATUS	50E0 0014h
800h	32	SPINLOCK_LOCK_REG	50E0 0800h

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4.28.1 MSS_SPINLOCK0_REVISION Registers

4.28.1.1 SPINLOCK0_REVISION Register (Offset = 0h) [reset = 66fa6100h]

Short Description: Peripheral ID register

Long Description:

Return to Summary Table

Table 4-2456. Instance Table

Instance Name	Physical Address
SPINLOCK0	50E0 0000h

Figure 4-848. REVISION Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNCTION											
R		R		R											
1		10		11011111010											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER				MAJOR_REV				CUSTOM		MINOR_REV					
R				R				R		R					
1100				1				0		0					

Access Types Legend

Table 4-2457. REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used.
29 - 28	BU	R	Ah	BU identifier
27 - 16	FUNCTION	R	290503862h	Module family.
15 - 11	RTL_VER	R	44Ch	RTL version. R of X.Y.R.Z
10 - 8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z
7 - 6	CUSTOM	R	0h	Special version number
5 - 0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z

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4.28.2 MSS_SPINLOCK0_SYSCONFIG Registers

4.28.2.1 SPINLOCK0_SYSCONFIG Register (Offset = 10h) [reset = 0h]

Short Description: SpinLock top level configuration

Long Description:

Return to Summary Table

Table 4-2458. Instance Table

Instance Name	Physical Address
SPINLOCK0	50E0 0010h

Figure 4-849. SPINLOCK_SYSCONFIG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														SOFT_RESET	RESERVED
NONE														R/W	NONE
0														0	0

Access Types Legend

Table 4-2459. SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0 It has the same effect as the hardware reset Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and free all of the locks
	RESERVED	NONE		Reserved

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4.28.3 MSS_SPINLOCK0_SYSTATUS Registers

4.28.3.1 SPINLOCK0_SYSTATUS Register (Offset = 14h) [reset = 8000000h]

Short Description: SpinLock top level status

Long Description:

Return to Summary Table

Table 4-2460. Instance Table

Instance Name	Physical Address
SPINLOCK0	50E0 0014h

Figure 4-850. SPINLOCK_SYSTATUS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NUM_LOCKS								RESERVED							
R								NONE							
1000								0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								IN_USE7	IN_USE6	IN_USE5	IN_USE4	IN_USE3	IN_USE2	IN_USE1	IN_USE0
NONE								R	R	R	R	R	R	R	R
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2461. SYSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	NUM_LOCKS	R	3E8h	Module configuration parameter n, the total number of spinlocks divided by 32. e.g. For 256 spin locks, this will return the number 0x08
	RESERVED	NONE		Reserved
7	IN_USE7	R	0h	In-Use flag 7 covering lock registers 224 - 255. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 224 - 255 are in the Not Taken state Read 1 : At least one of the lock registers 224 - 255 are in the Taken state
6	IN_USE6	R	0h	In-Use flag 6 covering lock registers 192 - 223. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 192 - 223 are in the Not Taken state Read 1 : At least one of the lock registers 192 - 223 are in the Taken state
5	IN_USE5	R	0h	In-Use flag 5 covering lock registers 160 - 191. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 160 - 191 are in the Not Taken state Read 1 : At least one of the lock registers 160 - 191 are in the Taken state
4	IN_USE4	R	0h	In-Use flag 4 covering lock registers 128 - 159. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 128 - 159 are in the Not Taken state Read 1 : At least one of the lock registers 128 - 159 are in the Taken state
3	IN_USE3	R	0h	In-Use flag 3 covering lock registers 96 - 127. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 96 - 127 are in the Not Taken state Read 1 : At least one of the lock registers 96 - 127 are in the Taken state
2	IN_USE2	R	0h	In-Use flag 2 covering lock registers 64 - 95. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 64 - 95 are in the Not Taken state Read 1 : At least one of the lock registers 64 - 95 are in the Taken state

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Table 4-2461. SYSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	IN_USE1	R	0h	In-Use flag 1 covering lock registers 32 - 63. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 32 - 63 are in the Not Taken state Read 1 : At least one of the lock registers 32 - 63 are in the Taken state
0	IN_USE0	R	0h	In-Use flag 0 covering lock registers 0 - 31. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 0 - 31 are in the Not Taken state Read 1 : At least one of the lock registers 0 - 31 are in the Taken state

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4.28.4 MSS_SPINLOCK0_LOCK_REG Registers

4.28.4.1 SPINLOCK0_LOCK_REG Register (Offset = 800h) [reset = 0h]

Short Description: Lock[a] register

Long Description:

Return to Summary Table

Table 4-2462. Instance Table

Instance Name	Physical Address
SPINLOCK0	50E0 0800h

Figure 4-851. SPINLOCK_LOCK_REG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															TAKEN
NONE															R/W
0															0

Access Types Legend

Table 4-2463. LOCK_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
0	TAKEN	R/W	0h	Lock Status Read 0 : Lock was previously free. The reader now has been granted the lock. Read 1 : Lock was previously taken. The reader has not been granted the lock and must retry. Write 0 : Free the lock by setting TAKEN to zero. Write 1 : No effect

4.28.5 Access Table

Table 4-2464. Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read / Write

4.29 TCM Registers

Table 4-2465. MSS_TCMA_RAM Registers Base Address Table

Offset	Length	Acronym	MSS_TCMA Physical Address
0h	32	TCM_RAM_START_TCMA	0002 0000h
7FFCh	32	TCM_RAM_END_TCMA	0002 7FFCh

Table 4-2466. MSS_TCMB_RAM Registers Base Address Table

Offset	Length	Acronym	Register Name	MSS_TCMB Physical Address
0h	32	TCM_RAM_START_TCMB	R/W	0008 0000h
7FFCh	32	TCM_RAM_END_TCMB	R/W	0008 7FFCh

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4.29.1 MSS_TCMA_RAM_START_TCMA Registers

4.29.1.1 R5SS0_CORE0_RAM_START_TCMA Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 4-2467. Instance Table

Instance Name	Physical Address
R5SS0_CORE0_TCMA_RAM	0002 0000h

Access Types Legend

Table 4-2468. RAM_START_TCMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RAM_START	R/W	0h	RAM start address of master sub system TCMA

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4.29.2 MSS_TCMA_RAM_END_TCMA Registers

4.29.2.1 R5SS0_TCMA_RAM_RAM_END_TCMA Register (Offset = 7FFCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 4-2469. Instance Table

Instance Name	Physical Address
R5SS0_CORE0_TCMA_RAM	0002 7FFCh

Access Types Legend

Table 4-2470. RAM_END_TCMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RAM_END	RW	0h	RAM end address of master sub system tcma

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4.29.3 MSS_TCMA_RAM_START_TCMA Registers

4.29.3.1 R5SS0_TCMB_RAM_RAM_START_TCMA Register (Offset = 0h) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 4-2471. Instance Table

Instance Name	Physical Address
R5SS0_CORE0_TCMB_RAM	0008 0000h

Access Types Legend

Table 4-2472. RAM_START_TCMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RAM_START	RW	0h	RAM start address of master sub system tcma

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4.29.4 MSS_TCMA_RAM_END_TCMA Registers

4.29.4.1 R5SS0_TCMB_RAM_RAM_END_TCMA Register (Offset = 7FFCh) [reset = h]

Short Description: RW

Long Description:

Return to Summary Table

Table 4-2473. Instance Table

Instance Name	Physical Address
R5SS0_CORE0_TCMB_RAM	0008 7FFCh

Access Types Legend

Table 4-2474. RAM_END_TCMA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RAM_END	RW	0h	RAM end address of master sub system tcma

4.29.5 Access Table

Table 4-2475. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write

4.30 TCMA_CR5B Registers

Table 4-2476. R5SS[0:1]_CORE1_TCMA Registers Base Address Table

Offset	Length	Acronym	R5SS0_CORE1_TCMA Physical Address	R5SS1_CORE1_TCMA Physical Address
0h	32	TCMA_CR5B_START	7820 0000h	7860 0000h
7FFCh	32	TCMA_CR5B_END	7820 7FFCh	7860 7FFCh

Note

n = 0 to 1 for the TCM registers defined below.

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MSS_TCMA_CR5A_START Registers

4.30.1 R5SSn_TCMA_START Register (Offset = 0h) [reset = h]

Short Description:

Long Description:

Return to Summary Table

Table 4-2477. Instance Table

Instance Name	Physical Address
R5SS0_CORE1_TCMA	7820 0000h
R5SS1_CORE1_TCMA	7860 0000h

Figure 4-852. START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
R/W															
0															

Access Types Legend

Table 4-2478. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	RW	0h	TCMA start address

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MSS_TCMA_CR5B_END Registers

4.30.2 R5SSn_TCMA_END Register (Offset = 7FFCh) [reset = h]

Short Description:

Long Description:

Return to Summary Table

Table 4-2479. Instance Table

Instance Name	Physical Address
R5SS0_CORE1_TCMA	7820 7FFCh
R5SS1_CORE1_TCMA	7860 7FFCh

Figure 4-853. END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
R/W															
0															

Access Types Legend

Table 4-2480. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	END	R/W	0h	TCMA end address

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Table 4-2481. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write

4.31 TCMA_CR5A Registers

Table 4-2482. R5SS[0:1]_CORE0_TCMA Registers Base Address Table

Offset	Length	Acronym	R5SS0_CORE0_TCMA Physical Address	R5SS1_CORE0_TCMA Physical Address
0h	32	TCMA_CR5A_START	7800 0000h	7840 0000h
FFFCh	32	TCMA_CR5A_END	7800 FFFCh	7840 FFFCh

Note

n = 0 to 1 for the TCM registers defined below.

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MSS_TCMA_CR5A_START Registers

4.31.1 R5SSn_TCMA_START Register (Offset = 0h) [reset = h]

Short Description:

Long Description:

Return to Summary Table

Table 4-2483. Instance Table

Instance Name	Physical Address
R5SS0_CORE0_TCMA	7800 0000h
R5SS1_CORE0_TCMA	7840 0000h

Figure 4-854. START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
R/W															
0															

Access Types Legend

Table 4-2484. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	R/W	0h	TCMA start address

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MSS_TCMA_CR5A_END Registers

4.31.2 R5SSn_TCMA_END Register (Offset = FFFCh) [reset = h]

Short Description: R/W

Long Description:

Return to Summary Table

Table 4-2485. Instance Table

Instance Name	Physical Address
R5SS0_CORE0_TCMA	7800 FFFCh
R5SS1_CORE0_TCMA	7840 FFFCh

Figure 4-855. END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
R/W															
0															

Access Types Legend

Table 4-2486. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	END	R/W	0h	TCMA end address

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Table 4-2487. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write

4.32 TCMB_CR5A Registers

Table 4-2488. R5SS[0:1]_CORE0_TCMB Registers Base Address Table

Offset	Length	Acronym	R5SS0_CORE0_TCMB Physical Address	R5SS1_CORE0_TCMB Physical Address
0h	32	TCMB_CR5A_START	7810 0000h	7850 0000h
FFFCh	32	TCMB_CR5A_END	7810 FFFCh	7850 FFFCh

Note

n = 0 to 1 for the TCM registers defined below.

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MSS_TCMA_CR5A_START Registers

4.32.1 R5SSn_TCMB_START Register (Offset = 0h) [reset = h]

Short Description:

Long Description:

Return to Summary Table

Table 4-2489. Instance Table

Instance Name	Physical Address
R5SS0_CORE0_TCMB	7810 0000h
R5SS1_CORE0_TCMB	7850 0000h

Figure 4-856. START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
R/W															
0															

Access Types Legend

Table 4-2490. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	R/W	0h	TCMB start address

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MSS_TCMB_CR5A_END Registers

4.32.2 R5SSn_TCMB_END Register (Offset = FFFCh) [reset = h]

Short Description:

Long Description:

Return to Summary Table

Table 4-2491. Instance Table

Instance Name	Physical Address
R5SS0_CORE0_TCMB	7810 FFFCh
R5SS1_CORE0_TCMB	7850 FFFCh

Figure 4-857. END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
R/W															
0															

Access Types Legend

Table 4-2492. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	END	R/W	0h	TCMB end address

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Table 4-2493. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write

4.33 TCMB_CR5B Registers

Table 4-2494. R5SS[0:1]_CORE1_TCMB Registers Base Address Table

Offset	Length	Acronym	R5SS0_CORE1_TCMB Physical Address	R5SS1_CORE1_TCMB Physical Address
0h	32	TCMB_CR5B_START	7830 0000h	7870 0000h
7FFCh	32	TCMB_CR5B_END	7830 7FFCh	7870 7FFCh

Note

n = 0 to 1 for the TCM registers defined below.

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MSS_TCMA_CR5A_START Registers

4.33.1 R5SSn_TCMB_START Register (Offset = 0h) [reset = h]

Short Description:

Long Description:

Return to Summary Table

Table 4-2495. Instance Table

Instance Name	Physical Address
R5SS0_CORE1_TCMB	7830 0000h
R5SS1_CORE1_TCMB	7870 0000h

Figure 4-858. START Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START															
R/W															
0															

Access Types Legend

Table 4-2496. START Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	START	R/W	0h	TCMB start address

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MSS_TCMB_CR5B_END Registers

4.33.2 R5SSn_TCMB_END Register (Offset = 7FFCh) [reset = h]

Short Description:

Long Description:

Return to Summary Table

Table 4-2497. Instance Table

Instance Name	Physical Address
R5SS0_CORE1_TCMB	7830 7FFCh
R5SS1_CORE1_TCMB	7870 7FFCh

Figure 4-859. END Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END															
R/W															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END															
R/W															
0															

Access Types Legend

Table 4-2498. END Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	END	R/W	0h	TCMB end address

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Table 4-2499. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write

4.34 UART Registers

Table 4-2500. MSS_UART[0:2] Registers Base Address Table

Offset	Length	Acronym	MSS_UART0 Physical Address	MSS_UART1 Physical Address	MSS_UART2 Physical Address
0h	32	UART_DLL	5230 0000h	5230 1000h	5230 2000h
0h	32	UART_RHR	5230 0000h	5230 1000h	5230 2000h
0h	32	UART_THR	5230 0000h	5230 1000h	5230 2000h
4h	32	UART_DLH	5230 0004h	5230 1004h	5230 2004h
4h	32	UART_IER_CIR	5230 0004h	5230 1004h	5230 2004h
4h	32	UART_IER_IRDA	5230 0004h	5230 1004h	5230 2004h
4h	32	UART_IER_UART	5230 0004h	5230 1004h	5230 2004h
8h	32	UART_EFR	5230 0008h	5230 1008h	5230 2008h
8h	32	UART_FCR	5230 0008h	5230 1008h	5230 2008h
8h	32	UART_IIR_CIR	5230 0008h	5230 1008h	5230 2008h
8h	32	UART_IIR_IRDA	5230 0008h	5230 1008h	5230 2008h
8h	32	UART_IIR_UART	5230 0008h	5230 1008h	5230 2008h
Ch	32	UART_LCR	5230 000Ch	5230 100Ch	5230 200Ch
10h	32	UART_MCR	5230 0010h	5230 1010h	5230 2010h
10h	32	UART_XON1_ADDR1	5230 0010h	5230 1010h	5230 2010h
14h	32	UART_LSR_CIR	5230 0014h	5230 1014h	5230 2014h
14h	32	UART_LSR_IRDA	5230 0014h	5230 1014h	5230 2014h
14h	32	UART_LSR_UART	5230 0014h	5230 1014h	5230 2014h
14h	32	UART_XON2_ADDR2	5230 0014h	5230 1014h	5230 2014h
18h	32	UART_MSR	5230 0018h	5230 1018h	5230 2018h
18h	32	UART_TCR	5230 0018h	5230 1018h	5230 2018h
18h	32	UART_XOFF1	5230 0018h	5230 1018h	5230 2018h
1Ch	32	UART_SPR	5230 001Ch	5230 101Ch	5230 201Ch
1Ch	32	UART_TLR	5230 001Ch	5230 101Ch	5230 201Ch
1Ch	32	UART_XOFF2	5230 001Ch	5230 101Ch	5230 201Ch
20h	32	UART_MDR1	5230 0020h	5230 1020h	5230 2020h
24h	32	UART_MDR2	5230 0024h	5230 1024h	5230 2024h
28h	32	UART_SFLSR	5230 0028h	5230 1028h	5230 2028h
28h	32	UART_TXFLL	5230 0028h	5230 1028h	5230 2028h
2Ch	32	UART_RESUME	5230 002Ch	5230 102Ch	5230 202Ch
2Ch	32	UART_TXFLH	5230 002Ch	5230 102Ch	5230 202Ch
30h	32	UART_RXFLL	5230 0030h	5230 1030h	5230 2030h
30h	32	UART_SFREGL	5230 0030h	5230 1030h	5230 2030h
34h	32	UART_RXFLH	5230 0034h	5230 1034h	5230 2034h
34h	32	UART_SFREGH	5230 0034h	5230 1034h	5230 2034h
38h	32	UART_BLR	5230 0038h	5230 1038h	5230 2038h
38h	32	UART_UASR	5230 0038h	5230 1038h	5230 2038h
3Ch	32	UART_ACREG	5230 003Ch	5230 103Ch	5230 203Ch
40h	32	UART_SCR	5230 0040h	5230 1040h	5230 2040h
44h	32	UART_SSR	5230 0044h	5230 1044h	5230 2044h

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Table 4-2500. MSS_UART[0:2] Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_UART0 Physical Address	MSS_UART1 Physical Address	MSS_UART2 Physical Address
48h	32	UART_EBLR	5230 0048h	5230 1048h	5230 2048h
50h	32	UART_MVR	5230 0050h	5230 1050h	5230 2050h
54h	32	UART_SYSC	5230 0054h	5230 1054h	5230 2054h
58h	32	UART_SYSS	5230 0058h	5230 1058h	5230 2058h
5Ch	32	UART_WER	5230 005Ch	5230 105Ch	5230 205Ch
60h	32	UART_CFPS	5230 0060h	5230 1060h	5230 2060h
64h	32	UART_RXFIFO_LVL	5230 0064h	5230 1064h	5230 2064h
68h	32	UART_TXFIFO_LVL	5230 0068h	5230 1068h	5230 2068h
6Ch	32	UART_IER2	5230 006Ch	5230 106Ch	5230 206Ch
70h	32	UART_ISR2	5230 0070h	5230 1070h	5230 2070h
74h	32	UART_FREQ_SEL	5230 0074h	5230 1074h	5230 2074h
78h	32	UART_ABAUD_1ST_CHAR	5230 0078h	5230 1078h	5230 2078h
7Ch	32	UART_BAUD_2ND_CHAR	5230 007Ch	5230 107Ch	5230 207Ch
80h	32	UART_MDR3	5230 0080h	5230 1080h	5230 2080h
84h	32	UART_TX_DMA_THRESHOLD	5230 0084h	5230 1084h	5230 2084h
88h	32	UART_MDR4	5230 0088h	5230 1088h	5230 2088h
8Ch	32	UART_EFR2	5230 008Ch	5230 108Ch	5230 208Ch
90h	32	UART_ECR	5230 0090h	5230 1090h	5230 2090h
94h	32	UART_TIMEGUARD	5230 0094h	5230 1094h	5230 2094h
98h	32	UART_TIMEOUTL	5230 0098h	5230 1098h	5230 2098h
9Ch	32	UART_TIMEOUTH	5230 009Ch	5230 109Ch	5230 209Ch
A0h	32	UART_SCCR	5230 00A0h	5230 10A0h	5230 20A0h
A4h	32	UART_ERHR	5230 00A4h	5230 10A4h	5230 20A4h
A4h	32	UART_ETHR	5230 00A4h	5230 10A4h	5230 20A4h
A8h	32	UART_MAR	5230 00A8h	5230 10A8h	5230 20A8h
ACh	32	UART_MMR	5230 00ACh	5230 10ACh	5230 20ACh
B0h	32	UART_MBR	5230 00B0h	5230 10B0h	5230 20B0h

Table 4-2501. MSS_UART[3:5] Registers Base Address Table

Offset	Length	Acronym	MSS_UART3 Physical Address	MSS_UART4 Physical Address	MSS_UART5 Physical Address
0h	32	UART_DLL	5230 3000h	5230 4000h	5230 5000h
0h	32	UART_RHR	5230 3000h	5230 4000h	5230 5000h
0h	32	UART_THR	5230 3000h	5230 4000h	5230 5000h
4h	32	UART_DLH	5230 3004h	5230 4004h	5230 5004h
4h	32	UART_IER_CIR	5230 3004h	5230 4004h	5230 5004h
4h	32	UART_IER_IRDA	5230 3004h	5230 4004h	5230 5004h
4h	32	UART_IER_UART	5230 3004h	5230 4004h	5230 5004h
8h	32	UART_EFR	5230 3008h	5230 4008h	5230 5008h
8h	32	UART_FCR	5230 3008h	5230 4008h	5230 5008h
8h	32	UART_IIR_CIR	5230 3008h	5230 4008h	5230 5008h
8h	32	UART_IIR_IRDA	5230 3008h	5230 4008h	5230 5008h
8h	32	UART_IIR_UART	5230 3008h	5230 4008h	5230 5008h
Ch	32	UART_LCR	5230 300Ch	5230 400Ch	5230 500Ch
10h	32	UART_MCR	5230 3010h	5230 4010h	5230 5010h
10h	32	UART_XON1_ADDR1	5230 3010h	5230 4010h	5230 5010h

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Table 4-2501. MSS_UART[3:5] Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_UART3 Physical Address	MSS_UART4 Physical Address	MSS_UART5 Physical Address
14h	32	UART_LSR_CIR	5230 3014h	5230 4014h	5230 5014h
14h	32	UART_LSR_IRDA	5230 3014h	5230 4014h	5230 5014h
14h	32	UART_LSR_UART	5230 3014h	5230 4014h	5230 5014h
14h	32	UART_XON2_ADDR2	5230 3014h	5230 4014h	5230 5014h
18h	32	UART_MSR	5230 3018h	5230 4018h	5230 5018h
18h	32	UART_TCR	5230 3018h	5230 4018h	5230 5018h
18h	32	UART_XOFF1	5230 3018h	5230 4018h	5230 5018h
1Ch	32	UART_SPR	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	32	UART_TLR	5230 301Ch	5230 401Ch	5230 501Ch
1Ch	32	UART_XOFF2	5230 301Ch	5230 401Ch	5230 501Ch
20h	32	UART_MDR1	5230 3020h	5230 4020h	5230 5020h
24h	32	UART_MDR2	5230 3024h	5230 4024h	5230 5024h
28h	32	UART_SFLSR	5230 3028h	5230 4028h	5230 5028h
28h	32	UART_TXFLL	5230 3028h	5230 4028h	5230 5028h
2Ch	32	UART_RESUME	5230 302Ch	5230 402Ch	5230 502Ch
2Ch	32	UART_TXFLH	5230 302Ch	5230 402Ch	5230 502Ch
30h	32	UART_RXFLL	5230 3030h	5230 4030h	5230 5030h
30h	32	UART_SFREGL	5230 3030h	5230 4030h	5230 5030h
34h	32	UART_RXFLH	5230 3034h	5230 4034h	5230 5034h
34h	32	UART_SFREGH	5230 3034h	5230 4034h	5230 5034h
38h	32	UART_BLR	5230 3038h	5230 4038h	5230 5038h
38h	32	UART_UASR	5230 3038h	5230 4038h	5230 5038h
3Ch	32	UART_ACREG	5230 303Ch	5230 403Ch	5230 503Ch
40h	32	UART_SCR	5230 3040h	5230 4040h	5230 5040h
44h	32	UART_SSR	5230 3044h	5230 4044h	5230 5044h
48h	32	UART_EBLR	5230 3048h	5230 4048h	5230 5048h
50h	32	UART_MVR	5230 3050h	5230 4050h	5230 5050h
54h	32	UART_SYSC	5230 3054h	5230 4054h	5230 5054h
58h	32	UART_SYSS	5230 3058h	5230 4058h	5230 5058h
5Ch	32	UART_WER	5230 305Ch	5230 405Ch	5230 505Ch
60h	32	UART_CFPS	5230 3060h	5230 4060h	5230 5060h
64h	32	UART_RXFIFO_LVL	5230 3064h	5230 4064h	5230 5064h
68h	32	UART_TXFIFO_LVL	5230 3068h	5230 4068h	5230 5068h
6Ch	32	UART_IER2	5230 306Ch	5230 406Ch	5230 506Ch
70h	32	UART_ISR2	5230 3070h	5230 4070h	5230 5070h
74h	32	UART_FREQ_SEL	5230 3074h	5230 4074h	5230 5074h
78h	32	UART_ABAUD_1ST_CHAR	5230 3078h	5230 4078h	5230 5078h
7Ch	32	UART_BAUD_2ND_CHAR	5230 307Ch	5230 407Ch	5230 507Ch
80h	32	UART_MDR3	5230 3080h	5230 4080h	5230 5080h
84h	32	UART_TX_DMA_THRESHOLD	5230 3084h	5230 4084h	5230 5084h
88h	32	UART_MDR4	5230 3088h	5230 4088h	5230 5088h
8Ch	32	UART_EFR2	5230 308Ch	5230 408Ch	5230 508Ch
90h	32	UART_ECR	5230 3090h	5230 4090h	5230 5090h
94h	32	UART_TIMEGUARD	5230 3094h	5230 4094h	5230 5094h
98h	32	UART_TIMEOUTL	5230 3098h	5230 4098h	5230 5098h
9Ch	32	UART_TIMEOUTH	5230 309Ch	5230 409Ch	5230 509Ch

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Table 4-2501. MSS_UART[3:5] Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_UART3 Physical Address	MSS_UART4 Physical Address	MSS_UART5 Physical Address
A0h	32	UART_SCCR	5230 30A0h	5230 40A0h	5230 50A0h
A4h	32	UART_ERHR	5230 30A4h	5230 40A4h	5230 50A4h
A4h	32	UART_ETHR	5230 30A4h	5230 40A4h	5230 50A4h
A8h	32	UART_MAR	5230 30A8h	5230 40A8h	5230 50A8h
ACh	32	UART_MMR	5230 30ACh	5230 40ACh	5230 50ACh
B0h	32	UART_MBR	5230 30B0h	5230 40B0h	5230 50B0h

4.34.1 UART Instance Count Note

Note

n = 0 to 5 for the UART registers defined below.

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4.34.2 MSS_UARTn_DLL Registers

4.34.2.1 UARTn_DLL Register (Offset = 0h) [reset = 0h]

Short Description: Baud clock divisor LSB value register

Long Description: This register, with UART_DLH, stores the 14-bit divisor for generation of the baud clock in the baud rate generator. UART_DLH stores the most-significant part of the divisor. UART_DLL stores the least-significant part of the divisor.

Return to Summary Table

Table 4-2502. Instance Table

Instance Name	Physical Address
UART0	5230 0000h
UART1	5230 1000h
UART2	5230 2000h
UART3	5230 3000h
UART4	5230 4000h
UART5	5230 5000h

Figure 4-860. UART_DLL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CLOCK_LSB							
NONE								R/W							
0								0							

Access Types Legend

Table 4-2503. DLL Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	CLOCK_LSB	R/W	0h	Used to store the 8-bit LSB divisor value

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4.34.3 MSS_UARTn_RHR Registers

4.34.3.1 UARTn_RHR Register (Offset = 0h) [reset = 0h]

Short Description: Receiver holding register

Long Description: The receiver section consists of the receiver holding register (UART_RHR) and the receiver shift register. The UART_RHR is a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the UART_RHR. If the FIFO is disabled, location 0 of the FIFO stores the single data character. Note: If an overflow occurs, the data in the UART_RHR is not overwritten.

Return to Summary Table

Table 4-2504. Instance Table

Instance Name	Physical Address
UART0	5230 0000h
UART1	5230 1000h
UART2	5230 2000h
UART3	5230 3000h
UART4	5230 4000h
UART5	5230 5000h

Figure 4-861. UART_RHR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RHR							
R								R							
0								0							

Access Types Legend

Table 4-2505. RHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 0	RHR	R	0h	Receive holding register

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4.34.4 MSS_UARTn_THR Registers

4.34.4.1 UARTn_THR Register (Offset = 0h) [reset = 0h]

Short Description: Transmit holding register

Long Description: The transmitter section consists of the transmit holding register (UART_THR) and the transmit shift register. The UART_THR is a 64-byte FIFO. The local host (LH) writes data to the UART_THR. The data is placed in the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled, location 0 of the FIFO stores the data.

Return to Summary Table

Table 4-2506. Instance Table

Instance Name	Physical Address
UART0	5230 0000h
UART1	5230 1000h
UART2	5230 2000h
UART3	5230 3000h
UART4	5230 4000h
UART5	5230 5000h

Figure 4-862. UART_THR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								THR							
R								W							
0								0							

Access Types Legend

Table 4-2507. THR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 0	THR	W	0h	TRANSMIT HOLDING REGISTER

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4.34.5 MSS_UARTn_DLH Registers

4.34.5.1 UARTn_DLH Register (Offset = 4h) [reset = 0h]

Short Description: Baud clock divisor MSB value register

Long Description: This register, with UART_DLL, stores the 14-bit divisor for generating the baud clock in the baud rate generator. DLH stores the most-significant part of the divisor. DLL stores the least-significant part of the divisor

Return to Summary Table

Table 4-2508. Instance Table

Instance Name	Physical Address
UART0	5230 0004h
UART1	5230 1004h
UART2	5230 2004h
UART3	5230 3004h
UART4	5230 4004h
UART5	5230 5004h

Figure 4-863. UART_DLH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CLOCK_MSB							
NONE								R/W							
0								0							

Access Types Legend

Table 4-2509. DLH Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	CLOCK_MSB	R/W	0h	Used to store the 8-bit MSB divisor value

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4.34.6 MSS_UARTn_IER_CIR Registers

4.34.6.1 UARTn_IER_CIR Register (Offset = 4h) [reset = 0h]

Short Description: CIR mode interrupt enable register

Long Description: There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually. Notes: The RX_STOP_IT interrupt is generated based on the value set in the BOF Length register (UART_EBLR). In IR-CIR mode, contrary to the IR-IRDA mode, the TX_STATUS_IT has only one meaning corresponding to the case UART_MDR2[0] = 0.

Return to Summary Table

Table 4-2510. Instance Table

Instance Name	Physical Address
UART0	5230 0004h
UART1	5230 1004h
UART2	5230 2004h
UART3	5230 3004h
UART4	5230 4004h
UART5	5230 5004h

Figure 4-864. UART_IER_CIR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								NOT_USED2		TX_STATUS_IT	NOT_USED1	RX_OVERRUN_IT	RX_STOP_IT	THR_IT	RHR_IT
NONE								R/W		R/W	R/W	R/W	R/W	R/W	R/W
0								0		0	0	0	0	0	0

Access Types Legend

Table 4-2511. IER_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 6	NOT_USED2	R/W	0h	
5	TX_STATUS_IT	R/W	0h	1 | TX_STATUS_IT_Value_1 | Enables the TX status interrupt.
4	NOT_USED1	R/W	0h	
3	RX_OVERRUN_IT	R/W	0h	1 | RX_OVERRUN_IT_Value_1 | Enables the RX overrun interrupt.
2	RX_STOP_IT	R/W	0h	1 | RX_STOP_IT_Value_1 | Enables the receive stop interrupt.
1	THR_IT	R/W	0h	1 | THR_IT_Value_1 | Enables the THR interrupt.
0	RHR_IT	R/W	0h	1 | RHR_IT_Value_1 | Enables the RHR interrupt.

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4.34.7 MSS_UARTn_IER_IRDA Registers

4.34.7.1 UARTn_IER_RDA Register (Offset = 4h) [reset = 0h]

Short Description: IrDA mode interrupt enable register

Long Description: There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/ disabled individually. Note: The TX_STATUS_IT interrupt reflects two possible conditions. The UART_MDR2[0] should be read to determine the status in the event of this interrupt.

Return to Summary Table

Table 4-2512. Instance Table

Instance Name	Physical Address
UART0	5230 0004h
UART1	5230 1004h
UART2	5230 2004h
UART3	5230 3004h
UART4	5230 4004h
UART5	5230 5004h

Figure 4-865. UART_IER_IRDA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_TRIG_IT	RX_OVERRUN_IT	LAST_RX_BYTE_IT	THR_IT	RHR_IT
NONE								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2513. IER_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7	EOF_IT	R/W	0h	1 | EOF_IT_Value_1 | Enables the received EOF interrupt.
6	LINE_STS_IT	R/W	0h	1 | LINE_STS_IT_Value_1 | Enables the receiver line status interrupt.
5	TX_STATUS_IT	R/W	0h	1 | TX_STATUS_IT_Value_1 | Enables the TX status interrupt.
4	STS_FIFO_TRIG_IT	R/W	0h	1 | STS_FIFO_TRIG_IT_Value_1 | Enables the status FIFO trigger level interrupt.
3	RX_OVERRUN_IT	R/W	0h	1 | RX_OVERRUN_IT_Value_1 | Enables the RX overrun interrupt.
2	LAST_RX_BYTE_IT	R/W	0h	1 | LAST_RX_BYTE_IT_Value_1 | Enables the last byte of frame in RX FIFO interrupt.
1	THR_IT	R/W	0h	1 | THR_IT_Value_1 | Enables the THR interrupt.
0	RHR_IT	R/W	0h	1 | RHR_IT_Value_1 | Enables the RHR interrupt.

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4.34.8 MSS_UARTn_IER_UART Registers

4.34.8.1 UARTn_IER_UART Register (Offset = 4h) [reset = 0h]

Short Description: UART mode Interrupt Enable Register

Long Description: The interrupt enable register (UART_IER_UART) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, UART_RHR interrupt, UART_THR interrupt, XOFF received and CTS*/RTS* change of state from low to high. Each interrupt can be enabled/ disabled individually. There is also a sleep mode enable bit.

Return to Summary Table

Table 4-2514. Instance Table

Instance Name	Physical Address
UART0	5230 0004h
UART1	5230 1004h
UART2	5230 2004h
UART3	5230 3004h
UART4	5230 4004h
UART5	5230 5004h

Figure 4-866. UART_IER_UART Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CTS_IT	RTS_IT	XOFF_IT	SLEEP_MODE	MODEM_STS_IT	LINE_STS_IT	THR_IT	RHR_IT
R								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2515. IER_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED	R		
7	CTS_IT	R/W	0h	1 | CTS_IT_Value_1 | Enables the CTS* interrupt
6	RTS_IT	R/W	0h	1 | RTS_IT_Value_1 | Enables the RTS* interrupt
5	XOFF_IT	R/W	0h	1 | XOFF_IT_Value_1 | Enables the XOFF interrupt
4	SLEEP_MODE	R/W	0h	1 | SLEEP_MODE_Value_1 | Enables sleep mode (stop baud rate clock when the module is inactive)
3	MODEM_STS_IT	R/W	0h	1 | MODEM_STS_IT_Value_1 | Enables the modem status register interrupt
2	LINE_STS_IT	R/W	0h	1 | LINE_STS_IT_u_Value_1 | Enables the receiver line status interrupt
1	THR_IT	R/W	0h	1 | THR_IT_Value_1 | Enables the THR interrupt
0	RHR_IT	R/W	0h	1 | RHR_IT_Value_1 | Enables the RHR interrupt and time out interrupt.

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4.34.9 MSS_UARTn_EFR Registers

4.34.9.1 UARTn_EFR Register (Offset = 8h) [reset = 0h]

Short Description: Enhanced Feature Register

Long Description: This register enables or disables enhanced features. Most of the enhanced functions apply only to UART modes, but UART_EFR[4] enables write accesses to UART_FCR[5:4], the TX trigger level, which is also used in IrDA modes.

Return to Summary Table

Table 4-2516. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 4-867. UART_EFR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								AUTO_CTS_EN	AUTO_RTS_EN	SPECIAL_CHAR_DETECT	ENHANCED_EN	SW_FLOW_CONTROL			
NONE								R/W	R/W	R/W	R/W	R/W			
0								0	0	0	0	0			

Access Types Legend

Table 4-2517. EFR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7	AUTO_CTS_EN	R/W	0h	Auto-CTS enable bit. 0: Normal operation. 1: Auto-CTS flow control is enabled i.e. transmission is halted when the CTS* pin is high (inactive).
6	AUTO_RTS_EN	R/W	0h	Auto-RTS enable bit. 0: Normal operation. 1: Auto- RTS flow control is enabled i.e. RTS* pin goes high (inactive) when the receiver FIFO HALT trigger level, TCR[3:0], is reached, and goes low (active) when the receiver FIFO RESTORE transmission trigger level is reached.
5	SPECIAL_CHAR_DETECT	R/W	0h	0: Normal operation. 1: Special character detect enable. Received data is compared with XOFF2 data. If a match occurs the received data is transferred to RX FIFO and IIR bit 4 is set to 1 to indicate a special character has been detected.
4	ENHANCED_EN	R/W	0h	Enhanced functions write enable bit. 0: Disables writing to IER bits 4-7, FCR bits 4-5, and MCR bits 5-7. 1: Enables writing to IER bits 4-7, FCR bits 4-5, and MCR bits 5-7.
3 - 0	SW_FLOW_CONTROL	R/W	0h	Combinations of Software flow control can be selected by programming bit 3 - bit 0. See Software Flow Control Options

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4.34.10 MSS_UARTn_FCR Registers

4.34.10.1 UARTn_FCR Register (Offset = 8h) [reset = 0h]

Short Description: FIFO control register

Long Description: Bits 4 and 5 can only be written to when UART_EFR[4] = 1. Bits 0 and 3 can be changed only when the baud clock is not running (DLL and DLH set to 0). See UART TX FIFO Trigger Level Setting Summary Table for UART_FCR[5:4] setting restriction when UART_SCR[6] = 1. See UART RX FIFO Trigger-Level Setting Summary Table for UART_FCR[7:6] setting restriction when UART_SCR[7] = 1.

Return to Summary Table

Table 4-2518. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 4-868. UART_FCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RX_FIFO_TRIG		TX_FIFO_TRIG		DMA_MODE	TX_FIFO_CLEAR	RX_FIFO_CLEAR	FIFO_EN
R								W		W		W	W	W	W
0								0		0		0	0	0	0

Access Types Legend

Table 4-2519. FCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 6	RX_FIFO_TRIG	W	0h	Sets the trigger level for the RX FIFO: If SCR[7] = 0 and TLR[7:4] = 0000: 00: 8 characters 01: 16 characters 10: 56 characters 11: 60 characters If SCR[7] = 0 and TLR[7:4] != 0000, RX_FIFO_TRIG is not considered. If SCR[7]=1, RX_FIFO_TRIG is 2 LSB of the trigger level [1-63 on 6 bits] with the granularity 1.
5 - 4	TX_FIFO_TRIG	W	0h	Sets the trigger level for the TX FIFO: If SCR[6] = 0 and TLR[3:0] = 0000: 00: 8 spaces 01: 16 spaces 10: 32 spaces 11: 56 spaces If SCR[6] = 0 and TLR[3:0] != 0000, TX_FIFO_TRIG is not considered. If SCR[6]=1, TX_FIFO_TRIG is 2 LSB of the trigger level [1-63 on 6 bits] with the granularity 1
3	DMA_MODE	W	0h	This register is considered if SCR[0] = 0. 1 | DMA_MODE_Value_1 | DMA_MODE 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX)
2	TX_FIFO_CLEAR	W	0h	1 | TX_FIFO_CLEAR_Value_1 | Clears the transmit FIFO and resets its counter logic to zero. Returns to zero after clearing FIFO.
1	RX_FIFO_CLEAR	W	0h	1 | RX_FIFO_CLEAR_Value_1 | Clears the receive FIFO and resets its counter logic to zero. Returns to zero after clearing FIFO.

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Table 4-2519. FCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FIFO_EN	W	0h	1 | FIFO_EN_Value_1 | : Enables the transmit and receive FIFOs.The transmit and receive holding registers are 64-bytes FIFOs.

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4.34.11 MSS_UARTn_IIR_CIR Registers

4.34.11.1 UARTn_IIR_CIR Register (Offset = 8h) [reset = 0h]

Short Description: CIR mode interrupt identification register

Long Description: The interrupt line is activated whenever one of the 6 interrupts is active/

Return to Summary Table

Table 4-2520. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 4-869. UART_IIR_CIR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										TX_STATUS_IT	RESERVED	RX_OE_IT	RX_STOP_IT	THR_IT	RHR_IT
NONE										R	NONE	R	R	R	R
0										0	0	0	0	0	0

Access Types Legend

Table 4-2521. IIR_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
5	TX_STATUS_IT	R	0h	1 | TX_STATUS_IT_Value_1 | TX status interrupt active
	RESERVED	NONE		Reserved
3	RX_OE_IT	R	0h	1 | RX_OE_IT_Value_1 | RX overrun interrupt active
2	RX_STOP_IT	R	0h	1 | RX_STOP_IT_Value_1 | Receive stop interrupt active
1	THR_IT	R	0h	1 | THR_IT_Value_1 | THR interrupt active
0	RHR_IT	R	0h	1 | RHR_IT_Value_1 | RHR interrupt active

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4.34.12 MSS_UARTn_IIR_IRDA Registers

4.34.12.1 UARTn_IIR_IRDA Register (Offset = 8h) [reset = 0h]

Short Description: IrDA mode interrupt enable register

Long Description: There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/ disabled individually. Note: The TX_STATUS_IT interrupt reflects two possible conditions. The UART_MDR2[0] should be read to determine the status in the event of this interrupt.

Return to Summary Table

Table 4-2522. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 4-870. UART_IIR_IRDA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								EOF_IT	LINE_STS_IT	TX_STATUS_IT	STS_FIFO_IT	RX_OE_IT	RX_FIFO_LAST_BYTE_IT	THR_IT	RHR_IT
NONE								R	R	R	R	R	R	R	R
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2523. IIR_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7	EOF_IT	R	0h	1 | EOF_IT_Value_1 | Received EOF interrupt active
6	LINE_STS_IT	R	0h	1 | LINE_STS_IT_Value_1 | Receiver line status interrupt active
5	TX_STATUS_IT	R	0h	1 | TX_STATUS_IT_Value_1 | TX status interrupt active
4	STS_FIFO_IT	R	0h	1 | STS_FIFO_IT_Value_1 | Status FIFO trigger level interrupt active
3	RX_OE_IT	R	0h	1 | RX_OE_IT_Value_1 | RX overrun interrupt active
2	RX_FIFO_LAST_BYTE_IT	R	0h	1 | RX_FIFO_LAST_BYTE_IT_Value_1 | Last byte of frame in RX FIFO interrupt active
1	THR_IT	R	0h	1 | THR_IT_Value_1 | THR interrupt active
0	RHR_IT	R	0h	1 | RHR_IT_Value_1 | RHR interrupt active

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4.34.13 MSS_UARTn_IIR_UART Registers

4.34.13.1 UARTn_IR_UART Register (Offset = 8h) [reset = 1h]

Short Description: UART mode interrupt identification register

Long Description: The UART_IIR_UART is a read-only register that provides the source of the interrupt in a prioritized manner.

Return to Summary Table

Table 4-2524. Instance Table

Instance Name	Physical Address
UART0	5230 0008h
UART1	5230 1008h
UART2	5230 2008h
UART3	5230 3008h
UART4	5230 4008h
UART5	5230 5008h

Figure 4-871. UART_IIR_UART Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								FCR_MIRROR		IT_TYPE					IT_PENDING
R								R		R					R
0								0		0					1

Access Types Legend

Table 4-2525. IIR_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 6	FCR_MIRROR	R	0h	Mirror the contents of FCR[0] on both bits.
5 - 1	IT_TYPE	R	0h	16 | IT_TYPE_Value_10 | CTS, RTS, DSR change state from active (low) to inactive (high). Priority=6 8 | IT_TYPE_Value_8 | Xoff/Special character. Priority=5 6 | IT_TYPE_Value_6 | Rx timeout. Priority=2 3 | IT_TYPE_Value_3 | Receiver line status error. Priority=3 2 | IT_TYPE_Value_2 | RHR interrupt. Priority=2 1 | IT_TYPE_Value_1 | THR interrupt. Priority=3
0	IT_PENDING	R	1h	1 | IT_PENDING_Value_1 | No interrupt is pending

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4.34.14 MSS_UARTn_LCR Registers

4.34.14.1 UARTn_LCR Register (Offset = Ch) [reset = 0h]

Short Description: Line control register

Long Description: Line control register UART_LCR[6:0] define transmission and reception parameters. Note: When UART_LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as UART_LCR[6] = 1.

Return to Summary Table

Table 4-2526. Instance Table

Instance Name	Physical Address
UART0	5230 000Ch
UART1	5230 100Ch
UART2	5230 200Ch
UART3	5230 300Ch
UART4	5230 400Ch
UART5	5230 500Ch

Figure 4-872. UART_LCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								DIV_EN	BREAK_EN	PARITY_TYPE2	PARITY_TYPE1	PARITY_EN	NB_STOP	CHAR_LENGTH	
R								R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0								0	0	0	0	0	0	0	

Access Types Legend

Table 4-2527. LCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7	DIV_EN	R/W	0h	1 | DIV_EN_Value_1 | Divisor latch enable. Allows to access to DLL, DLH and other registers (refer to the registers mapping)
6	BREAK_EN	R/W	0h	Break control bit. 1 | BREAK_EN_Value_1 | Forces the transmitter output to go low to alert the communication terminal
5	PARITY_TYPE2	R/W	0h	Selects the forced parity format [if LCR[3] = 1]. If LCR[5] = 1 and LCR[4] = 0, the parity bit is forced to 1 in the transmitted and received data. If LCR[5] = 1 and LCR[4] = 1, the parity bit is forced to 0 in the transmitted and received data.
4	PARITY_TYPE1	R/W	0h	1 | PARITY_TYPE1_Value_1 | Even parity is generated (if LCR[3] = 1)
3	PARITY_EN	R/W	0h	1 | PARITY_EN_Value_1 | A parity bit is generated during transmission and the receiver checks for received parity.
2	NB_STOP	R/W	0h	Specifies the number of stop bits: 1 | NB_STOP_Value_1 | 1.5 stop bits (word length = 5) in USART mode. 2 stop bits (word length = 6, 7, 8)
1 - 0	CHAR_LENGTH	R/W	0h	Specifies the word length to be transmitted or received. 3 | CHAR_LENGTH_Value_3 | 8 bits 2 | CHAR_LENGTH_Value_2 | 7 bits 1 | CHAR_LENGTH_Value_1 | 6 bits

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4.34.15 MSS_UARTn_MCR Registers

4.34.15.1 UARTn_MCR Register (Offset = 10h) [reset = 0h]

Short Description: Modem control register

Long Description: Modem control register UART_MCR[3:0] controls the interface with the modem, data set, or peripheral device that emulates the modem.

Return to Summary Table

Table 4-2528. Instance Table

Instance Name	Physical Address
UART0	5230 0010h
UART1	5230 1010h
UART2	5230 2010h
UART3	5230 3010h
UART4	5230 4010h
UART5	5230 5010h

Figure 4-873. UART_MCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED	TCR_TLR	XON_EN	LOOPBACK_EN	CD_STS_CH	RI_STS_CH	RTS	DTR
R								R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2529. MCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7	RESERVED	R		
6	TCR_TLR	R/W	0h	1 | TCR_TLR_Value_1 | Enables access to the TCR and TLR registers.
5	XON_EN	R/W	0h	1 | XON_EN_Value_1 | Enable 'XON any' function
4	LOOPBACK_EN	R/W	0h	1 | LOOPBACK_EN_Value_1 | Enable local loopback mode (internal). In this mode the MCR[3:0] signals are looped back into MSR[7:4]. The transmit output is looped back to the receive input internally
3	CD_STS_CH	R/W	0h	1 | CD_STS_CH_Value_1 | In loopback forces DCD* input low and IRQ outputs to inactive state.
2	RI_STS_CH	R/W	0h	1 | RI_STS_CH_Value_1 | In loopback forces RI* input low.
1	RTS	R/W	0h	In loop back controls MSR[4]. If auto-RTS is enabled the RTS* output is controlled by hardware flow control. 1 | RTS_Value_1 | Force RTS* output to active (low).
0	DTR	R/W	0h	1 | DTR_Value_1 | Force DTR* output to active (low).

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4.34.16 MSS_UARTn_XON1_ADDR1 Registers

4.34.16.1 UARTn_XON1_ADDR1 Register (Offset = 10h) [reset = 0h]

Short Description: UART mode XON1 character, IrDA mode ADDR1 address register

Long Description: UART mode: XON1 character, IrDA mode: ADDR1 address

Return to Summary Table

Table 4-2530. Instance Table

Instance Name	Physical Address
UART0	5230 0010h
UART1	5230 1010h
UART2	5230 2010h
UART3	5230 3010h
UART4	5230 4010h
UART5	5230 5010h

Figure 4-874. UART_XON1_ADDR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								XON_WORD1							
NONE								R/W							
0								0							

Access Types Legend

Table 4-2531. XON1_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	XON_WORD1	R/W	0h	Used to store the 8-bit XON1 character in UART modes and ADDR1 address 1 for IrDA modes.

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4.34.17 MSS_UARTn_LSR_CIR Registers

4.34.17.1 UARTn_LSR_CIR Register (Offset = 14h) [reset = 81h]

Short Description: CIR mode line status register

Long Description: CIR mode line status register

Return to Summary Table

Table 4-2532. Instance Table

Instance Name	Physical Address
UART0	5230 0014h
UART1	5230 1014h
UART2	5230 2014h
UART3	5230 3014h
UART4	5230 4014h
UART5	5230 5014h

Figure 4-875. UART_LSR_CIR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								THR_EMPTY	RESERVED	RX_STOP	RESERVED				RX_FIFO_E
NONE								R	R	R	NONE				R
0								1	0	0	0				1

Access Types Legend

Table 4-2533. LSR_CIR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7	THR_EMPTY	R	1h	1 | THR_EMPTY_Value_1 | Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed
6	RESERVED	R		
5	RX_STOP	R	0h	The RX_STOP is generated based on the value set in the BOF Length register (EBLR). It is cleared on a single read of the LSR register 1 | RX_STOP_Value_1 | Reception is completed
	RESERVED	NONE		Reserved
0	RX_FIFO_E	R	1h	1 | RX_FIFO_E_Value_1 | At least one data character in the RX FIFO

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4.34.18 MSS_UARTn_LSR_IRDA Registers

4.34.18.1 UARTn_LSR_IRDA Register (Offset = 14h) [reset = 83h]

Short Description: IrDA mode line status register

Long Description: When the LSR is read, LSR[4:2] reflect the error bits [FL, CRC, ABORT] of the frame at the top of the STATUS FIFO (next frame status to be read).

Return to Summary Table

Table 4-2534. Instance Table

Instance Name	Physical Address
UART0	5230 0014h
UART1	5230 1014h
UART2	5230 2014h
UART3	5230 3014h
UART4	5230 4014h
UART5	5230 5014h

Figure 4-876. UART_LSR_IRDA Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								THR_EMPTY	STS_FIFO_FULL	RX_LAST_BYTE	FRAME_TOO_LONG	ABORT	CRC	STS_FIFO_E	RX_FIFO_E
NONE								R	R	R	R	R	R	R	R
0								1	0	0	0	0	0	1	1

Access Types Legend

Table 4-2535. LSR_IRDA Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7	THR_EMPTY	R	1h	1 | THR_EMPTY_Value_1 | Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed
6	STS_FIFO_FULL	R	0h	1 | STS_FIFO_FULL_Value_1 | Status FIFO full
5	RX_LAST_BYTE	R	0h	1 | RX_LAST_BYTE_Value_1 | The RX FIFO (RHR) contains the last byte of the frame to be read.This bit is only set when the last byte of a frame is available to be read. It is used to determine the frame boundary. It is cleared on a single read of the LSR register
4	FRAME_TOO_LONG	R	0h	1 | FRAME_TOO_LONG_Value_1 | Frame-too-long error in the frame at the top of the STATUS FIFO, [next character to be read]. This bit is set to 1 when a frame exceeding the maximum length (set by RXFLH and RXFLL registers) has been received. When this error is detected, current frame reception is terminated. Reception is stopped until the next START flag is detected
3	ABORT	R	0h	1 | ABORT_Value_1 | Abort pattern is received. SIR & MIR: Abort pattern. FIR: Illegal symbol
2	CRC	R	0h	1 | CRC_Value_1 | CRC error in the frame at the top of the STATUS FIFO (next character to be read)
1	STS_FIFO_E	R	1h	1 | STS_FIFO_E_Value_1 | Status FIFO empty

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Table 4-2535. LSR_IRDA Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RX_FIFO_E	R	1h	1 | RX_FIFO_E_Value_1 | At least one data character in the RX FIFO

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4.34.19 MSS_UARTn_LSR_UART Registers

4.34.19.1 UARTn_LSR_UART Register (Offset = 14h) [reset = 60h]

Short Description: UART mode line status register

Long Description: UART mode line status register

Return to Summary Table

Table 4-2536. Instance Table

Instance Name	Physical Address
UART0	5230 0014h
UART1	5230 1014h
UART2	5230 2014h
UART3	5230 3014h
UART4	5230 4014h
UART5	5230 5014h

Figure 4-877. UART_LSR_UART Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RX_FIFO_STS	TX_SR_E	TX_FIFO_E	RX_BI	RX_FE	RX_PE	RX_OE	RX_FIFO_E
R								R	R	R	R	R	R	R	R
0								0	1	1	0	0	0	0	0

Access Types Legend

Table 4-2537. LSR_UART Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7	RX_FIFO_STS	R	0h	1 | RX_FIFO_STS_Value_1 | At least one parity error, framing error or break indication in the RX FIFO. Bit 7 is cleared when no more errors are present in the RX FIFO.
6	TX_SR_E	R	1h	1 | TX_SR_E_Value_1 | Transmitter hold (TX FIFO) and shift registers are empty
5	TX_FIFO_E	R	1h	1 | TX_FIFO_E_Value_1 | Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed.
4	RX_BI	R	0h	1 | RX_BI_Value_1 | A break was detected while the data being read from the RX FIFO was being received. (i.e. RX input was low for one character + 1 bit time frame).
3	RX_FE	R	0h	1 | RX_FE_Value_1 | Framing error occurred in data being read from RX FIFO.(received data did not have a valid stop bit)
2	RX_PE	R	0h	1 | RX_PE_Value_1 | Parity error in data being read from RX FIFO
1	RX_OE	R	0h	1 | RX_OE_Value_1 | Overrun error has occurred. Set when the character held in the receive shift register is not transferred to the RX FIFO. This case can occurs only when receive FIFO is full.
0	RX_FIFO_E	R	0h	1 | RX_FIFO_E_Value_1 | At least one data character in the RX FIFO

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4.34.20 MSS_UARTn_XON2_ADDR2 Registers

4.34.20.1 UARTn_XON2_ADDR2 Register (Offset = 14h) [reset = 0h]

Short Description: UART mode XON2 character, IrDA mode ADDR2 address register

Long Description: Stores the 8-bit XON2 character in UART moldes and ADDR2 address 2 for IrDA modes

Return to Summary Table

Table 4-2538. Instance Table

Instance Name	Physical Address
UART0	5230 0014h
UART1	5230 1014h
UART2	5230 2014h
UART3	5230 3014h
UART4	5230 4014h
UART5	5230 5014h

Figure 4-878. UART_XON2_ADDR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								XON_WORD2							
NONE								R/W							
0								0							

Access Types Legend

Table 4-2539. XON2_ADDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	XON_WORD2	R/W	0h	Used to store the 8-bit XON2 character in UART modes and ADDR2 address 2 for IrDA modes.

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4.34.21 MSS_UARTn_MSR Registers

4.34.21.1 UARTn_MSR Register (Offset = 18h) [reset = 0h]

Short Description: Modem status register for UART mode only

Long Description: This register provides information about the current state of the control lines from the modem, data set, or peripheral device to the LH. It also indicates when a control input from the modem changes state.

Return to Summary Table

Table 4-2540. Instance Table

Instance Name	Physical Address
UART0	5230 0018h
UART1	5230 1018h
UART2	5230 2018h
UART3	5230 3018h
UART4	5230 4018h
UART5	5230 5018h

Figure 4-879. UART_MSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								NCD_STS	NRI_STS	NDSR_STS	NCTS_STS	DCD_STS	RI_STS	DSR_STS	CTS_STS
R								R	R	R	R	R	R	R	R
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2541. MSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7	NCD_STS	R	0h	This bit is the complement of the DCD* input. In loop-back mode it is equivalent to MCR[3]
6	NRI_STS	R	0h	This bit is the complement of the RI* input. In loop-back mode it is equivalent to MCR[2]
5	NDSR_STS	R	0h	This bit is the complement of the DSR* input. In loop-back mode, it is equivalent to MCR[0]
4	NCTS_STS	R	0h	This bit is the complement of the CTS* input. In loop-back mode it is equivalent to MCR[1]
3	DCD_STS	R	0h	Indicates that DCD* input [or MCR[3] in loop back] has changed. Cleared on a read.
2	RI_STS	R	0h	Indicates that RI* input [or MCR[2] in loop back] has changed state from low to high. Cleared on a read.
1	DSR_STS	R	0h	1 | DSR_STS_Value_1 | Indicates that DSR* input (or MCR[0] in loop back) has changed state. Cleared on a read
0	CTS_STS	R	0h	1 | CTS_STS_Value_1 | Indicates that CTS* input (or MCR[1] in loop back) has changed state. Cleared on a read.

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4.34.22 MSS_UARTn_TCR Registers

4.34.22.1 UARTn_TCR Register (Offset = 18h) [reset = fh]

Short Description: Transmission control register

Long Description: This register stores the RX FIFO threshold levels to start/stop transmission during hardware/software flow control. Notes: Trigger levels from 0 to 60 bytes are available with a granularity of 4. (Trigger level = 4 x [4-bit register value]) The programmer must ensure that UART_TCR[3:0] > UART_TCR[7:4] when auto-RTS or software flow control is enabled to avoid a mis-operation of the device. In FIFO interrupt mode with flow control, the programmer must ensure that the trigger level to halt transmission is greater than or equal to the RX FIFO trigger level (UART_TLR[7:4] or UART_FCR[7:6]); otherwise, FIFO operation stalls. In FIFO DMA mode with flow control, this concept does not exist because a DMA request is sent each time a byte is received.

Return to Summary Table

Table 4-2542. Instance Table

Instance Name	Physical Address
UART0	5230 0018h
UART1	5230 1018h
UART2	5230 2018h
UART3	5230 3018h
UART4	5230 4018h
UART5	5230 5018h

Figure 4-880. UART_TCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_FIFO_TRIG_START				RX_FIFO_TRIG_HALT			
NONE								R/W				R/W			
0								0				1111			

Access Types Legend

Table 4-2543. TCR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 4	RX_FIFO_TRIG_START	R/W	0h	RX FIFO trigger level to RESTORE transmission (0 - 60)
3 - 0	RX_FIFO_TRIG_HALT	R/W	Fh	RX FIFO trigger level to HALT transmission (0 - 60)

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4.34.23 MSS_UARTn_XOFF1 Registers

4.34.23.1 UARTn_XOFF1 Register (Offset = 18h) [reset = 0h]

Short Description: UART mode XOFF1 character

Long Description: UART mode XOFF1 character

Return to Summary Table

Table 4-2544. Instance Table

Instance Name	Physical Address
UART0	5230 0018h
UART1	5230 1018h
UART2	5230 2018h
UART3	5230 3018h
UART4	5230 4018h
UART5	5230 5018h

Figure 4-881. UART_XOFF1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								XOFF_WORD1							
NONE								R/W							
0								0							

Access Types Legend

Table 4-2545. XOFF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	XOFF_WORD1	R/W	0h	Used to store the 8-bit XOFF1 character in used in UART modes.

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4.34.24 MSS_UARTn_SPR Registers

4.34.24.1 UARTn_SPR Register (Offset = 1Ch) [reset = 0h]

Short Description: Scratchpad register

Long Description: This read/write register does not control the module. It is a scratchpad register to be used by the programmer to hold temporary data.

Return to Summary Table

Table 4-2546. Instance Table

Instance Name	Physical Address
UART0	5230 001Ch
UART1	5230 101Ch
UART2	5230 201Ch
UART3	5230 301Ch
UART4	5230 401Ch
UART5	5230 501Ch

Figure 4-882. UART_SPR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								SPR_WORD							
R								R/W							
0								0							

Access Types Legend

Table 4-2547. SPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 0	SPR_WORD	R/W	0h	Scratchpad register

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4.34.25 MSS_UARTn_TLR Registers

4.34.25.1 UARTn_TLR Register (Offset = 1Ch) [reset = 0h]

Short Description: Trigger level register

Long Description: This register stores the programmable transmit and RX FIFO trigger levels for DMA and IRQ generation.

Return to Summary Table

Table 4-2548. Instance Table

Instance Name	Physical Address
UART0	5230 001Ch
UART1	5230 101Ch
UART2	5230 201Ch
UART3	5230 301Ch
UART4	5230 401Ch
UART5	5230 501Ch

Figure 4-883. UART_TLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RX_FIFO_TRIG_DMA				TX_FIFO_TRIG_DMA			
NONE								R/W				R/W			
0								0				0			

Access Types Legend

Table 4-2549. TLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 4	RX_FIFO_TRIG_DMA	R/W	0h	Receive FIFO trigger level
3 - 0	TX_FIFO_TRIG_DMA	R/W	0h	Transmit FIFO trigger level

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4.34.26 MSS_UARTn_XOFF2 Registers

4.34.26.1 UARTn_XOFF2 Register (Offset = 1Ch) [reset = 0h]

Short Description: UART mode XOFF2 character

Long Description: UART mode XOFF2 character

Return to Summary Table

Table 4-2550. Instance Table

Instance Name	Physical Address
UART0	5230 001Ch
UART1	5230 101Ch
UART2	5230 201Ch
UART3	5230 301Ch
UART4	5230 401Ch
UART5	5230 501Ch

Figure 4-884. UART_XOFF2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								XOFF_WORD2							
NONE								R/W							
0								0							

Access Types Legend

Table 4-2551. XOFF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	XOFF_WORD2	R/W	0h	Used to store the 8-bit XOFF2 character in used in UART modes.

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4.34.27 MSS_UARTn_MDR1 Registers

4.34.27.1 UARTn_MDR1 Register (Offset = 20h) [reset = 7h]

Short Description: Mode definition register 1

Long Description: The mode of operation can be programmed by writing to MDR1[2:0] and therefore the UART_MDR1 must be programmed on startup after configuration of the configuration registers (UART_DLL, UART_DLH, and UART_LCR). The value of MDR1[2:0] must not be changed again during normal operation. Note: If the module is disabled by setting the MODE_SELECT field to 111, interrupt requests can still be generated unless disabled through the interrupt enable register (UART_IER). In this case, UART mode interrupts are visible. Reading the interrupt identification register (UART_IIR) shows UART mode interrupt flags.

Return to Summary Table

Table 4-2552. Instance Table

Instance Name	Physical Address
UART0	5230 0020h
UART1	5230 1020h
UART2	5230 2020h
UART3	5230 3020h
UART4	5230 4020h
UART5	5230 5020h

Figure 4-885. UART_MDR1 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								FRAME_END_MODE	SIP_MODE	SCT	SET_TXIR	IR_SLEEP	MODE_SELECT		
R								R/W	R/W	R/W	R/W	R/W	R/W		
0								0	0	0	0	0	111		

Access Types Legend

Table 4-2553. MDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7	FRAME_END_MODE	R/W	0h	IrDA mode only. 1 | FRAME_END_MODE_Value_1 | Set EOT bit method
6	SIP_MODE	R/W	0h	MIR/FIR modes only. 1 | SIP_MODE_Value_1 | Automatic SIP mode: SIP is generated after each transmission.
5	SCT	R/W	0h	Store and control the transmission 1 | SCT_Value_1 | Starts the Infrared transmission with the control of ACREG[2]. Note: before starting any transmission, there must be no reception on going.
4	SET_TXIR	R/W	0h	Used to configure the infrared transceiver. 1 | SET_TXIR_Value_1 | TXIR pin output is forced high (not dependant of MDR2[7] value).
3	IR_SLEEP	R/W	0h	1 | IR_SLEEP_Value_1 | IrDA/CIR sleep mode enabled

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Table 4-2553. MDR1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2 - 0	MODE_SELECT	R/W	7h	7 | MODE_SELECT_Value_7 | Disable (default state) 6 | MODE_SELECT_Value_6 | CIR mode 5 | MODE_SELECT_Value_5 | FIR mode 4 | MODE_SELECT_Value_4 | MIR mode 3 | MODE_SELECT_Value_3 | UART 13x mode 2 | MODE_SELECT_Value_2 | UART 16x auto-baud 1 | MODE_SELECT_Value_1 | SIR mode

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4.34.28 MSS_UARTn_MDR2 Registers

4.34.28.1 UARTn_MDR2 Register (Offset = 24h) [reset = 0h]

Short Description: Mode definition register 2

Long Description: IR-IrDA and IR-CIR modes only. UART_MDR2[0] describes the status of the interrupt in UART_IIR[5]. The IRTX_UNDERRUN bit should be read after an UART_IIR[5] TX_STATUS_IT interrupt. The bits [2:1] of this register set the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in UART_MDR1[2:0].

Note

The UART_MDR2[6] gives the flexibility to invert the RX pin in the UART to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most transceivers invert the IR receive pin.

Return to Summary Table

Table 4-2554. Instance Table

Instance Name	Physical Address
UART0	5230 0024h
UART1	5230 1024h
UART2	5230 2024h
UART3	5230 3024h
UART4	5230 4024h
UART5	5230 5024h

Figure 4-886. UART_MDR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								SET_TXIR_ALT	IRRXINVERT	CIR_PULSE_MODE		UART_PULSE	STS_FIFO_TRIG		IRTX_UNDERRUN
R								R/W	R/W	R/W		R/W	R/W		R
0								0	0	0		0	0		0

Access Types Legend

Table 4-2555. MDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7	SET_TXIR_ALT	R/W	0h	Provide alternate functionnality for MDR1[4] [SET_TXIR] 1 | SET_TXIR_ALT_Value_1 | Alternate mode for SET_TXIR
6	IRRXINVERT	R/W	0h	Only for IR mode [IRDA & CIR]Invert RX pin inside the module before the voting or sampling system logic of the infra red block. This will not affect the RX path in UART Modem modes. 1 | IRRXINVERT_Value_1 | No inversion is performed
5 - 4	CIR_PULSE_MODE	R/W	0h	CIR Pulse modulation definition. It defines high level of the pulse width associated with a digit: 3 | CIR_PULSE_MODE_Value_3 | Pulse width of 6 from 12 cycles 2 | CIR_PULSE_MODE_Value_2 | Pulse width of 5 from 12 cycles 1 | CIR_PULSE_MODE_Value_1 | Pulse width of 4 from 12 cycles
3	UART_PULSE	R/W	0h	UART mode only. Used to allow pulse shaping in UART mode. 1 | UART_PULSE_Value_1 | UART mode with a pulse shaping

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Table 4-2555. MDR2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2 - 1	STS_FIFO_TRIG	R/W	0h	Only for IR-IRDA mode. Frame Status FIFO Threshold select: 3 | STS_FIFO_TRIG_Value_3 | 8 entries 2 | STS_FIFO_TRIG_Value_2 | 7 entries 1 | STS_FIFO_TRIG_Value_1 | 4 entries
0	IRTX_UNDERRUN	R	0h	IRDA Transmission status interrupt.When the IIR[5] interrupt occurs, the meaning of the interrupt is : 1 | IRTX_UNDERRUN_Value_1 | an underrun has occurred. The last bit of the frame has been transmitted but with an underrun error present. The bit is reset to '0' when the RESUME register is read.

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4.34.29 MSS_UARTn_SFLSR Registers

4.34.29.1 UARTn_SFLSR Register (Offset = 28h) [reset = 0h]

Short Description: Status FIFO line status register

Long Description: IrDA modes only. Reading this register effectively reads frame status information from the status FIFO (this register does not physically exist). Reading this register increments the status FIFO read pointer (UART_SFREGL and UART_SFREGH must be read first).

Return to Summary Table

Table 4-2556. Instance Table

Instance Name	Physical Address
UART0	5230 0028h
UART1	5230 1028h
UART2	5230 2028h
UART3	5230 3028h
UART4	5230 4028h
UART5	5230 5028h

Figure 4-887. UART_SFLSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED5			OE_ERROR	FRAME_TOO_LONG_ERROR	ABORT_DETECT	CRC_ERROR	RESERVED0
R								R			R	R	R	R	R
0								0			0	0	0	0	0

Access Types Legend

Table 4-2557. SFLSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 5	RESERVED5	R	0h	
4	OE_ERROR	R	0h	1 | OE_ERROR_Value_1 | Overrun error in RX FIFO when frame at top of RX FIFO was received.
3	FRAME_TOO_LONG_ERROR	R	0h	1 | FRAME_TOO_LONG_ERROR_Value_1 | Frame-length too long error in frame at top of RX FIFO.
2	ABORT_DETECT	R	0h	1 | ABORT_DETECT_Value_1 | Abort pattern detected in frame at top of RX FIFO
1	CRC_ERROR	R	0h	1 | CRC_ERROR_Value_1 | CRC error in frame at top of RX FIFO. top of RX FIFO = Next frame to be read from RX FIFO
0	RESERVED0	R	0h	

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4.34.30 MSS_UARTn_TXFLL Registers

4.34.30.1 UARTn_TXFLL Register (Offset = 28h) [reset = 0h]

Short Description: Transmit frame length register low

Long Description: IrDA modes only. The UART_TXFLL and UART_TXFLH registers hold the 13-bit transmit frame length (expressed in bytes). UART_TXFLL holds the LSBs and UART_TXFLH holds the MSBs. The frame length value is used if the frame length method of frame closing is used.

Return to Summary Table

Table 4-2558. Instance Table

Instance Name	Physical Address
UART0	5230 0028h
UART1	5230 1028h
UART2	5230 2028h
UART3	5230 3028h
UART4	5230 4028h
UART5	5230 5028h

Figure 4-888. UART_TXFLL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								TXFLL							
R								W							
0								0							

Access Types Legend

Table 4-2559. TXFLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 0	TXFLL	W	0h	LSB register used to specify the frame length

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4.34.31 MSS_UARTn_RESUME Registers

4.34.31.1 UARTn_RESUME Register (Offset = 2Ch) [reset = 0h]

Short Description: Resume halted operation register

Long Description: IR-IrDA and IR-CIR modes only. This register is used to clear internal flags, which halt transmission/reception when an underrun/overrun error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.

Return to Summary Table

Table 4-2560. Instance Table

Instance Name	Physical Address
UART0	5230 002Ch
UART1	5230 102Ch
UART2	5230 202Ch
UART3	5230 302Ch
UART4	5230 402Ch
UART5	5230 502Ch

Figure 4-889. UART_RESUME Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESUME							
R								R							
0								0							

Access Types Legend

Table 4-2561. RESUME Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 0	RESUME	R	0h	Dummy read to restart the TX or RX

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4.34.32 MSS_UARTn_TXFLH Registers

4.34.32.1 UARTn_TXFLH Register (Offset = 2Ch) [reset = 0h]

Short Description: Transmit frame length register high

Long Description: IrDA modes only. The UART_TXFLL and UART_TXFLH registers hold the 13-bit transmit frame length (expressed in bytes). UART_TXFLL holds the LSBs and UART_TXFLH holds the MSBs. The frame length value is used if the frame length method of frame closing is used.

Return to Summary Table

Table 4-2562. Instance Table

Instance Name	Physical Address
UART0	5230 002Ch
UART1	5230 102Ch
UART2	5230 202Ch
UART3	5230 302Ch
UART4	5230 402Ch
UART5	5230 502Ch

Figure 4-890. UART_TXFLH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED			TXFLH				
R								R			W				
0								0			0				

Access Types Legend

Table 4-2563. TXFLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 5	RESERVED	R		
4 - 0	TXFLH	W	0h	MSB register used to specify the frame length

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4.34.33 MSS_UARTn_RXFLL Registers

4.34.33.1 UARTn_RXFLL Register (Offset = 30h) [reset = 0h]

Short Description: Received frame length register low

Long Description: IrDA modes only. The UART_RXFLL and UART_RXFLH registers hold the 12-bit receive maximum frame length. UART_RXFLL holds the LSBs and UART_RXFLH holds the MSBs. If the intended maximum receive frame length is n bytes, program the UART_RXFLL and UART_RXFLH registers to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are the result of frame format with CRC and stop flag; 2 bytes are associated with the FIR stop flag). T

Return to Summary Table

Table 4-2564. Instance Table

Instance Name	Physical Address
UART0	5230 0030h
UART1	5230 1030h
UART2	5230 2030h
UART3	5230 3030h
UART4	5230 4030h
UART5	5230 5030h

Figure 4-891. UART_RXFLL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RXFLL							
R								W							
0								0							

Access Types Legend

Table 4-2565. RXFLL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 0	RXFLL	W	0h	LSB register used to specify the frame length in reception

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4.34.34 MSS_UARTn_SFREGL Registers

4.34.34.1 UARTn_SFREGL Register (Offset = 30h) [reset = 0h]

Short Description: Status FIFO register high

Long Description: IrDA modes only. The frame lengths of received frames are written into the status FIFO. This information can be read by reading the UART_SFREGL and UART_SFREGH registers (these registers do not physically exist). The LSBs are read from UART_SFREGL and the MSBs are read from UART_SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the UART_SFLSR register.

Return to Summary Table

Table 4-2566. Instance Table

Instance Name	Physical Address
UART0	5230 0030h
UART1	5230 1030h
UART2	5230 2030h
UART3	5230 3030h
UART4	5230 4030h
UART5	5230 5030h

Figure 4-892. UART_SFREGL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								SFREGL							
R								R							
0								0							

Access Types Legend

Table 4-2567. SFREGL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 0	SFREGL	R	0h	LSB part of the frame length

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4.34.35 MSS_UARTn_RXFLH Registers

4.34.35.1 UARTn_RXFLH Register (Offset = 34h) [reset = 0h]

Short Description: Received frame length register high

Long Description: IrDA modes only. The UART_RXFLL and UART_RXFLH registers hold the 12-bit receive maximum frame length. UART_RXFLL holds the LSBs and UART_RXFLH holds the MSBs. If the intended maximum receive frame length is n bytes, program the UART_RXFLL and UART_RXFLH to be n + 3 in SIR or MIR modes and n + 6 in FIR mode (+3 and +6 are the result of frame format with CRC and stop flag; 2 bytes are associated with the FIR stop flag).

Return to Summary Table

Table 4-2568. Instance Table

Instance Name	Physical Address
UART0	5230 0034h
UART1	5230 1034h
UART2	5230 2034h
UART3	5230 3034h
UART4	5230 4034h
UART5	5230 5034h

Figure 4-893. UART_RXFLH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED				RXFLH			
R								R				W			
0								0				0			

Access Types Legend

Table 4-2569. RXFLH Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 4	RESERVED	R		
3 - 0	RXFLH	W	0h	MSB register used to specify the frame length in reception

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4.34.36 MSS_UARTn_SFREGH Registers

4.34.36.1 UARTn_SFREGH Register (Offset = 34h) [reset = 0h]

Short Description: Status FIFO register high

Long Description: IrDA modes only. The frame lengths of received frames are written into the status FIFO. This information can be read by reading the UART_SFREGL and UART_SFREGH registers (these registers do not physically exist). The LSBs are read from UART_SFREGL and the MSBs are read from UART_SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the UART_SFLSR register

Return to Summary Table

Table 4-2570. Instance Table

Instance Name	Physical Address
UART0	5230 0034h
UART1	5230 1034h
UART2	5230 2034h
UART3	5230 3034h
UART4	5230 4034h
UART5	5230 5034h

Figure 4-894. UART_SFREGH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED				SFREGH			
R								R				R			
0								0				0			

Access Types Legend

Table 4-2571. SFREGH Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 4	RESERVED	R		
3 - 0	SFREGH	R	0h	MSB part of the frame length

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4.34.37 MSS_UARTn_BLR Registers

4.34.37.1 UARTn_BLR Register (Offset = 38h) [reset = 40h]

Short Description: BOF control register

Long Description: IrDA modes only. The UART_BLR[6] bit selects whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR mode. If only one start flag is required, this is always 0xC0. If n start flags are required, (-1) 0xC0 or (-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).

Return to Summary Table

Table 4-2572. Instance Table

Instance Name	Physical Address
UART0	5230 0038h
UART1	5230 1038h
UART2	5230 2038h
UART3	5230 3038h
UART4	5230 4038h
UART5	5230 5038h

Figure 4-895. UART_BLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								STS_FIFO_RESET	XBOF_TYPE	RESERVED					
R								R/W1TS	R/W	R					
0								0	1	0					

Access Types Legend

Table 4-2573. BLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7	STS_FIFO_RESET	R/W1TS	0h	Status FIFO reset. This bit is self-clearing
6	XBOF_TYPE	R/W	1h	SIR xBOF select. 1 | XBOF_TYPE_Value_1 | 0xC0
5 - 0	RESERVED	R		

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4.34.38 MSS_UARTn_UASR Registers

4.34.38.1 UARTn_UASR Register (Offset = 38h) [reset = 0h]

Short Description: UART autobauding status register

Long Description: UART autobauding mode only. This status register returns the speed, the number of bits by characters, and the type of the parity in UART autobauding mode. In autobauding mode, the input frequency of the UART modem must be fixed to 48 MHz. Any other module clock frequency results in incorrect baud rate recognition. Note: When the UART is in autobauding mode, this register, instead of the UART_LCR, UART_DLL, and UART_DLH registers, is used to set up transmission according to the characteristics of the previous reception. To reset the autobauding hardware (to start a new AT detection), set UART_MDR1[2:0] to 111 (reset value), then set UART_MDR1[2:1] to 010 (UART in autobaud mode). To set the UART to standard mode (no autobaud), set UART_MDR1[2:1] to 000.

Return to Summary Table

Table 4-2574. Instance Table

Instance Name	Physical Address
UART0	5230 0038h
UART1	5230 1038h
UART2	5230 2038h
UART3	5230 3038h
UART4	5230 4038h
UART5	5230 5038h

Figure 4-896. UART_UASR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PARITY_TYPE		BIT_BY_CHAR	SPEED				
NONE								R		R	R				
0								0		0	0				

Access Types Legend

Table 4-2575. UASR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 6	PARITY_TYPE	R	0h	00 => No Parity identified. 01 => Parity space. 10 => Even Parity. 11 => Odd Parity
5	BIT_BY_CHAR	R	0h	0 => 7 bits character identified. 1 => 8 bits character identified
4 - 0	SPEED	R	0h	Used to report the speed identified. 00000 => No speed identified. 00001 => 115200 bauds. 00010 => 57600 bauds. 00011 => 38400 bauds. 00100 => 28800 bauds. 00101 => 19200 bauds. 00110 => 14400 bauds. 00111 => 9600 bauds. 01000 => 4800 bauds. 01001 => 2400 bauds. 01010 => 1200 bauds

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4.34.39 MSS_UARTn_ACREG Registers

4.34.39.1 UARTn_ACREG Register (Offset = 3Ch) [reset = 0h]

Short Description: Auxiliary control register

Long Description: IR-IrDA and IR-CIR modes only

Return to Summary Table

Table 4-2576. Instance Table

Instance Name	Physical Address
UART0	5230 003Ch
UART1	5230 103Ch
UART2	5230 203Ch
UART3	5230 303Ch
UART4	5230 403Ch
UART5	5230 503Ch

Figure 4-897. UART_ACREG Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								PULSE_TYPE	SD_MOD	DIS_IR_RX	DIS_TX_UNDERRUN	SEND_SIP	SCTX_EN	ABORT_EN	EOT_EN
R								R/W	R/W	R/W	R/W	R/W1TS	R/W1TS	R/W	R/W1TS
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2577. ACREG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7	PULSE_TYPE	R/W	0h	SIR pulse width select: 1 | PULSE_TYPE_Value_1 | 1.6us
6	SD_MOD	R/W	0h	Primary output used to configure transceivers. Connected to the SD/MODE input pin of IrDA transceivers. 1 | SD_MOD_Value_1 | SD pin is set to low
5	DIS_IR_RX	R/W	0h	1 | DIS_IR_RX_Value_1 | Disables RX input (permanent state - independent of transmit).
4	DIS_TX_UNDERRUN	R/W	0h	It is recommended to disable TX FIFO underrun capability by masking corresponding underrun interrupt. When disabling underrun by setting ACREG[4]=1, garbage data is sent over TX line. 1 | DIS_TX_UNDERRUN_Value_1 | Long stop bits can be transmitted, TX underrun is disabled
3	SEND_SIP	R/W1TS	0h	MIR/FIR Modes only.Send Serial Infrared Interaction Pulse [SIP] If this bit is set during a MIR/FIR transmission, the SIP will be send at the end of it.This bit automatically gets cleared at the end of the SIP transmission. 1 | SEND_SIP_Value_1 | Send SIP pulse.
2	SCTX_EN	R/W1TS	0h	Store and controlled TX start. When MDR1[5] = 1 and the LH writes 1 to this bit the TX state machine starts frame transmission. This bit is self-clearing.

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Table 4-2577. ACREG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ABORT_EN	R/W	0h	Frame Abort. The LH can intentionally abort transmission of a frame by writing 1 to this bit. Neither the end flag nor the CRC bits are appended to the frame. If transmit FIFO is not empty and MDR1[5]=1, UART IrDA will start a new transfer with data of previous frame as soon as abort frame has been sent. Therefore, TX FIFO must be reset before sending an abort frame.
0	EOT_EN	R/W1TS	0h	EOT [end of transmission] bit. The LH writes 1 to this bit just before it writes the last byte to the TX FIFO in set-EOT bit frame closing method. This bit automatically gets cleared when the LH writes to the THR [TX FIFO].

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4.34.40 MSS_UARTn_SCR Registers

4.34.40.1 UARTn_SCR Register (Offset = 40h) [reset = 0h]

Short Description: Supplementary control register

Long Description: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the UART_IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the UART_IIR register, the UART_SSR[1] bit must be checked. To clear the wake-up interrupt, bit UART_SCR[4] must be reset to 0.

Return to Summary Table

Table 4-2578. Instance Table

Instance Name	Physical Address
UART0	5230 0040h
UART1	5230 1040h
UART2	5230 2040h
UART3	5230 3040h
UART4	5230 4040h
UART5	5230 5040h

Figure 4-898. UART_SCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RX_TRIG_GRANU1	TX_TRIG_GRANU1	DSR_IT	RX_CTS_DSR_WAKE_UP_ENABLE	TX_EMPTY_CTL_IT	DMA_MODE_2		DMA_MODE_CTL
R								R/W	R/W	R/W	R/W	R/W	R/W		R/W
0								0	0	0	0	0	0		0

Access Types Legend

Table 4-2579. SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7	RX_TRIG_GRANU1	R/W	0h	1 | RX_TRIG_GRANU1_Value_1 | ENABLES THE GRANULARITY OF 1 FOR TRIGGER RX LEVEL.
6	TX_TRIG_GRANU1	R/W	0h	1 | TX_TRIG_GRANU1_Value_1 | Enables the granularity of 1 for trigger TX level.
5	DSR_IT	R/W	0h	1 | DSR_IT_Value_1 | ENABLES DSR* INTERRUPT.
4	RX_CTS_DSR_WAKE_UP_ENABLE	R/W	0h	1 | RX_CTS_DSR_WAKE_UP_ENABLE_Value_1 | Waits for a falling edge of pins RX, CTS* or DSR* to generate an interrupt
3	TX_EMPTY_CTL_IT	R/W	0h	1 | TX_EMPTY_CTL_IT_Value_1 | THE THR INTERRUPT IS GENERATED WHEN TX FIFO AND TX SHIFT REGISTER ARE EMPTY.
2 - 1	DMA_MODE_2	R/W	0h	Used to specify the DMA mode valid if SCR[0] = 1 3 | DMA_MODE_2_Value_3 | DMA mode 3 (UART_nDMA_REQ[0] in TX) 2 | DMA_MODE_2_Value_2 | DMA mode 2 (UART_nDMA_REQ[0] in RX) 1 | DMA_MODE_2_Value_1 | DMA mode 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX)

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Table 4-2579. SCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DMA_MODE_CTL	R/W	0h	1 | DMA_MODE_CTL_Value_1 | The DMA_MODE is set with SCR[2:1]

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4.34.41 MSS_UARTn_SSR Registers

4.34.41.1 UARTn_SSR Register (Offset = 44h) [reset = 4h]

Short Description: Supplementary status register

Long Description: Bit 1 is reset only when UART_SCR[4] is reset to 0.

Return to Summary Table

Table 4-2580. Instance Table

Instance Name	Physical Address
UART0	5230 0044h
UART1	5230 1044h
UART2	5230 2044h
UART3	5230 3044h
UART4	5230 4044h
UART5	5230 5044h

Figure 4-899. UART_SSR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED					DMA_COUNTER_RST	RX_CTS_DSR_WAKE_UP_STS	TX_FIFO_FULL
R								R					R/W	R	R
0								0					1	0	0

Access Types Legend

Table 4-2581. SSR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 3	RESERVED	R		
2	DMA_COUNTER_RST	R/W	1h	1 | DMA_COUNTER_RST_Value_1 | The DMA counter will be reset if corresponding FIFO is reset (via FCR[1] or FCR[2])
1	RX_CTS_DSR_WAKE_UP_STS	R	0h	1 | RX_CTS_DSR_WAKE_UP_STS_Value_1 | A falling edge occurred on RX, CTS* or DSR*
0	TX_FIFO_FULL	R	0h	1 | TX_FIFO_FULL_Value_1 | TX FIFO is full.

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4.34.42 MSS_UARTn_EBLR Registers

4.34.42.1 UARTn_EBLR Register (Offset = 48h) [reset = 0h]

Short Description: BOF length register

Long Description: IR-IrDA and IR-CIR modes only. In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must account for the BOF character; therefore, to send only one BOF with no XBOF, this register must be set to 1. To send one BOF with N XBOF, this register must be set to N + 1. The value 0 sends 1 BOF plus 255 XBOF. In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags). In IR-CIR mode, this register specifies the number of consecutive 0s to be received before generating the RX_STOP interrupt (UART_IIR[2]). All received 0s are stored in the RX FIFO. When the register is set to 0, this feature is deactivated and always in reception state, which can be disabled by setting the UART_ACREG[5] to 1.

Note

If the RX_STOP interrupt occurs before a byte boundary, the remaining bits of the last byte are filled with 0s and passed into the RX FIFO.

Return to Summary Table

Table 4-2582. Instance Table

Instance Name	Physical Address
UART0	5230 0048h
UART1	5230 1048h
UART2	5230 2048h
UART3	5230 3048h
UART4	5230 4048h
UART5	5230 5048h

Figure 4-900. UART_EBLR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								EBLR							
R								R/W							
0								0							

Access Types Legend

Table 4-2583. EBLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 0	EBLR	R/W	0h	IR-IRDA mode: This register allows to define up to 176 xBOFs, the maximum required by IrDA specification. IR-CIR mode: This register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt [IIR[2]]. 0x00: feature disabled. 0x01: generate RX_STOP interrupt after receiving one zero bit. ... 0xFF: generate RX_STOP interrupt after receiving 255 zero bits.

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4.34.43 MSS_UARTn_MVR Registers

4.34.43.1 UARTn_MVR Register (Offset = 50h) [reset = 47424603h]

Short Description: Module version register

Long Description: The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returned.

Return to Summary Table

Table 4-2584. Instance Table

Instance Name	Physical Address
UART0	5230 0050h
UART1	5230 1050h
UART2	5230 2050h
UART3	5230 3050h
UART4	5230 4050h
UART5	5230 5050h

Figure 4-901. UART_MVR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		RESERVED		FUNC											
R		R		R											
1		0		11101000010											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R					R			R		R					
1000					110			0		11					

Access Types Legend

Table 4-2585. MVR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	R	1h	Scheme revision number of module
29 - 28	RESERVED	R		
27 - 16	FUNC	R	742h	Function revision number of module
15 - 11	RTL	R	3E8h	Rtl revision number of module
10 - 8	MAJOR	R	6Eh	Major revision number of the module.
7 - 6	CUSTOM	R	0h	Custom revision number of the module.
5 - 0	MINOR	R	Bh	Minor revision number of the module.

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4.34.44 MSS_UARTn_SYSC Registers

4.34.44.1 UARTn_SYSC Register (Offset = 54h) [reset = 0h]

Short Description: System configuration register

Long Description: The AUTOIDLE bit controls a power-saving technique to reduce the logic power consumption of the open-core protocol (OCP) interface. When the feature is enabled, the clock is gated off until an OCP command for this device is detected. When the software reset bit is set high, it causes a full device reset.

Return to Summary Table

Table 4-2586. Instance Table

Instance Name	Physical Address
UART0	5230 0054h
UART1	5230 1054h
UART2	5230 2054h
UART3	5230 3054h
UART4	5230 4054h
UART5	5230 5054h

Figure 4-902. UART_SYSC Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED			IDLEMODE		ENAWAKEUP	SOFTRESET	AUTOIDLE
R								R			R/W		R/W	W	R/W
0								0			0		0	0	0

Access Types Legend

Table 4-2587. SYSC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 5	RESERVED	R		
4 - 3	IDLEMODE	R/W	0h	POWER MANAGEMENT REQ/ACK CONTROL REF: OCP DESIGN GUIDELINES VERSION 1.1 3 | IDLEMODE_Value_3 | reserved 2 | IDLEMODE_Value_2 | Smart idle. Acknowledgement to an idle request is given based in the internal activity of the module. 1 | IDLEMODE_Value_1 | No-idle. An idle request is never acknowledged.
2	ENAWAKEUP	R/W	0h	WAKE UP FEATURE CONTROL 1 | ENAWAKEUP_Value_1 | Wake up capability is enabled
1	SOFTRESET	W	0h	Software reset. Set this bit to 1 to trigger a module reset. This bit is automatically reset by the hardware. During reads it always returns a 0. 1 | SOFTRESET_Value_1 | The module is reset
0	AUTOIDLE	R/W	0h	Internal OCP clock gating strategy 1 | AUTOIDLE_Value_1 | Automatic OCP clock gating strategy is applied, based on the OCP interface activity

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4.34.45 MSS_UARTn_SYSS Registers

4.34.45.1 UARTn_SYSS Register (Offset = 58h) [reset = 0h]

Short Description: System status register

Long Description: System status register

Return to Summary Table

Table 4-2588. Instance Table

Instance Name	Physical Address
UART0	5230 0058h
UART1	5230 1058h
UART2	5230 2058h
UART3	5230 3058h
UART4	5230 4058h
UART5	5230 5058h

Figure 4-903. UART_SYSS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								RESERVED							RESETDONE
R								R							R
0								0							0

Access Types Legend

Table 4-2589. SYSS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 1	RESERVED	R		
0	RESETDONE	R	0h	Internal Reset Monitoring 1 | RESETDONE_Value_1 | Reset completed

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4.34.46 MSS_UARTn_WER Registers

4.34.46.1 UARTn_WER Register (Offset = 5Ch) [reset = ffh]

Short Description: Wake-up enable register

Long Description: The UART wake-up enable register is used to mask and unmask a UART event that would subsequently notify the system. An event is any activity in the logic that could cause an interrupt and/or an activity that would require the system to wake up. Even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, the UART registers the interrupt.

Return to Summary Table

Table 4-2590. Instance Table

Instance Name	Physical Address
UART0	5230 005Ch
UART1	5230 105Ch
UART2	5230 205Ch
UART3	5230 305Ch
UART4	5230 405Ch
UART5	5230 505Ch

Figure 4-904. UART_WER Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								EVENT_7_TX_WAKEUP_EN	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	EVENT_5_RHR_INTERRUPT	EVENT_4_RX_ACTIVITY	EVENT_3_DCD_CD_ACTIVITY	EVENT_2_RI_ACTIVITY	EVENT_1_DSR_ACTIVITY	EVENT_0_CTS_ACTIVITY
R								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0								1	1	1	1	1	1	1	1

Access Types Legend

Table 4-2591. WER Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7	EVENT_7_TX_WAKEUP_EN	R/W	1h	1 | Event_7_TX_WAKEUP_EN_Value_1 | EVENT CAN WAKE UP THE SYSTEM: Event can be: THR_IT or TX_DMA request and/or TX_SATUS_IT
6	EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT	R/W	1h	1 | Event_6_Receiver_Line_Status_Interrupt_Value_1 | Event can wake up the system
5	EVENT_5_RHR_INTERRUPT	R/W	1h	1 | Event_5_RHR_Interrupt_Value_1 | Event can wake up the system
4	EVENT_4_RX_ACTIVITY	R/W	1h	1 | Event_4_RX_Activity_Value_1 | Event can wake up the system
3	EVENT_3_DCD_CD_ACTIVITY	R/W	1h	1 | Event_3_DCD_CD_Activity_Value_1 | Event can wake up the system
2	EVENT_2_RI_ACTIVITY	R/W	1h	1 | Event_2_RI_Activity_Value_1 | Event can wake up the system

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Table 4-2591. WER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	EVENT_1_DSR_ACTIVITY	R/W	1h	1 | Event_1_DSR_Activity_Value_1 | Event can wake up the system
0	EVENT_0_CTS_ACTIVITY	R/W	1h	1 | Event_0_CTS_activity_Value_1 | Event can wake up the system

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4.34.47 MSS_UARTn_CFPS Registers

4.34.47.1 UARTn_CFPS Register (Offset = 60h) [reset = 69h]

Short Description: Carrier frequency prescaler

Long Description: Because the consumer IR works at modulation rates of 30 to 56.8 kHz, the 48-MHz clock must be prescaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote-control requirements in baud multiples of 12x. The value of the CFPS at reset is 0105 decimal, which equals 38.1 kHz output from starting conditions. The 48-MHz carrier is prescaled by the CFPS, which is then divided by the 12x baud multiple.

Return to Summary Table

Table 4-2592. Instance Table

Instance Name	Physical Address
UART0	5230 0060h
UART1	5230 1060h
UART2	5230 2060h
UART3	5230 3060h
UART4	5230 4060h
UART5	5230 5060h

Figure 4-905. UART_CFPS Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED_24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED_24								CFPS							
R								R/W							
0								1101001							

Access Types Legend

Table 4-2593. CFPS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED_24	R	0h	
7 - 0	CFPS	R/W	10CCC9h	System clock frequency prescaler at [12x multiple]. Examples for CFPS values are given in the table below. Target Freq [KHz] CFPS [decimal] Actual Freq[KHz] 30 133 30.08 32.75 122 32.79 36 111 36.04 36.7 109 36.69 38* 105 38.1 40 100 40 56.8 70 57.14 * configured at reset to this value Note: CFPS = 0 is not supported.

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4.34.48 MSS_UARTn_RXFIFO_LVL Registers

4.34.48.1 UARTn_RXFIFO_LVL Register (Offset = 64h) [reset = 0h]

Short Description: RX FIFO level register

Long Description: RX FIFO level register

Return to Summary Table

Table 4-2594. Instance Table

Instance Name	Physical Address
UART0	5230 0064h
UART1	5230 1064h
UART2	5230 2064h
UART3	5230 3064h
UART4	5230 4064h
UART5	5230 5064h

Figure 4-906. UART_RXFIFO_LVL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED24								RXFIFO_LVL							
R								R							
0								0							

Access Types Legend

Table 4-2595. RXFIFO_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED24	R	0h	
7 - 0	RXFIFO_LVL	R	0h	

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4.34.49 MSS_UARTn_TXFIFO_LVL Registers

4.34.49.1 UARTn_TXFIFO_LVL Register (Offset = 68h) [reset = 0h]

Short Description: TX FIFO level register

Long Description: Level of the TX FIFO

Return to Summary Table

Table 4-2596. Instance Table

Instance Name	Physical Address
UART0	5230 0068h
UART1	5230 1068h
UART2	5230 2068h
UART3	5230 3068h
UART4	5230 4068h
UART5	5230 5068h

Figure 4-907. UART_TXFIFO_LVL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED24															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED24								TXFIFO_LVL							
R								R							
0								0							

Access Types Legend

Table 4-2597. TXFIFO_LVL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED24	R	0h	
7 - 0	TXFIFO_LVL	R	0h	

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4.34.50 MSS_UARTn_IER2 Registers

4.34.50.1 UARTn_IER2 Register (Offset = 6Ch) [reset = 0h]

Short Description: Interrupt enable register 2

Long Description: Enables RX/TX FIFOs empty corresponding interrupts

Return to Summary Table

Table 4-2598. Instance Table

Instance Name	Physical Address
UART0	5230 006Ch
UART1	5230 106Ch
UART2	5230 206Ch
UART3	5230 306Ch
UART4	5230 406Ch
UART5	5230 506Ch

Figure 4-908. UART_IER2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								RESERVED					RHR_IT_DIS	EN_TXFIFO_EMPTY	EN_RXFIFO_EMPTY
R								R					R/W	R/W	R/W
0								0					0	0	0

Access Types Legend

Table 4-2599. IER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED1	R	0h	
7 - 3	RESERVED	R		
2	RHR_IT_DIS	R/W	0h	1 | RHR_IT_DIS_Value_1 | Disables the RHR interrupt.
1	EN_TXFIFO_EMPTY	R/W	0h	Enables[1]/DISABLES[00 EN_TXFIFO_EMPTY interrupt.
0	EN_RXFIFO_EMPTY	R/W	0h	Enables[1]/disables[0] EN_RXFIFO_EMPTY interrupt.

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4.34.51 MSS_UARTn_ISR2 Registers

4.34.51.1 UARTn_ISR2 Register (Offset = 70h) [reset = 3h]

Short Description: Interrupt status register 2

Long Description: Status of RX/TX FIFOs empty corresponding interrupts

Return to Summary Table

Table 4-2600. Instance Table

Instance Name	Physical Address
UART0	5230 0070h
UART1	5230 1070h
UART2	5230 2070h
UART3	5230 3070h
UART4	5230 4070h
UART5	5230 5070h

Figure 4-909. UART_ISR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								RESERVED						TXFIFO_EMPTY_STS	RXFIFO_EMPTY_STS
R								R						R/W1TC	R/W1TC
0								0						1	1

Access Types Legend

Table 4-2601. ISR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED1	R	0h	
7 - 2	RESERVED	R		
1	TXFIFO_EMPTY_STS	R/W1TC	1h	TXFIFO interrupt pending 1 | TXFIFO_EMPTY_STS_Value_1 | TXFIFO_EMPTY interrupt pending.
0	RXFIFO_EMPTY_STS	R/W1TC	1h	RXFIFO interrupt pending 1 | RXFIFO_EMPTY_STS_Value_1 | RXFIFO_EMPTY interrupt pending.

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4.34.52 MSS_UARTn_FREQ_SEL Registers

4.34.52.1 UARTn_FREQ_SEL Register (Offset = 74h) [reset = 1ah]

Short Description: Sample per bit selector register

Long Description: Sample per bit selector

Return to Summary Table

Table 4-2602. Instance Table

Instance Name	Physical Address
UART0	5230 0074h
UART1	5230 1074h
UART2	5230 2074h
UART3	5230 3074h
UART4	5230 4074h
UART5	5230 5074h

Figure 4-910. UART_FREQ_SEL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED2								FREQ_SEL							
R								R/W							
0								11010							

Access Types Legend

Table 4-2603. FREQ_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED2	R	0h	RESERVED
7 - 0	FREQ_SEL	R/W	2B02h	Sets the sample per bit if non default frequency is used. MDR3[1] must be set to 1 after this value is set. Must be equal or higher then 6.

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4.34.53 MSS_UARTn_ABAUD_1ST_CHAR Registers

4.34.53.1 UARTn_ABAUD_1ST_CHAR Register (Offset = 78h) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-2604. Instance Table

Instance Name	Physical Address
UART0	5230 0078h
UART1	5230 1078h
UART2	5230 2078h
UART3	5230 3078h
UART4	5230 4078h
UART5	5230 5078h

Figure 4-911. UART_ABAUD_1ST_CHAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R															
0															

Access Types Legend

Table 4-2605. ABAUD_1ST_CHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED	R		

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4.34.54 MSS_UARTn_BAUD_2ND_CHAR Registers

4.34.54.1 UARTn_BAUD_2ND_CHAR Register (Offset = 7Ch) [reset = 0h]

Short Description:

Long Description:

Return to Summary Table

Table 4-2606. Instance Table

Instance Name	Physical Address
UART0	5230 007Ch
UART1	5230 107Ch
UART2	5230 207Ch
UART3	5230 307Ch
UART4	5230 407Ch
UART5	5230 507Ch

Figure 4-912. UART_BAUD_2ND_CHAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R															
0															

Access Types Legend

Table 4-2607. BAUD_2ND_CHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	RESERVED	R		

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4.34.55 MSS_UARTn_MDR3 Registers

4.34.55.1 UARTn_MDR3 Register (Offset = 80h) [reset = 0h]

Short Description: Mode definition register 3

Long Description: Mode definition register 3

Return to Summary Table

Table 4-2608. Instance Table

Instance Name	Physical Address
UART0	5230 0080h
UART1	5230 1080h
UART2	5230 2080h
UART3	5230 3080h
UART4	5230 4080h
UART5	5230 5080h

Figure 4-913. UART_MDR3 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED2															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED2								RESERVED1			DIR_EN	DIR_POL	SET_DMA_TX_THRESHOLD	NONDEFAULT_FREQ	DISABLE_CIR_RX_DEMOD
R								R			R/W	R/W	R/W	R/W	R/W
0								0			0	0	0	0	0

Access Types Legend

Table 4-2609. MDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED2	R	0h	
7 - 5	RESERVED1	R	0h	Reserved
4	DIR_EN	R/W	0h	RS-485 External Transceiver Direction Enable
3	DIR_POL	R/W	0h	RS-485 External Transceiver Direction Polarity. 0 => TX: RTS=0, RX: RTS=1. 1 => TX: RTS=1, RX: RTS=0
2	SET_DMA_TX_THRESHOLD	R/W	0h	Enable to set different TX DMA threshold then 64-trigger [usage of new register TX_DNA_THRESHOLD]
1	NONDEFAULT_FREQ	R/W	0h	Enables[1]/Disables[0] using NONDEFAULT fclk frequencies
0	DISABLE_CIR_RX_DEMOD	R/W	0h	Disables[1]/Enables[0] CIR RX demodulation 1 | DISABLE_CIR_RX_DEMOD_Value_1 | Disables CIR RX demodulation

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4.34.56 MSS_UARTn_TX_DMA_THRESHOLD Registers

4.34.56.1 UARTn_TX_DMA_THRESHOLD Register (Offset = 84h) [reset = 0h]

Short Description: TX DMA threshold level register

Long Description: Use to manually set the TX DMA threshold level. UART_MDR3[2] SET_TX_DMA_THRESHOLD must be 1 and must be value + tx_trigger_level = 64 (TX FIFO size). If not, 64-tx_trigger_level will be used without modifying the value of this register.

Return to Summary Table

Table 4-2610. Instance Table

Instance Name	Physical Address
UART0	5230 0084h
UART1	5230 1084h
UART2	5230 2084h
UART3	5230 3084h
UART4	5230 4084h
UART5	5230 5084h

Figure 4-914. UART_TX_DMA_THRESHOLD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								RESERVED		TX_DMA_THRESHOLD					
R								R		R/W					
0								0		0					

Access Types Legend

Table 4-2611. TX_DMA_THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED1	R	0h	RESERVED
7 - 6	RESERVED	R		Reserved
5 - 0	TX_DMA_THRESHOLD	R/W	0h	Use to manually set the TX DMA threshold level.

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4.34.57 MSS_UARTn_MDR4 Registers

4.34.57.1 UARTn_MDR4 Register (Offset = 88h) [reset = 0h]

Short Description: Mode definition register 4

Long Description: Mode definition register 4

Return to Summary Table

Table 4-2612. Instance Table

Instance Name	Physical Address
UART0	5230 0088h
UART1	5230 1088h
UART2	5230 2088h
UART3	5230 3088h
UART4	5230 4088h
UART5	5230 5088h

Figure 4-915. UART_MDR4 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								RESERVED	MODE9	FREQ_SEL_H			MODE		
R								R	R/W	R/W			R/W		
0								0	0	0			0		

Access Types Legend

Table 4-2613. MDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED1	R	0h	
7	RESERVED	R		
6	MODE9	R/W	0h	9-bit character length. When '1', overrides character length setting in LCR
5 - 3	FREQ_SEL_H	R/W	0h	Upper 3 bits of FREQ_SEL register for higher division values, as required for example for FI/Di in ISO7816 mode
2 - 0	MODE	R/W	0h	New modes [when set, overrides MDR1 modes] 7 | Reserved2 | reserved 6 | Reserved1 | reserved 5 | ISO7816_1 | ISO 7816 mode T=1 4 | ISO7816_0 | ISO 7816 mode T=0 3 | Synch_gen | Synchronous mode with generated clock 2 | Synch_ext | Synchronous mode with external clock 1 | Reserved | reserved

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4.34.58 MSS_UARTn_EFR2 Registers

4.34.58.1 UARTn_EFR2 Register (Offset = 8Ch) [reset = 0h]

Short Description: Enhanced Features Register 2

Long Description: Enhanced Features Register 2

Return to Summary Table

Table 4-2614. Instance Table

Instance Name	Physical Address
UART0	5230 008Ch
UART1	5230 108Ch
UART2	5230 208Ch
UART3	5230 308Ch
UART4	5230 408Ch
UART5	5230 508Ch

Figure 4-916. UART_EFR2 Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								BROADCAST	TIMEOUT_BEHAVE	C8	C4	C2	MULTIDROP	RHR_OVERRUN	ENDIAN
R								R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0								0	0	0	0	0	0	0	0

Access Types Legend

Table 4-2615. EFR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED1	R	0h	
7	BROADCAST	R/W	0h	Enables broadcast address matching in multi-drop address match mode
6	TIMEOUT_BEHAVE	R/W	0h	Specifies how timeout is measured 1 | _1 | periodic timeout even when no character has been received
5	C8	R/W	0h	Value for ISO 7816 C8 pin for software control
4	C4	R/W	0h	Value for ISO 7816 C4 pin for software control
3	C2	R/W	0h	Value for ISO 7816 reset pin [software controllable]
2	MULTIDROP	R/W	0h	Enables parity Multi-drop mode [overrides LCR[5..3]] when '1'
1	RHR_OVERRUN	R/W	0h	RHR Overrun behaviour when buffer full 1 | Atmel | data in RHR is overwritten when buffer full (and FIFO disabled)
0	ENDIAN	R/W	0h	Endianness 1 | Big_Endian | Big Endian (MSB First)

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4.34.59 MSS_UARTn_ECR Registers

4.34.59.1 UARTn_ECR Register (Offset = 90h) [reset = 18h]

Short Description: Enhanced Control register

Long Description: Enhanced Control register

Return to Summary Table

Table 4-2616. Instance Table

Instance Name	Physical Address
UART0	5230 0090h
UART1	5230 1090h
UART2	5230 2090h
UART3	5230 3090h
UART4	5230 4090h
UART5	5230 5090h

Figure 4-917. UART_ECR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								RESERVED		CLEAR_TX_PE	TX_EN	RX_EN	TX_RST	RX_RST	A_MULTIDROP
R								R		W	R/W	R/W	W	W	W
0								0		0	1	1	0	0	0

Access Types Legend

Table 4-2617. ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED1	R	0h	
7 - 6	RESERVED	R		
5	CLEAR_TX_PE	W	0h	Write 1 to clear parity error from the Transmitter to allow it to continue to try sending data [ISO7816 transmit only]
4	TX_EN	R/W	1h	Enables/Disables the transmitter 1 | Enabled | Transmitter is working
3	RX_EN	R/W	1h	Enables/Disables the receiver 1 | Enabled | Receiver is operating
2	TX_RST	W	0h	Writing '1' resets the transmitter
1	RX_RST	W	0h	Writing '1' resets the receiver
0	A_MULTIDROP	W	0h	In multi-drop mode, when written with the value '1' causes the next byte written into THR to be transmitted with the parity bit set, signaling an address

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4.34.60 MSS_UARTn_TIMEGUARD Registers

4.34.60.1 UARTn_TIMEGUARD Register (Offset = 94h) [reset = 0h]

Short Description: Timeguard register

Long Description: Timeguard

Return to Summary Table

Table 4-2618. Instance Table

Instance Name	Physical Address
UART0	5230 0094h
UART1	5230 1094h
UART2	5230 2094h
UART3	5230 3094h
UART4	5230 4094h
UART5	5230 5094h

Figure 4-918. UART_TIMEGUARD Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TIMEGUARD							
R								R/W							
0								0							

Access Types Legend

Table 4-2619. TIMEGUARD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED	R		
7 - 0	TIMEGUARD	R/W	0h	Specifies the amount of idle baud clocks [transmitter bit period] to insert between transmitted bytes, useful when comunicating with slower devices

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4.34.61 MSS_UARTn_TIMEOUTL Registers

4.34.61.1 UARTn_TIMEOUTL Register (Offset = 98h) [reset = 0h]

Short Description: Timeout lower byte register

Long Description: Timeout lower byte register

Return to Summary Table

Table 4-2620. Instance Table

Instance Name	Physical Address
UART0	5230 0098h
UART1	5230 1098h
UART2	5230 2098h
UART3	5230 3098h
UART4	5230 4098h
UART5	5230 5098h

Figure 4-919. UART_TIMEOUTL Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TIMEOUT_L							
R								R/W							
0								0							

Access Types Legend

Table 4-2621. TIMEOUTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED	R		
7 - 0	TIMEOUT_L	R/W	0h	Custom timeout period in baud clocks, to override the internal value, when different from 0. [Lower byte of the 16 bit value]

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4.34.62 MSS_UARTn_TIMEOUTH Registers

4.34.62.1 UARTn_TIMEOUTH Register (Offset = 9Ch) [reset = 0h]

Short Description: Timeout higher byte register

Long Description: Timeout higher byte register

Return to Summary Table

Table 4-2622. Instance Table

Instance Name	Physical Address
UART0	5230 009Ch
UART1	5230 109Ch
UART2	5230 209Ch
UART3	5230 309Ch
UART4	5230 409Ch
UART5	5230 509Ch

Figure 4-920. UART_TIMEOUTH Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TIMEOUT_H							
R								R/W							
0								0							

Access Types Legend

Table 4-2623. TIMEOUTH Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED	R		
7 - 0	TIMEOUT_H	R/W	0h	Custom timeout period in baud clocks, to override the internal value, when different from 0. [Higher byte of the 16 bit value]

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4.34.63 MSS_UARTn_SCCR Registers

4.34.63.1 UARTn_SCCR Register (Offset = A0h) [reset = 7h]

Short Description: Smartcard mode control register

Long Description: Smartcard (ISO7816) mode Control Register

Return to Summary Table

Table 4-2624. Instance Table

Instance Name	Physical Address
UART0	5230 00A0h
UART1	5230 10A0h
UART2	5230 20A0h
UART3	5230 30A0h
UART4	5230 40A0h
UART5	5230 50A0h

Figure 4-921. UART_SCCR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED1															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED1								DSNACK	INACK	RESERVED			MAX_ITERATION		
R								R/W	R/W	R			R/W		
0								0	0	0			111		

Access Types Legend

Table 4-2625. SCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RESERVED1	R	0h	
7	DSNACK	R/W	0h	Applies Max_Iteration to receiver aswell - when maximum number of NACKs have been returned, the receiver will accept the data regardless of error. The data will be loaded into the receiver FIFO and PE will be set when reading it.
6	INACK	R/W	0h	Inhibit NACK when receiving, even if an error is received. The data will be loaded into the receiver FIFO and PE will be set when reading it.
5 - 3	RESERVED	R		
2 - 0	MAX_ITERATION	R/W	6Fh	Number of times to repeat transmitted character, if the receiver did not acknowledge. If not acknowledged after the max value is reached, the USART transmitter will set parity error, stop and not continue until it is cleared.

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4.34.64 MSS_UARTn_ERHR Registers

4.34.64.1 UARTn_ERHR Register (Offset = A4h) [reset = 0h]

Short Description: Extended receive holding register

Long Description: Extended receive holding register

Return to Summary Table

Table 4-2626. Instance Table

Instance Name	Physical Address
UART0	5230 00A4h
UART1	5230 10A4h
UART2	5230 20A4h
UART3	5230 30A4h
UART4	5230 40A4h
UART5	5230 50A4h

Figure 4-922. UART_ERHR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							ERHR								
R							R								
0							0								

Access Types Legend

Table 4-2627. ERHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 9	RESERVED	R		
8 - 0	ERHR	R	0h	Extended Receive Holding Register - allows accessing the full 9bit RHR

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4.34.65 MSS_UARTn_ETHR Registers

4.34.65.1 UARTn_ETHR Register (Offset = A4h) [reset = 0h]

Short Description: Extended Transmit Holding Register

Long Description: Extended Transmit Holding Register

Return to Summary Table

Table 4-2628. Instance Table

Instance Name	Physical Address
UART0	5230 00A4h
UART1	5230 10A4h
UART2	5230 20A4h
UART3	5230 30A4h
UART4	5230 40A4h
UART5	5230 50A4h

Figure 4-923. UART_ETHR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							ETHR								
R							W								
0							0								

Access Types Legend

Table 4-2629. ETHR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 9	RESERVED	R		
8 - 0	ETHR	W	0h	Extended Transmit Holding Register - allows writing the full 9bit RHR

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4.34.66 MSS_UARTn_MAR Registers

4.34.66.1 UARTn_MAR Register (Offset = A8h) [reset = 0h]

Short Description: Multidrop Address Register

Long Description: Multidrop Address Register

Return to Summary Table

Table 4-2630. Instance Table

Instance Name	Physical Address
UART0	5230 00A8h
UART1	5230 10A8h
UART2	5230 20A8h
UART3	5230 30A8h
UART4	5230 40A8h
UART5	5230 50A8h

Figure 4-924. UART_MAR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ADDRESS							
NONE								R/W							
0								0							

Access Types Legend

Table 4-2631. MAR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	ADDRESS	R/W	0h	Multidrop match address value

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4.34.67 MSS_UARTn_MMR Registers

4.34.67.1 UARTn_MMR Register (Offset = ACh) [reset = 0h]

Short Description: Multidrop Mask Register

Long Description: Multidrop Mask Register

Return to Summary Table

Table 4-2632. Instance Table

Instance Name	Physical Address
UART0	5230 00ACh
UART1	5230 10ACh
UART2	5230 20ACh
UART3	5230 30ACh
UART4	5230 40ACh
UART5	5230 50ACh

Figure 4-925. UART_MMR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MASK							
NONE								R/W							
0								0							

Access Types Legend

Table 4-2633. MMR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	MASK	R/W	0h	Address match masking value ? writing a 0 to a bit means that the corresponding address bit will be ignored in matching

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4.34.68 MSS_UARTn_MBR Registers

4.34.68.1 UARTn_MBR Register (Offset = B0h) [reset = 0h]

Short Description: Multidrop Broadcast Address Register

Long Description: Multidrop Broadcast Address Register

Return to Summary Table

Table 4-2634. Instance Table

Instance Name	Physical Address
UART0	5230 00B0h
UART1	5230 10B0h
UART2	5230 20B0h
UART3	5230 30B0h
UART4	5230 40B0h
UART5	5230 50B0h

Figure 4-926. UART_MBR Name Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
NONE															
0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BROADCAST_ADDRESS							
NONE								R/W							
0								0							

Access Types Legend

Table 4-2635. MBR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
7 - 0	BROADCAST_ADDRESS	R/W	0h	Broadcast address for address matching

4.34.69 Access Table

Table 4-2636. Access Type Codes

Access Type	Code	Description
R/W	R/W	Read / Write
R	R	Read
W	W	Write
R/W1TS	R/W1TS	Read/Write 1 To Set
R/W1TC	R/W1TC	Read/Write 1 To Clear

4.35 VIM Registers

Table 4-2637. MSS_VIM Registers Base Address Table

Offset	Length	Acronym	MSS_VIM Physical Address
0h	32	VIM_PID	50F0 0000h
4h	32	VIM_INFO	50F0 0004h
8h	32	VIM_PRIIRQ	50F0 0008h
Ch	32	VIM_PRIFIQ	50F0 000Ch

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Table 4-2637. MSS_VIM Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_VIM Physical Address
10h	32	VIM_IRQGSTS	50F0 0010h
14h	32	VIM_FIQGSTS	50F0 0014h
18h	32	VIM_IRQVEC	50F0 0018h
1Ch	32	VIM_FIQVEC	50F0 001Ch
20h	32	VIM_ACTIRQ	50F0 0020h
24h	32	VIM_ACTFIQ	50F0 0024h
28h	32	VIM_IRQPRIMSK	50F0 0028h
2Ch	32	VIM_FIQPRIMSK	50F0 002Ch
30h	32	VIM_DEDVEC	50F0 0030h
400h	32	VIM_RAW	50F0 0400h
404h	32	VIM_STS	50F0 0404h
408h	32	VIM_INTR_EN_SET	50F0 0408h
40Ch	32	VIM_INTER_EN_CLR	50F0 040Ch
410h	32	VIM_IRQSTS	50F0 0410h
414h	32	VIM_FIQSTS	50F0 0414h
418h	32	VIM_INTMAP	50F0 0418h
41Ch	32	VIM_INTTYPE	50F0 041Ch
420h	32	VIM_RAW_1	50F0 0420h
424h	32	VIM_STS_1	50F0 0424h
428h	32	VIM_INTR_EN_SET_1	50F0 0428h
42Ch	32	VIM_INTER_EN_CLR_1	50F0 042Ch
430h	32	VIM_IRQSTS_1	50F0 0430h
434h	32	VIM_FIQSTS_1	50F0 0434h
438h	32	VIM_INTMAP_1	50F0 0438h
43Ch	32	VIM_INTTYPE_1	50F0 043Ch
440h	32	VIM_RAW_2	50F0 0440h
444h	32	VIM_STS_2	50F0 0444h
448h	32	VIM_INTR_EN_SET_2	50F0 0448h
44Ch	32	VIM_INTER_EN_CLR_2	50F0 044Ch
450h	32	VIM_IRQSTS_2	50F0 0450h
454h	32	VIM_FIQSTS_2	50F0 0454h
458h	32	VIM_INTMAP_2	50F0 0458h
45Ch	32	VIM_INTTYPE_2	50F0 045Ch
460h	32	VIM_RAW_3	50F0 0460h
464h	32	VIM_STS_3	50F0 0464h
468h	32	VIM_INTR_EN_SET_3	50F0 0468h
46Ch	32	VIM_INTER_EN_CLR_3	50F0 046Ch
470h	32	VIM_IRQSTS_3	50F0 0470h
474h	32	VIM_FIQSTS_3	50F0 0474h
478h	32	VIM_INTMAP_3	50F0 0478h
47Ch	32	VIM_INTTYPE_3	50F0 047Ch
480h	32	VIM_RAW_4	50F0 0480h
484h	32	VIM_STS_4	50F0 0484h
488h	32	VIM_INTR_EN_SET_4	50F0 0488h
48Ch	32	VIM_INTER_EN_CLR_4	50F0 048Ch
490h	32	VIM_IRQSTS_4	50F0 0490h
494h	32	VIM_FIQSTS_4	50F0 0494h

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Table 4-2637. MSS_VIM Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_VIM Physical Address
498h	32	VIM_INTMAP_4	50F0 0498h
49Ch	32	VIM_INTTYPE_4	50F0 049Ch
4A0h	32	VIM_RAW_5	50F0 04A0h
4A4h	32	VIM_STS_5	50F0 04A4h
4A8h	32	VIM_INTR_EN_SET_5	50F0 04A8h
4ACh	32	VIM_INTER_EN_CLR_5	50F0 04ACh
4B0h	32	VIM_IRQSTS_5	50F0 04B0h
4B4h	32	VIM_FIQSTS_5	50F0 04B4h
4B8h	32	VIM_INTMAP_5	50F0 04B8h
4BCh	32	VIM_INTTYPE_5	50F0 04BCh
4C0h	32	VIM_RAW_6	50F0 04C0h
4C4h	32	VIM_STS_6	50F0 04C4h
4C8h	32	VIM_INTR_EN_SET_6	50F0 04C8h
4CCh	32	VIM_INTER_EN_CLR_6	50F0 04CCh
4D0h	32	VIM_IRQSTS_6	50F0 04D0h
4D4h	32	VIM_FIQSTS_6	50F0 04D4h
4D8h	32	VIM_INTMAP_6	50F0 04D8h
4DCh	32	VIM_INTTYPE_6	50F0 04DCh
4E0h	32	VIM_RAW_7	50F0 04E0h
4E4h	32	VIM_STS_7	50F0 04E4h
4E8h	32	VIM_INTR_EN_SET_7	50F0 04E8h
4ECh	32	VIM_INTER_EN_CLR_7	50F0 04ECh
4F0h	32	VIM_IRQSTS_7	50F0 04F0h
4F4h	32	VIM_FIQSTS_7	50F0 04F4h
4F8h	32	VIM_INTMAP_7	50F0 04F8h
4FCh	32	VIM_INTTYPE_7	50F0 04FCh
1000h	32	VIM_INTPRIORITY_0	50F0 1000h
1004h	32	VIM_INTPRIORITY_1	50F0 1004h
1008h	32	VIM_INTPRIORITY_2	50F0 1008h
100Ch	32	VIM_INTPRIORITY_3	50F0 100Ch
1010h	32	VIM_INTPRIORITY_4	50F0 1010h
1014h	32	VIM_INTPRIORITY_5	50F0 1014h
1018h	32	VIM_INTPRIORITY_6	50F0 1018h
101Ch	32	VIM_INTPRIORITY_7	50F0 101Ch
1020h	32	VIM_INTPRIORITY_8	50F0 1020h
1024h	32	VIM_INTPRIORITY_9	50F0 1024h
1028h	32	VIM_INTPRIORITY_10	50F0 1028h
102Ch	32	VIM_INTPRIORITY_11	50F0 102Ch
1030h	32	VIM_INTPRIORITY_12	50F0 1030h
1034h	32	VIM_INTPRIORITY_13	50F0 1034h
1038h	32	VIM_INTPRIORITY_14	50F0 1038h
103Ch	32	VIM_INTPRIORITY_15	50F0 103Ch
1040h	32	VIM_INTPRIORITY_16	50F0 1040h
1044h	32	VIM_INTPRIORITY_17	50F0 1044h
1048h	32	VIM_INTPRIORITY_18	50F0 1048h
104Ch	32	VIM_INTPRIORITY_19	50F0 104Ch
1050h	32	VIM_INTPRIORITY_20	50F0 1050h

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Table 4-2637. MSS_VIM Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_VIM Physical Address
1054h	32	VIM_INTPRIORITY_21	50F0 1054h
1058h	32	VIM_INTPRIORITY_22	50F0 1058h
105Ch	32	VIM_INTPRIORITY_23	50F0 105Ch
1060h	32	VIM_INTPRIORITY_24	50F0 1060h
1064h	32	VIM_INTPRIORITY_25	50F0 1064h
1068h	32	VIM_INTPRIORITY_26	50F0 1068h
106Ch	32	VIM_INTPRIORITY_27	50F0 106Ch
1070h	32	VIM_INTPRIORITY_28	50F0 1070h
1074h	32	VIM_INTPRIORITY_29	50F0 1074h
1078h	32	VIM_INTPRIORITY_30	50F0 1078h
107Ch	32	VIM_INTPRIORITY_31	50F0 107Ch
1080h	32	VIM_INTPRIORITY_32	50F0 1080h
1084h	32	VIM_INTPRIORITY_33	50F0 1084h
1088h	32	VIM_INTPRIORITY_34	50F0 1088h
108Ch	32	VIM_INTPRIORITY_35	50F0 108Ch
1090h	32	VIM_INTPRIORITY_36	50F0 1090h
1094h	32	VIM_INTPRIORITY_37	50F0 1094h
1098h	32	VIM_INTPRIORITY_38	50F0 1098h
109Ch	32	VIM_INTPRIORITY_39	50F0 109Ch
10A0h	32	VIM_INTPRIORITY_40	50F0 10A0h
10A4h	32	VIM_INTPRIORITY_41	50F0 10A4h
10A8h	32	VIM_INTPRIORITY_42	50F0 10A8h
10ACh	32	VIM_INTPRIORITY_43	50F0 10ACh
10B0h	32	VIM_INTPRIORITY_44	50F0 10B0h
10B4h	32	VIM_INTPRIORITY_45	50F0 10B4h
10B8h	32	VIM_INTPRIORITY_46	50F0 10B8h
10BCh	32	VIM_INTPRIORITY_47	50F0 10BCh
10C0h	32	VIM_INTPRIORITY_48	50F0 10C0h
10C4h	32	VIM_INTPRIORITY_49	50F0 10C4h
10C8h	32	VIM_INTPRIORITY_50	50F0 10C8h
10CCh	32	VIM_INTPRIORITY_51	50F0 10CCh
10D0h	32	VIM_INTPRIORITY_52	50F0 10D0h
10D4h	32	VIM_INTPRIORITY_53	50F0 10D4h
10D8h	32	VIM_INTPRIORITY_54	50F0 10D8h
10DCh	32	VIM_INTPRIORITY_55	50F0 10DCh
10E0h	32	VIM_INTPRIORITY_56	50F0 10E0h
10E4h	32	VIM_INTPRIORITY_57	50F0 10E4h
10E8h	32	VIM_INTPRIORITY_58	50F0 10E8h
10ECh	32	VIM_INTPRIORITY_59	50F0 10ECh
10F0h	32	VIM_INTPRIORITY_60	50F0 10F0h
10F4h	32	VIM_INTPRIORITY_61	50F0 10F4h
10F8h	32	VIM_INTPRIORITY_62	50F0 10F8h
10FCh	32	VIM_INTPRIORITY_63	50F0 10FCh
1100h	32	VIM_INTPRIORITY_64	50F0 1100h
1104h	32	VIM_INTPRIORITY_65	50F0 1104h
1108h	32	VIM_INTPRIORITY_66	50F0 1108h
110Ch	32	VIM_INTPRIORITY_67	50F0 110Ch

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Table 4-2637. MSS_VIM Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_VIM Physical Address
1110h	32	VIM_INTPRIORITY_68	50F0 1110h
1114h	32	VIM_INTPRIORITY_69	50F0 1114h
1118h	32	VIM_INTPRIORITY_70	50F0 1118h
111Ch	32	VIM_INTPRIORITY_71	50F0 111Ch
1120h	32	VIM_INTPRIORITY_72	50F0 1120h
1124h	32	VIM_INTPRIORITY_73	50F0 1124h
1128h	32	VIM_INTPRIORITY_74	50F0 1128h
112Ch	32	VIM_INTPRIORITY_75	50F0 112Ch
1130h	32	VIM_INTPRIORITY_76	50F0 1130h
1134h	32	VIM_INTPRIORITY_77	50F0 1134h
1138h	32	VIM_INTPRIORITY_78	50F0 1138h
113Ch	32	VIM_INTPRIORITY_79	50F0 113Ch
1140h	32	VIM_INTPRIORITY_80	50F0 1140h
1144h	32	VIM_INTPRIORITY_81	50F0 1144h
1148h	32	VIM_INTPRIORITY_82	50F0 1148h
114Ch	32	VIM_INTPRIORITY_83	50F0 114Ch
1150h	32	VIM_INTPRIORITY_84	50F0 1150h
1154h	32	VIM_INTPRIORITY_85	50F0 1154h
1158h	32	VIM_INTPRIORITY_86	50F0 1158h
115Ch	32	VIM_INTPRIORITY_87	50F0 115Ch
1160h	32	VIM_INTPRIORITY_88	50F0 1160h
1164h	32	VIM_INTPRIORITY_89	50F0 1164h
1168h	32	VIM_INTPRIORITY_90	50F0 1168h
116Ch	32	VIM_INTPRIORITY_91	50F0 116Ch
1170h	32	VIM_INTPRIORITY_92	50F0 1170h
1174h	32	VIM_INTPRIORITY_93	50F0 1174h
1178h	32	VIM_INTPRIORITY_94	50F0 1178h
117Ch	32	VIM_INTPRIORITY_95	50F0 117Ch
1180h	32	VIM_INTPRIORITY_96	50F0 1180h
1184h	32	VIM_INTPRIORITY_97	50F0 1184h
1188h	32	VIM_INTPRIORITY_98	50F0 1188h
118Ch	32	VIM_INTPRIORITY_99	50F0 118Ch
1190h	32	VIM_INTPRIORITY_100	50F0 1190h
1194h	32	VIM_INTPRIORITY_101	50F0 1194h
1198h	32	VIM_INTPRIORITY_102	50F0 1198h
119Ch	32	VIM_INTPRIORITY_103	50F0 119Ch
11A0h	32	VIM_INTPRIORITY_104	50F0 11A0h
11A4h	32	VIM_INTPRIORITY_105	50F0 11A4h
11A8h	32	VIM_INTPRIORITY_106	50F0 11A8h
11ACh	32	VIM_INTPRIORITY_107	50F0 11ACh
11B0h	32	VIM_INTPRIORITY_108	50F0 11B0h
11B4h	32	VIM_INTPRIORITY_109	50F0 11B4h
11B8h	32	VIM_INTPRIORITY_110	50F0 11B8h
11BCh	32	VIM_INTPRIORITY_111	50F0 11BCh
11C0h	32	VIM_INTPRIORITY_112	50F0 11C0h
11C4h	32	VIM_INTPRIORITY_113	50F0 11C4h
11C8h	32	VIM_INTPRIORITY_114	50F0 11C8h

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Table 4-2637. MSS_VIM Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_VIM Physical Address
11CCh	32	VIM_INTPRIORITY_115	50F0 11CCh
11D0h	32	VIM_INTPRIORITY_116	50F0 11D0h
11D4h	32	VIM_INTPRIORITY_117	50F0 11D4h
11D8h	32	VIM_INTPRIORITY_118	50F0 11D8h
11DCh	32	VIM_INTPRIORITY_119	50F0 11DCh
11E0h	32	VIM_INTPRIORITY_120	50F0 11E0h
11E4h	32	VIM_INTPRIORITY_121	50F0 11E4h
11E8h	32	VIM_INTPRIORITY_122	50F0 11E8h
11ECh	32	VIM_INTPRIORITY_123	50F0 11ECh
11F0h	32	VIM_INTPRIORITY_124	50F0 11F0h
11F4h	32	VIM_INTPRIORITY_125	50F0 11F4h
11F8h	32	VIM_INTPRIORITY_126	50F0 11F8h
11FCh	32	VIM_INTPRIORITY_127	50F0 11FCh
1200h	32	VIM_INTPRIORITY_128	50F0 1200h
1204h	32	VIM_INTPRIORITY_129	50F0 1204h
1208h	32	VIM_INTPRIORITY_130	50F0 1208h
120Ch	32	VIM_INTPRIORITY_131	50F0 120Ch
1210h	32	VIM_INTPRIORITY_132	50F0 1210h
1214h	32	VIM_INTPRIORITY_133	50F0 1214h
1218h	32	VIM_INTPRIORITY_134	50F0 1218h
121Ch	32	VIM_INTPRIORITY_135	50F0 121Ch
1220h	32	VIM_INTPRIORITY_136	50F0 1220h
1224h	32	VIM_INTPRIORITY_137	50F0 1224h
1228h	32	VIM_INTPRIORITY_138	50F0 1228h
122Ch	32	VIM_INTPRIORITY_139	50F0 122Ch
1230h	32	VIM_INTPRIORITY_140	50F0 1230h
1234h	32	VIM_INTPRIORITY_141	50F0 1234h
1238h	32	VIM_INTPRIORITY_142	50F0 1238h
123Ch	32	VIM_INTPRIORITY_143	50F0 123Ch
1240h	32	VIM_INTPRIORITY_144	50F0 1240h
1244h	32	VIM_INTPRIORITY_145	50F0 1244h
1248h	32	VIM_INTPRIORITY_146	50F0 1248h
124Ch	32	VIM_INTPRIORITY_147	50F0 124Ch
1250h	32	VIM_INTPRIORITY_148	50F0 1250h
1254h	32	VIM_INTPRIORITY_149	50F0 1254h
1258h	32	VIM_INTPRIORITY_150	50F0 1258h
125Ch	32	VIM_INTPRIORITY_151	50F0 125Ch
1260h	32	VIM_INTPRIORITY_152	50F0 1260h
1264h	32	VIM_INTPRIORITY_153	50F0 1264h
1268h	32	VIM_INTPRIORITY_154	50F0 1268h
126Ch	32	VIM_INTPRIORITY_155	50F0 126Ch
1270h	32	VIM_INTPRIORITY_156	50F0 1270h
1274h	32	VIM_INTPRIORITY_157	50F0 1274h
1278h	32	VIM_INTPRIORITY_158	50F0 1278h
127Ch	32	VIM_INTPRIORITY_159	50F0 127Ch
1280h	32	VIM_INTPRIORITY_160	50F0 1280h
1284h	32	VIM_INTPRIORITY_161	50F0 1284h

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Table 4-2637. MSS_VIM Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_VIM Physical Address
1288h	32	VIM_INTPRIORITY_162	50F0 1288h
128Ch	32	VIM_INTPRIORITY_163	50F0 128Ch
1290h	32	VIM_INTPRIORITY_164	50F0 1290h
1294h	32	VIM_INTPRIORITY_165	50F0 1294h
1298h	32	VIM_INTPRIORITY_166	50F0 1298h
129Ch	32	VIM_INTPRIORITY_167	50F0 129Ch
12A0h	32	VIM_INTPRIORITY_168	50F0 12A0h
12A4h	32	VIM_INTPRIORITY_169	50F0 12A4h
12A8h	32	VIM_INTPRIORITY_170	50F0 12A8h
12ACh	32	VIM_INTPRIORITY_171	50F0 12ACh
12B0h	32	VIM_INTPRIORITY_172	50F0 12B0h
12B4h	32	VIM_INTPRIORITY_173	50F0 12B4h
12B8h	32	VIM_INTPRIORITY_174	50F0 12B8h
12BCh	32	VIM_INTPRIORITY_175	50F0 12BCh
12C0h	32	VIM_INTPRIORITY_176	50F0 12C0h
12C4h	32	VIM_INTPRIORITY_177	50F0 12C4h
12C8h	32	VIM_INTPRIORITY_178	50F0 12C8h
12CCh	32	VIM_INTPRIORITY_179	50F0 12CCh
12D0h	32	VIM_INTPRIORITY_180	50F0 12D0h
12D4h	32	VIM_INTPRIORITY_181	50F0 12D4h
12D8h	32	VIM_INTPRIORITY_182	50F0 12D8h
12DCh	32	VIM_INTPRIORITY_183	50F0 12DCh
12E0h	32	VIM_INTPRIORITY_184	50F0 12E0h
12E4h	32	VIM_INTPRIORITY_185	50F0 12E4h
12E8h	32	VIM_INTPRIORITY_186	50F0 12E8h
12ECh	32	VIM_INTPRIORITY_187	50F0 12ECh
12F0h	32	VIM_INTPRIORITY_188	50F0 12F0h
12F4h	32	VIM_INTPRIORITY_189	50F0 12F4h
12F8h	32	VIM_INTPRIORITY_190	50F0 12F8h
12FCh	32	VIM_INTPRIORITY_191	50F0 12FCh
1300h	32	VIM_INTPRIORITY_192	50F0 1300h
1304h	32	VIM_INTPRIORITY_193	50F0 1304h
1308h	32	VIM_INTPRIORITY_194	50F0 1308h
130Ch	32	VIM_INTPRIORITY_195	50F0 130Ch
1310h	32	VIM_INTPRIORITY_196	50F0 1310h
1314h	32	VIM_INTPRIORITY_197	50F0 1314h
1318h	32	VIM_INTPRIORITY_198	50F0 1318h
131Ch	32	VIM_INTPRIORITY_199	50F0 131Ch
1320h	32	VIM_INTPRIORITY_200	50F0 1320h
1324h	32	VIM_INTPRIORITY_201	50F0 1324h
1328h	32	VIM_INTPRIORITY_202	50F0 1328h
132Ch	32	VIM_INTPRIORITY_203	50F0 132Ch
1330h	32	VIM_INTPRIORITY_204	50F0 1330h
1334h	32	VIM_INTPRIORITY_205	50F0 1334h
1338h	32	VIM_INTPRIORITY_206	50F0 1338h
133Ch	32	VIM_INTPRIORITY_207	50F0 133Ch
1340h	32	VIM_INTPRIORITY_208	50F0 1340h

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Table 4-2637. MSS_VIM Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_VIM Physical Address
1344h	32	VIM_INTPRIORITY_209	50F0 1344h
1348h	32	VIM_INTPRIORITY_210	50F0 1348h
134Ch	32	VIM_INTPRIORITY_211	50F0 134Ch
1350h	32	VIM_INTPRIORITY_212	50F0 1350h
1354h	32	VIM_INTPRIORITY_213	50F0 1354h
1358h	32	VIM_INTPRIORITY_214	50F0 1358h
135Ch	32	VIM_INTPRIORITY_215	50F0 135Ch
1360h	32	VIM_INTPRIORITY_216	50F0 1360h
1364h	32	VIM_INTPRIORITY_217	50F0 1364h
1368h	32	VIM_INTPRIORITY_218	50F0 1368h
136Ch	32	VIM_INTPRIORITY_219	50F0 136Ch
1370h	32	VIM_INTPRIORITY_220	50F0 1370h
1374h	32	VIM_INTPRIORITY_221	50F0 1374h
1378h	32	VIM_INTPRIORITY_222	50F0 1378h
137Ch	32	VIM_INTPRIORITY_223	50F0 137Ch
1380h	32	VIM_INTPRIORITY_224	50F0 1380h
1384h	32	VIM_INTPRIORITY_225	50F0 1384h
1388h	32	VIM_INTPRIORITY_226	50F0 1388h
138Ch	32	VIM_INTPRIORITY_227	50F0 138Ch
1390h	32	VIM_INTPRIORITY_228	50F0 1390h
1394h	32	VIM_INTPRIORITY_229	50F0 1394h
1398h	32	VIM_INTPRIORITY_230	50F0 1398h
139Ch	32	VIM_INTPRIORITY_231	50F0 139Ch
13A0h	32	VIM_INTPRIORITY_232	50F0 13A0h
13A4h	32	VIM_INTPRIORITY_233	50F0 13A4h
13A8h	32	VIM_INTPRIORITY_234	50F0 13A8h
13ACh	32	VIM_INTPRIORITY_235	50F0 13ACh
13B0h	32	VIM_INTPRIORITY_236	50F0 13B0h
13B4h	32	VIM_INTPRIORITY_237	50F0 13B4h
13B8h	32	VIM_INTPRIORITY_238	50F0 13B8h
13BCh	32	VIM_INTPRIORITY_239	50F0 13BCh
13C0h	32	VIM_INTPRIORITY_240	50F0 13C0h
13C4h	32	VIM_INTPRIORITY_241	50F0 13C4h
13C8h	32	VIM_INTPRIORITY_242	50F0 13C8h
13CCh	32	VIM_INTPRIORITY_243	50F0 13CCh
13D0h	32	VIM_INTPRIORITY_244	50F0 13D0h
13D4h	32	VIM_INTPRIORITY_245	50F0 13D4h
13D8h	32	VIM_INTPRIORITY_246	50F0 13D8h
13DCh	32	VIM_INTPRIORITY_247	50F0 13DCh
13E0h	32	VIM_INTPRIORITY_248	50F0 13E0h
13E4h	32	VIM_INTPRIORITY_249	50F0 13E4h
13E8h	32	VIM_INTPRIORITY_250	50F0 13E8h
13ECh	32	VIM_INTPRIORITY_251	50F0 13ECh
13F0h	32	VIM_INTPRIORITY_252	50F0 13F0h
13F4h	32	VIM_INTPRIORITY_253	50F0 13F4h
13F8h	32	VIM_INTPRIORITY_254	50F0 13F8h
13FCh	32	VIM_INTPRIORITY_255	50F0 13FCh

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Table 4-2637. MSS_VIM Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_VIM Physical Address
2000h	32	VIM_INTVECTOR_0	50F0 2000h
2004h	32	VIM_INTVECTOR_1	50F0 2004h
2008h	32	VIM_INTVECTOR_2	50F0 2008h
200Ch	32	VIM_INTVECTOR_3	50F0 200Ch
2010h	32	VIM_INTVECTOR_4	50F0 2010h
2014h	32	VIM_INTVECTOR_5	50F0 2014h
2018h	32	VIM_INTVECTOR_6	50F0 2018h
201Ch	32	VIM_INTVECTOR_7	50F0 201Ch
2020h	32	VIM_INTVECTOR_8	50F0 2020h
2024h	32	VIM_INTVECTOR_9	50F0 2024h
2028h	32	VIM_INTVECTOR_10	50F0 2028h
202Ch	32	VIM_INTVECTOR_11	50F0 202Ch
2030h	32	VIM_INTVECTOR_12	50F0 2030h
2034h	32	VIM_INTVECTOR_13	50F0 2034h
2038h	32	VIM_INTVECTOR_14	50F0 2038h
203Ch	32	VIM_INTVECTOR_15	50F0 203Ch
2040h	32	VIM_INTVECTOR_16	50F0 2040h
2044h	32	VIM_INTVECTOR_17	50F0 2044h
2048h	32	VIM_INTVECTOR_18	50F0 2048h
204Ch	32	VIM_INTVECTOR_19	50F0 204Ch
2050h	32	VIM_INTVECTOR_20	50F0 2050h
2054h	32	VIM_INTVECTOR_21	50F0 2054h
2058h	32	VIM_INTVECTOR_22	50F0 2058h
205Ch	32	VIM_INTVECTOR_23	50F0 205Ch
2060h	32	VIM_INTVECTOR_24	50F0 2060h
2064h	32	VIM_INTVECTOR_25	50F0 2064h
2068h	32	VIM_INTVECTOR_26	50F0 2068h
206Ch	32	VIM_INTVECTOR_27	50F0 206Ch
2070h	32	VIM_INTVECTOR_28	50F0 2070h
2074h	32	VIM_INTVECTOR_29	50F0 2074h
2078h	32	VIM_INTVECTOR_30	50F0 2078h
207Ch	32	VIM_INTVECTOR_31	50F0 207Ch
2080h	32	VIM_INTVECTOR_32	50F0 2080h
2084h	32	VIM_INTVECTOR_33	50F0 2084h
2088h	32	VIM_INTVECTOR_34	50F0 2088h
208Ch	32	VIM_INTVECTOR_35	50F0 208Ch
2090h	32	VIM_INTVECTOR_36	50F0 2090h
2094h	32	VIM_INTVECTOR_37	50F0 2094h
2098h	32	VIM_INTVECTOR_38	50F0 2098h
209Ch	32	VIM_INTVECTOR_39	50F0 209Ch
20A0h	32	VIM_INTVECTOR_40	50F0 20A0h
20A4h	32	VIM_INTVECTOR_41	50F0 20A4h
20A8h	32	VIM_INTVECTOR_42	50F0 20A8h
20ACh	32	VIM_INTVECTOR_43	50F0 20ACh
20B0h	32	VIM_INTVECTOR_44	50F0 20B0h
20B4h	32	VIM_INTVECTOR_45	50F0 20B4h
20B8h	32	VIM_INTVECTOR_46	50F0 20B8h

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Table 4-2637. MSS_VIM Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_VIM Physical Address
20BCh	32	VIM_INTVECTOR_47	50F0 20BCh
20C0h	32	VIM_INTVECTOR_48	50F0 20C0h
20C4h	32	VIM_INTVECTOR_49	50F0 20C4h
20C8h	32	VIM_INTVECTOR_50	50F0 20C8h
20CCh	32	VIM_INTVECTOR_51	50F0 20CCh
20D0h	32	VIM_INTVECTOR_52	50F0 20D0h
20D4h	32	VIM_INTVECTOR_53	50F0 20D4h
20D8h	32	VIM_INTVECTOR_54	50F0 20D8h
20DCh	32	VIM_INTVECTOR_55	50F0 20DCh
20E0h	32	VIM_INTVECTOR_56	50F0 20E0h
20E4h	32	VIM_INTVECTOR_57	50F0 20E4h
20E8h	32	VIM_INTVECTOR_58	50F0 20E8h
20ECh	32	VIM_INTVECTOR_59	50F0 20ECh
20F0h	32	VIM_INTVECTOR_60	50F0 20F0h
20F4h	32	VIM_INTVECTOR_61	50F0 20F4h
20F8h	32	VIM_INTVECTOR_62	50F0 20F8h
20FCh	32	VIM_INTVECTOR_63	50F0 20FCh
2100h	32	VIM_INTVECTOR_64	50F0 2100h
2104h	32	VIM_INTVECTOR_65	50F0 2104h
2108h	32	VIM_INTVECTOR_66	50F0 2108h
210Ch	32	VIM_INTVECTOR_67	50F0 210Ch
2110h	32	VIM_INTVECTOR_68	50F0 2110h
2114h	32	VIM_INTVECTOR_69	50F0 2114h
2118h	32	VIM_INTVECTOR_70	50F0 2118h
211Ch	32	VIM_INTVECTOR_71	50F0 211Ch
2120h	32	VIM_INTVECTOR_72	50F0 2120h
2124h	32	VIM_INTVECTOR_73	50F0 2124h
2128h	32	VIM_INTVECTOR_74	50F0 2128h
212Ch	32	VIM_INTVECTOR_75	50F0 212Ch
2130h	32	VIM_INTVECTOR_76	50F0 2130h
2134h	32	VIM_INTVECTOR_77	50F0 2134h
2138h	32	VIM_INTVECTOR_78	50F0 2138h
213Ch	32	VIM_INTVECTOR_79	50F0 213Ch
2140h	32	VIM_INTVECTOR_80	50F0 2140h
2144h	32	VIM_INTVECTOR_81	50F0 2144h
2148h	32	VIM_INTVECTOR_82	50F0 2148h
214Ch	32	VIM_INTVECTOR_83	50F0 214Ch
2150h	32	VIM_INTVECTOR_84	50F0 2150h
2154h	32	VIM_INTVECTOR_85	50F0 2154h
2158h	32	VIM_INTVECTOR_86	50F0 2158h
215Ch	32	VIM_INTVECTOR_87	50F0 215Ch
2160h	32	VIM_INTVECTOR_88	50F0 2160h
2164h	32	VIM_INTVECTOR_89	50F0 2164h
2168h	32	VIM_INTVECTOR_90	50F0 2168h
216Ch	32	VIM_INTVECTOR_91	50F0 216Ch
2170h	32	VIM_INTVECTOR_92	50F0 2170h
2174h	32	VIM_INTVECTOR_93	50F0 2174h

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Table 4-2637. MSS_VIM Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_VIM Physical Address
2178h	32	VIM_INTVECTOR_94	50F0 2178h
217Ch	32	VIM_INTVECTOR_95	50F0 217Ch
2180h	32	VIM_INTVECTOR_96	50F0 2180h
2184h	32	VIM_INTVECTOR_97	50F0 2184h
2188h	32	VIM_INTVECTOR_98	50F0 2188h
218Ch	32	VIM_INTVECTOR_99	50F0 218Ch
2190h	32	VIM_INTVECTOR_100	50F0 2190h
2194h	32	VIM_INTVECTOR_101	50F0 2194h
2198h	32	VIM_INTVECTOR_102	50F0 2198h
219Ch	32	VIM_INTVECTOR_103	50F0 219Ch
21A0h	32	VIM_INTVECTOR_104	50F0 21A0h
21A4h	32	VIM_INTVECTOR_105	50F0 21A4h
21A8h	32	VIM_INTVECTOR_106	50F0 21A8h
21ACh	32	VIM_INTVECTOR_107	50F0 21ACh
21B0h	32	VIM_INTVECTOR_108	50F0 21B0h
21B4h	32	VIM_INTVECTOR_109	50F0 21B4h
21B8h	32	VIM_INTVECTOR_110	50F0 21B8h
21BCh	32	VIM_INTVECTOR_111	50F0 21BCh
21C0h	32	VIM_INTVECTOR_112	50F0 21C0h
21C4h	32	VIM_INTVECTOR_113	50F0 21C4h
21C8h	32	VIM_INTVECTOR_114	50F0 21C8h
21CCh	32	VIM_INTVECTOR_115	50F0 21CCh
21D0h	32	VIM_INTVECTOR_116	50F0 21D0h
21D4h	32	VIM_INTVECTOR_117	50F0 21D4h
21D8h	32	VIM_INTVECTOR_118	50F0 21D8h
21DCh	32	VIM_INTVECTOR_119	50F0 21DCh
21E0h	32	VIM_INTVECTOR_120	50F0 21E0h
21E4h	32	VIM_INTVECTOR_121	50F0 21E4h
21E8h	32	VIM_INTVECTOR_122	50F0 21E8h
21ECh	32	VIM_INTVECTOR_123	50F0 21ECh
21F0h	32	VIM_INTVECTOR_124	50F0 21F0h
21F4h	32	VIM_INTVECTOR_125	50F0 21F4h
21F8h	32	VIM_INTVECTOR_126	50F0 21F8h
21FCh	32	VIM_INTVECTOR_127	50F0 21FCh
2200h	32	VIM_INTVECTOR_128	50F0 2200h
2204h	32	VIM_INTVECTOR_129	50F0 2204h
2208h	32	VIM_INTVECTOR_130	50F0 2208h
220Ch	32	VIM_INTVECTOR_131	50F0 220Ch
2210h	32	VIM_INTVECTOR_132	50F0 2210h
2214h	32	VIM_INTVECTOR_133	50F0 2214h
2218h	32	VIM_INTVECTOR_134	50F0 2218h
221Ch	32	VIM_INTVECTOR_135	50F0 221Ch
2220h	32	VIM_INTVECTOR_136	50F0 2220h
2224h	32	VIM_INTVECTOR_137	50F0 2224h
2228h	32	VIM_INTVECTOR_138	50F0 2228h
222Ch	32	VIM_INTVECTOR_139	50F0 222Ch
2230h	32	VIM_INTVECTOR_140	50F0 2230h

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Table 4-2637. MSS_VIM Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_VIM Physical Address
2234h	32	VIM_INTVECTOR_141	50F0 2234h
2238h	32	VIM_INTVECTOR_142	50F0 2238h
223Ch	32	VIM_INTVECTOR_143	50F0 223Ch
2240h	32	VIM_INTVECTOR_144	50F0 2240h
2244h	32	VIM_INTVECTOR_145	50F0 2244h
2248h	32	VIM_INTVECTOR_146	50F0 2248h
224Ch	32	VIM_INTVECTOR_147	50F0 224Ch
2250h	32	VIM_INTVECTOR_148	50F0 2250h
2254h	32	VIM_INTVECTOR_149	50F0 2254h
2258h	32	VIM_INTVECTOR_150	50F0 2258h
225Ch	32	VIM_INTVECTOR_151	50F0 225Ch
2260h	32	VIM_INTVECTOR_152	50F0 2260h
2264h	32	VIM_INTVECTOR_153	50F0 2264h
2268h	32	VIM_INTVECTOR_154	50F0 2268h
226Ch	32	VIM_INTVECTOR_155	50F0 226Ch
2270h	32	VIM_INTVECTOR_156	50F0 2270h
2274h	32	VIM_INTVECTOR_157	50F0 2274h
2278h	32	VIM_INTVECTOR_158	50F0 2278h
227Ch	32	VIM_INTVECTOR_159	50F0 227Ch
2280h	32	VIM_INTVECTOR_160	50F0 2280h
2284h	32	VIM_INTVECTOR_161	50F0 2284h
2288h	32	VIM_INTVECTOR_162	50F0 2288h
228Ch	32	VIM_INTVECTOR_163	50F0 228Ch
2290h	32	VIM_INTVECTOR_164	50F0 2290h
2294h	32	VIM_INTVECTOR_165	50F0 2294h
2298h	32	VIM_INTVECTOR_166	50F0 2298h
229Ch	32	VIM_INTVECTOR_167	50F0 229Ch
22A0h	32	VIM_INTVECTOR_168	50F0 22A0h
22A4h	32	VIM_INTVECTOR_169	50F0 22A4h
22A8h	32	VIM_INTVECTOR_170	50F0 22A8h
22ACh	32	VIM_INTVECTOR_171	50F0 22ACh
22B0h	32	VIM_INTVECTOR_172	50F0 22B0h
22B4h	32	VIM_INTVECTOR_173	50F0 22B4h
22B8h	32	VIM_INTVECTOR_174	50F0 22B8h
22BCh	32	VIM_INTVECTOR_175	50F0 22BCh
22C0h	32	VIM_INTVECTOR_176	50F0 22C0h
22C4h	32	VIM_INTVECTOR_177	50F0 22C4h
22C8h	32	VIM_INTVECTOR_178	50F0 22C8h
22CCh	32	VIM_INTVECTOR_179	50F0 22CCh
22D0h	32	VIM_INTVECTOR_180	50F0 22D0h
22D4h	32	VIM_INTVECTOR_181	50F0 22D4h
22D8h	32	VIM_INTVECTOR_182	50F0 22D8h
22DCh	32	VIM_INTVECTOR_183	50F0 22DCh
22E0h	32	VIM_INTVECTOR_184	50F0 22E0h
22E4h	32	VIM_INTVECTOR_185	50F0 22E4h
22E8h	32	VIM_INTVECTOR_186	50F0 22E8h
22ECh	32	VIM_INTVECTOR_187	50F0 22ECh

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Table 4-2637. MSS_VIM Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_VIM Physical Address
22F0h	32	VIM_INTVECTOR_188	50F0 22F0h
22F4h	32	VIM_INTVECTOR_189	50F0 22F4h
22F8h	32	VIM_INTVECTOR_190	50F0 22F8h
22FCh	32	VIM_INTVECTOR_191	50F0 22FCh
2300h	32	VIM_INTVECTOR_192	50F0 2300h
2304h	32	VIM_INTVECTOR_193	50F0 2304h
2308h	32	VIM_INTVECTOR_194	50F0 2308h
230Ch	32	VIM_INTVECTOR_195	50F0 230Ch
2310h	32	VIM_INTVECTOR_196	50F0 2310h
2314h	32	VIM_INTVECTOR_197	50F0 2314h
2318h	32	VIM_INTVECTOR_198	50F0 2318h
231Ch	32	VIM_INTVECTOR_199	50F0 231Ch
2320h	32	VIM_INTVECTOR_200	50F0 2320h
2324h	32	VIM_INTVECTOR_201	50F0 2324h
2328h	32	VIM_INTVECTOR_202	50F0 2328h
232Ch	32	VIM_INTVECTOR_203	50F0 232Ch
2330h	32	VIM_INTVECTOR_204	50F0 2330h
2334h	32	VIM_INTVECTOR_205	50F0 2334h
2338h	32	VIM_INTVECTOR_206	50F0 2338h
233Ch	32	VIM_INTVECTOR_207	50F0 233Ch
2340h	32	VIM_INTVECTOR_208	50F0 2340h
2344h	32	VIM_INTVECTOR_209	50F0 2344h
2348h	32	VIM_INTVECTOR_210	50F0 2348h
234Ch	32	VIM_INTVECTOR_211	50F0 234Ch
2350h	32	VIM_INTVECTOR_212	50F0 2350h
2354h	32	VIM_INTVECTOR_213	50F0 2354h
2358h	32	VIM_INTVECTOR_214	50F0 2358h
235Ch	32	VIM_INTVECTOR_215	50F0 235Ch
2360h	32	VIM_INTVECTOR_216	50F0 2360h
2364h	32	VIM_INTVECTOR_217	50F0 2364h
2368h	32	VIM_INTVECTOR_218	50F0 2368h
236Ch	32	VIM_INTVECTOR_219	50F0 236Ch
2370h	32	VIM_INTVECTOR_220	50F0 2370h
2374h	32	VIM_INTVECTOR_221	50F0 2374h
2378h	32	VIM_INTVECTOR_222	50F0 2378h
237Ch	32	VIM_INTVECTOR_223	50F0 237Ch
2380h	32	VIM_INTVECTOR_224	50F0 2380h
2384h	32	VIM_INTVECTOR_225	50F0 2384h
2388h	32	VIM_INTVECTOR_226	50F0 2388h
238Ch	32	VIM_INTVECTOR_227	50F0 238Ch
2390h	32	VIM_INTVECTOR_228	50F0 2390h
2394h	32	VIM_INTVECTOR_229	50F0 2394h
2398h	32	VIM_INTVECTOR_230	50F0 2398h
239Ch	32	VIM_INTVECTOR_231	50F0 239Ch
23A0h	32	VIM_INTVECTOR_232	50F0 23A0h
23A4h	32	VIM_INTVECTOR_233	50F0 23A4h
23A8h	32	VIM_INTVECTOR_234	50F0 23A8h

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Table 4-2637. MSS_VIM Registers Base Address Table (continued)

Offset	Length	Acronym	MSS_VIM Physical Address
23ACh	32	VIM_INTVECTOR_235	50F0 23ACh
23B0h	32	VIM_INTVECTOR_236	50F0 23B0h
23B4h	32	VIM_INTVECTOR_237	50F0 23B4h
23B8h	32	VIM_INTVECTOR_238	50F0 23B8h
23BCh	32	VIM_INTVECTOR_239	50F0 23BCh
23C0h	32	VIM_INTVECTOR_240	50F0 23C0h
23C4h	32	VIM_INTVECTOR_241	50F0 23C4h
23C8h	32	VIM_INTVECTOR_242	50F0 23C8h
23CCh	32	VIM_INTVECTOR_243	50F0 23CCh
23D0h	32	VIM_INTVECTOR_244	50F0 23D0h
23D4h	32	VIM_INTVECTOR_245	50F0 23D4h
23D8h	32	VIM_INTVECTOR_246	50F0 23D8h
23DCh	32	VIM_INTVECTOR_247	50F0 23DCh
23E0h	32	VIM_INTVECTOR_248	50F0 23E0h
23E4h	32	VIM_INTVECTOR_249	50F0 23E4h
23E8h	32	VIM_INTVECTOR_250	50F0 23E8h
23ECh	32	VIM_INTVECTOR_251	50F0 23ECh
23F0h	32	VIM_INTVECTOR_252	50F0 23F0h
23F4h	32	VIM_INTVECTOR_253	50F0 23F4h
23F8h	32	VIM_INTVECTOR_254	50F0 23F8h
23FCh	32	VIM_INTVECTOR_255	50F0 23FCh

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4.35.1 MSS_VIM_PID Registers

4.35.1.1 VIM_PID Register (Offset = 0h) [reset = h]

Short Description: The Revision Register contains the major and minor revisions for the module.

Long Description:

Return to Summary Table

Table 4-2638. Instance Table

Instance Name	Physical Address
VIM	50F0 0000h

Access Types Legend

Table 4-2639. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID register scheme
29 - 28	BU	RO	Ah	Business Unit: 10 = Processors
27 - 16	FUNC	RO	98BD90h	Module ID
15 - 11	RTL	RO	0h	RTL revision. Will vary depending on release.
10 - 8	MAJOR	RO	0h	Major revision
7 - 6	CUSTOM	RO	0h	Custom
5 - 0	MINOR	RO	1h	Minor revision

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4.35.2 MSS_VIM_INFO Registers

4.35.2.1 VIM_INFO Register (Offset = 4h) [reset = h]

Short Description: The Info Register gives the configuration Inforrmation of this VIM.

Long Description:

Return to Summary Table

Table 4-2640. Instance Table

Instance Name	Physical Address
VIM	50F0 0004h

Access Types Legend

Table 4-2641. INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 11	RES1	RO	0h	RESERVE FIELD
10 - 0	INTERRUPTS	RO	5F5E100h	Total number of Interrupts

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4.35.3 MSS_VIM_PRIIRQ Registers

4.35.3.1 VIM_PRIIRQ Register (Offset = 8h) [reset = h]

Short Description: The Prioritized IRQ Register shows the number of the highest priority pending IRQ.

Long Description:

Return to Summary Table

Table 4-2642. Instance Table

Instance Name	Physical Address
VIM	50F0 0008h

Access Types Legend

Table 4-2643. PRIIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	RO	0h	Indicates that the num field is valid.
30 - 20	RES2	RO	0h	RESERVE FIELD
19 - 16	PRI	RO	0h	Priority of the highest priority pending IRQ. valid only if the valid flag is set.
15 - 10	RES3	RO	0h	RESERVE FIELD
9 - 0	NUM	RO	0h	Number of the highest priority pending IRQ. valid only if the valid flag is set.

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4.35.4 MSS_VIM_PRIFIQ Registers

4.35.4.1 VIM_PRIFIQ Register (Offset = Ch) [reset = h]

Short Description: The Prioritized FIQ Register shows the number of the highest priority pending FIQ.

Long Description:

Return to Summary Table

Table 4-2644. Instance Table

Instance Name	Physical Address
VIM	50F0 000Ch

Access Types Legend

Table 4-2645. PRIFIQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	RO	0h	Indicates that the num field is valid.
30 - 20	RES4	RO	0h	RESERVE FIELD
19 - 16	PRI	RO	0h	Priority of the highest priority pending FIQ. valid only if the valid flag is set.
15 - 10	RES5	RO	0h	RESERVE FIELD
9 - 0	NUM	RO	0h	Number of the highest priority pending FIQ. valid only if the valid flag is set.

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4.35.5 MSS_VIM_IRQGSTS Registers

4.35.5.1 VIM_IRQGSTS Register (Offset = 10h) [reset = h]

Short Description: The IRQ Group Status Register indicates which groups have pending IRQ interrupts.

Long Description:

Return to Summary Table

Table 4-2646. Instance Table

Instance Name	Physical Address
VIM	50F0 0010h

Access Types Legend

Table 4-2647. IRQGSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RO	0h	Indicates that the num field is valid.

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4.35.6 MSS_VIM_FIQGSTS Registers

4.35.6.1 VIM_FIQGSTS Register (Offset = 14h) [reset = h]

Short Description: The FIQ Group Status Register indicates which groups have pending FIQ interrupts.

Long Description:

Return to Summary Table

Table 4-2648. Instance Table

Instance Name	Physical Address
VIM	50F0 0014h

Access Types Legend

Table 4-2649. FIQGSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RO	0h	Indicates that the num field is valid.

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4.35.7 MSS_VIM_IRQVEC Registers

4.35.7.1 VIM_IRQVEC Register (Offset = 18h) [reset = h]

Short Description: The IRQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pendind IRQ.

Long Description:

Return to Summary Table

Table 4-2650. Instance Table

Instance Name	Physical Address
VIM	50F0 0018h

Access Types Legend

Table 4-2651. IRQVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	Upper 30 bits of the 32-bit vector address. Only valid if the Prioritized IRQ Register valid flag is true.
1 - 0	RES21	RO	0h	RESERVE FIELD

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4.35.8 MSS_VIM_FIQVEC Registers

4.35.8.1 VIM_FIQVEC Register (Offset = 1Ch) [reset = h]

Short Description: The FIQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pendind FIQ.

Long Description:

Return to Summary Table

Table 4-2652. Instance Table

Instance Name	Physical Address
VIM	50F0 001Ch

Access Types Legend

Table 4-2653. FIQVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	Upper 30 bits of the 32-bit vector address. Only valid if the Prioritized FIQ Register valid flag is true.
1 - 0	RES22	RO	0h	RESERVE FIELD

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4.35.9 MSS_VIM_ACTIRQ Registers

4.35.9.1 VIM_ACTIRQ Register (Offset = 20h) [reset = h]

Short Description: The Active IRQ Register shows the number of the currently active IRQ.

Long Description:

Return to Summary Table

Table 4-2654. Instance Table

Instance Name	Physical Address
VIM	50F0 0020h

Access Types Legend

Table 4-2655. ACTIRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	RO	0h	Indicates that the num field is valid. Set when the IRQ Vector Address Register is read and cleared whenever the IRQ Vector Address Register is written.
30 - 20	RES6	RO	0h	RESERVE FIELD
19 - 16	PRI	RO	0h	Priority of the highest priority pending IRQ. valid only if the valid flag is set.
15 - 10	RES7	RO	0h	RESERVE FIELD
9 - 0	NUM	RO	0h	Number of the currently active IRQ. Loaded from teh Prioritized IRQ Register whenever the IRQ Vector Address is read. Valid only if the valid flag is set.

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4.35.10 MSS_VIM_ACTFIQ Registers

4.35.10.1 VIM_ACTFIQ Register (Offset = 24h) [reset = h]

Short Description: The Active FIQ Register shows the number of the currently active FIQ.

Long Description:

Return to Summary Table

Table 4-2656. Instance Table

Instance Name	Physical Address
VIM	50F0 0024h

Access Types Legend

Table 4-2657. ACTFIQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31	VALID	RO	0h	Indicates that the num field is valid. Set when the FIQ Vector Address Register is read and cleared whenever the FIQ Vector Address Register is written.
30 - 20	RES8	RO	0h	RESERVE FIELD
19 - 16	PRI	RO	0h	Priority of the highest priority pending IRQ. valid only if the valid flag is set.
15 - 10	RES9	RO	0h	RESERVE FIELD
9 - 0	NUM	RO	0h	Number of the currently active FIQ. Loaded from teh Prioritized FIQ Register whenever the FIQ Vector Address is read. Valid only if the valid flag is set.

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4.35.11 MSS_VIM_IRQPRIMSK Registers

4.35.11.1 VIM_IRQPRIMSK Register (Offset = 28h) [reset = h]

Short Description: The IRQ Priority Mask Register allows all IRQs of a particular priority to be enabled or disabled.

Long Description:

Return to Summary Table

Table 4-2658. Instance Table

Instance Name	Physical Address
VIM	50F0 0028h

Access Types Legend

Table 4-2659. IRQPRIMSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RES24	RO	0h	RESERVE FIELD
15 - 0	MSK	RW	3F28CB715 71C7h	Each bit corresponds to the given priority. 1 - IRQs of this priority are enabled. 0 - IRQs of this priority are disabled.

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4.35.12 MSS_VIM_FIQPRIMSK Registers

4.35.12.1 VIM_FIQPRIMSK Register (Offset = 2Ch) [reset = h]

Short Description: The FIQ Priority Mask Register allows all FIQs of a particular priority to be enabled or disabled.

Long Description:

Return to Summary Table

Table 4-2660. Instance Table

Instance Name	Physical Address
VIM	50F0 002Ch

Access Types Legend

Table 4-2661. FIQPRIMSK Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RES24	RO	0h	RESERVE FIELD
15 - 0	MSK	RW	3F28CB715 71C7h	Each bit corresponds to the given priority. 1 - FIQs of this priority are enabled. 0 - FIQs of this priority are disabled.

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4.35.13 MSS_VIM_DEDVEC Registers

4.35.13.1 VIM_DEDVEC Register (Offset = 30h) [reset = h]

Short Description: The DED Vector Address contains a default vector address for when an uncorrectable error is detected for an active IRQ or FIQ.

Long Description:

Return to Summary Table

Table 4-2662. Instance Table

Instance Name	Physical Address
VIM	50F0 0030h

Access Types Legend

Table 4-2663. DEDVEC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	Upper 30 bits of the 32-bit vector address.
1 - 0	RES23	RO	0h	RESERVE FIELD

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4.35.14 MSS_VIM_RAW Registers

4.35.14.1 VIM_RAW Register (Offset = 400h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description:

Return to Summary Table

Table 4-2664. Instance Table

Instance Name	Physical Address
VIM	50F0 0400h

Access Types Legend

Table 4-2665. RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

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4.35.15 MSS_VIM_STS Registers

4.35.15.1 VIM_STS Register (Offset = 404h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description:

Return to Summary Table

Table 4-2666. Instance Table

Instance Name	Physical Address
VIM	50F0 0404h

Access Types Legend

Table 4-2667. STS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

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4.35.16 MSS_VIM_INTR_EN_SET Registers

4.35.16.1 VIM_INTR_EN_SET Register (Offset = 408h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description:

Return to Summary Table

Table 4-2668. Instance Table

Instance Name	Physical Address
VIM	50F0 0408h

Access Types Legend

Table 4-2669. INTR_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

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4.35.17 MSS_VIM_INTER_EN_CLR Registers

4.35.17.1 VIM_INTER_EN_CLR Register (Offset = 40Ch) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description:

Return to Summary Table

Table 4-2670. Instance Table

Instance Name	Physical Address
VIM	50F0 040Ch

Access Types Legend

Table 4-2671. INTER_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

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4.35.18 MSS_VIM_IRQSTS Registers

4.35.18.1 VIM_IRQSTS Register (Offset = 410h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description:

Return to Summary Table

Table 4-2672. Instance Table

Instance Name	Physical Address
VIM	50F0 0410h

Access Types Legend

Table 4-2673. IRQSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

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4.35.19 MSS_VIM_FIQSTS Registers

4.35.19.1 VIM_FIQSTS Register (Offset = 414h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description:

Return to Summary Table

Table 4-2674. Instance Table

Instance Name	Physical Address
VIM	50F0 0414h

Access Types Legend

Table 4-2675. FIQSTS Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

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4.35.20 MSS_VIM_INTMAP Registers

4.35.20.1 VIM_INTMAP Register (Offset = 418h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description:

Return to Summary Table

Table 4-2676. Instance Table

Instance Name	Physical Address
VIM	50F0 0418h

Access Types Legend

Table 4-2677. INTMAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

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4.35.21 MSS_VIM_INTTYPE Registers

4.35.21.1 VIM_INTTYPE Register (Offset = 41Ch) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description:

Return to Summary Table

Table 4-2678. Instance Table

Instance Name	Physical Address
VIM	50F0 041Ch

Access Types Legend

Table 4-2679. INTTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

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4.35.22 MSS_VIM_RAW_1 Registers

4.35.22.1 VIM_RAW_1 Register (Offset = 420h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description:

Return to Summary Table

Table 4-2680. Instance Table

Instance Name	Physical Address
VIM	50F0 0420h

Access Types Legend

Table 4-2681. RAW_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

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4.35.23 MSS_VIM_STS_1 Registers

4.35.23.1 VIM_STS_1 Register (Offset = 424h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description:

Return to Summary Table

Table 4-2682. Instance Table

Instance Name	Physical Address
VIM	50F0 0424h

Access Types Legend

Table 4-2683. STS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

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4.35.24 MSS_VIM_INTR_EN_SET_1 Registers

4.35.24.1 VIM_INTR_EN_SET_1 Register (Offset = 428h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description:

Return to Summary Table

Table 4-2684. Instance Table

Instance Name	Physical Address
VIM	50F0 0428h

Access Types Legend

Table 4-2685. INTR_EN_SET_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

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4.35.25 MSS_VIM_INTER_EN_CLR_1 Registers

4.35.25.1 VIM_INTER_EN_CLR_1 Register (Offset = 42Ch) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description:

Return to Summary Table

Table 4-2686. Instance Table

Instance Name	Physical Address
VIM	50F0 042Ch

Access Types Legend

Table 4-2687. INTER_EN_CLR_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

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4.35.26 MSS_VIM_IRQSTS_1 Registers

4.35.26.1 VIM_IRQSTS_1 Register (Offset = 430h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description:

Return to Summary Table

Table 4-2688. Instance Table

Instance Name	Physical Address
VIM	50F0 0430h

Access Types Legend

Table 4-2689. IRQSTS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

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4.35.27 MSS_VIM_FIQSTS_1 Registers

4.35.27.1 VIM_FIQSTS_1 Register (Offset = 434h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description:

Return to Summary Table

Table 4-2690. Instance Table

Instance Name	Physical Address
VIM	50F0 0434h

Access Types Legend

Table 4-2691. FIQSTS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

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4.35.28 MSS_VIM_INTMAP_1 Registers

4.35.28.1 VIM_INTMAP_1 Register (Offset = 438h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description:

Return to Summary Table

Table 4-2692. Instance Table

Instance Name	Physical Address
VIM	50F0 0438h

Access Types Legend

Table 4-2693. INTMAP_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

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4.35.29 MSS_VIM_INTTYPE_1 Registers

4.35.29.1 VIM_INTTYPE_1 Register (Offset = 43Ch) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description:

Return to Summary Table

Table 4-2694. Instance Table

Instance Name	Physical Address
VIM	50F0 043Ch

Access Types Legend

Table 4-2695. INTTYPE_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

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4.35.30 MSS_VIM_RAW_2 Registers

4.35.30.1 VIM_RAW_2 Register (Offset = 440h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description:

Return to Summary Table

Table 4-2696. Instance Table

Instance Name	Physical Address
VIM	50F0 0440h

Access Types Legend

Table 4-2697. RAW_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

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4.35.31 MSS_VIM_STS_2 Registers

4.35.31.1 VIM_STS_2 Register (Offset = 444h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description:

Return to Summary Table

Table 4-2698. Instance Table

Instance Name	Physical Address
VIM	50F0 0444h

Access Types Legend

Table 4-2699. STS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

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4.35.32 MSS_VIM_INTR_EN_SET_2 Registers

4.35.32.1 VIM_INTR_EN_SET_2 Register (Offset = 448h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description:

Return to Summary Table

Table 4-2700. Instance Table

Instance Name	Physical Address
VIM	50F0 0448h

Access Types Legend

Table 4-2701. INTR_EN_SET_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

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4.35.33 MSS_VIM_INTER_EN_CLR_2 Registers

4.35.33.1 VIM_INTER_EN_CLR_2 Register (Offset = 44Ch) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description:

Return to Summary Table

Table 4-2702. Instance Table

Instance Name	Physical Address
VIM	50F0 044Ch

Access Types Legend

Table 4-2703. INTER_EN_CLR_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

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4.35.34 MSS_VIM_IRQSTS_2 Registers

4.35.34.1 VIM_IRQSTS_2 Register (Offset = 450h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description:

Return to Summary Table

Table 4-2704. Instance Table

Instance Name	Physical Address
VIM	50F0 0450h

Access Types Legend

Table 4-2705. IRQSTS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

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4.35.35 MSS_VIM_FIQSTS_2 Registers

4.35.35.1 VIM_FIQSTS_2 Register (Offset = 454h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description:

Return to Summary Table

Table 4-2706. Instance Table

Instance Name	Physical Address
VIM	50F0 0454h

Access Types Legend

Table 4-2707. FIQSTS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

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4.35.36 MSS_VIM_INTMAP_2 Registers

4.35.36.1 VIM_INTMAP_2 Register (Offset = 458h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description:

Return to Summary Table

Table 4-2708. Instance Table

Instance Name	Physical Address
VIM	50F0 0458h

Access Types Legend

Table 4-2709. INTMAP_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

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4.35.37 MSS_VIM_INTTYPE_2 Registers

4.35.37.1 VIM_INTTYPE_2 Register (Offset = 45Ch) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description:

Return to Summary Table

Table 4-2710. Instance Table

Instance Name	Physical Address
VIM	50F0 045Ch

Access Types Legend

Table 4-2711. INTTYPE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

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4.35.38 MSS_VIM_RAW_3 Registers

4.35.38.1 VIM_RAW_3 Register (Offset = 460h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description:

Return to Summary Table

Table 4-2712. Instance Table

Instance Name	Physical Address
VIM	50F0 0460h

Access Types Legend

Table 4-2713. RAW_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

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4.35.39 MSS_VIM_STS_3 Registers

4.35.39.1 VIM_STS_3 Register (Offset = 464h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description:

Return to Summary Table

Table 4-2714. Instance Table

Instance Name	Physical Address
VIM	50F0 0464h

Access Types Legend

Table 4-2715. STS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

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4.35.40 MSS_VIM_INTR_EN_SET_3 Registers

4.35.40.1 VIM_INTR_EN_SET_3 Register (Offset = 468h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description:

Return to Summary Table

Table 4-2716. Instance Table

Instance Name	Physical Address
VIM	50F0 0468h

Access Types Legend

Table 4-2717. INTR_EN_SET_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

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4.35.41 MSS_VIM_INTER_EN_CLR_3 Registers

4.35.41.1 VIM_INTER_EN_CLR_3 Register (Offset = 46Ch) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description:

Return to Summary Table

Table 4-2718. Instance Table

Instance Name	Physical Address
VIM	50F0 046Ch

Access Types Legend

Table 4-2719. INTER_EN_CLR_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

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4.35.42 MSS_VIM_IRQSTS_3 Registers

4.35.42.1 VIM_IRQSTS_3 Register (Offset = 470h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description:

Return to Summary Table

Table 4-2720. Instance Table

Instance Name	Physical Address
VIM	50F0 0470h

Access Types Legend

Table 4-2721. IRQSTS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

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4.35.43 MSS_VIM_FIQSTS_3 Registers

4.35.43.1 VIM_FIQSTS_3 Register (Offset = 474h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description:

Return to Summary Table

Table 4-2722. Instance Table

Instance Name	Physical Address
VIM	50F0 0474h

Access Types Legend

Table 4-2723. FIQSTS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

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4.35.44 MSS_VIM_INTMAP_3 Registers

4.35.44.1 VIM_INTMAP_3 Register (Offset = 478h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description:

Return to Summary Table

Table 4-2724. Instance Table

Instance Name	Physical Address
VIM	50F0 0478h

Access Types Legend

Table 4-2725. INTMAP_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

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4.35.45 MSS_VIM_INTTYPE_3 Registers

4.35.45.1 VIM_INTTYPE_3 Register (Offset = 47Ch) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description:

Return to Summary Table

Table 4-2726. Instance Table

Instance Name	Physical Address
VIM	50F0 047Ch

Access Types Legend

Table 4-2727. INTTYPE_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

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4.35.46 MSS_VIM_RAW_4 Registers

4.35.46.1 VIM_RAW_4 Register (Offset = 480h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description:

Return to Summary Table

Table 4-2728. Instance Table

Instance Name	Physical Address
VIM	50F0 0480h

Access Types Legend

Table 4-2729. RAW_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

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4.35.47 MSS_VIM_STS_4 Registers

4.35.47.1 VIM_STS_4 Register (Offset = 484h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description:

Return to Summary Table

Table 4-2730. Instance Table

Instance Name	Physical Address
VIM	50F0 0484h

Access Types Legend

Table 4-2731. STS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

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4.35.48 MSS_VIM_INTR_EN_SET_4 Registers

4.35.48.1 VIM_INTR_EN_SET_4 Register (Offset = 488h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description:

Return to Summary Table

Table 4-2732. Instance Table

Instance Name	Physical Address
VIM	50F0 0488h

Access Types Legend

Table 4-2733. INTR_EN_SET_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

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4.35.49 MSS_VIM_INTER_EN_CLR_4 Registers

4.35.49.1 VIM_INTER_EN_CLR_4 Register (Offset = 48Ch) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description:

Return to Summary Table

Table 4-2734. Instance Table

Instance Name	Physical Address
VIM	50F0 048Ch

Access Types Legend

Table 4-2735. INTER_EN_CLR_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

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4.35.50 MSS_VIM_IRQSTS_4 Registers

4.35.50.1 VIM_IRQSTS_4 Register (Offset = 490h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description:

Return to Summary Table

Table 4-2736. Instance Table

Instance Name	Physical Address
VIM	50F0 0490h

Access Types Legend

Table 4-2737. IRQSTS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

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4.35.51 MSS_VIM_FIQSTS_4 Registers

4.35.51.1 VIM_FIQSTS_4 Register (Offset = 494h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description:

Return to Summary Table

Table 4-2738. Instance Table

Instance Name	Physical Address
VIM	50F0 0494h

Access Types Legend

Table 4-2739. FIQSTS_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

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4.35.52 MSS_VIM_INTMAP_4 Registers

4.35.52.1 VIM_INTMAP_4 Register (Offset = 498h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description:

Return to Summary Table

Table 4-2740. Instance Table

Instance Name	Physical Address
VIM	50F0 0498h

Access Types Legend

Table 4-2741. INTMAP_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

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4.35.53 MSS_VIM_INTTYPE_4 Registers

4.35.53.1 VIM_INTTYPE_4 Register (Offset = 49Ch) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description:

Return to Summary Table

Table 4-2742. Instance Table

Instance Name	Physical Address
VIM	50F0 049Ch

Access Types Legend

Table 4-2743. INTTYPE_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

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4.35.54 MSS_VIM_RAW_5 Registers

4.35.54.1 VIM_RAW_5 Register (Offset = 4A0h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description:

Return to Summary Table

Table 4-2744. Instance Table

Instance Name	Physical Address
VIM	50F0 04A0h

Access Types Legend

Table 4-2745. RAW_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

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4.35.55 MSS_VIM_STS_5 Registers

4.35.55.1 VIM_STS_5 Register (Offset = 4A4h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description:

Return to Summary Table

Table 4-2746. Instance Table

Instance Name	Physical Address
VIM	50F0 04A4h

Access Types Legend

Table 4-2747. STS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

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4.35.56 MSS_VIM_INTR_EN_SET_5 Registers

4.35.56.1 VIM_INTR_EN_SET_5 Register (Offset = 4A8h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description:

Return to Summary Table

Table 4-2748. Instance Table

Instance Name	Physical Address
VIM	50F0 04A8h

Access Types Legend

Table 4-2749. INTR_EN_SET_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

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4.35.57 MSS_VIM_INTER_EN_CLR_5 Registers

4.35.57.1 VIM_INTER_EN_CLR_5 Register (Offset = 4ACh) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description:

Return to Summary Table

Table 4-2750. Instance Table

Instance Name	Physical Address
VIM	50F0 04ACh

Access Types Legend

Table 4-2751. INTER_EN_CLR_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

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4.35.58 MSS_VIM_IRQSTS_5 Registers

4.35.58.1 VIM_IRQSTS_5 Register (Offset = 4B0h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description:

Return to Summary Table

Table 4-2752. Instance Table

Instance Name	Physical Address
VIM	50F0 04B0h

Access Types Legend

Table 4-2753. IRQSTS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

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4.35.59 MSS_VIM_FIQSTS_5 Registers

4.35.59.1 VIM_FIQSTS_5 Register (Offset = 4B4h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description:

Return to Summary Table

Table 4-2754. Instance Table

Instance Name	Physical Address
VIM	50F0 04B4h

Access Types Legend

Table 4-2755. FIQSTS_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

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4.35.60 MSS_VIM_INTMAP_5 Registers

4.35.60.1 VIM_INTMAP_5 Register (Offset = 4B8h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description:

Return to Summary Table

Table 4-2756. Instance Table

Instance Name	Physical Address
VIM	50F0 04B8h

Access Types Legend

Table 4-2757. INTMAP_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

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4.35.61 MSS_VIM_INTTYPE_5 Registers

4.35.61.1 VIM_INTTYPE_5 Register (Offset = 4BCh) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description:

Return to Summary Table

Table 4-2758. Instance Table

Instance Name	Physical Address
VIM	50F0 04BCh

Access Types Legend

Table 4-2759. INTTYPE_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

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4.35.62 MSS_VIM_RAW_6 Registers

4.35.62.1 VIM_RAW_6 Register (Offset = 4C0h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description:

Return to Summary Table

Table 4-2760. Instance Table

Instance Name	Physical Address
VIM	50F0 04C0h

Access Types Legend

Table 4-2761. RAW_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

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4.35.63 MSS_VIM_STS_6 Registers

4.35.63.1 VIM_STS_6 Register (Offset = 4C4h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description:

Return to Summary Table

Table 4-2762. Instance Table

Instance Name	Physical Address
VIM	50F0 04C4h

Access Types Legend

Table 4-2763. STS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

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4.35.64 MSS_VIM_INTR_EN_SET_6 Registers

4.35.64.1 VIM_INTR_EN_SET_6 Register (Offset = 4C8h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description:

Return to Summary Table

Table 4-2764. Instance Table

Instance Name	Physical Address
VIM	50F0 04C8h

Access Types Legend

Table 4-2765. INTR_EN_SET_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

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4.35.65 MSS_VIM_INTER_EN_CLR_6 Registers

4.35.65.1 VIM_INTER_EN_CLR_6 Register (Offset = 4CCh) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description:

Return to Summary Table

Table 4-2766. Instance Table

Instance Name	Physical Address
VIM	50F0 04CCh

Access Types Legend

Table 4-2767. INTER_EN_CLR_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

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4.35.66 MSS_VIM_IRQSTS_6 Registers

4.35.66.1 VIM_IRQSTS_6 Register (Offset = 4D0h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description:

Return to Summary Table

Table 4-2768. Instance Table

Instance Name	Physical Address
VIM	50F0 04D0h

Access Types Legend

Table 4-2769. IRQSTS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

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4.35.67 MSS_VIM_FIQSTS_6 Registers

4.35.67.1 VIM_FIQSTS_6 Register (Offset = 4D4h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description:

Return to Summary Table

Table 4-2770. Instance Table

Instance Name	Physical Address
VIM	50F0 04D4h

Access Types Legend

Table 4-2771. FIQSTS_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

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4.35.68 MSS_VIM_INTMAP_6 Registers

4.35.68.1 VIM_INTMAP_6 Register (Offset = 4D8h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description:

Return to Summary Table

Table 4-2772. Instance Table

Instance Name	Physical Address
VIM	50F0 04D8h

Access Types Legend

Table 4-2773. INTMAP_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

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4.35.69 MSS_VIM_INTTYPE_6 Registers

4.35.69.1 VIM_INTTYPE_6 Register (Offset = 4DCh) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description:

Return to Summary Table

Table 4-2774. Instance Table

Instance Name	Physical Address
VIM	50F0 04DCh

Access Types Legend

Table 4-2775. INTTYPE_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

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4.35.70 MSS_VIM_RAW_7 Registers

4.35.70.1 VIM_RAW_7 Register (Offset = 4E0h) [reset = h]

Short Description: Group M Interrupt Raw Status/Set Register (M is 0 to 7) h400 + M x h20 + h00

Long Description:

Return to Summary Table

Table 4-2776. Instance Table

Instance Name	Physical Address
VIM	50F0 04E0h

Access Types Legend

Table 4-2777. RAW_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RW	0h	This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 InactiveRead 1 Active/ PendingWrite 0 No effectWrite 1 Set to Interrupt Raw Status

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4.35.71 MSS_VIM_STS_7 Registers

4.35.71.1 VIM_STS_7 Register (Offset = 4E4h) [reset = h]

Short Description: Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h04

Long Description:

Return to Summary Table

Table 4-2778. Instance Table

Instance Name	Physical Address
VIM	50F0 04E4h

Access Types Legend

Table 4-2779. STS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit Read 0 Inactive or DisabledRead 1 Active/Pending and EnabledWrite 0 No effectWrite 1 Clear Interrupt Raw Status

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4.35.72 MSS_VIM_INTR_EN_SET_7 Registers

4.35.72.1 VIM_INTR_EN_SET_7 Register (Offset = 4E8h) [reset = h]

Short Description: Group M Interrupt Enabled Set Register (M is 0 to 7) h400 + M x h20 + h08

Long Description:

Return to Summary Table

Table 4-2780. Instance Table

Instance Name	Physical Address
VIM	50F0 04E8h

Access Types Legend

Table 4-2781. INTR_EN_SET_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Set Enable

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4.35.73 MSS_VIM_INTER_EN_CLR_7 Registers

4.35.73.1 VIM_INTER_EN_CLR_7 Register (Offset = 4ECh) [reset = h]

Short Description: Group M Interrupt Enabled Clear Register (M is 0 to 7) h400 + M x h20 + h0C

Long Description:

Return to Summary Table

Table 4-2782. Instance Table

Instance Name	Physical Address
VIM	50F0 04ECh

Access Types Legend

Table 4-2783. INTER_EN_CLR_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+BitRead 0 DisabledRead 1 EnabledWrite 0 No effectWrite 1 Clear Enable

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4.35.74 MSS_VIM_IRQSTS_7 Registers

4.35.74.1 VIM_IRQSTS_7 Register (Offset = 4F0h) [reset = h]

Short Description: Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h10

Long Description:

Return to Summary Table

Table 4-2784. Instance Table

Instance Name	Physical Address
VIM	50F0 04F0h

Access Types Legend

Table 4-2785. IRQSTS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an IRQRead 1 Active/Pending, Enabled, and IRQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if IRQ)

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4.35.75 MSS_VIM_FIQSTS_7 Registers

4.35.75.1 VIM_FIQSTS_7 Register (Offset = 4F4h) [reset = h]

Short Description: Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) h400 + M x h20 + h14

Long Description:

Return to Summary Table

Table 4-2786. Instance Table

Instance Name	Physical Address
VIM	50F0 04F4h

Access Types Legend

Table 4-2787. FIQSTS_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+BitRead 0 Inactive, Disabled, or not an FIQRead 1 Active/Pending, Enabled, and FIQWrite 0 No effectWrite 1 Clear Interrupt Raw Status (if FIQ)

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4.35.76 MSS_VIM_INTMAP_7 Registers

4.35.76.1 VIM_INTMAP_7 Register (Offset = 4F8h) [reset = h]

Short Description: Group M Interrupt Map Register (M is 0 to 7) h400 + M x h20 + h18

Long Description:

Return to Summary Table

Table 4-2788. Instance Table

Instance Name	Physical Address
VIM	50F0 04F8h

Access Types Legend

Table 4-2789. INTMAP_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	MASK	RW	0h	This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group M. Each bit corresponds to event Q where Q = Mx32+Bit 0 IRQ Interrupt (default)1 FIQ Interrupt

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4.35.77 MSS_VIM_INTTYPE_7 Registers

4.35.77.1 VIM_INTTYPE_7 Register (Offset = 4FCh) [reset = h]

Short Description: Group M Type Map Register (M is 0 to 7) h400 + M x h20 + 0x1C

Long Description:

Return to Summary Table

Table 4-2790. Instance Table

Instance Name	Physical Address
VIM	50F0 04FCh

Access Types Legend

Table 4-2791. INTTYPE_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	VAL	RW	0h	This field is used to indicate whether the source of an interrupt is a level (default) or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event (see 3.4 Interrupt Handling). The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit0 Level (default)1 Pulse

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4.35.78 MSS_VIM_INTPRIORITY Registers

4.35.78.1 VIM_INTPRIORITY Register (Offset = 1000h) [reset = h]

Short Description: Interrupt Q Priority Register (Q is 0 to 255 , Q= M+1 x 32)

Long Description:

N = h1000 + Q x h4

Return to Summary Table

Table 4-2792. Instance Table

Instance Name	Physical Address
VIM	50F0 **N**h

Access Types Legend

Table 4-2793. INTPRIORITY Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 4	RES19	RO	0h	RESERVE FIELD
3 - 0	PRI	RW	457h	This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration 0 Highest Priority 15 Lowest Priority (Default)

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4.35.79 MSS_VIM_INTVECTOR_Q Registers

4.35.79.1 VIM_INTVECTOR_Q Register (Offset = 2000h) [reset = h]

Short Description: Interrupt Q Vector Register (Q is 0 to 255 , Q= M+1 x 32)

Long Description:

N = h2000 + Q x h4

Return to Summary Table

Table 4-2794. Instance Table

Instance Name	Physical Address
VIM	50F0 **N**h

Access Types Legend

Table 4-2795. INTVECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	ADDR	RW	0h	This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address (Base Address + 0x18) or FIQ Vector Address (Base Address + 0x1C) and the VECADDR pin when interrupt Q is the active interrupt.Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed.Reads to this register will stall the MMR interface until the read is able to be completed at the RAM.
1 - 0	RES20	RO	0h	Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.

4.35.80 Access Table

Table 4-2796. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

4.36 SOC_TSXBAR_INTR Registers

Table 4-2797. SOC_TSXBAR_INTR Registers Base Address Table

Offset	Length	Acronym	SOC_TSXBAR_INTR Physical Address
0h	32	SOC_TSXBAR_INTR_PID	52E0 4000h
4h	16	SOC_TSXBAR_INTR_MUXCNTL	52E0 4004h

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4.36.1 SOC_TSXBAR_INTR_PID Registers

4.36.1.1 SOC_TSXBAR_INTR_PID Register (Offset = 0h) [reset = h]

Short Description: Identification register

Long Description:

Return to Summary Table

Table 4-2798. Instance Table

Instance Name	Physical Address
SOC_TIMESYNC_XBAR1	52E0 4000h

Access Types Legend

Table 4-2799. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	scheme
29 - 28	BU	RO	2h	bu
27 - 16	FUNCTION	RO	694h	function
15 - 11	RTLVER	RO	10h	rtl version
10 - 8	MAJREV	RO	1h	major version
7 - 6	CUSTOM	RO	0h	custom id
5 - 0	MINREV	RO	0h	minor version

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4.36.2 SOC_TSXBAR_INTR_MUXCNTL Registers

4.36.2.1 SOC_TSXBAR_INTR_MUXCNTL Register (Offset = 4h) [reset = h]

Short Description: Interrupt mux control register

Long Description:

Return to Summary Table

Table 4-2800. Instance Table

Instance Name	Physical Address
SOC_TIMESYNC_XBAR1	52E0 4004h

Access Types Legend

Table 4-2801. MUXCNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
16	INT_ENABLE	RW	0h	interrupt output enable for interrupt N
	RESERVED	NONE		Reserved
3 - 0	ENABLE	RW	0h	Mux control for interrupt N

4.36.3 Access Table

Table 4-2802. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write

4.37 TOP_ESM Registers

Table 4-2803. TOP_ESM Registers Base Address Table

Offset	Length	Acronym	TOP_ESM Physical Address
0h	32	TOP_ESM_PID	52D0 0000h
4h	32	TOP_ESM_INFO	52D0 0004h
8h	8	TOP_ESM_EN	52D0 0008h
Ch	8	TOP_ESM_SFT_RST	52D0 000Ch
10h	8	TOP_ESM_ERR_RAW	52D0 0010h
14h	8	TOP_ESM_ERR_STS	52D0 0014h
18h	8	TOP_ESM_ERR_EN_SET	52D0 0018h
1Ch	8	TOP_ESM_ERR_EN_CLR	52D0 001Ch
20h	32	TOP_ESM_LOW_PRI	52D0 0020h
24h	32	TOP_ESM_HI_PRI	52D0 0024h
28h	32	TOP_ESM_LOW	52D0 0028h
2Ch	32	TOP_ESM_HI	52D0 002Ch
30h	16	TOP_ESM_EOI	52D0 0030h
40h	8	TOP_ESM_PIN_CTRL	52D0 0040h
44h	0	TOP_ESM_PIN_STS	52D0 0044h
48h	24	TOP_ESM_PIN_CNTR	52D0 0048h
4Ch	24	TOP_ESM_PIN_CNTR_PRE	52D0 004Ch
50h	24	TOP_ESM_PWMH_PIN_CNTR	52D0 0050h
54h	24	TOP_ESM_PWMH_PIN_CNTR_PRE	52D0 0054h
58h	24	TOP_ESM_PWML_PIN_CNTR	52D0 0058h

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Table 4-2803. TOP_ESM Registers Base Address Table (continued)

Offset	Length	Acronym	TOP_ESM Physical Address
5Ch	24	TOP_ESM_PWML_PIN_CNTR_PRE	52D0 005Ch

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4.37.1 TOP_ESM_PID Registers

4.37.1.1 TOP_ESM_PID Register (Offset = 0h) [reset = h]

Short Description: The Revision Register contains the major and minor revisions for the module.

Long Description:

Return to Summary Table

Table 4-2804. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0000h

Access Types Legend

Table 4-2805. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID register scheme
29 - 28	BU	RO	2h	Business Unit: 10 = Processors
27 - 16	FUNC	RO	FE0h	Module ID
15 - 11	RTL	RO	9h	RTL revision. Will vary depending on release.
10 - 8	MAJOR	RO	1h	Major revision
7 - 6	CUSTOM	RO	0h	Custom
5 - 0	MINOR	RO	0h	Minor revision

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4.37.2 TOP_ESM_INFO Registers

4.37.2.1 TOP_ESM_INFO Register (Offset = 4h) [reset = h]

Short Description: The Info Register gives the configuration Inforrmation of this ESM.

Long Description:

Return to Summary Table

Table 4-2806. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0004h

Access Types Legend

Table 4-2807. INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LAST_RESET	RO	0h	Indicates the Source of the last Reset
	RESERVED	NONE		Reserved
15 - 8	PULSE_GROUPS	RO	1h	Number of Pulse Error Groups
7 - 0	GROUPS	RO	Bh	Total number of Error Groups

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4.37.3 TOP_ESM_EN Registers

4.37.3.1 TOP_ESM_EN Register (Offset = 8h) [reset = h]

Short Description: The Global Enable Register has the master interrupt mask

Long Description:

Return to Summary Table

Table 4-2808. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0008h

Access Types Legend

Table 4-2809. EN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	KEY	RW	0h	Global Enable

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4.37.4 TOP_ESM_SFT_RST Registers

4.37.4.1 TOP_ESM_SFT_RST Register (Offset = Ch) [reset = h]

Short Description: The Global Soft Reset Register controls the global clear for raw status and enables

Long Description:

Return to Summary Table

Table 4-2810. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 000Ch

Access Types Legend

Table 4-2811. SFT_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3 - 0	KEY	WO	0h	Global Soft Reset

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4.37.5 TOP_ESM_ERR_RAW Registers

4.37.5.1 TOP_ESM_ERR_RAW Register (Offset = 10h) [reset = h]

Short Description: Raw Status/Set Register for Configuration Errors

Long Description:

Return to Summary Table

Table 4-2812. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0010h

Access Types Legend

Table 4-2813. ERR_RAW Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	STS	RW	0h	This is the raw status for config errors

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4.37.6 TOP_ESM_ERR_STS Registers

4.37.6.1 TOP_ESM_ERR_STS Register (Offset = 14h) [reset = h]

Short Description: Config Error Enable and Clear Register

Long Description:

Return to Summary Table

Table 4-2814. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0014h

Access Types Legend

Table 4-2815. ERR_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	MSK	RW	0h	This is the masked status/clear for config errors

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4.37.7 TOP_ESM_ERR_EN_SET Registers

4.37.7.1 TOP_ESM_ERR_EN_SET Register (Offset = 18h) [reset = h]

Short Description: Config Error Enable Set Register

Long Description:

Return to Summary Table

Table 4-2816. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0018h

Access Types Legend

Table 4-2817. ERR_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	MSK	RW	0h	This is the mask enable set for config errors

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4.37.8 TOP_ESM_ERR_EN_CLR Registers

4.37.8.1 TOP_ESM_ERR_EN_CLR Register (Offset = 1Ch) [reset = h]

Short Description: Config Error Interrupt Enabled Clear register

Long Description:

Return to Summary Table

Table 4-2818. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 001Ch

Access Types Legend

Table 4-2819. ERR_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	MSK	RW	0h	This is the mask enable clear for config errors

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4.37.9 TOP_ESM_LOW_PRI Registers

4.37.9.1 TOP_ESM_LOW_PRI Register (Offset = 20h) [reset = h]

Short Description: Shows which is the highest priority outstanding low priority interrupt

Long Description:

Return to Summary Table

Table 4-2820. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0020h

Access Types Legend

Table 4-2821. LOW_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PLS	RO	FFFFh	This is the highest priority outstanding low priority pulse interrupt
15 - 0	LVL	RO	FFFFh	This is the highest priority outstanding low priority level interrupt

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4.37.10 TOP_ESM_HI_PRI Registers

4.37.10.1 TOP_ESM_HI_PRI Register (Offset = 24h) [reset = h]

Short Description: Shows which is the highest priority outstanding high priority interrupt

Long Description:

Return to Summary Table

Table 4-2822. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0024h

Access Types Legend

Table 4-2823. HI_PRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	PLS	RO	FFFFh	This is the highest priority outstanding high priority pulse interrupt
15 - 0	LVL	RO	FFFFh	This is the highest priority outstanding high priority level interrupt

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4.37.11 TOP_ESM_LOW Registers

4.37.11.1 TOP_ESM_LOW Register (Offset = 28h) [reset = h]

Short Description: Shows which groups have oustanding low priority interrupts

Long Description:

Return to Summary Table

Table 4-2824. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0028h

Access Types Legend

Table 4-2825. LOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RO	0h	This is the raw status for config errors

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4.37.12 TOP_ESM_HI Registers

4.37.12.1 TOP_ESM_HI Register (Offset = 2Ch) [reset = h]

Short Description: Shows which groups have oustanding high priority interrupts

Long Description:

Return to Summary Table

Table 4-2826. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 002Ch

Access Types Legend

Table 4-2827. HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	STS	RO	0h	This is the raw status for config errors

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4.37.13 TOP_ESM_EOI Registers

4.37.13.1 TOP_ESM_EOI Register (Offset = 30h) [reset = h]

Short Description: End of Interrupt Register

Long Description:

Return to Summary Table

Table 4-2828. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0030h

Access Types Legend

Table 4-2829. EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
10 - 0	KEY	WO	0h	This is the interrupt being serviced

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4.37.14 TOP_ESM_PIN_CTRL Registers

4.37.14.1 TOP_ESM_PIN_CTRL Register (Offset = 40h) [reset = h]

Short Description: This register controls the error_pin_n output

Long Description:

Return to Summary Table

Table 4-2830. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0040h

Access Types Legend

Table 4-2831. PIN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 4	PWM_EN	RW	0h	PWM enable
3 - 0	KEY	RW	0h	Pin Control Key

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4.37.15 TOP_ESM_PIN_STS Registers

4.37.15.1 TOP_ESM_PIN_STS Register (Offset = 44h) [reset = h]

Short Description: This register reflects the status of the error_pin_n output

Long Description:

Return to Summary Table

Table 4-2832. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0044h

Access Types Legend

Table 4-2833. PIN_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
0	VAL	RO	0h	Value of the error_pin_n

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4.37.16 TOP_ESM_PIN_CNTR Registers

4.37.16.1 TOP_ESM_PIN_CNTR Register (Offset = 48h) [reset = h]

Short Description: This register shows the current value of the error pin counter

Long Description:

Return to Summary Table

Table 4-2834. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0048h

Access Types Legend

Table 4-2835. PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RO	0h	Current Counter Value

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4.37.17 TOP_ESM_PIN_CNTR_PRE Registers

4.37.17.1 TOP_ESM_PIN_CNTR_PRE Register (Offset = 4Ch) [reset = h]

Short Description: This register contains the value that is loaded in to the Error Counter

Long Description:

Return to Summary Table

Table 4-2836. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 004Ch

Access Types Legend

Table 4-2837. PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RW	0h	Counter Pre-Load Value

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4.37.18 TOP_ESM_PWMH_PIN_CNTR Registers

4.37.18.1 TOP_ESM_PWMH_PIN_CNTR Register (Offset = 50h) [reset = h]

Short Description: This register shows the current value of the error pin PWM high counter

Long Description:

Return to Summary Table

Table 4-2838. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0050h

Access Types Legend

Table 4-2839. PWMH_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RO	0h	Current Counter Value

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4.37.19 TOP_ESM_PWMH_PIN_CNTR_PRE Registers

4.37.19.1 TOP_ESM_PWMH_PIN_CNTR_PRE Register (Offset = 54h) [reset = h]

Short Description: This register contains the value that is loaded in to the Error PWM High Counter

Long Description:

Return to Summary Table

Table 4-2840. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0054h

Access Types Legend

Table 4-2841. PWMH_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RW	0h	Counter Pre-Load Value

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4.37.20 TOP_ESM_PWML_PIN_CNTR Registers

4.37.20.1 TOP_ESM_PWML_PIN_CNTR Register (Offset = 58h) [reset = h]

Short Description: This register shows the current value of the error pin PWM low counter

Long Description:

Return to Summary Table

Table 4-2842. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 0058h

Access Types Legend

Table 4-2843. PWML_PIN_CNTR Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RO	0h	Current Counter Value

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4.37.21 TOP_ESM_PWML_PIN_CNTR_PRE Registers

4.37.21.1 TOP_ESM_PWML_PIN_CNTR_PRE Register (Offset = 5Ch) [reset = h]

Short Description: This register contains the value that is loaded in to the Error PWM Low Counter

Long Description:

Return to Summary Table

Table 4-2844. Instance Table

Instance Name	Physical Address
TOP_ESM	52D0 005Ch

Access Types Legend

Table 4-2845. PWML_PIN_CNTR_PRE Register Field Descriptions

Bit	Field	Type	Reset	Description
23 - 0	COUNT	RW	0h	Counter Pre-Load Value

4.37.22 Access Table

Table 4-2846. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
WO	WO	Write

4.38 TPCC Registers

Table 4-2847. TPCC0 Registers Base Address Table

Offset	Length	Acronym	TPCC0 Physical Address
0h	32	TPCC_PID	4702 0000h
4h	32	TPCC_CCCFG	4702 0004h
200h	32	TPCC_QCHMAPN	4702 0200h
240h	32	TPCC_DMAQNUMN	4702 0240h
260h	32	TPCC_QDMAQNUM	4702 0260h
280h	32	TPCC_QUETCMAP	4702 0280h
284h	32	TPCC_QUEPRI	4702 0284h
300h	32	TPCC_EMR	4702 0300h
304h	32	TPCC_EMRH	4702 0304h
308h	32	TPCC_EMCR	4702 0308h
30Ch	32	TPCC_EMCRH	4702 030Ch
310h	32	TPCC_QEMR	4702 0310h
314h	32	TPCC_QEMCR	4702 0314h
318h	32	TPCC_CCERR	4702 0318h
31Ch	32	TPCC_CCERRCLR	4702 031Ch
320h	32	TPCC_EEVAL	4702 0320h
340h	32	TPCC_DRAEM	4702 0340h
344h	32	TPCC_DRAEHM	4702 0344h
380h	32	TPCC_QRAEN	4702 0380h
400h	32	TPCC_QNE0	4702 0400h
404h	32	TPCC_QNE1	4702 0404h

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Table 4-2847. TPCC0 Registers Base Address Table (continued)

Offset	Length	Acronym	TPCC0 Physical Address
408h	32	TPCC_QNE2	4702 0408h
40Ch	32	TPCC_QNE3	4702 040Ch
410h	32	TPCC_QNE4	4702 0410h
414h	32	TPCC_QNE5	4702 0414h
418h	32	TPCC_QNE6	4702 0418h
41Ch	32	TPCC_QNE7	4702 041Ch
420h	32	TPCC_QNE8	4702 0420h
424h	32	TPCC_QNE9	4702 0424h
428h	32	TPCC_QNE10	4702 0428h
42Ch	32	TPCC_QNE11	4702 042Ch
430h	32	TPCC_QNE12	4702 0430h
434h	32	TPCC_QNE13	4702 0434h
438h	32	TPCC_QNE14	4702 0438h
43Ch	32	TPCC_QNE15	4702 043Ch
600h	32	TPCC_QSTATN	4702 0600h
620h	32	TPCC_QWMTHRA	4702 0620h
640h	32	TPCC_CCSTAT	4702 0640h
700h	32	TPCC_AETCTL	4702 0700h
704h	32	TPCC_AETSTAT	4702 0704h
708h	32	TPCC_AETCMD	4702 0708h
1000h	32	TPCC_ER	4702 1000h
1004h	32	TPCC_ERH	4702 1004h
1008h	32	TPCC_ECR	4702 1008h
100Ch	32	TPCC_ECRH	4702 100Ch
1010h	32	TPCC_ESR	4702 1010h
1014h	32	TPCC_ESRH	4702 1014h
1018h	32	TPCC_CER	4702 1018h
101Ch	32	TPCC_CERH	4702 101Ch
1020h	32	TPCC_EER	4702 1020h
1024h	32	TPCC_EERH	4702 1024h
1028h	32	TPCC_EECR	4702 1028h
102Ch	32	TPCC_EECRH	4702 102Ch
1030h	32	TPCC_EESR	4702 1030h
1034h	32	TPCC_EESRH	4702 1034h
1038h	32	TPCC_SER	4702 1038h
103Ch	32	TPCC_SERH	4702 103Ch
1040h	32	TPCC_SECR	4702 1040h
1044h	32	TPCC_SECRH	4702 1044h
1050h	32	TPCC_IER	4702 1050h
1054h	32	TPCC_IERH	4702 1054h
1058h	32	TPCC_IECR	4702 1058h
105Ch	32	TPCC_IECRH	4702 105Ch
1060h	32	TPCC_IESR	4702 1060h
1064h	32	TPCC_IESRH	4702 1064h
1068h	32	TPCC_IPR	4702 1068h
106Ch	32	TPCC_IPRH	4702 106Ch
1070h	32	TPCC_ICR	4702 1070h

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Table 4-2847. TPCC0 Registers Base Address Table (continued)

Offset	Length	Acronym	TPCC0 Physical Address
1074h	32	TPCC_ICRH	4702 1074h
1078h	32	TPCC_IEVAL	4702 1078h
1080h	32	TPCC_QER	4702 1080h
1084h	32	TPCC_QEER	4702 1084h
1088h	32	TPCC_QEECR	4702 1088h
108Ch	32	TPCC_QEESR	4702 108Ch
1090h	32	TPCC_QSER	4702 1090h
1094h	32	TPCC_QSECR	4702 1094h
2000h	32	TPCC_ER_RN	4702 2000h
2004h	32	TPCC_ERH_RN	4702 2004h
2008h	32	TPCC_ECR_RN	4702 2008h
200Ch	32	TPCC_ECRH_RN	4702 200Ch
2010h	32	TPCC_ESR_RN	4702 2010h
2014h	32	TPCC_ESRH_RN	4702 2014h
2018h	32	TPCC_CER_RN	4702 2018h
201Ch	32	TPCC_CERH_RN	4702 201Ch
2020h	32	TPCC_EER_RN	4702 2020h
2024h	32	TPCC_EERH_RN	4702 2024h
2028h	32	TPCC_EECR_RN	4702 2028h
202Ch	32	TPCC_EECRH_RN	4702 202Ch
2030h	32	TPCC_EESR_RN	4702 2030h
2034h	32	TPCC_EESRH_RN	4702 2034h
2038h	32	TPCC_SER_RN	4702 2038h
203Ch	32	TPCC_SERH_RN	4702 203Ch
2040h	32	TPCC_SECR_RN	4702 2040h
2044h	32	TPCC_SECRH_RN	4702 2044h
2050h	32	TPCC_IER_RN	4702 2050h
2054h	32	TPCC_IERH_RN	4702 2054h
2058h	32	TPCC_IECR_RN	4702 2058h
205Ch	32	TPCC_IECRH_RN	4702 205Ch
2060h	32	TPCC_IESR_RN	4702 2060h
2064h	32	TPCC_IESRH_RN	4702 2064h
2068h	32	TPCC_IPR_RN	4702 2068h
206Ch	32	TPCC_IPRH_RN	4702 206Ch
2070h	32	TPCC_ICR_RN	4702 2070h
2074h	32	TPCC_ICRH_RN	4702 2074h
2078h	32	TPCC_IEVAL_RN	4702 2078h
2080h	32	TPCC_QER_RN	4702 2080h
2084h	32	TPCC_QEER_RN	4702 2084h
2088h	32	TPCC_QEECR_RN	4702 2088h
208Ch	32	TPCC_QEESR_RN	4702 208Ch
2090h	32	TPCC_QSER_RN	4702 2090h
2094h	32	TPCC_QSECR_RN	4702 2094h
4000h	32	TPCC_OPT	4702 4000h
4004h	32	TPCC_SRC	4702 4004h
4008h	32	TPCC_ABCNT	4702 4008h
400Ch	32	TPCC_DST	4702 400Ch

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Table 4-2847. TPCC0 Registers Base Address Table (continued)

Offset	Length	Acronym	TPCC0 Physical Address
4010h	32	TPCC_BIDX	4702 4010h
4014h	32	TPCC_LNK	4702 4014h
4018h	32	TPCC_CIDX	4702 4018h
401Ch	32	TPCC_CCNT	4702 401Ch

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4.38.1 TPCC0_PID Registers

4.38.1.1 TPCC0_PID Register (Offset = 0h) [reset = h]

Short Description: Peripheral ID Register

Long Description:

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Table 4-2848. Instance Table

Instance Name	Physical Address
TPCC0	4702 0000h

Access Types Legend

Table 4-2849. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID Scheme: Used to distinguish between old ID scheme and current. Spare bit to encode future schemes EDMA uses 'new scheme' indicated with value of 0x1.
29 - 28	RES1	RO	0h	RESERVE FIELD
27 - 16	FUNC	RO	1h	Function indicates a software compatible module family.
15 - 11	RTL	RO	2775h	RTL Version
10 - 8	MAJOR	RO	Bh	Major Revision
7 - 6	CUSTOM	RO	0h	Custom revision field: Not used on this version of EDMA.
5 - 0	MINOR	RO	0h	Minor Revision

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4.38.2 TPCC0_CCCFG Registers

4.38.2.1 TPCC0_CCCFG Register (Offset = 4h) [reset = h]

Short Description: CC Configuration Register

Long Description:

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Table 4-2850. Instance Table

Instance Name	Physical Address
TPCC0	4702 0004h

Access Types Legend

Table 4-2851. CCCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 26	RES2	RO	0h	RESERVE FIELD
25	MPEXIST	RO	0h	Memory Protection Existence MPEXIST = 0 : No memory protection. MPEXIST = 1 : Memory Protection logic included.
24	CHMAPEXIST	RO	0h	Channel Mapping Existence CHMAPEXIST = 0 : No Channel mapping. CHMAPEXIST = 1 : Channel mapping logic included.
23 - 22	RES3	RO	0h	RESERVE FIELD
21 - 20	NUMREGN	RO	2h	Number of MP and Shadow regions
19	RES4	RO	0h	RESERVE FIELD
18 - 16	NUMTC	RO	1h	Number of Queues/Number of TCs
15	RES5	RO	0h	RESERVE FIELD
14 - 12	NUMPAENTRY	RO	Bh	Number of PaRAM entries
11	RES6	RO	0h	RESERVE FIELD
10 - 8	NUMINTCH	RO	4h	Number of Interrupt Channels
7	RES7	RO	0h	RESERVE FIELD
6 - 4	NUMQDMACH	RO	4h	Number of QDMA Channels
3	RES8	RO	0h	RESERVE FIELD
2 - 0	NUMDMACH	RO	5h	Number of DMA Channels

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4.38.3 TPCC0_QCHMAPN Registers

4.38.3.1 TPCC0_QCHMAPN Register (Offset = 200h) [reset = h]

Short Description: QDMA Channel N Mapping Register

Long Description:

Return to Summary Table

Table 4-2852. Instance Table

Instance Name	Physical Address
TPCC0	4702 0200h

Access Types Legend

Table 4-2853. QCHMAPN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 14	RES10	RO	0h	RESERVE FIELD
13 - 5	PAENTRY	RW	0h	PaRAM Entry number for QDMA Channel N.
4 - 2	TRWORD	RW	0h	TRWORD points to the specific trigger word of the PaRAM Entry defined by PAENTRY. A write to the trigger word results in a QDMA Event being recognized.
	RESERVED	NONE		Reserved

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4.38.4 TPCC0_DMAQNUMN Registers

4.38.4.1 TPCC0_DMAQNUMN Register (Offset = 240h) [reset = h]

Short Description: DMA Queue Number Register n Contains the Event queue number to be used for the corresponding DMA Channel.

Long Description:

Return to Summary Table

Table 4-2854. Instance Table

Instance Name	Physical Address
TPCC0	4702 0240h

Access Types Legend

Table 4-2855. DMAQNUMN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES11	RO	0h	RESERVE FIELD
30 - 28	E7	RW	0h	DMA Queue Number for event #7
27	RES12	RO	0h	RESERVE FIELD
26 - 24	E6	RW	0h	DMA Queue Number for event #6
23	RES13	RO	0h	RESERVE FIELD
22 - 20	E5	RW	0h	DMA Queue Number for event #5
19	RES14	RO	0h	RESERVE FIELD
18 - 16	E4	RW	0h	DMA Queue Number for event #4
15	RES15	RO	0h	RESERVE FIELD
14 - 12	E3	RW	0h	DMA Queue Number for event #3
11	RES16	RO	0h	RESERVE FIELD
10 - 8	E2	RW	0h	DMA Queue Number for event #2
7	RES17	RO	0h	RESERVE FIELD
6 - 4	E1	RW	0h	DMA Queue Number for event #1
3	RES18	RO	0h	RESERVE FIELD
2 - 0	E0	RW	0h	DMA Queue Number for event #0

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4.38.5 TPCC0_QDMAQNUM Registers

4.38.5.1 TPCC0_QDMAQNUM Register (Offset = 260h) [reset = h]

Short Description: QDMA Queue Number Register Contains the Event queue number to be used for the corresponding QDMA Channel.

Long Description:

Return to Summary Table

Table 4-2856. Instance Table

Instance Name	Physical Address
TPCC0	4702 0260h

Access Types Legend

Table 4-2857. QDMAQNUM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RES19	RO	0h	RESERVE FIELD
30 - 28	E7	RW	0h	QDMA Queue Number for event #7
27	RES20	RO	0h	RESERVE FIELD
26 - 24	E6	RW	0h	QDMA Queue Number for event #6
23	RES21	RO	0h	RESERVE FIELD
22 - 20	E5	RW	0h	QDMA Queue Number for event #5
19	RES22	RO	0h	RESERVE FIELD
18 - 16	E4	RW	0h	QDMA Queue Number for event #4
15	RES23	RO	0h	RESERVE FIELD
14 - 12	E3	RW	0h	QDMA Queue Number for event #3
11	RES24	RO	0h	RESERVE FIELD
10 - 8	E2	RW	0h	QDMA Queue Number for event #2
7	RES25	RO	0h	RESERVE FIELD
6 - 4	E1	RW	0h	QDMA Queue Number for event #1
3	RES26	RO	0h	RESERVE FIELD
2 - 0	E0	RW	0h	QDMA Queue Number for event #0

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4.38.6 TPCC0_QUETCMAP Registers

4.38.6.1 TPCC0_QUETCMAP Register (Offset = 280h) [reset = h]

Short Description: Queue to TC Mapping

Long Description:

Return to Summary Table

Table 4-2858. Instance Table

Instance Name	Physical Address
TPCC0	4702 0280h

Access Types Legend

Table 4-2859. QUETCMAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RES27	RO	0h	RESERVE FIELD
6 - 4	TCNUMQ1	RW	1h	TC Number for Queue N: Defines the TC number that Event Queue N TRs are written to.
3	RES28	RO	0h	RESERVE FIELD
2 - 0	TCNUMQ0	RW	0h	TC Number for Queue N: Defines the TC number that Event Queue N TRs are written to.

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4.38.7 TPCC0_QUEPRI Registers

4.38.7.1 TPCC0_QUEPRI Register (Offset = 284h) [reset = h]

Short Description: Queue Priority

Long Description:

Return to Summary Table

Table 4-2860. Instance Table

Instance Name	Physical Address
TPCC0	4702 0284h

Access Types Legend

Table 4-2861. QUEPRI Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 7	RES29	RO	0h	RESERVE FIELD
6 - 4	PRIQ1	RW	0h	Priority Level for Queue 1 Dictates the priority level used for the OPTIONS field programmation for Qn TRs. Sets the priority used for TC read and write commands.
3	RES30	RO	0h	RESERVE FIELD
2 - 0	PRIQ0	RW	0h	Priority Level for Queue 0 Dictates the priority level used for the OPTIONS field programmation for Qn TRs. Sets the priority used for TC read and write commands.

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4.38.8 TPCC0_EMR Registers

4.38.8.1 TPCC0_EMR Register (Offset = 300h) [reset = h]

Short Description: Event Missed Register: The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

Long Description:

Return to Summary Table

Table 4-2862. Instance Table

Instance Name	Physical Address
TPCC0	4702 0300h

Access Types Legend

Table 4-2863. EMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event Missed #31
30	E30	RO	0h	Event Missed #30
29	E29	RO	0h	Event Missed #29
28	E28	RO	0h	Event Missed #28
27	E27	RO	0h	Event Missed #27
26	E26	RO	0h	Event Missed #26
25	E25	RO	0h	Event Missed #25
24	E24	RO	0h	Event Missed #24
23	E23	RO	0h	Event Missed #23
22	E22	RO	0h	Event Missed #22
21	E21	RO	0h	Event Missed #21
20	E20	RO	0h	Event Missed #20
19	E19	RO	0h	Event Missed #19
18	E18	RO	0h	Event Missed #18
17	E17	RO	0h	Event Missed #17
16	E16	RO	0h	Event Missed #16
15	E15	RO	0h	Event Missed #15
14	E14	RO	0h	Event Missed #14
13	E13	RO	0h	Event Missed #13
12	E12	RO	0h	Event Missed #12
11	E11	RO	0h	Event Missed #11
10	E10	RO	0h	Event Missed #10
9	E9	RO	0h	Event Missed #9
8	E8	RO	0h	Event Missed #8
7	E7	RO	0h	Event Missed #7
6	E6	RO	0h	Event Missed #6
5	E5	RO	0h	Event Missed #5
4	E4	RO	0h	Event Missed #4
3	E3	RO	0h	Event Missed #3
2	E2	RO	0h	Event Missed #2
1	E1	RO	0h	Event Missed #1

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Table 4-2863. EMR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	E0	RO	0h	Event Missed #0

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4.38.9 TPCC0_EMRH Registers

4.38.9.1 TPCC0_EMRH Register (Offset = 304h) [reset = h]

Short Description: Event Missed Register (High Part): The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/ CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

Long Description:

Return to Summary Table

Table 4-2864. Instance Table

Instance Name	Physical Address
TPCC0	4702 0304h

Access Types Legend

Table 4-2865. EMRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event Missed #63
30	E62	RO	0h	Event Missed #62
29	E61	RO	0h	Event Missed #61
28	E60	RO	0h	Event Missed #60
27	E59	RO	0h	Event Missed #59
26	E58	RO	0h	Event Missed #58
25	E57	RO	0h	Event Missed #57
24	E56	RO	0h	Event Missed #56
23	E55	RO	0h	Event Missed #55
22	E54	RO	0h	Event Missed #54
21	E53	RO	0h	Event Missed #53
20	E52	RO	0h	Event Missed #52
19	E51	RO	0h	Event Missed #51
18	E50	RO	0h	Event Missed #50
17	E49	RO	0h	Event Missed #49
16	E48	RO	0h	Event Missed #48
15	E47	RO	0h	Event Missed #47
14	E46	RO	0h	Event Missed #46
13	E45	RO	0h	Event Missed #45
12	E44	RO	0h	Event Missed #44
11	E43	RO	0h	Event Missed #43
10	E42	RO	0h	Event Missed #42
9	E41	RO	0h	Event Missed #41
8	E40	RO	0h	Event Missed #40
7	E39	RO	0h	Event Missed #39
6	E38	RO	0h	Event Missed #38
5	E37	RO	0h	Event Missed #37
4	E36	RO	0h	Event Missed #36
3	E35	RO	0h	Event Missed #35
2	E34	RO	0h	Event Missed #34
1	E33	RO	0h	Event Missed #33

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Table 4-2865. EMRH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	E32	RO	0h	Event Missed #32

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4.38.10 TPCC0_EMCR Registers

4.38.10.1 TPCC0_EMCR Register (Offset = 308h) [reset = h]

Short Description: Event Missed Clear Register: CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-2866. Instance Table

Instance Name	Physical Address
TPCC0	4702 0308h

Access Types Legend

Table 4-2867. EMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event Missed Clear #31
30	E30	WO	0h	Event Missed Clear #30
29	E29	WO	0h	Event Missed Clear #29
28	E28	WO	0h	Event Missed Clear #28
27	E27	WO	0h	Event Missed Clear #27
26	E26	WO	0h	Event Missed Clear #26
25	E25	WO	0h	Event Missed Clear #25
24	E24	WO	0h	Event Missed Clear #24
23	E23	WO	0h	Event Missed Clear #23
22	E22	WO	0h	Event Missed Clear #22
21	E21	WO	0h	Event Missed Clear #21
20	E20	WO	0h	Event Missed Clear #20
19	E19	WO	0h	Event Missed Clear #19
18	E18	WO	0h	Event Missed Clear #18
17	E17	WO	0h	Event Missed Clear #17
16	E16	WO	0h	Event Missed Clear #16
15	E15	WO	0h	Event Missed Clear #15
14	E14	WO	0h	Event Missed Clear #14
13	E13	WO	0h	Event Missed Clear #13
12	E12	WO	0h	Event Missed Clear #12
11	E11	WO	0h	Event Missed Clear #11
10	E10	WO	0h	Event Missed Clear #10
9	E9	WO	0h	Event Missed Clear #9
8	E8	WO	0h	Event Missed Clear #8
7	E7	WO	0h	Event Missed Clear #7
6	E6	WO	0h	Event Missed Clear #6
5	E5	WO	0h	Event Missed Clear #5
4	E4	WO	0h	Event Missed Clear #4
3	E3	WO	0h	Event Missed Clear #3
2	E2	WO	0h	Event Missed Clear #2
1	E1	WO	0h	Event Missed Clear #1
0	E0	WO	0h	Event Missed Clear #0

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4.38.11 TPCC0_EMCRH Registers

4.38.11.1 TPCC0_EMCRH Register (Offset = 30Ch) [reset = h]

Short Description: Event Missed Clear Register (High Part): CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-2868. Instance Table

Instance Name	Physical Address
TPCC0	4702 030Ch

Access Types Legend

Table 4-2869. EMCRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event Missed Clear #63
30	E62	WO	0h	Event Missed Clear #62
29	E61	WO	0h	Event Missed Clear #61
28	E60	WO	0h	Event Missed Clear #60
27	E59	WO	0h	Event Missed Clear #59
26	E58	WO	0h	Event Missed Clear #58
25	E57	WO	0h	Event Missed Clear #57
24	E56	WO	0h	Event Missed Clear #56
23	E55	WO	0h	Event Missed Clear #55
22	E54	WO	0h	Event Missed Clear #54
21	E53	WO	0h	Event Missed Clear #53
20	E52	WO	0h	Event Missed Clear #52
19	E51	WO	0h	Event Missed Clear #51
18	E50	WO	0h	Event Missed Clear #50
17	E49	WO	0h	Event Missed Clear #49
16	E48	WO	0h	Event Missed Clear #48
15	E47	WO	0h	Event Missed Clear #47
14	E46	WO	0h	Event Missed Clear #46
13	E45	WO	0h	Event Missed Clear #45
12	E44	WO	0h	Event Missed Clear #44
11	E43	WO	0h	Event Missed Clear #43
10	E42	WO	0h	Event Missed Clear #42
9	E41	WO	0h	Event Missed Clear #41
8	E40	WO	0h	Event Missed Clear #40
7	E39	WO	0h	Event Missed Clear #39
6	E38	WO	0h	Event Missed Clear #38
5	E37	WO	0h	Event Missed Clear #37
4	E36	WO	0h	Event Missed Clear #36
3	E35	WO	0h	Event Missed Clear #35
2	E34	WO	0h	Event Missed Clear #34
1	E33	WO	0h	Event Missed Clear #33
0	E32	WO	0h	Event Missed Clear #32

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4.38.12 TPCC0_QEMR Registers

4.38.12.1 TPCC0_QEMR Register (Offset = 310h) [reset = h]

Short Description: QDMA Event Missed Register: The QDMA Event Missed register is set if 2 QDMA events are detected without the first event being cleared or if a Null TR is serviced.. If any bit in the QEMR register is set (and all errors (including EMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

Long Description:

Return to Summary Table

Table 4-2870. Instance Table

Instance Name	Physical Address
TPCC0	4702 0310h

Access Types Legend

Table 4-2871. QEMR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES31	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event Missed #7
6	E6	RO	0h	Event Missed #6
5	E5	RO	0h	Event Missed #5
4	E4	RO	0h	Event Missed #4
3	E3	RO	0h	Event Missed #3
2	E2	RO	0h	Event Missed #2
1	E1	RO	0h	Event Missed #1
0	E0	RO	0h	Event Missed #0

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4.38.13 TPCC0_QEMCR Registers

4.38.13.1 TPCC0_QEMCR Register (Offset = 314h) [reset = h]

Short Description: QDMA Event Missed Clear Register: CPU write of '1' to the QEMCR.En bit causes the QEMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-2872. Instance Table

Instance Name	Physical Address
TPCC0	4702 0314h

Access Types Legend

Table 4-2873. QEMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES32	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event Missed Clear #7
6	E6	WO	0h	Event Missed Clear #6
5	E5	WO	0h	Event Missed Clear #5
4	E4	WO	0h	Event Missed Clear #4
3	E3	WO	0h	Event Missed Clear #3
2	E2	WO	0h	Event Missed Clear #2
1	E1	WO	0h	Event Missed Clear #1
0	E0	WO	0h	Event Missed Clear #0

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4.38.14 TPCC0_CCERR Registers

4.38.14.1 TPCC0_CCERR Register (Offset = 318h) [reset = h]

Short Description: CC Error Register

Long Description:

Return to Summary Table

Table 4-2874. Instance Table

Instance Name	Physical Address
TPCC0	4702 0318h

Access Types Legend

Table 4-2875. CCERR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RES33	RO	0h	RESERVE FIELD
16	TCERR	RO	0h	Transfer Completion Code Error: TCCERR = 0 : Total number of allowed TCCs outstanding has not been reached. TCCERR = 1 : Total number of allowed TCCs has been reached. TCCERR can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors were previously clear) then an error will be signaled with TPCC error interrupt.
15 - 8	RES34	RO	0h	RESERVE FIELD
7	QTHRXCD7	RO	0h	Queue Threshold Error for Q7: QTHRXCD7 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD7 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD7 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
6	QTHRXCD6	RO	0h	Queue Threshold Error for Q6: QTHRXCD6 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD6 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD6 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
5	QTHRXCD5	RO	0h	Queue Threshold Error for Q5: QTHRXCD5 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD5 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD5 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
4	QTHRXCD4	RO	0h	Queue Threshold Error for Q4: QTHRXCD4 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD4 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD4 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
3	QTHRXCD3	RO	0h	Queue Threshold Error for Q3: QTHRXCD3 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD3 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD3 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.

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Table 4-2875. CCERR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	QTHRXCD2	RO	0h	Queue Threshold Error for Q2: QTHRXCD2 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD2 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD2 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
1	QTHRXCD1	RO	0h	Queue Threshold Error for Q1: QTHRXCD1 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD1 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD1 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.
0	QTHRXCD0	RO	0h	Queue Threshold Error for Q0: QTHRXCD0 = 0 : Watermark/ threshold has not been exceeded. QTHRXCD0 = 1 : Watermark/ threshold has been exceeded. CCERR.QTHRXCD0 can be cleared by writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set (and all errors (including EMR/QEMR) were previously clear) then an error will be signaled with the TPCC error interrupt.

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4.38.15 TPCC0_CCERRCLR Registers

4.38.15.1 TPCC0_CCERRCLR Register (Offset = 31Ch) [reset = h]

Short Description: CC Error Clear Register

Long Description:

Return to Summary Table

Table 4-2876. Instance Table

Instance Name	Physical Address
TPCC0	4702 031Ch

Access Types Legend

Table 4-2877. CCERRCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 17	RES35	RO	0h	RESERVE FIELD
16	TCERR	WO	0h	Clear Error for CCERR.TCERR: Write of '1' clears the value of CCERR bit N. Writes of '0' have no affect.
15 - 8	RES36	RO	0h	RESERVE FIELD
7	QTHRXCD7	WO	0h	Clear error for CCERR.QTHRXCD7: Write of '1' clears the values of QSTAT7.WM QSTAT7.THRXCD CCERR.QTHRXCD7 Writes of '0' have no affect.
6	QTHRXCD6	WO	0h	Clear error for CCERR.QTHRXCD6: Write of '1' clears the values of QSTAT6.WM QSTAT6.THRXCD CCERR.QTHRXCD6 Writes of '0' have no affect.
5	QTHRXCD5	WO	0h	Clear error for CCERR.QTHRXCD5: Write of '1' clears the values of QSTAT5.WM QSTAT5.THRXCD CCERR.QTHRXCD5 Writes of '0' have no affect.
4	QTHRXCD4	WO	0h	Clear error for CCERR.QTHRXCD4: Write of '1' clears the values of QSTAT4.WM QSTAT4.THRXCD CCERR.QTHRXCD4 Writes of '0' have no affect.
3	QTHRXCD3	WO	0h	Clear error for CCERR.QTHRXCD3: Write of '1' clears the values of QSTAT3.WM QSTAT3.THRXCD CCERR.QTHRXCD3 Writes of '0' have no affect.
2	QTHRXCD2	WO	0h	Clear error for CCERR.QTHRXCD2: Write of '1' clears the values of QSTAT2.WM QSTAT2.THRXCD CCERR.QTHRXCD2 Writes of '0' have no affect.
1	QTHRXCD1	WO	0h	Clear error for CCERR.QTHRXCD1: Write of '1' clears the values of QSTAT1.WM QSTAT1.THRXCD CCERR.QTHRXCD1 Writes of '0' have no affect.
0	QTHRXCD0	WO	0h	Clear error for CCERR.QTHRXCD0: Write of '1' clears the values of QSTAT0.WM QSTAT0.THRXCD CCERR.QTHRXCD0 Writes of '0' have no affect.

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4.38.16 TPCC0_EEVAL Registers

4.38.16.1 TPCC0_EEVAL Register (Offset = 320h) [reset = h]

Short Description: Error Eval Register

Long Description:

Return to Summary Table

Table 4-2878. Instance Table

Instance Name	Physical Address
TPCC0	4702 0320h

Access Types Legend

Table 4-2879. EEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RES37	RO	0h	RESERVE FIELD
1	SET	WO	0h	Error Interrupt Set: CPU write of '1' to the SET bit causes the TPCC error interrupt to be pulsed regardless of state of EMR/EMRH QEMR or CCERR. CPU write of '0' has no effect.
0	EVAL	WO	0h	Error Interrupt Evaluate: CPU write of '1' to the EVAL bit causes the TPCC error interrupt to be pulsed if any errors have not been cleared in the EMR/EMRH QEMR or CCERR registers. CPU write of '0' has no effect.

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4.38.17 TPCC0_DRAEM Registers

4.38.17.1 TPCC0_DRAEM Register (Offset = 340h) [reset = h]

Short Description: DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.

Long Description:

Return to Summary Table

Table 4-2880. Instance Table

Instance Name	Physical Address
TPCC0	4702 0340h

Access Types Legend

Table 4-2881. DRAEM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RW	0h	DMA Region Access enable for Region M bit #31
30	E30	RW	0h	DMA Region Access enable for Region M bit #30
29	E29	RW	0h	DMA Region Access enable for Region M bit #29
28	E28	RW	0h	DMA Region Access enable for Region M bit #28
27	E27	RW	0h	DMA Region Access enable for Region M bit #27
26	E26	RW	0h	DMA Region Access enable for Region M bit #26
25	E25	RW	0h	DMA Region Access enable for Region M bit #25
24	E24	RW	0h	DMA Region Access enable for Region M bit #24
23	E23	RW	0h	DMA Region Access enable for Region M bit #23
22	E22	RW	0h	DMA Region Access enable for Region M bit #22
21	E21	RW	0h	DMA Region Access enable for Region M bit #21
20	E20	RW	0h	DMA Region Access enable for Region M bit #20
19	E19	RW	0h	DMA Region Access enable for Region M bit #19
18	E18	RW	0h	DMA Region Access enable for Region M bit #18
17	E17	RW	0h	DMA Region Access enable for Region M bit #17
16	E16	RW	0h	DMA Region Access enable for Region M bit #16
15	E15	RW	0h	DMA Region Access enable for Region M bit #15
14	E14	RW	0h	DMA Region Access enable for Region M bit #14
13	E13	RW	0h	DMA Region Access enable for Region M bit #13
12	E12	RW	0h	DMA Region Access enable for Region M bit #12
11	E11	RW	0h	DMA Region Access enable for Region M bit #11
10	E10	RW	0h	DMA Region Access enable for Region M bit #10
9	E9	RW	0h	DMA Region Access enable for Region M bit #9
8	E8	RW	0h	DMA Region Access enable for Region M bit #8
7	E7	RW	0h	DMA Region Access enable for Region M bit #7
6	E6	RW	0h	DMA Region Access enable for Region M bit #6
5	E5	RW	0h	DMA Region Access enable for Region M bit #5
4	E4	RW	0h	DMA Region Access enable for Region M bit #4
3	E3	RW	0h	DMA Region Access enable for Region M bit #3
2	E2	RW	0h	DMA Region Access enable for Region M bit #2

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Table 4-2881. DRAEM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	E1	RW	0h	DMA Region Access enable for Region M bit #1
0	E0	RW	0h	DMA Region Access enable for Region M bit #0

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4.38.18 TPCC0_DRAEHM Registers

4.38.18.1 TPCC0_DRAEHM Register (Offset = 344h) [reset = h]

Short Description: DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt. En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Readswill return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.

Long Description:

Return to Summary Table

Table 4-2882. Instance Table

Instance Name	Physical Address
TPCC0	4702 0344h

Access Types Legend

Table 4-2883. DRAEHM Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RW	0h	DMA Region Access enable for Region M bit #63
30	E62	RW	0h	DMA Region Access enable for Region M bit #62
29	E61	RW	0h	DMA Region Access enable for Region M bit #61
28	E60	RW	0h	DMA Region Access enable for Region M bit #60
27	E59	RW	0h	DMA Region Access enable for Region M bit #59
26	E58	RW	0h	DMA Region Access enable for Region M bit #58
25	E57	RW	0h	DMA Region Access enable for Region M bit #57
24	E56	RW	0h	DMA Region Access enable for Region M bit #56
23	E55	RW	0h	DMA Region Access enable for Region M bit #55
22	E54	RW	0h	DMA Region Access enable for Region M bit #54
21	E53	RW	0h	DMA Region Access enable for Region M bit #53
20	E52	RW	0h	DMA Region Access enable for Region M bit #52
19	E51	RW	0h	DMA Region Access enable for Region M bit #51
18	E50	RW	0h	DMA Region Access enable for Region M bit #50
17	E49	RW	0h	DMA Region Access enable for Region M bit #49
16	E48	RW	0h	DMA Region Access enable for Region M bit #48
15	E47	RW	0h	DMA Region Access enable for Region M bit #47
14	E46	RW	0h	DMA Region Access enable for Region M bit #46
13	E45	RW	0h	DMA Region Access enable for Region M bit #45
12	E44	RW	0h	DMA Region Access enable for Region M bit #44
11	E43	RW	0h	DMA Region Access enable for Region M bit #43
10	E42	RW	0h	DMA Region Access enable for Region M bit #42
9	E41	RW	0h	DMA Region Access enable for Region M bit #41
8	E40	RW	0h	DMA Region Access enable for Region M bit #40
7	E39	RW	0h	DMA Region Access enable for Region M bit #39

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Table 4-2883. DRAEHM Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	E38	RW	0h	DMA Region Access enable for Region M bit #38
5	E37	RW	0h	DMA Region Access enable for Region M bit #37
4	E36	RW	0h	DMA Region Access enable for Region M bit #36
3	E35	RW	0h	DMA Region Access enable for Region M bit #35
2	E34	RW	0h	DMA Region Access enable for Region M bit #34
1	E33	RW	0h	DMA Region Access enable for Region M bit #33
0	E32	RW	0h	DMA Region Access enable for Region M bit #32

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4.38.19 TPCC0_QRAEN Registers

4.38.19.1 TPCC0_QRAEN Register (Offset = 380h) [reset = h]

Short Description: QDMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any QDMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any QDMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region n interrupt.

Long Description:

Return to Summary Table

Table 4-2884. Instance Table

Instance Name	Physical Address
TPCC0	4702 0380h

Access Types Legend

Table 4-2885. QRAEN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES38	RO	0h	RESERVE FIELD
7	E7	RW	0h	QDMA Region Access enable for Region M bit #7
6	E6	RW	0h	QDMA Region Access enable for Region M bit #6
5	E5	RW	0h	QDMA Region Access enable for Region M bit #5
4	E4	RW	0h	QDMA Region Access enable for Region M bit #4
3	E3	RW	0h	QDMA Region Access enable for Region M bit #3
2	E2	RW	0h	QDMA Region Access enable for Region M bit #2
1	E1	RW	0h	QDMA Region Access enable for Region M bit #1
0	E0	RW	0h	QDMA Region Access enable for Region M bit #0

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4.38.20 TPCC0_QNE0 Registers

4.38.20.1 TPCC0_QNE0 Register (Offset = 400h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 0

Long Description:

Return to Summary Table

Table 4-2886. Instance Table

Instance Name	Physical Address
TPCC0	4702 0400h

Access Types Legend

Table 4-2887. QNE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES39	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

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4.38.21 TPCC0_QNE1 Registers

4.38.21.1 TPCC0_QNE1 Register (Offset = 404h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 1

Long Description:

Return to Summary Table

Table 4-2888. Instance Table

Instance Name	Physical Address
TPCC0	4702 0404h

Access Types Legend

Table 4-2889. QNE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES40	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

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4.38.22 TPCC0_QNE2 Registers

4.38.22.1 TPCC0_QNE2 Register (Offset = 408h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 2

Long Description:

Return to Summary Table

Table 4-2890. Instance Table

Instance Name	Physical Address
TPCC0	4702 0408h

Access Types Legend

Table 4-2891. QNE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES41	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

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4.38.23 TPCC0_QNE3 Registers

4.38.23.1 TPCC0_QNE3 Register (Offset = 40Ch) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 3

Long Description:

Return to Summary Table

Table 4-2892. Instance Table

Instance Name	Physical Address
TPCC0	4702 040Ch

Access Types Legend

Table 4-2893. QNE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES42	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

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4.38.24 TPCC0_QNE4 Registers

4.38.24.1 TPCC0_QNE4 Register (Offset = 410h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 4

Long Description:

Return to Summary Table

Table 4-2894. Instance Table

Instance Name	Physical Address
TPCC0	4702 0410h

Access Types Legend

Table 4-2895. QNE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES43	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

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4.38.25 TPCC0_QNE5 Registers

4.38.25.1 TPCC0_QNE5 Register (Offset = 414h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 5

Long Description:

Return to Summary Table

Table 4-2896. Instance Table

Instance Name	Physical Address
TPCC0	4702 0414h

Access Types Legend

Table 4-2897. QNE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES44	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

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4.38.26 TPCC0_QNE6 Registers

4.38.26.1 TPCC0_QNE6 Register (Offset = 418h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 6

Long Description:

Return to Summary Table

Table 4-2898. Instance Table

Instance Name	Physical Address
TPCC0	4702 0418h

Access Types Legend

Table 4-2899. QNE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES45	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

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4.38.27 TPCC0_QNE7 Registers

4.38.27.1 TPCC0_QNE7 Register (Offset = 41Ch) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 7

Long Description:

Return to Summary Table

Table 4-2900. Instance Table

Instance Name	Physical Address
TPCC0	4702 041Ch

Access Types Legend

Table 4-2901. QNE7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES46	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

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4.38.28 TPCC0_QNE8 Registers

4.38.28.1 TPCC0_QNE8 Register (Offset = 420h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 8

Long Description:

Return to Summary Table

Table 4-2902. Instance Table

Instance Name	Physical Address
TPCC0	4702 0420h

Access Types Legend

Table 4-2903. QNE8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES47	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

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4.38.29 TPCC0_QNE9 Registers

4.38.29.1 TPCC0_QNE9 Register (Offset = 424h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 9

Long Description:

Return to Summary Table

Table 4-2904. Instance Table

Instance Name	Physical Address
TPCC0	4702 0424h

Access Types Legend

Table 4-2905. QNE9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES48	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

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4.38.30 TPCC0_QNE10 Registers

4.38.30.1 TPCC0_QNE10 Register (Offset = 428h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 0

Long Description:

Return to Summary Table

Table 4-2906. Instance Table

Instance Name	Physical Address
TPCC0	4702 0428h

Access Types Legend

Table 4-2907. QNE10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES49	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

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4.38.31 TPCC0_QNE11 Registers

4.38.31.1 TPCC0_QNE11 Register (Offset = 42Ch) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 11

Long Description:

Return to Summary Table

Table 4-2908. Instance Table

Instance Name	Physical Address
TPCC0	4702 042Ch

Access Types Legend

Table 4-2909. QNE11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES50	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

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4.38.32 TPCC0_QNE12 Registers

4.38.32.1 TPCC0_QNE12 Register (Offset = 430h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 12

Long Description:

Return to Summary Table

Table 4-2910. Instance Table

Instance Name	Physical Address
TPCC0	4702 0430h

Access Types Legend

Table 4-2911. QNE12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES51	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

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4.38.33 TPCC0_QNE13 Registers

4.38.33.1 TPCC0_QNE13 Register (Offset = 434h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 13

Long Description:

Return to Summary Table

Table 4-2912. Instance Table

Instance Name	Physical Address
TPCC0	4702 0434h

Access Types Legend

Table 4-2913. QNE13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES52	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

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4.38.34 TPCC0_QNE14 Registers

4.38.34.1 TPCC0_QNE14 Register (Offset = 438h) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 14

Long Description:

Return to Summary Table

Table 4-2914. Instance Table

Instance Name	Physical Address
TPCC0	4702 0438h

Access Types Legend

Table 4-2915. QNE14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES53	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

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4.38.35 TPCC0_QNE15 Registers

4.38.35.1 TPCC0_QNE15 Register (Offset = 43Ch) [reset = h]

Short Description: Event Queue Entry Diagram for Queue n - Entry 15

Long Description:

Return to Summary Table

Table 4-2916. Instance Table

Instance Name	Physical Address
TPCC0	4702 043Ch

Access Types Legend

Table 4-2917. QNE15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES54	RO	0h	RESERVE FIELD
7 - 6	ETYPE	RO	0h	Event Type: Specifies the specific Event Type for the given entry in the Event Queue.
5 - 0	ENUM	RO	0h	Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events (ER/ESR/CER) ENUM will range between 0 and NUM_DMACH (up to 63). For QDMA Channel events (QER) ENUM will range between 0 and NUM_QDMACH (up to 7).

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4.38.36 TPCC0_QSTATN Registers

4.38.36.1 TPCC0_QSTATN Register (Offset = 600h) [reset = h]

Short Description: QSTATn Register Set

Long Description:

Return to Summary Table

Table 4-2918. Instance Table

Instance Name	Physical Address
TPCC0	4702 0600h

Access Types Legend

Table 4-2919. QSTATN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 25	RES55	RO	0h	RESERVE FIELD
24	THRXCD	RO	0h	Threshold Exceeded: THRXCD = 0 : Threshold specified by QWMTHR(A B).Qn has not been exceeded. THRXCD = 1 : Threshold specified by QWMTHR(A B).Qn has been exceeded. QSTATn.THRXCD is cleared via CCERR.WMCLRn bit.
23 - 21	RES56	RO	0h	RESERVE FIELD
20 - 16	WM	RO	0h	Watermark for Maximum Queue Usage: Watermark tracks the most entries that have been in QueueN since reset or since the last time that the watermark (WM) was cleared. QSTATn.WM is cleared via CCERR.WMCLRn bit. Legal values = 0x0 (empty) to 0x10 (full)
15 - 13	RES57	RO	0h	RESERVE FIELD
12 - 8	NUMVAL	RO	0h	Number of Valid Entries in QueueN: Represents the total number of entries residing in the Queue Manager FIFO at a given instant. Always enabled. Legal values = 0x0 (empty) to 0x10 (full)
7 - 4	RES58	RO	0h	RESERVE FIELD
3 - 0	STRTPTR	RO	0h	Start Pointer: Represents the offset to the head entry of QueueN in units of entries. Always enabled. Legal values = 0x0 (0th entry) to 0xF (15th entry)

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4.38.37 TPCC0_QWMTHRA Registers

4.38.37.1 TPCC0_QWMTHRA Register (Offset = 620h) [reset = h]

Short Description: Queue Threshold A for Q[3:0]: CCERR.QTHRXCDn and QSTATn.THRXCD error bit is set when the number of Events in QueueN at an instant in time (visible via QSTATn.NUMVAL) equals or exceeds the value specified by QWMTHRA.Qn. Legal values = 0x0 (ever used?) to 0x10 (ever full?) A value of 0x11 disables threshold errors.

Long Description:

Return to Summary Table

Table 4-2920. Instance Table

Instance Name	Physical Address
TPCC0	4702 0620h

Access Types Legend

Table 4-2921. QWMTHRA Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 13	RES59	RO	0h	RESERVE FIELD
12 - 8	Q1	RW	2710h	Queue Threshold for Q1 value
7 - 5	RES60	RO	0h	RESERVE FIELD
4 - 0	Q0	RW	2710h	Queue Threshold for Q0 value

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4.38.38 TPCC0_CCSTAT Registers

4.38.38.1 TPCC0_CCSTAT Register (Offset = 640h) [reset = h]

Short Description: CC Status Register

Long Description:

Return to Summary Table

Table 4-2922. Instance Table

Instance Name	Physical Address
TPCC0	4702 0640h

Access Types Legend

Table 4-2923. CCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 24	RES61	RO	0h	RESERVE FIELD
23	QUEACTV7	RO	0h	Queue 7 Active QUEACTV7 = 0 : No Evts are queued in Q7. QUEACTV7 = 1 : At least one TR is queued in Q7.
22	QUEACTV6	RO	0h	Queue 6 Active QUEACTV6 = 0 : No Evts are queued in Q6. QUEACTV6 = 1 : At least one TR is queued in Q6.
21	QUEACTV5	RO	0h	Queue 5 Active QUEACTV5 = 0 : No Evts are queued in Q5. QUEACTV5 = 1 : At least one TR is queued in Q5.
20	QUEACTV4	RO	0h	Queue 4 Active QUEACTV4 = 0 : No Evts are queued in Q4. QUEACTV4 = 1 : At least one TR is queued in Q4.
19	QUEACTV3	RO	0h	Queue 3 Active QUEACTV3 = 0 : No Evts are queued in Q3. QUEACTV3 = 1 : At least one TR is queued in Q3.
18	QUEACTV2	RO	0h	Queue 2 Active QUEACTV2 = 0 : No Evts are queued in Q2. QUEACTV2 = 1 : At least one TR is queued in Q2.
17	QUEACTV1	RO	0h	Queue 1 Active QUEACTV1 = 0 : No Evts are queued in Q1. QUEACTV1 = 1 : At least one TR is queued in Q1.
16	QUEACTV0	RO	0h	Queue 0 Active QUEACTV0 = 0 : No Evts are queued in Q0. QUEACTV0 = 1 : At least one TR is queued in Q0.
15 - 14	RES62	RO	0h	RESERVE FIELD
13 - 8	COMPACTV	RO	0h	Completion Request Active: Counter that tracks the total number of completion requests submitted to the TC. The counter increments when a TR is submitted with TCINTEN or TCCHEN set to '1'. The counter decrements for every valid completion code received from any of the external TCs. The CC will not service new TRs if COMPACTV count is already at the limit. COMPACTV = 0 : No completion requests outstanding. COMPACTV = 1: Total of '1' completion request outstanding. ... COMPACTV = 63 : Total of 63 completion requests are outstanding. No additional TRs will be submitted until count is less than 63.
7 - 5	RES63	RO	0h	RESERVE FIELD
4	ACTV	RO	0h	Channel Controller Active: Channel Controller Active is a logical-OR of each of the ACTV signals. The ACTV bit must remain high through the life of a TR. ACTV = 0 : Channel is idle. ACTV = 1 : Channel is busy.
3	RES64	RO	0h	RESERVE FIELD
2	TRACTV	RO	0h	Transfer Request Active: TRACTV = 0 : Transfer Request processing/submission logic is inactive. TRACTV = 1 : Transfer Request processing/submission logic is active.
1	QEVTACTV	RO	0h	QDMA Event Active: QEVTACTV = 0 : No enabled QDMA Events are active within the CC. QEVTACTV = 1 : At least one enabled DMA Event (ER & EER ESR CER) is active within the CC.

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Table 4-2923. CCSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EVTACTV	RO	0h	DMA Event Active: EVTACTV = 0 : No enabled DMA Events are active within the CC. EVTACTV = 1 : At least one enabled DMA Event (ER & EER ESR CER) is active within the CC.

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4.38.39 TPCC0_AETCTL Registers

4.38.39.1 TPCC0_AETCTL Register (Offset = 700h) [reset = h]

Short Description: Advanced Event Trigger Control

Long Description:

Return to Summary Table

Table 4-2924. Instance Table

Instance Name	Physical Address
TPCC0	4702 0700h

Access Types Legend

Table 4-2925. AETCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	RW	0h	AET Enable: EN = 0 : AET event generation is disabled. EN = 1 : AET event generation is enabled.
30 - 14	RES65	RO	0h	RESERVE FIELD
13 - 8	ENDINT	RW	0h	AET End Interrupt: Dictates the completion interrupt number that will force the tpcc_aet signal to be deasserted (low)
7	RES66	RO	0h	RESERVE FIELD
6	TYPE	RW	0h	AET Event Type: TYPE = 0 : Event specified by STARTEVT applies to DMA Events (set by ER ESR or CER) TYPE = 1 : Event specified by STARTEVT applies to QDMA Events
5 - 0	STRTEVT	RW	0h	AET Start Event: Dictates the Event Number that will force the tpcc_aet signal to be asserted (high)

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4.38.40 TPCC0_AETSTAT Registers

4.38.40.1 TPCC0_AETSTAT Register (Offset = 704h) [reset = h]

Short Description: Advanced Event Trigger Stat

Long Description:

Return to Summary Table

Table 4-2926. Instance Table

Instance Name	Physical Address
TPCC0	4702 0704h

Access Types Legend

Table 4-2927. AETSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	RES67	RO	0h	RESERVE FIELD
0	STAT	RO	0h	AET Status: AETSTAT = 0 : tpcc_aet is currently low. AETSTAT = 1 : tpcc_aet is currently high.

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4.38.41 TPCC0_AETCMD Registers

4.38.41.1 TPCC0_AETCMD Register (Offset = 708h) [reset = h]

Short Description: AET Command

Long Description:

Return to Summary Table

Table 4-2928. Instance Table

Instance Name	Physical Address
TPCC0	4702 0708h

Access Types Legend

Table 4-2929. AETCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 1	RES68	RO	0h	RESERVE FIELD
0	CLR	WO	0h	AET Clear command: CPU write of '1' to the CLR bit causes the tpcc_aet output signal and AETSTAT.STAT register to be cleared. CPU write of '0' has no effect..

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4.38.42 TPCC0_ER Registers

4.38.42.1 TPCC0_ER Register (Offset = 1000h) [reset = h]

Short Description: Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.

Long Description:

Return to Summary Table

Table 4-2930. Instance Table

Instance Name	Physical Address
TPCC0	4702 1000h

Access Types Legend

Table 4-2931. ER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3

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Table 4-2931. ER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

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4.38.43 TPCC0_ERH Registers

4.38.43.1 TPCC0_ERH Register (Offset = 1004h) [reset = h]

Short Description: Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.

Long Description:

Return to Summary Table

Table 4-2932. Instance Table

Instance Name	Physical Address
TPCC0	4702 1004h

Access Types Legend

Table 4-2933. ERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35

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Table 4-2933. ERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

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4.38.44 TPCC0_ECR Registers

4.38.44.1 TPCC0_ECR Register (Offset = 1008h) [reset = h]

Short Description: Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-2934. Instance Table

Instance Name	Physical Address
TPCC0	4702 1008h

Access Types Legend

Table 4-2935. ECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

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4.38.45 TPCC0_ECRH Registers

4.38.45.1 TPCC0_ECRH Register (Offset = 100Ch) [reset = h]

Short Description: Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-2936. Instance Table

Instance Name	Physical Address
TPCC0	4702 100Ch

Access Types Legend

Table 4-2937. ECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

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4.38.46 TPCC0_ESR Registers

4.38.46.1 TPCC0_ESR Register (Offset = 1010h) [reset = h]

Short Description: Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-2938. Instance Table

Instance Name	Physical Address
TPCC0	4702 1010h

Access Types Legend

Table 4-2939. ESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

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4.38.47 TPCC0_ESRH Registers

4.38.47.1 TPCC0_ESRH Register (Offset = 1014h) [reset = h]

Short Description: Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-2940. Instance Table

Instance Name	Physical Address
TPCC0	4702 1014h

Access Types Legend

Table 4-2941. ESRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

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4.38.48 TPCC0_CER Registers

4.38.48.1 TPCC0_CER Register (Offset = 1018h) [reset = h]

Short Description: Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.

Long Description:

Return to Summary Table

Table 4-2942. Instance Table

Instance Name	Physical Address
TPCC0	4702 1018h

Access Types Legend

Table 4-2943. CER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3

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Table 4-2943. CER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

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4.38.49 TPCC0_CERH Registers

4.38.49.1 TPCC0_CERH Register (Offset = 101Ch) [reset = h]

Short Description: Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.

Long Description:

Return to Summary Table

Table 4-2944. Instance Table

Instance Name	Physical Address
TPCC0	4702 101Ch

Access Types Legend

Table 4-2945. CERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35

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Table 4-2945. CERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

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4.38.50 TPCC0_EER Registers

4.38.50.1 TPCC0_EER Register (Offset = 1020h) [reset = h]

Short Description: Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.

Long Description:

Return to Summary Table

Table 4-2946. Instance Table

Instance Name	Physical Address
TPCC0	4702 1020h

Access Types Legend

Table 4-2947. EER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3

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Table 4-2947. EER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

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4.38.51 TPCC0_EERH Registers

4.38.51.1 TPCC0_EERH Register (Offset = 1024h) [reset = h]

Short Description: Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.

Long Description:

Return to Summary Table

Table 4-2948. Instance Table

Instance Name	Physical Address
TPCC0	4702 1024h

Access Types Legend

Table 4-2949. EERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35

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Table 4-2949. EERH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

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4.38.52 TPCC0_EECR Registers

4.38.52.1 TPCC0_EECR Register (Offset = 1028h) [reset = h]

Short Description: Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-2950. Instance Table

Instance Name	Physical Address
TPCC0	4702 1028h

Access Types Legend

Table 4-2951. EECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

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4.38.53 TPCC0_EECRH Registers

4.38.53.1 TPCC0_EECRH Register (Offset = 102Ch) [reset = h]

Short Description: Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-2952. Instance Table

Instance Name	Physical Address
TPCC0	4702 102Ch

Access Types Legend

Table 4-2953. EECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

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4.38.54 TPCC0_EESR Registers

4.38.54.1 TPCC0_EESR Register (Offset = 1030h) [reset = h]

Short Description: Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-2954. Instance Table

Instance Name	Physical Address
TPCC0	4702 1030h

Access Types Legend

Table 4-2955. EESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

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4.38.55 TPCC0_EESRH Registers

4.38.55.1 TPCC0_EESRH Register (Offset = 1034h) [reset = h]

Short Description: Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-2956. Instance Table

Instance Name	Physical Address
TPCC0	4702 1034h

Access Types Legend

Table 4-2957. EESRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

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4.38.56 TPCC0_SER Registers

4.38.56.1 TPCC0_SER Register (Offset = 1038h) [reset = h]

Short Description: Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

Return to Summary Table

Table 4-2958. Instance Table

Instance Name	Physical Address
TPCC0	4702 1038h

Access Types Legend

Table 4-2959. SER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

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4.38.57 TPCC0_SERH Registers

4.38.57.1 TPCC0_SERH Register (Offset = 103Ch) [reset = h]

Short Description: Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

Return to Summary Table

Table 4-2960. Instance Table

Instance Name	Physical Address
TPCC0	4702 103Ch

Access Types Legend

Table 4-2961. SERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

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4.38.58 TPCC0_SECR Registers

4.38.58.1 TPCC0_SECR Register (Offset = 1040h) [reset = h]

Short Description: Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-2962. Instance Table

Instance Name	Physical Address
TPCC0	4702 1040h

Access Types Legend

Table 4-2963. SECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

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4.38.59 TPCC0_SECRH Registers

4.38.59.1 TPCC0_SECRH Register (Offset = 1044h) [reset = h]

Short Description: Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-2964. Instance Table

Instance Name	Physical Address
TPCC0	4702 1044h

Access Types Legend

Table 4-2965. SECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

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4.38.60 TPCC0_IER Registers

4.38.60.1 TPCC0_IER Register (Offset = 1050h) [reset = h]

Short Description: Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.

Long Description:

Return to Summary Table

Table 4-2966. Instance Table

Instance Name	Physical Address
TPCC0	4702 1050h

Access Types Legend

Table 4-2967. IER Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	RO	0h	Interrupt associated with TCC #31
30	I30	RO	0h	Interrupt associated with TCC #30
29	I29	RO	0h	Interrupt associated with TCC #29
28	I28	RO	0h	Interrupt associated with TCC #28
27	I27	RO	0h	Interrupt associated with TCC #27
26	I26	RO	0h	Interrupt associated with TCC #26
25	I25	RO	0h	Interrupt associated with TCC #25
24	I24	RO	0h	Interrupt associated with TCC #24
23	I23	RO	0h	Interrupt associated with TCC #23
22	I22	RO	0h	Interrupt associated with TCC #22
21	I21	RO	0h	Interrupt associated with TCC #21
20	I20	RO	0h	Interrupt associated with TCC #20
19	I19	RO	0h	Interrupt associated with TCC #19
18	I18	RO	0h	Interrupt associated with TCC #18
17	I17	RO	0h	Interrupt associated with TCC #17
16	I16	RO	0h	Interrupt associated with TCC #16
15	I15	RO	0h	Interrupt associated with TCC #15
14	I14	RO	0h	Interrupt associated with TCC #14
13	I13	RO	0h	Interrupt associated with TCC #13
12	I12	RO	0h	Interrupt associated with TCC #12
11	I11	RO	0h	Interrupt associated with TCC #11
10	I10	RO	0h	Interrupt associated with TCC #10
9	I9	RO	0h	Interrupt associated with TCC #9
8	I8	RO	0h	Interrupt associated with TCC #8
7	I7	RO	0h	Interrupt associated with TCC #7
6	I6	RO	0h	Interrupt associated with TCC #6
5	I5	RO	0h	Interrupt associated with TCC #5
4	I4	RO	0h	Interrupt associated with TCC #4
3	I3	RO	0h	Interrupt associated with TCC #3
2	I2	RO	0h	Interrupt associated with TCC #2
1	I1	RO	0h	Interrupt associated with TCC #1
0	I0	RO	0h	Interrupt associated with TCC #0

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4.38.61 TPCC0_IERH Registers

4.38.61.1 TPCC0_IERH Register (Offset = 1054h) [reset = h]

Short Description: Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.

Long Description:

Return to Summary Table

Table 4-2968. Instance Table

Instance Name	Physical Address
TPCC0	4702 1054h

Access Types Legend

Table 4-2969. IERH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	RO	0h	Interrupt associated with TCC #63
30	I62	RO	0h	Interrupt associated with TCC #62
29	I61	RO	0h	Interrupt associated with TCC #61
28	I60	RO	0h	Interrupt associated with TCC #60
27	I59	RO	0h	Interrupt associated with TCC #59
26	I58	RO	0h	Interrupt associated with TCC #58
25	I57	RO	0h	Interrupt associated with TCC #57
24	I56	RO	0h	Interrupt associated with TCC #56
23	I55	RO	0h	Interrupt associated with TCC #55
22	I54	RO	0h	Interrupt associated with TCC #54
21	I53	RO	0h	Interrupt associated with TCC #53
20	I52	RO	0h	Interrupt associated with TCC #52
19	I51	RO	0h	Interrupt associated with TCC #51
18	I50	RO	0h	Interrupt associated with TCC #50
17	I49	RO	0h	Interrupt associated with TCC #49
16	I48	RO	0h	Interrupt associated with TCC #48
15	I47	RO	0h	Interrupt associated with TCC #47
14	I46	RO	0h	Interrupt associated with TCC #46
13	I45	RO	0h	Interrupt associated with TCC #45
12	I44	RO	0h	Interrupt associated with TCC #44
11	I43	RO	0h	Interrupt associated with TCC #43
10	I42	RO	0h	Interrupt associated with TCC #42
9	I41	RO	0h	Interrupt associated with TCC #41
8	I40	RO	0h	Interrupt associated with TCC #40
7	I39	RO	0h	Interrupt associated with TCC #39
6	I38	RO	0h	Interrupt associated with TCC #38
5	I37	RO	0h	Interrupt associated with TCC #37
4	I36	RO	0h	Interrupt associated with TCC #36
3	I35	RO	0h	Interrupt associated with TCC #35
2	I34	RO	0h	Interrupt associated with TCC #34
1	I33	RO	0h	Interrupt associated with TCC #33
0	I32	RO	0h	Interrupt associated with TCC #32

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4.38.62 TPCC0_IECR Registers

4.38.62.1 TPCC0_IECR Register (Offset = 1058h) [reset = h]

Short Description: Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-2970. Instance Table

Instance Name	Physical Address
TPCC0	4702 1058h

Access Types Legend

Table 4-2971. IECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

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4.38.63 TPCC0_IECRH Registers

4.38.63.1 TPCC0_IECRH Register (Offset = 105Ch) [reset = h]

Short Description: Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-2972. Instance Table

Instance Name	Physical Address
TPCC0	4702 105Ch

Access Types Legend

Table 4-2973. IECRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39
6	I38	WO	0h	Interrupt associated with TCC #38
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

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4.38.64 TPCC0_IESR Registers

4.38.64.1 TPCC0_IESR Register (Offset = 1060h) [reset = h]

Short Description: Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-2974. Instance Table

Instance Name	Physical Address
TPCC0	4702 1060h

Access Types Legend

Table 4-2975. IESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

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4.38.65 TPCC0_IESRH Registers

4.38.65.1 TPCC0_IESRH Register (Offset = 1064h) [reset = h]

Short Description: Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-2976. Instance Table

Instance Name	Physical Address
TPCC0	4702 1064h

Access Types Legend

Table 4-2977. IESRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39
6	I38	WO	0h	Interrupt associated with TCC #38
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

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4.38.66 TPCC0_IPR Registers

4.38.66.1 TPCC0_IPR Register (Offset = 1068h) [reset = h]

Short Description: Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.

Long Description:

Return to Summary Table

Table 4-2978. Instance Table

Instance Name	Physical Address
TPCC0	4702 1068h

Access Types Legend

Table 4-2979. IPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	RO	0h	Interrupt associated with TCC #31
30	I30	RO	0h	Interrupt associated with TCC #30
29	I29	RO	0h	Interrupt associated with TCC #29
28	I28	RO	0h	Interrupt associated with TCC #28
27	I27	RO	0h	Interrupt associated with TCC #27
26	I26	RO	0h	Interrupt associated with TCC #26
25	I25	RO	0h	Interrupt associated with TCC #25
24	I24	RO	0h	Interrupt associated with TCC #24
23	I23	RO	0h	Interrupt associated with TCC #23
22	I22	RO	0h	Interrupt associated with TCC #22
21	I21	RO	0h	Interrupt associated with TCC #21
20	I20	RO	0h	Interrupt associated with TCC #20
19	I19	RO	0h	Interrupt associated with TCC #19
18	I18	RO	0h	Interrupt associated with TCC #18
17	I17	RO	0h	Interrupt associated with TCC #17
16	I16	RO	0h	Interrupt associated with TCC #16
15	I15	RO	0h	Interrupt associated with TCC #15
14	I14	RO	0h	Interrupt associated with TCC #14
13	I13	RO	0h	Interrupt associated with TCC #13
12	I12	RO	0h	Interrupt associated with TCC #12
11	I11	RO	0h	Interrupt associated with TCC #11
10	I10	RO	0h	Interrupt associated with TCC #10
9	I9	RO	0h	Interrupt associated with TCC #9
8	I8	RO	0h	Interrupt associated with TCC #8
7	I7	RO	0h	Interrupt associated with TCC #7
6	I6	RO	0h	Interrupt associated with TCC #6
5	I5	RO	0h	Interrupt associated with TCC #5
4	I4	RO	0h	Interrupt associated with TCC #4
3	I3	RO	0h	Interrupt associated with TCC #3
2	I2	RO	0h	Interrupt associated with TCC #2
1	I1	RO	0h	Interrupt associated with TCC #1
0	I0	RO	0h	Interrupt associated with TCC #0

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4.38.67 TPCC0_IPRH Registers

4.38.67.1 TPCC0_IPRH Register (Offset = 106Ch) [reset = h]

Short Description: Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.

Long Description:

Return to Summary Table

Table 4-2980. Instance Table

Instance Name	Physical Address
TPCC0	4702 106Ch

Access Types Legend

Table 4-2981. IPRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	RO	0h	Interrupt associated with TCC #63
30	I62	RO	0h	Interrupt associated with TCC #62
29	I61	RO	0h	Interrupt associated with TCC #61
28	I60	RO	0h	Interrupt associated with TCC #60
27	I59	RO	0h	Interrupt associated with TCC #59
26	I58	RO	0h	Interrupt associated with TCC #58
25	I57	RO	0h	Interrupt associated with TCC #57
24	I56	RO	0h	Interrupt associated with TCC #56
23	I55	RO	0h	Interrupt associated with TCC #55
22	I54	RO	0h	Interrupt associated with TCC #54
21	I53	RO	0h	Interrupt associated with TCC #53
20	I52	RO	0h	Interrupt associated with TCC #52
19	I51	RO	0h	Interrupt associated with TCC #51
18	I50	RO	0h	Interrupt associated with TCC #50
17	I49	RO	0h	Interrupt associated with TCC #49
16	I48	RO	0h	Interrupt associated with TCC #48
15	I47	RO	0h	Interrupt associated with TCC #47
14	I46	RO	0h	Interrupt associated with TCC #46
13	I45	RO	0h	Interrupt associated with TCC #45
12	I44	RO	0h	Interrupt associated with TCC #44
11	I43	RO	0h	Interrupt associated with TCC #43
10	I42	RO	0h	Interrupt associated with TCC #42
9	I41	RO	0h	Interrupt associated with TCC #41
8	I40	RO	0h	Interrupt associated with TCC #40
7	I39	RO	0h	Interrupt associated with TCC #39
6	I38	RO	0h	Interrupt associated with TCC #38
5	I37	RO	0h	Interrupt associated with TCC #37
4	I36	RO	0h	Interrupt associated with TCC #36
3	I35	RO	0h	Interrupt associated with TCC #35
2	I34	RO	0h	Interrupt associated with TCC #34
1	I33	RO	0h	Interrupt associated with TCC #33
0	I32	RO	0h	Interrupt associated with TCC #32

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4.38.68 TPCC0_ICR Registers

4.38.68.1 TPCC0_ICR Register (Offset = 1070h) [reset = h]

Short Description: Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-2982. Instance Table

Instance Name	Physical Address
TPCC0	4702 1070h

Access Types Legend

Table 4-2983. ICR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

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4.38.69 TPCC0_ICRH Registers

4.38.69.1 TPCC0_ICRH Register (Offset = 1074h) [reset = h]

Short Description: Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-2984. Instance Table

Instance Name	Physical Address
TPCC0	4702 1074h

Access Types Legend

Table 4-2985. ICRH Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39
6	I38	WO	0h	Interrupt associated with TCC #38
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

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4.38.70 TPCC0_IEVAL Registers

4.38.70.1 TPCC0_IEVAL Register (Offset = 1078h) [reset = h]

Short Description: Interrupt Eval Register

Long Description:

Return to Summary Table

Table 4-2986. Instance Table

Instance Name	Physical Address
TPCC0	4702 1078h

Access Types Legend

Table 4-2987. IEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RES69	RO	0h	RESERVE FIELD
1	SET	WO	0h	Interrupt Set: CPU write of '1' to the SETn bit causes the tpcc_intN output signal to be pulsed egardless of state of interrupts enable (IERn) and status (IPRn). CPU write of '0' has no effect.
0	EVAL	WO	0h	Interrupt Evaluate: CPU write of '1' to the EVALn bit causes the tpcc_intN output signal to be pulsed if any enabled interrupts (IERn) are still pending (IPRn). CPU write of '0' has no effect..

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4.38.71 TPCC0_QER Registers

4.38.71.1 TPCC0_QER Register (Offset = 1080h) [reset = h]

Short Description: QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.

Long Description:

Return to Summary Table

Table 4-2988. Instance Table

Instance Name	Physical Address
TPCC0	4702 1080h

Access Types Legend

Table 4-2989. QER Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES70	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

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4.38.72 TPCC0_QEER Registers

4.38.72.1 TPCC0_QEER Register (Offset = 1084h) [reset = h]

Short Description: QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/latched in QER.En.

Long Description:

Return to Summary Table

Table 4-2990. Instance Table

Instance Name	Physical Address
TPCC0	4702 1084h

Access Types Legend

Table 4-2991. QEER Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES71	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

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4.38.73 TPCC0_QEECR Registers

4.38.73.1 TPCC0_QEECR Register (Offset = 1088h) [reset = h]

Short Description: QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-2992. Instance Table

Instance Name	Physical Address
TPCC0	4702 1088h

Access Types Legend

Table 4-2993. QEECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES72	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

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4.38.74 TPCC0_QEESR Registers

4.38.74.1 TPCC0_QEESR Register (Offset = 108Ch) [reset = h]

Short Description: QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-2994. Instance Table

Instance Name	Physical Address
TPCC0	4702 108Ch

Access Types Legend

Table 4-2995. QEESR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES73	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

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4.38.75 TPCC0_QSER Registers

4.38.75.1 TPCC0_QSER Register (Offset = 1090h) [reset = h]

Short Description: QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

Return to Summary Table

Table 4-2996. Instance Table

Instance Name	Physical Address
TPCC0	4702 1090h

Access Types Legend

Table 4-2997. QSER Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES74	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

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4.38.76 TPCC0_QSECR Registers

4.38.76.1 TPCC0_QSECR Register (Offset = 1094h) [reset = h]

Short Description: QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-2998. Instance Table

Instance Name	Physical Address
TPCC0	4702 1094h

Access Types Legend

Table 4-2999. QSECR Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES75	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

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4.38.77 TPCC0_ER_RN Registers

4.38.77.1 TPCC0_ER_RN Register (Offset = 2000h) [reset = h]

Short Description: Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.

Long Description:

Return to Summary Table

Table 4-3000. Instance Table

Instance Name	Physical Address
TPCC0	4702 2000h

Access Types Legend

Table 4-3001. ER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3

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Table 4-3001. ER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

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4.38.78 TPCC0_ERH_RN Registers

4.38.78.1 TPCC0_ERH_RN Register (Offset = 2004h) [reset = h]

Short Description: Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.

Long Description:

Return to Summary Table

Table 4-3002. Instance Table

Instance Name	Physical Address
TPCC0	4702 2004h

Access Types Legend

Table 4-3003. ERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35

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Table 4-3003. ERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

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4.38.79 TPCC0_ECR_RN Registers

4.38.79.1 TPCC0_ECR_RN Register (Offset = 2008h) [reset = h]

Short Description: Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-3004. Instance Table

Instance Name	Physical Address
TPCC0	4702 2008h

Access Types Legend

Table 4-3005. ECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

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4.38.80 TPCC0_ECRH_RN Registers

4.38.80.1 TPCC0_ECRH_RN Register (Offset = 200Ch) [reset = h]

Short Description: Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-3006. Instance Table

Instance Name	Physical Address
TPCC0	4702 200Ch

Access Types Legend

Table 4-3007. ECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

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4.38.81 TPCC0_ESR_RN Registers

4.38.81.1 TPCC0_ESR_RN Register (Offset = 2010h) [reset = h]

Short Description: Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-3008. Instance Table

Instance Name	Physical Address
TPCC0	4702 2010h

Access Types Legend

Table 4-3009. ESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

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4.38.82 TPCC0_ESRH_RN Registers

4.38.82.1 TPCC0_ESRH_RN Register (Offset = 2014h) [reset = h]

Short Description: Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-3010. Instance Table

Instance Name	Physical Address
TPCC0	4702 2014h

Access Types Legend

Table 4-3011. ESRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

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4.38.83 TPCC0_CER_RN Registers

4.38.83.1 TPCC0_CER_RN Register (Offset = 2018h) [reset = h]

Short Description: Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.

Long Description:

Return to Summary Table

Table 4-3012. Instance Table

Instance Name	Physical Address
TPCC0	4702 2018h

Access Types Legend

Table 4-3013. CER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3

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Table 4-3013. CER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

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4.38.84 TPCC0_CERH_RN Registers

4.38.84.1 TPCC0_CERH_RN Register (Offset = 201Ch) [reset = h]

Short Description: Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.

Long Description:

Return to Summary Table

Table 4-3014. Instance Table

Instance Name	Physical Address
TPCC0	4702 201Ch

Access Types Legend

Table 4-3015. CERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35

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Table 4-3015. CERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

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4.38.85 TPCC0_EER_RN Registers

4.38.85.1 TPCC0_EER_RN Register (Offset = 2020h) [reset = h]

Short Description: Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.

Long Description:

Return to Summary Table

Table 4-3016. Instance Table

Instance Name	Physical Address
TPCC0	4702 2020h

Access Types Legend

Table 4-3017. EER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3

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Table 4-3017. EER_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

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4.38.86 TPCC0_EERH_RN Registers

4.38.86.1 TPCC0_EERH_RN Register (Offset = 2024h) [reset = h]

Short Description: Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc_eventN_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.

Long Description:

Return to Summary Table

Table 4-3018. Instance Table

Instance Name	Physical Address
TPCC0	4702 2024h

Access Types Legend

Table 4-3019. EERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35

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Table 4-3019. EERH_RN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

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4.38.87 TPCC0_EECR_RN Registers

4.38.87.1 TPCC0_EECR_RN Register (Offset = 2028h) [reset = h]

Short Description: Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-3020. Instance Table

Instance Name	Physical Address
TPCC0	4702 2028h

Access Types Legend

Table 4-3021. EECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

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4.38.88 TPCC0_EECRH_RN Registers

4.38.88.1 TPCC0_EECRH_RN Register (Offset = 202Ch) [reset = h]

Short Description: Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-3022. Instance Table

Instance Name	Physical Address
TPCC0	4702 202Ch

Access Types Legend

Table 4-3023. EECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

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4.38.89 TPCC0_EESR_RN Registers

4.38.89.1 TPCC0_EESR_RN Register (Offset = 2030h) [reset = h]

Short Description: Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-3024. Instance Table

Instance Name	Physical Address
TPCC0	4702 2030h

Access Types Legend

Table 4-3025. EESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

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4.38.90 TPCC0_EESRH_RN Registers

4.38.90.1 TPCC0_EESRH_RN Register (Offset = 2034h) [reset = h]

Short Description: Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-3026. Instance Table

Instance Name	Physical Address
TPCC0	4702 2034h

Access Types Legend

Table 4-3027. EESRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

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4.38.91 TPCC0_SER_RN Registers

4.38.91.1 TPCC0_SER_RN Register (Offset = 2038h) [reset = h]

Short Description: Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

Return to Summary Table

Table 4-3028. Instance Table

Instance Name	Physical Address
TPCC0	4702 2038h

Access Types Legend

Table 4-3029. SER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	RO	0h	Event #31
30	E30	RO	0h	Event #30
29	E29	RO	0h	Event #29
28	E28	RO	0h	Event #28
27	E27	RO	0h	Event #27
26	E26	RO	0h	Event #26
25	E25	RO	0h	Event #25
24	E24	RO	0h	Event #24
23	E23	RO	0h	Event #23
22	E22	RO	0h	Event #22
21	E21	RO	0h	Event #21
20	E20	RO	0h	Event #20
19	E19	RO	0h	Event #19
18	E18	RO	0h	Event #18
17	E17	RO	0h	Event #17
16	E16	RO	0h	Event #16
15	E15	RO	0h	Event #15
14	E14	RO	0h	Event #14
13	E13	RO	0h	Event #13
12	E12	RO	0h	Event #12
11	E11	RO	0h	Event #11
10	E10	RO	0h	Event #10
9	E9	RO	0h	Event #9
8	E8	RO	0h	Event #8
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

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4.38.92 TPCC0_SERH_RN Registers

4.38.92.1 TPCC0_SERH_RN Register (Offset = 203Ch) [reset = h]

Short Description: Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

Return to Summary Table

Table 4-3030. Instance Table

Instance Name	Physical Address
TPCC0	4702 203Ch

Access Types Legend

Table 4-3031. SERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	RO	0h	Event #63
30	E62	RO	0h	Event #62
29	E61	RO	0h	Event #61
28	E60	RO	0h	Event #60
27	E59	RO	0h	Event #59
26	E58	RO	0h	Event #58
25	E57	RO	0h	Event #57
24	E56	RO	0h	Event #56
23	E55	RO	0h	Event #55
22	E54	RO	0h	Event #54
21	E53	RO	0h	Event #53
20	E52	RO	0h	Event #52
19	E51	RO	0h	Event #51
18	E50	RO	0h	Event #50
17	E49	RO	0h	Event #49
16	E48	RO	0h	Event #48
15	E47	RO	0h	Event #47
14	E46	RO	0h	Event #46
13	E45	RO	0h	Event #45
12	E44	RO	0h	Event #44
11	E43	RO	0h	Event #43
10	E42	RO	0h	Event #42
9	E41	RO	0h	Event #41
8	E40	RO	0h	Event #40
7	E39	RO	0h	Event #39
6	E38	RO	0h	Event #38
5	E37	RO	0h	Event #37
4	E36	RO	0h	Event #36
3	E35	RO	0h	Event #35
2	E34	RO	0h	Event #34
1	E33	RO	0h	Event #33
0	E32	RO	0h	Event #32

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4.38.93 TPCC0_SECR_RN Registers

4.38.93.1 TPCC0_SECR_RN Register (Offset = 2040h) [reset = h]

Short Description: Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-3032. Instance Table

Instance Name	Physical Address
TPCC0	4702 2040h

Access Types Legend

Table 4-3033. SECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E31	WO	0h	Event #31
30	E30	WO	0h	Event #30
29	E29	WO	0h	Event #29
28	E28	WO	0h	Event #28
27	E27	WO	0h	Event #27
26	E26	WO	0h	Event #26
25	E25	WO	0h	Event #25
24	E24	WO	0h	Event #24
23	E23	WO	0h	Event #23
22	E22	WO	0h	Event #22
21	E21	WO	0h	Event #21
20	E20	WO	0h	Event #20
19	E19	WO	0h	Event #19
18	E18	WO	0h	Event #18
17	E17	WO	0h	Event #17
16	E16	WO	0h	Event #16
15	E15	WO	0h	Event #15
14	E14	WO	0h	Event #14
13	E13	WO	0h	Event #13
12	E12	WO	0h	Event #12
11	E11	WO	0h	Event #11
10	E10	WO	0h	Event #10
9	E9	WO	0h	Event #9
8	E8	WO	0h	Event #8
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

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4.38.94 TPCC0_SECRH_RN Registers

4.38.94.1 TPCC0_SECRH_RN Register (Offset = 2044h) [reset = h]

Short Description: Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.

Long Description:

Return to Summary Table

Table 4-3034. Instance Table

Instance Name	Physical Address
TPCC0	4702 2044h

Access Types Legend

Table 4-3035. SECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	E63	WO	0h	Event #63
30	E62	WO	0h	Event #62
29	E61	WO	0h	Event #61
28	E60	WO	0h	Event #60
27	E59	WO	0h	Event #59
26	E58	WO	0h	Event #58
25	E57	WO	0h	Event #57
24	E56	WO	0h	Event #56
23	E55	WO	0h	Event #55
22	E54	WO	0h	Event #54
21	E53	WO	0h	Event #53
20	E52	WO	0h	Event #52
19	E51	WO	0h	Event #51
18	E50	WO	0h	Event #50
17	E49	WO	0h	Event #49
16	E48	WO	0h	Event #48
15	E47	WO	0h	Event #47
14	E46	WO	0h	Event #46
13	E45	WO	0h	Event #45
12	E44	WO	0h	Event #44
11	E43	WO	0h	Event #43
10	E42	WO	0h	Event #42
9	E41	WO	0h	Event #41
8	E40	WO	0h	Event #40
7	E39	WO	0h	Event #39
6	E38	WO	0h	Event #38
5	E37	WO	0h	Event #37
4	E36	WO	0h	Event #36
3	E35	WO	0h	Event #35
2	E34	WO	0h	Event #34
1	E33	WO	0h	Event #33
0	E32	WO	0h	Event #32

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4.38.95 TPCC0_IER_RN Registers

4.38.95.1 TPCC0_IER_RN Register (Offset = 2050h) [reset = h]

Short Description: Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.

Long Description:

Return to Summary Table

Table 4-3036. Instance Table

Instance Name	Physical Address
TPCC0	4702 2050h

Access Types Legend

Table 4-3037. IER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	RO	0h	Interrupt associated with TCC #31
30	I30	RO	0h	Interrupt associated with TCC #30
29	I29	RO	0h	Interrupt associated with TCC #29
28	I28	RO	0h	Interrupt associated with TCC #28
27	I27	RO	0h	Interrupt associated with TCC #27
26	I26	RO	0h	Interrupt associated with TCC #26
25	I25	RO	0h	Interrupt associated with TCC #25
24	I24	RO	0h	Interrupt associated with TCC #24
23	I23	RO	0h	Interrupt associated with TCC #23
22	I22	RO	0h	Interrupt associated with TCC #22
21	I21	RO	0h	Interrupt associated with TCC #21
20	I20	RO	0h	Interrupt associated with TCC #20
19	I19	RO	0h	Interrupt associated with TCC #19
18	I18	RO	0h	Interrupt associated with TCC #18
17	I17	RO	0h	Interrupt associated with TCC #17
16	I16	RO	0h	Interrupt associated with TCC #16
15	I15	RO	0h	Interrupt associated with TCC #15
14	I14	RO	0h	Interrupt associated with TCC #14
13	I13	RO	0h	Interrupt associated with TCC #13
12	I12	RO	0h	Interrupt associated with TCC #12
11	I11	RO	0h	Interrupt associated with TCC #11
10	I10	RO	0h	Interrupt associated with TCC #10
9	I9	RO	0h	Interrupt associated with TCC #9
8	I8	RO	0h	Interrupt associated with TCC #8
7	I7	RO	0h	Interrupt associated with TCC #7
6	I6	RO	0h	Interrupt associated with TCC #6
5	I5	RO	0h	Interrupt associated with TCC #5
4	I4	RO	0h	Interrupt associated with TCC #4
3	I3	RO	0h	Interrupt associated with TCC #3
2	I2	RO	0h	Interrupt associated with TCC #2
1	I1	RO	0h	Interrupt associated with TCC #1
0	I0	RO	0h	Interrupt associated with TCC #0

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4.38.96 TPCC0_IERH_RN Registers

4.38.96.1 TPCC0_IERH_RN Register (Offset = 2054h) [reset = h]

Short Description: Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.

Long Description:

Return to Summary Table

Table 4-3038. Instance Table

Instance Name	Physical Address
TPCC0	4702 2054h

Access Types Legend

Table 4-3039. IERH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	RO	0h	Interrupt associated with TCC #63
30	I62	RO	0h	Interrupt associated with TCC #62
29	I61	RO	0h	Interrupt associated with TCC #61
28	I60	RO	0h	Interrupt associated with TCC #60
27	I59	RO	0h	Interrupt associated with TCC #59
26	I58	RO	0h	Interrupt associated with TCC #58
25	I57	RO	0h	Interrupt associated with TCC #57
24	I56	RO	0h	Interrupt associated with TCC #56
23	I55	RO	0h	Interrupt associated with TCC #55
22	I54	RO	0h	Interrupt associated with TCC #54
21	I53	RO	0h	Interrupt associated with TCC #53
20	I52	RO	0h	Interrupt associated with TCC #52
19	I51	RO	0h	Interrupt associated with TCC #51
18	I50	RO	0h	Interrupt associated with TCC #50
17	I49	RO	0h	Interrupt associated with TCC #49
16	I48	RO	0h	Interrupt associated with TCC #48
15	I47	RO	0h	Interrupt associated with TCC #47
14	I46	RO	0h	Interrupt associated with TCC #46
13	I45	RO	0h	Interrupt associated with TCC #45
12	I44	RO	0h	Interrupt associated with TCC #44
11	I43	RO	0h	Interrupt associated with TCC #43
10	I42	RO	0h	Interrupt associated with TCC #42
9	I41	RO	0h	Interrupt associated with TCC #41
8	I40	RO	0h	Interrupt associated with TCC #40
7	I39	RO	0h	Interrupt associated with TCC #39
6	I38	RO	0h	Interrupt associated with TCC #38
5	I37	RO	0h	Interrupt associated with TCC #37
4	I36	RO	0h	Interrupt associated with TCC #36
3	I35	RO	0h	Interrupt associated with TCC #35
2	I34	RO	0h	Interrupt associated with TCC #34
1	I33	RO	0h	Interrupt associated with TCC #33
0	I32	RO	0h	Interrupt associated with TCC #32

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4.38.97 TPCC0_IECR_RN Registers

4.38.97.1 TPCC0_IECR_RN Register (Offset = 2058h) [reset = h]

Short Description: Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-3040. Instance Table

Instance Name	Physical Address
TPCC0	4702 2058h

Access Types Legend

Table 4-3041. IECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

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4.38.98 TPCC0_IECRH_RN Registers

4.38.98.1 TPCC0_IECRH_RN Register (Offset = 205Ch) [reset = h]

Short Description: Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-3042. Instance Table

Instance Name	Physical Address
TPCC0	4702 205Ch

Access Types Legend

Table 4-3043. IECRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39
6	I38	WO	0h	Interrupt associated with TCC #38
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

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4.38.99 TPCC0_IESR_RN Registers

4.38.99.1 TPCC0_IESR_RN Register (Offset = 2060h) [reset = h]

Short Description: Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-3044. Instance Table

Instance Name	Physical Address
TPCC0	4702 2060h

Access Types Legend

Table 4-3045. IESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

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4.38.100 TPCC0_IESRH_RN Registers

4.38.100.1 TPCC0_IESRH_RN Register (Offset = 2064h) [reset = h]

Short Description: Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-3046. Instance Table

Instance Name	Physical Address
TPCC0	4702 2064h

Access Types Legend

Table 4-3047. IESRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39
6	I38	WO	0h	Interrupt associated with TCC #38
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

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4.38.101 TPCC0_IPR_RN Registers

4.38.101.1 TPCC0_IPR_RN Register (Offset = 2068h) [reset = h]

Short Description: Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.

Long Description:

Return to Summary Table

Table 4-3048. Instance Table

Instance Name	Physical Address
TPCC0	4702 2068h

Access Types Legend

Table 4-3049. IPR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	RO	0h	Interrupt associated with TCC #31
30	I30	RO	0h	Interrupt associated with TCC #30
29	I29	RO	0h	Interrupt associated with TCC #29
28	I28	RO	0h	Interrupt associated with TCC #28
27	I27	RO	0h	Interrupt associated with TCC #27
26	I26	RO	0h	Interrupt associated with TCC #26
25	I25	RO	0h	Interrupt associated with TCC #25
24	I24	RO	0h	Interrupt associated with TCC #24
23	I23	RO	0h	Interrupt associated with TCC #23
22	I22	RO	0h	Interrupt associated with TCC #22
21	I21	RO	0h	Interrupt associated with TCC #21
20	I20	RO	0h	Interrupt associated with TCC #20
19	I19	RO	0h	Interrupt associated with TCC #19
18	I18	RO	0h	Interrupt associated with TCC #18
17	I17	RO	0h	Interrupt associated with TCC #17
16	I16	RO	0h	Interrupt associated with TCC #16
15	I15	RO	0h	Interrupt associated with TCC #15
14	I14	RO	0h	Interrupt associated with TCC #14
13	I13	RO	0h	Interrupt associated with TCC #13
12	I12	RO	0h	Interrupt associated with TCC #12
11	I11	RO	0h	Interrupt associated with TCC #11
10	I10	RO	0h	Interrupt associated with TCC #10
9	I9	RO	0h	Interrupt associated with TCC #9
8	I8	RO	0h	Interrupt associated with TCC #8
7	I7	RO	0h	Interrupt associated with TCC #7
6	I6	RO	0h	Interrupt associated with TCC #6
5	I5	RO	0h	Interrupt associated with TCC #5
4	I4	RO	0h	Interrupt associated with TCC #4
3	I3	RO	0h	Interrupt associated with TCC #3
2	I2	RO	0h	Interrupt associated with TCC #2
1	I1	RO	0h	Interrupt associated with TCC #1
0	I0	RO	0h	Interrupt associated with TCC #0

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4.38.102 TPCC0_IPRH_RN Registers

4.38.102.1 TPCC0_IPRH_RN Register (Offset = 206Ch) [reset = h]

Short Description: Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.

Long Description:

Return to Summary Table

Table 4-3050. Instance Table

Instance Name	Physical Address
TPCC0	4702 206Ch

Access Types Legend

Table 4-3051. IPRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	RO	0h	Interrupt associated with TCC #63
30	I62	RO	0h	Interrupt associated with TCC #62
29	I61	RO	0h	Interrupt associated with TCC #61
28	I60	RO	0h	Interrupt associated with TCC #60
27	I59	RO	0h	Interrupt associated with TCC #59
26	I58	RO	0h	Interrupt associated with TCC #58
25	I57	RO	0h	Interrupt associated with TCC #57
24	I56	RO	0h	Interrupt associated with TCC #56
23	I55	RO	0h	Interrupt associated with TCC #55
22	I54	RO	0h	Interrupt associated with TCC #54
21	I53	RO	0h	Interrupt associated with TCC #53
20	I52	RO	0h	Interrupt associated with TCC #52
19	I51	RO	0h	Interrupt associated with TCC #51
18	I50	RO	0h	Interrupt associated with TCC #50
17	I49	RO	0h	Interrupt associated with TCC #49
16	I48	RO	0h	Interrupt associated with TCC #48
15	I47	RO	0h	Interrupt associated with TCC #47
14	I46	RO	0h	Interrupt associated with TCC #46
13	I45	RO	0h	Interrupt associated with TCC #45
12	I44	RO	0h	Interrupt associated with TCC #44
11	I43	RO	0h	Interrupt associated with TCC #43
10	I42	RO	0h	Interrupt associated with TCC #42
9	I41	RO	0h	Interrupt associated with TCC #41
8	I40	RO	0h	Interrupt associated with TCC #40
7	I39	RO	0h	Interrupt associated with TCC #39
6	I38	RO	0h	Interrupt associated with TCC #38
5	I37	RO	0h	Interrupt associated with TCC #37
4	I36	RO	0h	Interrupt associated with TCC #36
3	I35	RO	0h	Interrupt associated with TCC #35
2	I34	RO	0h	Interrupt associated with TCC #34
1	I33	RO	0h	Interrupt associated with TCC #33
0	I32	RO	0h	Interrupt associated with TCC #32

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4.38.103 TPCC0_ICR_RN Registers

4.38.103.1 TPCC0_ICR_RN Register (Offset = 2070h) [reset = h]

Short Description: Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-3052. Instance Table

Instance Name	Physical Address
TPCC0	4702 2070h

Access Types Legend

Table 4-3053. ICR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I31	WO	0h	Interrupt associated with TCC #31
30	I30	WO	0h	Interrupt associated with TCC #30
29	I29	WO	0h	Interrupt associated with TCC #29
28	I28	WO	0h	Interrupt associated with TCC #28
27	I27	WO	0h	Interrupt associated with TCC #27
26	I26	WO	0h	Interrupt associated with TCC #26
25	I25	WO	0h	Interrupt associated with TCC #25
24	I24	WO	0h	Interrupt associated with TCC #24
23	I23	WO	0h	Interrupt associated with TCC #23
22	I22	WO	0h	Interrupt associated with TCC #22
21	I21	WO	0h	Interrupt associated with TCC #21
20	I20	WO	0h	Interrupt associated with TCC #20
19	I19	WO	0h	Interrupt associated with TCC #19
18	I18	WO	0h	Interrupt associated with TCC #18
17	I17	WO	0h	Interrupt associated with TCC #17
16	I16	WO	0h	Interrupt associated with TCC #16
15	I15	WO	0h	Interrupt associated with TCC #15
14	I14	WO	0h	Interrupt associated with TCC #14
13	I13	WO	0h	Interrupt associated with TCC #13
12	I12	WO	0h	Interrupt associated with TCC #12
11	I11	WO	0h	Interrupt associated with TCC #11
10	I10	WO	0h	Interrupt associated with TCC #10
9	I9	WO	0h	Interrupt associated with TCC #9
8	I8	WO	0h	Interrupt associated with TCC #8
7	I7	WO	0h	Interrupt associated with TCC #7
6	I6	WO	0h	Interrupt associated with TCC #6
5	I5	WO	0h	Interrupt associated with TCC #5
4	I4	WO	0h	Interrupt associated with TCC #4
3	I3	WO	0h	Interrupt associated with TCC #3
2	I2	WO	0h	Interrupt associated with TCC #2
1	I1	WO	0h	Interrupt associated with TCC #1
0	I0	WO	0h	Interrupt associated with TCC #0

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4.38.104 TPCC0_ICRH_RN Registers

4.38.104.1 TPCC0_ICRH_RN Register (Offset = 2074h) [reset = h]

Short Description: Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.

Long Description:

Return to Summary Table

Table 4-3054. Instance Table

Instance Name	Physical Address
TPCC0	4702 2074h

Access Types Legend

Table 4-3055. ICRH_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31	I63	WO	0h	Interrupt associated with TCC #63
30	I62	WO	0h	Interrupt associated with TCC #62
29	I61	WO	0h	Interrupt associated with TCC #61
28	I60	WO	0h	Interrupt associated with TCC #60
27	I59	WO	0h	Interrupt associated with TCC #59
26	I58	WO	0h	Interrupt associated with TCC #58
25	I57	WO	0h	Interrupt associated with TCC #57
24	I56	WO	0h	Interrupt associated with TCC #56
23	I55	WO	0h	Interrupt associated with TCC #55
22	I54	WO	0h	Interrupt associated with TCC #54
21	I53	WO	0h	Interrupt associated with TCC #53
20	I52	WO	0h	Interrupt associated with TCC #52
19	I51	WO	0h	Interrupt associated with TCC #51
18	I50	WO	0h	Interrupt associated with TCC #50
17	I49	WO	0h	Interrupt associated with TCC #49
16	I48	WO	0h	Interrupt associated with TCC #48
15	I47	WO	0h	Interrupt associated with TCC #47
14	I46	WO	0h	Interrupt associated with TCC #46
13	I45	WO	0h	Interrupt associated with TCC #45
12	I44	WO	0h	Interrupt associated with TCC #44
11	I43	WO	0h	Interrupt associated with TCC #43
10	I42	WO	0h	Interrupt associated with TCC #42
9	I41	WO	0h	Interrupt associated with TCC #41
8	I40	WO	0h	Interrupt associated with TCC #40
7	I39	WO	0h	Interrupt associated with TCC #39
6	I38	WO	0h	Interrupt associated with TCC #38
5	I37	WO	0h	Interrupt associated with TCC #37
4	I36	WO	0h	Interrupt associated with TCC #36
3	I35	WO	0h	Interrupt associated with TCC #35
2	I34	WO	0h	Interrupt associated with TCC #34
1	I33	WO	0h	Interrupt associated with TCC #33
0	I32	WO	0h	Interrupt associated with TCC #32

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4.38.105 TPCC0_IEVAL_RN Registers

4.38.105.1 TPCC0_IEVAL_RN Register (Offset = 2078h) [reset = h]

Short Description: Interrupt Eval Register

Long Description:

Return to Summary Table

Table 4-3056. Instance Table

Instance Name	Physical Address
TPCC0	4702 2078h

Access Types Legend

Table 4-3057. IEVAL_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 2	RES76	RO	0h	RESERVE FIELD
1	SET	WO	0h	Interrupt Set: CPU write of '1' to the SETn bit causes the tpcc_intN output signal to be pulsed egardless of state of interrupts enable (IERn) and status (IPRn). CPU write of '0' has no effect.
0	EVAL	WO	0h	Interrupt Evaluate: CPU write of '1' to the EVALn bit causes the tpcc_intN output signal to be pulsed if any enabled interrupts (IERn) are still pending (IPRn). CPU write of '0' has no effect..

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4.38.106 TPCC0_QER_RN Registers

4.38.106.1 TPCC0_QER_RN Register (Offset = 2080h) [reset = h]

Short Description: QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.

Long Description:

Return to Summary Table

Table 4-3058. Instance Table

Instance Name	Physical Address
TPCC0	4702 2080h

Access Types Legend

Table 4-3059. QER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES77	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

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4.38.107 TPCC0_QEER_RN Registers

4.38.107.1 TPCC0_QEER_RN Register (Offset = 2084h) [reset = h]

Short Description: QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/latched in QER.En.

Long Description:

Return to Summary Table

Table 4-3060. Instance Table

Instance Name	Physical Address
TPCC0	4702 2084h

Access Types Legend

Table 4-3061. QEER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES78	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

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4.38.108 TPCC0_QEECR_RN Registers

4.38.108.1 TPCC0_QEECR_RN Register (Offset = 2088h) [reset = h]

Short Description: QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-3062. Instance Table

Instance Name	Physical Address
TPCC0	4702 2088h

Access Types Legend

Table 4-3063. QEECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES79	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

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4.38.109 TPCC0_QEESR_RN Registers

4.38.109.1 TPCC0_QEESR_RN Register (Offset = 208Ch) [reset = h]

Short Description: QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-3064. Instance Table

Instance Name	Physical Address
TPCC0	4702 208Ch

Access Types Legend

Table 4-3065. QEESR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES80	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

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4.38.110 TPCC0_QSER_RN Registers

4.38.110.1 TPCC0_QSER_RN Register (Offset = 2090h) [reset = h]

Short Description: QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Long Description:

Return to Summary Table

Table 4-3066. Instance Table

Instance Name	Physical Address
TPCC0	4702 2090h

Access Types Legend

Table 4-3067. QSER_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES81	RO	0h	RESERVE FIELD
7	E7	RO	0h	Event #7
6	E6	RO	0h	Event #6
5	E5	RO	0h	Event #5
4	E4	RO	0h	Event #4
3	E3	RO	0h	Event #3
2	E2	RO	0h	Event #2
1	E1	RO	0h	Event #1
0	E0	RO	0h	Event #0

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4.38.111 TPCC0_QSECR_RN Registers

4.38.111.1 TPCC0_QSECR_RN Register (Offset = 2094h) [reset = h]

Short Description: QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..

Long Description:

Return to Summary Table

Table 4-3068. Instance Table

Instance Name	Physical Address
TPCC0	4702 2094h

Access Types Legend

Table 4-3069. QSECR_RN Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 8	RES82	RO	0h	RESERVE FIELD
7	E7	WO	0h	Event #7
6	E6	WO	0h	Event #6
5	E5	WO	0h	Event #5
4	E4	WO	0h	Event #4
3	E3	WO	0h	Event #3
2	E2	WO	0h	Event #2
1	E1	WO	0h	Event #1
0	E0	WO	0h	Event #0

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4.38.112 TPCC0_OPT Registers

4.38.112.1 TPCC0_OPT Register (Offset = 4000h) [reset = h]

Short Description: Options Parameter

Long Description:

Return to Summary Table

Table 4-3070. Instance Table

Instance Name	Physical Address
TPCC0	4702 4000h

Access Types Legend

Table 4-3071. OPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PRIV	RO	0h	Privilege level: privilege level (supervisor vs. user) for the host/cpu/dma that programmed this PaRAM Entry. Value is set with the vbus priv value when any part of the PaRAM Entry is written. Not writeable via vbus wdata bus. Is readable via VBus rdata bus. PRIV = 0 : User level privilege PRIV = 1 : Supervisor level privilege
30 - 28	RES83	RO	0h	RESERVE FIELD
27 - 24	PRIVID	RO	0h	Privilege ID: Privilege ID for the external host/cpu/dma that programmed this PaRAM Entry. This value is set with the vbus privid value when any part of the PaRAM Entry is written. Not writeable via vbus wdata bus. Is readable via VBus rdata bus.
23	ITCCHEN	RW	0h	Intermediate transfer completion chaining enable: 0: Intermediate transfer complete chaining is disabled. 1: Intermediate transfer complete chaining is enabled.
22	TCCHEN	RW	0h	Transfer complete chaining enable: 0: Transfer complete chaining is disabled. 1: Transfer complete chaining is enabled.
21	ITCINTEN	RW	0h	Intermediate transfer completion interrupt enable: 0: Intermediate transfer complete interrupt is disabled. 1: Intermediate transfer complete interrupt is enabled (corresponding IER[TCC] bit must be set to 1 to generate interrupt)
20	TCINTEN	RW	0h	Transfer complete interrupt enable: 0: Transfer complete interrupt is disabled. 1: Transfer complete interrupt is enabled (corresponding IER[TCC] bit must be set to 1 to generate interrupt)
19	WIMODE	RW	0h	Backward compatibility mode: 0: Normal operation 1 : WI Backwards Compatibility mode forces BCNT to be adjusted by '1' upon TR submission (0 means 1 1 means 2 ...) and forces ACNT to be treated as a word-count (left shifted by 2 by hardware to create byte cnt for TR submission)
18	RES84	RO	0h	RESERVE FIELD
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER (bit CER[TCC]) for chaining or in IER (bit IER[TCC]) for interrupts.
11	TCCMODE	RW	0h	Transfer complete code mode: Indicates the point at which a transfer is considered completed. Applies to both chaining and interrupt. 0: Normal Completion A transfer is considered completed after the transfer parameters are returned to the CC from the TC (which was returned from the peripheral). 1: Early Completion A transfer is considered completed after the CC submits a TR to the TC. CC generates completion code internally .
10 - 8	FWID	RW	0h	FIFO width: Applies if either SAM or DAM is set to FIFO mode. Pass-thru to TC.
7 - 4	RES85	RO	0h	RESERVE FIELD

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Table 4-3071. OPT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	STATIC	RW	0h	Static Entry: 0: Entry is updated as normal 1: Entry is static Count and Address updates are not updated after TRP is submitted. Linking is not performed.
2	SYNCDIM	RW	0h	Transfer Synchronization Dimension: 0: A-Sync Each event triggers the transfer of ACNT elements. 1: AB-Sync Each event triggers the transfer of BCNT arrays of ACNT elements
1	DAM	RW	0h	Destination Address Mode: Destination Address Mode within an array. Pass-thru to TC. 0: INCR Dst addressing within an array increments. Dst is not a FIFO. 1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode: Source Address Mode within an array. Pass-thru to TC. 0: INCR Src addressing within an array increments. Source is not a FIFO. 1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

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4.38.113 TPCC0_SRC Registers

4.38.113.1 TPCC0_SRC Register (Offset = 4004h) [reset = h]

Short Description: Source Address

Long Description:

Return to Summary Table

Table 4-3072. Instance Table

Instance Name	Physical Address
TPCC0	4702 4004h

Access Types Legend

Table 4-3073. SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SRC	RW	0h	Source Address: The 32-bit source address parameters specify the starting byte address of the source . If SAM is set to FIFO mode then the user should program the Source address to be aligned to the value specified by the OPT.FWID field. No errors are recognized here but TC will assert error if this is not true.

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4.38.114 TPCC0_ABCNT Registers

4.38.114.1 TPCC0_ABCNT Register (Offset = 4008h) [reset = h]

Short Description: A and B byte count

Long Description:

Return to Summary Table

Table 4-3074. Instance Table

Instance Name	Physical Address
TPCC0	4702 4008h

Access Types Legend

Table 4-3075. ABCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	BCNT	RW	0h	BCNT : Count for 2nd Dimension: BCNT is a 16-bit unsigned value that specifies the number of arrays of length ACNT. For normal operation valid values for BCNT can be anywhere between 1 and 65535. Therefore the maximum number of arrays in a frame is 65535 (64K-1 arrays). BCNT=1 means 1 array in the frame and BCNT=0 means 0 arrays in the frame. In normal mode a BCNT of '0' is considered as either a Null or Dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. If the OPT.WIMODE bit is set then the programmed BCNT value will be incremented by '1' before submission to TC. I.e. 0 means 1 1 means 2 2 means 3 ...
15 - 0	ACNT	RW	0h	ACNT : number of bytes in 1st dimension: ACNT represents the number of bytes within the first dimension of a transfer. ACNT is a 16-bit unsigned value with valid values between 0 and 65535. Therefore the maximum number of bytes in an array is 65535 bytes (64K-1 bytes). ACNT must be greater than or equal to '1' for a TR to be submitted to TC. An ACNT of '0' is considered as either a null or dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. If the OPT.WIMODE bit is set then the ACNT field represents a word count. The CC must internally multiply by 4 to translate the word count to a byte count prior to submission to the TC. The 2 MSBs of the 16-bit ACNT are reserved and should always be written as 'b00 by the user. If user writes a value other than 0 it will still be treated as 0 since the multiply-by-4 operation (to translate between a word count and a byte count) will dropthe 2 msbits. For dummy and null transfer definition the ACNT definition will disregard the 2 msbits. I.e. a programmed ACNT value of 0x8000 in WI-mode will be treated as 0 byte transfer resulting in null or dummy operation dependent on the state of BCNT and CCNT.

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4.38.115 TPCC0_DST Registers

4.38.115.1 TPCC0_DST Register (Offset = 400Ch) [reset = h]

Short Description: Destination Address

Long Description:

Return to Summary Table

Table 4-3076. Instance Table

Instance Name	Physical Address
TPCC0	4702 400Ch

Access Types Legend

Table 4-3077. DST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DST	RW	0h	Destination Address: The 32-bit destination address parameters specify the starting byte address of the destination. If DAM is set to FIFO mode then the user should program the Destination address to be aligned to the value specified by the OPT.FWID field. No errors are recognized here but TC will assert error if this is not true.

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4.38.116 TPCC0_BIDX Registers

4.38.116.1 TPCC0_BIDX Register (Offset = 4010h) [reset = h]

Short Description: Register description is not available

Long Description:

Return to Summary Table

Table 4-3078. Instance Table

Instance Name	Physical Address
TPCC0	4702 4010h

Access Types Legend

Table 4-3079. BIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RW	0h	Destination 2nd Dimension Index: DBIDX is a 16-bit signed value (2's complement) used for destination address modification in between each array in the 2nd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the destination array to the beginning of the next destination array within the current frame. It applies to both A-Sync and AB-Sync transfers.
15 - 0	SBIDX	RW	0h	Source 2nd Dimension Index: SBIDX is a 16-bit signed value (2's complement) used for source address modification in between each array in the 2nd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the source array to the beginning of the next source array. It applies to both A-sync and AB-sync transfers.

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4.38.117 TPCC0_LNK Registers

4.38.117.1 TPCC0_LNK Register (Offset = 4014h) [reset = h]

Short Description: Link and Reload parameters

Long Description:

Return to Summary Table

Table 4-3080. Instance Table

Instance Name	Physical Address
TPCC0	4702 4014h

Access Types Legend

Table 4-3081. LNK Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	BCNTRLD	RW	0h	BCNT Reload: BCNTRLD is a 16-bit unsigned value used to reload the BCNT field once the last array in the 2nd dimension is transferred. This field is only used for A-Sync'ed transfers. In this case the CC decrements the BCNT value by one on each TR submission. When BCNT (conceptually) reaches zero then the CC decrements CCNT and uses the BCNTRLD value to reinitialize the BCNT value. For AB-synchronized transfers the CC submits the BCNT in the TR and therefore the TC is responsible to keep track of BCNT not thus BCNTRLD is a don't care field.
15 - 0	LINK	RW	0h	Link Address: The CC provides a mechanism to reload the current PaRAM Entry upon its natural termination (i.e. after count fields are decremented to '0') with a new PaRAM Entry. This is called 'linking'. The 16-bit parameter LINK specifies the byte address offset in the PaRAM from which the CC loads/reloads the next PaRAM entry in the link. The CC should disregard the value in the upper 2 bits of the LINK field as well as the lower 5-bits of the LINK field. The upper two bits are ignored such that the user can program either the 'literal' byte address of the LINK parameter or the 'PaRAM base-relative' address of the link field. Therefore if the user uses the literal address with a range from 0x4000 to 0x7FFF it will be treated as a PaRAM-base-relative value of 0x0000 to 0x3FFF. The lower-5 bits are ignored and treated as 'b00000 thereby guaranteeing that all Link pointers point to a 32-byte aligned PaRAM entry. In the latter case (5-lsbs) behavior is undefined forthe user (i.e. don't have to test it). In the former case (2 msbs) user should be able to take advantage of this feature (i.e. do have to test it). If a Link Update is requested to a PaRAM address that is beyond the actual range of implemented PaRAM then the Link will be treated as a Null Linkand all 0s plus 0xFFFF will be written to the current entry location. A LINK value of 0xFFFF is referred to as a NULL link which should cause the CC to write 0x0 to all entries of the current PaRAM Entry except for the LINK field which is set to 0xFFFF. The Priv/Privid/Secure state is overwritten to 0x0 when linking. MSBs and LSBS should not be masked when comparing against the 0xFFFF value. I.e. a value of 0x3FFE is a non-NULL PaRAM link field.

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4.38.118 TPCC0_CIDX Registers

4.38.118.1 TPCC0_CIDX Register (Offset = 4018h) [reset = h]

Short Description: Register description is not available

Long Description:

Return to Summary Table

Table 4-3082. Instance Table

Instance Name	Physical Address
TPCC0	4702 4018h

Access Types Legend

Table 4-3083. CIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DCIDX	RW	0h	Destination Frame Index: DCIDX is a 16-bit signed value (2's complement) used for destination address modification for the 3rd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the current array (pointed to by DST address) to the beginning of the first destination array in the next frame. It applies to both A-sync and AB-sync transfers. Note that when DCIDX is applied the current array in an A-sync transfer is the last array in the frame while the current array in a ABsync transfer is the first array in the frame.
15 - 0	SCIDX	RW	0h	Source Frame Index: SCIDX is a 16-bit signed value (2's complement) used for source address modification for the 3rd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the current array (pointed to by SRC address) to the beginning of the first source array in the next frame. It applies to both A-sync and AB-sync transfers. Note that when SCIDX is applied the current array in an A-sync transfer is the last array in the frame while the current array in a AB-sync transfer is the first array in the frame.

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4.38.119 TPCC0_CCNT Registers

4.38.119.1 TPCC0_CCNT Register (Offset = 401Ch) [reset = h]

Short Description: C byte count

Long Description:

Return to Summary Table

Table 4-3084. Instance Table

Instance Name	Physical Address
TPCC0	4702 401Ch

Access Types Legend

Table 4-3085. CCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	RES86	RO	0h	RESERVE FIELD
15 - 0	CCNT	RW	0h	CCNT : Count for 3rd Dimension: CCNT is a 16-bit unsigned value that specifies the number of frames in a block. Valid values for CCNT can be anywhere between 1 and 65535. Therefore the maximum number of frames in a block is 65535 (64K-1 frames). CCNT of '1' means '1' frame in the block and CCNT of '0' means '0' frames in the block. A CCNT value of '0' is considered as either a null or dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. WIMODE has no affect on CCNT operation.

4.38.120 Access Table

Table 4-3086. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
WO	WO	Write

4.39 TPTC Registers

Table 4-3087. TPTC0[0:1] Registers Base Address Table

Offset	Length	Acronym	TPTC00 Physical Address	TPTC01 Physical Address
0h	32	TPTC_PID	4704 0000h	4706 0000h
4h	16	TPTC_TCCFG	4704 0004h	4706 0004h
100h	16	TPTC_TCSTAT	4704 0100h	4706 0100h
104h	8	TPTC_INTSTAT	4704 0104h	4706 0104h
108h	8	TPTC_INTEN	4704 0108h	4706 0108h
10Ch	8	TPTC_INTCLR	4704 010Ch	4706 010Ch
110h	8	TPTC_INTCMD	4704 0110h	4706 0110h
120h	8	TPTC_ERRSTAT	4704 0120h	4706 0120h
124h	8	TPTC_ERREN	4704 0124h	4706 0124h
128h	8	TPTC_ERRCLR	4704 0128h	4706 0128h
12Ch	24	TPTC_ERRDET	4704 012Ch	4706 012Ch
130h	8	TPTC_ERRCMD	4704 0130h	4706 0130h
140h	8	TPTC_RDRATE	4704 0140h	4706 0140h
200h	32	TPTC_POPT	4704 0200h	4706 0200h
204h	32	TPTC_PSRC	4704 0204h	4706 0204h

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Table 4-3087. TPTC0[0:1] Registers Base Address Table (continued)

Offset	Length	Acronym	TPTC00 Physical Address	TPTC01 Physical Address
208h	32	TPTC_PCNT	4704 0208h	4706 0208h
20Ch	32	TPTC_PDST	4704 020Ch	4706 020Ch
210h	32	TPTC_PBIDX	4704 0210h	4706 0210h
214h	16	TPTC_PMPPRXY	4704 0214h	4706 0214h
240h	32	TPTC_SAOPT	4704 0240h	4706 0240h
244h	32	TPTC_SASRC	4704 0244h	4706 0244h
248h	24	TPTC_SACNT	4704 0248h	4706 0248h
24Ch	32	TPTC_SADST	4704 024Ch	4706 024Ch
250h	32	TPTC_SABIDX	4704 0250h	4706 0250h
254h	16	TPTC_SAMPPRXY	4704 0254h	4706 0254h
258h	16	TPTC_SACNTRLD	4704 0258h	4706 0258h
25Ch	32	TPTC_SASRCBREF	4704 025Ch	4706 025Ch
260h	32	TPTC_SADSTBREF	4704 0260h	4706 0260h
264h	16	TPTC_SABCNT	4704 0264h	4706 0264h
280h	16	TPTC_DFCNTRLD	4704 0280h	4706 0280h
284h	32	TPTC_DFSRCBREF	4704 0284h	4706 0284h
300h	32	TPTC_DFOPT0	4704 0300h	4706 0300h
304h	32	TPTC_DFSRC0	4704 0304h	4706 0304h
308h	24	TPTC_DFACNT0	4704 0308h	4706 0308h
30Ch	32	TPTC_DFDST0	4704 030Ch	4706 030Ch
310h	32	TPTC_DFBIDX0	4704 0310h	4706 0310h
314h	16	TPTC_DFMPPRXY0	4704 0314h	4706 0314h
318h	16	TPTC_DFBCNT0	4704 0318h	4706 0318h
340h	32	TPTC_DFOPT1	4704 0340h	4706 0340h
344h	32	TPTC_DFSRC1	4704 0344h	4706 0344h
348h	24	TPTC_DFACNT1	4704 0348h	4706 0348h
34Ch	32	TPTC_DFDST1	4704 034Ch	4706 034Ch
350h	32	TPTC_DFBIDX1	4704 0350h	4706 0350h
354h	16	TPTC_DFMPPRXY1	4704 0354h	4706 0354h
358h	16	TPTC_DFBCNT1	4704 0358h	4706 0358h

4.39.1 TPTC Instance Count Note

Note

n = 0 to 1 for the TPTC registers defined below.

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4.39.2 TPTC0n_PID Registers

4.39.2.1 TPTC0n_PID Register (Offset = 0h) [reset = h]

Short Description: Peripheral ID Register

Long Description:

Return to Summary Table

Table 4-3088. Instance Table

Instance Name	Physical Address
TPTC00	4704 0000h
TPTC01	4706 0000h

Access Types Legend

Table 4-3089. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 30	SCHEME	RO	1h	PID Scheme: Used to distinguish between old ID scheme and current. Spare bit to encode future schemes EDMA uses 'new scheme' indicated with value of 0x1.
	RESERVED	NONE		Reserved
27 - 16	FUNC	RO	0h	Function indicates a software compatible module family.
15 - 11	RTL	RO	1h	RTL Version
10 - 8	MAJOR	RO	Bh	Major Revision
7 - 6	CUSTOM	RO	0h	Custom revision field: Not used on this version of EDMA.
5 - 0	MINOR	RO	1h	Minor Revision

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4.39.3 TPTC0n_TCCFG Registers

4.39.3.1 TPTC0n_TCCFG Register (Offset = 4h) [reset = h]

Short Description: TC Configuration Register

Long Description:

Return to Summary Table

Table 4-3090. Instance Table

Instance Name	Physical Address
TPTC00	4704 0004h
TPTC01	4706 0004h

Access Types Legend

Table 4-3091. TCCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9 - 8	DREGDEPTH	RO	2h	Dst Register FIFO Depth Parameterization
	RESERVED	NONE		Reserved
5 - 4	BUSWIDTH	RO	2h	Bus Width Parameterization
	RESERVED	NONE		Reserved
2 - 0	FIFOSIZE	RO	4h	Fifo Size Parameterization

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4.39.4 TPTC0n_TCSTAT Registers

4.39.4.1 TPTC0n_TCSTAT Register (Offset = 100h) [reset = h]

Short Description: TC Status Register

Long Description:

Return to Summary Table

Table 4-3092. Instance Table

Instance Name	Physical Address
TPTC00	4704 0100h
TPTC01	4706 0100h

Access Types Legend

Table 4-3093. TCSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
13 - 12	DFSTRTPTR	RO	0h	Dst FIFO Start PointerRepresents the offset to the head entry of Dst Register FIFO in units of entries. Legal values = 0x0 to 0x3
	RESERVED	NONE		Reserved
8	ACTV	RO	1h	Channel ActiveChannel Active is a logical-OR of each of the BUSY/ ACTV signals. The ACTV bit must remain high through the life of a TR.ACTV = 0 : Channel is idle.ACTV = 1 : Channel is busy.
	RESERVED	NONE		Reserved
6 - 4	DSTACTV	RO	0h	Destination Active StateSpecifies the number of TRs that are resident in the Dst Register FIFO at a given instant.Legal values are constrained by the DSTREGDEPTH parameter.
	RESERVED	NONE		Reserved
2	WSACTV	RO	0h	Write Status ActiveWSACTV = 0 : Write status is not pending. Write status has been received for all previously issued write commands.WSACTV = 1 : Write Status is pending. Write status has not been received for all previously issued write commands.
1	SRCACTV	RO	0h	Source Active StateSRCACTV = 0 : Source Active set is idle. Any TR written to Prog Set will immediately transition to Source Active set as long as the Dst FIFO Set is not full [DSTFULL == 1].SRCACTV = 1 : Source Active set is busy either performing read transfers or waiting to perform read transfers for current Transfer Request.
0	PROGBUSY	RO	0h	Program Register Set BusyPROGBUSY = 0 : Prog set idle and is available for programming.PROGBUSY = 1 : Prog set busy. User should poll for PROGBUSY equal to '0' prior to re-programming the Program Register set.

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4.39.5 TPTC0n_INTSTAT Registers

4.39.5.1 TPTC0n_INTSTAT Register (Offset = 104h) [reset = h]

Short Description: Interrupt Status Register

Long Description:

Return to Summary Table

Table 4-3094. Instance Table

Instance Name	Physical Address
TPTC00	4704 0104h
TPTC01	4706 0104h

Access Types Legend

Table 4-3095. INTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TRDONE	RO	0h	TR Done Event Status:TRDONE = 0 : Condition not detected.TRDONE = 1 : Set when TC has completed a Transfer Request. TRDONE should be set when the write status is returned for the final write of a TR. Cleared when user writes '1' to INTCLR.TRDONE register bit.
0	PROGEMPTY	RO	0h	Program Set Empty Event Status:PROGEMPTY = 0 : Condition not detected.PROGEMPTY = 1 : Set when Program Register set transitions to empty state. Cleared when user writes '1' to INTCLR.PROGEMPTY register bit.

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4.39.6 TPTC0n_INTEN Registers

4.39.6.1 TPTC0n_INTEN Register (Offset = 108h) [reset = h]

Short Description: Interrupt Enable Register

Long Description:

Return to Summary Table

Table 4-3096. Instance Table

Instance Name	Physical Address
TPTC00	4704 0108h
TPTC01	4706 0108h

Access Types Legend

Table 4-3097. INTEN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TRDONE	RW	0h	TR Done Event Enable:INTEN.TRDONE = 0 : TRDONE Event is disabled.INTEN.TRDONE = 1 : TRDONE Event is enabled and contributes to interrupt generation
0	PROGEMPTY	RW	0h	Program Set Empty Event Enable:INTEN.PROGEMPTY = 0 : PROGEMPTY Event is disabled.INTEN.PROGEMPTY = 1 : PROGEMPTY Event is enabled and contributes to interrupt generation

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4.39.7 TPTC0n_INTCLR Registers

4.39.7.1 TPTC0n_INTCLR Register (Offset = 10Ch) [reset = h]

Short Description: Interrupt Clear Register

Long Description:

Return to Summary Table

Table 4-3098. Instance Table

Instance Name	Physical Address
TPTC00	4704 010Ch
TPTC01	4706 010Ch

Access Types Legend

Table 4-3099. INTCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	TRDONE	WO	0h	TR Done Event Clear:INTCLR.TRDONE = 0 : Writes of '0' have no effect.INTCLR.TRDONE = 1 : Write of '1' clears INTSTAT.TRDONE bit
0	PROGEMPTY	WO	0h	Program Set Empty Event Clear:INTCLR.PROGEMPTY = 0 : Writes of '0' have no effect.INTCLR.PROGEMPTY = 1 : Write of '1' clears INTSTAT.PROGEMPTY bit

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4.39.8 TPTC0n_INTCMD Registers

4.39.8.1 TPTC0n_INTCMD Register (Offset = 110h) [reset = h]

Short Description: Interrupt Command Register

Long Description:

Return to Summary Table

Table 4-3100. Instance Table

Instance Name	Physical Address
TPTC00	4704 0110h
TPTC01	4706 0110h

Access Types Legend

Table 4-3101. INTCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	SET	WO	0h	Set TPTC interrupt:Write of '1' to SET causes TPTC interrupt to be pulsed unconditionally.Writes of '0' have no affect.
0	EVAL	WO	0h	Evaluate state of TPTC interruptWrite of '1' to EVAL causes TPTC interrupt to be pulsed if any of the INTSTAT bits are set to '1'.Writes of '0' have no affect.

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4.39.9 TPTC0n_ERRSTAT Registers

4.39.9.1 TPTC0n_ERRSTAT Register (Offset = 120h) [reset = h]

Short Description: Error Status Register

Long Description:

Return to Summary Table

Table 4-3102. Instance Table

Instance Name	Physical Address
TPTC00	4704 0120h
TPTC01	4706 0120h

Access Types Legend

Table 4-3103. ERRSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	MMRAERR	RO	0h	MMR Address Error:MMRAERR = 0 : Condition not detected.MMRAERR = 1 : User attempted to read or write to invalid address configuration memory map. [Is only be set for non-emulation accesses]. No additional error information is recorded.
2	TRERR	RO	0h	TR Error:TR detected that violates FIFO Mode transfer [SAM or DAM is '1'] alignment rules or has ACNT or BCNT == 0. No additional error information is recorded.
	RESERVED	NONE		Reserved
0	BUSERR	RO	0h	Bus Error Event:BUSERR = 0: Condition not detected.BUSERR = 1: TC has detected an error code on the write response bus or read response bus. Error information is stored in Error Details Register [ERRDET].

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4.39.10 TPTC0n_ERREN Registers

4.39.10.1 TPTC0n_ERREN Register (Offset = 124h) [reset = h]

Short Description: Error Enable Register

Long Description:

Return to Summary Table

Table 4-3104. Instance Table

Instance Name	Physical Address
TPTC00	4704 0124h
TPTC01	4706 0124h

Access Types Legend

Table 4-3105. ERREN Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	MMRAERR	RW	0h	Interrupt enable for ERRSTAT.MMRAERR:ERREN.MMRAERR = 0 : BUSERR is disabled.ERREN.MMRAERR = 1 : MMRAERR is enabled and contributes to the TPTC error interrupt generation.
2	TRERR	RW	0h	Interrupt enable for ERRSTAT.TRERR:ERREN.TRERR = 0 : BUSERR is disabled.ERREN.TRERR = 1 : TRERR is enabled and contributes to the TPTC error interrupt generation.
	RESERVED	NONE		Reserved
0	BUSERR	RW	0h	Interrupt enable for ERRSTAT.BUSERR:ERREN.BUSERR = 0 : BUSERR is disabled.ERREN.BUSERR = 1 : BUSERR is enabled and contributes to the TPTC error interrupt generation.

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4.39.11 TPTC0n_ERRCLR Registers

4.39.11.1 TPTC0n_ERRCLR Register (Offset = 128h) [reset = h]

Short Description: Error Clear Register

Long Description:

Return to Summary Table

Table 4-3106. Instance Table

Instance Name	Physical Address
TPTC00	4704 0128h
TPTC01	4706 0128h

Access Types Legend

Table 4-3107. ERRCLR Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
3	MMRAERR	WO	0h	Interrupt clear for ERRSTAT.MMRAERR:ERRCLR.MMRAERR = 0 : Writes of '0' have no effect.ERRCLR.MMRAERR = 1 : Write of '1' clears ERRSTAT.MMRAERR bit. Write of '1' to ERRCLR.MMRAERR does not clear the ERRDET register.
2	TRERR	WO	0h	Interrupt clear for ERRSTAT.TRERR:ERRCLR.TRERR = 0 : Writes of '0' have no effect.ERRCLR.TRERR = 1 : Write of '1' clears ERRSTAT.TRERR bit. Write of '1' to ERRCLR.TRERR does not clear the ERRDET register.
	RESERVED	NONE		Reserved
0	BUSERR	WO	0h	Interrupt clear for ERRSTAT.BUSERR:ERRCLR.BUSERR = 0 : Writes of '0' have no effect.ERRCLR.BUSERR = 1 : Write of '1' clears ERRSTAT.BUSERR bit. Write of '1' to ERRCLR.BUSERR clears the ERRDET register.

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4.39.12 TPTC0n_ERRDET Registers

4.39.12.1 TPTC0n_ERRDET Register (Offset = 12Ch) [reset = h]

Short Description: Error Details Register

Long Description:

Return to Summary Table

Table 4-3108. Instance Table

Instance Name	Physical Address
TPTC00	4704 012Ch
TPTC01	4706 012Ch

Access Types Legend

Table 4-3109. ERRDET Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
17	TCCHEN	RO	0h	Contains the OPT.TCCHEN value programmed by the user for the Read or Write transaction that resulted in an error.
16	TCINTEN	RO	0h	Contains the OPT.TCINTEN value programmed by the user for the Read or Write transaction that resulted in an error.
	RESERVED	NONE		Reserved
13 - 8	TCC	RO	0h	Transfer Complete Code: Contains the OPT.TCC value programmed by the user for the Read or Write transaction that resulted in an error.
	RESERVED	NONE		Reserved
3 - 0	STAT	RO	0h	Transaction Status:Stores the non-zero status/error code that was detected on the read status or write status bus.MS-bit effectively serves as the read vs. write error code.If read status and write status are returned on the same cycle then the TC chooses non-zero version. If both are non-zero then write status is treated as higher priority.Encoding of errors matches the CBA spec.

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4.39.13 TPTC0n_ERRCMD Registers

4.39.13.1 TPTC0n_ERRCMD Register (Offset = 130h) [reset = h]

Short Description: Error Command Register

Long Description:

Return to Summary Table

Table 4-3110. Instance Table

Instance Name	Physical Address
TPTC00	4704 0130h
TPTC01	4706 0130h

Access Types Legend

Table 4-3111. ERRCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
1	SET	WO	0h	Set TPTC error interrupt:Write of '1' to SET causes TPTC error interrupt to be pulsed unconditionally.Writes of '0' have no affect.
0	EVAL	WO	0h	Evaluate state of TPTC error interruptWrite of '1' to EVAL causes TPTC error interrupt to be pulsed if any of the ERRSTAT bits are set to '1'.Writes of '0' have no affect.

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4.39.14 TPTC0n_RDRATE Registers

4.39.14.1 TPTC0n_RDRATE Register (Offset = 140h) [reset = h]

Short Description: Read Rate Register

Long Description:

Return to Summary Table

Table 4-3112. Instance Table

Instance Name	Physical Address
TPTC00	4704 0140h
TPTC01	4706 0140h

Access Types Legend

Table 4-3113. RDRATE Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
2 - 0	RDRATE	RW	0h	Read Rate Control: Controls the number of cycles between read commands. This is a global setting that applies to all TRs for this TC.

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4.39.15 TPTC0n_POPT Registers

4.39.15.1 TPTC0n_POPT Register (Offset = 200h) [reset = h]

Short Description: Prog Set Options

Long Description:

Return to Summary Table

Table 4-3114. Instance Table

Instance Name	Physical Address
TPTC00	4704 0200h
TPTC01	4706 0200h

Access Types Legend

Table 4-3115. POPT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

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4.39.16 TPTC0n_PSRC Registers

4.39.16.1 TPTC0n_PSRC Register (Offset = 204h) [reset = h]

Short Description: Prog Set Src Address

Long Description:

Return to Summary Table

Table 4-3116. Instance Table

Instance Name	Physical Address
TPTC00	4704 0204h
TPTC01	4706 0204h

Access Types Legend

Table 4-3117. PSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RW	0h	Source address for Program Register Set

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4.39.17 TPTC0n_PCNT Registers

4.39.17.1 TPTC0n_PCNT Register (Offset = 208h) [reset = h]

Short Description: Prog Set Count

Long Description:

Return to Summary Table

Table 4-3118. Instance Table

Instance Name	Physical Address
TPTC00	4704 0208h
TPTC01	4706 0208h

Access Types Legend

Table 4-3119. PCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	BCNT	RW	0h	B-Dimension count. Number of arrays to be transferred where each array is ACNT in length.
15 - 0	ACNT	RW	0h	A-Dimension count. Number of bytes to be transferred in first dimension.

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4.39.18 TPTC0n_PDST Registers

4.39.18.1 TPTC0n_PDST Register (Offset = 20Ch) [reset = h]

Short Description: Prog Set Dst Address

Long Description:

Return to Summary Table

Table 4-3120. Instance Table

Instance Name	Physical Address
TPTC00	4704 020Ch
TPTC01	4706 020Ch

Access Types Legend

Table 4-3121. PDST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RW	0h	Destination address for Program Register Set

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4.39.19 TPTC0n_PBIDX Registers

4.39.19.1 TPTC0n_PBIDX Register (Offset = 210h) [reset = h]

Short Description: Prog Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-3122. Instance Table

Instance Name	Physical Address
TPTC00	4704 0210h
TPTC01	4706 0210h

Access Types Legend

Table 4-3123. PBIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RW	0h	Dest B-Idx for Program Register Set:B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RW	0h	Source B-Idx for Program Register Set:B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

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4.39.20 TPTC0n_PMPPRXY Registers

4.39.20.1 TPTC0n_PMPPRXY Register (Offset = 214h) [reset = h]

Short Description: Prog Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-3124. Instance Table

Instance Name	Physical Address
TPTC00	4704 0214h
TPTC01	4706 0214h

Access Types Legend

Table 4-3125. PMPPRXY Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

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4.39.21 TPTC0n_SAOPT Registers

4.39.21.1 TPTC0n_SAOPT Register (Offset = 240h) [reset = h]

Short Description: Src Actv Set Options

Long Description:

Return to Summary Table

Table 4-3126. Instance Table

Instance Name	Physical Address
TPTC00	4704 0240h
TPTC01	4706 0240h

Access Types Legend

Table 4-3127. SAOPT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

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4.39.22 TPTC0n_SASRC Registers

4.39.22.1 TPTC0n_SASRC Register (Offset = 244h) [reset = h]

Short Description: Src Actv Set Src Address

Long Description:

Return to Summary Table

Table 4-3128. Instance Table

Instance Name	Physical Address
TPTC00	4704 0244h
TPTC01	4706 0244h

Access Types Legend

Table 4-3129. SASRC Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RO	0h	Source address for Source Active Register Set

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4.39.23 TPTC0n_SACNT Registers

4.39.23.1 TPTC0n_SACNT Register (Offset = 248h) [reset = h]

Short Description: Src Actv Set A-Count

Long Description:

Return to Summary Table

Table 4-3130. Instance Table

Instance Name	Physical Address
TPTC00	4704 0248h
TPTC01	4706 0248h

Access Types Legend

Table 4-3131. SACNT Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 0	ACNT	RO	0h	A-Dimension count. Number of bytes to be transferred in first dimension.

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4.39.24 TPTC0n_SADST Registers

4.39.24.1 TPTC0n_SADST Register (Offset = 24Ch) [reset = h]

Short Description: Src Actv Set Dst Address

Long Description:

Return to Summary Table

Table 4-3132. Instance Table

Instance Name	Physical Address
TPTC00	4704 024Ch
TPTC01	4706 024Ch

Access Types Legend

Table 4-3133. SADST Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RO	0h	Destination address for Source Active Register Set

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4.39.25 TPTC0n_SABIDX Registers

4.39.25.1 TPTC0n_SABIDX Register (Offset = 250h) [reset = h]

Short Description: Src Actv Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-3134. Instance Table

Instance Name	Physical Address
TPTC00	4704 0250h
TPTC01	4706 0250h

Access Types Legend

Table 4-3135. SABIDX Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RO	0h	Dest B-Idx for Source Active Register Set:B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RO	0h	Source B-Idx for Source Active Register Set:B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

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4.39.26 TPTC0n_SAMPPRXY Registers

4.39.26.1 TPTC0n_SAMPPRXY Register (Offset = 254h) [reset = h]

Short Description: Src Actv Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-3136. Instance Table

Instance Name	Physical Address
TPTC00	4704 0254h
TPTC01	4706 0254h

Access Types Legend

Table 4-3137. SAMPPRXY Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

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4.39.27 TPTC0n_SACNTRLD Registers

4.39.27.1 TPTC0n_SACNTRLD Register (Offset = 258h) [reset = h]

Short Description: Src Actv Set Cnt Reload

Long Description:

Return to Summary Table

Table 4-3138. Instance Table

Instance Name	Physical Address
TPTC00	4704 0258h
TPTC01	4706 0258h

Access Types Legend

Table 4-3139. SACNTRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	ACNTRLD	RO	0h	A-Cnt Reload value for Source Active Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT.The Reload value is used to reinitialize ACNT after each array is serviced [i.e. ACNT decrements to 0]. by the Src offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT bytes]

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4.39.28 TPTC0n_SASRCBREF Registers

4.39.28.1 TPTC0n_SASRCBREF Register (Offset = 25Ch) [reset = h]

Short Description: Src Actv Set Src Addr B-Reference

Long Description:

Return to Summary Table

Table 4-3140. Instance Table

Instance Name	Physical Address
TPTC00	4704 025Ch
TPTC01	4706 025Ch

Access Types Legend

Table 4-3141. SASRCBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDRBREF	RO	0h	Source address reference for Source Active Register Set:Represents the starting address for the array currently being read. The next array's starting address is calculated as the 'reference address' plus the 'source b-idx' value.

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4.39.29 TPTC0n_SADSTBREF Registers

4.39.29.1 TPTC0n_SADSTBREF Register (Offset = 260h) [reset = h]

Short Description: Src Actv Set Dst Addr B-Reference

Long Description:

Return to Summary Table

Table 4-3142. Instance Table

Instance Name	Physical Address
TPTC00	4704 0260h
TPTC01	4706 0260h

Access Types Legend

Table 4-3143. SADSTBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDRBREF	RO	0h	Dst address reference is not applicable for Src Active Register Set. Reads return 0x0.

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4.39.30 TPTC0n_SABCNT Registers

4.39.30.1 TPTC0n_SABCNT Register (Offset = 264h) [reset = h]

Short Description: Src Actv Set B-Count

Long Description:

Return to Summary Table

Table 4-3144. Instance Table

Instance Name	Physical Address
TPTC00	4704 0264h
TPTC01	4706 0264h

Access Types Legend

Table 4-3145. SABCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BCNT	RO	0h	B-Dimension count:Number of arrays to be transferred where each array is ACNT in length.Count Remaining for Src Active Register Set. Represents the amount of data remaining to be read. Initial value is copied from PCNT. TC decrements ACNT and BCNT as necessary after each read command is issued. Final value should be 0 when TR is complete.

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4.39.31 TPTC0n_DFCNTRLD Registers

4.39.31.1 TPTC0n_DFCNTRLD Register (Offset = 280h) [reset = h]

Short Description: Dst FIFO Set Cnt Reload

Long Description:

Return to Summary Table

Table 4-3146. Instance Table

Instance Name	Physical Address
TPTC00	4704 0280h
TPTC01	4706 0280h

Access Types Legend

Table 4-3147. DFCNTRLD Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	ACNTRLD	RO	0h	A-Cnt Reload value for Destination FIFO Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT.The Reload value is used to reinitialize ACNT after each array is serviced [i.e. ACNT decrements to 0]. by the Src offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT bytes]

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4.39.32 TPTC0n_DFSRCBREF Registers

4.39.32.1 TPTC0n_DFSRCBREF Register (Offset = 284h) [reset = h]

Short Description: Dst FIFO Set Src Addr B-Reference

Long Description:

Return to Summary Table

Table 4-3148. Instance Table

Instance Name	Physical Address
TPTC00	4704 0284h
TPTC01	4706 0284h

Access Types Legend

Table 4-3149. DFSRCBREF Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDRBREF	RO	0h	Source address reference for Destination FIFO Register Set:Represents the starting address for the array currently being read. The next array's starting address is calculated as the 'reference address' plus the 'source b-idx' value.

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4.39.33 TPTC0n_DFOPT0 Registers

4.39.33.1 TPTC0n_DFOPT0 Register (Offset = 300h) [reset = h]

Short Description: Dst FIFO Set Options

Long Description:

Return to Summary Table

Table 4-3150. Instance Table

Instance Name	Physical Address
TPTC00	4704 0300h
TPTC01	4706 0300h

Access Types Legend

Table 4-3151. DFOPT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

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4.39.34 TPTC0n_DFSRC0 Registers

4.39.34.1 TPTC0n_DFSRC0 Register (Offset = 304h) [reset = h]

Short Description: Dst FIFO Set Src Address

Long Description:

Return to Summary Table

Table 4-3152. Instance Table

Instance Name	Physical Address
TPTC00	4704 0304h
TPTC01	4706 0304h

Access Types Legend

Table 4-3153. DFSRC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RO	0h	Source address is not applicable for Dst FIFO Register Set: Reads return 0x0.

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4.39.35 TPTC0n_DFACNT0 Registers

4.39.35.1 TPTC0n_DFACNT0 Register (Offset = 308h) [reset = h]

Short Description: Dst FIFO Set A-Count

Long Description:

Return to Summary Table

Table 4-3154. Instance Table

Instance Name	Physical Address
TPTC00	4704 0308h
TPTC01	4706 0308h

Access Types Legend

Table 4-3155. DFACNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 0	ACNT	RO	0h	A-Dimension count. Number of bytes to be transferred infirst dimension.

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4.39.36 TPTC0n_DFDST0 Registers

4.39.36.1 TPTC0n_DFDST0 Register (Offset = 30Ch) [reset = h]

Short Description: Dst FIFO Set Dst Address

Long Description:

Return to Summary Table

Table 4-3156. Instance Table

Instance Name	Physical Address
TPTC00	4704 030Ch
TPTC01	4706 030Ch

Access Types Legend

Table 4-3157. DFDST0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RO	0h	Destination address for Dst FIFO Register Set:Initial value is copied from PDST.DADDR.TC updates value according to destination addressing mode [OPT.SAM] and/or dest index value [BIDX.DBIDX] after each write command is issued.When a TR is complete the final value should be the address of the last write command issued.

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4.39.37 TPTC0n_DFBIDX0 Registers

4.39.37.1 TPTC0n_DFBIDX0 Register (Offset = 310h) [reset = h]

Short Description: Dst FIFO Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-3158. Instance Table

Instance Name	Physical Address
TPTC00	4704 0310h
TPTC01	4706 0310h

Access Types Legend

Table 4-3159. DFBIDX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RO	0h	Dest B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements].DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RO	0h	Src B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements].SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

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4.39.38 TPTC0n_DFMPPRXY0 Registers

4.39.38.1 TPTC0n_DFMPPRXY0 Register (Offset = 314h) [reset = h]

Short Description: Dst FIFO Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-3160. Instance Table

Instance Name	Physical Address
TPTC00	4704 0314h
TPTC01	4706 0314h

Access Types Legend

Table 4-3161. DFMPPRXY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

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4.39.39 TPTC0n_DFBCNT0 Registers

4.39.39.1 TPTC0n_DFBCNT0 Register (Offset = 318h) [reset = h]

Short Description: Dst FIFO Set B-Count

Long Description:

Return to Summary Table

Table 4-3162. Instance Table

Instance Name	Physical Address
TPTC00	4704 0318h
TPTC01	4706 0318h

Access Types Legend

Table 4-3163. DFBCNT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BCNT	RO	0h	B-Count Remaining for Dst Register Set:Number of arrays to be transferred where each array is ACNT in length.Represents the amount of data remaining to be written.Initial value is copied from PCNT.TC decrements ACNT and BCNT as necessary after each write dataphase is issued. Final value should be 0 when TR is complete.

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4.39.40 TPTC0n_DFOPT1 Registers

4.39.40.1 TPTC0n_DFOPT1 Register (Offset = 340h) [reset = h]

Short Description: Dst FIFO Set Options

Long Description:

Return to Summary Table

Table 4-3164. Instance Table

Instance Name	Physical Address
TPTC00	4704 0340h
TPTC01	4706 0340h

Access Types Legend

Table 4-3165. DFOPT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
29 - 28	DBG_ID	RW	0h	Debug IDValue driven on the read (tptc_r_dbg_channel_id) and write (tptc_w_dbg_channel_id) command bus.Used at system level for trace/profiling of user selected transfers in systems that include this feature.
	RESERVED	NONE		Reserved
22	TCCHEN	RW	0h	Transfer complete chaining enable:0: Transfer complete chaining is disabled.1: Transfer complete chaining is enabled.
	RESERVED	NONE		Reserved
20	TCINTEN	RW	0h	Transfer complete interrupt enable:0: Transfer complete interrupt is disabled.1: Transfer complete interrupt is enabled.
	RESERVED	NONE		Reserved
17 - 12	TCC	RW	0h	Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.
	RESERVED	NONE		Reserved
10 - 8	FWID	RW	0h	FIFO width control: Applies if either SAM or DAM is set to FIFO mode.
	RESERVED	NONE		Reserved
6 - 4	PRI	RW	0h	Transfer Priority:0: Priority 0 - Highest priority1: Priority 1 ...7: Priority 7 - Lowest priority
	RESERVED	NONE		Reserved
1	DAM	RW	0h	Destination Address Mode within an array:0: INCR Dst addressing within an array increments.1: FIFO Dst addressing within an array wraps around upon reaching FIFO width.
0	SAM	RW	0h	Source Address Mode within an array:0: INCR Src addressing within an array increments.1: FIFO Src addressing within an array wraps around upon reaching FIFO width.

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4.39.41 TPTC0n_DFSRC1 Registers

4.39.41.1 TPTC0n_DFSRC1 Register (Offset = 344h) [reset = h]

Short Description: Dst FIFO Set Src Address

Long Description:

Return to Summary Table

Table 4-3166. Instance Table

Instance Name	Physical Address
TPTC00	4704 0344h
TPTC01	4706 0344h

Access Types Legend

Table 4-3167. DFSRC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	SADDR	RO	0h	Source address is not applicable for Dst FIFO Register Set: Reads return 0x0.

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4.39.42 TPTC0n_DFACNT1 Registers

4.39.42.1 TPTC0n_DFACNT1 Register (Offset = 348h) [reset = h]

Short Description: Dst FIFO Set A-Count

Long Description:

Return to Summary Table

Table 4-3168. Instance Table

Instance Name	Physical Address
TPTC00	4704 0348h
TPTC01	4706 0348h

Access Types Legend

Table 4-3169. DFACNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
22 - 0	ACNT	RO	0h	A-Dimension count. Number of bytes to be transferred infirst dimension.

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4.39.43 TPTC0n_DFDST1 Registers

4.39.43.1 TPTC0n_DFDST1 Register (Offset = 34Ch) [reset = h]

Short Description: Dst FIFO Set Dst Address

Long Description:

Return to Summary Table

Table 4-3170. Instance Table

Instance Name	Physical Address
TPTC00	4704 034Ch
TPTC01	4706 034Ch

Access Types Legend

Table 4-3171. DFDST1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 0	DADDR	RO	0h	Destination address for Dst FIFO Register Set:Initial value is copied from PDST.DADDR.TC updates value according to destination addressing mode [OPT.SAM] and/or dest index value [BIDX.DBIDX] after each write command is issued.When a TR is complete the final value should be the address of the last write command issued.

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4.39.44 TPTC0n_DFBIDX1 Registers

4.39.44.1 TPTC0n_DFBIDX1 Register (Offset = 350h) [reset = h]

Short Description: Dst FIFO Set B-Dim Idx

Long Description:

Return to Summary Table

Table 4-3172. Instance Table

Instance Name	Physical Address
TPTC00	4704 0350h
TPTC01	4706 0350h

Access Types Legend

Table 4-3173. DFBIDX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31 - 16	DBIDX	RO	0h	Dest B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements].DBIDX is always used regardless of whether DAM is Increment or FIFO mode.
15 - 0	SBIDX	RO	0h	Src B-Idx for Dest FIFO Register Set.Value copied from PBIDX: B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements].SBIDX is always used regardless of whether SAM is Increment or FIFO mode.

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4.39.45 TPTC0n_DFMPPRXY1 Registers

4.39.45.1 TPTC0n_DFMPPRXY1 Register (Offset = 354h) [reset = h]

Short Description: Dst FIFO Set Mem Protect Proxy

Long Description:

Return to Summary Table

Table 4-3174. Instance Table

Instance Name	Physical Address
TPTC00	4704 0354h
TPTC01	4706 0354h

Access Types Legend

Table 4-3175. DFMPPRXY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
	RESERVED	NONE		Reserved
9	SECURE	RO	0h	Secure Level: Deprecated, always read as 0.
8	PRIV	RO	0h	Privilege Level:PRIV = 0 : User level privilegePRIV = 1 : Supervisor level privilegePMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction.
	RESERVED	NONE		Reserved
3 - 0	PRIVID	RO	0h	Privilege ID:PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values.The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.

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4.39.46 TPTC0n_DFBCNT1 Registers

4.39.46.1 TPTC0n_DFBCNT1 Register (Offset = 358h) [reset = h]

Short Description: Dst FIFO Set B-Count

Long Description:

Return to Summary Table

Table 4-3176. Instance Table

Instance Name	Physical Address
TPTC00	4704 0358h
TPTC01	4706 0358h

Access Types Legend

Table 4-3177. DFBCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15 - 0	BCNT	RO	0h	B-Count Remaining for Dst Register Set:Number of arrays to be transferred where each array is ACNT in length.Represents the amount of data remaining to be written.Initial value is copied from PCNT.TC decrements ACNT and BCNT as necessary after each write dataphase is issued. Final value should be 0 when TR is complete.

4.39.47 Access Table

Table 4-3178. Access Type Codes

Access Type	Code	Description
RO	RO	Read
RW	RW	Read / Write
WO	WO	Write

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from October 1, 2022 to December 15, 2022 (from Revision B (October 2022) to Revision C (November 2022)) **Page**

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