User's Guide

Migration Between TMS320F28P5xx and TMS320F280013x/TMS320F280015

ABSTRACT

This migration guide describes the hardware and software differences to be aware of when moving between F280013x/15x and F28P55x C2000™ real-time MCUs. This document shows the block diagram between the two MCUs as a visual representation on what blocks are similar or different. It also highlights the features that are unique between the two devices for all available packages in a device comparison table. The F280013x and F28P55x devices have one package in common 64-pin PM. The F280015x and F28P55x devices have two packages in common; 80-pin PN and 64-pin PM so a PCB hardware section has been added to aid in migration between the three common packages. The digital general-purpose input/output (GPIO) and analog multiplex comparison tables show pin functionality between the two MCUs. This is a good reference for hardware design and signal routing when considering a move between the two devices. Lastly, like the F280013x/15x device, the F28P55x software support is only in EABI format.

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1 Feature Differences Between F280013x/15x and F28P55x

F28P55x is a superset of F280013x/15x. The F280013x and F28P55x devices have one package in common; a 64-pin PM. The F280015x and F28P55x devices have two packages in common; 80-pin PN and 64-pin PM It is possible to migrate between F280013x/15x and F28P55x with the caveats in this document taken into account.

Note

This comparison guide focuses on the super-set devices: F2800137/157 and F28P55xSJ9. Other part numbers in this product family have reduced feature support. For details specific to part numbers, see the device-specific data sheet.

1.1 F280013x/15x and F28P55x Feature Comparison

An overlaid block diagram of F280013x/15x and F28P55x is shown in Figure 1-1 while feature comparison of the superset part numbers for the F280013x/15x and F28P55x devices is shown in Table 1-1 .

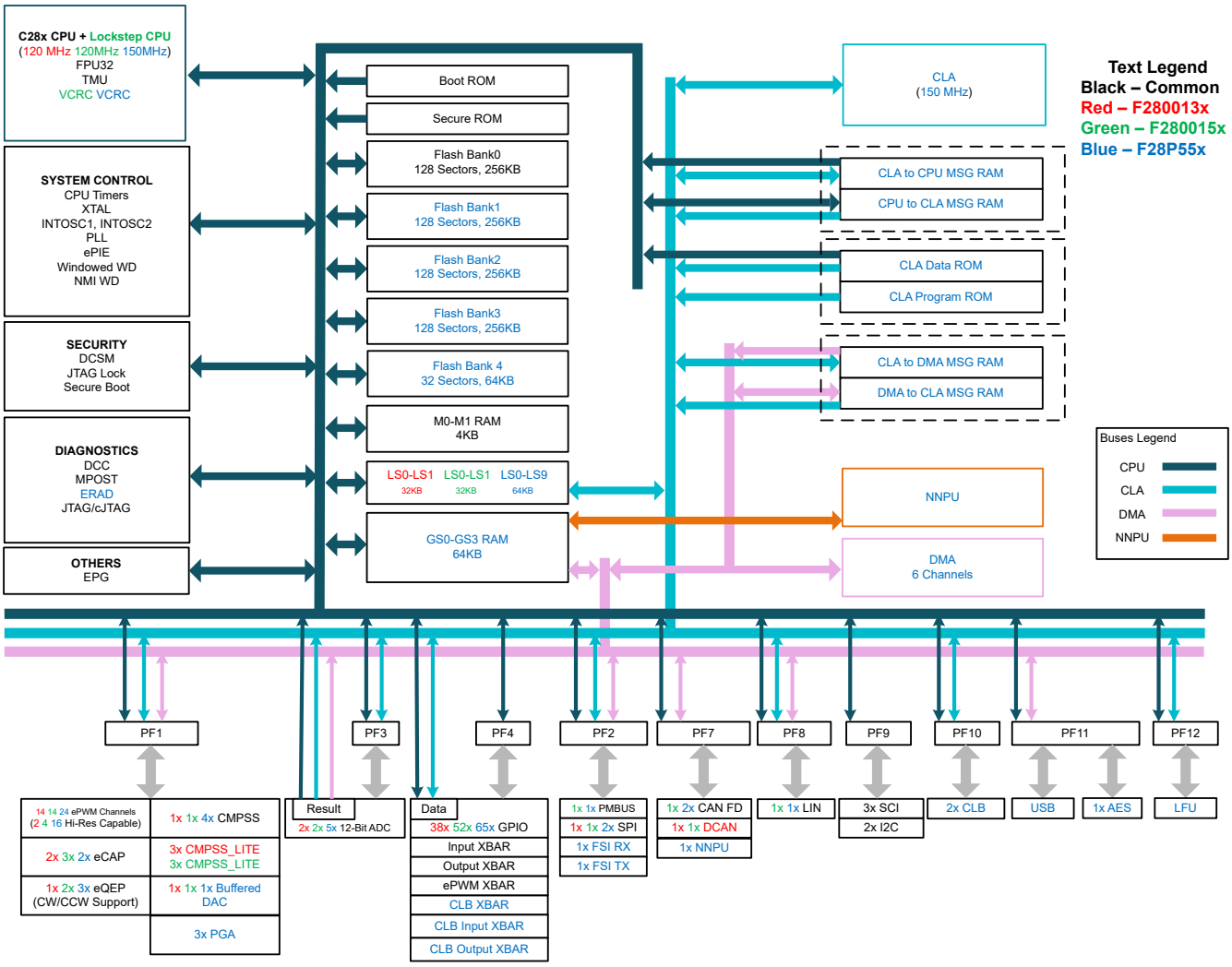

Figure 1-1. F280013x/15x and F28P55x Overlaid Functional Block Diagram

Table 1-1. IP Differences

Feature		F280013x	F280015x	F28P55x
CPU Frequency (MHz)		120	120	150
Memory				
Flash		256KB	256KB	1088KB
RAM	Local Shared	32KB	32KB	64KB
	Global Shared	-	-	64KB
System				
Control Law Accelerator (CLA)		-	-	1
Configurable Logic Block (CLB)		-	-	2 Tiles
Motor Control Libraries in ROM		Yes	Yes	No
ERAD		-	-	1 - Type 1
AES		-	-	1 - Type 0
LFU		-	-	Yes
DMA		-	-	Yes
Neural-Network Processing Unit (NNPU)		-	-	1 - Type 0
Analog Peripherals				
ADC 12-bit	Number of ADCs	2 - Type 5	2 - Type 5	5- Type 6
	MSPS	4	4	4
	Conversion Time (ns)	250	250	186.67
CMPSS		1 - Type 3	1 - Type 5	4 - Type 6
CMPSS_LITE		3 - Type 0	3 - Type 0	-
Buffered DAC		-	-	1 - Type 2
Programmable Gain Amplifier (PGA)		-	-	3 - Type 2
Output DAC from CMPSS DACL		1	1	1
Control Peripherals				
eCAP/HRCAP Modules		2 - Type 2	3 - Type 2	2 - Type 2
ePWM/HRPWM channels - Type 4		14 (2 with HRPWM)	14 (4 with HRPWM)	24 (16 with HRPWM)
eQEP - Type 2		1	2	3
Communications Peripherals				
CAN (DCAN) - Type 0		1	1	-
CANFD (MCAN) - Type 1		1	1	2
I2C		2 - Type 1	2 - Type 1	2 - Type 2
LIN - Type 1		-	1	1
PMBUS		-	1 - Type 1	1 - Type 2
SCI - Type 0		3	3	3
FSI		-	-	1 - Type 2
USB		-	-	1- Type 0

Table 1-2. 80-pin IO and Analog Channel Counts

IO Type	F280015x	F28P55x
Digital		
AIO (analog with digital inputs)	10	12
AGPIO (analog with digital inputs and outputs)	11	16
Additional GPIO	4 (2 from cJTAG and 2 from X1/X2)	4 (2 from cJTAG and 2 from X1/X2)
Standard GPIO	37	32
Total GPIO	52	52
Total GPIO + AIO	62	64
Analog		
ADC Channels (single-ended)	21	28

Table 1-3. 64-pin IO and Analog Channel Counts

IO Type	F280013x	F280013xV/15x	F28P55x
Digital			
AIO (analog with digital inputs)	10	10	12
AGPIO (analog with digital inputs and outputs)	11	11	16
Additional GPIO	4 (2 from cJTAG and 2 from X1/X2)	4 (2 from cJTAG and 2 from X1/X2)	4 (2 from cJTAG and 2 from X1/X2)
Standard GPIO	23	22	17
Total GPIO	38	37	37
Total GPIO + AIO	48	47	49
Analog			
ADC Channels (single-ended)	21	21	28

2 PCB Hardware Changes

The F280013x and F28P55x device have one package in common: a 64-pin PM. The F280015x and F28P55x device have two packages in common: 80-pin PNA/PN, 64-pin PM. The following sections describe the pin migration in detail.

Note

Overall compatibility depends on more than just the pins. Review all of the changes in this document during the migration process.

Also Note that the 80pin PNA on the F28P55x has 0.4mm pin pitch vs the PN on the F280015x has 0.5mm pin pitch

2.1 PCB Hardware Changes for the 80-Pin PN/PNA, 64-Pin PM Packages

This section describes the F280013x/15x and F28P55x differences that exist between the 80-Pin PN/PNA, 64-Pin PM packages.

80-Pin PN/PNA: Figure 2-1 outlines the differences. Please note that the package pitch is changed with the F280015x having a 0.5mm pin pitch and the F28P55x having a 0.4mm pin pitch.

64-Pin PM: The 13xV variant and all 15x devics have VREGENZ pin where the non V devices do not. All F28P55x devices have a VREGENZ pin. 64-Pin PM F280013x/15x and F28P55x Pin-Overlay outlines the differences.

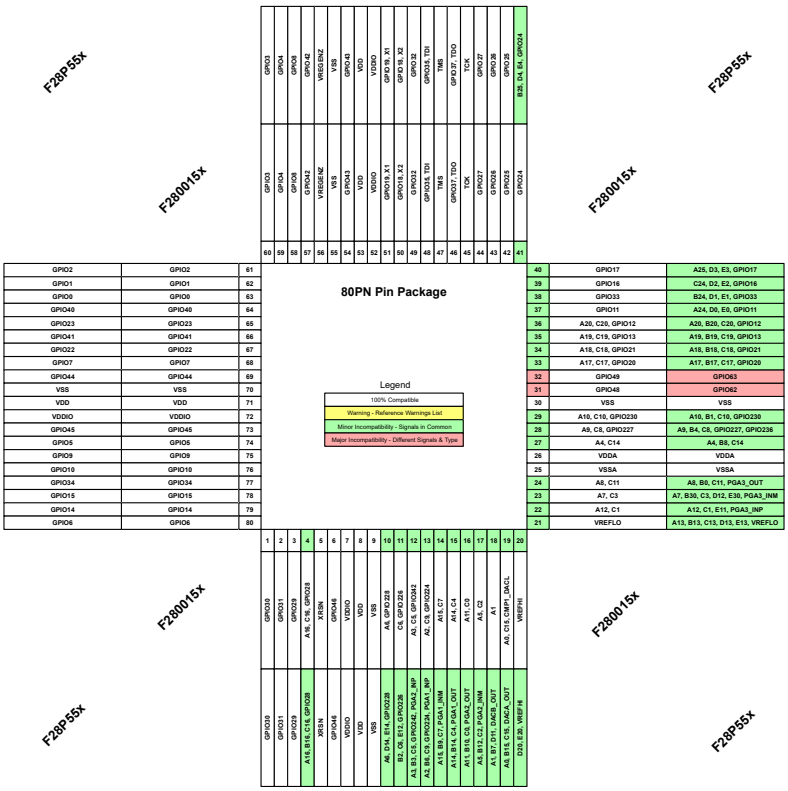

Figure 2-1. 80-Pin PN/PNA, F280015x and F28P55x Pin-Overlay

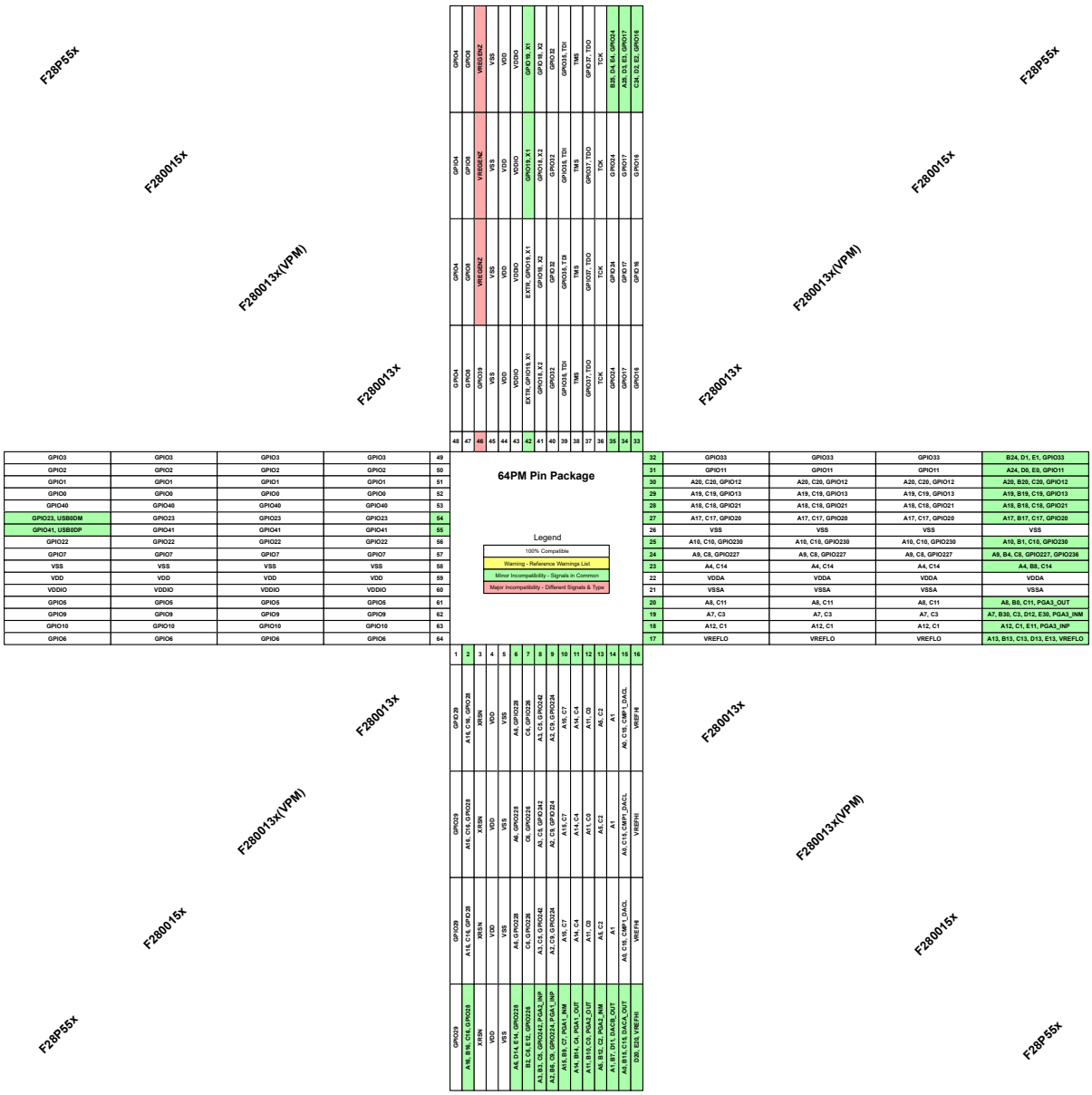

Figure 2-2. 64-Pin PM F280013x/15x and F28P55x Pin-Overlay

2.2 80-Pin PNA, 64-Pin PM Migration Between F280013x/15x and F28P55x For New and Existing PCB

For the color legend, see Figure 2-1 and Figure 2-2.

Table 2-1. 80-Pin PNA and 64-Pin PM Migration Between F280013x/15x and F28P55x For New and Existing PCB

Pin No		Pin Name			Action
80	64	F280013x/15	F28P55x	Transition Type	F280013x/15 to F28P55x
Minor Incompatibility - Signals in Common [1]					
4	2	A16, C16, GPIO28	A16, B16, C16, GPIO28		Use A16, C16, GPIO28
10	6	A6, GPIO228	A6, D14, E14, GPIO228		Use A6 or GPIO228
11	7	C6, GPIO226	B2, C6, E12, GPIO226		Use C6 or GPIO226
12	8	A3, C5, GPIO224	A3, B3, C5 GPIO242, PGA2_INP		Use A3, C5 or GPIO224
13	9	A2, C9, GPIO224	A2, B6, C9, GPIO224, PGA1_INP		Use A2, C9, GPIO224
14	10	A15, C7	A15, B9, C7, PGA1_INM		Use A15 or C7
15	11	A14, C4	A14, B14, C4, PGA1_OUT		Use A14 or C4
16	12	A11, C0	A11, B10, C0, PGA2_OUT		Use A11 or C0
17	13	A5, C2	A5, B12, C2, PGA2_INM		Use A5 or C2
18	14	A1	A1, B7, D11, DACB_OUT		Use A1
19	15	A0, C15, CMP1_DACL	A0, B15, C15, DACA_OUT		Use A0, C15, or DACA_OUT
20	16	VREFHI	D20, E20, VREFHI	Common Analog Channel	Use VREFHI
21	17	VREFLO	A13, B13, C13, D13, E13, VREFLO		Use VREFLO
22	18	A12, C1	A12, C1, E11, PGA3_INP		Use A12 or C1
23	19	A7, C3	A7, B30, C3, D12, E30, PGA3_INM		Use A7 or C3
24	20	A8, C11	A8, B0, C11, PGA3_OUT		Use A8 or C11
27	23	A4, C14	A4, B8, C14		Use A4 or C14
28	24	A9, C8, GPIO227	A9, B4, C8, GPIO227		Use A9, C8, or GPIO227
29	25	A10, C10, GPIO230	A10, B1, C10, GPIO230		Use A10, C10, or GPIO230
33	27	A17, C17, GPIO20	A17, B17, C17, GPIO20		Use A17, C17, or GPIO20
34	28	A18, C18, GPIO21	A18, B18, C18, GPIO21		Use A18, C18, GPIO21
35	29	A19, C19, GPIO13	A19, B19, C19, GPIO13		Use A19, C19, GPIO13
36	30	A20, C20, GPIO12	A20, B20, C20, GPIO12		Use A20, C20, GPIO12
37	31	GPIO11	A24, D0, E0, GPIO11		Use GPIO11
38	32	GPIO33	B24, D1, E1, GPIO33		Use GPIO33
39	33	GPIO16	C24, D2, E2, GPIO16		Use GPIO16
40	34	GPIO17	A25, D3, E3, GPIO17	GPIO to Analog with GPIO	Use GPIO17
41	35	GPIO24	B25, D4, E4, GPIO24		Use GPIO24
65	54	GPIO23	GPIO23, USB0DM		Use GPIO23
66	55	GPIO41	GPIO41, USB0DP		Use GPIO41
31	-	GPIO48	GPIO62	GPIO number change	GPIOMux allows same functions on F28P55x, please see Table 3-12
32	-	GPIO49	GPIO63		

Table 2-1. 80-Pin PNA and 64-Pin PM Migration Between F280013x/15x and F28P55x For New and Existing PCB (continued)

Pin No		Pin Name			Action
80	64	F280013x/15	F28P55x	Transition Type	F280013x/15 to F28P55x
(280013x Only) Major Incompatibility - Different Signals and Types					
-	46	GPIO39	VREGENZ	GPIO removal	External VREG not supported on F280013x device. Tie off with 0-Ohm resistor VSSA or VDDA on F28P55x based on internal VREG use. Replace with 2.2k PU/PD on the F280013x.

(1) Channel to use selected in software.

3 Feature Differences for System Consideration

The differences and similarities that exist when moving between the F280013x/15xx and the F28P55x device is explored in this section.

3.1 New Features in F28P55x

This section outlines features that only exist in the F28P55x device. For details on each of these new features, see the *TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual* (SPRUJ53).

3.1.1 Advance Encryption Standard (AES)

The AES module provides hardware-accelerated data encryption and decryption operations based on a binary key. The AES is a symmetric cipher module that supports a 128-, 192-, or 256-bit key in hardware for encryption and decryption. The AES module is based on a symmetric algorithm, which means that the encryption and decryption keys are identical. To encrypt data means to convert it from plain text to an unintelligible form called cipher text. Decrypting cipher text converts previously encrypted data to its original plain text form. The main features of the AES accelerator are:

AES encrypt and decrypt operations are supported by:

- Galois/Counter mode (GCM), with basic GHASH operation
- Counter mode with CBC-MAC (CCM)
- XTS mode

The following feedback operating modes are available:

- Electronic code book mode (ECB)
- Cipher block chaining mode (CBC)
- Counter mode (CTR)
- Cipher feedback mode (CFB), 128-bit
- F8 mode
- Key sizes: 128, 192, and 256 bits
- Support for CBC_MAC and Fedora 9 (F9) authentication modes
- Basic GHASH operation (when selecting no encryption)
- Key scheduling in hardware
- Support for µDMA transfers
- Fully synchronous design

3.1.2 Universal Serial Bus (USB)

The USB controller operates as a full-speed function controller during point-to-point communications with the USB host. The controller complies with the USB 2.0 standard, which includes SUSPEND and RESUME signaling. The USB controller has thirty-two endpoints, one-half of them being for IN transactions and one-half of them being for OUT transactions. One IN and one OUT endpoint are fixed-function endpoints used for control transfers; the others are defined by firmware. A dynamically sizable FIFO supports queuing multiple packets. Software-controlled connect and disconnect allow flexibility during USB device startup.

3.1.3 Configurable Logic Block (CLB)

The configurable logic block (CLB) is a collection of configurable blocks that can be inter-connected using software to implement custom digital logic functions. The CLB is able to enhance existing peripherals through a set of crossbar interconnections, which provide a high level of connectivity to existing control peripherals such as enhanced pulse width modulators (ePWM), enhanced capture modules (eCAP), and enhanced quadrature encoder pulse modules (eQEP). The crossbars also allow the CLB to be connected to external GPIO pins. In this way, the CLB can be configured to interact with device peripherals to perform small logical functions such as simple PWM generators, or to implement custom serial data exchange protocols.

The CLB peripheral is configured through the CLB tool. For more information on the CLB tool, available examples, application reports, and user's guide, refer to the following location in your C2000WARE package (C2000Ware_2_00_00_03 and higher):

3.1.4 Live Firmware Update (LFU)

The F28P55x device has in-built hardware to facilitate live firmware updates. It supports fast context switching from the old firmware to the new firmware to minimize application downtime when updating the device firmware.

3.1.5 Programmable Gain Amplifier (PGA)

The F28P55x adds 3 Programmable Gain Amplifiers(PGA) inline with the ADC. Supporting unity gain and gains by a factor of 2 from 2 to 64, the PGA can be used to amplify small signal sources to take advantage of the full dynamic range of the on-chip ADC. Post gain filtering is also supported. While the PGA was also on the TMS320F28004x device, this is a new type, please consult the F28P55x documentation for the full feature set supported.

3.1.6 ERAD

The ERAD module is shown in Figure 3-1.

The ERAD enhances the debug and system analysis capabilities of the device external to the CPU. The C28x CPU alone has two analysis resources; Analysis Unit 1 (AU1) and Analysis Unit 2 (AU2). The first analysis unit counts events or monitors address buses. The second analysis unit monitors address and data buses. The two analysis units can be configured for hardware breakpoints or hardware watch points, and additionally the first analysis unit can be configured as a benchmark counter or event counter. The ERAD module further expands this capability to provide additional hardware breakpoints, hardware watch points, and counters for profiling, as well as other advanced features. The ERAD module can be utilized by the debugger, and also by the application software. For many real-time systems, it is not always possible to connect a debugger and perform an intrusive debug. Under these situations, the user's code has the ability to set up and control the ERAD module in order to debug and profile the system without disturbing the end application.

The ERAD module consists of eight enhanced bus comparator (EBC) units and four system event counter (SEC) units. The EBC units monitor buses and generate output events. The SEC units can be used with EBC units to profile and analyze the system. These units are described in detail in the following sections.

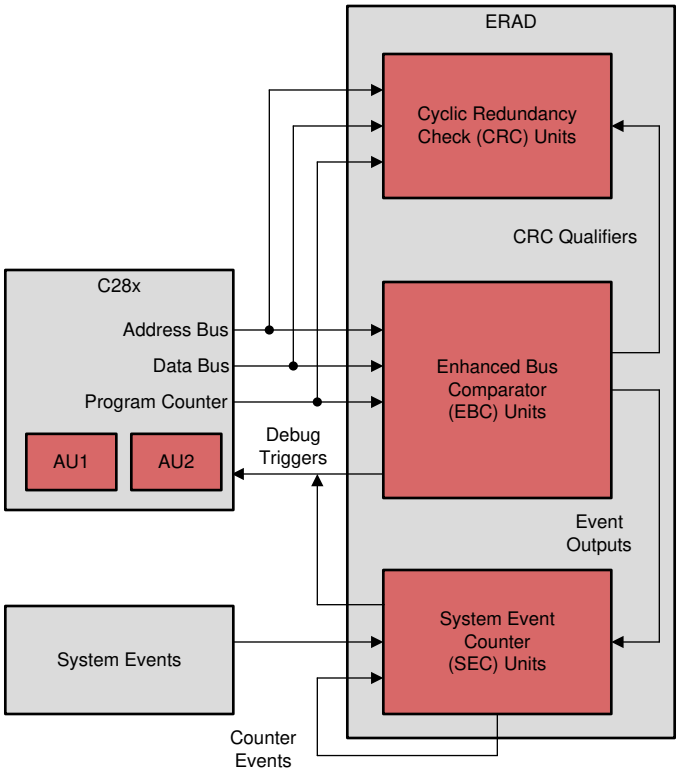

Figure 3-1. ERAD Overview

3.1.7 FSI

The Fast Serial Interface (FSI) module is a serial communication peripheral capable of reliable high-speed communication across isolation devices. Galvanic isolation devices are used in situations where two different electronic circuits, which do not have common power and ground connections, must exchange information. Though isolation devices facilitate these signal communications, they can also introduce a large delay on the signal lines and add skew between the signals. The FSI is designed specifically to ensure reliable high-speed communication for system scenarios that involve communication across isolation barriers without adding components.

The FSI consists of independent transmitter (FSITX) and receiver (FSIRX) cores. The FSITX and FSIRX cores are configured and operated independently.

For additional information on the FSI module, refer to *Fast Serial Interface (FSI) Skew Compensation*.

3.1.8 5V Failsafe IOs

The F28P55x device has four GPIOs: GPIO2, GPIO3, GPIO9, and GPIO32 that support 5V inputs. These pins also support applied voltage prior to power applied to the device.

3.2 Communication Module Changes

Communication module changes between the F280013x/15x and F28P55x devices affect the number of modules, FSI and USB added modules. Details are available in Table 3-1.

Table 3-1. Communication Module Instances

Module	Category	F280013x/15x	F28P55x	Notes
LIN	Number	2 - LINA, LINB	1- LINA	Type 1 LIN on both devices
CAN	Number	1- CANA	-	
MCAN	Number	1 - MCANA(CAN-FD)	2 - MCANA, MCANB(CAN-FD)	
SCI	Number	3 - SCIA, SCIB, SCIC	3 - SCIA, SCIB, SCIC	Type 0 SCI on both devices
SPI	Number	1 - SPIA, SPIB	2 - SPIA, SPIB	Type 2 SPI on both devices
	HW		High Speed Mode Support	GPIO2, 3, 9, 21, 32, and 41 do not support High Speed SPI mode.
I2C	Number	2 -I2CA, I2CB	2 - I2CA, I2CB	F280013x/15x has Type 1 I2C F28P55x has Type 2 I2C
	Register			
PMBUS	Number	1 - PMBUSA	1 - PMBUSA	F280013x/15x has Type 0 PMBUS F28P55x has Type 1 PMBUS
	HW Change		Supports Fast+ mode - 1MHz clock	
	Register	-	PMBUS_IO_DRVSEL	Configure increased drive strength to support Fast+ mode(1MHz)
		-	PMBUS_IO_MODESEL	Configure pin level, either 3.3V or 1.35V support
FSITX/RX	Number	-	1 - FSITXA/RXA	Type 2 FSI on F28P55x

3.3 Control Module Changes

There are minimal changes in the control modules between the F280013x/15x and F28P55x devices. Table 3-2 shows the module instances differences which should be considered when migrating applications between F280013x/15x and F28P55x.

Table 3-2. Control Module Differences

Module	Category	F280013x/15x	F28P55x	Notes
eQEP	Number	1(13x) or 2(15x) - EQEP1, EQEP2	3 - EQEP1, EQEP2, EQEP3	Type 2 eQEP on both devices
eCAP	Number	2(13x) or 3(15x) - ECAP1..3	2 - ECAP1, ECAP2	Type 2 eCAP on both devices
ePWM	Number	7 - EPWM1..7	12 - EPWM1..12	Type 4 PWM on both devices
HRPWM	Number	1(13x) or 2(15x) - HRPWM1..4	8 - HRPWM1..8	Type 4 HRPWM on both devices

3.4 Analog Module Differences

This section outlines the analog differences between F280013x/15x and F28P55x. Three Programmable Gain Amplifiers(PGA) are a new addition to the F28P55x and there are now five ADCs vs the two ADCs on the F280013x/15x device. There are several enhancements inside the CMPSS and ADC modules.

Table 3-3. Analog Module Differences

Module	Category	F280013x/15x	F28P55x	Notes
Analog SysCtrl	HW Changes	-	Global Sychronous SW Trigger for ADC	Allows for SW Trigger to ADC sent to selected ADCs simultaneously
		-	New register for VREFHI selection	Support for per ADC VREFHI selection reference voltage: 1. Internal VREFHI 2. External VREFHI 3. VDDA
		-	New register for VREFHI selection	Support for per ADC VREFLO selection reference voltage: 1. VREFLO pin 2. VSSA
		-	Support for full 3.3V FSR with External VREFHI	Can supply 1.65V on VREFHI in external mode to have FSR = 3.3V
		-	12mA Drive on Select GPIOs	For compatiblity with I2C and PMBUS High Speed + mode, GPIO 2/3/9/32 have option for 12mA drive strength (IOL)
		-	1.35V VIH compatibility on select GPIOs	Changes VIH for GPIO 2/3/9/32 to 1.35V
	Register	ANAREFCTL.ANAREFSEL	ANAREFPCTRL.REFPMUXSELx	x = ADC A/B/C/D/E Each ADC is now configured independently for VREFHI source
		-	ANAREFNCTL.REFNMUXSELx	x = ADC A/B/C/D/E Each ADC has VREFLO selection capability
		ANAREFCTL.ANAREF2P5SEL	ANAREFPCTL.ANAREFx1P65SEL	x = ADC A/B/C/D/E Each ADC has independent 1.65V(3.3V FSR) or 2.5V FSR selection. Also effects external reference mode.
		-	IO_DRVSEL	Configure selected GPIO drive strength (IOL) for either 4mA(default) or 12mA
		-	IO_MODESEL	Configure selected GPIO VIH to either 3.3V(default) or 1.35V

Table 3-3. Analog Module Differences (continued)

Module	Category	F280013x/15x	F28P55x	Notes
ADC [1]	Number	2 - ADCA, ADCB	5 - ADCA, ADCB, ADCC, ADCD, ADCE	F280013x/15x has Type 5 ADC F28P55x has Type 6 ADC
	Max Speed	60MHz	75MHz	Max throughput is the same at 4MSPS
	HW Changes	-	New PPB features 1. Summing/Max/Min/Abs value 2. Oversampling Support w repeat block 3. Previous Conversion Delta 4. Output Filtering	1. Ability for PPB to Sum/Max/Min/Abs value of concurent results 2. Automatically aggregates and averages user defined number of samples, returns only the average to a result register. Used with ADC Repater Block 3. Compares last conversion to current conversion and gerenates corresponding action 4. Returns values that are in range of filter window only, discarding others.
		-	ADC Repeater Logic	Ability to initate subseqent triggers automatically, with option to add phase delay. Can use with PPB to realize oversampling without CPU overhead
		-	Global SW Force SOC Trigger	Ability to initiate a SW SOC trigger to all ADCs simultaneously
		-	ADC S/H Cap Reset	Ability to reset the S/H Cap to VSSA between samples
	Register	ADCTL1	ADCTL1	Addition of External Mux Control and DMA Trigger Timings
		ADCSOCxCTL.TRIGSEL	ADCSOCxCTL.TRIGSEL	Increased Trigger Options for ePWM and repeat block support
		INTFLGCLR	ADCINTFLGCLR	
		ADCINTSOCSEL2	ADCINTSOCSEL1	All SOC interrupt triggers moved to INTSOCSEL1
GPDAC	Number	-	1- GPDACA	Type 1 GPDAC on F28P55x

Table 3-3. Analog Module Differences (continued)

Module	Category	F280013x/15x	F28P55x	Notes
CMPSS [1] [2]	Number	1 - CMPSS1	4 - CMPSS1 to CMPSS4	F280013x has Type 2 CMPSS F280015x and F28P55x have Type 3 CMPSS
	HW changes		1. Added DAC Ramp Generator to Low Side Comparator 2. Ramp Generator includes up ramp support	
	Registers	RAMPMAXREFA	RAMPHREFA	Register Name Change(F280013x Only)
		RAMMAXREFS	RAMPHREFS	Register Name Change(F280013x Only)
		RAMPDECVALA	RAMPHSTEPVALA	Register Name Change(F280013x Only)
		RAMPDECVALS	RAMPHSTEPVALS	Register Name Change(F280013x Only)
		RAMPSTS	RAMPHSTS	Register Name Change(F280013x Only)
		RAMPDLYA	RAMPHDLYA	Register Name Change(F280013x Only)
		RAMPDLYS	RAMPHDLYS	Register Name Change(F280013x Only)
		CTRIPLFILCTL	CTRIPLFILCTL - Field Changes	Additions and changes to fields within this register. For more details, see the device-specific TRMs.
		CTRIPLFILCLKCTL	CTRIPLFILCLKCTL - Field Changes	Increased prescalar range
		CTRIPHFILCTL	CTRIPHFILCTL - Field Changes	Additions and changes to fields within this register. For more details, see the device-specific TRMs.
		CTRIPHFILCLKCTL	CTRIPHFILCLKCTL - Field Changes	Increased prescalar range
		-	COMPDACLCTL	Register and functionality added to support dual ramp generators
		-	RAMPLREFA	Register and functionality added to support dual ramp generators(F280013x Only)
		-	RAMPLREFS	Register and functionality added to support dual ramp generators(F280013x Only)
		-	RAMPLSTEPVALA	Register and functionality added to support dual ramp generators(F280013x Only)
		-	RAMPLSTEPVALS	Register and functionality added to support dual ramp generators(F280013x Only)
		-	RAMPLSTS	Register and functionality added to support dual ramp generators(F280013x Only)
		-	RAMPLDLYA	Register and functionality added to support dual ramp generators(F280013x Only)
		-	RAMPLDLYS	Register and functionality added to support dual ramp generators(F280013x Only)
		-	CTRIPLFILCLKCTL2	Register and functionality added to support dual ramp generators
		-	CTRIPHFILCLKCTL2	Register and functionality added to support dual ramp generators
CMPSS_LITE	Number	3	-	CMPSS_LITE replaced with full CMPSS on the F28P55x
Temp Sensor	Number	1 - (in ADCC ch 12)	1 - (in ADCC ch12)	

1. In porting software from F280013x/15x to F28P55x (or the other way around), care must be taken to ensure that the correct ADC channels are used because of a difference in channel assignment, see Analog Multiplexing Changes.
2. Only applies to F280013x to F28P55x

3.5 Other Device Changes

This section describes feature differences between F280013x/15x and F28P55x that were not covered in the previous sections, as such the changes identified below must be considered when migrating applications between devices.

3.5.1 PLL

The PLL blocks of F280013x/15x and F28P55x devices are the same, however the maximum PLL Raw Clock for F28P55x is higher to accommodate the SYSCLK frequency requirement of F28P55x. Table 3-4 lists the PLL features for both devices for comparison. for more information, consult the TMS320F28P55x microcontrollers technical reference manual.

Table 3-4. PLL Features

Feature	F280013x/15x	F28P55x
Max CPU Clock	120 MHz	150 MHz
VCO Range	220 - 600 MHz	220 - 600 MHz
PLL Raw Clock Range	6 - 240 MHz	6- 300 MHz
X1 Input Range (PLL enable)	2 - 25 MHz	2 - 25 MHz
REFCLK Divider	Yes [1..32]	Yes [1..32]
PLL Slip Detect	No (use DCC)	No (use DCC)
Fractional PLLMULT	No	No

3.5.2 PIE Channel Mapping

Pie channel mapping between F280013x/15x and F28P55x is different due to peripheral module changes between these devices. Table 3-6 summarizes the common and unique pie channel assignments on these two devices.

Table 3-5. Mux Legend

Color	Description
	mux function common for both devices
	mux function applicable only for F280013x and F280015x
	mux function applicable only for F28P55x
	mux function applicable only for F28P55x and F280015x
	mux function only applicable for F280015x

Table 3-6. Pie Table Comparison

index	INTx.1	INTx.2	INTx.3	INTx.4	INTx.5	INTx.6	INTx.7	INTx.8	INTx.9	INTx.10	INTx.11	INTx.12	INTx.13	INTx.14	INTx.15	INTx.16
INT1.y	INT_ADCA1	INT_ADCB1 INT_ADCC1	INT_ADCC1	INT_XINT1	INT_XINT2	INT_SYS_ERR	INT_TIMER0	INT_WAKE	INT_ADCD1	INT_ADCE1						
INT2.y	INT_EPWM1_TZ	INT_EPWM2_TZ	INT_EPWM3_TZ	INT_EPWM4_TZ	INT_EPWM5_TZ	INT_EPWM6_TZ	INT_EPWM7_TZ	INT_EPWM8_TZ	INT_EPWM9_TZ	INT_EPWM10_TZ	INT_EPWM11_TZ	INT_EPWM12_TZ				
INT3.y	INT_EPWM1	INT_EPWM2	INT_EPWM3	INT_EPWM4	INT_EPWM5	INT_EPWM6	INT_EPWM7	INT_EPWM8	INT_EPWM9	INT_EPWM10	INT_EPWM11	INT_EPWM12				
INT4.y	INT_ECAP1	INT_ECAP2	INT_ECAP3													
INT5.y	INT_EQEP1	INT_EQEP2	INT_EQEP3		INT_CLB1	INT_CLB2										
INT6.y	INT_SPIA_RX	INT_SPIA_TX	INT_SPIB_RX	INT_SPIB_TX	INT_LINA_0	INT_LINA_1	INT_DCC0	INT_DCC1								
INT7.y	INT_DMA_CH1	INT_DMA_CH2	INT_DMA_CH3	INT_DMA_CH4	INT_DMA_CH5	INT_DMA_CH6	INT_PMBUSA				INT_FSITXA1	INT_FSITXA2	INT_FSIRXA1	INT_FSIRXA2		
INT8.y	INT_I2CA	INT_I2CA_FIFO	INT_I2CB	INT_I2CB_FIFO	INT_SCIC_RX	INT_SCIC_TX			INT_LINA_0	INT_LINA_1						

Table 3-6. Pie Table Comparison (continued)

index	INTx.1	INTx.2	INTx.3	INTx.4	INTx.5	INTx.6	INTx.7	INTx.8	INTx.9	INTx.10	INTx.11	INTx.12	INTx.13	INTx.14	INTx.15	INTx.16
INT9.y	INT_SCIA_RX	INT_SCIA_TX	INT_SCIB_RX	INT_SCIB_TX	INT_CANA0	INT_CANA1	INT_MCANA_0	INT_MCANA_1	INT_MCANB_0	INT_MCANB_1	INT_MCANB_ECC	INT_MCANB_WAKE			INT_USB	
INT10.y	INT_ADCA_EVT	INT_ADCA2	INT_ADCA3	INT_ADCA4	INT_ADCB_EVT	INT_ADCB2	INT_ADCB3	INT_ADCB4	INT_ADCC_EVT	INT_ADCC2	INT_ADCC3	INT_ADCC4	INT_ADCD_EVT	INT_ADCD2	INT_ADCD3	INT_ADCD4
					INT_ADCC_EVT	INT_ADCC2	INT_ADCC3	INT_ADCC4								
INT11.y	INT_CLA1_1	INT_CLA1_2	INT_CLA1_3	INT_CLA1_4	INT_CLA1_5	INT_CLA1_6	INT_CLA1_7	INT_CLA1_8	INT_ADCE_EVT	INT_ADCE2	INT_ADCE3	INT_ADCE4				
INT12.y	INT_XINT3	INT_XINT4	INT_XINT5		INT_FLSS	INT_VCU	INT_MCANA_ECC	INT_MCANA_WAKE					INT_AES			
							INT_MCANA_WAKE	INT_MCANA_ECC								

3.5.3 Bootrom

For bootrom similarities and differences between F280013x/15x and the F28P55x see Table 3-8 and Table 3-9.

Table 3-7. Boot options Legend

Color	Description
	Options common for both devices but BOOTDEFx values may differ
	Options applicable only for F280013x/15x
	Options applicable only for F28P55x

Table 3-8. Bootloaders and GPIO Assignment Comparison

Bootloader	Option	BOOTDEFx	F280013x/15x	F28P55x
Parallel	0	0x00	D0-D7=GPIO0,1,3,5,7,24,28,29; DSP=224; Host=242	D0-D7=GPIO0 to 7; DSP=16; Host=29
	1	0x20	D0-D7=GPIO0,1,2,3,5,6,7,24; DSP=12; Host=13	D0-D7=GPIO0,1,2,3,5,6,7,24; DSP=12; Host=13
	2	0x40	D0-D7=GPIO0,1,2,3,5,6,7,24: DSP=16; Host=29	-
SCIA	0	0x01	TX=29; RX=28	TX=29; RX=28
	1	0x21	TX=1; RX=0	TX=1; RX=0
	2	0x41	TX=8; RX=9	TX=8; RX=9
	3	0x61	TX=7; RX=3	TX=7; RX=3
	4	0x81	TX=16; RX=3	TX=16; RX=3
CAN[1]	0	0x02	TX=4;RX=5(13x) TX=7;RX=5(15x)	TX=4; RX=5
	1	0x22	TX=32; RX=33	TX=1; RX=0
	2	0x42	TX=2; RX=3	TX=13; RX=12
	3	0x62	TX=13; RX=12	-
MCAN(CAN-FD)	0	0x08	TX=1; RX=0	TX=4; RX=5
	1	0x28	TX=4; RX=5	TX=1; RX=0
	2	0x48	TX=13; RX=12	TX=13; RX=12
SPI	0	0x06	SIMO=7 SOMI=1; CLK=3; STE=5	PICO=2 POCI=1; CLK=3; PTE=5
	1	0x26	SIMO=16 SOMI=1; CLK=3; STE=0	PICO=16 POCI=1; CLK=3; PTE=0
	2	0x46	SIMO=8 SOMI=10; CLK=9; STE=11	PICO=8 POCI=10; CLK=9; PTE=11
	3	0x66	SIMO=16 SOMI=13; CLK=12; STE=29	PICO=16 POCI=12; CLK=9; PTE=24

Table 3-8. Bootloaders and GPIO Assignment Comparison (continued)

Bootloader	Option	BOOTDEFx	F280013x/15x	F28P55x
I2C	0	0x07	SDA=0; SCL=1	SDA=0; SCL=1
	1	0x27	SDA=32; SCL=33	SDA=32; SCL=33
	2	0x47	SDA=5; SCL=4	SDA=5; SCL=4
USB	0	0x09	-	DM=23; DP=41

1. For the F28P55x device "CAN" boot mode is supported by the MCAN module with FD mode set to "off"

Table 3-9. Boot Modes Comparison

Boot Mode	Option	BOOTDEFx	F280013x/15x	F28P55x
Flash/Secure Flash	0	0x03	Entry=0x00080000; Bank/Sector=0/0	Entry=0x00080000; Bank/Sector=0/0
	1	0x23	Entry=0x00088000; Bank/Sector=0/32	Entry=0x00088000; Bank/Sector=0/32
	2	0x43	Entry=0x0008FFF0; Bank/Sector=0/63	Entry=0x000C0000; Bank/Sector=0/64
	3	0x63	Entry=0x00090000; Bank/Sector=0/64	Entry=0x000C8000; Bank/Sector=1/64
	4	0x83	Entry=0x00098000; Bank/Sector=0/96	Entry=0x00100000; Bank/Sector=2/16
	5(Flash Only)	0xA3	Entry=0x0009FFF0; Bank/Sector=0/127	-
LFU Flash	0	0x0B	-	Entry=0x00080000; Bank=0 Entry=0x000C0000; Bank=2
	1	0x2B	-	Entry=0x00088000; Bank=0 Entry=0x000C8000; Bank=2
Wait	0	0x04	Watchdog enabled	Watchdog enabled
	1	0x24	Watchdog disabled	Watchdog disabled
RAM	0	0x05	Entry=0x00000000	Entry=0x00000000

3.6 Power Management

The F280013xV, F280015x and F28P55x devices support dual-rail (3.3 V and 1.2 V) or single-rail (3.3 V) with the internal LDO VREG providing the 1.2 V rail. The F280013x device has the internal LDO permently enalbled. This section describes the power management differences and similarities between the two devices.

3.6.1 LDO/VREG

Both F280015x and F28P55x supports internal and external VREG for the 1.2V supply selectable using the VREGENZ pin. However, only the F280013xV supports the external VREG option and has a VREGENZ pin. All other F280013x devices replaced this with a GPIO. For F28P55x all packages have a VREGENZ pin.

3.6.2 POR/BOR

There are no functional changes for the POR and BOR.

3.6.3 Power Consumption

If similar IP sets and target frequency is identical between the F280013x/15x and F28P55x then the power consumption should be approximately the same. See the datasheet for per peripheral and max currents for either device.

3.7 Memory Module Changes

RAM and FLASH memories in F280013x/15x and F28P55x devices have some similarities and differences. Table 3-10 summarizes the memory features including error-checking and security assignment.

Table 3-10. RAM and FLASH Memory Changes

Memory		F280013x/15x			F28P55x		
		Size	Parity/ ECC	Secured	Size	Parity/ ECC	Secured
RAM	Dedicated(M0, M1)	4KB	ECC	No	4KB	ECC	No
	Local Shared(LS0)	16KB	Parity	DCSM-controlled	4KB	Parity	DCSM-controlled
	LS1	16KB	Parity	DCSM-controlled	4KB	Parity	DCSM-controlled
	LS2-LS7	-	-	-	24KB	Parity	DCSM-controlled
	Local Shared(LS8-LS9)	-	-	-	32KB	Parity	DCSM-controlled
	Global Shared(GS0-GS3)	-	-	-	64KB	Parity	No
	Message	- -	-	-	512B(CPU-CLA) 512B(CLA-DMA)	Parity	No
	Total RAM	**32KB**			**133KB**		
FLASH	Per Sector	2KB	-	-	2KB	-	-
	Per Bank	256KB(1 bank)	ECC	DCSM-controlled	256KB(4 banks) 64KB(1 bank)	ECC	DCSM-controlled
	Total FLASH	**256KB(1 banks)**			**1088KB(5 banks)**		

3.8 GPIO Multiplexing Changes

GPIO Muxed Pins outlines the differences and similarities that exist in the GPIO mux between F280013x/15x and F28P55x.

Table 3-11. Mux Legend

Color	Description
	mux function common for both devices
	mux function applicable only for F280013x and F280015x
	mux function applicable only for F28P55x
	mux function applicable only for F28P55x and F280015x
	mux function only applicable for F280015x

Table 3-12. GPIO Muxed Pins

0	1	2	3	5	6	7	9	10	11	13	14	15
GPIO0	EPWM1_A	CANA_RX	OUTPUTXBAR7	SCIA_RX	I2CA_SDA	SPIA_PTE SPIA_STE	FSIRXA_CLK	MCANA_RX MCAN_RX	CLB_OUTPUTXBAR8	EQEP1_INDEX		EPWM3_A
GPIO1	EPWM1_B	EMU0		SCIA_TX	I2CA_SCL	SPIA_POCI SPIA_SOMI	EQEP1_STROBE	MCANA_TX MCAN_TX	CLB_OUTPUTXBAR7	EPWM10_B		EPWM3_B
GPIO2	EPWM2_A	EMU1		OUTPUTXBAR1	PMBUSA_SDA	SPIA_PICO SPIA_SIMO	SCIA_TX	FSIRXA_D1	I2CB_SDA	EPWM10_A	MCANB_TX CANA_TX	EPWM4_A
GPIO3	EPWM2_B	OUTPUTXBAR2		OUTPUTXBAR2	PMBUSA_SCL	SPIA_CLK	SCIA_RX	FSIRXA_D0	I2CB_SCL		MCANB_RX CANA_RX	EPWM4_B
GPIO4	EPWM3_A	I2CA_SCL	MCANA_TX MCAN_TX	OUTPUTXBAR3	CANA_TX	SPIB_CLK	EQEP2_STROBE	FSIRXA_CLK	CLB_OUTPUTXBAR6	EPWM11_B	SPIA_POCI SPIA_SOMI	EPWM1_A
GPIO5	EPWM3_B	I2CA_SDA	OUTPUTXBAR3	MCANA_RX MCAN_RX	CANA_RX	SPIA_PTE SPIA_STE	FSITXA_D1	CLB_OUTPUTXBAR5	SCIA_RX			EPWM1_B
GPIO6	EPWM4_A	OUTPUTXBAR4	SYNCOUT	EQEP1_A		SPIB_POCI	FSITXA_D0		FSITXA_D1	USB0_IVBUSVALID	CLB_OUTPUTXBAR8	EPWM2_A
GPIO7	EPWM4_B	EPWM2_A	OUTPUTXBAR5	EQEP1_B		SPIB_PICO SPIA_SIMO	FSITXA_CLK	CLB_OUTPUTXBAR2	SCIA_TX		MCANA_TX CANA_TX	EPWM2_B

Table 3-12. GPIO Muxed Pins (continued)

0	1	2	3	5	6	7	9	10	11	13	14	15
GPIO8	EPWM5_A		ADCSOCAO	EQEP1_STROBE	SCIA_TX	SPIA_PICO SPIA_SIMO	I2CA_SCL	FSITXA_D1	CLB_OUTPUTXBAR5	EPWM11_A		
GPIO9	EPWM5_B	SCIB_TX	OUTPUTXBAR6	EQEP1_INDEX	SCIA_RX	SPIA_CLK	I2CA_SCL	FSITXA_D0	LINA_RX	PMBUSA_SCL	I2CB_SCL	EQEP3_B
GPIO10	EPWM6_A		ADCSOCBO	EQEP1_A	SCIB_TX	SPIA_POCI SPIA_SOMI	I2CA_SDA	FSITXA_CLK	LINA_TX	EQEP3_STROBE		CLB_OUTPUTXBAR4
GPIO11	EPWM6_B	MCANA_RX CANA_RX	OUTPUTXBAR7	EQEP1_B	SCIB_RX	SPIA_PTE SPIA_STE	FSIRXA_D1	LINA_RX	EQEP2_A	SPIA_PICO SPIA_SIMO		EQEP3_INDEX
GPIO12	EPWM7_A		MCANA_RX MCAN_RX	EQEP1_STROBE	SCIB_TX	PMBUSA_CTL	FSIRXA_D0	LINA_TX	SPIA_CLK	CANA_RX		
GPIO13	EPWM7_B		MCANA_TX MCAN_TX	EQEP1_INDEX	SCIB_RX	PMBUSA_ALERT	FSIRXA_CLK	LINA_RX	SPIA_POCI SPIA_SOMI	CANA_TX		
GPIO14	EPWM8_A	SCIB_TX		I2CB_SDA	OUTPUTXBAR3	PMBUSA_SDA	SPIB_CLK	EQEP2_A	LINA_TX	EPWM3_A	CLB_OUTPUTXBAR7	USB0_ODPDAT
GPIO15	EPWM8_B	SCIB_RX		I2CB_SCL	OUTPUTXBAR4	PMBUSA_SCL	SPIB_PTE	EQEP2_B	LINA_RX	EPWM3_B	CLB_OUTPUTXBAR6	USB0_ODMSE0
GPIO16	SPIA_PICO SPIA_SIMO		OUTPUTXBAR7	EPWM9_A EPWM5_A	SCIA_TX		EQEP1_STROBE	PMBUSA_SCL	XCLKOUT	EQEP2_B	SPIB_POCI	EQEP3_STROBE
GPIO17	SPIA_POCI SPIA_SOMI		OUTPUTXBAR8	EPWM9_B EPWM5_B	SCIA_RX		EQEP1_INDEX	PMBUSA_SDA	MCANA_TX CANA_TX		EPWM6_A	
GPIO18	SPIA_CLK	SCIB_TX	MCANB_RX CANA_RX	EPWM6_A	I2CA_SCL		EQEP2_A	PMBUSA_CTL	XCLKOUT	LINA_TX		EQEP3_INDEX
GPIO19	SPIA_PTE SPIA_STE	SCIB_RX	MCANB_TX CANA_TX	EPWM6_B	I2CA_SDA		EQEP2_B	PMBUSA_ALERT	CLB_OUTPUTXBAR1	LINA_RX		
GPIO20	EQEP1_A		CANA_TX	EPWM12_A	SPIB_PICO SPIA_SIMO		MCANA_TX MCAN_TX	ADCE_EXTMUXSEL0	I2CA_SCL			SCIC_TX
GPIO21	EQEP1_B		CANA_RX	EPWM12_B	SPIB_POCI SPIA_SOMI		MCANA_RX MCAN_RX	ADCE_EXTMUXSEL1	I2CA_SDA			SCIC_RX
GPIO22	EQEP1_STROBE		SCIB_TX		SPIB_CLK		LINA_TX	CLB_OUTPUTXBAR1	LINA_TX		EPWM4_A	EQEP3_A
GPIO23	EQEP1_INDEX		SCIB_RX		SPIB_PTE		LINA_RX	CLB_OUTPUTXBAR3	LINA_RX	EPWM12_A	EPWM4_B	
GPIO24	OUTPUTXBAR1	EQEP2_A	SPIA_PTE SPIA_STE	EPWM8_A EPWM4_A	SPIB_PICO SPIA_SIMO		LINA_TX	PMBUSA_SCL	SCIA_TX	ERRORSTS	EPWM9_A	
GPIO25	OUTPUTXBAR2	EQEP2_B		EQEP1_A	SPIB_POCI		FSITXA_D1	PMBUSA_SDA	SCIA_RX	EQEP3_A		

Table 3-12. GPIO Muxed Pins (continued)

0	1	2	3	5	6	7	9	10	11	13	14	15
GPIO26	OUTPUTXBAR3	EQEP2_INDEX		OUTPUTXBAR3	SPIB_CLK		FSITXA_D0	PMBUSA_CTL	I2CA_SDA	EQEP3_B		
GPIO27	OUTPUTXBAR4	EQEP2_STROBE		OUTPUTXBAR4	SPIB_PTE		FSITXA_CLK	PMBUSA_ALERT	I2CA_SCL	EQEP3_STROBE		
GPIO28	SCIA_RX		EPWM7_A	OUTPUTXBAR5	EQEP1_A		EQEP2_STROBE	LINA_TX	SPIB_CLK SPIA_CLK	ERRORSTS	I2CB_SDA	
GPIO29	SCIA_TX		EPWM7_B	OUTPUTXBAR6	EQEP1_B		EQEP2_INDEX	LINA_RX	SPIB_PTE SPIA_STE	ERRORSTS	I2CB_SCL	
GPIO30	CANA_RX		SPIB_PICO	OUTPUTXBAR7	EQEP1_STROBE		FSIRXA_CLK	MCANA_RX MCAN_RX	EPWM1_A	EQEP3_INDEX		
GPIO31	CANA_TX		SPIB_POCI	OUTPUTXBAR8	EQEP1_INDEX		FSIRXA_D1	MCANA_TX MCAN_TX	EPWM1_B			
GPIO32	I2CA_SDA	EQEP1_INDEX	SPIB_CLK SPIA_CLK	EPWM8_B EPWM4_B	LINA_TX		FSIRXA_D0	MCANB_TX CANA_TX	PMBUSA_SDA	ADCSOCBO		
GPIO33	I2CA_SCL		SPIB_PTE	OUTPUTXBAR4	LINA_RX		FSIRXA_CLK	MCANB_RX CANA_RX	EQEP2_B	ADCSOCAO		SCIC_RX
GPIO34	OUTPUTXBAR1				PMBUSA_SDA						I2CB_SDA	
GPIO35	SCIA_RX	SPIA_POCI SPIA_SOMI	I2CA_SDA	MCANB_RX CANA_RX	PMBUSA_SCL	LINA_RX	EQEP1_A	PMBUSA_CTL	EPWM5_B			TDI
GPIO37	OUTPUTXBAR2	SPIA_PTE SPIA_STE	I2CA_SCL	SCIA_TX	MCANB_TX CANA_TX	LINA_TX	EQEP1_B	PMBUSA_ALERT	EPWM5_A			TDO
GPIO39					MCAN_RX		EQEP2_INDEX			SYNCOUT	EQEP1_INDEX	
GPIO40	SPIB_PICO		EMU0	EPWM2_B	PMBUSA_SDA	FSIRXA_D0	SCIB_TX	EQEP1_A	LINA_TX		CLB_OUTPUTXBAR4	EQEP3_STROBE
GPIO41	EPWM7_A		EMU1	EPWM2_A	PMBUSA_SCL	FSIRXA_D1	SCIB_RX	EQEP1_B	LINA_RX	EPWM12_B	SPIB_POCI	
GPIO42		LINA_RX	OUTPUTXBAR5	PMBUSA_CTL	I2CA_SDA	SCIC_RX		EQEP1_STROBE	CLB_OUTPUTXBAR3			
GPIO43			OUTPUTXBAR6	PMBUSA_ALERT	I2CA_SCL	SCIC_TX	PMBUSA_ALERT	EQEP1_INDEX	CLB_OUTPUTXBAR4			
GPIO44			OUTPUTXBAR7	EQEP1_A	PMBUSA_SDA	FSITXA_CLK	PMBUSA_CTL	CLB_OUTPUTXBAR3	FSIRXA_D0		LINA_TX	
GPIO45			OUTPUTXBAR8			FSITXA_D0	PMBUSA_ALERT	CLB_OUTPUTXBAR4				

Table 3-12. GPIO Muxed Pins (continued)

0	1	2	3	5	6	7	9	10	11	13	14	15
GPIO46			LINA_TX	MCANA_TX MCAN_TX		FSITXA_D1	PMBUSA_SDA					
GPIO47			LINA_RX	MCANA_RX		CLB_OUTPUTXBAR2	PMBUSA_SCL					
GPIO48	OUTPUTXBAR3		CANA_TX	MCANA_TX MCAN_TX	SCIA_TX		PMBUSA_SDA					
GPIO49	OUTPUTXBAR4		CANA_RX	MCANA_RX MCAN_RX	SCIA_RX		LINA_RX				FSITXA_D0	
GPIO50	EQEP1_A			MCANA_TX	SPIB_PICO		I2CB_SDA				FSITXA_D1	
GPIO51	EQEP1_B			MCANA_RX	SPIB_POCI		I2CB_SCL				FSITXA_CLK	
GPIO52	EQEP1_STROBE			CLB_OUTPUTXBAR5	SPIB_CLK		SYNCOUT				FSIRXA_D0	
GPIO53	EQEP1_INDEX			CLB_OUTPUTXBAR6	SPIB_PTE		ADCSOCAO	MCANB_RX			FSIRXA_D1	
GPIO54	SPIA_PICO			EQEP2_A	OUTPUTXBAR2		ADCSOCBO	LINA_TX			FSIRXA_CLK	
GPIO55	SPIA_POCI			EQEP2_B	OUTPUTXBAR3		ERRORSTS	LINA_RX				
GPIO56	SPIA_CLK	CLB_OUTPUTXBAR7	MCANA_TX	EQEP2_STROBE	SCIB_TX		SPIB_PICO	I2CA_SDA	EQEP1_A		FSIRXA_D1	
GPIO57	SPIA_PTE	CLB_OUTPUTXBAR8	MCANA_RX	EQEP2_INDEX	SCIB_RX		SPIB_POCI	I2CA_SCL	EQEP1_B		FSIRXA_CLK	
GPIO58				OUTPUTXBAR1	SPIB_CLK		LINA_TX	MCANB_TX	EQEP1_STROBE		FSIRXA_D0	
GPIO59				OUTPUTXBAR2	SPIB_PTE		LINA_RX	MCANB_RX	EQEP1_INDEX			
GPIO60	EPWM12_B		MCANA_TX	OUTPUTXBAR3	SPIB_PICO							
GPIO61			MCANA_RX	OUTPUTXBAR4	SPIB_POCI						MCANB_RX	
GPIO62	EPWM10_A	OUTPUTXBAR3		MCANA_TX	SCIA_TX		PMBUSA_SDA					USB0_OIDPULLUP
GPIO63	EPWM10_B	OUTPUTXBAR4		MCANA_RX	SCIA_RX		LINA_RX					USB0_OSPEED
GPIO64	SCIA_RX	EPWM11_A	EPWM7_A	OUTPUTXBAR5	EQEP1_A		EQEP2_STROBE	LINA_TX	SPIB_CLK	ERRORSTS	I2CB_SDA	USB0_OSUSPEND
GPIO65	EQEP1_A	EPWM11_B			SPIB_PICO		MCANA_TX		I2CA_SCL		USB0_OFSD_1_N	

Table 3-12. GPIO Muxed Pins (continued)

0	1	2	3	5	6	7	9	10	11	13	14	15
GPIO66	EQEP1_B	EPWM12_A			SPIB_POCI		MCANA_RX		I2CA_SDA		USB0_ODISCHRGVBUS	
GPIO67	EPWM7_B	EPWM12_B	MCANA_TX	EQEP1_INDEX	SCIB_RX	PMBUSA_ALERT	FSIRXA_CLK	LINA_RX	SPIA_POCI		USB0_OCHRGVBUS	SCIC_RX
GPIO68	EPWM7_A	EPWM3_A	MCANA_RX	EQEP1_STROBE	SCIB_TX	PMBUSA_CTL	FSIRXA_D0	LINA_TX	SPIA_CLK		USB0_ODMPULLDN	SCIC_TX
GPIO69	EPWM6_B	EPWM3_B	OUTPUTXBAR7	EQEP1_B	SCIB_RX	SPIA_PTE	FSIRXA_D1	LINA_RX	EQEP2_A	SPIA_PICO	USB0_ODPPULLDN	EQEP3_INDEX
GPIO70	I2CA_SCL		SPIB_PTE	OUTPUTXBAR4	LINA_RX		FSIRXA_CLK	MCANA_RX	EQEP2_B	ADCSOCAO	USB0_OLSD_2_N	EQEP3_A
GPIO71	SPIA_PICO	EPWM4_B	OUTPUTXBAR7	EPWM9_A	SCIA_TX		EQEP1_STROBE	PMBUSA_SCL	XCLKOUT	EQEP2_INDEX	SPIB_POCI	EQEP3_STROBE
GPIO72	SPIA_POCI	EPWM5_A	OUTPUTXBAR8	EPWM9_B	SCIA_RX		EQEP1_INDEX	PMBUSA_SDA	MCANA_TX	USB0_OLSD_1_N	EPWM6_A	EQEP3_B
GPIO73	OUTPUTXBAR1	EPWM5_B	SPIA_PTE	EPWM8_A	SPIB_PICO		LINA_TX	PMBUSA_SCL	SCIA_TX	ERRORSTS	EPWM9_A	USB0_OOE
GPIO74	EPWM2_B		ADCSOCAO	MCANA_TX	SPIA_POCI				EQEP1_B	USB0_IID		
GPIO75	EPWM1_B		LINA_RX	EPWM6_A	SPIA_CLK				EQEP1_STROBE	USB0_ISESSEND	SCIC_RX	
GPIO76	EPWM4_A			OUTPUTXBAR2	SPIA_PTE			MCANA_RX	EQEP1_INDEX	USB0_IAVALID		
GPIO77	EPWM1_A			OUTPUTXBAR3	SPIA_PICO			MCANA_TX	EQEP1_A	USB0_IXRCV	SCIC_TX	
GPIO78		EPWM8_A	EPWM3_A	OUTPUTXBAR1	EPWM2_B		FSITXA_CLK			USB0_IDM		
GPIO79		EPWM8_B	EPWM3_B	MCANA_RX	EPWM2_A	I2CA_SDA	PMBUSA_SCL			USB0_IDP		
GPIO80	EPWM1_A		OUTPUTXBAR7	SCIA_RX	I2CB_SDA	SPIA_PTE	FSITXA_D0	MCANA_RX	CLB_OUTPUTXBAR8	EQEP1_INDEX	USB0_OFSD_2_N	EPWM3_A
GPIO81	EPWM1_B	OUTPUTXBAR6	SCIC_RX	SPIB_CLK	I2CB_SCL		FSITXA_D1	MCANA_TX	EQEP3_INDEX			
GPIO211	EPWM10_A			EQEP3_A								
GPIO212	EPWM10_B			EQEP3_B								
GPIO213	EPWM11_A			EQEP3_STROBE								
GPIO214	EPWM11_B			EQEP3_INDEX								
GPIO215	EPWM7_B			EQEP2_A								

Table 3-12. GPIO Muxed Pins (continued)

0	1	2	3	5	6	7	9	10	11	13	14	15
GPIO224	EPWM11_B			OUTPUTXBAR3	SPIA_PICO SPIA_SIMO		EPWM1_A	MCANA_TX CANA_TX	EQEP1_A	ADCE_EXTMUXSEL3	SCIC_TX	
GPIO226	EPWM10_B		LINA_RX	EPWM6_A	SPIA_CLK		EPWM1_B		EQEP1_STROBE	ADCE_EXTMUXSEL1	SCIC_RX	
GPIO227	I2CB_SCL		EPWM3_A	OUTPUTXBAR1	EPWM2_B							
GPIO228	EPWM10_A	EMU1	ADCSOCAO	MCANA_TX CANA_TX	SPIA_POCI SPIA_SOMI		EPWM2_B		EQEP1_B	ADCE_EXTMUXSEL0		
GPIO230	I2CB_SDA		EPWM3_B	MCANA_RX CANA_RX	EPWM2_A	I2CA_SDA	PMBUSA_SCL					
GPIO236												
GPIO242	EPWM11_A			OUTPUTXBAR2	SPIA_PTE SPIA_STE		EPWM4_A	MCANA_RX CANA_RX	EQEP1_INDEX	ADCE_EXTMUXSEL2		
GPIO247	EPWM12_B											
GPIO253	EPWM12_A											
AIO208												
AIO209												
AIO210												
AIO225												
AIO229												
AIO231												
AIO232												
AIO233												
AIO234												
AIO235												
AIO237												
AIO238												
AIO239												
AIO240												
AIO241												
AIO244												
AIO245												
AIO248												
AIO249												

Table 3-12. GPIO Muxed Pins (continued)

0	1	2	3	5	6	7	9	10	11	13	14	15
AIO251												
AIO252												

3.9 Analog Multiplexing Changes

outlines the differences and similarities that exist in the analog mux between F280015x and F28P55x for the 80-Pin PN/PNA and the F280013x/15x and F28P55x for the 64-Pin PM packages. The legend for the table is Table 3-13. The main change is the addition of ADCD, ADCE and the PGA. There are also many more AGPIOs on the F28P55x

Table 3-13. Mux Legend

Color	Description
	mux function common for both devices
	mux function applicable only for F28013x/15x
	mux function applicable only for F28P55x

Table 3-14. F280013x/15 and F28P55x 80-Pin PN/PNA and 64-Pin PM Analog Mux Table Differences

(F280013x/15x Pin Name)	Package Pin		ADC					Comparator Subsystem (MUX)				AIO/ AGPIO Input
F28P55x Pin Name	80 PNA	64 PM	A	B	C	D	E	High Positive	High Negative	Low Positive	Low Negative	
VREFHI	20	16										
VREFLO	21	17	A13	-	C13	-	-					
				B13		D13	E13					
Analog Group 1								**CMP1**				
(A6)	10	6	A6	-	-	-	-	CMP1 (HPMXSEL=2)		CMP1 (LPMXSEL=2)		AGPIO228
A6/D14/E14						D14	E14					
(A2/C9)	13	9	A2	-	C9	-	-	CMP1 (HPMXSEL=0)		CMP1 (LPMXSEL=0)		AGPIO224
A2/B6/C9/ PGA1_INP				B6								
(A15/C7)	14	10	A15	-	C7	-	-	CMP1 (HPMXSEL=3)	CMP1 (HNMXSEL=0)	CMP1 (LPMXSEL=3)	CMP1 (LNMXSEL=0)	AIO233
A15/B9/C7/ PGA1_INM				B9								AGPIO223
(A11/C0)	16	12	A11	-	C0	-	-	CMP1 (HPMXSEL=1)	CMP1 (HNMXSEL=1)	CMP1 (LPMXSEL=1)	CMP1 (LNMXSEL=1)	AIO237
A11/B10/C0/ PGA2_OUT				B10								
(A1)	18	14	A1	-	-	-	-	CMP1 (HPMXSEL=4)		CMP1 (LPMXSEL=4)		AIO232
A1/B7/D11/ DACB_OUT				B7		D11						
Analog Group 2								**CMP2**				
(A10/C10)	29	25	A10	-	C10	-	-	CMP2 (HPMXSEL=3)	CMP2 (HNMXSEL=0)	CMP2 (LPMXSEL=3)	CMP2 (LNMXSEL=0)	GPIO230
A10/B1/C10				B1								
Analog Group 3								**CMP3**				
(C6)	11	7	-	-	C6	-	-	CMP3 (HPMXSEL=0)		CMP3 (LPMXSEL=0)		GPIO226
B2/C6/E12				B2			E12					
(A3/C5)	12	8	A3	-	C5	-	-	CMP3 (HPMXSEL=3) CMP3 (HPMXSEL=5)	CMP3 (HNMXSEL=0)	CMP3 (LPMXSEL=3)CMP 3 (LPMXSEL=5)	CMP3 (LNMXSEL=0)	GPIO242
A3/B3/C5/ PGA2_INP				B3								
(A14/C4)	15	11	A14	-	C4	-	-	CMP3 (HPMXSEL=4)		CMP3 (LPMXSEL=4)		AIO239
A14/B14/C4/ PGA1_OUT				B14								
(A0/C15/ DACA_OUT) A0/B15/C15/ DACA_OUT	15	11	A0	-	C15	-	-	CMP3 (HPMXSEL=2)		CMP3 (LPMXSEL=2)		AIO231
				B15								
Analog Group 4								**CMP4**				
(A7/C3)	23	19	A7	-	C3	-	-	CMP4 (HPMXSEL=1)	CMP4 (HNMXSEL=1)	CMP4 (LPMXSEL=1)	CMP4 (LNMXSEL=1)	AIO245
A7/B30/C3/D12/E30				B30		D12	E30					
Analog Group 2/3								**CMP2/3**				

Table 3-14. F280013x/15 and F28P55x 80-Pin PN/PNA and 64-Pin PM Analog Mux Table Differences (continued)

(F280013x/15x Pin Name)	Package Pin		ADC					Comparator Subsystem (MUX)				AIO/ AGPIO Input
F28P55x Pin Name	80 PNA	64 PM	A	B	C	D	E	High Positive	High Negative	Low Positive	Low Negative	
A5/C2	17	13	A5	-	C2	-	-	CMP3 (HPMXSEL=1)	CMP3 (HNMXSEL=1)	CMP3 (LPMXSEL=1)	CMP3 (LNMXSEL=1)	AIO244
A5/B12/C2/ PGA2_INM	17	13	A5	B12	C2	-	-	CMP2 (HPMXSEL=5)CMP 3 (HPMXSEL=1)		CMP2 (LPMXSEL=5)CMP 3 (LPMXSEL=1)		AIO244/ AIO249
Combined Analog Group 2/4								**CMP2/4**				
(A12/C1)	22	18	A12	-	C1	-	-	CMP2 (HPMXSEL=1) CMP4 (HPMXSEL=2)	CMP2 (HNMXSEL=1)	CMP2 (LPMXSEL=1) CMP4 (LPMXSEL=2)	CMP2 (LNMXSEL=1)	AIO238
A12/C1/E11/ PGA3_INP							E11					AIO238/ AIO248
(A8/C11)	24	20	A8	-	C11	-	-	CMP2 (HPMXSEL=4) CMP4 (HPMXSEL=4)		CMP2 (LPMXSEL=4) CMP4 (LPMXSEL=4)		AIO241
A8/B0/C11/ PGA3_OUT				B0				CMP4 (HPMXSEL=4)		CMP4 (LPMXSEL=4)		
(A4/C14)	27	23	A4	-	C14	-	-	CMP2 (HPMXSEL=0) CMP4 (HPMXSEL=3)	CMP4 (HNMXSEL=0)	CMP2 (LPMXSEL=0) CMP4 (LPMXSEL=3)	CMP4 (LNMXSEL=0)	AIO225
A4/B8/C14				B8								
(A9/C8)	28	24	A9	-	C8	-	-	CMP2 (HPMXSEL=2) CMP4 (HPMXSEL=0)		CMP2 (LPMXSEL=2) CMP4 (LPMXSEL=0)		AGPIO227
A9/B4/C8				B4								AIO236/ AGPIO227
Other Analog												
A16	4	2	A16	-	-	-	-	-	-	-	-	AGPIO28
A16/B16/C16				B16	C16	-	-					
A17	33	27	A17	-	-	-	-	-	-	-	-	AGPIO20
A17/B17/C17				B17	C17	-	-					
A18	34	28	A18	-	-	-	-	-	-	-	-	AGPIO21
A18/B18/C18				B18	C18	-	-					
A19	35	29	A19	-	-	-	-	-	-	-	-	AGPIO13
A19/B19/C19				B19	C19	-	-					
A20	36	30	A20	-	-	-	-	-	-	-	-	AGPIO21
A20/B20/C20				B20	C20	-	-					
-	37	31	-	-	-	-	-					GPIO11
A24/D0/E0			A24	-	-	D0	E0					AGPIO11
-	38	32	-	-	-	-	-					GPIO33
B24/D1/E1			B24	-	-	D1	E1					AGPIO33
-	39	33	-	-	-	-	-					GPIO16
C24/D2/E2			-	-	C24	D2	E2					AGPIO16
-	40	34	-	-	-	-	-					GPIO17
A25/D3/E3			A25	-	-	D3	E3					AGPIO17
-	41	35	-	-	-	-	-					GPIO24
B25/D4/E4			-	B25	-	D4	E4					AGPIO24
PGA1_OUT_INT(internal)								CMP1 (HPMXSEL=6)		CMP1 (LPMXSEL=6)		
PGA2_OUT_INT(internal)								CMP2 (HPMXSEL=6)		CMP2 (LPMXSEL=6)		
PGA3_OUT_INT(internal)								CMP3 (HPMXSEL=6)		CMP=3 (LPMXSEL=6)		
TempSensor	-	-	-	-	C12	-	-	CMP2(HPMXSEL=7)				

4 Application Code Migration From F280013x/15x to F28P55x

The following section describes code changes when migrating from F280013x/15x to F28P55x. Software examples for the new features in F28P55x are also discussed in this section.

4.1 C2000Ware Header Files

Header files for both F280013x/15x and F28P55x devices are available in C2000Ware under the device_support sub directory.

4.2 Linker Command Files

Linker command files for both F280013x/15x and F28P55x devices are available in C2000Ware under the device_support sub directory. Both F280013x/15x and F28P55x, have to be compiled to the Embedded Application Binary Interface (EABI) format, section names would also need to conform to the EABI standard.

4.3 C2000Ware Examples

C2000Ware has examples specific for both F280013x/15x and F28P55x devices.

5 Specific Use Cases Related to F28P55x New Features

This section outlines the new examples in C2000Ware for the F28P55x device to support the new features on F28P55x that do not exist on F280013x/15x.

5.1 AES

C2000Ware has examples that demonstrate the encryption and decryption capabilities of the AES module.

5.2 PGA

C2000Ware has examples that demonstrate the capability of the new PGA on the F28P55x device.

5.3 USB

C2000Ware has examples that support the USB module that is on the F28P55x.

6 EABI Support

Both F280013x/15x and F28P55x devices use the Embedded Application Binary Interface (EABI) format for the binary executable output.

6.1 Flash API

F280013x/15x has one Flash bank. F28P55x has up to five Flash banks. Both F280013x/15x and F28P55x Flash API library is compiled for EABI format. Sector sizes are the same for all the devices. The Flash wait-state configuration requirement is the different between the two devices due to the higher operating frequency of the F28P55x. These features are summarized in Table 6-1.

Table 6-1. Flash API Differences

Feature	F280013x/15x	F28P55x
Library Name	FlashAPI_F280013x/15x_FPU32.lib	FlashAPI_F28P55x_FPU32.lib
Library Executable Output	EABI	EABI
Erase, Blank-check, Program and Verify	Operation on one bank	Operation on five banks
Sector Size	1K x 16-bit word	1K x 16-bit word
Flash Wait States	2 (120MHz)	3 (150MHz)
Flash API Major Version	2	4
FlashAPI Minor Version	0	0

7 References

- Texas Instruments: *TMS320F280013x Microcontrollers Technical Reference Manual*
- Texas Instruments: *TMS320F280015x Microcontrollers Technical Reference Manual*
- Texas Instruments: *TMS320F28P55x Microcontrollers Technical Referene Manual*
- Texas Instruments: *TMS320F280013x Microcontrollers Data Sheet*
- Texas Instruments: *TMS320F280015x Microcontrollers Data Sheet*
- Texas Instruments: *TMS320F28003x Microcontrollers Data Sheet*

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