EVM User's Guide: J742S2XH01EVM

J742S2XH01EVM Evaluation Module

Description

The J742S2XH01EVM evaluation module (EVM) is a platform for evaluating the TDA4VPE-Q1 and TDA4APE-Q1 processors in vision analytics and networking applications throughout automotive and industrial markets. These processors perform particularly well in multicamera, sensor fusion and advanced driver-assistance system (ADAS) domain-control applications. The J742S2XH01EVM is supported by SDK processor, which includes foundational drivers, compute and vision kernels, and example application frameworks and demonstrations that show how to take advantage of the powerful heterogeneous architecture of Jacinto™ 7 processors.

Get Started

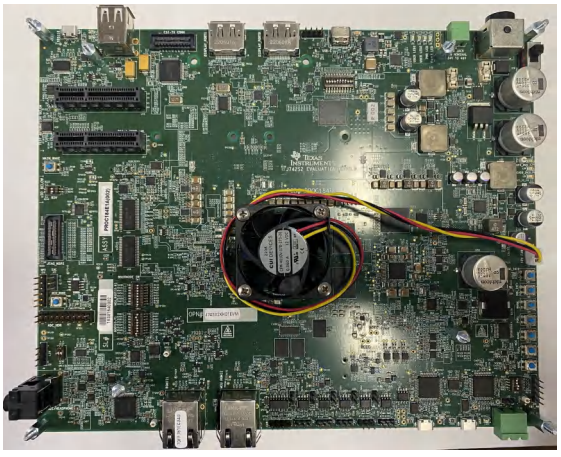
1. Order the EVM at J742S2XH01EVM.
2. Download the EVM Design Files.
3. Download the software from J742S2XH01EVM.
4. Read this user's guide.

Features

- Processing capabilities includes four Arm® Cortex®-A72 microprocessor subsystem up to 2.0GHz, eight Arm® Cortex®-R5F single cores up to 1.0GHz. Up to three C7x floating point DSP supporting 320GFLOPs at 1.0GHz. Up to two deep-learning accelerators supporting 32TOPS at 1.0GHz
- Triple display supported including two 3840 x 2160p (4K) displays using single DisplayPort™ connector with Multi-Stream Transport (MST). Second DisplayPort interface supports 1,920 x 1080p via DisplayPort. Graphics processing is capable of supporting 50GFLOPS, 4GTexels/s
- Capture capability includes three MIPI-CSI2 ports each supporting rates of 10Gb/s. Supports up to twelve cameras with multi-camera hub module (separate module). Processing includes dual Vision Processing Accelerators with ISP (VPAC), Depth and Motion accelerators (DMPAC), and multiple vision assist accelerators
- Multiple different storage technologies are supported allowing variety of configurations and test scenarios – including LPDDR, Octal-Serial NOR/NAND, Universal Flash Storage (UFS), Embedded Mult-Media Card (eMMC) and removable Secure Digital card (SD/MMC)
- Software support includes TI processor SDK Linux, RT-Linux, RTOS MCU+ SDK, QNX SDK, out-of-box demos including Android

Applications

- Automotive and industrial
  - Automotive front camera systems
  - Automotive surround view and park assistance systems
  - Industrial HMI
  - Robot teach pendant



J742S2XH01EVM

1 Evaluation Module Overview

1.1 Introduction

The J742S2XH01EVM is a standalone test, development, and evaluation module that contains a variety of both on-board peripherals and external interfaces, giving customers the flexibility to customize the platform to their needs. This design is not a reference design, as the design includes circuity for software development/debug and configuration flexibility. However, some portions of the design are optimized and can be considered as reference (LPDDR4 implementation as an example). The J742S2XH01EVM EVM supports multiple feature-rich software development kits (SDK) not covered in this user's guide. This document describes how to use the hardware as well as some of the architecture and design elements of the EVM.

The TDA4VPE-Q1 and TDA4APE-Q1 processors have a powerful heterogeneous architecture that includes a mix of DSP cores, Arm Cortex-A72 cores, matrix math acceleration for artificial intelligence (AI), integrated image signal processor (ISP) and vision-processing acceleration, 3D graphics processing unit (GPU) cores, and H.264 and H.265 encode and decode acceleration. An integrated safety microcontroller unit (MCU) includes dual-lockstep Arm Cortex-R5F cores that aid the system in achieving ASIL-D-level certification.

The EVM allows for multicamera inpust via CSI-2 ports and multi-display connectivity via the DisplayPort and display serial interface (DSI). Connectivity includes a USB3.1 Gen 1 (Dual role) Type C interface, two PCI-Express (Gen3) card interfaces, dual Gigabit Ethernet® interfaces, multiple CAN Bus interfaces with CAN-FD support, onboard XDS110 Joint Action Group (JTAG) emulator, and six universal asynchronous receiver-transmitters (UARTs) via USB2.0-B.

1.2 Kit Contents

The EVM orderable part number is: J742S2XH01EVM. This kit includes:

- J742S2XH01EVM
- Micro-SD card (blank)
- USB cable (Type-A to Micro-B) for serial terminal/logging
- USB cable (Type-A to Type-C®)
- USB adapter (Type-C Plug to Type-A receptacle)
- Ethernet cable (RJ45)
- DisplayPort cable
- EVM user's guide pamphlet
- EVM disclaimer and standard terms

The EVM is powered from a 4-pin DIN power jack. A power supply is NOT included. For more information on the types of supplies recommended with the EVM, see Section 2.3.

1.3 Device Information

Many different devices and technologies are used to create this EVM. The list below details some key Texas Instruments devices included on this design and links to get additional information.

Function	Device Information
Processor, SoC	TDA4VPE-Q1, TDA4APE-Q1
Power management, SoC	TPS6594113A
Power regulator, SoC	TPS62873-Q1
Audio Codec	PCM3168A-Q1
CAN-FD Bus transceiver	TCAN1042HG-Q1
DisplayPort Bridge	SN65DSI86, SN65DSI86-Q1
Emulator (XDS110)	TM4C1294NCPDT
Ethernet PHY, Gb	DP83867E
IO expansion	TCA6408A-Q1, TCA6416A, TCA6424A
Power monitor	INA226, INA226-Q1
Power regulator (3V3, 5V)	LM5141-Q1, LM5143-Q1

Function	Device Information
Power regulator (LDO)	TPS74801-Q1
Temperature sensor	TMP100, TMP100-Q1
USB Hub controller	TUSB4041I-Q1
USB Power regulator	TPS25830-Q1
USB Type-C controller	TUSB321

1.4 Specification

The figure below shows the functional block diagram of the EVM.

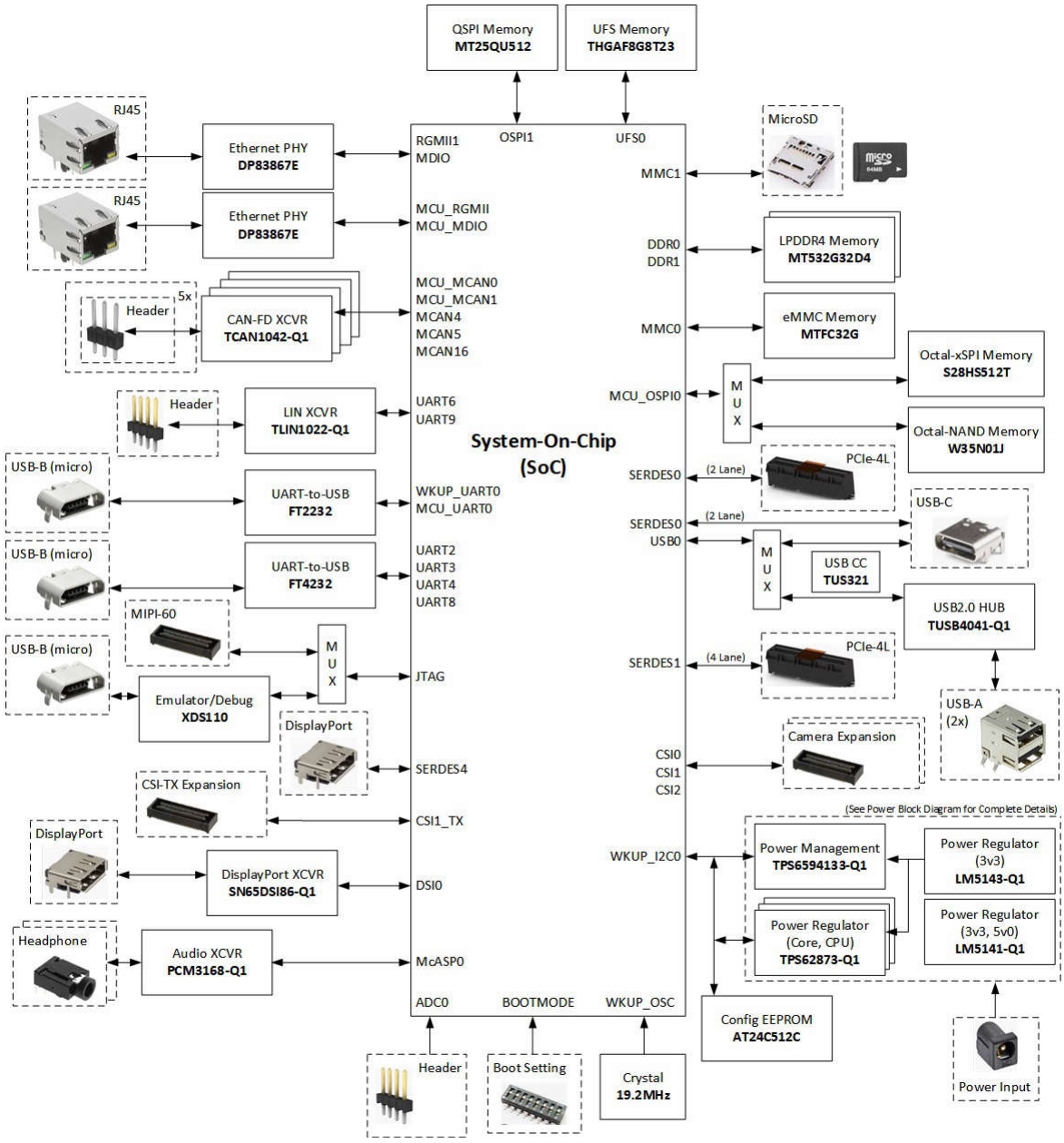


Figure 1-1. J742S2XH01EVM Block Diagram

2 Hardware

2.1 Key Features and Interfaces

The J742S2XH01EVM is a high performance, standalone development platform that enables users to evaluate and develop automotive and industrial applications using the Texas Instruments' J742S2/TDA4VPE/TDA4APE processor. A summary of the EVM features include:

- Processor (also referred to as SoC or System-on-Chip):
  - Texas Instruments' Jacinto J742S2 super-set device
- Optimized power management design:
  - Dynamic voltage scaling
  - Multiple clock and power domains
  - Multiple low power/sleep modes (MCU only, IO retention)
- Memory:
  - 16GB LPDDR4 DRAM (4266 MT/s), support inline ECC
  - Two 512Mb non-volatile NOR Memories, 1x Octal-SPI and 1x Quad-SPI
  - 1Gb non-volatile NAND Memory, Octal-SPI
  - 32GB non-volatile eMMC Memory, JEDEC/MMC v5.1 compliant
  - 32GB non-volatile UFS Memory, 2Lane, Gear3
  - Multimedia card (MMC)/secure digital card (Micro-SD) cage, UHS-1
- USB:
  - USB3.1 (Gen 1) Type C interface, support DFP, DRP, UFP modes
  - USB2.0 Hub to 2x Type A (host), 1x pin header for PCIe WiFi® support
  - Two USB2.0 Micro B (for dual/quad UART-over-USB transceiver)
- Display:
  - VESA DisplayPort (v1.4), supports 4K UHD with MST support
  - VESA DisplayPort (v1.4), supports 2K QHD
  - Custom CSI2-TX expansion interface
- Wired network:
  - Two gigabit Ethernet (RJ45 connector)
  - Six CAN-FD interfaces
  - Two LIN interfaces
- Camera:
  - Three CSI2-RX camera interfaces (custom interface/dual-QSH connectors)
- Audio:
  - 3.5mm stereo input and output
- Expansion/add-on:
  - Two PCIe/Gen3 4L card slots (1x with 4Lane support, 1x with 2L support)
  - Multiple pin headers for ADC, I2C, I3C, and SPI access
- User control/indication:
  - Pushbuttons (resets, power modes, user defined)
  - LEDs (power, user defined, serial port)
  - User configurations (boot mode, USB mode)
  - External or onboard emulator support (MIPI-60 w/ adapters to 14-pin or 20-pin CTI)

The EVM images identify the locations of these key features and user interfaces (top and bottom view).

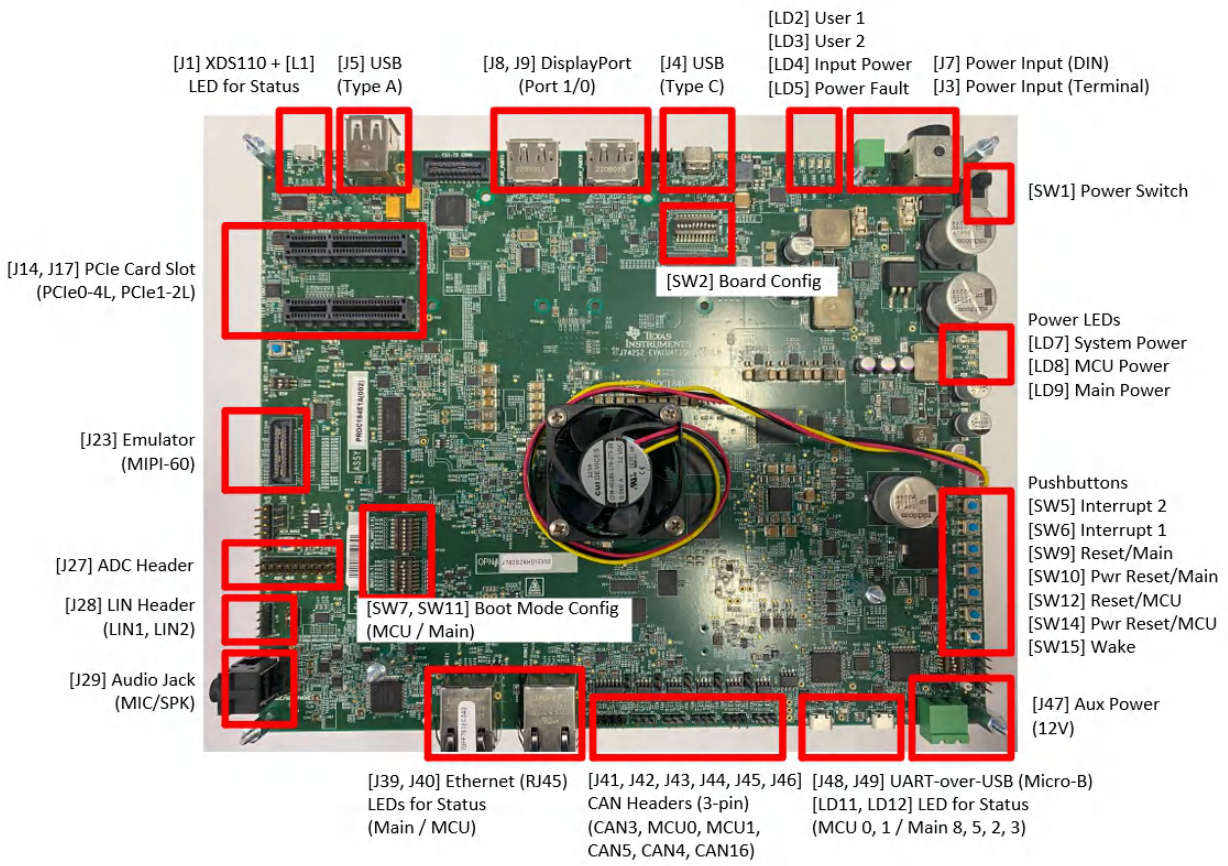


Figure 2-1. Key Features and Interfaces (Top)

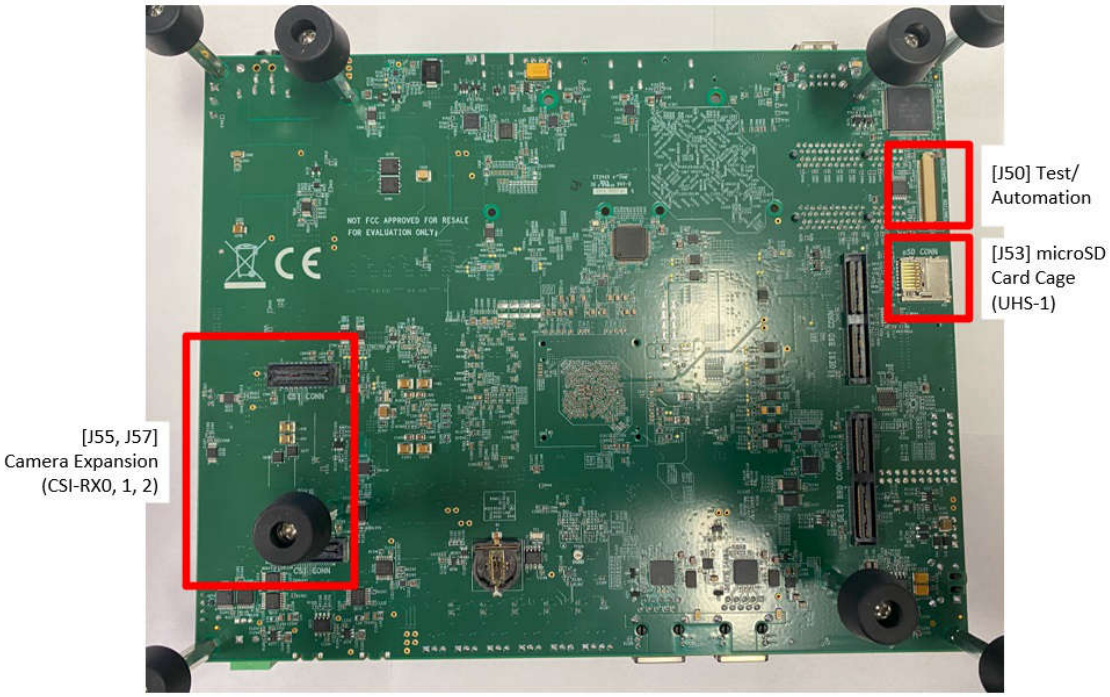


Figure 2-2. Key Features and Interfaces (Bottom)

2.2 Power On/Off Procedure

The below procedure is a brief summary of the steps required to power on and off the EVM. For more in-depth information, please refer to follow-on sections of this guide.

Power ON Procedure

1. Set the boot dip switches of the EVM [SW7, SW11] to the desired boot mode. See Boot Configuration Settings for additional information on how to configure the boot mode of the EVM. By default, switches should be set to boot from MicroSD card.
2. Connect the boot media (if applicable).
3. Attach the power supply cable to the power input connector [J7] of the EVM. See Section 2.3 for additional information on power supply requirements.
4. Connect the power supply to power source (AC power outlet or other).
5. Visually inspect the Input Power LED [LD4] is illuminated (color green).
6. Toggle/Move the power switch [SW1] from the OFF position to the ON position.
7. Visually inspect the power LEDs [LD7, LD8, LD9] are illuminated (color green).

Power OFF Procedure

1. Toggle/Move the power switch [SW1] from the ON position to the OFF position.
2. Visually inspect the power LEDs [LD7, LD8, LD9] are not illuminated.
3. (Optional) Disconnect your power supply from power source (AC power outlet or other).
4. If Step 3 performed, then visually inspect the power LED [LD4] is not illuminated.
5. (Optional) Remove the power supply cable from the EVM [J7].

2.3 Power Input

A power supply is not included with the EVM and must be purchased separately. The requirements for the external power supply/accessory are:

- Nominal Output Voltage: 24-48 VDC
- Output Power Capacity: 100-160 W (depending on use case and connected peripherals)
- Efficiency Level V

Note

TI recommends using and external power supply or power accessory which complies with the applicable regional safety standards such as (by example) UL, CSA, VDA, CCC, PSE, etc.

2.3.1 Power Supply

The EVM supports two separate power input connectors [J7] [J3], either of which can be used to power the system. (Note both must not be used as the same time, as connecting power supply outputs together can cause damage to the EVM and power supplies.) The input can accept a wide range of voltages (20 to 48 VDC). The exact power required for the EVM is largely dependent on the application and connected peripherals. There are many power supply manufactures and models available in the market, and testing the EVM with every combination is not possible. The table below lists several recommended supplies tested with the EVM.

Table 2-1. Recommended External Power Supply

Manufacturer	Part #/Model #	Description	Ordering Information
CUI Inc.	SDI120-24-UC-P51	AC/DC DESKTOP ADAPTER 24V 120W	102-4664-ND [Digikey part#]
CUI Inc.	SDI160-48-UC-P51	AC/DC DESKTOP ADAPTER 48V 158W	SDI160-48-UC-P51-ND [Digikey part#]

A green power led [LD4] is illuminated when a valid power source is connected to either power input. A red power led [LD5] is illuminated when a power source not within the correct voltage range (less than 22 VDC or greater than 52 VDC).

2.3.2 Power Control

The EVM supports a manual switch [SW1] for power control to the EVM. The switch [SW1] is a two-position switch. The OFF position disconnects input power from on-board circuitry. The ON position connects the input power.

Three status LEDs [LD7][LD8][LD9] are used to communicated power status to the user.

Table 2-2. Power Domain Status

LED	'ON' State	'OFF' State
[LD7]	Power switch [SW1] is in the ON position, and input power is being supplied to the EVM.	Power switch [SW1] is in the OFF or there is some other issue causing power to not be supplied.
[LD8]	MCU domain of the EVM is powered	MCU domain of the EVM is not powered/OFF (1)
[LD9]	MAIN domain of the EVM is powered	MAIN domain of the EVM is not powered/OFF (1)

Note

The power management IC (PMIC) includes functions to monitor power domains, including over/under voltage, over current, and residual voltage. If the PMIC detects and error, then the PMIC can transition to *safe-mode* where the PMIC powers down both the MCU and MAIN domains.

2.3.3 Power Budget Considerations

The exact power required for the EVM is largely dependent on the application, usage of the on-board peripherals, and power needs of the add-on devices. Table 2-3 shows the design's power allocations. Again, the input supply must be capable of supplying the power needs of your application.

Table 2-3. Power Allocation

Function	Power	Description
Processor core	Up to 50W	Processor, DDR memory
Onboard peripherals	Up to 10W	SD Card, Ethernet, boot logic, non-volatile memory
USB ports	Up to 15W	Type A ports, Type-C
Displays	Up to 3W	DisplayPort panels, DP transceivers
Expansion interfaces	Up to 50W	2x PCIe, camera expansion

2.4 User Inputs and Settings

The EVM supports several mechanisms for the user to configure, control, and provide input to the system.

2.4.1 Boot Configuration Settings

The boot mode for the EVM is defined by two banks of dip switches [SW7, SW11]. These switch settings are mapped directly to the BOOTMODE pins of the processor. See the technical reference manual (TRM) of the processor for a complete definition of all supported boot modes.

Note

An OFF setting provides a logic low level ('0') and an ON setting provides a logic high level ('1'). The Test Automation Interfaces provides capability to over-ride these switch settings, but that advanced feature not discussed in this manual.

As shown in the diagram, the BOOTMODE order is reversed from the Dip Switch assignment. For example, MCU_BOOTMODE [2:0] selects the PLL configuration. The EVM uses a 19.2Mhz clock source, thus MCU_BOOTMODE [2:0] must be set to '000'. The EVM assigns MCU_BOOTMODE [1:0] to '00'. Dip switch SW7[1] maps to MCU_BOOTMODE [2] and must be set to OFF or '0'.

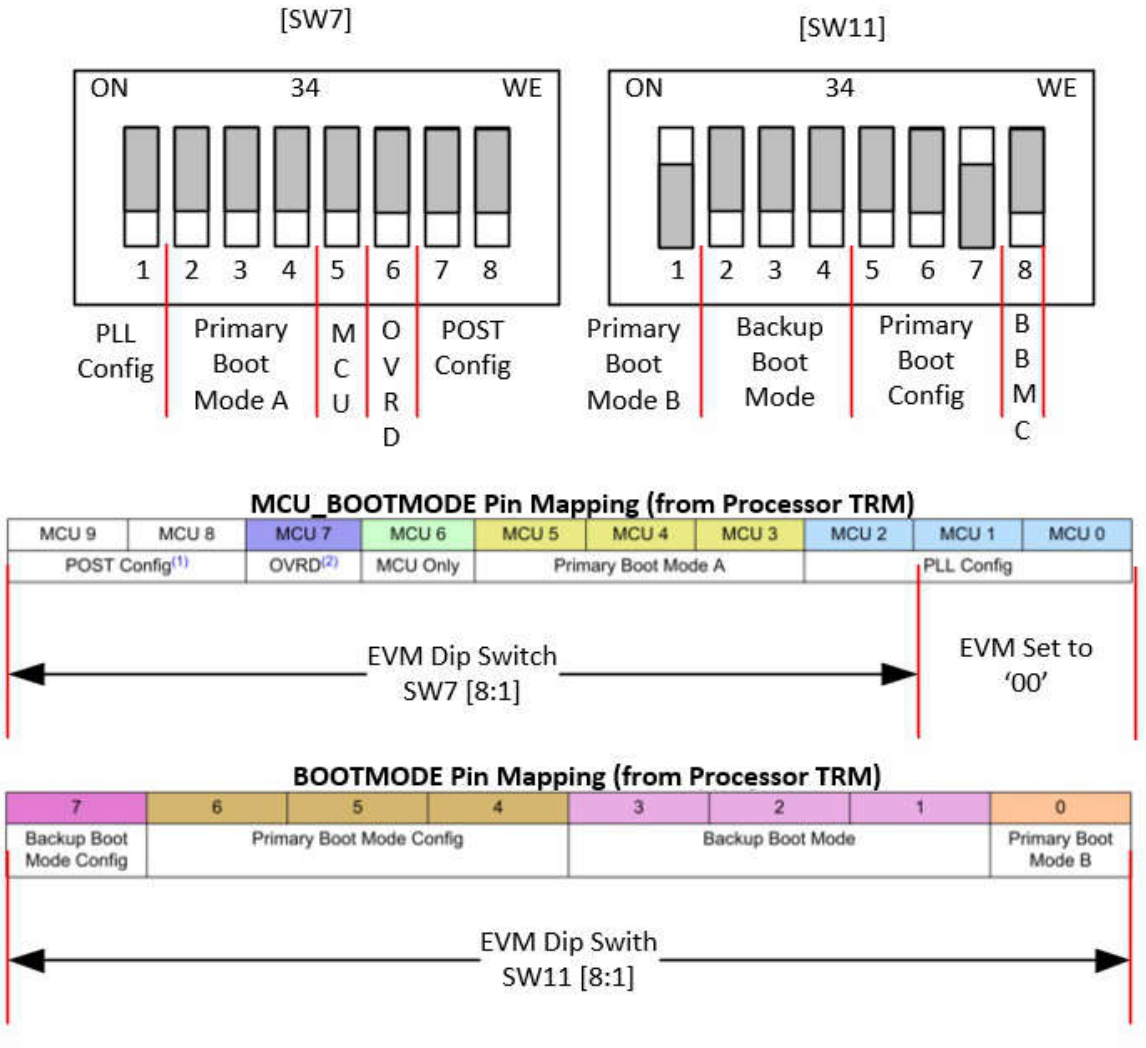


Figure 2-3. Dip Switch [SW7, SW11] Mapping to Boot Mode

The default setting of the EVM is configured for Micro SD card boot. The boot settings are:

SW7[1:8] = 0000 0000, SW11[1:8] = 1000 0010

Another common boot configuration is No-Boot. This is used when downloading code using an emulator/ XDS110. That boot settings is:

SW7[1:8] = 0111 000, SW11[1:8] = 1000 1000

Other boot modes such as eMMC, Serial Flash, USB, Ethernet, and UART are supported. Please refer to processor's TRM for specific settings and complete list of supported modes.

2.4.2 Board Configuration Settings

Dip switches [SW2] [SW4] [SW13] [SW16] are used to configure different options available on the EVM. The tables below lists each switch and the assigned function and definition.

Table 2-4. Board Configuration Settings [SW2] [SW13]

[SW2] Position	Function	Description
SW2.1	Octal-SPI Memory Selection	(OFF) = xSPI NOR Memory is selected (default) (ON) = Octal-NAND is selected
SW2.2	Debug/Trace Enable	(OFF) = Standard Features of EVM are selected or enabled (ON) = Debug/Trace is enabled to MIPI-60 emulation interface (default)
SW2.[4:3]	USB Type C Mode Selection	(OFF/OFF) = DFP (Downstream Facing Port) (Default) (OFF/ON) = DRP (Dual Role Port) (ON, Don't Care) = UFP (Upstream Facing Port)
SW2.5	PCIe0 Mode Selection	(OFF) = Root Complex (default) (ON) = End Point
SW2.6	PCIe1 Mode Selection	(OFF) = Root Complex (default) (ON) = End Point
SW2.7	IO Voltage for Serial Camera Add-on Boards	(OFF) = IO Levels are set to 3.3VDC (ON) = IO Levels are set to 1.8VDC (default)
SW2.8	Test Automation Selection	(OFF) = Test Automation is controlled from TIVA micro (XDS110) (ON) = Test Automation is controlled from dedicated connector [J50] (default)
SW2.9	EVM Configuration EEPROM Write Protection	(OFF) = Configuration EEPROM can be updated (ON) = Configuration EEPROM cannot be updated/is protected (default)
SW2.10	User Defined, maps to GPIO for access (see IO tables)	(OFF) = User Defined (ON) = User Defined (default)
SW13.1	LIN1 Controller/Target Mode Selection	(OFF) = Target Mode (default) (ON) = Controller Mode
SW13.2	LIN2 Controller/Target Mode Selection	(OFF) = Target Mode (default) (ON) = Controller Mode

Note

A variety of signals multiplex with the Debug/Trace interface on the processor. If Trace is enabled, then the some peripheral interfaced can be impacted, including: Audio, CAN Bus 4/5, and RGMII1 Ethernet.

Table 2-5. Test Mode Configuration Settings

[SW16] Position	Default	Function	Description
SW4.1	OFF	Reserved / Test Mode (Wait-In-Reset)	Reserved, Must set to (OFF) for normal EVM operation (only used in Test Mode)
SW4.2	OFF	Reserved / Test Mode (Wait-In-Reset)	Reserved, Must set to (OFF) for normal EVM operation (only used in Test Mode)
SW16.1	ON	Reserved / Tests Mode (PMIC Enable)	Reserved, Must set to (ON) for normal EVM operation (only used in Test Mode) (OFF) = Disable PMIC (Do Not Use) (ON) = Enable PMIC
SW16.2	ON	Reserved / Test Mode (VMonitor Enable)	Reserved, Must set to (ON) for normal EVM operation (only used in Test Mode) (OFF) = Disable Voltage Monitor (Do Not Use) (ON) = Enable Voltage Monitor
SW16.3	ON	Reserved / Test Mode (Disable)	Reserved, Must set to (ON) for normal EVM operation (OFF) = Enable Test Mode (Do Not Use) (ON) = Disable Test Mode
SW16.4	ON	PMIC Watchdog Disable	(OFF) = Watchdog Timer is Enabled. (Note this can cause processor reset if watchdog is not managed.) (ON) = Watchdog Timer is Disabled (default)

2.4.3 Reset Pushbuttons

When pressed, the specific EVM domain is issued a reset, and is held in reset until the button is released.

Table 2-6. Reset Pushbuttons

Push Button	Domain	Function	Description
[SW14]	All	Power-On Reset	Power-on/cold reset for EVM, resets both processor domains (MCU, MAIN) and all EVM peripherals
[SW12]	MCU	MCU Warm Reset	Warm reset for MCU domain
[SW10]	MAIN	Power-On Reset	Power-on/cold reset for MAIN domain, MCU domain is unaffected
[SW9]		Warm Reset	Warm reset for MAIN domain, MCU domain is unaffected

2.4.4 User Pushbuttons

The pushbuttons primary function is to be user and application defined. The inputs can be monitored and configured to generate an interrupt. Some pushbuttons support a secondary function. Some pushbuttons can be used to wake the system from a low power mode. The table below lists a complete definition for each pushbutton.

Table 2-7. User Pushbuttons and LEDs

Push Button	Primary Function	Alternate Function
[SW3]	User Defined (GPIO0_11)	Wake from low power mode (MAIN IO_RET)
[SW5]	User Defined (WKUP_GPIO0_7)	Wake from software initiated power-down (OFF)
[SW6]	User Defined (GPIO0_0)	External Interrupt (EXTINTn)
[SW8]	User Defined (WKUP_GPIO0_70)	Wake from low power mode (MCU IO_RET)
[SW15]	User Defined (PMIC_GPIO4)	Wake from low power mode (any LP_STBY).
LED	**Primary Function**	**Alternate Function**
[LD2]	User Defined (IO_EXP 0x22, bit P26)	None
[LD3]	User Defined (IO_EXP 0x22, bit P27)	None

Note

The user-defined pushbutton inputs and LED outputs are connected to processor pins and/or IO expanders. The pins can be accessed via GPIO functions of the pin or controlled via I2C commands. The specific pin/GPIO used is identified in the table.

2.5 Standard Interfaces

The EVM provides industry standard interfaces/connectors to connect with a wide variety of peripherals. As these interfaces are standard, pin specific information is not provided in this document.

2.5.1 Audio Input and Output

The EVM supports stacked 3.5mm jacks [J29] for audio input and output. Texas Instruments PCM3168A codec provides the audio conversion with sampling rates up to 96KHz ADC/192KHz DAC(ADC and DAC). The top jack supports stereo microphone (with Mic bias) and the bottom jack supports stereo headphone outputs.

2.5.2 Display Port Interfaces

The EVM supports two DisplayPort panels via standard DP cables interfaces [J8] [J9]. The processor's native DP [J9] supports resolutions up to 4K UHD (3840x216) and includes MST (Multi-Stream Transport) for connecting multiple panels. The second DisplayPort [J8] is supported via DP bridge device (SN65DSI86) and supports resolutions up to 1080p. The second DisplayPort (via bridge device) does not support integrated audio.

2.5.3 Gigabit Ethernet

Two wired Ethernet networks are supported via RJ45 cable interfaces [J39] [J40]. Both are compatible with IEEE 802.3 10BASE-Te, 100BASE-TX, ad 1000BASE-T specification. The connector includes LEDs for link status and activity. The Ethernet PHY supported on the EVM is Texas Instruments DP83867E.

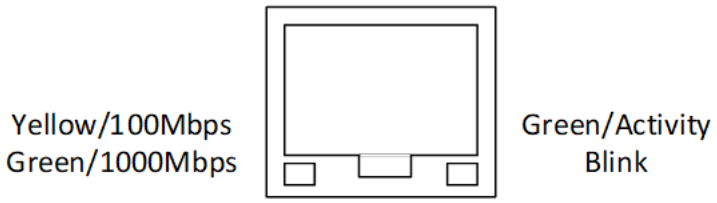


Figure 2-4. RJ45 LED Indicators [39] [J40]

Power-Over-Ethernet (PoE) is not supported.

2.5.4 JTAG/Emulation Interface

The EVM supports an integrated XDS110 emulator for loading and debugging software. The USB micro-B connector [J1] of the EVM is connected to a Host-PC using supplied USB cable (Type-A to Micro-B). The computer can use Texas Instruments' Code Composer Studio (CCS) to establish a connection with the processor and download and debug software on the various processor cores. The emulator circuit is powered via USB VBUS power. LEDs [LD1] [LD6] are used to indicate an active connection with Host-PC/processor. The green LED [LD6] indicates USB connection with Host-PC and the red LED [LD1] indicates processor connection with CCS.

Optionally, an external JTAG emulation/debugger can connect using a dedicated emulation connector [J23]. The connector is aligned with the MIPI 60-pin Emulator standard and expands the debug capability to include TRACE support. Several different Texas Instruments' emulators can be used, including XDS560v2, XDS110, and XDS200. Note that some can require 3rd party adapters for interfacing with the MIPI-60 connector.

Selection between the on-board and external emulator is done automatically, while switching to external emulator is only when connection is made to the MIPI-60 connector [J23].

2.5.5 MicroSD Card Cage

The EVM supports a micro-SD card cage [J53]. The EVM supports UHS-1 class memory cards, including SDHC and SXDC. The connector is a push-push connector, meaning your push to insert the card and push again to eject the card.

A micro-SD card (blank) is included with the EVM.

2.5.6 PCIe Card Slot

The EVM supports two 4Lane PCIe Card slots for interfacing with full size PCIe cards. PCIe0 interface [J14] supports the full 4 Lanes up to Gen3 data rates, while PCIe1 interface [J17] bandwidth is reduced to 2 Lanes (at Gen3 data rates). The PCIe1 interfaces [J17] requires the processor to generate the REFCLK (100MHz). For PCIe0 [J14], the REFCLK is automatically generated (on-board).

The EVM can supply up to 25W per PCIe interface, which complies with the PCIe specification.

2.5.7 UARTs for Terminal/Logging

Six UART ports are provided for terminal and logging functions using two UART-over-USB transceivers. When the USB micro-B connectors [J48] or [J49] of the EVM are connected to a Host-PC using supplied USB cable (Type-A to Micro-B), the computer can establish Virtual Com Ports to be used with any terminal application. Virtual Com Port drivers for the transceivers can be obtained from FTDI Chip.

Once installed, the Host-PC creates the Virtual Com Ports (two ports for FT2232, four ports for FT4232). Depending on the other Host-PC resources available, the Com Ports are not located at COM1-2 or COM3-6. However, the ports remain in the same numerical order for each transceiver.

Table 2-8. UART to COM Port Mapping [J48] w/ Status [LD11]

UART Port	Host-PC COM Port
MCU_UART0	COM 1
WKUP_UART0	COM 2

Table 2-9. UART to COM Port Mapping [J49] w/ Status [LD12]

UART Port	Host-PC COM Port
UART8	COM 1
UART5	COM 2
UART2	COM 3
UART3	COM 4

The circuits are powered from USB bus power and therefore the COM connection are not lost when the EVM power is removed. LEDs [LD11] [LD12] are used to indicated an active COM connection with Host-PC. The EEPROM of FTDI bridges are programmed with the EVM serial number, allowing users to identify the connected COM port with board serial number when one or more boards connected a single computer.

Note

The maximum length for the IO cables must not exceed three meters.

2.5.8 USB Interface

The EVM supports one USB3.1 Gen1 Type C interface [J4], which can function as DFP, UFP, or DRP. The configurable modes provide support for the USB boot modes of the processor. For details on how to select the USB mode, see Section 2.4.2. The VBUS output for this port is limited to 1.5A. When operating as UFP, the EVM cannot be powered from this port.

The EVM also supports two USB2.0 Type A interfaces [J5] via an on-board USB hub. These ports can only function as Host. The VBUS output for each port is limited to 0.5A.

The processor supports a single USB interface. Therefore, the user must configure for either the USB3.1 Type C interface or the USB2.0 Type A interface. Both cannot be operated simultaneously

Note

The USB2.0 Micro-B connectors [J48] [J49] and [J1] are discussed in the UART-over-USB and Emulation sections. These are USB interfaces dedicated to peripherals and cannot be used for generic USB peripherals.

2.6 Expansion Interfaces

The EVM provides several expansion interfaces that have non-standard/custom pinouts. Each of these interfaces are introduced and specific pin information is provided.

Note that some of the interfaces include ‘Direction’ information. This is relative to the EVM, so INPUT is input to the EVM/output of the connected device. OUTPUT is output of the EVM/input to the connected device.

2.6.1 Accessory Power Connector

A power output connector [J47] is provided for conditions where an expansion board requires additional power. The 2-pin connector (Phoenix 1757242) supplies a regulated 12V output, up to 5000mA.

Table 2-10. Accessory Power Connector [J47]

Pin #	Pin Name	Description	Dir
1	GND	Ground	
2	Power	Power, 12V	Output

2.6.2 Analog-to-Digital Conversion

The EVM supports a interface for connecting external peripherals with ADC inputs. A 20-pin, dual row, 2.54mm pitch pin header [J27] supports eight input channels to ADC0, two channels to ADC1, and trigger, and ADC reference signals.

Table 2-11. Analog-to-Digital Expansion Pin Definition [J27]

Pin #	Pin Name	Description Processor Resource for [J57] / [J55]	Dir
1	GND	Ground	
2	ADC0_AIN3	ADC Instance 0, Channel 3	Input
3	ADC0_AIN7	ADC Instance 0, Channel 7	Input
4	ADC0_AIN0	ADC Instance 0, Channel 0	Input
5	ADC0_AIN1	ADC Instance 0, Channel 1	Input
6	ADC0_AIN6	ADC Instance 0, Channel 6	Input
7	GND	Ground	
8	GND	Ground	
9	ADC0_AIN4	ADC Instance 0, Channel 4	Input
10	ADC0_REFP	ADC Reference Voltage, Positive	Input
11	ADC0_AIN2	ADC Instance 0, Channel 2	Input
12	ADC0_REFN	ADC Reference Voltage, Negative	Input
13	GND	Ground	
14	GND	Ground	
15	ADC0_AIN5	ADC Instance 0, Channel 5	Input
16	ADC_TRIGGER	Conversion Trigger, configurable to ADC Instance 0 or 1	Input
17	ADC1_AIN0	ADC Instance 1, Channel 0	Input
18	ADC1_AIN1	ADC Instance 1, Channel 1	Input
19	GND	Ground	
20	GND	Ground	

2.6.3 Camera Interface

The EVM includes dual 40-pin (2x20, 0.5mm pitch) high speed connectors [J57] [J55] for connecting with cameras and other image capture devices. Each expansion connectors can support up to two MIPI-DPHY CSI2 interfaces. The bandwidth of each CSI2 interface is 10Gbps (each CSI2 port supports 4 data lanes each lanes up to 2.5Gbps). The expansion connectors also includes power and other IO for communicating with the capture devices. All control signals are configurable for 3.3V or 1.8V IO voltage levels. See Section 2.4.1 for configuration details.

Table 2-12. High Speed Camera Expansion Pin Definition [J57][J55]

Pin #	Pin Name	Description Processor Resource for [J57] / [J55]	Dir
1	Power	Power, 12V	Output
2	I2C_SCL	I2C Bus Clock (I2C5)	Bi-Dir
3	Power	Power, 12V	Output
4	I2C_SDA	I2C Bus Data (I2C5)	Bi-Dir
5	CSIa_CLK_P	CSI Port 0 / Port 2	Input
6	GPIO0/PWMA	IO Expander 0x20 bit P1 / Open	Output
7	CSIa_CLK_N	CSI Port 0 / Port 2	Input
8	GPIO1/PWMV	IO Expander 0x20 bit P2 / bit P4	Bi-Dir
9	CSIa_D0_P	CSI Port 0 / Port 2	Input
10	REFCLK	25MHz Reference Clock	Output
11	CSIa_D0_N	CSI Port 0 / Port 2	Input
12	GND	Ground	
13	CSIa_D1_P	CSI Port 0 / Port 2	Input
14	RESETz	GPIO, IO Expander 0x20 bit P0	Output
15	CSIa_D1_N	CSI Port 0 / Port 2	Input
16	GND	Ground	
17	CSIa_D2_P	CSI Port 0 / Port 2	Input
18	GPIO2	GPIO0_26 / IO Expander 0x20 bit P5	Bi-Dir
19	CSIa_D2_N	CSI Port 0 / Port 2	Input
20	GPIO3	IO Expander 0x20 bit P3 / bit P6	Bi-Dir
21	CSIa_D3_P	CSI Port 0 / Port 2	Input
22	GPIO4	GPIO0_28 / IO Expander 0x20 bit P7	Bi-Dir
23	CSIa_D3_N	CSI Port 0 / Port 2	Input
24	GND	Ground	
25	CSIb_CLK_P	CSI Port 1 / Open	Input
26	CSIb_D3_P	CSI Port 1 / Open	Input
27	CSIb_CLK_N	CSI Port 1 / Open	Input
28	CSIb_D3_N	CSI Port 1 / Open	Input
29	CSIb_D0_P	CSI Port 1 / Open	Input
30	Power	Power, 3.3V	Output
31	CSIb_D0_N	CSI Port 1 / Open	Input
32	Power	Power, 3.3V	Output
33	CSIb_D1_P	CSI Port 1 / Open	Input
34	Power	Power, 3.3V	Output
35	CSIb_D1_N	CSI Port 1 / Open	Input
36	Power	Power, 3.3V	Output
37	CSIb_D2_P	CSI Port 1 / Open	Input
38	Power	Power, IO Level (1.8V or 3.3V)	Output
39	CSIb_D2_N	CSI Port 1 / Open	Input

Table 2-12. High Speed Camera Expansion Pin Definition [J57][J55] (continued)

Pin #	Pin Name	Description Processor Resource for [J57] / [J55]	Dir
40	Power	Power, IO Level (1.8V or 3.3V)	Output

2.6.4 CAN-Bus Interface

The EVM supports up to six (6) CAN Bus interfaces.

Table 2-13. CAN-FD Interface Assignment

Connector	Process Resource
J41	CAN3
J42	MCU CAN0
J43	MCU CAN1
J44	CAN5
J45	CAN4
J46	CAN16

Each Controller Area Network (CAN) Bus interface is supported on a 3-pin, 2.54mm pitch header. The interface meets ISO 11898-2 and ISO 11898-5 physical standards, and supports CAN and optimized CAN-FD performance up to 8Mbps. Each includes CAN Bus end-point termination. If the EVM is included in a network with more than two nodes, then the termination can need to be adjusted.

Table 2-14. CAN-FD Header Pin Definition [J41-J46]

Pin #	Pin Name	Description	Direction
1	CAN-H	High-Level CAN Bus Line	BI-Dir
2	GND	Ground	
3	CAN-L	Low-Level CAN Bus Line	Bi-Dir
4	WAKE (J41 only)	Assert PHY Wake Function	Input

2.6.5 Fan Header

The heat sink supports cooling of the device at ambient temperatures. If the environment or use case requires additional cooling, then a fan can be added to the heat sink.

The fan connector is a 3-pin header (440054-3 from TE Connectivity), and supports 12VDC fans. Mating connector is 440129-3 and 1735801-1.

Table 2-15. Fan Header Pin Definition [J24]

Pin #	Pin Name	Description	Direction
1	<open>	Unconnected	n/a
2	12V	12V Supply	Output
3	GND	Ground	

2.6.6 LIN-Bus Interface

The EVM supports up to two LIN Bus interfaces. The Local Interconnect Network (LIN) is a single wire bidirectional bus used for low speed in-vehicle networks. The two EVM interfaces are supported on a 4-pin, 2.54mm pitch header [J28]. The interface meets LIN 2.2A and ISO/DIS17987-4.2 physical standards, and supports rates up to 100kbps, and is designed to support 12V applications. Each LIN interface has option of being controller or target. See Section 2.4.2 for configuration details.

Table 2-16. LIN Header Pin Definition [J28]

Pin #	Pin Name	Description	Direction
1	VBUS_LIN	LIN Bus Power (4V-45V)	Input (optional)
2	LIN #1	Interface using UART6	Bi-Dir
3	LIN #2	Interface using UART9	Bi-Dir

Table 2-16. LIN Header Pin Definition [J28] (continued)

Pin #	Pin Name	Description	Direction
4	GND	Ground	

2.6.7 Test and Automation Control Interface

The EVM supports an interface to allow for automated control of the system, including functions like on/off, reset, and boot mode settings.

Table 2-17. Test Automation Interface Pin Definition [J50]

Pin #	Pin Name	Description	Dir
1	Power	Power, 3.3V	Output
2	Power	Power, 3.3V	Output
3	Power	Power, 3.3V	Output
4-6	<open>		
7	GND	Ground	
8-15	<open>		
16	GND	Ground	
17-24	<open>		
25	GND	Ground	
26	POWERDOWNz	EVM Power Down	Input
27	PORz	EVM Power-On/Cold Reset (MCU_PORz)	Input
28	RESETz	EVM Warm Reset (RESETz)	Input
29	<open>		
30	INT1z	EXTINT / GPIO0_0	Input
31	INT2z	WKUP_GPIO0_7	Bi-Dir
32	<open>		
33	BOOTMODE_RSTz	Bootmode Buffer Reset	Input
34	GND	Ground	
35	<open>		
36	Bus #1 I2C_SCL	INA Bus #1 I2C (optional connection to Processor I2C1)	Bi-Dir
37	Bus #2 I2C_SCL	INA Bus #2 I2C	Input
38	Bus #1 I2C_SDA	INA Bus #1 I2C (optional connection to Processor I2C1)	Bi-Dir
39	Bus #2 I2C_SDA	INA Bus #2 I2C	Bi-Dir
40	GND	Ground	
41	GND	Ground	
42	GND	Ground	

Note

The Signal polarity is defined with a trailing 'z' in the Pin Name, which indicates the signal is active LOW. For example, POWERDOWNz is an active low signal, meaning '0' = EVM is Powered Down, '1' = EVM is NOT Powered Down.

2.7 Circuit Details

This sections provides additional details on the EVM design and processor connections. The top level block diagram shows the overall connectivity of the EVM (Section 1.4).

2.7.1 Interface Mapping

The EVM interface mapping tables is provided in Table 2-18.

Table 2-18. Interface Mapping

Connected Peripheral	Processor Resources	Component/Part Numbers
Memory, LPDDR4 DRAM	DDR0, DDR1	(2x) Micron, MT53E2G32D4DE-046 AUT:C
Memory, xSPI NOR Flash	MCU_OSPI0	Cypress, S28HS512TGABHM010
Memory, Octal NAND	MCU_OSPI0	Winbond, W35N01JWTBAG
Memory, Quad SPI NOR Flash	MCU_OSPI1	Micron, MT25QU512ABB8E12-0SIT
Memory, eMMC	MMC0	Micron, MTFC16GAPALBH-AAT ES
Memory, microSD Card	MMC1	
EEPROM, Board Identification	WKUP_I2C0	On-Semi, CAT24C256WI-GT3
EEPROM, Boot	MCU_I2C0	Microchip Tech, AT24CM01
Memory, UFS 2L Gear3	UFS0	Toshiba, THGAF8G8T23BAIL
Wired Ethernet	MCU_RGMII1, RGMII1	(2x) Texas Instruments, DP83867ERGZT
USB Type C + CC Controller	USB0 + SERDES0 (L2, L3)	Texas Instruments, TUSB321RWBR
USB Type A (2x)	USB0	Texas Instruments, TUSB4041IPAP
Audio Codec	McASP0	Texas Instruments, PCM3168APAP
PCIe 4L Card Slot	PCIe1 / SERDES0 (L0, L1)	
PCIe 4L Card Slot	PCIe0, SERDES1	
Quad USART Terminal	UART 8,5,2 & 3	FTDI, FT4232HL
Dual USART Terminal	WKUP_UART0, MCU_UART0	FTDI, FT2232HL
CAN (6x)	MCU_MCAN0, MCU_MCAN1, MCAN4, MCAN5, MCAN16	Texas Instruments, TCAN1042HGVD
	MCAN3	Texas Instruments, TCAN1043-Q1
LIN (2x)	UART6, UART9	Texas Instruments, TLIN1022DMTTQ1
CSI RX Interface	CSI0, CSI1, CSI2	QSH Connector-J57(QSH-020-01-L-D-DP-A-K)
Display Port	DP0	
	DSI0	Texas Instruments, SN65DSI86IPAPQ1
ADC Header	MCU_ADC0	

Note

MCU_OSPI1 is connected to two different flash memories, targeted memory selected via a mux.

2.7.2 Shared Interfaces / Signal Muxing

Due to the number of features available on the EVM, there are some limitations for which features can be used simultaneously. Many of the conflicts revolve around the emulation/trace functionality. When trace is selected/ enabled, the following features are not accessible: Audio, Power Measurement (access from processor), LIN Bus, reduce CAN-FD availability (only MCU and MCAN16 available), as well as few other items. See schematic for a complete definition of interfaces which share resources.

2.7.3 I2C Address Mapping

Table 2-19 provides the complete I2C address mapping details supported on the EVM.

Table 2-19. I2C Mapping

Connected Peripheral	Processor Resources		Component / Part Number
	I2C Port	I2C Address	
EEPROM, Board Identification	WKUP_I2C0	0x50	On-Semi, CAT24C256WI-GT3
Power Management IC (PMIC)	WKUP_I2C0	0x48-4B	Texas Instruments, TPS659413
Power Management IC (PMIC)	WKUP_I2C0	0x40, 0x43	(2x) Texas Instruments, TPS62873
Voltage Monitor	WKUP_I2C0	0x30, 0x31	(2x) Texas Instruments, PPS38900603NRTERQ1
Temperature Sensors	MCU_I2C0	0x48, 0x49	Texas Instruments, TMP100NA/3K
EEPROM, Boot	MCU_I2C0	0x50, 0x51	Microchip Tech, AT24CM01
PCIe0 / PCIE1 Card Slots	I2C0	0x70, Add-On	Texas Instruments, TCA9543APWR
RTC Clock	I2C0	0x57,0x6F	Microchip, MCP79410-I/SN
Clock Generator, SERDES	I2C0	0x77,0x76	Texas Instruments, CDCI6214
Clock Generator, Peripherals	I2C0	0x6D	Texas Instruments, CDCEL937-Q1
I2C IO Expander, 16b	I2C0	0x20	Texas Instruments, TCA6416ARGJR
I2C IO Expander, 24b	I2C0	0x22	Texas Instruments, TCA6424ARGJR
ADC, Power Measurement	I2C1	0x40 to 0x4F	Texas Instruments, INA226
I2C IO Expander, 8b	I2C3	0x20	Texas Instruments, TCA6408ARGTR
Audio Codec	I2C3	0x44	Texas Instruments, PCM3168A-Q1
I2C IO Expander, 8b	I2C4	0x20	Texas Instruments, TCA6408ARGTR
DisplayPort, Bridge	I2C4	0x2C, Add-On	Texas Instruments, SN65DSI86IPAPQ1
Expansion, Camera	WKUP_I2C0, I2C5	Add-On	

2.7.4 GPIO Mapping

The General Purpose IOs (GPIO) of the EVM are broken into two major groups, IO connected to processor or connected to I2C-based Expander and are separated into two tables below.

Table 2-20. Processor Controlled GPIO

J784S4 GPIO	Function	DIR/Level	Remarks
WKUP_GPIO0_1	Boot EEPROM Write Protect	Output	'0' – Memory is NOT Write-Protected '1' – Memory is Write-Protected (default)
WKUP_GPIO0_2	MCU CAN Bus #1 Stand-by	Output	'0' – Normal Mode '1' – Standby Mode (default)
WKUP_GPIO0_3	MCU CPSW2G Ethernet Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Requested (default)
WKUP_GPIO0_6	SPI Flash Memory Selection	Bi-Dir	'0' – xSPI NOR Flash is selected '1' – Octal-NAND Flash is selected (Note Default is set via dip switch)
WKUP_GPIO0_7	Pushbutton [SW5] System / User Interrupt	Input	'0' – Pushbutton is pressed '1' – Pushbutton is NOT pressed (default)
WKUP_GPIO0_28	USB Type C Cable Orientation	Input	'0' – Low Position Detected (Default) '1' – High Position Detected
WKUP_GPIO0_39	Power Management IC (PMIC) Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Requested (default)

Table 2-20. Processor Controlled GPIO (continued)

J784S4 GPIO	Function	DIR/Level	Remarks
WKUP_GPIO0_55	System Power Down	Output	'0' – Normal Operation (default) '1' – System Power Down/Off
WKUP_GPIO0_56	MCU CPSW2G Ethernet Reset	Output	'0' – Ethernet PHY is Reset '1' – Ethernet PHYT is NOT Reset (default)
WKUP_GPIO0_66	Power Measurement Bus Selection	Bi-Dir	'0' – Selects Bus #1 for access to INAs (default) '1' – Selects Bus #2 for access to INAs
WKUP_GPIO0_69	MCU CAN Bus #0 Stand-by	Output	'0' – Normal Mode '1' – Standby Mode (default)
WKUP_GPIO0_70	Pushbutton [SW8] System / User Interrupt	Input	'0' – Pushbutton is pressed '1' – Pushbutton is NOT pressed (default)
WKUP_GPIO0_84	Serial Ethernet Expansion #1 Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Requested (default)
WKUP_GPIO0_85	Serial Ethernet Expansion #2 Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Requested (default)
WKUP_GPIO0_86	IO Expander Interrupt (Bus I2C0)	Input	'0' – Active Interrupt Request '1' – No Interrupt Requested (default)
GPIO_3	DSI/DisplayPort Bridge Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Requested (default)
GPIO_8	SD Card IO Voltage Selection	Output	'0' – SD Card IO Voltage is 1.8V '1' – SD Card IO Voltage is 3.3V (default)
GPIO_11	Pushbutton [SW3] System / User Interrupt	Input	'0' – Pushbutton is pressed '1' – Pushbutton is NOT pressed (default)
GPIO_18	IO Expander Interrupt (Bus I2C5)	Input	'0' – Active Interrupt Request '1' – No Interrupt Requested (default)
GPIO_21	CPSW2G Ethernet Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Requested (default)
GPIO_26	Camera Expansion #1 GPIO #2	Bi-Dir	Camera Expansion Board Specific (Pin 18)
GPIO_28	Camera Expansion #1 GPIO #4	Bi-Dir	Camera Expansion Board Specific (Pin 22)

Note

GPIO functions sometimes share pins with other functions. The default state of these IO are set by the MCU_BOOTMODE and/or BOOTMODE pins. For the EVM, these pins are set via dip switches.

Table 2-21. Expander Controller GPIO

I2C0/TCA6416 Addr: 0x20	Function	DIR/Level	Remarks
P00	PCIe1 Mode Selection	Input	'0' – Processor/PCIe1 is Root Complex '1' – Processor/PCIe1 is End Point (Note Default is set via dip switch)
P01	PCIe1 PERSTz Status	Input	'0' – PCIe1 Reset is asserted '1' – PCIe1 Reset is NOT asserted
P02	PCIe1 PERSTz Output (Root Complex Mode)	Output	'0' – PCIe1 Reset is asserted '1' – PCIe1 Reset is NOT asserted
P03	PCIe1 PERSTz to PORz (End Point Mode)	Output	'0' – PCIe1 PERSTz is separate from PORz '1' – PCIe1 PERSTz can control PORz

Table 2-21. Expander Controller GPIO (continued)

I2C0/TCA6416 Addr: 0x20	Function	DIR/Level	Remarks
P04	PCIe0 Mode Selection	Input	'0' – Processor/PCIe0 is Root Complex '1' – Processor/PCIe0 is End Point (Note Default is set via dip switch)
P05	PCIe0 PERSTz Status	Input	'0' – PCIe0 Reset is asserted '1' – PCIe0 Reset is NOT asserted
P06	PCIe0 PERSTz Output (Root Complex Mode)	Output	'0' – PCIe0 Reset is asserted '1' – PCIe0 Reset is NOT asserted
P07	PCIe0 PERSTz to PORz (End Point Mode)	Output	'0' – PCIe0 PERSTz is separate from PORz '1' – PCIe0 PERSTz can control PORz
P10	PCIe1 Card Presence Detection	Input	'0' – Card detected for PCIe1 '1' – Card NOT detected for PCIe1 (default)
P11	PCIe0 Card Presence Detection	Input	'0' – Card detected for PCIe0 '1' – Card NOT detected for PCIe0 (default)
P12	External Clock enabled for PCIe0	Output	'0' – External Clock is NOT enabled for PCIe0 '1' – External Clock is enabled for PCIe0 (default)
P13	External Clock enabled for PCIe1	Output	'0' – External Clock is NOT enabled for PCIe1 '1' – External Clock is enabled for PCIe1 (default)
P14	McASP (Audio) / CAN Mux Select	Output	'0' – McASP0 is selected to Codec (CAN3, CAN5 are disabled) (default) '1' – CAN3, CAN5 are selected, McASP0 (audio) is disabled
P15	GESI Expansion Mux Control	Output	Reserved (GESI Expansion is not supported)
P16	GESI Expansion Mux Control	Output	Reserved (GESI Expansion is not supported)
P17	GESI Expansion Ethernet Reset	Output	Reserved (GESI Expansion is not supported)
I2C0/TCA6424 Addr: 0x22	**Function**	**DIR/Level**	**Remarks**
P00	Serial Ethernet #1 Expansion Power Down	Output	'0' – Expansion board is active (default) '1' – Expansion board is powered down
P01	Serial Ethernet #1 GPIO1	Output	Expansion Board specific (Pin 46)
P02	Serial Ethernet REFCLK Program Enable	Output	'0' – I2C is not connected to CDC clock def (default) '1' – Expansion board is NOT reset
P03	Serial Ethernet #1 GPIO2	Bi-Dir	Expansion Board specific (Pin 47)
P04	Serial Ethernet #2 Expansion Reset	Output	'0' – Expansion board is RESET (default) '1' – Expansion board is NOT reset
P05	User Dip Switch Input [SW2]	Input	'0' – Dip Switch SW2 position 10 set to OFF '1' – Dip Switch SW2 position 10 set to ON (Note Default is set via dip switch SW2)
P06	User LED [LD2]	Output	'0' – LED [LD2] is ON '1' – LED [LD2] is OFF (default)
P07	User LED [LD3]	Output	'0' – LED [LD3] is ON '1' – LED [LD3] is OFF (default)
P10	Power Measurement Bus Enable	Output	'0' – Enabled access to INA from processor (I2C1) (default) '1' – Disables access to INA from processor

Table 2-21. Expander Controller GPIO (continued)

I2C0/TCA6416 Addr: 0x20	Function	DIR/Level	Remarks
P11	Serial Ethernet #2 Expansion Power Down	Output	'0' – Expansion board is active (default) '1' – Expansion board is powered down
P12	Serial Ethernet #2 GPIO2	Bi-Dir	Expansion Board specific (Pin 47)
P13	External Clock Generator Reset	Output	'0' – Expansion board is RESET '1' – Expansion board is NOT reset (default)
P14	USB0 Mux Select	Output	'0' – USB0 is connected to Type C (default) '1' – USB0 interface is connected Type A (via hub)
P15	Debug/Trace Enable (Note: This setting can affect other interfaces.)	Bi-Dir	'0' – Debug/Trace signals are enabled to MIPI-60 emulation interface [J23] '1' – Debug/Trace signals are NOT enabled to MIPI-60 interface [J23] (Note Default is set via dip switch SW2.2)
P16	Interface Mux Selection #1 (Note: This setting can affect other interfaces.)	Output	'0' – Alternate Interfaces are selected for Mux #1 '1' – Standard Interfaces are selected for Mux #1 (default)
P17	Interface Mux Selection #2 (Note: This setting can affect other interfaces.)	Output	'0' – Alternate Interfaces are selected for Mux #2 '1' – Standard Interfaces are selected for Mux #2 (default)
P20	CPSW2G Ethernet Reset	Output	'0' – Ethernet PHY is Reset '1' – Ethernet PHYT is NOT Reset (default)
P21	Serial Ethernet #2 GPIO1	Output	Expansion Board specific (Pin 46)
P22	SD Card Power Enable/Reset	Output	'0' – SD Card Power is disabled/Reset '1' – SD Card Power is enabled/active (default)
P23	USB Type C Power Enable	Output	'0' – USB Type C Power is disabled '1' – USB Type C Power is enabled (default)
P24	USB Type C Mode Selection	Bi-Dir	'00' = DFP (Downstream Facing Port) '01' = DRP (Dual Role Port)
P25			'1x' = UFP (Upstream Facing Port) (Note Default is set via dip switch [SW2 bits 3:4])
P26	LIN Bus PHY Enable	Output	'0' – LIN Bus PHY is Disabled (default) '1' – LIN Bus PHY is Enabled
P27	CAN Bus #3, #4, #5 Stand-by	Output	'0' – Normal Mode '1' – Standby Mode (default)
I2C3/TCA6408 Addr: 0x20	**Function**	**DIR/Level**	**Remarks**
P00	Audio Codec Enable/Reset	Output	'0' – Audio Codec is disabled/Reset (default) '1' – Audio Codec is enabled/active
P01 – P07	Reserved / Unused	Bi-Dir	Reserved / Unused
I2C4/TCA6408 Addr: 0x20	**Function**	**DIR/Level**	**Remarks**
P00	DisplayPort #0 Power Enable	Output	'0' – DisplayPort Power is disabled (default) '1' – DisplayPort Power is enabled
P01	DisplayPort #1 Power Enable	Output	'0' – DisplayPort Power is disabled (default) '1' – DisplayPort Power is enabled
P02	DisplayPort #1 Transmitter Enable	Output	'0' – DisplayPort Transmitter is disabled (default) '1' – DisplayPort Transmitter is enabled

Table 2-21. Expander Controller GPIO (continued)

I2C0/TCA6416 Addr: 0x20	Function	DIR/Level	Remarks
P03-P07	Reserved / Unused	Bi-Dir	Reserved / Unused
I2C5/TCA6408 Addr: 0x20	**Function**	**DIR/Level**	**Remarks**
P00	Camera Expansion Reset (#1 and #2)	Output	'0' – Camera Expansion is disabled/Reset (default) '1' – Camera Expansion is enabled/active
P01	Camera Expansion #1 GPIO #0	Bi-Dir	Camera Expansion Board Specific (Pin 6)
P02	Camera Expansion #1 GPIO #1	Bi-Dir	Camera Expansion Board Specific (Pin 8)
P03	Camera Expansion #1 GPIO #3	Bi-Dir	Camera Expansion Board Specific (Pin 20)
P04	Camera Expansion #2 GPIO #1	Bi-Dir	Camera Expansion Board Specific (Pin 8)
P05	Camera Expansion #2 GPIO #2	Bi-Dir	Camera Expansion Board Specific (Pin 18)
P06	Camera Expansion #2 GPIO #3	Bi-Dir	Camera Expansion Board Specific (Pin 20)
P07	Camera Expansion #2 GPIO #4	Bi-Dir	Camera Expansion Board Specific (Pin 22)

2.7.5 Power Monitoring

The EVM includes power monitoring and measurement capability for 32 discrete power rails, giving user critical power usage details for optimizing the processor application. The on-board analog-to-digital converters (INA226) are accessed via I2C. The processor can access using I2C1. The test automation [J50] can access the I2C bus, or can be accessed externally via 5-pin header [J30]. Due to the number of rails, the ADCs are split across two I2C buses. Selection of the buses is done via mux setting (see Section 2.7.4).

Table 2-22. Power Monitor Mapping

Bus #1 Address	Power Rail	Nom V	Shunt Value	Bus #2 Address	Power Rail	Nom V	Shunt Value
0x40	Processor MCU VDD (VDD_MCU_0V85)	0.85V	10m-ohm	0x40	Processor IO at 1.8V (VDD_IO_1V8)	1.8V	10m-ohm
0x41	Processor MCU RAM (VDD_MCU_RAM_0V85)	0.85V	10m-ohm	0x41	Processor IO at 3.3V (VDD_IO_3V3)	3.3V	10m-ohm
0x42	(VDA_MCU_1V8)	1.8V	10m-ohm	0x42	Processor Dual Voltage IO (VDD_SD_DV)	DV	10m-ohm
0x43	Processor MCU IO at 3.3V (VDD_MCUIO_3V3)	3.3V	10m-ohm	0x43	LPDDR4 Memory (VDD1) (VDD1_DDR_1V8)	1.8V	10m-ohm
0x44	Processor MCU IO at 1.8V (VDD_MCUIO_1V8)	1.8V	10m-ohm	0x44	(VDD_DDR_SOC_1V1)	1.1V	
0x45	(VDD_CORE_0V8)	N/A	N/A	0x45	(VCCA_3V3_CORE)	3.3V	5m-ohm
0x46	(VDD_RAM_0V85)	0.85V	10m-ohm	0x46	MCU Peripherals at 1.8V (VSYS_MCUIO_1V8)	1.8V	10m-ohm
0x47	(VDD_GPIORET_WK_0V8)	0.8V	10m-ohm	0x47	MCU Peripherals at 3.3V (VSYS_MCUIO_3V3)	3.3V	10m-ohm
0x48	(VDD_CPU_AVS)	N/A	N/A	0x48	(VSYS_IO_1V8)	1.8V	10m-ohm
0x49	(VSYS_GPIORET_IO_3V3)	3.3V	10m-ohm	0x49	(VSYS_IO_3V3)	3.3V	10m-ohm
0x4A	Processor LPDDR IO (VDD_DDR_1V1)	N/A	N/A	0x4A	(VCC_12V0_N)	12V	??m-Ohm
0x4B	(VDD_PHYCORE_0V8)	0.8V	10m-ohm	0x4B	(VSYS_5V0)	5V0	
0x4C	(VDA_PLL_1V8)	1.8V	10m-ohm	0x4C	(VSYS_3V3)	3V3	
0x4D	(VDA_PHY_1V8)	1.8V	10m-ohm	0x4D	(VCCA_3V3_DDR)	3.3V	10m-ohm

Table 2-22. Power Monitor Mapping (continued)

Bus #1 Address	Power Rail	Nom V	Shunt Value	Bus #2 Address	Power Rail	Nom V	Shunt Value
0x4E	(VDA_USB_3V3)	3.3V	10m-ohm	0x4E	(VDA_DLL_0V8)	0.8V	10m-ohm
0x4F	(VDD_GPIORET_IO_3V3)	3.3V	10m-ohm	0x4F	(VCCA_3V3_CPU_AVS)	3.3V	5m-ohm

Note

In the table, the '(_name)' refers to the net name used in the schematic.

2.7.6 Power Delivery Network (PDN)

The details for the EVM's power delivery network (PDN) are not included in this document.

2.7.7 Identification EEPROM

The EVM board identity and revision information are stored in an onboard EEPROM. The first 259 bytes of the memory are preprogrammed with EVM identification information. The format of that data is provided in the table below. The remaining 32509 bytes are available for data or code storage.

The EEPROM is accessible from WKUP I2C0 port of processor at address 0x51.

Table 2-23. Board ID Memory Header Information

Field Name	Offset /Size	Value	Comments
MAGIC	0000 / 4B (Hex)	0xEE3355AA	Header Identifier
M_TYPE	0004 / 1B (Hex)	0x1	Fixed length and variable position board ID header
M_LENGTH	0005 / 2B (Hex)	0x10B	Size of payload
B_TYPE	0007 / 1B (Hex)	0x10	Payload type
B_LENGTH	0008 / 2B (Hex)	0x2E	Offset to next header
B_NAME	000A / 16B (CHAR)	J742S2X-EVM	Name of the board
DESGIN_REV	001A / 2B (CHAR)	E1	Revision number of the design
PROC_NBR	001C / 4B (CHAR)	184	PROC number
VARIANT	0020 / 2B (CHAR)	2	Design variant number
PCB_REV	0022 / 2B (CHAR)	E1	Revision number of the PCB
SCHBOM_REV	0024 / 2B (CHAR)	0	Revision number of the schematic
SWR_REV	0026 / 2B (CHAR)	1	first software release number
VENDORID	0028 / 2B (CHAR)	1	0x1: Manufactured by Mistral
BUILD_WK	002A / 2B (CHAR)		week of the year of production
BUILD_YR	002C / 2B (CHAR)		year of production
BOARDID	002E / 6B (CHAR)	0	
SERIAL_NBR	0034 / 4B (CHAR)	4	incrementing board number
DDR_TYPE	0038 / 1B (Hex)	0x11	DDR Header Identifier
DDR_LENGTH	0039 / 2B (Hex)	0x2	offset to next header
DDR_CONTROL	003B / 2B (Hex)	0xC560	DDR Control Word Bit 1:0 = '00' First DDR Bit 3:2 = '00' No SPD Bit 5:4 = '10' LPDDR4 Bit 7:6 = '01' 32 bits Bit 9:8 = '01' 32 bits Bit 10 = '1' dual rank Bit 13:11 = '000' Density 64 Gb(bit 0 to 3) Bit 14 = '1' ECC bits present (inline, not separate bits) Bit 15 = '1' Density 64 Gb (bit 4)

Table 2-23. Board ID Memory Header Information (continued)

Field Name	Offset /Size	Value	Comments
DDR_TYPE	003D / 1B (Hex)	0x11	DDR Header Identifier
DDR_LENGTH	003E / 2B (Hex)	0x2	offset to next header
DDR_CONTROL	0040 / 2B (Hex)	0xC561	DDR Control Word)
MAC_TYPE	0042 / 1B (Hex)	0x13	MAC address Header Identifier
MAC_LENGTH	0043 / 2B (Hex)	0xC2	Size of payload
MAC_CONTROL	0045 / 1B (Hex)	0x0	MAC header control word (0 = 1 MAC address)
MAC_ADDRS	0047 / 192B (Hex)		MAC address
END_LIST	0107 / 1B (Hex)	0xFE	End Marker

3 Hardware Design Files

The hardware design files are combined to a single package and available for download at Design Files. The package file can contain multiple EVM board revisions (directories). The naming convention is as follows for PROC*xyz*E*wq*_RP where:

- PROC: Indicates TI's Processor Product.

- *xyz*: Unique ID for this Evaluation Board (example is '170' for this design).

- E: E indicates Pre-Production, blank for Production.

- *wq*: Indicates Revision (w - Major, blank/q - Minor).

- _RP: Release Package Notation.

Example (oldest to latest revision):

PROC184E1A: Pre-Production, version '1A'

PROC184E2: Pre-Production, Version '2'.

PROC184A: Production, Version 'A'.

See schematic history/change log for complete list of changes for each revision.

3.1 Schematics

The schematics are available in both design format (Cadence Allegro, *_SCH.DSN) and searchable PDF (*_SCH.PDF). Both are included as part of the design package and available for download at Design Files.

3.2 PCB Layouts

The PCB design and manufacturing information is available in several different file formats. Below is a list of PCB files included in the design package available for download at Design Files.

Table 3-1. PCB Design and Manufacturing Files

File Type (Extension)	Description
Design file (*_BRD.ZIP)	Allegro PCB design file/zip
Design file (*_ODBGRB.ZIP)	Design file exported to ODB++/Zip
Design file extract (ALG)	For import into other design tools
Fabrication drawing (*_FAB.PDF)	Fabrication info in viewable format
Manufacturing file (_274XGBR.ZIP)	Gerber data, RS-274/ZIP
Manufacturing file (*_STL.ZIP)	Gerber data, STL/Zip
Manufacturing file (*_BRD.IPC)	IPC-D 465 Gerber data supplement
Layers drawing (*_LAYERS.PDF)	Viewable images of each PCB Layer
Stack-up (*_STACKUP.PDF)	PCB Stack-up from PCB manufacturer

3.3 Bill of Materials (BOM)

The Bill Of Materials (BOM) is available in spreadsheet format (Microsoft Excel, *_BOM.XLSX) and is included as part of the design package download at Design Files.

4 Compliance Information

4.1 EMC, EMI, and ESD Compliance

Components installed on the product are sensitive to Electrostatic Discharge (ESD). TI recommends this product be used in an ESD controlled environment. This can include a temperature or humidity controlled environment to limit the buildup of ESD. TI also recommends to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is to be used in the basic electromagnetic environment, as in laboratory conditions, and the applied standard is as per EN IEC 61326-1:2021.

4.2 Reach Compliance

In compliance with the Article 33 provision of the EU REACH regulation, we are notifying you that this EVM includes components containing at least one Substance of Very High Concern (SVHC) above 0.1%. These uses from Texas Instruments do not exceed 1 ton per year. The SVHC's are listed in Table 4-1.

Table 4-1. SVHC Related Components

Component Manufacturer	Component type	Component part number	SVHC Substance	SVHC CAS (when available)
Littelfuse	Power fuse	015406.3DR	Lead	7439-92-1

4.3 Thermal Compliance

There is opportunity for elevated heat on or near the processor or heat sink, use caution particularly at elevated ambient temperatures. Although the processor or heat sink is not a burn hazard, caution must be used when handling the EVM due to increased heat in the area of the heat sink.

CAUTION

Caution

Hot surface. Contact can cause burns. Do not touch.

5 Additional Information

5.1 Known Hardware or Software Issues

There are no known issues with the EVM.

5.2 Trademarks

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NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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