TPS80032 ES1.1 and ES1.2 Register Map

Technical Reference Manual

Literature Number: SWCU096C
November 2011–Revised November 2014

Contents

TPS80032 Register Map

This document describes the register map of the TPS80032 ES1.1and ES1.2. The operation of the IC is described in the Data Sheet and Data Manual.

1 Summary

This section summarizes the registers of the different ID addresses together with a list of the registers including the register bit naming.The addresses are:

- 0x12 (ID0): DVS-I2C Registers
- 0x48 (ID1): CTL-I2C Registers
- 0x49 (ID2): CTL-I2C Registers
- 0x4A (ID3): CTL-I2C Registers

1.1 Definitions

1.1.1 Instance definition

This section described registers instance field.
The instance field shows the reset domain for each register.
The instance field value can be:

- Config domain
- Backup domain
- State domain
- Charger Domain

  Reset domains and reset events are described in Table 1

Table 1. Reset Domains

RESET TRIGGER	RESET DOMAINS				PMIC STATE	NRESPWRON TRANSITION
	BACKUP	CONFIG	STATE	CHARGER		
Power on reset	X	X	X	X	No Supply	Low
32KHz crystal failure detection	X	X	X	X	Wait-On or Backup	Low
VBAT<VBAT MIN_LO	-	X	X	X	Wait-On or Backup	High→Low
NRESWARM	-	X	-	X	Active	High→Low
SW reset	-	X	X	X	Active	High→Low→High
Lonk Key Press	-	X	X	X	Wait-On	High→Low
Primary Watchdog	-	X	X	X	Wait-On	High→Low
Thermal shutdown	-	X	X	X	Wait-On	High→Low

1.1.2 Type definition

This section described registers "type" field.
The type field shows allowed access for each bit.
The type field value can be:

- R: Read only
- W: Write only
- R/W: Read and Write
- R/S/C: Separate registers for read, Set (_SET) and Clear (_CLR)
- W/A: Automatically cleared after a write

1.2 Overview of the registers

1.2.1 ID0 = 12h - @ [55 – 5C]h - PMC Slave SMPS Register Map

Table 2. ID0 = 12h - @ [55 – 5C]h – PMC Slave SMPS Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12	49	73	SMPS5_CFG_FORCE	CMD_1	CMD_0	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0
12	4A	74	SMPS5_CFG_VOLTAGE	WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0
12	55	85	SMPS1_CFG_FORCE	CMD_1	CMD_0	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0
12	56	86	SMPS1_CFG_VOLTAGE	WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0
12	5B	91	SMPS2_CFG_FORCE	CMD_1	CMD_0	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0
12	5C	92	SMPS2_CFG_VOLTAGE	WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

1.2.2 ID1 = 48h - @ [00 – 16]h – RTC Register Map

Table 3. ID1 = 48h - @ [00 – 16]h – RTC Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
48	00	0	SECONDS_REG	RESERVED	SEC1_2	SEC1_1	SEC1_0	SEC0_3	SEC0_2	SEC0_1	SEC0_0
48	01	1	MINUTES_REG	RESERVED	MIN1_2	MIN1_1	MIN1_0	MIN0_3	MIN0_2	MIN0_1	MIN0_0
48	02	2	HOURS_REG	PM_nAM	RESERVED	HOUR1_1	HOUR1_0	HOUR0_3	HOUR0_2	HOUR0_1	HOUR0_0
48	03	3	DAYS_REG	RESERVED	RESERVED	DAY1_1	DAY1_0	DAY0_3	DAY0_2	DAY0_1	DAY0_0
48	04	4	MONTHS_REG	RESERVED	RESERVED	RESERVED	MONTH1_0	MONTH0_3	MONTH0_2	MONTH0_1	MONTH0_0
48	05	5	YEARS_REG	YEAR1_3	YEAR1_2	YEAR1_1	YEAR1_0	YEAR0_3	YEAR0_2	YEAR0_1	YEAR0_0
48	06	6	WEEKS_REG	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	WEEK_2	WEEK_1	WEEK_0
48	08	8	ALARM_SECONDS_REG	RESERVED	ALARM_SEC1_2	ALARM_SEC1_1	ALARM_SEC1_0	ALARM_SEC0_3	ALARM_SEC0_2	ALARM_SEC0_1	ALARM_SEC0_0
48	09	9	ALARM_MINUTES_REG	RESERVED	ALARM_MIN1_2	ALARM_MIN1_1	ALARM_MIN1_0	ALARM_MIN0_3	ALARM_MIN0_2	ALARM_MIN0_1	ALARM_MIN0_0
48	0A	10	ALARM_HOURS_REG	ALARM_PM_nAM	RESERVED	ALARM_HOUR1_1	ALARM_HOUR1_0	ALARM_HOUR0_3	ALARM_HOUR0_2	ALARM_HOUR0_1	ALARM_HOUR0_0
48	0B	11	ALARM_DAYS_REG	RESERVED	RESERVED	ALARM_DAY1_1	ALARM_DAY1_0	ALARM_DAY0_3	ALARM_DAY0_2	ALARM_DAY0_1	ALARM_DAY0_0
48	0C	12	ALARM_MONTHS_REG	RESERVED	RESERVED	RESERVED	ALARM_MONTH1_0	ALARM_MONTH0_3	ALARM_MONTH0_2	ALARM_MONTH0_1	ALARM_MONTH0_0
48	0D	13	ALARM_YEARS_REG	ALARM_YEAR1_3	ALARM_YEAR1_2	ALARM_YEAR1_1	ALARM_YEAR1_0	ALARM_YEAR0_3	ALARM_YEAR0_2	ALARM_YEAR0_1	ALARM_YEAR0_0
48	10	16	RTC_CTRL_REG	RTC_V_OPT	GET_TIME	SET_32_COUNTER	RESERVED	MODE_12_24	AUTO_COMP	ROUND_30S	STOP_RTC
48	11	17	RTC_STATUS_REG	POWER_UP	ALARM	1D_EVENT	1H_EVENT	1M_EVENT	1S_EVENT	RUN	RESERVED
48	12	18	RTC_INTERRUPTS_REG	RESERVED	RESERVED	RESERVED	IT_SLEEP_MASK_EN	IT_ALARM	IT_TIMER	EVERY_1	EVERY_0
48	13	19	RTC_COMP_LSB_REG	RTC_COMP_LSB_7	RTC_COMP_LSB_6	RTC_COMP_LSB_5	RTC_COMP_LSB_4	RTC_COMP_LSB_3	RTC_COMP_LSB_2	RTC_COMP_LSB_1	RTC_COMP_LSB_0
48	14	20	RTC_COMP_MSB_REG	RTC_COMP_MSB_7	RTC_COMP_MSB_6	RTC_COMP_MSB_5	RTC_COMP_MSB_4	RTC_COMP_MSB_3	RTC_COMP_MSB_2	RTC_COMP_MSB_1	RTC_COMP_MSB_0
48	16	22	RTC_RESET_STATUS_REG	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESET_STATUS

1.2.3 ID1 = 48h - @ [17 – 30]h – Memory Register Map

Table 4. ID1 = 48h - @ [17 – 30]h – Memory Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
48	17	23	VALIDITY0	BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0
48	18	24	VALIDITY1	BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0
48	19	25	VALIDITY2	BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0
48	1A	26	VALIDITY3	BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0
48	1B	27	VALIDITY4	BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0
48	1C	28	VALIDITY5	BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0
48	1D	29	VALIDITY6	BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0
48	1E	30	VALIDITY7	BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0
48	35	53	VALIDITY8	BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0
48	36	54	VALIDITY9	BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0
48	37	55	VALIDITY10	BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0
48	38	56	VALIDITY11	BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0

1.2.4 ID1 = 48h - @ [1F - 2D]h - PMC Master Register Map

Table 5. ID1 = 48h - @ [1F - 2D]h - PMC Master Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
48	1F	31	PHOENIX_START_CONDITION	RESERVED	RESTART_BB	FIRST_BAT_INS	STRT_ON_RTC	STRT_ON_PLUG_DET	STRT_ON_USB_ID	STRT_ON_RPWRON	STRT_ON_PWRON
48	20	32	PHOENIX_MSK_TRANSITION	MSK_PREQ3	MSK_PREQ2	MSK_PREQ1	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
48	21	33	STS_HW_CONDITIONS	STS_PREQ3	STS_PREQ2	STS_PREQ1	STS_VSYSMIN_HI	STS_PLUG_DET	STS_USB_ID	STS_RPWRON	STS_PWRON
48	22	34	PHOENIX_LAST_TURNOFF_STS	FALLBACK	DEVOFF_RPWRON	DEVOFF_SHORT	DEVOFF_WDT	DEVOFF_TSHUT	DEVOFF_BCK	DEVOFF_LPK	OSC_RC32K
48	23	35	VSYSMIN_LO_THRESHOLD	RESERVED	RESERVED	VSYS_5	VSYS_4	VSYS_3	VSYS_2	VSYS_1	VSYS_0
48	24	36	VSYSMIN_HI_THRESHOLD	RESERVED	RESERVED	VSYS_5	VSYS_4	VSYS_3	VSYS_2	VSYS_1	VSYS_0
48	25	37	PHOENIX_DEV_ON	RESERVED	SW_RESET	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	DEVOFF
48	26	38	VBATMIN_HI_THRESHOLD	RESERVED	RESERVED	VBAT_5	VBAT_4	VBAT_3	VBAT_2	VBAT_1	VBAT_0
48	27	39	STS_PWR_GRP_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	28	40	PH_CFG_VSYSLOW	BB_SEL	BB_MSK	DELAY_5	DELAY_4	DELAY_3	DELAY_2	DELAY_1	DELAY_0
48	29	41	PH_STS_BOOT	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BOOT2	BOOT1	BOOT0
48	2A	42	PHOENIX_SENS_TRANSITION	SENS_PREQ3	SENS_PREQ2	SENS_PREQ1	RESERVED	RESERVED	RESERVED	RESERVED	PREQ3_VOLT_CFG
48	2B	43	PHOENIX_SEQ_CFG	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	SPARE	SEQ_MSK_VSYS_CMP
48	2C	44	PRIMARY_WATCHDOG_CFG	RESERVED	WDT_6	WDT_5	WDT_4	WDT_3	WDT_2	WDT_1	WDT_0
48	2D	45	KEY_PRESS_DURATION_CFG	KPD_STS	LPK_TIME	RESERVED	KPD_4	KPD_3	KPD_2	KPD_1	KPD_0
48	2E	46	SMPS_LDO_SHORT_STS	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	SHORTLDO7	SHORTLDO5	SHORTSMPSLDO

1.2.5 ID1 = 48h - @ [30 - 34]h - PMC Slave Miscellaneous Register Map

Table 6. ID1 = 48h - @ [30 - 34]h - PMC Slave Miscellaneous Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
48	31	49	BROADCAST_ADDRESS_ALL	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	32	50	BROADCAST_ADDRESS_REF	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	33	51	BROADCAST_ADDRESS_PROV	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	34	52	BROADCAST_ADDRESS_CLK_RST	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

1.2.6 ID1 = 48h - @ [40 - 68]h - PMC Slave SMPS Register Map

Table 7. ID1 = 48h - @ [40 - 68]h - PMC Slave SMPS Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
48	41	65	SMPS4_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	42	66	SMPS4_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	44	68	SMPS4_CFG_VOLTAGE	WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0
48	47	71	SMPS5_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	48	72	SMPS5_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	4B	75	SMPS5_CFG_STEP	NO_STEP	RESERVED	RESERVED	STEP_4	STEP_3	STEP_2	STEP_1	STEP_0

Table 8. ID1 = 48h - @ [40 - 68]h - PMC Slave SMPS Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
48	53	83	SMPS1_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	54	84	SMPS1_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	57	87	SMPS1_CFG_STEP	NO_STEP	RESERVED	RESERVED	STEP_4	STEP_3	STEP_2	STEP_1	STEP_0
48	59	89	SMPS2_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	5A	90	SMPS2_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	5D	93	SMPS2_CFG_STEP	NO_STEP	RESERVED	RESERVED	STEP_4	STEP_3	STEP_2	STEP_1	STEP_0
48	65	101	SMPS3_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	66	102	SMPS3_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	68	104	SMPS3_CFG_VOLTAGE	WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

1.2.7 ID1 = 48h - @ [80 - A7]h - PMC Slave LDO Register Map

Table 9. ID1 = 48h - @ [80 - A7]h - PMC Slave LDO Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
48	81	129	VANA_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	82	130	VANA_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	83	131	VANA_CFG_VOLTAGE	WR_S	RESERVED	RESERVED	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0
48	85	133	LDO2_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	86	134	LDO2_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	87	135	LDO2_CFG_VOLTAGE	WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0
48	89	137	LDO4_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	8A	138	LDO4_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	8B	139	LDO4_CFG_VOLTAGE	WR_S	RESERVED	RESERVED	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0
48	8D	141	LDO3_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	8E	142	LDO3_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	8F	143	LDO3_CFG_VOLTAGE	WR_S	RESERVED	RESERVED	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0
48	91	145	LDO6_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	92	146	LDO6_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	93	147	LDO6_CFG_VOLTAGE	WR_S	RESERVED	RESERVED	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Table 10. ID1 = 48h - @ [80 - A7]h - PMC Slave LDO Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
48	95	149	LDOLN_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	96	150	LDOLN_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	97	151	LDOLN_CFG_VOLTAGE	WR_S	RESERVED	RESERVED	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0
48	99	153	LDO5_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	9A	154	LDO5_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	9B	155	LDO5_CFG_VOLTAGE	WR_S	RESERVED	RESERVED	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0
48	9D	157	LDO1_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	9E	158	LDO1_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	9F	159	LDO1_CFG_VOLTAGE	WR_S	RESERVED	RESERVED	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0
48	A1	161	LDOUSB_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	A2	162	LDOUSB_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	A3	163	LDOUSB_CFG_VOLTAGE	WR_S	RESERVED	RESERVED	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0
48	A5	165	LDO7_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	A6	166	LDO7_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	A7	167	LDO7_CFG_VOLTAGE	WR_S	RESERVED	RESERVED	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

1.2.8 ID1 = 48h - @ [AD - D0]h - PMC Slave Resources Register Map

Table 11. ID1 = 48h - @ [AD - D0]h - PMC Slave Resources Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
48	AE	174	REGEN1_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	AF	175	REGEN1_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	B1	177	REGEN2_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	B2	178	REGEN2_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	B4	180	SYSEN_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	B5	181	SYSEN_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	B7	183	NRESPWRON_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	B8	184	NRESPWRON_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	BA	186	CLK32KAO_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	BB	187	CLK32KAO_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	BD	189	CLK32KG_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	BE	190	CLK32KG_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Table 12. ID1 = 48h - @ [AD - D0]h - PMC Slave Resources Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
48	C0	192	CLK32KAUDIO_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	C1	193	CLK32KAUDIO_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	C3	195	VRTC_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	C4	196	VRTC_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	C6	198	BIAS_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	C7	199	BIAS_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	C9	201	VSYSMIN_HI_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	CA	202	VSYSMIN_HI_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	CC	204	RC6MHZ_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	CD	205	RC6MHZ_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0
48	CF	207	TMP_CFG_TRANS	RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0
48	D0	208	TMP_CFG_STATE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

1.2.9 ID1 = 48h - @ [DA - DF]h – PREQ2/PREQ3 Assignment Register Map

Table 13. ID1 = 48h - @ [DA - DF]h – PREQ2/PREQ3 Assignment Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
48	D7	215	PREQ1_RES_ASS_A	RESERVED	RESERVED	LDOUSB	SMPS5	SMPS4	SMPS3	SMPS2	SMPS1
48	D8	216	PREQ1_RES_ASS_B	LDOLN	LDO7	LDO6	LDO5	LDO4	LDO3	LDO2	LDO1
48	D9	227	PREQ1_RES_ASS_C	RESERVED	RESERVED	VSYSMIN_HI	CLK32KG	CLK32KAUDIO	SYSEN	REGEN2	REGEN1
48	DA	218	PREQ2_RES_ASS_A	RESERVED	RESERVED	LDOUSB	SMPS5	SMPS4	SMPS3	SMPS2	SMPS1
48	DB	219	PREQ2_RES_ASS_B	LDOLN	LDO7	LDO6	LDO5	LDO4	LDO3	LDO2	LDO1
48	DC	220	PREQ2_RES_ASS_C	RESERVED	RESERVED	VSYSMIN_HI	CLK32KG	CLK32KAUDIO	SYSEN	REGEN2	REGEN1
48	DD	221	PREQ3_RES_ASS_A	RESERVED	RESERVED	LDOUSB	SMPS5	SMPS4	SMPS3	SMPS2	SMPS1
48	DE	222	PREQ3_RES_ASS_B	LDOLN	LDO7	LDO6	LDO5	LDO4	LDO3	LDO2	LDO1
48	DF	223	PREQ3_RES_ASS_C	RESERVED	RESERVED	VSYSMIN_HI	CLK32KG	CLK32KAUDIO	SYSEN	REGEN2	REGEN1

1.2.10 ID1 = 48h - @ [E2 - EF]h - PMC Miscellaneous Register Map

Table 14. ID1 = 48h - @ [E2 - EF]h - PMC Miscellaneous Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
48	E0	224	SMPS_OFFSET	OFFSET_R/W	SMPS3	RESERVED	SMPS2	SMPS1	RESERVED	SMPS5	SMPS4
48	E3	227	SMPS_MULT	MULT_R/W	SMPS3	TRACK_LDO	SMPS2	SMPS1	RESERVED	SMPS5	SMPS4
48	E4	228	MISC1	RESERVED	RESERVED	RESERVED	OSC_BYPASS	OSC_HPMODE	VACMEAS	VSYS_MEAS	BB_MEAS
48	E6	230	BBSPOR_CFG	RESERVED	VRTC_EN_SLP_STS	VRTC_EN_OFF_STS	VRTC_PWEN	BB_CHG_EN	BB_SEL_1	BB_SEL_0	RESERVED
48	E7	231	TMP_CFG	RESERVED	RESERVED	RESERVED	THERM_HD	RESERVED	RESERVED	THERM_HD_SEL_1	THERM_HD_SEL_0
48	EB	235	SIMDEBOUNCING	SIM_DEB_BYPASS	SINS_DEB_3	SINS_DEB_2	SINS_DEB_1	SINS_DEB_0	SEXT_DEB_2	SEXT_DEB_1	SEXT_DEB_0
48	EC	236	SIMCTRL	RESERVED	LDO7_DEL	SIM_BATDET_1	SIM_BATDET_0	VSIM_AUTO_OFF	SW_FC	STS_BAT	STS_SIM
48	ED	237	MMCDEBOUNCING	MMC_DEB_BYPASS	MINS_DEB_3	MINS_DEB_2	MINS_DEB_1	MINS_DEB_0	MEXT_DEB_2	MEXT_DEB_1	MEXT_DEB_0
48	EE	238	MMCCTRL	RESERVED	RESERVED	RESERVED	RESERVED	LDO5_AUTO_OFF	SW_FC	RESERVED	STS_MMC
48	EF	239	BATDEBOUNCING	SYS_DEB_BYPASS	BINS_DEB_3	BINS_DEB_2	BINS_DEB_1	BINS_DEB_0	BEXT_DEB_2	BEXT_DEB_1	BEXT_DEB_0

1.2.11 ID1 = 48h - @ [F0 - F6]h - PMC Pull-Up / Pull-Down / High-Z Register Map

Table 15. ID1 = 48h - @ [F0 - F6]h - PMC Pull-Up / Pull-Down / High-Z Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
48	F0	240	CFG_INPUT_PUPD1	SPARE	SPARE	SPARE	SPARE	PREQ2_PU	PREQ2_PD	PREQ1_PU	PREQ1_PD
48	F1	241	CFG_INPUT_PUPD2	RESERVED	CHRG_EXTCHRG_STATZ_PU	SPARE	RESERVED	RESERVED	NRESWARM_PU	PREQ3_PU	PREQ3_PD
48	F2	242	CFG_INPUT_PUPD3	RESERVED	RESERVED	RESERVED	GPADC_START_PD	MMC_PU	MMC_PD	SIM_PU	SIM_PD
48	F3	243	CFG_INPUT_PUPD4	RESERVED	RESERVED	RESERVED	RESERVED	CTLI2C_SDA_PU	CTLI2C_SCL_PU	DVSI2C_SDA_PU	DVSI2C_SCL_PU
48	F4	244	CFG_LDO_PD1	LDO1	LDO5	LDOLN	LDO6	LDO3	LDO4	LDO2	VANA
48	F5	245	CFG_LDO_PD2	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LDO7	LDOUSB
48	F6	246	CFG_SMPS_PD	RESERVED	SMPS3	RESERVED	SMPS2	SMPS1	RESERVED	SMPS5	SMPS4

1.2.12 ID1 = 48h - @ [FA - FA]h - OTG Backup Register Map

Table 16. ID1 = 48h - @ [FA - FA]h - OTG Backup Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
48	FA	250	BACKUP_REG	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	OTG_REV	ID_WK_UP_COMP

1.2.13 ID2 = 49h - @ [00 - 1A]h - USB OTG Register Map

Table 17. ID2 = 49h - @ [00 - 1A]h - USB OTG Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
49	00	0	USB_VENDOR_ID_LSB	VENDOR_ID_7	VENDOR_ID_7	VENDOR_ID_7	VENDOR_ID_7	VENDOR_ID_7	VENDOR_ID_7	VENDOR_ID_7	VENDOR_ID_7
49	01	1	USB_VENDOR_ID_MSB	VENDOR_ID_15	VENDOR_ID_14	VENDOR_ID_13	VENDOR_ID_12	VENDOR_ID_11	VENDOR_ID_10	VENDOR_ID_9	VENDOR_ID_8
49	02	2	USB_PRODUCT_ID_LSB	PRODUCT_ID_7	PRODUCT_ID_7	PRODUCT_ID_7	PRODUCT_ID_7	PRODUCT_ID_7	PRODUCT_ID_7	PRODUCT_ID_7	PRODUCT_ID_7
49	03	3	USB_PRODUCT_ID_MSB	PRODUCT_ID_15	PRODUCT_ID_14	PRODUCT_ID_13	PRODUCT_ID_12	PRODUCT_ID_11	PRODUCT_ID_10	PRODUCT_ID_9	PRODUCT_ID_8
49	04	4	USB_VBUS_CTRL_SET	VBUS_CHRG_VSYS	VBUS_CHRG_PMID	VBUS_DISCHRG	VBUS_IADP_SRC	VBUS_IADP_SINK	VBUS_ACT_COMP	RESERVED	VBUS_MEAS
49	05	5	USB_VBUS_CTRL_CLR	VBUS_CHRG_VSYS	VBUS_CHRG_PMID	VBUS_DISCHRG	VBUS_IADP_SRC	VBUS_IADP_SINK	VBUS_ACT_COMP	RESERVED	VBUS_MEAS
49	06	6	USB_ID_CTRL_SET	ID_PU_220K	ID_PU_100K	ID_GND_DRV	ID_SRC_16U	ID_SRC_5U	ID_ACT_COMP	RESERVED	ID_MEAS
49	07	7	USB_ID_CTRL_CLR	ID_PU_220K	ID_PU_100K	ID_GND_DRV	ID_SRC_16U	ID_SRC_5U	ID_ACT_COMP	RESERVED	ID_MEAS
49	08	8	USB_VBUS_INT_SRC	VOTG_SESS_VLD	VADP_PRB	VAP_SNS	RESERVED	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END
49	09	9	USB_VBUS_INT_LATCH_SET	VOTG_SESS_VLD	VADP_PRB	VAP_SNS	ADP	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END
49	0A	10	USB_VBUS_INT_LATCH_CLR	VOTG_SESS_VLD	VADP_PRB	VAP_SNS	ADP	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END
49	0B	11	USB_VBUS_INT_EN_LO_SET	VOTG_SESS_VLD	VADP_PRB	VAP_SNS	RESERVED	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END
49	0C	12	USB_VBUS_INT_EN_LO_CLR	VOTG_SESS_VLD	VADP_PRB	VAP_SNS	RESERVED	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END
49	0D	13	USB_VBUS_INT_EN_HI_SET	VOTG_SESS_VLD	VADP_PRB	VAP_SNS	ADP	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END
49	0E	14	USB_VBUS_INT_EN_HI_CLR	VOTG_SESS_VLD	VADP_PRB	VAP_SNS	ADP	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END
49	0F	15	USB_ID_INT_SRC	RESERVED	RESERVED	RESERVED	ID_FLOAT	ID_A	ID_B	ID_C	ID_GND
49	10	16	USB_ID_INT_LATCH_SET	RESERVED	RESERVED	RESERVED	ID_FLOAT	ID_A	ID_B	ID_C	ID_GND
49	11	17	USB_ID_INT_LATCH_CLR	RESERVED	RESERVED	RESERVED	ID_FLOAT	ID_A	ID_B	ID_C	ID_GND
49	12	18	USB_ID_INT_EN_LO_SET	RESERVED	RESERVED	RESERVED	ID_FLOAT	ID_A	ID_B	ID_C	ID_GND
49	13	19	USB_ID_INT_EN_LO_CLR	RESERVED	RESERVED	RESERVED	ID_FLOAT	ID_A	ID_B	ID_C	ID_GND
49	14	20	USB_ID_INT_EN_HI_SET	RESERVED	RESERVED	RESERVED	ID_FLOAT	ID_A	ID_B	ID_C	ID_GND
49	15	21	USB_ID_INT_EN_HI_CLR	RESERVED	RESERVED	RESERVED	ID_FLOAT	ID_A	ID_B	ID_C	ID_GND

Table 18. ID2 = 49h - @ [00 - 1A]h - USB OTG Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
49	16	22	USB_OTG_ADP_CTRL	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	ADP_MODE_1	ADP_MODE_0
49	17	23	USB_OTG_ADP_HIGH	T_ADP_HIGH_7	T_ADP_HIGH_6	T_ADP_HIGH_5	T_ADP_HIGH_4	T_ADP_HIGH_3	T_ADP_HIGH_2	T_ADP_HIGH_1	T_ADP_HIGH_0
49	18	24	USB_OTG_ADP_LOW	T_ADP_LOW_7	T_ADP_LOW_6	T_ADP_LOW_5	T_ADP_LOW_4	T_ADP_LOW_3	T_ADP_LOW_2	T_ADP_LOW_1	T_ADP_LOW_0
49	19	25	USB_OTG_ADP_RISE	T_ADP_RISE_7	T_ADP_RISE_6	T_ADP_RISE_5	T_ADP_RISE_4	T_ADP_RISE_3	T_ADP_RISE_2	T_ADP_RISE_1	T_ADP_RISE_0
49	1A	26	USB_OTG_REVISION	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

1.2.14 ID2 = 49h - @ [2E - 36]h - GPADC Control Register Map

Table 19. ID2 = 49h - @ [2E - 36]h - GPADC Control Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
49	2E	46	GPADC_CTRL	GPADC_ISOURCE_EN	TMP2_EN_MONITOR	TMP1_EN_MONITOR	GPADC_SCALER_EN_CH11	VSYS_SCALER_DIV4	GPADC_SCALER_EN_CH2	GPADC_TEMP2_EN	GPADC_TEMP1_EN
49	2F	47	GPADC_CTRL2	RESERVED	RESERVED	RESERVED	RESERVED	VBAT_SCALER_DIV4	GPADC_SCALER_EN_CH18	GPADC_REMSENSE_1	GPADC_REMSENSE_0
49	32	50	RTSELECT_LSB	CH_7	CH_6	CH_5	CH_4	CH_3	CH_2	CH_1	CH_0
49	33	51	RTSELECT_ISB	CH_15	CH_14	CH_13	CH_12	CH_11	CH_10	CH_9	CH_8
49	34	52	RTSELECT_MSB	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CH18	CH_17	CH_16
49	35	53	GPSELECT_ISB	RESERVED	RESERVED	RESERVED	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0
49	36	54	CTRL_P1	RESERVED	RESERVED	RESERVED	RESERVED	SP1	EOCRT	EOCP1	BUSY

1.2.15 ID2 = 49h - @ [37 – 3C]h - GPADCResult Register Map

Table 20. ID2 = 49h - @ [37 – 3C]h - GPADCResult Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
49	37	55	RTCH0_LSB	BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0
49	38	56	RTCH0_MSB	RESERVED	RESERVED	RESERVED	COLLISION_RT	BIT_11	BIT_10	BIT_9	BIT_8
49	39	57	RTCH1_LSB	BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0
49	3A	58	RTCH1_MSB	RESERVED	RESERVED	RESERVED	COLLISION_RT	BIT_11	BIT_10	BIT_9	BIT_8
49	3B	59	GPCH0_LSB	BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0
49	3C	60	GPCH0_MSB	RESERVED	RESERVED	RESERVED	COLLISION_GP	BIT_11	BIT_10	BIT_9	BIT_8

1.2.16 ID2 = 49h - @ [90 - 9C]h - Auxiliaries Register Map

Table 21. ID2 = 49h - @ [90 - 9C]h - Auxiliaries Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
49	90	144	TOGGLE1	FGDITHS	FGDITHR	FGS	FGR	GPADC_START_POLARITY	GPADC_SAMP_WINDOW	GPADCS	GPADCR
49	91	145	TOGGLE2	VIBS	VIBR	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
49	92	146	TOGGLE3	RESERVED	RESERVED	PWM2EN	PWM2S	PWM2R	PWM1EN	PWM1S	PWM1R
49	93	147	PWDNSTATUS1	RESERVED	RESERVED	FGDITH_EN	FG_EN	RESERVED	RESERVED	VIB_EN	GPADC_EN
49	94	148	PWDNSTATUS2	RESERVED	RESERVED	START_POLARITY_STS	SAMP_WINDOW_STS	PWM2_CLK_EN	PWM2_STS	PWM1_CLK_EN	PWM1_STS
49	9B	155	VIBCTRL	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	DSEL_1	DSEL_0
49	9C	156	VIBMODE	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	FREQ_1	FREQ_0

1.2.17 ID2 = 49h - @ [BA - BE]h - PWM Register Map

Table 22. ID2 = 49h - @ [BA - BE]h - PWM Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
49	BA	186	PWM1ON	PWM1_LENGTH	PWM1ON_6	PWM1ON_5	PWM1ON_4	PWM1ON_3	PWM1ON_2	PWM1ON_1	PWM1ON_0
49	BB	187	PWM1OFF	RESERVED	PWM1OFF_6	PWM1OFF_5	PWM1OFF_4	PWM1OFF_3	PWM1OFF_2	PWM1OFF_1	PWM1OFF_0
49	BD	189	PWM2ON	PWM2_LENGTH	PWM2ON_6	PWM2ON_5	PWM2ON_4	PWM2ON_3	PWM2ON_2	PWM2ON_1	PWM2ON_0
49	BE	190	PWM2OFF	RESERVED	PWM2OFF_6	PWM2OFF_5	PWM2OFF_4	PWM2OFF_3	PWM2OFF_2	PWM2OFF_1	PWM2OFF_0

1.2.18 ID2 = 49h - @ [C0 - CB]h - Gas Gauge Register Map

Table 23. ID2 = 49h - @ [C0 - CB]h - Gas Gauge Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
49	C0	192	FG_REG_00	CC_ACTIVE_MODE_1	CC_ACTIVE_MODE_0	RESERVED	RESERVED	RESERVED	CC_AUTOCLEAR	CC_CAL_EN	CC_PAUSE
49	C1	193	FG_REG_01	CC_SAMPLE_CNTR_07	CC_SAMPLE_CNTR_06	CC_SAMPLE_CNTR_05	CC_SAMPLE_CNTR_04	CC_SAMPLE_CNTR_03	CC_SAMPLE_CNTR_02	CC_SAMPLE_CNTR_01	CC_SAMPLE_CNTR_00
49	C2	194	FG_REG_02	CC_SAMPLE_CNTR_15	CC_SAMPLE_CNTR_14	CC_SAMPLE_CNTR_13	CC_SAMPLE_CNTR_12	CC_SAMPLE_CNTR_11	CC_SAMPLE_CNTR_10	CC_SAMPLE_CNTR_09	CC_SAMPLE_CNTR_08
49	C3	195	FG_REG_03	CC_SAMPLE_CNTR_23	CC_SAMPLE_CNTR_22	CC_SAMPLE_CNTR_21	CC_SAMPLE_CNTR_20	CC_SAMPLE_CNTR_19	CC_SAMPLE_CNTR_18	CC_SAMPLE_CNTR_17	CC_SAMPLE_CNTR_16
49	C4	196	FG_REG_04	CC_ACCUM_07	CC_ACCUM_06	CC_ACCUM_05	CC_ACCUM_04	CC_ACCUM_03	CC_ACCUM_02	CC_ACCUM_01	CC_ACCUM_00
49	C5	197	FG_REG_05	CC_ACCUM_15	CC_ACCUM_14	CC_ACCUM_13	CC_ACCUM_12	CC_ACCUM_11	CC_ACCUM_10	CC_ACCUM_09	CC_ACCUM_08
49	C6	198	FG_REG_06	CC_ACCUM_23	CC_ACCUM_22	CC_ACCUM_21	CC_ACCUM_20	CC_ACCUM_19	CC_ACCUM_18	CC_ACCUM_17	CC_ACCUM_16
49	C7	199	FG_REG_07	CC_ACCUM_31	CC_ACCUM_30	CC_ACCUM_29	CC_ACCUM_28	CC_ACCUM_27	CC_ACCUM_26	CC_ACCUM_25	CC_ACCUM_24
49	C8	200	FG_REG_08	CC_OFFSET_07	CC_OFFSET_06	CC_OFFSET_05	CC_OFFSET_04	CC_OFFSET_03	CC_OFFSET_02	CC_OFFSET_01	CC_OFFSET_00
49	C9	201	FG_REG_09	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CC_OFFSET_09	CC_OFFSET_08
49	CA	202	FG_REG_10	CC_INTEG_07	CC_INTEG_06	CC_INTEG_05	CC_INTEG_04	CC_INTEG_03	CC_INTEG_02	CC_INTEG_01	CC_INTEG_00
49	CB	203	FG_REG_11	RESERVED	RESERVED	CC_INTEG_13	CC_INTEG_12	CC_INTEG_11	CC_INTEG_10	CC_INTEG_09	CC_INTEG_08

1.2.19 ID2 = 49h - @[D0 - D8]h - Interfaces Interrupts Register Map

Table 24. ID2 = 49h - @[D0 - D8]h - Interfaces Interrupts Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
49	D0	208	INT_STS_A	INT_STS_7	INT_STS_6	INT_STS_5	INT_STS_4	INT_STS_3	INT_STS_2	INT_STS_1	INT_STS_0
49	D1	209	INT_STS_B	INT_STS_15	INT_STS_14	INT_STS_13	INT_STS_12	INT_STS_11	INT_STS_10	INT_STS_9	INT_STS_8
49	D2	210	INT_STS_C	INT_STS_23	INT_STS_22	INT_STS_21	INT_STS_20	INT_STS_19	INT_STS_18	INT_STS_17	INT_STS_16
49	D3	211	INT_MSK_LINE_A	INT_MSK_LINE_7	INT_MSK_LINE_6	INT_MSK_LINE_5	INT_MSK_LINE_4	INT_MSK_LINE_3	INT_MSK_LINE_2	INT_MSK_LINE_1	INT_MSK_LINE_0
49	D4	212	INT_MSK_LINE_B	INT_MSK_LINE_15	INT_MSK_LINE_14	INT_MSK_LINE_13	INT_MSK_LINE_12	INT_MSK_LINE_11	INT_MSK_LINE_10	INT_MSK_LINE_9	INT_MSK_LINE_8
49	D5	213	INT_MSK_LINE_C	INT_MSK_LINE_23	INT_MSK_LINE_22	INT_MSK_LINE_21	INT_MSK_LINE_20	INT_MSK_LINE_19	INT_MSK_LINE_18	INT_MSK_LINE_17	INT_MSK_LINE_16
49	D6	214	INT_MSK_STS_A	INT_MSK_STS_7	INT_MSK_STS_6	INT_MSK_STS_5	INT_MSK_STS_4	INT_MSK_STS_3	INT_MSK_STS_2	INT_MSK_STS_1	INT_MSK_STS_0

Table 24. ID2 = 49h - @[D0 - D8]h - Interfaces Interrupts Register Map (continued)

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
49	D7	215	INT_MSK_STS_B	INT_MSK_STS_15	INT_MSK_STS_14	INT_MSK_STS_13	INT_MSK_STS_12	INT_MSK_STS_11	INT_MSK_STS_10	INT_MSK_STS_9	INT_MSK_STS_8
49	D8	216	INT_MSK_STS_C	INT_MSK_STS_23	INT_MSK_STS_22	INT_MSK_STS_21	INT_MSK_STS_20	INT_MSK_STS_19	INT_MSK_STS_18	INT_MSK_STS_17	INT_MSK_STS_16

1.2.20 ID2 = 49h - @ [E0 - F5]h - Charger Register Map

Table 25. ID2 = 49h - @ [E0 - F5]h - Charger Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
49	DA	218	CONTROLLER_CTRL2	RESERVED	VSYS_PC2	VSELSUPPCOMP2	VSELSUPPCOMP1	VSYS_PC	LINCH_DLY	EN_DPPM	SUP_MASK
49	DB	219	CONTROLLER_VSEL_COMP	RESERVED	DLIN_2	DLIN_1	VBATFULL_CHRG_3	VBATFULL_CHRG_2	VBATFULL_CHRG_1	VBATSHORT_2	VBATSHORT_1
49	DC	220	CHARGERUSB_VSYSREG	VSYS_SW_CTRL	RESERVED	VSYSREG_5	VSYSREG _4	VSYSREG _3	VSYSREG _2	VSYSREG _1	VSYSREG _0
49	DD	221	CHARGERUSB_VICHRG_PC	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VICHRG_1	VICHRG_0
49	DE	222	LINEAR_CHRG_STS	RESERVED	CRYSTAL_OSC_OK	END_OF_CHARGE	VBATOV	VSYSOV	DPPM_STS	CV_STS	CC_STS
49	E0	224	CONTROLLER_INT_MASK	MVAC_FAULT	MVAC_EOC	LINCH_GATED	MBAT_REMOVED	MFAULT_WDG	MBAT_TEMP	MVAC_DET	MVBUS_DET
49	E1	225	CONTROLLER_CTRL1	RESERVED	RESERVED	EN_LINCH	EN_CHARGER	SEL_CHARGER	RESERVED	RESERVED	RESERVED
49	E2	226	CONTROLLER_WDG	WDG_RST	WDT_6	WDT_5	WDT_4	WDT_3	WDT_2	WDT_1	WDT_0
49	E3	227	CONTROLLER_STAT1	CHRG_EXTCHRG_STATZ	LINCH_GATED	CHRG_DET_N	FAULT_WDG	VAC_DET	VBUS_DET	BAT_REMOVED	BAT_TEMP_OVRANGE
49	E4	228	CHARGERUSB_INT_STATUS	RESERVED	RESERVED	RESERVED	EN_LINCH	CURRENT_TERM	CHARGERUSB_STAT	CHARGERUSB_THMREG	CHARGERUSB_FAULT
49	E5	229	CHARGERUSB_INT_MASK	RESERVED	RESERVED	RESERVED	MEN_LINCH	MCURRENT_TERM	MCHARGERUSB_STAT	MCHARGERUSB_THMREG	MCHARGERUSB_FAULT
49	E6	230	CHARGERUSB_STATUS_INT1	TMREG	NO_BAT	BST_OCP	TH_SHUTD	BAT_OVP	POOR_SRC	SLP_MODE	VBUS_OVP
49	E7	231	CHARGERUSB_STATUS_INT2	RESERVED	RESERVED	RESERVED	RESERVED	ICCLOOP	CURRENT_TERM	CHARGE_DONE	ANTICOLLAPSE
49	E8	232	CHARGERUSB_CTRL1	SUSPEND_BOOT	OPA_MODE	HZ_MODE	TERM	RESERVED	RESERVED	RESERVED	RESERVED
49	E9	233	CHARGERUSB_CTRL2	VITERM_2	VITERM_1	VITERM_0	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
49	EA	234	CHARGERUSB_CTRL3	VBUSCHRG_LDO_OVRD	CHARGE_ONCE	BST_HW_PR_DIS	RESERVED	AUTOSUPPLY	GSMCAL_TM	BUCK_HSILIM_3A	BUCK_HSILIM
49	EC	236	CHARGERUSB_VOREG	RESERVED	RESERVED	VOREG_5	VOREG_4	VOREG_3	VOREG_2	VOREG_1	VOREG_0
49	ED	237	CHARGERUSB_VICHRG	RESERVED	RESERVED	RESERVED	RESERVED	VICHRG_3	VICHRG_2	VICHRG_1	VICHRG_0
49	EE	238	CHARGERUSB_CINLIMIT	RESERVED	RESERVED	CIN_LIMIT_5	CIN_LIMIT_4	CIN_LIMIT_3	CIN_LIMIT_2	CIN_LIMIT_1	CIN_LIMIT_0
49	EF	239	CHARGERUSB_CTRLLIMIT1	RESERVED	RESERVED	VOREGL_5	VOREGL_4	VOREGL_3	VOREGL_2	VOREGL_1	VOREGL_0
49	F0	240	CHARGERUSB_CTRLLIMIT2	RESERVED	RESERVED	RESERVED	LOCK_LIMIT	VICHRGL_3	VICHRGL_2	VICHRGL_1	VICHRGL_0
49	F1	241	ANTICOLLAPSE_CTRL1	BUCK_VTH_2	BUCK_VTH_1	BUCK_VTH_0	RESERVED	RESERVED	ANTICOLL_ANA	RESERVED	RESERVED
49	F4	244	LED_PWM_CTRL1	PWM_VAL_7	PWM_VAL_6	PWM_VAL_5	PWM_VAL_4	PWM_VAL_3	PWM_VAL_2	PWM_VAL_1	PWM_VAL_0
49	F5	245	LED_PWM_CTRL2	RESERVED	DIS_PULLDOWN	CURR_LED_1	CURR_LED_0	LED_IN_1	LED_IN_0	LED_MODE_1	LED_MODE_0

1.2.21 ID3 = 4Ah - @ [87 - 87]h - JTAG Interfaces Register Map

Table 26. ID3 = 4Ah - @ [87 - 87]h - JTAG Interfaces Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4A	87	135	JTAGVERNUM	RESERVED	RESERVED	RESERVED	RESERVED	VERNUM3	VERNUM2	VERNUM1	VERNUM0
4A	DF	223	EPROM_REV	EPROM_REVISION_7	EPROM_REVISION_6	EPROM_REVISION_5	EPROM_REVISION_4	EPROM_REVISION_3	EPROM_REVISION_2	EPROM_REVISION_1	EPROM_REVISION_0

1.2.22 ID3 = 4Ah - @ [DD - DE]h - GPADC Trimming Register Map

Table 27. ID3 = 4Ah - @ [DD - DE]h - GPADC Trimming Register Map

I2C	@Hex	@Dec	Register Name (Link)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
4A	CD	205	GPADC_TRIM1	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	GPADC_TRIM1_2	GPADC_TRIM1_1	GPADC_TRIM1_0
4A	CE	206	GPADC_TRIM2	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	GPADC_TRIM2_2	GPADC_TRIM2_1	GPADC_TRIM2_0
4A	CF	207	GPADC_TRIM3	RESERVED	RESERVED	RESERVED	GPADC_TRIM16_4	GPADC_TRIM16_3	GPADC_TRIM16_2	GPADC_TRIM16_1	GPADC_TRIM16_0
4A	D0	208	GPADC_TRIM4	RESERVED	RESERVED	GPADC_TRIM4_5	GPADC_TRIM4_4	GPADC_TRIM4_3	GPADC_TRIM4_2	GPADC_TRIM4_1	GPADC_TRIM4_0
4A	D1	209	GPADC_TRIM5	RESERVED	GPADC_TRIM5_6	GPADC_TRIM5_5	GPADC_TRIM5_4	GPADC_TRIM5_3	GPADC_TRIM5_2	GPADC_TRIM5_1	GPADC_TRIM5_0
4A	D2	210	GPADC_TRIM6	GPADC_TRIM6_7	GPADC_TRIM6_6	GPADC_TRIM6_5	GPADC_TRIM6_4	GPADC_TRIM6_3	GPADC_TRIM6_2	GPADC_TRIM6_1	GPADC_TRIM6_0
4A	D3	211	GPADC_TRIM7	RESERVED	RESERVED	RESERVED	GPADC_TRIM16_4	GPADC_TRIM16_3	GPADC_TRIM16_2	GPADC_TRIM16_1	GPADC_TRIM16_0
4A	D4	212	GPADC_TRIM8	RESERVED	RESERVED	RESERVED	GPADC_TRIM16_4	GPADC_TRIM16_3	GPADC_TRIM16_2	GPADC_TRIM16_1	GPADC_TRIM16_0
4A	D5	213	GPADC_TRIM9	RESERVED	RESERVED	RESERVED	RESERVED	GPADC_TRIM15_3	GPADC_TRIM15_2	GPADC_TRIM15_1	GPADC_TRIM15_0
4A	D6	214	GPADC_TRIM7	RESERVED	RESERVED	RESERVED	GPADC_TRIM16_4	GPADC_TRIM16_3	GPADC_TRIM16_2	GPADC_TRIM16_1	GPADC_TRIM16_0
4A	D7	215	GPADC_TRIM11	RESERVED	RESERVED	RESERVED	RESERVED	GPADC_TRIM15_3	GPADC_TRIM15_2	GPADC_TRIM15_1	GPADC_TRIM15_0
4A	D8	216	GPADC_TRIM12	RESERVED	RESERVED	RESERVED	GPADC_TRIM12_4	GPADC_TRIM12_3	GPADC_TRIM12_2	GPADC_TRIM12_1	GPADC_TRIM12_0
4A	D8	217	GPADC_TRIM13	RESERVED	RESERVED	RESERVED	RESERVED	GPADC_TRIM15_3	GPADC_TRIM15_2	GPADC_TRIM15_1	GPADC_TRIM15_0
4A	DA	218	GPADC_TRIM14	RESERVED	RESERVED	RESERVED	GPADC_TRIM16_4	GPADC_TRIM16_3	GPADC_TRIM16_2	GPADC_TRIM16_1	GPADC_TRIM16_0
4A	DB	219	GPADC_TRIM15	RESERVED	RESERVED	RESERVED	RESERVED	GPADC_TRIM15_3	GPADC_TRIM15_2	GPADC_TRIM15_1	GPADC_TRIM15_0
4A	DC	220	GPADC_TRIM16	RESERVED	RESERVED	RESERVED	GPADC_TRIM16_4	GPADC_TRIM16_3	GPADC_TRIM16_2	GPADC_TRIM16_1	GPADC_TRIM16_0
4A	DD	221	GPADC_TRIM17	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RATIO_TLO_2	RATIO_TLO_1	RATIO_TLO_0
4A	DE	222	GPADC_TRIM18	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RATIO_THI_2	RATIO_THI_1	RATIO_THI_0
4A	FD	253	GPADC_TRIM19	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	GPADC_TRIM19_0
4A	FE	254	GPADC_TRIM20	GPADC_TRIM20_7	GPADC_TRIM20_6	GPADC_TRIM20_5	GPADC_TRIM20_4	GPADC_TRIM20_3	GPADC_TRIM20_2	GPADC_TRIM20_1	GPADC_TRIM20_0
4A	FF	255	GPADC_TRIM21	GPADC_TRIM21_7	GPADC_TRIM21_6	GPADC_TRIM21_5	GPADC_TRIM21_4	GPADC_TRIM21_3	GPADC_TRIM21_2	GPADC_TRIM21_1	GPADC_TRIM21_0

2 Register Maps

2.1 Pullups/Pulldowns

2.1.1 CFG_INPUT_PUPD1 Register

Table 28. CFG_INPUT_PUPD1

Address	Dec 240, Hex F0		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
HOLD_WDG_INSLEEP	SPARE	SPARE	SPARE	PREQ2 _PU	PREQ2 _PD	PREQ1 _PU	PREQ1 _PD

Bits	Field Name	Description	Type	Reset
7	HOLD_WDG_INSLEEP	0: When low, primary watchdog is running in sleep mode. 1: When high, primary watchdog is hold in sleep mode.	R/W	0
6	SPARE	SPARE	R/W	1
5	SPARE	SPARE	R/W	0
4	SPARE	SPARE	R/W	1
3	PREQ2 _PU	0: Pullup is disabled. 1: Pullup is enabled.	R/W	0
2	PREQ2 _PD	0: Pulldown is disabled. 1: Pulldown is enabled.	R/W	1
1	PREQ1 _PU	0: Pullup is disabled. 1: Pullup is enabled.	R/W	0
0	PREQ1 _PD	0: Pulldown is disabled. 1: Pulldown is enabled.	R/W	1

2.1.2 CFG_INPUT_PUPD2 Register

Table 29. CFG_INPUT_PUPD2

Address	Dec 241, Hex F1		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	CHRG _EXT CHRG_ STATZ_PU	SPARE	RESERVED	RESERVED	NRES WARM _PU	PREQ3 _PU	PREQ3 _PD

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	CHRG _EXT CHRG_ STATZ_PU	0: Pullup is disabled. 1: Pullup is enabled.	R	1
5	SPARE	SPARE	R/W	1
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	NRES WARM _PU	0: Pullup is disabled. 1: Pullup is enabled.	R	1
1	PREQ3 _PU	0: Pullup is disabled. 1: Pullup is enabled.	R/W	0
0	PREQ3 _PD	0: Pulldown is disabled. 1: Pulldown is enabled.	R/W	1

2.1.3 CFG_INPUT_PUPD3 Register

Table 30. CFG_INPUT_PUPD3

Address	Dec 242, Hex F2		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	GPADC _START _PD	MMC_PU	MMC_PD	SIM_PU	SIM_PD

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	GPADC _START _PD	0: Pulldown is disabled. 1: Pulldown is enabled.	R/W	1
3	MMC_PU	0: Pullup is disabled. 1: Pullup is enabled.	R/W	0
2	MMC_PD	0: Pulldown is disabled. 1: Pulldown is enabled.	R/W	1
1	SIM_PU	0: Pullup is disabled. 1: Pullup is enabled.	R/W	0
0	SIM_PD	0: Pulldown is disabled. 1: Pulldown is enabled.	R/W	1

2.1.4 CFG_INPUT_PUPD4 Register

Table 31. CFG_INPUT_PUPD4

Address	Dec 243, Hex F3		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	CTLI2C _SDA _PU	CTLI2C _SCL _PU	DVSI2C _SDA _PU	DVSI2C _SCL _PU

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	CTLI2C _SDA _PU	0: Pullup is disabled. 1: Pullup is enabled.	R/W	0
2	CTLI2C _SCL _PU	0: Pullup is disabled. 1: Pullup is enabled.	R/W	0
1	DVSI2C _SDA _PU	0: Pullup is disabled. 1: Pullup is enabled.	R/W	0
0	DVSI2C _SCL _PU	0: Pullup is disabled. 1: Pullup is enabled.	R/W	0

2.1.5 CFG_LDO_PD1 Register

Table 32. CFG_LDO_PD1

Address	Dec 244, Hex F4		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
LDO1	LDO5	LDOLN	LDO6	LDO3	LDO4	LDO2	VANA

Bits	Field Name	Description	Type	Reset
7	LDO1	0: Pulldown is disabled. 1: Pulldown is enabled when LDO1 is in the OFF state.	R/W	1
6	LDO5	0: Pulldown is disabled. 1: Pulldown is enabled when LDO5 is in the OFF state.	R/W	1
5	LDOLN	0: Pulldown is disabled. 1: Pulldown is enabled when LDOLN is in the OFF state.	R/W	1
4	LDO6	0: Pulldown is disabled. 1: Pulldown is enabled when LDO6 is in the OFF state.	R/W	1
3	LDO3	0: Pulldown is disabled. 1: Pulldown is enabled when LDO3 is in the OFF state.	R/W	1
2	LDO4	0: Pulldown is disabled. 1: Pulldown is enabled when LDO4 is in the OFF state.	R/W	1
1	LDO2	0: Pulldown is disabled. 1: Pulldown is enabled when LDO2 is in the OFF state.	R/W	1
0	VANA	0: Pulldown is disabled. 1: Pulldown is enabled when VANA is in the OFF state.	R/W	1

2.1.6 CFG_LDO_PD2 Register

Table 33. CFG_LDO_PD2

Address	Dec 245, Hex F5		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LDO7	LDOUSB

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	LDO7	0: Pulldown is disabled. 1: Pulldown is enabled when LDO7 is in the OFF state.	R/W	1
0	LDOUSB	0: Pulldown is disabled. 1: Pulldown is enabled when LDOUSB is in the OFF state.	R/W	1

2.1.7 CFG_SMPS_PD Register

Table 34. CFG_SMPS_PD

Address	Dec 246, Hex F6		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	SMPS3	RESERVED	SMPS2	SMPS1	RESERVED	SMPS5	SMPS4

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	SMPS3	0: Pulldown is disabled. 1: Pulldown is enabled when SMPS3 is in the OFF state.	R/W	1
5	RESERVED	Reserved	R/W	1
4	SMPS2	0: Pulldown is disabled. 1: Pulldown is enabled when SMPS2 is in the OFF state.	R/W	1
3	SMPS1	0: Pulldown is disabled. 1: Pulldown is enabled when SMPS1 is in the OFF state.	R/W	1
2	RESERVED	Reserved	R/W	1
1	SMPS5	0: Pulldown is disabled. 1: Pulldown is enabled when SMPS5 is in the OFF state.	R/W	1
0	SMPS4	0: Pulldown is disabled. 1: Pulldown is enabled when SMPS4 is in the OFF state.	R/W	1

Notes:

- LDOs and SMPS pull-down enable register bits validate the control of the active discharge of each power resource to fulfill the turn-off timing requirements.
- When a pulldown is not activated, there is always a weak pulldown present at the output of the power resource, so that the device restarts correctly at the next power-up sequence.

2.2 Real-Time Clock

2.2.1 SECONDS_REG Register

Table 35. SECONDS_REG

Address	Dec 0, Hex 00		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description	Security: MSECURE		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	SEC1_2	SEC1_1	SEC1_0	SEC0_3	SEC0_2	SEC0_1	SEC0_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	SEC1_2	Second digit of seconds (range is 0 to 5)	R/W	0
5	SEC1_1		R/W	0
4	SEC1_0		R/W	0
3	SEC0_3	First digit of seconds (range is 0 to 9)	R/W	0
2	SEC0_2		R/W	0
1	SEC0_1		R/W	0
0	SEC0_0		R/W	0

2.2.2 MINUTES_REG Register

Table 36. MINUTES_REG

Address	Dec 1, Hex 01		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description	Security: MSECURE		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	MIN1_2	MIN1_1	MIN1_0	MIN0_3	MIN0_2	MIN0_1	MIN0_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	MIN1_2	Second digit of minutes (range is 0 to 5)	R/W	0
5	MIN1_1		R/W	0
4	MIN1_0		R/W	0
3	MIN0_3	First digit of minutes (range is 0 to 9)	R/W	0
2	MIN0_2		R/W	0
1	MIN0_1		R/W	0
0	MIN0_0		R/W	0

2.2.3 HOURS_REG Register

Table 37. HOURS_REG

Address	Dec 2, Hex 02		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description	Security: MSECURE		
Type	R/W		

7	6	5	4	3	2	1	0
PM_nAM	RESERVED	HOUR1_1	HOUR1_0	HOUR0_3	HOUR0_2	HOUR0_1	HOUR0_0

Bits	Field Name	Description	Type	Reset
7	PM_nAM	Only used in PM_AM mode (otherwise it is set to 0) 0: AM 1: PM	R/W	0
6	RESERVED	Reserved	R	0
5	HOUR1_1	Second digit of hours (range is 0 to 2)	R/W	0
4	HOUR1_0		R/W	0
3	HOUR0_3	First digit of hours (range is 0 to 9)	R/W	0
2	HOUR0_2		R/W	0
1	HOUR0_1		R/W	0
0	HOUR0_0		R/W	0

2.2.4 DAYS_REG Register

Table 38. DAYS_REG

Address	Dec 3, Hex 03		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description	Security: MSECURE		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	DAY1_1	DAY1_0	DAY0_3	DAY0_2	DAY0_1	DAY0_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	DAY1_1	Second digit of days (range is 0 to 3)	R/W	0
4	DAY1_0		R/W	0
3	DAY0_3	First digit of days (range is 0 to 9)	R/W	0
2	DAY0_2		R/W	0
1	DAY0_1		R/W	0
0	DAY0_0		R/W	1

2.2.5 MONTHS_REG Register

Table 39. MONTHS_REG

Address	Dec 4, Hex 04		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description	Security: MSECURE		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	MONTH1_0	MONTH0_3	MONTH0_2	MONTH0_1	MONTH0_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	MONTH1_0	Second digit of months (range is 0 to 1)	R/W	0
3	MONTH0_3	First digit of months (range is 0 to 9)	R/W	0
2	MONTH0_2		R/W	0
1	MONTH0_1		R/W	0
0	MONTH0_0		R/W	1

Notes:
The notification for month value is:

- 01: January (default value)
- 02: February
- …
- 12: December

2.2.6 YEARS_REG Register

Table 40. YEARS_REG

Address	Dec 5, Hex 05		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description	Security: MSECURE		
Type	R/W		

7	6	5	4	3	2	1	0
YEAR1_3	YEAR1_2	YEAR1_1	YEAR1_0	YEAR0_3	YEAR0_2	YEAR0_1	YEAR0_0

Bits	Field Name	Description	Type	Reset
7	YEAR1_3	Second digit of years (range is 0 to 9)	R/W	0
6	YEAR1_2		R/W	0
5	YEAR1_1		R/W	0
4	YEAR1_0		R/W	0
3	YEAR0_3	First digit of years (range is 0 to 9)	R/W	0
2	YEAR0_2		R/W	0
1	YEAR0_1		R/W	0
0	YEAR0_0		R/W	0

2.2.7 WEEKS_REG Register

Table 41. WEEKS_REG

Address	Dec 6, Hex 06		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description	Security: MSECURE		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	WEEK_2	WEEK_1	WEEK_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	WEEK_2	First digit of days in a week (range is 0 to 6)	R/W	0
1	WEEK_1		R/W	0
0	WEEK_0		R/W	0

Notes:

- Out of range value (that is, 0x7) is not supported and should not be used.
- The notification for week value is:
  - 00: Sunday (default value)
  - 01: Monday
  - …
  - 06: Saturday

2.2.8 ALARM_SECONDS_REG Register

Table 42. ALARM_SECONDS_REG

Address	Dec 8, Hex 08		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
Reserved	ALARM_SEC1_2	ALARM_SEC1_1	ALARM_SEC1_0	ALARM_SEC0_3	ALARM_SEC0_2	ALARM_SEC0_1	ALARM_SEC0_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	ALARM_SEC1_2	Second digit of seconds (range is 0 to 5)	R/W	0
5	ALARM_SEC1_1		R/W	0
4	ALARM_SEC1_0		R/W	0
3	ALARM_SEC0_3	First digit of seconds (range is 0 to 9)	R/W	0
2	ALARM_SEC0_2		R/W	0
1	ALARM_SEC0_1		R/W	0
0	ALARM_SEC0_0		R/W	0

2.2.9 ALARM_MINUTES_REG Register

Table 43. ALARM_MINUTES_REG

Address	Dec 9, Hex 09		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	ALARM_MIN1_2	ALARM_MIN1_1	ALARM_MIN1_0	ALARM_MIN0_3	ALARM_MIN0_2	ALARM_MIN0_1	ALARM_MIN0_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	ALARM_MIN1_2	Second digit of minutes (range is 0 to 5)	R/W	0
5	ALARM_MIN1_1		R/W	0
4	ALARM_MIN1_0		R/W	0
3	ALARM_MIN0_3	First digit of minutes (range is 0 to 9)	R/W	0
2	ALARM_MIN0_2		R/W	0
1	ALARM_MIN0_1		R/W	0
0	ALARM_MIN0_0		R/W	0

2.2.10 ALARM_HOURS_REG Register

Table 44. ALARM_HOURS_REG

Address	Dec 10, Hex 0A		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
ALARM_PM_nAM	RESERVED	ALARM_HOUR1_1	ALARM_HOUR1_0	ALARM_HOUR0_3	ALARM_HOUR0_2	ALARM_HOUR0_1	ALARM_HOUR0_0

Bits	Field Name	Description	Type	Reset
7	ALARM_PM_nAM	0: AM Only used in PM_AM mode (otherwise it is set to 0) 1: PM	R/W	0
6	RESERVED	Reserved	R	0
5	ALARM_HOUR1_1	Second digit of hours (range is 0 to 2)	R/W	0
4	ALARM_HOUR1_0		R/W	0
3	ALARM_HOUR0_3	First digit of hours (range is 0 to 9)	R/W	0
2	ALARM_HOUR0_2		R/W	0
1	ALARM_HOUR0_1		R/W	0
0	ALARM_HOUR0_0		R/W	0

2.2.11 ALARM_DAYS_REG Register

Table 45. ALARM_DAYS_REG

Address	Dec 11, Hex 0B		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	Reserved	ALARM_DAY1_1	ALARM_DAY1_0	ALARM_DAY0_3	ALARM_DAY0_2	ALARM_DAY0_1	ALARM_DAY0_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	ALARM_DAY1_1	Second digit of days (range is 0 to 3)	R/W	0
4	ALARM_DAY1_0		R/W	0
3	ALARM_DAY0_3	First digit of days (range is 0 to 9)	R/W	0
2	ALARM_DAY0_2		R/W	0
1	ALARM_DAY0_1		R/W	0
0	ALARM_DAY0_0		R/W	1

2.2.12 ALARM_MONTHS_REG Register

Table 46. ALARM_MONTHS_REG

Address	Dec 12, Hex 0C		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	ALARM_MONTH1_0	ALARM_MONTH0_3	ALARM_MONTH0_2	ALARM_MONTH0_1	ALARM_MONTH0_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	ALARM_MONTH1_0	Second digit of months (range is 0 to 1)	R/W	0
3	ALARM_MONTH0_3	First digit of months (range is 0 to 9)	R/W	0
2	ALARM_MONTH0_2		R/W	0
1	ALARM_MONTH0_1		R/W	0
0	ALARM_MONTH0_0		R/W	1

2.2.13 ALARM_YEARS_REG Register

Table 47. ALARM_YEARS_REG

Address	Dec 13, Hex 0D		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
ALARM_YEAR1_3	ALARM_YEAR1_2	ALARM_YEAR1_1	ALARM_YEAR1_0	ALARM_YEAR0_3	ALARM_YEAR0_2	ALARM_YEAR0_1	ALARM_YEAR0_0

Bits	Field Name	Description	Type	Reset
7	ALARM_YEAR1_3	Second digit of years (range is 0 to 9)	R/W	0
6	ALARM_YEAR1_2		R/W	0
5	ALARM_YEAR1_1		R/W	0
4	ALARM_YEAR1_0		R/W	0
3	ALARM_YEAR0_3	First digit of years (range is 0 to 9)	R/W	0
2	ALARM_YEAR0_2		R/W	0
1	ALARM_YEAR0_1		R/W	0
0	ALARM_YEAR0_0		R/W	0

2.2.14 RTC_CTRL_REG Register

Table 48. RTC_CTRL_REG

Address	Dec 16, Hex 10		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description	Security: MSECURE(except GET_TIME bit)		
Type	R/W		

7	6	5	4	3	2	1	0
RTC_V_OPT	GET_TIME	SET_32_COUNTER	RESERVED	MODE_12_24	AUTO_COMP	ROUND_30S	STOP_RTC

Bits	Field Name	Description	Type	Reset
7	RTC_V_OPT	RTC date / time register selection: 0: Read access directly to dynamic registers (SECONDS_REG, MINUTES_REG, HOURS_REG, DAYS_REG, MONTHS_REG, YEARS_REG, WEEKS_REG) 1: Read access to static shadowed registers (see GET_TIME bit).	R/W	0
6	GET_TIME	When writing 1 into this register, the content of the dynamic registers (SECONDS_REG, MINUTES_REG, HOURS_REG, DAYS_REG, MONTHS_REG, YEARS_REG, WEEKS_REG) is transferred into some static shadowed registers. Each update of these registers needs to be done by reasserting GET_TIME bit to 1 (that is,: reset it to 0 and then rewrite it to 1)	R/W	0
5	SET_32_COUNTER	0: No action 1: Set the 32-kHz counter with RTC_COMP_MSB_REG/ RTC_COMP_LSB_REG value (see notes).	R/W	0
4	RESERVED	Reserved	R/W	0
3	MODE_12_24	0: 24 hours mode (see notes) 1: 12 hours mode (PM-AM mode)	R/W	0
2	AUTO_COMP	0: No auto-compensation 1: Auto compensation enabled	R/W	0
1	ROUND_30S	0: No update (see notes) 1: When 1 is written, the time is rounded to the closest minute	R/W	0
0	STOP_RTC	0: RTC is frozen 1: RTC is running	R/W	0

Notes:

- The SET_32_COUNTER bit must only be used when the RTC is frozen(STOP_RTC set to "0").
- The ROUND_30S bit is a toggle bit, the microcontroller can only write 1 and the RTC clears it. If the microcontroller sets the ROUND_30S bit and then reads it, the microcontroller will read 1 until the round to the closet minute is performed at the next second.
- MODE_12_24: It is possible to switch between the two modes at any time without disturbing the RTC, read or write are always performed with the current mode.
- Shadowed registers, linked to the GET_TIME feature, are a parallel set of calendar static registers, at the same I2C addresses as the calendar dynamic registers
- The GET_TIME feature loads the RTC counter in the shadow registers and make the content of the shadow registers available and stable for reading.
- The GET_TIME bit has to be set to 0 and again to 1 to get a new timing value.
- If the time reading is done without GET_TIME, the read value comes directly from the RTC counter

and software has to manage the counter change during the reading.

- Time reading remains always at the same address, with or without using the GET_TIME feature.

2.2.15 RTC_STATUS_REG Register

Table 49. RTC_STATUS_REG

Address	Dec 17, Hex 11		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description			
Type			

7	6	5	4	3	2	1	0
POWER_UP	ALARM	1D_EVENT	1H_EVENT	1M_EVENT	1S_EVENT	RUN	RESERVED

Bits	Field Name	Description	Type	Reset
7	POWER_UP	Indicates that a reset occurred (bit cleared to 0 by writing 1) and that RTC data are not valid anymore.	R/W	1
6	ALARM	Indicates that an alarm interrupt has been generated (bit cleared by writing 1).	R/W	0
5	1D_EVENT	One day has occurred.	R	0
4	1H_EVENT	One hour has occurred.	R	0
3	1M_EVENT	One minute has occurred.	R	0
2	1S_EVENT	One second has occurred.	R	0
1	RUN	0: RTC is frozen 1: RTC is running	R	0
0	RESERVED	Reserved	R	0

Notes:

- A dummy read of this RTC_STATUS_REG register is necessary before each I2C read in order to update the status register value.
- The alarm interrupt keeps its low level, until the microcontroller writes 1 in the ALARM bit of the RTC_STATUS_REG register.
- The timer interrupt is a low-level pulse (15-µs duration).
- The RUN bit shows the real state of the RTC, indeed because of STOP_RTC (RTC_CTRL_REG) signal was resynchronized on 32-kHz clock, the action of this bit is delayed.
- POWER_UP is set by a reset, this bit is cleared by writing 1.
- The RESET_STATUS (RTC_RESET_STATUS_REG) and POWER_UP (RTC_STATUS_REG) register bits provide the same status.

2.2.16 RTC_INTERRUPTS_REG Register

Table 50. RTC_INTERRUPTS_REG

Address	Dec 18, Hex 12		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	IT_SLEEP_MASK_EN	IT_ALARM	IT_TIMER	EVERY_1	EVERY_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	IT_SLEEP_MASK_EN	1: Mask periodic interrupt while the Phoenix device is in SLEEP mode. Interrupt event is back up in a register and occurred as soon as the Phoenix device is no more in SLEEP mode. 0: Normal mode, no interrupt masked	R/W	0
3	IT_ALARM	Enable one interrupt when the alarm value is reached (TC alarm registers: ALARM_SECONDS_REG, ALARM_MINUTES_REG, ALARM_HOURS_REG, ALARM_DAYS_REG, ALARM_MONTHS_REG, ALARM_YEARS_REG) by the TC registers 0: Interrupt disabled 1: Interrupt enabled	R/W	0
2	IT_TIMER	Enable periodic interrupt 0: Interrupt disabled 1: Interrupt enabled	R/W	0
1	EVERY_1	Interrupt period 00: Every second 01: Every minute 10: Every hour 11: Every day	R/W	0
0	EVERY_0		R/W	0

2.2.17 RTC_COMP_LSB_REG Register

Table 51. RTC_COMP_LSB_REG

Address	Dec 19, Hex 13		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description	This register contains the number of 32-kHz periods to be added into the 32-kHz counter every hour [LSB]		
Type	R/W		

7	6	5	4	3	2	1	0
RTC_COMP_LSB_7	RTC_COMP_LSB_6	RTC_COMP_LSB_5	RTC_COMP_LSB_4	RTC_COMP_LSB_3	RTC_COMP_LSB_2	RTC_COMP_LSB_1	RTC_COMP_LSB_0

Bits	Field Name	Description	Type	Config Domain
7	RTC_COMP_LSB_7	This register contains the number of 32-kHz periods to be added into the 32-kHz counter every hour [LSB]	R/W	0
6	RTC_COMP_LSB_6		R/W	0
5	RTC_COMP_LSB_5		R/W	0
4	RTC_COMP_LSB_4		R/W	0
3	RTC_COMP_LSB_3		R/W	0
2	RTC_COMP_LSB_2		R/W	0
1	RTC_COMP_LSB_1		R/W	0
0	RTC_COMP_LSB_0		R/W	0

2.2.18 RTC_COMP_MSB_REG Register

Table 52. RTC_COMP_MSB_REG

Address	Dec 20, Hex 14		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description	This register contains the number of 32-kHz periods to be added into the 32-kHz counter every hour [MSB]		
Type	R/W		

7	6	5	4	3	2	1	0
RTC_COMP_MSB_7	RTC_COMP_MSB_6	RTC_COMP_MSB_5	RTC_COMP_MSB_4	RTC_COMP_MSB_3	RTC_COMP_MSB_2	RTC_COMP_MSB_1	RTC_COMP_MSB_0

Bits	Field Name	Description	Type	Reset
7	RTC_COMP_MSB_7	This register contains the number of 32-kHz periods to be added into the 32-kHz counter every hour [MSB]	R/W	0
6	RTC_COMP_MSB_6		R/W	0
5	RTC_COMP_MSB_5		R/W	0
4	RTC_COMP_MSB_4		R/W	0
3	RTC_COMP_MSB_3		R/W	0
2	RTC_COMP_MSB_2		R/W	0
1	RTC_COMP_MSB_1		R/W	0
0	RTC_COMP_MSB_0		R/W	0

Notes:

- This register must be written in 2's-complement.
- This means that to add one 32-kHz oscillator period every hour, the microcontroller needs to write FFFF into RTC_COMP_MSB_REG and RTC_COMP_LSB_REG.
- To remove one 32-kHz oscillator period every hour, the microcontroller needs to write 0001 into RTC_COMP_MSB_REG and RTC_COMP_LSB_REG.
- The value 7FFF is forbidden.

2.2.19 RTC_RESET_STATUS_REG Register

Table 53. RTC_RESET_STATUS_REG

Address	Dec 22, Hex 16		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESET_STATUS

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	RESERVED	Reserved	R	0
0	RESET_STATUS	This bit can only be set to one and is cleared when a manual reset or a POR occurs. If this bit is reset it means that the RTC has lost its configuration.	R/W	0

Note:

- The RESET_STATUS (RTC_RESET_STATUS_REG) and POWER_UP (RTC_STATUS_REG) register bits indicate the same information.

2.3 PMC Master Module

2.3.1 PHOENIX_START_CONDITION Register

Table 54. PHOENIX_START_CONDITION

Address	Dec 31, Hex 1F		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESTART_BB	FIRST_SYS_INS	STRT_ON_RTC	STRT_ON_PLUG_DET	STRT_ON_USB_ID	STRT_ON_RPWRON	STRT_ON_PWRON

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESTART_BB	This bit is set to 1 to indicate that the turn on event is a system supply bounce or battery re-insertion (with coin cell) according to PH_CFG_VSYSLOW BB_SEL configuration register bit transition from BACKUP to WAIT_ON and then to ACTIVE If BB_SEL = 0, switch on from BACKUP to ACTIVE on battery insertion. If BB_SEL = 1, restart on system supply (battery) bounce.	R/W	0
5	FIRST_SYS_INS	This bit is set to 1 to indicate that the turn on event is a battery insertion (or system supply rise) (transition from NO_SUPPLY to WAIT_ON and then to ACTIVE) Transition from BACKUP to WAITON on battery insertion is flagged by RESTART_BB (If BB_SEL bit of PH_CFG_VSYSLOW Register is 0)	R/W	0
4	STRT_ON_RTC	Indicates that the turn on condition is due to a RTC event or this event occurred before the NRESPWRON release.	R/W	0
3	STRT_ON_PLUG_DET	Indicates that the turn on condition is due to a PLUG_DET (AC or USB charger) event or this event occurred before the NRESPWRON release.	R/W	0
2	STRT_ON_USB_ID	Indicates that the turn on condition is due to a USB_ID event or this event occurred before the NRESPWRON release.	R/W	0
1	STRT_ON_RPWRON	Indicates that the turn on condition is due to a RPWRON event or this event occurred before the NRESPWRON release.	R/W	0
0	STRT_ON_PWRON	Indicates that the turn on condition is due to a PWRON event or this event occurred before the NRESPWRON release.	R/W	0

Notes:

- Cleared on a write access.

2.3.2 PHOENIX_MSK_TRANSITION Register

Table 55. PHOENIX_MSK_TRANSITION

Address	Dec 32, Hex 20		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
MSK_PREQ3	MSK_PREQ2	MSK_PREQ1	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7	MSK_PREQ3	0: PREQ3 control resources set in register PREQ3_ASS_EN* (only when device is in active mode). 1: PREQ3 does not affect resources state.	R/W	1
6	MSK_PREQ2	0: PREQ2 control resources set in register PREQ2_ASS_EN* (only when device is in active mode). 1: PREQ2 does not affect resources state.	R/W	1
5	MSK_PREQ1	0: PREQ1 does affect P1_ACT2SLP or P1_SLP2ACT transition. 1: PREQ1 does not affect P1_ACT2SLP or P1_SLP2ACT transition.	R/W	1
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	RESERVED	Reserved	R	0
0	RESERVED	Reserved	R	0

Notes:

- As soon as NRESPWRON goes low, the MSK_PREQ# register bits are automatically reconfigured to 1.

2.3.3 STS_HW_CONDITIONS Register

Table 56. STS_HW_CONDITIONS

Address	Dec 33, Hex 21		
Physical Address	ID1 = 48h	**Instance**	
Description			
Type	R		

7	6	5	4	3	2	1	0
STS_PREQ3	STS_PREQ2	STS_PREQ1	STS_VSYSMIN_HI	STS_PLUG_DET	STS_USB_ID	STS_RPWRON	STS_PWRON

Bits	Field Name	Description	Type	Reset
7	STS_PREQ3	Level status of PREQ3 0: Low 1: High	R	–
6	STS_PREQ2	Level status of PREQ2 0: Low 1: High	R	–
5	STS_PREQ1	Level status of PREQ1 0: Low 1: High	R	–
4	STS_VSYSMIN_HI	Level status of VSYSMIN_HI comparator 0: VSYS<VSYSMIN_HI 1: VSYS>VSYSMIN_HI	R	–
3	STS_PLUG_DET	Level status of an AC or USB charger plug detection 0: No charger plugged 1: A charger is plugged	R	–
2	STS_USB_ID	Level status of USB ID 0: ID pin not grounded 1: ID pin grounded	R	–
1	STS_RPWRON	Level status of RPWRON button after debouncing 0: Low 1: High	R	–
0	STS_PWRON	Level status of PWRON button after debouncing 0: Low 1: High	R	–

2.3.4 PHOENIX_LAST_TURNOFF_STS Register

Table 57. PHOENIX_LAST_TURNOFF_STS

Address	Dec 34, Hex 22		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description			
Type			

7	6	5	4	3	2	1	0
FALLBACK	DEVOFF_RPWRON	DEVOFF_SHORT	DEVOFF_WDT	DEVOFF_TSHUT	DEVOFF_BCK	DEVOFF_LPK	OSC_RC32K

Bits	Field Name	Description	Type	Reset
7	FALLBACK	This bit is set to 1 to indicate that the last turn off was due to a system supply drop below VSYSMIN_LO when PMIC is ACTIVE and a the Charger DCDC is ON. Cleared on a write access	R/W	0
6	DEVOFF_RPWRON	This bit is set to 1 to indicate that the last turn off was due to RPWRON. Cleared on a write access	R/W	0
5	DEVOFF_SHORT	This bit is set to 1 to indicate that the last turn off was due to a shorted power resource (LDO or SMPS). Cleared on a write access	R/W	0
4	DEVOFF_WDT	This bit is set to 1 to indicate that the last turn off was due to a primary watchdog expiration. Cleared on a write access	R/W	0
3	DEVOFF_TSHUT	This bit is set to 1 to indicate that the last turn off was due to a thermal shutdown event. Cleared on a write access	R/W	0
2	DEVOFF_BCK	This bit is set to 1 to indicate that the last turn off was due to a system supply (battery) bounce when ACTIVE or a battery removal when in WAIT_ON. Cleared on a write access	R/W	0
1	DEVOFF_LPK	This bit is set to 1 to indicate that the last turn off was due to a long key press event. Cleared on a write access	R/W	0
0	OSC_RC32K	0: 32-kHz clock from RC 32 kHz 1: 32-kHz clock from 32-kHz crystal oscillator	R	0

Notes:

- LDOs / SMPS short interrupt is cleared on a NRESPWRON falling edge

2.3.5 VSYSMIN_LO_THRESHOLD Register

Table 58. VSYSMIN_LO_THRESHOLD

Address	Dec 35, Hex 23		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	VSYS_5	VSYS_4	VSYS_3	VSYS_2	VSYS_1	VSYS_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	VSYS_5	VSYS[5:0] = 00000001 = 2.05 V VSYS[5:0] = 00000010 = 2.1 V VSYS[5:0] = 00000011 = 2.15 V VSYS[5:0] = 00000100 = 2.2 V VSYS[5:0] = 00000101 = 2.25 V VSYS[5:0] = 00000110 = 2.3 V VSYS[5:0] = 00000111 = 2.35 V VSYS[5:0] = 00001000 = 2.4 V VSYS[5:0] = 00001001 = 2.45 V	R	EPROM
4	VSYS_4	VSYS[5:0] = 00001010 = 2.5 V VSYS[5:0] = 00001011 = 2.55 V VSYS[5:0] = 00001100 = 2.6 V VSYS[5:0] = 00001101 = 2.65 V VSYS[5:0] = 00001110 = 2.7 V VSYS[5:0] = 00001111 = 2.75 V VSYS[5:0] = 00010000 = 2.8 V VSYS[5:0] = 00010001 = 2.85 V VSYS[5:0] = 00010010 = 2.9 V	R	EPROM
3	VSYS_3	VSYS[5:0] = 00010011 = 2.95 V VSYS[5:0] = 00010100 = 3 V VSYS[5:0] = 00010101 = 3.05 V VSYS[5:0] = 00010110 = 3.1 V VSYS[5:0] = 00010111 = Reserved .... VSYS[5:0] = 00111111= Reserved	R	EPROM
2	VSYS_2		R	EPROM
1	VSYS_1		R	EPROM
0	VSYS_0		R	EPROM

2.3.6 VSYSMIN_HI_THRESHOLD Register

Table 59. VSYSMIN_HI_THRESHOLD

Address	Dec 36, Hex 24		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	VSYS_5	VSYS_4	VSYS_3	VSYS_2	VSYS_1	VSYS_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	VSYS_5	VSYS[5:0] = 00000001 = 2.05 V VSYS[5:0] = 00000010 = 2.1 V VSYS[5:0] = 00000011 = 2.15 V VSYS[5:0] = 00000100 = 2.2 V VSYS[5:0] = 00000101 = 2.25 V VSYS[5:0] = 00000110 = 2.3 V VSYS[5:0] = 00000111 = 2.35 V VSYS[5:0] = 00001000 = 2.4 V VSYS[5:0] = 00001001 = 2.45 V	R/W	EPROM
4	VSYS_4	VSYS[5:0] = 00001010 = 2.5 V VSYS[5:0] = 00001011 = 2.55 V VSYS[5:0] = 00001100 = 2.6 V VSYS[5:0] = 00001101 = 2.65 V VSYS[5:0] = 00001110 = 2.7 V VSYS[5:0] = 00001111 = 2.75 V VSYS[5:0] = 00010000 = 2.8 V VSYS[5:0] = 00010001 = 2.85 V VSYS[5:0] = 00010010 = 2.9 V	R/W	EPROM
3	VSYS_3	VSYS[5:0] = 00010011 = 2.95 V VSYS[5:0] = 00010100 = 3 V VSYS[5:0] = 00010101 = 3.05 V VSYS[5:0] = 00010110 = 3.1 V VSYS[5:0] = 00010111 = 3.15 V VSYS[5:0] = 00011000 = 3.2 V VSYS[5:0] = 00011001 = 3.25 V VSYS[5:0] = 00011010 = 3.3 V VSYS[5:0] = 00011011 = 3.35 V	R/W	EPROM

Bits	Field Name	Description	Type	Reset
2	VSYS_2	VSYS[5:0] = 00011100 = 3.4 V VSYS[5:0] = 00011101 = 3.45 V VSYS[5:0] = 00011110 = 3.5 V VSYS[5:0] = 00011111 = 3.55 V VSYS[5:0] = 00100000 = 3.6 V VSYS[5:0] = 00100001 = 3.65 V VSYS[5:0] = 00100010 = 3.7 V VSYS[5:0] = 00100011 = 3.75 V VSYS[5:0] = 00100100 = 3.8 V	R/W	EPROM
1	VSYS_1	VSYS[5:0] = 00100101 = 3.85 V VSYS[5:0] = 00100110 = 3.9 V VSYS[5:0] = 00100111 = 3.95 V VSYS[5:0] = 00101000 = 4 V VSYS[5:0] = 00101001 = 4.05 V VSYS[5:0] = 00101001 = 4.1 V VSYS[5:0] = 00101011 = 4.15 V VSYS[5:0] = 00101100 = 4.2 V VSYS[5:0] = 00101101 = 4.25 V	R/W	EPROM
0	VSYS_0	VSYS[5:0] = 00101110 = 4.3 V VSYS[5:0] = 00101110 = 4.35 V VSYS[5:0] = 00110000 = 4.4 V VSYS[5:0] = 00110001 = 4.45 V VSYS[5:0] = 00110010 = 4.5 V VSYS[5:0] = 00110011 = 4.55 V VSYS[5:0] = 00110100 = 4.6 V	R/W	EPROM

Notes:

- This register is also used in write mode for VSYS_MONITORING comparator

2.3.7 PHOENIX_DEV_ON Register

Table 60. PHOENIX_DEV_ON

Address	Dec 37, Hex 25		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type	W/A		

7	6	5	4	3	2	1	0
RESERVED	SW_RESET	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	DEVOFF

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	SW_RESET	Writing 1 restarts the Phoenix device (turn-off sequence followed by turn-on sequence). This bit is cleared automatically.	W/A	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	RESERVED	Reserved	R	0
0	DEVOFF	Writing 1 starts an ACT2OFF or SLP2OFF transition. This bit is cleared automatically.	W/A	0

2.3.8 VBATMIN_HI_THRESHOLD Register

Table 61. VBATMIN_HI_THRESHOLD

Address	Dec 38, Hex 26		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	VBAT_5	VBAT_4	VBAT_3	VBAT_2	VBAT_1	VBAT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	VBAT_5	VBAT[5:0] <= 000000 = 2.95 V ...	R/W	EPROM
4	VBAT_4	VBAT[5:0] <= 010011 = 2.95 V VBAT[5:0] = 010100 = 3.05 V	R/W	EPROM
3	VBAT_3	VBAT[5:0] = 010101 = 3.05 V VBAT[5:0] = 010110 = 3.15 V VBAT[5:0] = 010111 = 3.15 V VBAT[5:0] = 011000 = 3.25 V	R/W	EPROM
2	VBAT_2	VBAT[5:0] = 011001 = 3.25 V VBAT[5:0] = 011010 = 3.35 V VBAT[5:0] = 011011 = 3.35 V VBAT[5:0] = 011100 = 3.45 V	R/W	EPROM
1	VBAT_1	VBAT[5:0] = 011101 = 3.45 V VBAT[5:0] = 011110 = 3.55 V VBAT[5:0] = 011111 = 3.55 V VBAT[5:0] >= 100000 = 3.70 V	R/W	EPROM
0	VBAT_0	... VBAT[5:0] >= 111111 = 3.70 V	R/W	EPROM

2.3.9 STS_PWR_GRP_STATE Register

Table 62. STS_PWR_GRP_STATE

Address	Dec 39, Hex 27		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	State of the device: 00: OFF 01: Reserved 10: ACTIVE 11: SLEEP	R	0
0	STATE_0		R	0

2.3.10 PH_CFG_VSYSLOW Register

Table 63. PH_CFG_VSYSLOW

Address	Dec 40, Hex 28		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
BB_SEL	BB_MSK	DELAY_5	DELAY_4	DELAY_3	DELAY_2	DELAY_1	DELAY_0

Bits	Field Name	Description	Type	Reset
7	BB_SEL	0: Battery re-insertion restart mode: If a good system voltage/battery is detected after the delay counter expiration, system will restart and will flag this event as starting condition. If a charger is plugged charger plug will be flagged as starting condition. 1: Battery bounce restart mode: If a good system voltage/battery is detected before the delay counter expiration (short disconnect), system will restart if previous state was active or sleep. If previous state was wait-on or if the counter delay expires, system waits for a switch-on event to restart. An EPROM bit allows masking this bit and forcing the functionality to be always battery re-insertion restart mode See PHOENIX_START_CONDITION RESTART_BB register bits	R/W	0
6	BB_MSK	0: It restarts in case of a system voltage bounce inferior to the DELAY 1: It does not restart on a $VSYS_{LOW}$ event	R/W	0
5	DELAY_5	$VSYS_{LOW}$ delay Minimum: delay x 40 ms + 20 ms Maximum: delay x 40 ms + 30 ms Note that the power cut accuracy is ±10 ms	R/W	0
4	DELAY_4		R/W	0
3	DELAY_3		R/W	0
2	DELAY_2		R/W	0
1	DELAY_1		R/W	0
0	DELAY_0		R/W	0

2.3.11 PH_STS_BOOT Register

Table 64. PH_STS_BOOT

Address	Dec 41, Hex 29		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description			
Type	N/A		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BOOT2	BOOT1	BOOT0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	BOOT2	EPROM PROGRAMMABLE	R	N/A
1	BOOT1	EPROM PROGRAMMABLE	R	N/A
0	BOOT0	0: High values used for VSYSMIN_HI and VSYSMIN_LO threshold(EPROM programmable) 1: Low values used for VSYSMIN_HI and VSYSMIN_LO threshol (EPROM programmable)	R	N/A

Note:

- This register is updated during the power transition from NOSUPPLY to WAITON state.

2.3.12 PHOENIX_SENS_TRANSITION Register

Table 65. PHOENIX_SENS_TRANSITION

Address	Dec 42, Hex 2A		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
SENS_PREQ3	SENS_PREQ2	SENS_PREQ1	RESERVED	RESERVED	RESERVED	RESERVED	PREQ3_VOLT_CFG

Bits	Field Name	Description	Type	Reset
7	SENS_PREQ3	Polarity PREQ3: 0: Resources assigned to PREQ3 are set active when PREQ3 = 0. 1: Resources assigned to PREQ3 are set active when PREQ3 = 1.	R/W	1
6	SENS_PREQ2	Polarity PREQ2: 0: Resources assigned to PREQ2 are set active when PREQ2 = 0. 1: Resources assigned to PREQ2 are set active when PREQ2 = 1.	R/W	1
5	SENS_PREQ1	0: The Phoenix device wakes up on a PREQ1 falling edge. 1: The Phoenix device wakes up on a PREQ1 rising edge.	R/W	1
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	RESERVED	Reserved	R	0
0	PREQ3_VOLT_CFG	0: 1.2-V input voltage supply (default) 1: 1.8-V input voltage supply	R/W	0

Notes:

- The sensitivity bit, SENS_PREQ, must be set before unmasking any PREQ event.

2.3.13 PHOENIX_SEQ_CFG Register

Table 66. PHOENIX_SEQ_CFG

Address	Dec 43, Hex 2B		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	SPARE	SEQ_MSK_VSYS_CMP

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	SPARE	SPARE	R/W	0
0	SEQ_MSK_VSYS_CMP	0: The VSYSMIN_HI voltage comparator output is not masked, to check a valid OFF to ACTIVE transition. The Phoenix device may start if VSYS > VSYSMIN_HI. 1: The VSYSMIN_HI voltage comparator output is disabled (comparator status is considered to be 1) to bypass this check in OFF to active transition or to avoid false interrupts when switching on. The Phoenix device may start if VSYS > VSYSMIN_LO.	R/W	0

2.3.14 PRIMARY_WATCHDOG_CFG Register

Table 67. PRIMARY_WATCHDOG_CFG

Address	Dec 44, Hex 2C		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	WDT_6	WDT_5	WDT_4	WDT_3	WDT_2	WDT_1	WDT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	WDT_6	Primary watchdog time value, from 1 second to 127 seconds, with a 1-second step: Writing 0000000 will set 0000001 (1 second). 0000000: 1 s 0000001: 1 s 0000010: 2 s 0000011: 3 s ... 0011111: 31 s 0100000: 32 s (default) 0100001: 33 s ... 1111111: 127 s	R/W	0
5	WDT_5		R/W	1
4	WDT_4		R/W	0
3	WDT_3		R/W	0
2	WDT_2		R/W	0
1	WDT_1		R/W	0
0	WDT_0		R/W	0

Notes:

- The primary watchdog counter is initialized with the PRIMARY_WATCHDOG_CFG register when NRESPWRON = 0.
- The counter starts as soon as NRESPWRON is released.
- The primary watchdog can be disabled by an EPROM bit.
- A T4 transition (switch-off) is performed when the watchdog timer expired.
- Software must periodically write desired value in this register to reset counter

2.3.15 KEY_PRESS_DURATION_CFG Register

Table 68. KEY_PRESS_DURATION_CFG

Address	Dec 45, Hex 2D		
Physical Address	ID1 = 48h	**Instance**	Backup Domain Config Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
KPD_STS	LPK_TIME	RESERVED	KPD_4	KPD_3	KPD_2	KPD_1	KPD_0

Bits	Field Name	Description		Type	Reset	
					Backup	Config
7	KPD_STS	Key press duration status. This bit is set to 1 if PWRON is maintained low for a duration time higher than KPD [4:0]. This bit is cleared on read.		R/W		0
6	LPK_TIME	Long press key time before switch off/restart[1] the device 0: 4 second 1: 8 second		R/W		1
5	RESERVED	Reserved		R	0	
4	KPD_4	Key press duration value, from 50 ms to 1.55 seconds, by 50-ms step:		R/W	0	
3	KPD_3	00000: 050 ms 00001: 050 ms 00010: 100 ms (default) 00011: 150 ms	10000: 800 ms 10001: 850 ms 10010: 900 ms 10011: 950 ms	R/W	0	
2	KPD_2	00100: 200 ms 00101: 250 ms 00110: 300 ms 00111: 350 ms	10100: 1000 ms 10101: 1050 ms 10110: 1100 ms 10111: 1150 ms	R/W	0	
1	KPD_1	01000: 400 ms 01001: 450 ms 01010: 500 ms 01011: 550 ms	11000: 1200 ms 11001: 1250 ms 11010: 1300 ms 11011: 1350 ms	R/W	0	
0	KPD_0	01100: 600 ms 01101: 650 ms 01110: 700 ms 01111: 750 ms	11100: 1400 ms 11101: 1450 ms 11110: 1500 ms 11111: 1550 ms	R/W	0	

(1) Long Key Press beavior depends on LPK_RESTART EPROM bit.

2.3.16 SMPS_LDO_SHORT_STS Register

Table 69. SMPS_LDO_SHORT_STS

Address	Dec 46, Hex 2E		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	SHORTLDO7	SHORTLDO5	SHORTSMPSLDO

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	SHORTLDO7	Indicate a short on LDO7 Status bit clear by a write access	R/W	0
1	SHORTLDO5	Indicate a short on LDO5 Status bit clear by a write access	R/W	0
0	SHORTSMPSLDO	Indicate a short on others LDO/SMPS Status bit clear by a write access	R/W	0

2.4 PMC Slave Module – Broadcast

2.4.1 BROADCAST_ADDRESS_ALL Register

Table 70. BROADCAST_ADDRESS_ALL

Address	Dec 49, Hex 31		
Physical Address	ID1 = 48h	**Instance**	
Description			
Type	W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	–
6	RESERVED	Reserved	R	–
5	RESERVED	Reserved	R	–
4	RESERVED	Reserved	R	–
3	RESERVED	Reserved	R	–
2	RESERVED	Reserved	R	–
1	STATE_1	Resource state: 00: OFF 01: ON 10: OFF 11: SLEEP	W	–
0	STATE_0		W	–

Notes:

- This register is used to broadcast a change state to all resources. GRP determines if the resource is targeted by the state change request.
- Note that a resource can be driven by several group command registers or directly with its own command register. A read will return the command apply to the resource.

Table 71. BROADCAST_ADDRESS_ALL Resources List

Provider			Clocks, Resets, and Comparators		Reference
SMPS	**LDO**	**External**	**Internal**	**External**	**Internal**
See Table 75			See Table 77		See Table 73

2.4.2 BROADCAST_ADDRESS_REF Register

Table 72. BROADCAST_ADDRESS_REF

Address	Dec 50, Hex 32		
Physical Address	ID1 = 48h	**Instance**	
Description			
Type	W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	–
6	RESERVED	Reserved	R	–
5	RESERVED	Reserved	R	–
4	RESERVED	Reserved	R	–
3	RESERVED	Reserved	R	–
2	RESERVED	Reserved	R	–
1	STATE_1	Resource state: 00: OFF 01: ON 10: OFF 11: SLEEP	W	–
0	STATE_0		W	–

Notes:

- Note that a resource can be driven by several group command registers or directly with its own command register. A read will return the command apply to the resource.
- This register is used to target all reference resources.

Table 73. BROADCAST_ADRESS_REF Resources List

Internal
BIAS_CFG_STATE
VRTC_CFG_STATE

2.4.3 BROADCAST_ADDRESS_PROV Register

Table 74. BROADCAST_ADDRESS_PROV

Address	Dec 51, Hex 33		
Physical Address	ID1 = 48h	**Instance**	
Description			
Type	W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	–
6	RESERVED	Reserved	R	–
5	RESERVED	Reserved	R	–
4	RESERVED	Reserved	R	–
3	RESERVED	Reserved	R	–
2	RESERVED	Reserved	R	–
1	STATE_1	Resource state: 00: OFF 01: ON 10: OFF 11: SLEEP	W	–
0	STATE_0		W	–

Notes:

- Note that a resource can be driven by several group command registers or directly with its own command register. A read will return the command apply to the resource.
- This register is used to target all power resources providers.

Table 75. BROADCAST_ADDRESS_PROV Resources List

SMPS	LDO	External
SMPS4_CFG_STATE	VANA_CFG_STATE	REGEN1_CFG_STATE
SMPS5_CFG_STATE	LDO2_CFG_STATE	REGEN2_CFG_STATE
SMPS1_CFG_STATE	LDO4_CFG_STATE	
SMPS2_CFG_STATE	LDO3_CFG_STATE	
SMPS3_CFG_STATE	LDO6_CFG_STATE	
	LDOLN_CFG_STATE	
	LDO5_CFG_STATE	
	LDO1_CFG_STATE	
	LDOUSB_CFG_STATE	
	LDO7_CFG_STATE	

2.4.4 BROADCAST_ADDRESS_CLK_RST Register

Table 76. BROADCAST_ADDRESS_CLK_RST

Address	Dec 52, Hex 34		
Physical Address	ID1 = 48h	**Instance**	
Description			
Type	W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	–
6	RESERVED	Reserved	R	–
5	RESERVED	Reserved	R	–
4	RESERVED	Reserved	R	–
3	RESERVED	Reserved	R	–
2	RESERVED	Reserved	R	–
1	STATE_1	Resource state: 00: OFF 01: ON 10: OFF 11: SLEEP	W	–
0	STATE_0		W	–

Notes:

- Note that a resource can be driven by several group command registers or directly with its own command register. A read will return the command apply to the resource.
- This register is used to target all clocks and resets resources.

Table 77. BROADCAST_ADDRESS_CLK_RST Resources List

Internal	External
NRESPWRON_CFG_STATE	SYSEN_CFG_STATE
CLK32KAO_CFG_STATE	
CLK32KG_CFG_STATE	
CLK32KAUDIO_CFG_STATE	
VSYSMIN_HI_CFG_STATE	
TMP_CFG_STATE	
RC6MHZ_CFG_STATE	

2.5 PMC Slave Module – SMPS Regulators

Notes:

- Setting a voltage to zero will turn off immediately the resource (*_CFG_STATE.STATE = 0x0). By setting back a voltage different to zero, the resource state is reassigned.
- Voltage register default value are reloaded after each FSM transition to WAITON.

The code for the different output voltages are summarized in Table 78. All the SMPS regulators have the same coding. Values are typical

Table 78. SMPS Output Voltage Selection Code (Standard Mode Without Offset)

CODE	VOUT (mV)	CODE	VOUT (mV)	CODE	VOUT (mV)	CODE	VOUT (mV)
000000	0	010000	797.6	100000	1000.2	110000	1202.7
000001	607.7	010001	810.3	100001	1012.8	110001	1215.4
000010	620.4	010010	822.9	100010	1025.5	110010	1228.0
000011	633.0	010011	835.6	100011	1038.1	110011	1240.7
000100	645.7	010100	848.2	100100	1050.8	110100	1253.4
000101	658.3	010101	860.9	100101	1063.5	110101	1266.0
000110	671.0	010110	873.6	100110	1076.1	110110	1278.7
000111	683.7	010111	886.2	100111	1088.8	110111	1291.3
001000	696.3	011000	898.9	101000	1101.4	111000	1304.0
001001	709.0	011001	911.5	101001	1114.1	111001	1316.7
001010	721.6	011010	924.2	101010	1126.8	111010	1367.4
001011	734.3	011011	936.9	101011	1139.4	111011	1519.3
001100	747.0	011100	949.5	101100	1152.1	111100	1823.1
001101	759.6	011101	962.2	101101	1164.7	111101	1924.4
001110	772.3	011110	974.8	101110	1177.4	111110	2127.0
001111	785.0	011111	987.5	101111	1190.1	111111	Reserved

Table 79. SMPS Output Voltage Selection Code (Standard Mode With Offset)

CODE	VOUT (mV)	CODE	VOUT (mV)	CODE	VOUT (mV)	CODE	VOUT (mV)
000000	0	010000	898.9	100000	1101.5	110000	1304.0
000001	709.0	010001	911.6	100001	1114.1	110001	1316.7
000010	721.7	010010	924.2	100010	1126.8	110010	1329.3
000011	734.3	010011	936.9	100011	1139.4	110011	1342.0
000100	747.0	010100	949.5	100100	1152.1	110100	1354.7
000101	759.6	010101	962.2	100101	1164.8	110101	1367.3
000110	772.3	010110	974.9	100110	1177.4	110110	1380.0
000111	785.0	010111	987.5	100111	1190.1	110111	1392.6
001000	797.6	011000	1000.2	101000	1202.7	111000	1405.3
001001	810.3	011001	1012.8	101001	1215.4	111001	1418.0
001010	822.9	011010	1025.5	101010	1228.1	111010	1367.4
001011	835.6	011011	1038.2	101011	1240.7	111011	1519.3
001100	848.3	011100	1050.8	101100	1253.4	111100	1823.1
001101	860.9	011101	1063.5	101101	1266.0	111101	1924.4
001110	873.6	011110	1076.1	101110	1278.7	111110	2127.0
001111	886.2	011111	1088.8	101111	1291.4	111111	Reserved

Table 80. SMPS Output Voltage Selection Code (Extended Mode Without Offset)

CODE	VOUT (V)	CODE	VOUT (V)	CODE	VOUT (V)	CODE	VOUT (V)
000000	0	010000	2.431	100000	3.048	110000	3.665
000001	1.852	010001	2.469	100001	3.087	110001	3.704
000010	1.891	010010	2.508	100010	3.125	110010	3.743
000011	1.929	010011	2.547	100011	3.164	110011	3.781
000100	1.968	010100	2.585	100100	3.202	110100	3.820
000101	2.006	010101	2.624	100101	3.241	110101	3.858
000110	2.045	010110	2.662	100110	3.280	110110	3.897
000111	2.084	010111	2.701	100111	3.318	110111	3.936
001000	2.122	011000	2.739	101000	3.357	111000	3.974
001001	2.161	011001	2.778	101001	3.395	111001	4.013
001010	2.199	011010	2.817	101010	3.434	111010	2.084
001011	2.238	011011	2.855	101011	3.473	111011	2.315
001100	2.276	011100	2.894	101100	3.511	111100	2.778
001101	2.315	011101	2.932	101101	3.550	111101	2.932
001110	2.354	011110	2.971	101110	3.588	111110	3.241
001111	2.392	011111	3.010	101111	3.627	111111	Reserved

The extended output voltage range can be enabled with an EPROM bit. In this mode, the SMPS voltage level step is 38.6 mV. Some trimming adjustments can shift those levels up or down by one or two settings, meaning ±9.7 mV or 19.3 mV. The resistor divider ratio is 21/64 versus the original configuration set (SMPS_MULT).

Table 81. SMPS Output Voltage Selection Code (Extended Mode With Offset)

CODE	VOUT (V)	CODE	VOUT (V)	CODE	VOUT (V)	CODE	VOUT (V)
000000	0	010000	2.739	100000	3.357	110000	3.974
000001	2.161	010001	2.778	100001	3.395	110001	4.013
000010	2.199	010010	2.817	100010	3.434	110010	4.051
000011	2.238	010011	2.855	100011	3.473	110011	4.090
000100	2.277	010100	2.894	100100	3.511	110100	4.128
000101	2.315	010101	2.932	100101	3.550	110101	4.167
000110	2.354	010110	2.971	100110	3.588	110110	4.206
000111	2.392	010111	3.010	100111	3.627	110111	4.244
001000	2.431	011000	3.048	101000	3.665	111000	4.283
001001	2.469	011001	3.087	101001	3.704	111001	4.321
001010	2.508	011010	3.125	101010	3.743	111010	4.167
001011	2.547	011011	3.164	101011	3.781	111011	2.315
001100	2.585	011100	3.202	101100	3.820	111100	2.778
001101	2.624	011101	3.241	101101	3.858	111101	2.932
001110	2.662	011110	3.280	101110	3.897	111110	3.241
001111	2.701	011111	3.318	101111	3.936	111111	Reserved

2.5.1 SMPS4_CFG_TRANS Register

Table 82. SMPS4_CFG_TRANS

Address	Dec 65, Hex 41		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: AUTO (PWM/PFM) 10: Reserved 11: FORCE PWM	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: AUTO (PWM/PFM) 10: Reserved 11: FORCE PWM	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: AUTO (PWM/PFM) 10: Reserved 11: FORCE PWM	R/W	0
0	ACT_0		R	1

2.5.2 SMPS4_CFG_STATE Register

Table 83. SMPS4_CFG_STATE

Address	Dec 66, Hex 42		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Provider		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.5.3 SMPS4_CFG_VOLTAGE Register

Table 84. SMPS4_CFG_VOLTAGE

Address	Dec 68, Hex 44		
Physical Address	ID0 = 48h	**Instance**	State Domain Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset	
				State Domian	Backup Domain
7	WR_S	Warm reset sensitivity 0: Reload the default VSEL [5:0] value when a warm reset occurs 1: Keep the voltage configuration settings, same VSEL [5:0] value just before the warm reset event	R/W		0
6	RESERVED	Reserved	R	0	
5	VSEL_5	Voltage to apply to the resource. See Table 78.	R/W	EPROM	
4	VSEL_4		R/W	EPROM	
3	VSEL_3		R/W	EPROM	
2	VSEL_2		R/W	EPROM	
1	VSEL_1		R/W	EPROM	
0	VSEL_0		R/W	EPROM	

2.5.4 SMPS5_CFG_TRANS Register

Table 85. SMPS5_CFG_TRANS

Address	Dec 71, Hex 47		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: AUTO (PWM/PFM) 10: Reserved 11: FORCE PWM	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: AUTO (PWM/PFM) 10: Reserved 11: FORCE PWM	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: AUTO (PWM/PFM) 10: Reserved 11: FORCE PWM	R/W	0
0	ACT_0		R	1

Notes:

- The register cannot be updated in real time since the DBB IC may be OFF in this situation.

2.5.5 SMPS5_CFG_STATE Register

Table 86. SMPS5_CFG_STATE

Address	Dec 72, Hex 48		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Provider		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.5.6 SMPS5_CFG_FORCE Register

Table 87. SMPS5_CFG_FORCE

Address	Dec 73, Hex 49		
Physical Address	ID0 = 12h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
CMD_1	CMD_0	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset
7	CMD_1	DVS command: 00: Force Active 01: Active	R/W	0
6	CMD_0	10 and VSEL [5:0] = 0x0: Off 10 and VSEL [5:0] ≠ 0x0: Force Sleep 11: Sleep	R/W	0
5	VSEL_5	Voltage to apply to the resource when it is a force command. See Table 78.	R/W	EPROM
4	VSEL_4		R/W	EPROM
3	VSEL_3		R/W	EPROM
2	VSEL_2		R/W	EPROM
1	VSEL_1		R/W	EPROM
0	VSEL_0		R/W	EPROM

2.5.7 SMPS5_CFG_VOLTAGE Register

Table 88. SMPS5_CFG_VOLTAGE

Address	Dec 74, Hex 4A		
Physical Address	ID0 = 12h	**Instance**	State Domain Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset	
				State Domian	Backup Domain
7	WR_S	Warm reset sensitivity 0: Reload the default VSEL [5:0] value when a warm reset occurs 1: Keep the voltage configuration settings, same VSEL [5:0] value just before the warm reset event	R/W		0
6	RESERVED	Reserved	R	0	
5	VSEL_5	Voltage to apply to the resource when it is not a DVS force command. See Table 78.	R/W	EPROM	
4	VSEL_4		R/W	EPROM	
3	VSEL_3		R/W	EPROM	
2	VSEL_2		R/W	EPROM	
1	VSEL_1		R/W	EPROM	
0	VSEL_0		R/W	EPROM	

2.5.8 SMPS5_CFG_STEP Register

Table 89. SMPS5_CFG_STEP

Address	Dec 75, Hex 4B		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
NO_STEP	RESERVED	RESERVED	STEP_4	STEP_3	STEP_2	STEP_1	STEP_0

Bits	Field Name	Description	Type	Reset
7	NO_STEP	0: Voltage applied according to step value 1: No voltage ramping, the voltage is directly applied	R/W	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	STEP_4	Define the voltage ramping delay between two voltage steps.Note that a minimum delay of 6 clock (6 MHz) cycles is hard coded (that is, 12.5mV/µs). So setting a lower value than 00110 has no effect on the step duration.	R/W	0
3	STEP_3		R/W	0
2	STEP_2		R/W	1
1	STEP_1		R/W	1
0	STEP_0		R/W	0

2.5.9 SMPS1_CFG_TRANS Register

Table 90. SMPS1_CFG_TRANS

Address	Dec 83, Hex 53		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: AUTO (PWM/PFM) 10: Reserved 11: FORCE PWM	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: AUTO (PWM/PFM) 10: Reserved 11: FORCE PWM	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: AUTO (PWM/PFM) 10: Reserved 11: FORCE PWM	R/W	0
0	ACT_0		R	1

2.5.10 SMPS1_CFG_STATE Register

Table 91. SMPS1_CFG_STATE

Address	Dec 84, Hex 54		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Provider		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.5.11 SMPS1_CFG_FORCE Register

Table 92. SMPS1_CFG_FORCE

Address	Dec 85, Hex 55		
Physical Address	ID0 = 12h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
CMD_1	CMD_0	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset
7	CMD_1	DVS command: 00: Force Active 01: Active	R/W	0
6	CMD_0	10 and VSEL [5:0] = 0x0: Off 10 and VSEL [5:0] ≠ 0x0: Force Sleep 11: Sleep	R/W	0
5	VSEL_5	Voltage to apply to the resource when it is a force command. See Table 78.	R/W	EPROM
4	VSEL_4		R/W	EPROM
3	VSEL_3		R/W	EPROM
2	VSEL_2		R/W	EPROM
1	VSEL_1		R/W	EPROM
0	VSEL_0		R/W	EPROM

2.5.12 SMPS1_CFG_VOLTAGE Register

Table 93. SMPS1_CFG_VOLTAGE

Address	Dec 86, Hex 56		
Physical Address	ID0 = 12h	**Instance**	State Domain Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset	
				State Domian	Backup Domain
7	WR_S	Warm reset sensitivity: 0: Reload the default VSEL [5:0] value when a warm reset occurs 1: Keep the voltage configuration settings, same VSEL [5:0] value just before the warm reset event	R/W		0
6	RESERVED	Reserved	R	0	
5	VSEL_5	Voltage to apply to the resource when it is not a DVS force command. See Table 78.	R/W	EPROM	
4	VSEL_4		R/W	EPROM	
3	VSEL_3		R/W	EPROM	
2	VSEL_2		R/W	EPROM	
1	VSEL_1		R/W	EPROM	
0	VSEL_0		R/W	EPROM	

2.5.13 SMPS1_CFG_STEP Register

Table 94. SMPS1_CFG_STEP

Address	Dec 87, Hex 57		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
NO_STEP	RESERVED	RESERVED	STEP_4	STEP_3	STEP_2	STEP_1	STEP_0

Bits	Field Name	Description	Type	Reset
7	NO_STEP	0: Voltage applied according to step value 1: No voltage ramping, the voltage is directly applied	R/W	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	STEP_4	Define the voltage ramping delay between two voltage steps.Note that a minimum delay of 6 clock (6 MHz) cycles is hard coded (that is, 12.5 mV/µs). So setting a lower value than 00110 has no effect on the step duration.	R/W	0
3	STEP_3		R/W	0
2	STEP_2		R/W	1
1	STEP_1		R/W	1
0	STEP_0		R/W	0

2.5.14 SMPS2_CFG_TRANS Register

Table 95. SMPS2_CFG_TRANS

Address	Dec 89, Hex 59		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: AUTO (PWM/PFM) 10: Reserved 11: FORCE PWM	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: AUTO (PWM/PFM) 10: Reserved 11: FORCE PWM	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: AUTO (PWM/PFM) 10: Reserved 11: FORCE PWM	R/W	0
0	ACT_0		R	1

2.5.15 SMPS2_CFG_STATE Register

Table 96. SMPS2_CFG_STATE

Address	Dec 90, Hex 5A		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.5.16 SMPS2_CFG_FORCE Register

Table 97. SMPS2_CFG_FORCE

Address	Dec 91, Hex 5B		
Physical Address	ID0 = 12h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
CMD_1	CMD_0	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset
7	CMD_1	DVS command: 00: Force Active 01: Active	R/W	0
6	CMD_0	10 and VSEL [5:0] = 0x0: Off 10 and VSEL [5:0] ≠ 0x0: Force Sleep 11: Sleep	R/W	0
5	VSEL_5	Voltage to apply to the resource when it is a force command. See Table 78.	R/W	EPROM
4	VSEL_4		R/W	EPROM
3	VSEL_3		R/W	EPROM
2	VSEL_2		R/W	EPROM
1	VSEL_1		R/W	EPROM
0	VSEL_0		R/W	EPROM

2.5.17 SMPS2_CFG_VOLTAGE Register

Table 98. SMPS2_CFG_VOLTAGE

Address	Dec 92, Hex 5C		
Physical Address	ID0 = 12h	**Instance**	State Domain Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset	
				State Domian	Backup Domain
7	WR_S	Warm reset sensitivity: 0: Reload the default VSEL [5:0] value when a warm reset occurs 1: Keep the voltage configuration settings, same VSEL [5:0] value just before the warm reset event	R/W		0
6	RESERVED	Reserved	R	0	
5	VSEL_5	Voltage to apply to the resource when it is not a DVS force command. See Table 78.	R/W	EPROM	
4	VSEL_4		R/W	EPROM	
3	VSEL_3		R/W	EPROM	
2	VSEL_2		R/W	EPROM	
1	VSEL_1		R/W	EPROM	
0	VSEL_0		R/W	EPROM	

2.5.18 SMPS2_CFG_STEP Register

Table 99. SMPS2_CFG_STEP

Address	Dec 93, Hex 5D		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
NO_STEP	RESERVED	RESERVED	STEP_4	STEP_3	STEP_2	STEP_1	STEP_0

Bits	Field Name	Description	Type	Reset
7	NO_STEP	0: Voltage applied according to step value 1: No voltage ramping, the voltage is directly applied	R/W	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	STEP_4	Define the voltage ramping delay between two voltage steps.Note that a minimum delay of 6 clock (6 MHz) cycles is hard coded (that is, 12.5 mV/µs). So setting a lower value than 00110 has no effect on the step duration.	R/W	0
3	STEP_3		R/W	0
2	STEP_2		R/W	1
1	STEP_1		R/W	1
0	STEP_0		R/W	0

2.5.19 SMPS3_CFG_TRANS Register

Table 100. SMPS3_CFG_TRANS

Address	Dec 101, Hex 65		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: AUTO (PWM/PFM) 10: Reserved 11: FORCE PWM	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: AUTO (PWM/PFM) 10: Reserved 11: FORCE PWM	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: AUTO (PWM/PFM) 10: Reserved 11: FORCE PWM	R/W	0
0	ACT_0		R	1

2.5.20 SMPS3_CFG_STATE Register

Table 101. SMPS3_CFG_STATE

Address	Dec 102, Hex 66		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Provider		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.5.21 SMPS3_CFG_VOLTAGE Register

Table 102. SMPS3_CFG_VOLTAGE

Address	Dec 104, Hex 68		
Physical Address	ID1 = 48h	**Instance**	State Domain Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset	
				State Domian	Backup Domain
7	WR_S	Warm reset sensitivity: 0: Reload the default VSEL [5:0] value when a warm reset occurs 1: Keep the voltage configuration settings, same VSEL [5:0] value just before the warm reset event	R/W		0
6	RESERVED	Reserved	R	0	
5	VSEL_5	Voltage to apply to the resource. See Table 78.	R/W	EPROM	
4	VSEL_4		R/W	EPROM	
3	VSEL_3		R/W	EPROM	
2	VSEL_2		R/W	EPROM	
1	VSEL_1		R/W	EPROM	
0	VSEL_0		R/W	EPROM	

2.6 PMC Slave Module – LDO Regulators

The code for the different output voltages are summarized in Table 103. All the LDO regulators have the same coding (except VRTC which is fixed). Values are typical.

Table 103. LDO Output Voltage Selection Code

Code	Vout (V)	Code	Vout (V)	Code	Vout (V)	Code	Vout (V)
00000000	0	00001000	1.731	00010000	2.545	00011000	3.359[1]
00000001	1.018	00001001	1.832	00010001	2.647	00011001	Reserved
00000010	1.120	00001010	1.934	00010010	2.749	00011010	Reserved
00000011	1.222	00001011	2.036	00010011	2.850	00011011	Reserved
00000100	1.323	00001100	2.138	00010100	2.952	00011100	Reserved
00000101	1.425	00001101	2.240	00010101	3.054	00011101	Reserved
00000110	1.527	00001110	2.341	00010110	3.156	00011110	Reserved
00000111	1.629	00001111	2.443	00010111	3.258	00011111	2.8

(1) 3.301 typical for LDOUSB

2.6.1 VANA_CFG_TRANS Register

Table 104. VANA_CFG_TRANS

Address	Dec 129, Hex 81		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R/W	0
0	ACT_0		R	1

2.6.2 VANA_CFG_STATE Register

Table 105. VANA_CFG_STATE

Address	Dec 130, Hex 82		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Provider		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.6.3 VANA_CFG_VOLTAGE Register

Table 106. VANA_CFG_VOLTAGE

Address	Dec 131, Hex 83		
Physical Address	ID1 = 48h	**Instance**	State Domain Backup Domain
Description			
Type			

7	6	5	4	3	2	1	0
WR_S	RESERVED	RESERVED	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset	
				State Domian	Backup Domain
7	WR_S	Warm reset sensitivity: 0: Reload the default VSEL [5:0] value when a warm reset occurs. 1: Keep the voltage configuration settings, same VSEL [5:0] value just before the warm reset event.	R/W		0
6	RESERVED	Reserved	R	0	
5	RESERVED	Reserved	R	0	
4	VSEL_4	Voltage to apply to the resource. See Table 103.	R/W	EPROM	
3	VSEL_3		R/W	EPROM	
2	VSEL_2		R/W	EPROM	
1	VSEL_1		R/W	EPROM	
0	VSEL_0		R/W	EPROM	

2.6.4 LDO2_CFG_TRANS Register

Table 107. LDO2_CFG_TRANS

Address	Dec 133, Hex 85		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: AMS (Sleep/Active) 01: Reserved 11: Active	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R/W	0
0	ACT_0		R	1

2.6.5 LDO2_CFG_STATE Register

Table 108. LDO2_CFG_STATE

Address	Dec 134, Hex 86		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Provider		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.6.6 LDO2_CFG_VOLTAGE Register

Table 109. LDO2_CFG_VOLTAGE

Address	Dec 135, Hex 87		
Physical Address	ID1 = 48h	**Instance**	State Domain Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset	
				State Domian	Backup Domain
7	WR_S	Warm reset sensitivity: 0: Reload the default VSEL [5:0] value when a warm reset occurs. 1: Keep the voltage configuration settings, same VSEL [5:0] value just before the warm reset event.	R/W		0
6	RESERVED	Reserved	R	0	
5	VSEL_5	Voltage to apply to the resource. See Table 103.	R/W	EPROM	
4	VSEL_4		R/W	EPROM	
3	VSEL_3		R/W	EPROM	
2	VSEL_2		R/W	EPROM	
1	VSEL_1		R/W	EPROM	
0	VSEL_0		R/W	EPROM	

2.6.7 LDO4_CFG_TRANS Register

Table 110. LDO4_CFG_TRANS

Address	Dec 137, Hex 89		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R/W	0
0	ACT_0		R	1

2.6.8 LDO4_CFG_STATE Register

Table 111. LDO4_CFG_STATE

Address	Dec 138, Hex 8A		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Provider		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.6.9 LDO4_CFG_VOLTAGE Register

Table 112. LDO4_CFG_VOLTAGE

Address	Dec 139, Hex 8B		
Physical Address	ID1 = 48h	**Instance**	State Domain Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset	
				State Domian	Backup Domain
7	WR_S	Warm reset sensitivity 0: Reload the default VSEL [5:0] value when a warm reset occurs. 1: Keep the voltage configuration settings, same VSEL [5:0] value just before the warm reset event.	R/W		0
6	RESERVED	Reserved	R	0	
5	VSEL_5	Voltage to apply to the resource. See Table 103.	R	0	
4	VSEL_4		R/W	EPROM	
3	VSEL_3		R/W	EPROM	
2	VSEL_2		R/W	EPROM	
1	VSEL_1		R/W	EPROM	
0	VSEL_0		R/W	EPROM	

2.6.10 LDO3_CFG_TRANS Register

Table 113. LDO3_CFG_TRANS

Address	Dec 141, Hex 8D		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R/W	0
0	ACT_0		R	1

2.6.11 LDO3_CFG_STATE Register

Table 114. LDO3_CFG_STATE

Address	Dec 142, Hex 8E		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Provider		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.6.12 LDO3_CFG_VOLTAGE Register

Table 115. LDO3_CFG_VOLTAGE

Address	Dec 143, Hex 8F		
Physical Address	ID1 = 48h	**Instance**	State Domain Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset	
				State Domian	Backup Domain
7	WR_S	Warm reset sensitivity: 0: Reload the default VSEL [5:0] value when a warm reset occurs. 1: Keep the voltage configuration settings, same VSEL [5:0] value just before the warm reset event.	R/W		0
6	RESERVED	Reserved	R	0	
5	VSEL_5	Voltage to apply to the resource. See Table 103.	R	0	
4	VSEL_4		R/W	EPROM	
3	VSEL_3		R/W	EPROM	
2	VSEL_2		R/W	EPROM	
1	VSEL_1		R/W	EPROM	
0	VSEL_0		R/W	EPROM	

2.6.13 LDO6_CFG_TRANS Register

Table 116. LDO6_CFG_TRANS

Address	Dec 145, Hex 91		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R/W	0
0	ACT_0		R	1

2.6.14 LDO6_CFG_STATE Register

Table 117. LDO6_CFG_STATE

Address	Dec 146, Hex 92		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Provider		
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.6.15 LDO6_CFG_VOLTAGE Register

Table 118. LDO6_CFG_VOLTAGE

Address	Dec 147, Hex 93		
Physical Address	ID1 = 48h	**Instance**	State Domain Backup Domain
Description			
Type			

7	6	5	4	3	2	1	0
WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset	
				State Domian	Backup Domain
7	WR_S	Warm reset sensitivity: 0: Reload the default VSEL [5:0] value when a warm reset occurs. 1: Keep the voltage configuration settings, same VSEL [5:0] value just before the warm reset event.	R/W		0
6	RESERVED	Reserved	R	0	
5	VSEL_5	Voltage to apply to the resource. See Table 103.	R	0	
4	VSEL_4		R/W	EPROM	
3	VSEL_3		R/W	EPROM	
2	VSEL_2		R/W	EPROM	
1	VSEL_1		R/W	EPROM	
0	VSEL_0		R/W	EPROM	

2.6.16 LDOLN_CFG_TRANS Register

Table 119. LDOLN_CFG_TRANS

Address	Dec 149, Hex 95		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R/W	0
0	ACT_0		R	1

2.6.17 LDOLN_CFG_STATE Register

Table 120. LDOLN_CFG_STATE

Address	Dec 150, Hex 96		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Provider		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.6.18 LDOLN_CFG_VOLTAGE Register

Table 121. LDOLN_CFG_VOLTAGE

Address	Dec 151, Hex 97		
Physical Address	ID1 = 48h	**Instance**	State Domain Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset	
				State Domian	Backup Domain
7	WR_S	Warm reset sensitivity: 0: Reload the default VSEL [5:0] value when a warm reset occurs. 1: Keep the voltage configuration settings, same VSEL [5:0] value just before the warm reset event.	R/W		0
6	RESERVED	Reserved	R	0	
5	VSEL_5	Voltage to apply to the resource. See Table 103.	R/W	EPROM	
4	VSEL_4		R/W	EPROM	
3	VSEL_3		R/W	EPROM	
2	VSEL_2		R/W	EPROM	
1	VSEL_1		R/W	EPROM	
0	VSEL_0		R/W	EPROM	

2.6.19 LDO5_CFG_TRANS Register

Table 122. LDO5_CFG_TRANS

Address	Dec 153, Hex 99		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R/W	0
0	ACT_0		R	1

2.6.20 LDO5_CFG_STATE Register

Table 123. LDO5_CFG_STATE

Address	Dec 154, Hex 9A		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Provider		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

Notes:

- On a MMC card extraction event, the LDO5 regulator is turned off, which means that the LDO5_CFG_STATE register is set to all power groups OFF.
- See MMCCTRL LDO5_AUTO_OFF register bit.

2.6.21 LDO5_CFG_VOLTAGE Register

Table 124. LDO5_CFG_VOLTAGE

Address	Dec 155, Hex 9B		
Physical Address	ID1 = 48h	**Instance**	State Domain Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset	
				State Domian	Backup Domain
7	WR_S	Warm reset sensitivity: 0: Reload the default VSEL [5:0] value when a warm reset occurs. 1: Keep the voltage configuration settings, same VSEL [5:0] value just before the warm reset event.	R/W		0
6	RESERVED	Reserved	R	0	
5	VSEL_5	Voltage to apply to the resource. See Table 103.	R	0	
4	VSEL_4		R/W	EPROM	
3	VSEL_3		R/W	EPROM	
2	VSEL_2		R/W	EPROM	
1	VSEL_1		R/W	EPROM	
0	VSEL_0		R/W	EPROM	

2.6.22 LDO1_CFG_TRANS Register

Table 125. LDO1_CFG_TRANS

Address	Dec 157, Hex 9D		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: AMS (Sleep/Active) 11: Active 10: Reserved	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R/W	0
0	ACT_0		R	1

2.6.23 LDO1_CFG_STATE Register

Table 126. LDO1_CFG_STATE

Address	Dec 158, Hex 9E		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Provider		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.6.24 LDO1_CFG_VOLTAGE Register

Table 127. LDO1_CFG_VOLTAGE

Address	Dec 159, Hex 9F		
Physical Address	ID1 = 48h	**Instance**	State Domain Backup Domain
Description			
Type			

7	6	5	4	3	2	1	0
WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset	
				State Domian	Backup Domain
7	WR_S	Warm reset sensitivity: 0: Reload the default VSEL [5:0] value when a warm reset occurs. 1: Keep the voltage configuration settings, same VSEL [5:0] value just before the warm reset event.	R/W		0
6	RESERVED	Reserved	R	0	
5	VSEL_5	Voltage to apply to the resource. See Table 103.	R	0	
4	VSEL_4		R/W	EPROM	
3	VSEL_3		R/W	EPROM	
2	VSEL_2		R/W	EPROM	
1	VSEL_1		R/W	EPROM	
0	VSEL_0		R/W	EPROM	

2.6.25 LDOUSB_CFG_TRANS Register

Table 128. LDOUSB_CFG_TRANS

Address	Dec 161, Hex A1		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R/W	0
0	ACT_0		R	1

Notes:

- Under certain conditions (charger type detection by USB PHY), LDOUSB can also be controlled by the battery charger.

2.6.26 LDOUSB_CFG_STATE Register

Table 129. LDOUSB_CFG_STATE

Address	Dec 162, Hex A2		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Provider		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.6.27 LDOUSB_CFG_VOLTAGE Register

Table 130. LDOUSB_CFG_VOLTAGE

Address	Dec 163, Hex A3		
Physical Address	ID1 = 48h	**Instance**	State Domain Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset	
				State Domian	Backup Domain
7	WR_S	Warm reset sensitivity: 0: Reload the default VSEL [5:0] value when a warm reset occurs. 1: Keep the voltage configuration settings, same VSEL [5:0] value just before the warm reset event.	R/W		0
6	RESERVED	Reserved	R	0	
5	VSEL_5	Voltage to apply to the resource. See Table 103.	R	0	
4	VSEL_4		R/W	EPROM	
3	VSEL_3		R/W	EPROM	
2	VSEL_2		R/W	EPROM	
1	VSEL_1		R/W	EPROM	
0	VSEL_0		R/W	EPROM	

2.6.28 LDO7_CFG_TRANS Register

Table 131. LDO7_CFG_TRANS

Address	Dec 165, Hex A5		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: AMS (Sleep/Active) 10: Reserved 11: Active	R/W	0
0	ACT_0		R	1

2.6.29 LDO7_CFG_STATE Register

Table 132. LDO7_CFG_STATE

Address	Dec 166, Hex A6		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Provider		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

Notes:

- On a SIM card extraction event, the LDO7 regulator is turned off, which means that the LDO7_CFG_STATE register is set to all power groups OFF
- See SIMCTRL VSIM_AUTO_OFF register bit

2.6.30 LDO7_CFG_VOLTAGE Register

Table 133. LDO7_CFG_VOLTAGE

Address	Dec 167, Hex A7		
Physical Address	ID1 = 48h	**Instance**	State Domain Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
WR_S	RESERVED	VSEL_5	VSEL_4	VSEL_3	VSEL_2	VSEL_1	VSEL_0

Bits	Field Name	Description	Type	Reset	
				State Domian	Backup Domain
7	WR_S	Warm reset sensitivity: 0: Reload the default VSEL [5:0] value when a warm reset occurs. 1: Keep the voltage configuration settings, same VSEL [5:0] value just before the warm reset event.	R/W		0
6	RESERVED	Reserved	R	0	
5	VSEL_5	Voltage to apply to the resource. See Table 103.	R	0	
4	VSEL_4		R/W	EPROM	
3	VSEL_3		R/W	EPROM	
2	VSEL_2		R/W	EPROM	
1	VSEL_1		R/W	EPROM	
0	VSEL_0		R/W	EPROM	

2.7 PMC Slave Module – External Control

2.7.1 REGEN1_CFG_TRANS Register

Table 134. REGEN1_CFG_TRANS

Address	Dec 174, Hex AE		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: ON 1X: Reserved	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: ON 1X: Reserved	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: ON 1X: Reserved	R	0
0	ACT_0		R/W	1

2.7.2 REGEN1_CFG_STATE Register

Table 135. REGEN1_CFG_STATE

Address	Dec 175, Hex AF		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Provider		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.7.3 REGEN2_CFG_TRANS Register

Table 136. REGEN2_CFG_TRANS

Address	Dec 177, Hex B1		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: ON 1X: Reserved	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: ON 1X: Reserved	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: ON 1X: Reserved	R	0
0	ACT_0		R/W	1

2.7.4 REGEN2_CFG_STATE Register

Table 137. REGEN2_CFG_STATE

Address	Dec 178, Hex B2		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Provider		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.7.5 SYSEN_CFG_TRANS Register

Table 138. SYSEN_CFG_TRANS

Address	Dec 180, Hex B4		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: ON 1X: Reserved	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: ON 1X: Reserved	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: ON 1X: Reserved	R	0
0	ACT_0		R/W	1

2.7.6 SYSEN_CFG_STATE Register

Table 139. SYSEN_CFG_STATE

Address	Dec 181, Hex B5		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Clocks, Resets, and Comparators		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.8 PMC Slave Module – Internal Control

Notes:

- NRESPWRON_CFG_TRANS registers are read only.
- NRESPWRON_CFG_STATE register can only be accessed by hardware (power management FSM) in write mode, I2C can only access in read mode, and I2C/JTAG accesses are available in test mode only.

2.8.1 NRESPWRON_CFG_TRANS Register

Table 140. NRESPWRON_CFG_TRANS

Address	Dec 183, Hex B7		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: ON 1X: Reserved	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: ON 1X: Reserved	R	0
2	SLEEP_0		R	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: ON 1X: Reserved	R	0
0	ACT_0		R	1

2.8.2 NRESPWRON_CFG_STATE Register

Table 141. NRESPWRON_CFG_STATE

Address	Dec 184, Hex B8		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Clocks, Resets, and Comparators		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.8.3 CLK32KAO_CFG_TRANS Register

Table 142. CLK32KAO_CFG_TRANS

Address	Dec 186, Hex BA		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: ON 1X: Reserved	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: ON 1X: Reserved	R	0
2	SLEEP_0		R	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: ON 1X: Reserved	R	0
0	ACT_0		R	1

Notes:

- The CLK32KAO_CFG_TRANS registers are read only.
- The CLK32KAO_CFG_STATE register can only be accessed by hardware (power management FSM) in write mode, I^2C can only access in read mode, and I^2C/JTAG accesses are available in test mode.

2.8.4 CLK32KAO_CFG_STATE Register

Table 143. CLK32KAO_CFG_STATE

Address	Dec 187, Hex BB		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Clocks, Resets, and Comparators		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.8.5 CLK32KG_CFG_TRANS Register

Table 144. CLK32KG_CFG_TRANS

Address	Dec 189, Hex BD		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: ON 1X: Reserved	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: ON 1X: Reserved	R	0
2	SLEEP_0		R/W	0
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: ON 1X: Reserved	R	0
0	ACT_0		R/W	1

2.8.6 CLK32KG_CFG_STATE Register

Table 145. CLK32KG_CFG_STATE

Address	Dec 190, Hex BE		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Clocks, Resets, and Comparators		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.8.7 CLK32KAUDIO_CFG_TRANS Register

Table 146. CLK32KAUDIO_CFG_TRANS

Address	Dec 192, Hex C0		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: ON 1X: Reserved	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: ON 1X: Reserved	R	0
2	SLEEP_0		R/W	0
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: ON 1X: Reserved	R	0
0	ACT_0		R/W	1

2.8.8 CLK32KAUDIO_CFG_STATE Register

Table 147. CLK32KAUDIO_CFG_STATE

Address	Dec 193, Hex C1		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Clocks, Resets, and Comparators		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.8.9 VRTC_CFG_TRANS Register

Table 148. VRTC_CFG_TRANS

Address	Dec 195, Hex C3		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: ON 1X: Reserved	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: ON 1X: Reserved	R	1
2	SLEEP_0		R	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: ON 1X: Reserved	R	0
0	ACT_0		R	1

Note:

- See also BBSPOR_CFG register

2.8.10 VRTC_CFG_STATE Register

Table 149. VRTC_CFG_STATE

Address	Dec 196, Hex C4		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Not considered as a provider		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

Notes:

- VRTC_CFG_TRANS registers are read only
- VRTC_CFG_STATE register can only be accessed by HW (Power Management FSM) in write mode, I2C can only access in read mode, I2C/JTAG accesses available in test mode only

2.8.11 BIAS_CFG_TRANS Register

Table 150. BIAS_CFG_TRANS

Address	Dec 198, Hex C6		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: ON 1X: Reserved	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: ON 1X: Reserved	R	0
2	SLEEP_0		R	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: ON 1X: Reserved	R	0
0	ACT_0		R	1

Notes:

- The BIAS_CFG_TRANS registers are read only.
- The BIAS_CFG_STATE register can only be accessed by hardware (power management FSM) in write mode, I^2C can only access in read mode, and I^2C/JTAG accesses are available in test mode only.

2.8.12 BIAS_CFG_STATE Register

Table 151. BIAS_CFG_STATE

Address	Dec 199, Hex C7		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Reference		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.8.13 VSYSMIN_HI_CFG_TRANS Register

Table 152. VSYSMIN_HI_CFG_TRANS

Address	Dec 201, Hex C9		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: ON 1X: Reserved	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: ON 1X: Reserved	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: ON 1X: Reserved	R	0
0	ACT_0		R	1

2.8.14 VSYSMIN_HI_CFG_STATE Register

Table 153. VSYSMIN_HI_CFG_STATE

Address	Dec 202, Hex CA		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Clocks, Resets, and Comparators		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.8.15 RC6MHZ_CFG_TRANS Register

Table 154. RC6MHZ_CFG_TRANS

Address	Dec 204, Hex CC		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: ON 1X: Reserved	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: ON 1X: Reserved	R	0
2	SLEEP_0		R/W	0
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: ON 1X: Reserved	R	0
0	ACT_0		R	1

Notes:

- The RC6MHZ_CFG_TRANS registers are read only.
- The RC6MHZ_CFG_STATE register can only be accessed by hardware (power management FSM) in write mode, I^2C can only access in read mode, and I^2C/JTAG accesses are available in test mode.

2.8.16 RC6MHZ_CFG_STATE Register

Table 155. RC6MHZ_CFG_STATE

Address	Dec 205, Hex CD		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Clocks, Resets, and Comparators		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

2.8.17 TMP_CFG_TRANS Register

Table 156. TMP_CFG_TRANS

Address	Dec 207, Hex CF		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OFF_1	OFF_0	SLEEP_1	SLEEP_0	ACT_1	ACT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	OFF_1	Command to apply to the resource in case of the OFF state: 00: OFF 01: ON 1X: Reserved	R	0
4	OFF_0		R	0
3	SLEEP_1	Command to apply to the resource in case of the SLEEP state: 00: OFF 01: ON 1X: Reserved	R	0
2	SLEEP_0		R/W	1
1	ACT_1	Command to apply to the resource in case of the ACTIVE state: 00: OFF 01: ON 1X: Reserved	R	0
0	ACT_0		R	1

Notes:

- The TMP resource refers to both thermal shutdown and hot-die warning features.
- The TMP resource does not control the charger dedicated thermal shutdown/hot die.
- The TMP_CFG_TRANS registers are read only.
- The TMP_CFG_STATE register can only be accessed by hardware (power management FSM) in write mode, I^2C can only access in read mode, and I^2C/JTAG accesses are available in test mode only

2.8.18 TMP_CFG_STATE Register

Table 157. TMP_CFG_STATE

Address	Dec 208, Hex D0		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description	Category: Clocks, Resets, and Comparators		
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	STATE_1	STATE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	STATE_1	Resource state to apply to the resource according to the power group qualifier: 00: OFF 01: ON 10: OFF 11: SLEEP	R/W	0
0	STATE_0		R/W	0

The TMP_CFG_STATE register controls integrated temperature sensors used for the thermal shutdown function.

2.9 PMC Slave Module – Resources Assignment

2.9.1 PREQ1_RES_ASS_A Register

Table 158. PREQ1_RES_ASS_A

Address	Dec 215, Hex D7		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	LDOUSB	SMPS5	SMPS4	SMPS3	SMPS2	SMPS1

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	LDOUSB	0: PREQ1 has no effect on LDOUSB. 1: LDOUSB control with PREQ1	R/W	EPROM
4	SMPS5	0: PREQ1 has no effect on SMPS5. 1: SMPS5 control with PREQ1	R/W	EPROM
3	SMPS4	0: PREQ1 has no effect on SMPS4. 1: SMPS4 control with PREQ1	R/W	EPROM
2	SMPS3	0: PREQ1 has no effect on SMPS3. 1: SMPS3 control with PREQ1	R/W	EPROM
1	SMPS2	0: PREQ1 has no effect on SMPS2. 1: SMPS2 control with PREQ1	R/W	EPROM
0	SMPS1	0: PREQ1 has no effect on SMPS1. 1: SMPS1 control with PREQ1	R/W	EPROM

2.9.2 PREQ1_RES_ASS_B Register

Table 159. PREQ1_RES_ASS_B

Address	Dec 216, Hex D8		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type			

7	6	5	4	3	2	1	0
LDOLN	LDO7	LDO6	LDO5	LDO4	LDO3	LDO2	LDO1

Bits	Field Name	Description	Type	Reset
7	LDOLN	0: PREQ1 has no effect on LDOLN. 1: LDOLN control with PREQ1	R/W	EPROM
6	LDO7	0: PREQ1 has no effect on LDO7. 1: LDO7 control with PREQ1	R/W	EPROM
5	LDO6	0: PREQ1 has no effect on LDO6. 1: LDO6 control with PREQ1	R/W	EPROM
4	LDO5	0: PREQ1 has no effect on LDO5. 1: LDO5 control with PREQ1	R/W	EPROM
3	LDO4	0: PREQ1 has no effect on LDO4. 1: LDO4 control with PREQ1	R/W	EPROM
2	LDO3	0: PREQ1 has no effect on LDO3. 1: LDO3 control with PREQ1	R/W	EPROM
1	LDO2	0: PREQ1 has no effect on LDO2. 1: LDO2 control with PREQ1	R/W	EPROM
0	LDO1	0: PREQ1 has no effect on LDO1. 1: LDO1 control with PREQ1	R/W	EPROM

2.9.3 PREQ1_RES_ASS_C Register

Table 160. PREQ1_RES_ASS_C

Address	Dec 217, Hex D9		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	VSYSMIN_HI	CLK32KG	CLK32KAUDIO	SYSEN	REGEN2	REGEN1

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	VSYSMIN_HI	0: PREQ1 has no effect on VSYSMIN_HI. 1: VSISMIN_HI control with PREQ1	R/W	EPROM
4	CLK32KG	0: PREQ1 has no effect on CLK32KG. 1: CLK32KG control with PREQ1	R/W	EPROM
3	CLK32KAUDIO	0: PREQ1 has no effect on CLK32KAUDIO. 1: CLK32KAUDIO control with PREQ1	R/W	EPROM
2	SYSEN	0: PREQ1 has no effect on SYSEN. 1: SYSEN control with PREQ1	R/W	EPROM
1	REGEN2	0: PREQ1 has no effect on REGEN2. 1: REGEN2 control with PREQ1	R/W	EPROM
0	REGEN1	0: PREQ1 has no effect on REGEN1. 1: REGEN1 control with PREQ1	R/W	EPROM

2.9.4 PREQ2_RES_ASS_A Register

Table 161. PREQ2_RES_ASS_A

Address	Dec 218, Hex DA		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	LDOUSB	SMPS5	SMPS4	SMPS3	SMPS2	SMPS1

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	LDOUSB	0: PREQ2 has no effect on LDOUSB. 1: LDOUSB control with PREQ2	R/W	0
4	SMPS5	0: PREQ2 has no effect on SMPS5. 1: SMPS5 control with PREQ2	R/W	0
3	SMPS4	0: PREQ2 has no effect on SMPS4. 1: SMPS4 control with PREQ2	R/W	0
2	SMPS3	0: PREQ2 has no effect on SMPS3. 1: SMPS3 control with PREQ2	R	0
1	SMPS2	0: PREQ2 has no effect on SMPS2. 1: SMPS2 control with PREQ2	R/W	0
0	SMPS1	0: PREQ2 has no effect on SMPS1. 1: SMPS1 control with PREQ2	R/W	0

2.9.5 PREQ2_RES_ASS_B Register

Table 162. PREQ2_RES_ASS_B

Address	Dec 219, Hex DB		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type			

7	6	5	4	3	2	1	0
LDOLN	LDO7	LDO6	LDO5	LDO4	LDO3	LDO2	LDO1

Bits	Field Name	Description	Type	Reset
7	LDOLN	0: PREQ2 has no effect on LDOLN. 1: LDOLN control with PREQ2	R/W	0
6	LDO7	0: PREQ2 has no effect on LDO7. 1: LDO7 control with PREQ2	R/W	0
5	LDO6	0: PREQ2 has no effect on LDO6. 1: LDO6 control with PREQ2	R/W	0
4	LDO5	0: PREQ2 has no effect on LDO5. 1: LDO5 control with PREQ2	R/W	0
3	LDO4	0: PREQ2 has no effect on LDO4. 1: LDO4 control with PREQ2	R/W	0
2	LDO3	0: PREQ2 has no effect on LDO3. 1: LDO3 control with PREQ2	R	0
1	LDO2	0: PREQ2 has no effect on LDO2. 1: LDO2 control with PREQ2	R/W	0
0	LDO1	0: PREQ2 has no effect on LDO1. 1: LDO1 control with PREQ2	R/W	0

2.9.6 PREQ2_RES_ASS_C Register

Table 163. PREQ2_RES_ASS_C

Address	Dec 220, Hex DC		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	VSYSMIN_HI	CLK32KG	CLK32KAUDIO	SYSEN	REGEN2	REGEN1

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	VSYSMIN_HI	0: PREQ2 has no effect on VSYSMIN_HI. 1: VSYSMIN_HI control with PREQ2	R/W	0
4	CLK32KG	0: PREQ2 has no effect on CLK32KG. 1: CLK32KG control with PREQ2	R/W	0
3	CLK32KAUDIO	0: PREQ2 has no effect on CLK32KAUDIO. 1: CLK32KAUDIO control with PREQ2	R/W	0
2	SYSEN	0: PREQ2 has no effect on SYSEN. 1: SYSEN control with PREQ2	R	0
1	REGEN2	0: PREQ2 has no effect on REGEN2. 1: REGEN2 control with PREQ2	R/W	0
0	REGEN1	0: PREQ2 has no effect on REGEN1. 1: REGEN1 control with PREQ2	R/W	0

2.9.7 PREQ3_RES_ASS_A Register

Table 164. PREQ3_RES_ASS_A

Address	Dec 221, Hex DD		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	LDOUSB	SMPS5	SMPS4	SMPS3	SMPS2	SMPS1

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	LDOUSB	0: PREQ3 has no effect on LDOUSB. 1: LDOUSB control with PREQ3	R/W	0
4	SMPS5	0: PREQ3 has no effect on SMPS5. 1: SMPS5 control with PREQ3	R/W	0
3	SMPS4	0: PREQ3 has no effect on SMPS4. 1: SMPS4 control with PREQ3	R/W	0
2	SMPS3	0: PREQ3 has no effect on SMPS3. 1: SMPS3 control with PREQ3	R	0
1	SMPS2	0: PREQ3 has no effect on SMPS2. 1: SMPS2 control with PREQ3	R/W	0
0	SMPS1	0: PREQ3 has no effect on SMPS1. 1: SMPS1 control with PREQ3	R/W	0

2.9.8 PREQ3_RES_ASS_B Register

Table 165. PREQ3_RES_ASS_B

Address	Dec 222, Hex DE		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type			

7	6	5	4	3	2	1	0
LDOLN	LDO7	LDO6	LDO5	LDO4	LDO3	LDO2	LDO1

Bits	Field Name	Description	Type	Reset
7	LDOLN	0: PREQ3 has no effect on LDOLN. 1: LDOLN control with PREQ3	R/W	0
6	LDO7	0: PREQ3 has no effect on LDO7. 1: LDO7 control with PREQ3	R/W	0
5	LDO6	0: PREQ3 has no effect on LDO6. 1: LDO6 control with PREQ3	R/W	0
4	LDO5	0: PREQ3 has no effect on LDO5. 1: LDO5 control with PREQ3	R/W	0
3	LDO4	0: PREQ3 has no effect on LDO4. 1: LDO4 control with PREQ3	R/W	0
2	LDO3	0: PREQ3 has no effect on LDO3. 1: LDO3 control with PREQ3	R	0
1	LDO2	0: PREQ3 has no effect on LDO2. 1: LDO2 control with PREQ3	R/W	0
0	LDO1	0: PREQ3 has no effect on LDO1. 1: LDO1 control with PREQ3	R/W	0

2.9.9 PREQ3_RES_ASS_C Register

Table 166. PREQ3_RES_ASS_C

Address	Dec 223, Hex DF		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	VSYSMIN_HI	CLK32KG	CLK32KAUDIO	SYSEN	REGEN2	REGEN1

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	VSYSMIN_HI	0: PREQ3 has no effect on VSYSMIN_HI. 1: VSYSMIN_HI control with PREQ3	R/W	0
4	CLK32KG	0: PREQ3 has no effect on CLK32KG. 1: CLK32KG control with PREQ3	R/W	0
3	CLK32KAUDIO	0: PREQ3 has no effect on CLK32KAUDIO. 1: CLK32KAUDIO control with PREQ3	R/W	0
2	SYSEN	0: PREQ3 has no effect on SYSEN. 1: SYSEN control with PREQ3	R	0
1	REGEN2	0: PREQ3 has no effect on REGEN2. 1: REGEN2 control with PREQ3	R/W	0
0	REGEN1	0: PREQ3 has no effect on REGEN1. 1: REGEN1 control with PREQ3	R/W	0

2.10 PMC Slave Module – Miscellaneous

2.10.1 SMPS_OFFSET Register

Table 167. SMPS_OFFSET

Address	Dec 224, Hex E0		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
OFFSET_R/W	SMPS3	RESERVED	SMPS2	SMPS1	RESERVED	SMPS5	SMPS4

Bits	Field Name	Description	Type	Reset
7	OFFSET_R/W	0: Read only register: SMPS_OFFSET [6:0] 1: Read / Write register: SMPS_OFFSET [6:0] Unlock OFFSET_RW R/W feature through EPROMWhen OFFSET_R/W bit is set to 0, the register cannot be changed anymore (locked).	R/W	EPROM
6	SMPS3	SMPS3 OFFSET	R/W	EPROM
5	RESERVED	Reserved	R	0
4	SMPS2	SMPS2 OFFSET	R/W	EPROM
3	SMPS1	SMPS1 OFFSET	R/W	EPROM
2	RESERVED	Reserved	R	0
1	SMPS5	SMPS5 OFFSET	R/W	EPROM
0	SMPS4	SMPS4 OFFSET	R/W	EPROM

2.10.2 SMPS_MULT Register

Table 168. SMPS_MULT

Address	Dec 227, Hex E3		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
MULT_R/W	SMPS3	TRACK_LDO	SMPS2	SMPS1	RESERVED	SMPS5	SMPS4

Bits	Field Name	Description	Type	Reset
7	MULT_R/W	0: Read only register: SMPS_MULT [6:0] 1: Read / Write register: SMPS_MULT [6:0] Unlock MULT_RW R/W feature through EPROMWhen OFFSET_R/W bit is set to 0, the register cannot be changed anymore (locked).	R/W	0
6	SMPS3	0: SMPS3 output voltage selection code (standard mode) 1: SMPS3 output voltage selection code (extended mode)	R/W	0
5	TRACK_LDO	Enable LDO output voltage trackin SMPS2 output voltage 0: LDO2 not in tracking mode 1: LDO2 is tracking SMPS2	R/W	EPROM
4	SMPS2	0: SMPS2 output voltage selection code (standard mode) 1: SMPS2 output voltage selection code (extended mode)	R/W	0
3	SMPS1	0: SMPS1 output voltage selection code (standard mode) 1: SMPS1 output voltage selection code (extended mode)	R/W	0
2	RESERVED	Reserved	R	0
1	SMPS5	0: SMPS5 output voltage selection code (standard mode) 1: SMPS5 output voltage selection code (extended mode)	R/W	0
0	SMPS4	0: SMPS4 output voltage selection code (standard mode) 1: SMPS4 output voltage selection code (extended mode)	R/W	0

Note:

- Default value is loaded during power-up sequence

2.10.3 MISC1 Register

Table 169. MISC1

Address	Dec 228, Hex E4		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	OSC_BYPASS	OSC_HPMODE	VAC_MEAS	VSYS_MEAS	BB_MEAS

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	OSC_BYPASS	0: Oscillator 32 kHz is using the crystal. 1: Oscillator 32 kHz is bypassed, a square wave is applied on OSC32KIN.	R/W	0
3	OSC_HPMODE	0: Oscillator 32 kHz is configured in normal mode. 1: Oscillator 32 kHz is configured in high-performance mode.	R/W	0
2	VAC_MEAS	Enable the Channel9 divider(11.25/1.25 V) to allow VAC measurement 0: Resistor divider disabled 1: Resistor divider enabled When device is in sleep or off state, this bit is forced to 0 outside of the register.	R/W	0
1	VSYS_MEAS	Enable the Channel7 divider(5/1.25 V or 6.25/1.25 V) to allow system voltage measurement(1) 0: Resistor divider disabled 1: Resistor divider enabled When device is in in sleep or off state, this bit is forced to 0 outside of the register.	R/W	0
0	BB_MEAS	Enable the Channel8 divider(6.25/1.25 V) to allow backup voltage measurement 0: Resistor divider disabled 1: Resistor divider enabled When device is in in sleep or off state, this bit is forced to 0 outside of the register.	R/W	0

(1) Divider value depends on VSYS_SCALER_DIV4 bit value in GPADC_CTRL register

2.10.4 MISC2 Register

Table 170. MISC2

Address	Dec 229, Hex E5		
Physical Address	ID1 = 48h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
SPARE	SPARE	SPARE	LDOUSB_IN_VSYS	LDOUSB_IN_PMID	RESERVED	RESERVED	SEL_VIB

Bits	Field Name	Description	Type	Reset
7	SPARE	Spare	R/W	0
6	SPARE	Spare	R/W	0
5	SPARE	Spare	R/W	0
4	LDOUSB_IN_VSYS	0: VDD_B3 (VSYS) input supply for the LDOUSB regulator is not selected. 1: VDD_B3 (VSYS) input supply for the LDOUSB regulator is selected.	R/W	0
3	LDOUSB_IN_PMID	0: CHRG_PMID (PMID) input supply for the LDOUSB regulator is not selected. 1: CHRG_PMID (PMID) input supply for the LDOUSB regulator is selected.	R/W	0
2	RESERVED	Reserved	R	0
1	RESERVED	Reserved	R	0
0	SEL_VIB	0: LDO3 is configured as a standard power resource. 1: LDO3 is configured as a vibrator.	R/W	0

Notes:

- For the LDOUSB regulator, it is not possible to configure both supply inputs at the same time.
- When MISC2[4:3] = 11 is requested, 00 is written, deselecting all input sources.
- LDOUSB_IN_PMID is opened if an over-voltage detection is present on CHRG_PMID, regardless the LDOUSB_IN_PMID prior setting.
- Setting MISC2[4:3] = 00 when LDOUSB_CFG_STATE is not 0x00 will trig a LDOUSB short circuit detection.

2.10.5 BBSPOR_CFG Register

Table 171. BBSPOR_CFG

Address	Dec 230, Hex E6		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	VRTC_EN_SLP_STS	VRTC_EN_OFF_STS	VRTC_PWEN	BB_CHG_EN	BB_SEL_1	BB_SEL_0	RESERVED

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	VRTC_EN_SLP_STS	0: VRTC is configured in the standard power mode configuration when all processors are in SLP state (biasing also in SLP state). 1: VRTC is configured in a low-power mode(VBRTC) configuration when all processors are in SLP state (biasing also in SLP state).	R/W	1
5	VRTC_EN_OFF_STS	0: VRTC is configured in the standard power mode configuration when all processors are in OFF state (biasing also in OFF state). 1: VRTC is configured in a low-power mode(VBRTC) configuration when all processors are in OFF state (biasing also in OFF state).	R/W	0
4	VRTC_PWEN	0: VRTC is configured in a low-power mode(VBRTC) configuration. 1: VRTC state depends on BBSPOR_CFG[6:5]	R/W/S	1
3	BB_CHG_EN	0: The backup battery charge is disabled. 1: The backup battery charge is enabled.	R/W	0
2	BB_SEL_1	Back-up battery end-of-charge voltage selection: 00: 3.0 V 01: 2.5 V 10: 3.15 V 11: VSYS	R/W	0
1	BB_SEL_0		R/W	1
0	RESERVED	Reserved	R	0

Notes:

- VRTC/VBRTC selection is described inTable 172:

Table 172. BBSPOR_CFG VRTC/VBRTC Selection

BBSPOR_CFG REGISTER BIT CONFIGURATION			ACTIVE MODE	SLLEP MODE	WAIT-ON MODE	BACKUP MODE
VRTC_PWEN	VRTC_EN_OFF_STS	VRTC_EN_SLP_STS	SEL	SEL	SEL	SEL
0	X	X	VBRTC	VBRTC	VBRTC	VBRTC
1	0	0	VRTC	VRTC	VRTC	VBRTC
1	0	1	VRTC	VBRTC	VRTC	VBRTC
1	1	0	VRTC	VRTC	VBRTC	VBRTC
1	1	1	VRTC	VBRTC	VBRTC	VBRTC

2.10.6 TMP_CFG Register

Table 173. TMP_CFG

Address	Dec 231, Hex E7		
Physical Address	ID1 = 48h	**Instance**	Config Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	THERM_HD	RESERVED	RESERVED	THERM_HD_SEL_1	THERM_HD_SEL_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	THERM_HD	Hot-die detection output: 0: The hot-die threshold is not reached. 1: The hot-die threshold is reached.	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	THERM_HD_SEL_1	Temperature selection for the hot-die detection(Rising / Falling temperature): 00: 117 / 108 °C 01: 121 / 112 °C 10: 125 / 116 °C 11: 130 / 120 °C	R/W	1
0	THERM_HD_SEL_0		R/W	1

Note:

- Two temperature sensors are instantiated in the Phoenix device. Both temperature sensors are driven together by the same register. To prevent glitches, the Hot-Die and Thermal Shutdown outputs are masked when the temperature sensors are turned on, for a minimum time of 240 µs.

2.11 Battery Charging Controller and Indicator LED

2.11.1 CONTROLLER_CTRL2 Register

Table 174. CONTROLLER_CTRL2

Address	Dec 218, Hex DA		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	VSYS_PC2	VSELSUPPCOMP2	VSELSUPPCOMP1	VSYS_PC	LINCH_DLY	EN_DPPM	SUP_MASK

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	VSYS_PC2	In trickle charge VSYS level is given by: VSYS_PC = '0' AND VSYS_PC2 = '0' --> 3.6V VSYS_PC = '1' AND VSYS_PC2 = '0' --> 3.8V VSYS_PC = '0' AND VSYS_PC2 = '1' --> 4V VSYS_PC = '1' AND VSYS_PC2 = '1' --> 4.2V	R/W	EPROM
5	VSELSUPPCOMP2	Supplement comparator threshold selection:(1) 00:20mV 01:30mV (Default) 10:40mV 11:50mV	R/W	0
4	VSELSUPPCOMP1		R/W	1
3	VSYS_PC	VSYS voltage selction in precharge: 0: 3.6 V 1: 3.8 V	R/W	EPROM
2	LINCH_DLY	0: Linear charge directly control by supplement comparator 1: Linear charge control 2 clock cycles after supplement mode goes low.	R/W	0
1	EN_DPPM	0: DPPM disable 1: DPPM enable	R/W	1
0	SUP_MASK	0: Supplement/current comparator disable 1: Supplement/current comparator unmasked	R/W	1

(1) If VBAT-VSYS>VSELSUPPCOMP,supplement mode is enabled

2.11.2 CONTROLLER_VSEL_COMP Register

Table 175. CONTROLLER_VSEL_COMP

Address	Dec 219, Hex DB		
Physical Address	ID2 = 49h	**Instance**	Charger Domain Charging group reset domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	DLIN_2	DLIN_1	VBATFULL_CHRG_3	VBATFULL_CHRG_2	VBATFULL_CHRG_1	VBATSHORT_2	VBATSHORT_1

Bits	Field Name	Description	Type	Reset	
				Charger Domain	Charging group reset domain
7	RESSERVED	Reserved	R	0	0
6	DLIN_2	Vbat tracking reference selection: DLIN[1:0] = 00 = 50 mV DLIN[1:0] = 01 = 100 mV DLIN[1:0] = 10 = 150 mV DLIN[1:0] = 11 = 200 mV	R/W	EPROM	EPROM
5	DLIN_1		R/W	EPROM	EPROM
4	VBATFULL_CHRG_3	Vbat full charge comparator threshold: VBAT_FULL_CHRG[2:0] = 000 = 2.65 V VBAT_FULL_CHRG[2:0] = 001 = 2.75 V VBAT_FULL_CHRG[2:0] = 010 = 2.85 V VBAT_FULL_CHRG[2:0] = 011 = 2.95 V VBAT_FULL_CHRG[2:0] = 100 = 3.05 V VBAT_FULL_CHRG[2:0] = 101 = 3.15 V VBAT_FULL_CHRG[2:0] = 110 = 3.25 V VBAT_FULL_CHRG[2:0] = 111 = 3.35 V	R/W	EPROM	EPROM
3	VBATFULL_CHRG_2		R/W	EPROM	EPROM
2	VBATFULL_CHRG_1		R/W	EPROM	EPROM
1	VBATSHORT_2	VBAT short threshold: VBAT_SHORT[1:0] = 00 = 2.1 V VBAT_SHORT[1:0] = 01 = 2.45 V VBAT_SHORT[1:0] = 10 = 2.8 V VBAT_SHORT[1:0] = 11 = 2.8 V	R/W	EPROM	EPROM
0	VBATSHORT_1		R/W	EPROM	EPROM

2.11.3 CHARGERUSB_VSYSREG Register

Table 176. CHARGERUSB_VSYSREG

Address	Dec 220, Hex DC		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
VSYS_SW_CTRL	RESERVED	VSYSREG_5	VSYSREG _4	VSYSREG _3	VSYSREG _2	VSYSREG _1	VSYSREG _0

Bits	Field Name	Description		Type	Reset
7	VSYS_SW_CTRL	VSYS software xontrol 0: VSYS = 3.6/3.8 V according to EPROM bit VSYS_PC 1: VSYS = VYSREG, VBAT tracking disable in full charge)		R/W	0
6	RESERVED	Reserved		R	0
5	VSYSREG_5	System supply/battery regulation voltage: 000000: 3.50 V 000001: 3.52 V 000010: 3.54 V (default) 000011: 3.56 V 000100: 3.58 V	100000: 4.14 V 100001: 4.16 V 100010: 4.18 V 100011: 4.20 V 100100: 4.22 V	R/W	0
4	VSYSREG_4	000101: 3.60 V 000110: 3.62 V 000111: 3.64 V 001000: 3.66 V 001001: 3.68 V	100101: 4.24 V 100110: 4.26 V 100111: 4.28 V 101000: 4.30 V 101001: 4.32 V	R/W	0
3	VSYSREG_3	001010: 3.70 V 001011: 3.72 V 001100: 3.74 V 001101: 3.76 V 001110: 3.78 V	101010: 4.34 V 101011: 4.36 V 101100: 4.38 V 101101: 4.40 V 101110: 4.42 V	R/W	0
2	VSYSREG_2	001111: 3.80 V 010000: 3.82 V 010001: 3.84 V 010010: 3.86 V 010011: 3.88 V	101111: 4.44 V 110000: 4.46 V 110001: 4.48 V 110010: 4.50 V 110011: 4.52 V	R/W	0
1	VSYSREG_1	010100: 3.90 V 010101: 3.92 V 010110: 3.94 V 010111: 3.96 V 011000: 3.98 V	110100: 4.54 V 110101: 4.56 V 110110: 4.58 V 110111: 4.60 V 111000: 4.62 V	R/W	1

Bits	Field Name	Description		Type	Reset
0	VSYSREG_0	011001: 4.00 V 011010: 4.02 V 011011: 4.04 V 011100: 4.06 V 011101: 4.08 V 011110: 4.10 V 011111: 4.12 V	111001: 4.64 V 111010: 4.66 V 111011: 4.68 V 111100: 4.70 V 111101: 4.72 V 111110: 4.74 V 111111: 4.76 V	R/W	0

2.11.4 CHARGERUSB_VICHRG_PC Register

Table 177. CHARGERUSB_VICHRG_PC

Address	Dec 221, Hex DD		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VICHRG_1	VICHRG_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	VICHRG_1	Charge current in precharge mode (default EPROM) 0000: 100 mA 0001: 200 mA 0010: 300 mA 0011: 400 mA	R/W	EPROM
0	VICHRG_0	when POP = 0 and AUTOCHARGE = 1 0000: 300 mA 0001: 350 mA 0010: 400 mA 0011: 450 mA	R/W	EPROM

NOTE: The VICHRG value is valid only if the sense resistor is 68 mΩ when POP_APPSCH = 0 and 20 mΩ when POP_APPSCH = 1.

If POP_APPSCH = 1, a 15-mΩ sense resistor is used; the value is multiplied by 20/15.

2.11.5 LINEAR_CHRG_STS Register

Table 178. LINEAR_CHRG_STS

Address	Dec 222, Hex DE		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	CRYSTAL_OSC_OK	END_OF_CHARGE	VBATOV	VSYSOV	DPPM_STS	CV_STS	CC_STS

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	CRYSTAL_OSC_OK	Crystal oscillator present	R	0
5	END_OF_CHARGE	End of chage	R	0
4	VBATOV	VBAT over voltage: VBAT rise above 117% above VOREG	R	0
3	VSYSOV	VSYS over voltage VSYS rise above 133% above VOREG	R	0
2	DPPM_STS	DPPM status: Charging current is lowered to avoid VSYS node to collapse	R	0
1	CV_STS	Constant Voltage charge in progress	R	0
0	CC_STS	Constant current charge in progress	R	0

2.11.6 CONTROLLER_INT_MASK Register

Table 179. CONTROLLER_INT_MASK

Address	Dec 224, Hex E0		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
MVAC_FAULT	MVAC_EOC	MLINCH_GATED	MBAT_REMOVED	MFAULT_WDG	MBAT_TEMP	MVBUS_DET	MVAC_DET

Bits	Field Name	Description	Type	Reset
7	MVAC_FAULT	Mask interrupt 21(EXT_CHRG) generation on an external charger fault(pulse on CHRG_EXTCHRG _STATZ pin) 0: Unmasked 1: Masked	R/W	0
6	MVAC_EOC	Mask interrupt 21(EXT_CHRG) generation on an external charger End Of Charge request (CHRG_EXTCHRG _STATZ pin release) 0: Unmasked 1: Masked	R/W	0
5	MLINCH_GATED	Mask interupt generation on LINCH_GATED event (CONTROLLER_STAT1[6]). 0: Unmasked 1: Masked	R	0
4	MBAT_REMOVED	Mask interupt generation on BAT_REMOVED event (CONTROLLER_STAT1[1]). 0: Unmasked 1: Masked	R/W	0
3	MFAULT_WDG	Mask interupt generation on FAULT_WDG event (CONTROLLER_STAT1[4]). 0: Unmasked 1: Masked	R/W	0
2	MBAT_TEMP	Mask interupt generation on BAT_TEMP_OVRANGE event (CONTROLLER_STAT1[0]). 0: Unmasked 1: Masked	R/W	0
1	MVBUS_DET	Mask interupt generation on VBUS_DETevent (CONTROLLER_STAT1[2]). 0: Unmasked 1: Masked	R/W	0
0	MVAC_DET	Mask interupt generation on VAC_DET event (CONTROLLER_STAT1[3]). 0: Unmasked 1: Masked	R/W	0

2.11.7 CONTROLLER_CTRL1 Register

Table 180. CONTROLLER_CTRL1

Address	Dec 225, Hex E1		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	EN_LINCH	EN_CHARGER	SEL_CHARGER	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	EN_LINCH	0 : Linear charge disable 1 : Linear charge enable if EN_CHARGER = 1.	R/W	0
4	EN_CHARGER	0: Charge is disabled (default). 1: Charger is enabled.	R/W	0
3	SEL_CHARGER	0: VBUS input supply path is selected (default). 1: VAC input supply path is selected.	R/W	0
2	RESERVED	Reserved	R	0
1	RESERVED	Reserved	R	0
0	RESERVED	Reserved	R	0

Note:

- EN_LINCH is used only if OTP bit POP_APPSCH = 1. This bit enables the control of the external Power Path FET regulating the charging current.
- If POP_APPSCH = 0 and the charger source is VBUS, EN_CHARGER directly controls the charger enable.
- If POP_APPSCH = 1 and the charger source is VBUS, EN_CHARGER controls the switched-mode system supply regulator.
- If charge has been started by hardware, registers are not updated and return 0 even if charge is ongoing.
- If the charger source is VAC, EN_CHARGER controls the CHRG_EXTCHRG_ENZ pin (inverted).

2.11.8 CONTROLLER_WDG Register

Table 181. CONTROLLER_WDG

Address	Dec 226, Hex E2		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
WDG_RST	WDT_6	WDT_5	WDT_4	WDT_3	WDT_2	WDT_1	WDT_0

Bits	Field Name	Description	Type	Reset
7	WDG_RST	0: No effect on the charging watchdog timer. 1: Reset the charging watchdog timer.	R/W	0
6	WDT_6	Software mode charging watchdog time value, from 0 to 127 seconds, with a 1-second step. Descriptions: 0000000: 0 s >> *Stop charging go to Watchdog Fault* 0000001: 1 s 0000010: 2 s 0000011: 3 s ... 0011111: 31 s 0100000: 32 s (default) 0100001: 33 s ... 1111111: 127 s (2 mn)	R/W	0
5	WDT_5		R/W	1
4	WDT_4		R/W	0
3	WDT_3		R/W	0
2	WDT_2		R/W	0
1	WDT_1		R/W	0
0	WDT_0		R/W	0

Note:

- Once the value is programmed, the watchdog is reset with the new value and restarts automatically (in software mode only). The watchdog monitors only the charging, not the VBUS OTG supply.

2.11.9 CONTROLLER_STAT1 Register

Table 182. CONTROLLER_STAT1

Address	Dec 227, Hex E3		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
CHRG_EXTCHRG_STATZ	LINCH_GATED	CHRG_DET_N	FAULT_WDG	VAC_DET	VBUS_DET	BAT_REMOVED	BAT_TEMP_OVRANGE

Bits	Field Name	Description	Type	Reset
7	CHRG_EXTCHRG_STATZ	0: CHRG_EXTCHRG_STATZ line is 0. 1: CHRG_EXTCHRG_STATZ line is 1. Falling and rising edge detection,triggers interrupt 21: EXT_CHRG	R	0
6	LINCH_GATED	0: Linear charge not gated 1: Linear charge gated. Triggers interrupt 20: CHRG_CTRL	R	0
5	CHRG_DET_N	0: CHRG_DET_N line is 0. 1: CHRG_DET_N line is 1. Does not generate an interrupt.	R	0
4	FAULT_WDG	0: No fault has occurred. 1: Watchdog fault is active. Rising edge detection, triggers interrupt 20: CHRG_CTRL	R	0
3	VAC_DET	0: VAC is not present. 1: VAC is present. Falling and rising edge detection, triggers interrupt 20: CHRG_CTRL	R	0
2	VBUS_DET	0: VBUS is not present. 1: VBUS is present. Falling and rising edge detection, triggers interrupt 20: CHRG_CTRL	R	0
1	BAT_REMOVED	0: Battery is not removed. 1: Battery has been removed. Detection is based on GPADC_IN0. Falling and rising edge detection, triggers interrupt 20: CHRG_CTRL	R	0
0	BAT_TEMP_OVRANGE	0: Battery temperature measurement is within valid range(1). 1: Battery temperature measurement is out of range. Falling and rising edge detection, triggers interrupt 20: CHRG_CTRL	R	0

(1) Valid range is defined by RATIO_TLO and RATIO_THI in GPADC_TRIM17 and GPADC_TRIM18 registers

Note:

- For the end user, the CHRG_EXTCHRG_STATZ bit is 1 by default, when no charger is attached.

2.11.10 CHARGERUSB_INT_STATUS Register

Table 183. CHARGERUSB_INT_STATUS

Address	Dec 228, Hex E4		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description	Interrupt trigged by this register is interrupt 22: INT_CHRG		
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	EN_LINCH	CURRENT_TERM	CHARGERUSB_STAT	CHARGERUSB_THMREG	CHARGERUSB_FAULT

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	EN_LINCH	0: No new event present 1: Linear charge has started Unmasked by default	R	0
3	CURRENT_TERM	0: VBUS charger current termination is not reached. 1: VBUS charger current termination has been reached. Unmasked by default	R	0
2	CHARGERUSB_STAT	Set to logical 1 when CHARGERUSB_STATUS_INT2 [3:0] value change Unmasked by default.	R	0
1	CHARGERUSB_THMREG	Set to logical 1 when CHARGERUSB_STATUS_INT1 [7] value change Unmasked by default.	R	0
0	CHARGERUSB_FAULT	Set to logical 1 when CHARGERUSB_STATUS_INT1 [6:0] value change Unmasked by default.	R	0

Note:

- All the bits in the register are cleared on read.

2.11.11 CHARGERUSB_INT_MASK Register

Table 184. CHARGERUSB_INT_MASK

Address	Dec 229, Hex E5		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	MEN_LINCH	MCURRENT_TERM	MCHARGERUSB_STAT	MCHARGERUSB_THMREG	MCHARGERUSB_FAULT

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	MEN_LINCH	Mask EN_LINCH interrupt 0: Unmasked 1: Masked	R/W	0
3	MCURRENT_TERM	Mask CURRENT_TERM interrupt 0: Unmasked 1: Masked	R/W	0
2	MCHARGERUSB_STAT	Mask CHARGERUSB_STAT interrupt 0: Unmasked 1: Masked	R/W	0
1	MCHARGERUSB_THMREG	Mask CHARGERUSB_THMREG interrupt 0: Unmasked 1: Masked	R/W	0
0	MCHARGERUSB_FAULT	Mask CHARGERUSB_FAULT interrupt 0: Unmasked 1: Masked	R/W	0

2.11.12 CHARGERUSB_STATUS_INT1 Register

Table 185. CHARGERUSB_STATUS_INT1

Address	Dec 230, Hex E6		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
TMREG	NO_BAT	BST_OCP	TH_SHUTD	BAT_OVP	POOR_SRC	SLP_MODE	VBUS_OVP

Bits	Field Name	Description	Type	Reset
7	TMREG	0: Thermal regulation is not activated. 1: Thermal regulation is on-going. Affects CHARGERUSB_THMREG bit in CHARGERUSB_INT_STATUS.	R	0
6	NO_BAT	0: Battery is present. 1: No battery is currently present. The detection is based on USB charger IP, disabled by default by EPROM bit POP_APPSCH. Affects CHARGERUSB_FAULT bit in CHARGERUSB_INT_STATUS	R	0
5	BST_OCP	0: No over current protection on-going on the boost 1: Boost over current load Affects CHARGERUSB_FAULT bit in CHARGERUSB_INT_STATUS.	R	0
4	TH_SHUTD	0: Charger normal temperature 1: Charger thermal shutdown occurred Affects CHARGERUSB_FAULT bit in CHARGERUSB_INT_STATUS.	R	0
3	BAT_OVP	0: Standard conditions 1: Battery over voltage Affects CHARGERUSB_FAULT bit in CHARGERUSB_INT_STATUS.	R	0
2	POOR_SRC	0: Satisfying input source 1: Poor input source Affects CHARGERUSB_FAULT bit in CHARGERUSB_INT_STATUS.	R	0
1	SLP_MODE	0: Normal mode 1: Sleep mode (VBAT ≥ VBUS in charger mode) Affects CHARGERUSB_FAULT bit in CHARGERUSB_INT_STATUS.	R	0
0	VBUS_OVP	0: Standard conditions 1: VBUS over voltage Affects CHARGERUSB_FAULT bit in CHARGERUSB_INT_STATUS.	R	0

Note:

- All register bits work on level.

2.11.13 CHARGERUSB_STATUS_INT2 Register

Table 186. CHARGERUSB_STATUS_INT2

Address	Dec 231, Hex E7		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	ICCLOOP	CURRENT_TERM	CHARGE_DONE	ANTICOLLAPSE

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	ICCLOOP	0: Input current (VBUS), control loop is inactive 1: Input current (VBUS), control loop is acting	R	0
2	CURRENT_TERM	0: Current termination mode has not occurred. 1: Current termination mode has occurred. Affects CURRENT_TERM bit in CHARGERUSB_INT_STATUS.	R	0
1	CHARGE_DONE	0: All other states 1: Reached CHARGE_DONE state Affects CHARGERUSB_STAT bit in CHARGERUSB_INT_STATUS.	R	0
0	ANTICOLLAPSE	0: Anticollapse feature is currently not activated. 1: Anticollapse feature is currently activated. Affects CHARGERUSB_STAT bit in CHARGERUSB_INT_STATUS.	R	0

2.11.14 CHARGERUSB_CTRL1 Register

Table 187. CHARGERUSB_CTRL1

Address	Dec 232, Hex E8		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
SUSPEND_BOOT	OPA_MODE	HZ_MODE	TERM	RESERVED	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7	SUSPEND_BOOT	0: No effect 1: Suspend boot is gating the USB charge.System regulator is kept ON	R/W	0
6	OPA_MODE	Control the charger's DCDC converter mode 0: Charger mode, the charge is authorized. 1: Boost mode for OTG purpose, hardware protection is set to forbid the charge.	R/W	0
5	HZ_MODE	0: USB charger is not in high-impedance mode on VBUS (default). 1: USB charger is in high-impedance mode.	R/W	0
4	TERM	0: Disable charge current termination (default). 1: Enable charge current termination.	R/W	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	RESERVED	Reserved	R	0
0	RESERVED	Reserved	R	0

2.11.15 CHARGERUSB_CTRL2 Register

Table 188. CHARGERUSB_CTRL2

Address	Dec 233, Hex E9		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
VITERM_2	VITERM_1	VITERM_0	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7	VITERM_2	Termination current level: 000: 50 mA 001: 100 mA (default) 010: 150 mA 011: 200 mA 100: 250 mA 101: 300 mA 110: 350 mA 111: 400 mA	R/W	EPROM
6	VITERM_1		R/W	EPROM
5	VITERM_0		R/W	EPROM
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	RESERVED	Reserved	R	0
0	RESERVED	Reserved	R	0

Note:

- The charging is terminated if the charging current during CV charging decreases to the termination current programmed level and the termination is enabled.
- VITERM value is Valid only if sense resitor is 68mΩ when POP_APPSCH=0 and 20mΩ when POP_APPSCH=1
- If POP_APPSCH=1 an 15mΩ sense resistor is used, value is multiplied by 20/15

2.11.16 CHARGERUSB_CTRL3 Register

Table 189. CHARGERUSB_CTRL3

Address	Dec 234, Hex EA		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type			

7	6	5	4	3	2	1	0
VBUSCHRG_LDO_OVRD	CHARGE_ONCE	BST_HW_PR_DIS	GSMCAL_PRESET / RESERVED	AUTOSUPPLY	GSMCAL_TM	BUCK_HSILIM_3A	BUCK_HSILIM

Bits	Field Name	Description	Type	Reset
7	VBUSCHRG_LDO_OVRD	0: No effect (FSM control) (default) 1: Force the LDOUSB LDO to turn on (no effect if charger is in Hi-Z mode).	R/W	0
6	CHARGE_ONCE	0: Charge once feature is disabled. 1: Charge once feature is turned on (automatic end of charge is enabled and the USB charge will stop once it reaches the end of the charge).	R/W	0
5	BST_HW_PR_DIS	ID line must be grounded to set the charger DC-DC converter in boost mode. Once started, boost can automatically be stopped if ID ground condition is not maintained. 0: Boost is automatically stopped. 1: Boost stays ON. On ES1.2, BST_HW_PR_DIS has a second functionality when GSMCALL_TM = 1: 0: VSYS overvoltage comparator enabled 1: VSYS overvoltage comparator disabled	R/W	0
4	RESERVED/ GSMCAL_PRESET	ES1.1: Reserved ES1.2: 0: No effect 1: Force the switched-mode system supply regulator in continuous mode for factory test mode	ES1.1: R ES1.2: R/W	0
3	AUTOSUPPLY	0: Q1 is not forced. 1: Q1 is disabled (Q1 blocking FET affects only the boost). Setting bit to 1 allows 5-V generation to the CHRG_PMID pin without connecting the voltage to VBUS line. This allows to generate supply for USB LDO without delivering VBUS.	R/W	0
2	GSMCAL_TM	Enable production test mode for GSM calibration in factory	R/W	0
1	BUCK_HSILIM_3A	Change cycle by cycle current limit for buck regulator (Must be configured to "0" only for factory GSM calibration).	R/W	1
0	BUCK_HSILIM	Set Q2 and Q3 current limit when in charging mode: With BUCK_HSILIM_3A set to 1 0: 2.55 A 1: 1.90 A With BUCK_HSILIM_3A set to 0 0: 3.7 A 1: 3.15 A	R/W	0

2.11.17 CHARGERUSB_VOREG Register

Table 190. CHARGERUSB_VOREG

Address	Dec 236, Hex EC		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	VOREG_5	VOREG_4	VOREG_3	VOREG_2	VOREG_1	VOREG_0

Bits	Field Name	Description		Type	Reset
7	RESERVED	Reserved		R	0
6	RESERVED	Reserved		R	0
5	VOREG_5	System supply/battery regulation voltage: 000000: 3.50 V 000001: 3.52 V 000010: 3.54 V (default) 000011: 3.56 V 000100: 3.58 V	100000: 4.14 V 100001: 4.16 V 100010: 4.18 V 100011: 4.20 V 100100: 4.22 V	R/W	EPROM
4	VOREG_4	000101: 3.60 V 000110: 3.62 V 000111: 3.64 V 001000: 3.66 V 001001: 3.68 V	100101: 4.24 V 100110: 4.26 V 100111: 4.28 V 101000: 4.30 V 101001: 4.32 V	R/W	EPROM
3	VOREG_3	001010: 3.70 V 001011: 3.72 V 001100: 3.74 V 001101: 3.76 V 001110: 3.78 V	101010: 4.34 V 101011: 4.36 V 101100: 4.38 V 101101: 4.40 V 101110: 4.42 V	R/W	EPROM
2	VOREG_2	001111: 3.80 V 010000: 3.82 V 010001: 3.84 V 010010: 3.86 V 010011: 3.88 V	101111: 4.44 V 110000: 4.46 V 110001: 4.48 V 110010: 4.50 V 110011: 4.52 V	R/W	EPROM
1	VOREG_1	010100: 3.90 V 010101: 3.92 V 010110: 3.94 V 010111: 3.96 V 011000: 3.98 V	110100: 4.54 V 110101: 4.56 V 110110: 4.58 V 110111: 4.60 V 111000: 4.62 V	R/W	EPROM
0	VOREG_0	011001: 4.00 V 011010: 4.02 V 011011: 4.04 V 011100: 4.06 V 011101: 4.08 V 011110: 4.10 V 011111: 4.12 V	111001: 4.64 V 111010: 4.66 V 111011: 4.68 V 111100: 4.70 V 111101: 4.72 V 111110: 4.74 V 111111: 4.76 V	R/W	EPROM

2.11.18 CHARGERUSB_VICHRG Register

Table 191. CHARGERUSB_VICHRG

Address	Dec 237, Hex ED		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	VICHRG_3	VICHRG_2	VICHRG_1	VICHRG_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	VICHRG_3	Charge current in full charge mode (default EPROM): POP = 0 (compliant with Phoenix): 0000: 300 mA 0001: 350 mA 0010: 400 mA 0011: 450 mA POP = 1: 0000: 100 mA 0001: 200 mA 0010: 300 mA 0011: 400 mA	R/W	EPROM
2	VICHRG_2	0100: 500 mA 0101: 600 mA 0110: 700 mA 0111: 800 mA 0100: 500 mA 0101: 600 mA 0110: 700 mA 0111: 800 mA	R/W	EPROM
1	VICHRG_1	1000: 900 mA 1001: 1000 mA 1010: 1100 mA 1011: 1200 mA 1000: 900 mA 1001: 1000 mA 1010: 1100 mA 1011: 1200 mA	R/W	EPROM
0	VICHRG_0	1100: 1300 mA 1101: 1400 mA 1110: 1500 mA 1111: 300 mA 1100: 1300 mA 1101: 1400 mA 1110: 1500 mA 1111: 300 mA	R/W	EPROM

NOTE: VICHRG value is Valid only if sense resitor is 68mΩ when POP_APPSCH=0 and 20mΩ when POP_APPSCH=1

If POP_APPSCH=1 an 15mΩ sense resistor is used, value is multiplied by 20/15

2.11.19 CHARGERUSB_CINLIMIT Register

Table 192. CHARGERUSB_CINLIMIT

Address	Dec 238, Hex EE		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	CIN_LIMIT_5	CIN_LIMIT_4	CIN_LIMIT_3	CIN_LIMIT_2	CIN_LIMIT_1	CIN_LIMIT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	CIN_LIMIT_5	Current limitation value on VBUS input: 000000: 50 mA 000001: 100 mA 000010: 150 mA 000011: 200 mA 000100: 250 mA 000101: 300 mA	R/W	EPROM
4	CIN_LIMIT_4	000110: 350 mA 000111: 400 mA 001000: 450 mA 001001: 500 mA 001010: 550 mA	R/W	EPROM
3	CIN_LIMIT_3	001011: 600 mA 001100: 650 mA 001101: 700 mA 001110: 750 mA 100111: 800 mA	R/W	EPROM
2	CIN_LIMIT_2	110111: 850 mA 101000: 900 mA 111000: 950 mA 101001: 1000 mA 111001: 1050 mA	R/W	EPROM
1	CIN_LIMIT_1	101010: 1100 mA 111010: 1150 mA 101011: 1200 mA 111011: 1250 mA 101100: 1300 mA	R/W	EPROM
0	CIN_LIMIT_0	111100: 1350 mA 101101: 1400 mA 111101: 1450 mA 101110: 1500 mA 100000: 1800mA 100001: 2100mA 100010: 2250mA XX1111: No input current limit	R/W	EPROM

2.11.20 CHARGERUSB_CTRLLIMIT1 Register

Table 193. CHARGERUSB_CTRLLIMIT1

Address	Dec 239, Hex EF		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	VOREGL_5	VOREGL_4	VOREGL_3	VOREGL_2	VOREGL_1	VOREGL_0

Bits	Field Name	Description		Type	Reset
7	RESERVED	Reserved		R	0
6	RESERVED	Reserved		R	0
5	VOREGL_5	System supply/battery regulation voltage limit: 000000: 3.50 V 000001: 3.52 V 000010: 3.54 V 000011: 3.56 V 000100: 3.58 V	100000: 4.14 V 100001: 4.16 V (default) 100010: 4.18 V 100011: 4.20 V 100100: 4.22 V	R/W	EPROM
4	VOREGL_4	000101: 3.60 V 000110: 3.62 V 000111: 3.64 V 001000: 3.66 V 001001: 3.68 V	100101: 4.24 V 100110: 4.26 V 100111: 4.28 V 101000: 4.30 V 101001: 4.32 V	R/W	EPROM
3	VOREGL_3	001010: 3.70 V 001011: 3.72 V 001100: 3.74 V 001101: 3.76 V 001110: 3.78 V	101010: 4.34 V 101011: 4.36 V 101100: 4.38 V 101101: 4.40 V 101110: 4.42 V	R/W	EPROM
2	VOREGL_2	001111: 3.80 V 010000: 3.82 V 010001: 3.84 V 010010: 3.86 V 010011: 3.88 V	101111: 4.44 V 110000: 4.46 V 110001: 4.48 V 110010: 4.50 V 110011: 4.52 V	R/W	EPROM
1	VOREGL_1	010100: 3.90 V 010101: 3.92 V 010110: 3.94 V 010111: 3.96 V 011000: 3.98 V	110100: 4.54 V 110101: 4.56 V 110110: 4.58 V 110111: 4.60 V 111000: 4.62 V	R/W	EPROM
0	VOREGL_0	011001: 4.00 V 011010: 4.02 V 011011: 4.04 V 011100: 4.06 V 011101: 4.08 V 011110: 4.10 V 011111: 4.12 V	111001: 4.64 V 111010: 4.66 V 111011: 4.68 V 111100: 4.70 V 111101: 4.72 V 111110: 4.74 V 111111: 4.76 V	R/W	EPROM

Note:

- The VOREGL register bits can be locked by software only once (write access only), see register CHARGERUSB_CTRLLIMIT2 LOCK_LIMIT bit.

2.11.21 CHARGERUSB_CTRLLIMIT2 Register

Table 194. CHARGERUSB_CTRLLIMIT2

Address	Dec 240, Hex F0		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	LOCK_LIMIT	VICHRGL_3	VICHRGL_2	VICHRGL_1	VICHRGL_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	LOCK_LIMIT	Bit register to lock the value on the register bits VICHRGL [3:0], VOREGL [5:0]: 0: VOREGL and VICHRGL are readable and writable. 1: VOREGL and VICHRGL are read only. LOCK_LIMIT bit is writable only once. To unlock the register bit, a NRESPWRON reset must be performed.	R/W	0
3	VICHRGL_3	Charge current limit: 0000: 100 mA 0001: 200 mA 0010: 300 mA 0011: 400 mA	R/W	EPROM
2	VICHRGL_2	0100: 500 mA 0101: 600 mA 0110: 700 mA 0111: 800 mA	R/W	EPROM
1	VICHRGL_1	1000: 900 mA (default) 1001: 1000 mA 1010: 1100 mA 1011: 1200 mA	R/W	EPROM
0	VICHRGL_0	1100: 1300 mA 1101: 1400 mA 1110: 1500 mA 1111: 1500 mA	R/W	EPROM

Note:

- The VICHRGL register bits can be locked by software only once (write access only), see register CHARGERUSB_CTRLLIMIT2 LOCK_LIMIT bit.
- VICHRGL value is Valid only if sense resitor is 68mΩ when POP_APPSCH=0 and 20mΩ when POP_APPSCH=1
- If POP_APPSCH=1 an 15mΩ sense resistor is used, value is multiplied by 20/15

2.11.22 ANTICOLLAPSE_CTRL1 Register

Table 195. ANTICOLLAPSE_CTRL1

Address	Dec 241, Hex F1		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
BUCK_VTH_2	BUCK_VTH_1	BUCK_VTH_0	RESERVED	RESERVED	ANTICOLL_ANA	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7	BUCK_VTH_2	Anticollapse threshold value: 000: 4.20 V 001: 4.28 V 010: 4.36 V 011: 4.44 V 100: 4.52 V 101: 4.60 V 110: 4.68 V 111: 4.76 V	R/W	0
6	BUCK_VTH_1		R/W	ES1.1: 0 ES1.2: 1
5	BUCK_VTH_0		R/W	ES1.1: 0 ES1.2: 1
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	ANTICOLL_ANA	0: Disable anticollapse loop 1: Enable anticollapse loop When enabled, if VBUS collapses below BUCK_VTH, the system current is automatically reduced to a value keeping the input voltage higher than preset value BUCK_VTH [2:0].	R/W	EPROM
1	RESERVED	Reserved	R/W	EPROM
0	RESERVED	Reserved	R	0

2.11.23 LED_PWM_CTRL1 Register

Table 196. LED_PWM_CTRL1

Address	Dec 244, Hex F4		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
PWM_VAL_7	PWM_VAL_6	PWM_VAL_5	PWM_VAL_4	PWM_VAL_3	PWM_VAL_2	PWM_VAL_1	PWM_VAL_0

Bits	Field Name	Description	Type	Reset
7	PWM_VAL_7	Set the value of the PWM duty cycle: 00000000: 1/256 00000001: 2/256 ... 11111110: 255/256 11111111: 256/256 (always on) (default)	R/W	1
6	PWM_VAL_6		R/W	1
5	PWM_VAL_5		R/W	1
4	PWM_VAL_4		R/W	1
3	PWM_VAL_3		R/W	1
2	PWM_VAL_2		R/W	1
1	PWM_VAL_1		R/W	1
0	PWM_VAL_0		R/W	1

Note:

- Dimming is done with a 128-Hz PWM signal which has 255 linear steps .

2.11.24 LED_PWM_CTRL2 Register

Table 197. LED_PWM_CTRL2

Address	Dec 245, Hex F5		
Physical Address	ID2 = 49h	**Instance**	Charger Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	DIS_PULLDOWN	CURR_LED_1	CURR_LED_0	LED_IN_1	LED_IN_0	LED_MODE_1	LED_MODE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	DIS_PULLDOWN	0: LED output pulldown enabled when module is disabled (default). 1: LED output pulldown disabled.	R/W	0
5	CURR_LED_1	LED current control: 00: 0 mA 01: 1 mA 10: 2.5 mA (default) 11: 5 mA	R/W	1
4	CURR_LED_0		R/W	0
3	LED_IN_1	When LED_MODE [1:0] = 01: 00: VBUS input source (default) 01: VAC input source 10: EXTPIN input source 11: VBUS input source	R/W	0
2	LED_IN_0		R/W	0
1	LED_MODE_1	00: LED driver controlled by charging modes (default). 01: LED driver enabled (independent of charging modes). 10: LED driver disabled totally (independent of charging modes). Current consumption is minimized. 11: LED driver controlled by charging modes.	R/W	0
0	LED_MODE_0		R/W	0

2.12 USB On-The-Go

USB registers have four columns to associate each bit with an USB feature:

- OTG 1.3: USB2.0 On-The-Go 1.3 specification
- OTG 2.0: USB2.0 On-The-Go 2.0 specification
- BC1.1: Battery charging 1.1 specification
- OTHER: other USB feature inside this device

A 'X' means that bit functionality is related with the corresponding USB feature.

2.12.1 BACKUP_REG Register

Table 198. BACKUP_REG

Address	Dec 250, Hex FA		
Physical Address	ID1 = 48h	**Instance**	Backup Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	OTG_REV	ID_WK_UP_COMP

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	RESERVED	Reserved					R	0
6	RESERVED	Reserved					R	0
5	RESERVED	Reserved					R	0
4	RESERVED	Reserved					R	0
3	RESERVED	Reserved					R	0
2	RESERVED	Reserved					R	0
1	OTG_REV	0: OTG Revision 1.3 (Associated VBUS detection features enabled) 1: OTG Revision 2.0 (Associated VBUS detection features enabled)	X	X			R/W	1
0	ID_WK_UP_COMP	0: Wake-up comparator disabled 1: Wake-up comparator enabled				X	R/W	0

2.12.2 USB_VENDOR_ID_LSB Register

Table 199. USB_VENDOR_ID_LSB

Address	Dec 0, Hex 00		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
VENDOR_ID_7	VENDOR_ID_6	VENDOR_ID_5	VENDOR_ID_4	VENDOR_ID_3	VENDOR_ID_2	VENDOR_ID_1	VENDOR_ID_0

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	VENDOR_ID_7	Texas Instruments USB Vendor ID (8 LSBs) - Default value: 0x51				X	R	0
6	VENDOR_ID_6					X	R	1
5	VENDOR_ID_5					X	R	0
4	VENDOR_ID_4					X	R	1
3	VENDOR_ID_3					X	R	0
2	VENDOR_ID_2					X	R	0
1	VENDOR_ID_1					X	R	0
0	VENDOR_ID_0					X	R	1

2.12.3 USB_VENDOR_ID_MSB Register

Table 200. USB_VENDOR_ID_MSB

Address	Dec 1, Hex 01		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
VENDOR_ID_15	VENDOR_ID_14	VENDOR_ID_13	VENDOR_ID_12	VENDOR_ID_11	VENDOR_ID_10	VENDOR_ID_9	VENDOR_ID_8

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	VENDOR_ID_15	Texas Instruments USB Vendor ID (8 MSBs) - Default value: 0x04				X	R	0
6	VENDOR_ID_14					X	R	0
5	VENDOR_ID_13					X	R	0
4	VENDOR_ID_12					X	R	0
3	VENDOR_ID_11					X	R	0
2	VENDOR_ID_10					X	R	1
1	VENDOR_ID_9					X	R	0
0	VENDOR_ID_8					X	R	0

2.12.4 USB_PRODUCT_ID_LSB Register

Table 201. USB_PRODUCT_ID_LSB

Address	Dec 2, Hex 02		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
PRODUCT_ID_7	PRODUCT_ID_6	PRODUCT_ID_5	PRODUCT_ID_4	PRODUCT_ID_3	PRODUCT_ID_2	PRODUCT_ID_1	PRODUCT_ID_0

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	PRODUCT_ID_7	USB Product ID (8 LSBs) - EPROM Default value				X	R	0
6	PRODUCT_ID_6					X	R	0
5	PRODUCT_ID_5					X	R	1
4	PRODUCT_ID_4					X	R	1
3	PRODUCT_ID_3					X	R	0
2	PRODUCT_ID_2					X	R	0
1	PRODUCT_ID_1					X	R	1
0	PRODUCT_ID_0					X	R	0

2.12.5 USB_PRODUCT_ID_MSB Register

Table 202. USB_PRODUCT_ID_MSB

Address	Dec 3, Hex 03		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
PRODUCT_ID_15	PRODUCT_ID_14	PRODUCT_ID_13	PRODUCT_ID_12	PRODUCT_ID_11	PRODUCT_ID_10	PRODUCT_ID_9	PRODUCT_ID_8

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	PRODUCT_ID_15	USB Product ID (8 MSBs) - Default value: 0xC0				X	R	1
6	PRODUCT_ID_14					X	R	1
5	PRODUCT_ID_13					X	R	0
4	PRODUCT_ID_12					X	R	0
3	PRODUCT_ID_11					X	R	0
2	PRODUCT_ID_10					X	R	0
1	PRODUCT_ID_9					X	R	0
0	PRODUCT_ID_8					X	R	0

2.12.6 USB_VBUS_CTRL_SET Register

Table 203. USB_VBUS_CTRL_SET

Address	Dec 4, Hex 04		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/S/C		

7	6	5	4	3	2	1	0
VBUS_CHRG_VSYS	VBUS_CHRG_PMID	VBUS_DISCHRG	VBUS_IADP_SRC	VBUS_IADP_SINK	VBUS_ACT_COMP	RESERVED	VBUS_MEAS

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	VBUS_CHRG_VSYS	0: VBUS 2.5-kΩ pullup on VSYS is disabled. 1: VBUS 2.5-kΩ pullup on VSYS is enabled (VBUS charge mode).	X				R/S/C	0
6	VBUS_CHRG_PMID	0: VBUS 2.5-kΩ pullup on CHRG_PMID is disabled. 1: VBUS 2.5-kΩ pullup on CHRG_PMID is enabled (VBUS charge mode).	X				R/S/C	0
5	VBUS_DISCHRG	0: VBUS 10-kΩ pulldown is disabled. 1: VBUS 10-kΩ pulldown is enabled (VBUS discharge mode).	X				R/S/C	0
4	VBUS_IADP_SRC	0: VBUS IADP 1.4-mA current source is disabled. 1: VBUS IADP 1.4-mA current source is enabled.		X			R/S/C	0
3	VBUS_IADP_SINK	0: VBUS IADP 1.5-mA current sink is disabled. 1: VBUS IADP 1.5-mA current sink is enabled.		X			R/S/C	0
2	VBUS_ACT_COMP	0: VBUS sleep / active comparators are disabled. 1: VBUS sleep / active comparators are enabled. If OTG 1.3 (OTG_REV = 0) selected & VBUS_ACT_COMP = 1, it enables:VA_VBUS_VLD, VA_SESS_VLD, VB_SESS_VLD, VB_SESS_END If OTG 2.0 (OTG_REV = 1) selected & VBUS_ACT_COMP = 1, it enables: VA_VBUS_VLD, VOTG_SESS_VLD, VADP_PRB, VADP_SNS	X	X			R/S/C	0
1	RESERVED	Reserved					R	0
0	VBUS_MEAS	0: Disable VBUS voltage measurement through GPADC. 1: Enable VBUS voltage measurement through GPADC.				X	R/S/C	0

Notes:

- The VBUS wake-up comparator is automatically turned on when a VAC or VBUS plug detection event occurs, in order to perform the precharge and enable the ACA feature.
- The VBUS over-voltage comparator is automatically turned on when a VBUS plug is present, in order to protect the LDOUSB LDO from the CHRG_PMID input supply.

2.12.7 USB_VBUS_CTRL_CLR Register

Table 204. USB_VBUS_CTRL_CLR

Address	Dec 5, Hex 05		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/S/C		

7	6	5	4	3	2	1	0
VBUS_CHRG_VSYS	VBUS_CHRG_PMID	VBUS_DISCHRG	VBUS_IADP_SRC	VBUS_IADP_SINK	VBUS_ACT_COMP	RESERVED	VBUS_MEAS

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	VBUS_CHRG_VSYS	See USB_VBUS_CTRL_SET description.	X				R/S/C	0
6	VBUS_CHRG_PMID	See USB_VBUS_CTRL_SET description.	X				R/S/C	0
5	VBUS_DISCHRG	See USB_VBUS_CTRL_SET description.	X				R/S/C	0
4	VBUS_IADP_SRC	See USB_VBUS_CTRL_SET description.		X			R/S/C	0
3	VBUS_IADP_SINK	See USB_VBUS_CTRL_SET description.		X			R/S/C	0
2	VBUS_ACT_COMP	See USB_VBUS_CTRL_SET description.	X	X			R/S/C	0
1	RESERVED	Reserved					R	0
0	VBUS_MEAS	See USB_VBUS_CTRL_SET description.				X	R/S/C	0

2.12.8 USB_ID_CTRL_SET Register

Table 205. USB_ID_CTRL_SET

Address	Dec 6, Hex 06		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/S/C		

7	6	5	4	3	2	1	0
ID_PU_220K	ID_PU_100K	ID_GND_DRV	ID_SRC_16U	ID_SRC_5U	ID_ACT_COMP	RESERVED	ID_MEAS

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	ID_PU_220K	0: ID 220-kΩ pullup on LDOUSB is disabled. 1: ID 220-kΩ pullup on LDOUSB is enabled.				X	R/S/C	0
6	ID_PU_100K	0: ID 100-kΩ pullup on LDOUSB is disabled. 1: ID 100-kΩ pullup on LDOUSB is enabled.				X	R/S/C	0
5	ID_GND_DRV	0: ID 10-kΩ pulldown is disabled. 1: ID 10-kΩ pulldown is enabled (ID ground drive mode).				X	R/S/C	0
4	ID_SRC_16U	0: ID 16-µA current source is disabled. 1: ID 16-µA current source is enabled.			X		R/S/C	0
3	ID_SRC_5U	0: ID 5-µA current source is disabled. 1: ID 5-µA current source is enabled.				X	R/S/C	0
2	ID_ACT_COMP	0: Sleep/active comparators disabled. 1: Sleep/active comparators enabled.	X	X	X		R/S/C	0
1	RESERVED	Reserved					R	0
0	ID_MEAS	0: Disable ID voltage measurement through GPADC. 1: Enable ID voltage measurement through GPADC.				X	R/S/C	0

Note:

- The ID wake-up comparator is controlled by the ID_WK_UP_COMP register bit, available in the power management backup domain.

2.12.9 USB_ID_CTRL_CLR Register

Table 206. USB_ID_CTRL_CLR

Address	Dec 7, Hex 07		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/S/C		

7	6	5	4	3	2	1	0
ID_PU_220K	ID_PU_100K	ID_GND_DRV	ID_SRC_16U	ID_SRC_5U	ID_ACT_COMP	RESERVED	ID_MEAS

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	ID_PU_220K	See USB_ID_CTRL_SET description.				X	R/S/C	0
6	ID_PU_100K	See USB_ID_CTRL_SET description.				X	R/S/C	0
5	ID_GND_DRV	See USB_ID_CTRL_SET description.				X	R/S/C	0
4	ID_SRC_16U	See USB_ID_CTRL_SET description.			X		R/S/C	0
3	ID_SRC_5U	See USB_ID_CTRL_SET description.				X	R/S/C	0
2	ID_ACT_COMP	See USB_ID_CTRL_SET description.	X	X	X		R/S/C	0
1	RESERVED	Reserved					R	0
0	ID_MEAS	See USB_ID_CTRL_SET description.				X	R/S/C	0

2.12.10 USB_VBUS_INT_SRC Register

Table 207. USB_VBUS_INT_SRC

Address	Dec 8, Hex 08		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
VOTG_SESS_VLD	VADP_PRB	VADP_SNS	RESERVED	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	VOTG_SESS_VLD	0: VBUS line does not reach VOTG_SESS_VLD threshold. 1: VBUS line reaches VOTG_SESS_VLD threshold.		X			R	0
6	VADP_PRB	0: VBUS line does not reach VADP_PRB threshold. 1: VBUS line reaches VADP_PRB threshold.		X			R	0
5	VADP_SNS	0: VBUS line does not reach VADP_SNS threshold. 1: VBUS line reaches VADP_SNS threshold.		X			R	0
4	RESERVED	Reserved					R	0
3	VA_VBUS_VLD	0: VBUS line does not reach VA_VBUS_VLD threshold. 1: VBUS line reaches VA_VBUS_VLD threshold.	X	X			R	0
2	VA_SESS_VLD	0: VBUS line does not reach VA_SESS_VLD threshold. 1: VBUS line reaches VA_SESS_VLD threshold.	X				R	0
1	VB_SESS_VLD	0: VBUS line does not reach VB_SESS_VLD threshold. 1: VBUS line reaches VB_SESS_VLD threshold.	X				R	0
0	VB_SESS_END	0: VBUS line reaches VB_SESS_END threshold. 1: VBUS line does not reach VB_SESS_END threshold.	X				R	1

Notes:

- The USB_VBUS_INT_SRC source register represents the debounced current status of the VBUS line.
- VBUS comparators outputs status are continuously updating this source register.
- The VB_SESS_END comparator polarity is inverted in the analog OTG section.
- Therefore, when no VBUS plug is present, only the VB_SESS_END status of the register USB_VBUS_INT_SRC is at 1.
- The USB_VBUS_INT_SRC source register is not affected by the configured low / high enables located

in the USB_VBUS_INT_EN_LO_SET, USB_VBUS_INT_EN_LO_CLR, USB_VBUS_INT_EN_HI_SET, and USB_VBUS_INT_EN_HI_CLR registers.

- Indeed, those enables are only affecting the latched interrupts USB_VBUS_INT_LATCH_SET and USB_VBUS_INT_LATCH_CLR registers.
- VB_SESS_END polarity is always inverted, even in USB_VBUS_INT_LATCH_SET and USB_VBUS_INT_LATCH_CLR registers.
- Reserved BIT_4 is used for ADP interrupt. It does not require a source or an enable low bit.

2.12.11 USB_VBUS_INT_LATCH_SET Register

Table 208. USB_VBUS_INT_LATCH_SET

Address	Dec 9, Hex 09		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/S/C		

7	6	5	4	3	2	1	0
VOTG_SESS_VLD	VADP_PRB	VADP_SNS	ADP	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	VOTG_SESS_VLD	See USB_VBUS_INT_SRC description.		X			R/S/C	0
6	VADP_PRB	See USB_VBUS_INT_SRC description.		X			R/S/C	0
5	VADP_SNS	See USB_VBUS_INT_SRC description.		X			R/S/C	0
4	ADP	Depending on USB_OTG_ADP_CTRL ADP_MODE [1:0]: 0: No ADP interrupt occurred (probing or sensing). 1: An ADP interrupt occurred (probing or sensing).		X			R/S/C	0
3	VA_VBUS_VLD	See USB_VBUS_INT_SRC description.	X	X			R/S/C	0
2	VA_SESS_VLD	See USB_VBUS_INT_SRC description.	X				R/S/C	0
1	VB_SESS_VLD	See USB_VBUS_INT_SRC description.	X				R/S/C	0
0	VB_SESS_END	See USB_VBUS_INT_SRC description.	X				R/S/C	0

Notes:

- In normal operation, this _SET register is generally used in read mode only.
- The VBUS wake-up comparator has its dedicated interrupt line.
- The VBUS over-voltage comparator has its interrupt mechanism located in the charger section.
- The interrupt mechanism is working identical for all VBUS interrupt sources, even for the specific analog inverted VB_SESS_END:
  - 0: No interrupt occurred.
  - 1: An interrupt occurred, on either a rising or falling edge of the VBUS.
- All VBUS active interrupts present in the USB_VBUS_INT_LATCH_SET and USB_VBUS_INT_LATCH_CLR registers are ORed to the same interrupt handler line #19 (VBUS).

2.12.12 USB_VBUS_INT_LATCH_CLR Register

Table 209. USB_VBUS_INT_LATCH_CLR

Address	Dec 10, Hex 0A		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/S/C		

7	6	5	4	3	2	1	0
VOTG_SESS_VLD	VADP_PRB	VADP_SNS	ADP	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	VOTG_SESS_VLD	See USB_VBUS_INT_SRC description.		X			R/S/C	0
6	VADP_PRB	See USB_VBUS_INT_SRC description.		X			R/S/C	0
5	VADP_SNS	See USB_VBUS_INT_SRC description.		X			R/S/C	0
4	ADP	See USB_VBUS_INT_LATCH_SET description.		X			R/S/C	0
3	VA_VBUS_VLD	See USB_VBUS_INT_SRC description.	X	X			R/S/C	0
2	VA_SESS_VLD	See USB_VBUS_INT_SRC description.	X				R/S/C	0
1	VB_SESS_VLD	See USB_VBUS_INT_SRC description.	X				R/S/C	0
0	VB_SESS_END	See USB_VBUS_INT_SRC description.	X				R/S/C	0

Note:

- Writing 0xFF clears all captured events

2.12.13 USB_VBUS_INT_EN_LO_SET Register

Table 210. USB_VBUS_INT_EN_LO_SET

Address	Dec 11, Hex 0B		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/S/C		

7	6	5	4	3	2	1	0
VOTG_SESS_VLD	VADP_PRB	VADP_SNS	RESERVED	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	VOTG_SESS_VLD	See USB_VBUS_INT_SRC description.		X			R/S/C	0
6	VADP_PRB	See USB_VBUS_INT_SRC description.		X			R/S/C	0
5	VADP_SNS	See USB_VBUS_INT_SRC description.		X			R/S/C	0
4	RESERVED	Reserved					R	0
3	VA_VBUS_VLD	See USB_VBUS_INT_SRC description.	X	X			R/S/C	0
2	VA_SESS_VLD	See USB_VBUS_INT_SRC description.	X				R/S/C	0
1	VB_SESS_VLD	See USB_VBUS_INT_SRC description.	X				R/S/C	0
0	VB_SESS_END	See USB_VBUS_INT_SRC description.	X				R/S/C	0

2.12.14 USB_VBUS_INT_EN_LO_CLR Register

Table 211. USB_VBUS_INT_EN_LO_CLR

Address	Dec 12, Hex 0C		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/S/C		

7	6	5	4	3	2	1	0
VOTG_SESS_VLD	VADP_PRB	VADP_SNS	RESERVED	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	VOTG_SESS_VLD	See USB_VBUS_INT_SRC description.		X			R/S/C	0
6	VADP_PRB	See USB_VBUS_INT_SRC description.		X			R/S/C	0
5	VADP_SNS	See USB_VBUS_INT_SRC description.		X			R/S/C	0
4	RESERVED	Reserved					R	0
3	VA_VBUS_VLD	See USB_VBUS_INT_SRC description.	X	X			R/S/C	0
2	VA_SESS_VLD	See USB_VBUS_INT_SRC description.	X				R/S/C	0
1	VB_SESS_VLD	See USB_VBUS_INT_SRC description.	X				R/S/C	0
0	VB_SESS_END	See USB_VBUS_INT_SRC description.	X				R/S/C	0

2.12.15 USB_VBUS_INT_EN_HI_SET Register

Table 212. USB_VBUS_INT_EN_HI_SET

Address	Dec 13, Hex 0D		
Physical Address	ID2 = 49h	**Instance**	State Dom,ain
Description			
Type	R/S/C		

7	6	5	4	3	2	1	0
VOTG_SESS_VLD	VADP_PRB	VADP_SNS	ADP	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	VOTG_SESS_VLD	See USB_VBUS_INT_SRC description.		X			R/S/C	0
6	VADP_PRB	See USB_VBUS_INT_SRC description.		X			R/S/C	0
5	VADP_SNS	See USB_VBUS_INT_SRC description.		X			R/S/C	0
4	ADP	See USB_VBUS_INT_LATCH_SET description.		X			R/S/C	0
3	VA_VBUS_VLD	See USB_VBUS_INT_SRC description.	X	X			R/S/C	0
2	VA_SESS_VLD	See USB_VBUS_INT_SRC description.	X				R/S/C	0
1	VB_SESS_VLD	See USB_VBUS_INT_SRC description.	X				R/S/C	0
0	VB_SESS_END	See USB_VBUS_INT_SRC description.	X				R/S/C	0

2.12.16 USB_VBUS_INT_EN_HI_CLR Register

Table 213. USB_VBUS_INT_EN_HI_CLR

Address	Dec 14, Hex 0E		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/S/C		

7	6	5	4	3	2	1	0
VOTG_SESS_VLD	VADP_PRB	VADP_SNS	ADP	VA_VBUS_VLD	VA_SESS_VLD	VB_SESS_VLD	VB_SESS_END

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	VOTG_SESS_VLD	See USB_VBUS_INT_SRC description.		X			R/S/C	0
6	VADP_PRB	See USB_VBUS_INT_SRC description.		X			R/S/C	0
5	VADP_SNS	See USB_VBUS_INT_SRC description.		X			R/S/C	0
4	ADP	See USB_VBUS_INT_LATCH_SET description.		X			R/S/C	0
3	VA_VBUS_VLD	See USB_VBUS_INT_SRC description.	X	X			R/S/C	0
2	VA_SESS_VLD	See USB_VBUS_INT_SRC description.	X				R/S/C	0
1	VB_SESS_VLD	See USB_VBUS_INT_SRC description.	X				R/S/C	0
0	VB_SESS_END	See USB_VBUS_INT_SRC description.	X				R/S/C	0

2.12.17 USB_ID_INT_SRC Register

Table 214. USB_ID_INT_SRC

Address	Dec 15, Hex 0F		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	ID_FLOAT	ID_A	ID_B	ID_C	ID_GND

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	RESERVED	Reserved					R	0
6	RESERVED	Reserved					R	0
5	RESERVED	Reserved					R	0
4	ID_FLOAT	0: ID line does not reach the ID_FLOAT threshold. 1: ID line reaches ID_FLOAT threshold.	X	X	X		R	0
3	ID_A	0: ID line does not reach the ID_A threshold. 1: ID line reaches ID_A threshold.			X		R	0
2	ID_B	0: ID line does not reach the ID_B threshold. 1: ID line reaches ID_B threshold.			X		R	0
1	ID_C	0: ID line does not reach the ID_C threshold. 1: ID line reaches ID_C threshold.			X		R	0
0	ID_GND	0: ID line does not reach the ID_GND threshold. 1: ID line reaches ID_GND threshold.	X	X	X		R	0

Notes:

- The USB_ID_INT_SRC source register represents the debounced current status of the ID line.
- ID comparators outputs status are continuously updating this source register.
- Only 1 comparator output at a time is showing a status at 1, the other outputs staying at 0.
- Therefore, when an ID plug is present or not, only one status of the register USB_ID_INT_SRC is at 1.
- The USB_ID_INT_SRC source register is not affected by the configured low / high enables located in the following registers USB_ID_INT_EN_LO_SET, USB_ID_INT_EN_LO_CLR, USB_ID_INT_EN_HI_SET, and USB_ID_INT_EN_HI_CLR.
- Indeed, those enables are only affecting the latched interrupts USB_ID_INT_LATCH_SET and Table 216 registers.
- All ID active interrupts present in the USB_ID_INT_LATCH_SET and USB_ID_INT_LATCH_CLR registers are ORed to the same interrupt handler line #18 (ID).

2.12.18 USB_ID_INT_LATCH_SET Register

Table 215. USB_ID_INT_LATCH_SET

Address	Dec 16, Hex 10		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/S/C		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	ID_FLOAT	ID_A	ID_B	ID_C	ID_GND

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	RESERVED	Reserved					R	0
6	RESERVED	Reserved					R	0
5	RESERVED	Reserved					R	0
4	ID_FLOAT	See USB_ID_INT_SRC description.	X	X	X		R/S/C	0
3	ID_A	See USB_ID_INT_SRC description.			X		R/S/C	0
2	ID_B	See USB_ID_INT_SRC description.			X		R/S/C	0
1	ID_C	See USB_ID_INT_SRC description.			X		R/S/C	0
0	ID_GND	See USB_ID_INT_SRC description.	X	X	X		R/S/C	0

2.12.19 USB_ID_INT_LATCH_CLR Register

Table 216. USB_ID_INT_LATCH_CLR

Address	Dec 17, Hex 11		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/S/C		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	ID_FLOAT	ID_A	ID_B	ID_C	ID_GND

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	RESERVED	Reserved					R	0
6	RESERVED	Reserved					R	0
5	RESERVED	Reserved					R	0
4	ID_FLOAT	See USB_ID_INT_SRC description.	X	X	X		R/S/C	0
3	ID_A	See USB_ID_INT_SRC description.			X		R/S/C	0
2	ID_B	See USB_ID_INT_SRC description.			X		R/S/C	0
1	ID_C	See USB_ID_INT_SRC description.			X		R/S/C	0
0	ID_GND	See USB_ID_INT_SRC description.	X	X	X		R/S/C	0

2.12.20 USB_ID_INT_EN_LO_SET Register

Table 217. USB_ID_INT_EN_LO_SET

Address	Dec 18, Hex 12		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/S/C		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	ID_FLOAT	ID_A	ID_B	ID_C	ID_GND

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	RESERVED	Reserved					R	0
6	RESERVED	Reserved					R	0
5	RESERVED	Reserved					R	0
4	ID_FLOAT	See USB_ID_INT_SRC description.	X	X	X		R/S/C	0
3	ID_A	See USB_ID_INT_SRC description.			X		R/S/C	0
2	ID_B	See USB_ID_INT_SRC description.			X		R/S/C	0
1	ID_C	See USB_ID_INT_SRC description.			X		R/S/C	0
0	ID_GND	See USB_ID_INT_SRC description.	X	X	X		R/S/C	0

2.12.21 USB_ID_INT_EN_LO_CLR Register

Table 218. USB_ID_INT_EN_LO_CLR

Address	Dec 19, Hex 13		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/S/C		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	ID_FLOAT	ID_A	ID_B	ID_C	ID_GND

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	RESERVED	Reserved					R	0
6	RESERVED	Reserved					R	0
5	RESERVED	Reserved					R	0
4	ID_FLOAT	See USB_ID_INT_SRC description.	X	X	X		R/S/C	0
3	ID_A	See USB_ID_INT_SRC description.			X		R/S/C	0
2	ID_B	See USB_ID_INT_SRC description.			X		R/S/C	0
1	ID_C	See USB_ID_INT_SRC description.			X		R/S/C	0
0	ID_GND	See USB_ID_INT_SRC description.	X	X	X		R/S/C	0

2.12.22 USB_ID_INT_EN_HI_SET Register

Table 219. USB_ID_INT_EN_HI_SET

Address	Dec 20, Hex 14		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/S/C		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	ID_FLOAT	ID_A	ID_B	ID_C	ID_GND

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	RESERVED	Reserved					R	0
6	RESERVED	Reserved					R	0
5	RESERVED	Reserved					R	0
4	ID_FLOAT	See USB_ID_INT_SRC description.	X	X	X		R/S/C	0
3	ID_A	See USB_ID_INT_SRC description.			X		R/S/C	0
2	ID_B	See USB_ID_INT_SRC description.			X		R/S/C	0
1	ID_C	See USB_ID_INT_SRC description.			X		R/S/C	0
0	ID_GND	See USB_ID_INT_SRC description.	X	X	X		R/S/C	0

2.12.23 USB_ID_INT_EN_HI_CLR Register

Table 220. USB_ID_INT_EN_HI_CLR

Address	Dec 21, Hex 15		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/S/C		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	ID_FLOAT	ID_A	ID_B	ID_C	ID_GND

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	RESERVED	Reserved					R	0
6	RESERVED	Reserved					R	0
5	RESERVED	Reserved					R	0
4	ID_FLOAT	See USB_ID_INT_SRC description.	X	X	X		R/S/C	0
3	ID_A	See USB_ID_INT_SRC description.			X		R/S/C	0
2	ID_B	See USB_ID_INT_SRC description.			X		R/S/C	0
1	ID_C	See USB_ID_INT_SRC description.			X		R/S/C	0
0	ID_GND	See USB_ID_INT_SRC description.	X	X	X		R/S/C	0

2.12.24 USB_OTG_ADP_CTRL Register

Table 221. USB_OTG_ADP_CTRL

Address	Dec 22, Hex 16		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	ADP_MODE_1	ADP_MODE_0

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	RESERVED	Reserved					R	0
6	RESERVED	Reserved					R	0
5	RESERVED	Reserved					R	0
4	RESERVED	Reserved					R	0
3	RESERVED	Reserved					R	0
2	RESERVED	Reserved					R	0
1	ADP_MODE_1	00: ADP digital module is disabled. 01: ADP sensing mode is enabled.		X			R/W	0
0	ADP_MODE_0	10: ADP probing mode as an A-device is enabled. 11: ADP probing mode as a B-device is enabled.		X			R/W	0

2.12.25 USB_OTG_ADP_HIGH Register

Table 222. USB_OTG_ADP_HIGH

Address	Dec 23, Hex 17		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
T_ADP_HIGH_7	T_ADP_HIGH_6	T_ADP_HIGH_5	T_ADP_HIGH_4	T_ADP_HIGH_3	T_ADP_HIGH_2	T_ADP_HIGH_1	T_ADP_HIGH_0

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	T_ADP_HIGH_7	Timing interval value (high limit) - Number of 32-kHz clock cycles: 00000000: 0 clock cycle 00000001: 1 clock cycle ... 11111110: 254 clock cycles 11111111: 255 clock cycles		X			R/W	0
6	T_ADP_HIGH_6			X			R/W	0
5	T_ADP_HIGH_5			X			R/W	0
4	T_ADP_HIGH_4			X			R/W	0
3	T_ADP_HIGH_3			X			R/W	0
2	T_ADP_HIGH_2			X			R/W	0
1	T_ADP_HIGH_1			X			R/W	0
0	T_ADP_HIGH_0			X			R/W	0

2.12.26 USB_OTG_ADP_LOW Register

Table 223. USB_OTG_ADP_LOW

Address	Dec 24, Hex 18		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
T_ADP_LOW_7	T_ADP_LOW_6	T_ADP_LOW_5	T_ADP_LOW_4	T_ADP_LOW_3	T_ADP_LOW_2	T_ADP_LOW_1	T_ADP_LOW_0

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	T_ADP_HIGH_7	Timing interval value (high limit) - Number of 32-kHz clock cycles: 00000000: 0 clock cycle 00000001: 1 clock cycle ... 11111110: 254 clock cycles 11111111: 255 clock cycles		X			R/W	0
6	T_ADP_HIGH_6			X			R/W	0
5	T_ADP_HIGH_5			X			R/W	0
4	T_ADP_HIGH_4			X			R/W	0
3	T_ADP_HIGH_3			X			R/W	0
2	T_ADP_HIGH_2			X			R/W	0
1	T_ADP_HIGH_1			X			R/W	0
0	T_ADP_HIGH_0			X			R/W	0

2.12.27 USB_OTG_ADP_RISE Register

Table 224. USB_OTG_ADP_RISE

Address	Dec 25, Hex 19		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
T_ADP_RISE_7	T_ADP_RISE_6	T_ADP_RISE_5	T_ADP_RISE_4	T_ADP_RISE_3	T_ADP_RISE_2	T_ADP_RISE_1	T_ADP_RISE_0

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	T_ADP_RISE_7	ADP charge time duration - Number of 32-kHz clock cycles: 00000000: 0 clock cycle 00000001: 1 clock cycle ... 11111110: 254 clock cycles 11111111: 255 clock cycles		X			R	0
6	T_ADP_RISE_6			X			R	0
5	T_ADP_RISE_5			X			R	0
4	T_ADP_RISE_4			X			R	0
3	T_ADP_RISE_3			X			R	0
2	T_ADP_RISE_2			X			R	0
1	T_ADP_RISE_1			X			R	0
0	T_ADP_RISE_0			X			R	0

2.12.28 USB_OTG_REVISION Register

Table 225. USB_OTG_REVISION

Address	Dec 26, Hex 1A		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	OTG 1.3	OTG 2.0	BC 1.1	OTHER	Type	Reset
7	RESERVED	Reserved					R	0
6	RESERVED	Reserved					R	0
5	RESERVED	Reserved					R	0
4	RESERVED	Reserved					R	0
3	RESERVED	Reserved					R	0
2	RESERVED	Reserved					R	0
1	RESERVED	Reserved					R	0
0	RESERVED	Reserved					R	0

2.13 Gas Gauge

2.13.1 FG_REG_00 Register

Table 226. FG_REG_00

Address	Dec 192, Hex C0		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
CC_ACTIVE_MODE_1	CC_ACTIVE_MODE_0	RESERVED	RESERVED	RESERVED	CC_AUTOCLEAR	CC_CAL_EN	CC_PAUSE

Bits	Field Name	Description	Type	Reset
7	CC_ACTIVE_MODE_1	00 = 250-ms update rate 01 = 62.5-ms update rate	R/W	0
6	CC_ACTIVE_MODE_0	10 = 15.6-ms update rate 11 = 3.9-ms update rate	R/W	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	CC_AUTOCLEAR	Register bit self clears upon completion of clearing function: 0 = No action 1 = Clears the values in the CC_OFFSETx, CC_SAMPLE_CNTRx, and CC_ACCUMx registers.	R/W	0
1	CC_CAL_EN	Toggle bit used to run an auto-calibration sequence. 0 = No action 1 = Enables calibration sequence.	R/W	0
0	CC_PAUSE	0 = Analog updates to registers allowed. 1 = Analog updates to registers inhibited.	R/W	0

2.13.2 FG_REG_01 Register

Table 227. FG_REG_01

Address	Dec 193, Hex C1		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description	Number of conversions since last register reset(NRESPWRON pin low or CC_AUTOCLEAR bit set to logical 1)		
Type	R/W		

7	6	5	4	3	2	1	0
CC_SAMPLE_CNTR_07	CC_SAMPLE_CNTR_06	CC_SAMPLE_CNTR_05	CC_SAMPLE_CNTR_04	CC_SAMPLE_CNTR_03	CC_SAMPLE_CNTR_02	CC_SAMPLE_CNTR_01	CC_SAMPLE_CNTR_00

Bits	Field Name	Description	Type	Reset
7	CC_SAMPLE_CNTR_07	24-bit unsigned sample counter value.	R/W	0
6	CC_SAMPLE_CNTR_06		R/W	0
5	CC_SAMPLE_CNTR_05		R/W	0
4	CC_SAMPLE_CNTR_04		R/W	0
3	CC_SAMPLE_CNTR_03		R/W	0
2	CC_SAMPLE_CNTR_02		R/W	0
1	CC_SAMPLE_CNTR_01		R/W	0
0	CC_SAMPLE_CNTR_00		R/W	0

2.13.3 FG_REG_02 Register

Table 228. FG_REG_02

Address	Dec 194, Hex C2		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description	Number of conversions since last register reset(NRESPWRON pin low or CC_AUTOCLEAR bit set to logical 1)		
Type	R/W		

7	6	5	4	3	2	1	0
CC_SAMPLE_CNTR_15	CC_SAMPLE_CNTR_14	CC_SAMPLE_CNTR_13	CC_SAMPLE_CNTR_12	CC_SAMPLE_CNTR_11	CC_SAMPLE_CNTR_10	CC_SAMPLE_CNTR_09	CC_SAMPLE_CNTR_08

Bits	Field Name	Description	Type	Reset
7	CC_SAMPLE_CNTR_15	24-bit unsigned sample counter value.	R/W	0
6	CC_SAMPLE_CNTR_14		R/W	0
5	CC_SAMPLE_CNTR_13		R/W	0
4	CC_SAMPLE_CNTR_12		R/W	0
3	CC_SAMPLE_CNTR_11		R/W	0
2	CC_SAMPLE_CNTR_10		R/W	0
1	CC_SAMPLE_CNTR_09		R/W	0
0	CC_SAMPLE_CNTR_08		R/W	0

2.13.4 FG_REG_03 Register

Table 229. FG_REG_03

Address	Dec 195, Hex C3		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description	Number of conversions since last register reset(NRESPWRON pin low or CC_AUTOCLEAR bit set to logical 1)		
Type	R/W		

7	6	5	4	3	2	1	0
CC_SAMPLE_CNTR_23	CC_SAMPLE_CNTR_22	CC_SAMPLE_CNTR_21	CC_SAMPLE_CNTR_20	CC_SAMPLE_CNTR_19	CC_SAMPLE_CNTR_18	CC_SAMPLE_CNTR_17	CC_SAMPLE_CNTR_16

Bits	Field Name	Description	Type	Reset
7	CC_SAMPLE_CNTR_23	24-bit unsigned sample counter value.	R/W	0
6	CC_SAMPLE_CNTR_22		R/W	0
5	CC_SAMPLE_CNTR_21		R/W	0
4	CC_SAMPLE_CNTR_20		R/W	0
3	CC_SAMPLE_CNTR_19		R/W	0
2	CC_SAMPLE_CNTR_18		R/W	0
1	CC_SAMPLE_CNTR_17		R/W	0
0	CC_SAMPLE_CNTR_16		R/W	0

2.13.5 FG_REG_04 Register

Table 230. FG_REG_04

Address	Dec 196, Hex C4		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description	Accumulated current value since last register reset(NRESPWRON pin low or CC_AUTOCLEAR bit set to logical 1)		
Type	R/W		

7	6	5	4	3	2	1	0
CC_ACCUM_07	CC_ACCUM_06	CC_ACCUM_05	CC_ACCUM_04	CC_ACCUM_03	CC_ACCUM_02	CC_ACCUM_01	CC_ACCUM_00

Bits	Field Name	Description	Type	Reset
7	CC_ACCUM_07	32-bit signed accumulator value 2's complement.	R/W	0
6	CC_ACCUM_06		R/W	0
5	CC_ACCUM_05		R/W	0
4	CC_ACCUM_04		R/W	0
3	CC_ACCUM_03		R/W	0
2	CC_ACCUM_02		R/W	0
1	CC_ACCUM_01		R/W	0
0	CC_ACCUM_00		R/W	0

2.13.6 FG_REG_05 Register

Table 231. FG_REG_05

Address	Dec 197, Hex C5		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description	Accumulated current value since last register reset(NRESPWRON pin low or CC_AUTOCLEAR bit set to logical 1)		
Type	R/W		

7	6	5	4	3	2	1	0
CC_ACCUM_15	CC_ACCUM_14	CC_ACCUM_13	CC_ACCUM_12	CC_ACCUM_11	CC_ACCUM_10	CC_ACCUM_09	CC_ACCUM_08

Bits	Field Name	Description	Type	Reset
7	CC_ACCUM_15	32-bit signed accumulator value 2's complement.	R/W	0
6	CC_ACCUM_14		R/W	0
5	CC_ACCUM_13		R/W	0
4	CC_ACCUM_12		R/W	0
3	CC_ACCUM_11		R/W	0
2	CC_ACCUM_10		R/W	0
1	CC_ACCUM_09		R/W	0
0	CC_ACCUM_08		R/W	0

2.13.7 FG_REG_06 Register

Table 232. FG_REG_06

Address	Dec 198, Hex C6		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description	Accumulated current value since last register reset(NRESPWRON pin low or CC_AUTOCLEAR bit set to logical 1)		
Type	R/W		

7	6	5	4	3	2	1	0
CC_ACCUM_23	CC_ACCUM_22	CC_ACCUM_21	CC_ACCUM_20	CC_ACCUM_19	CC_ACCUM_18	CC_ACCUM_17	CC_ACCUM_16

Bits	Field Name	Description	Type	Reset
7	CC_ACCUM_23	32-bit signed accumulator value 2's complement.	R/W	0
6	CC_ACCUM_22		R/W	0
5	CC_ACCUM_21		R/W	0
4	CC_ACCUM_20		R/W	0
3	CC_ACCUM_19		R/W	0
2	CC_ACCUM_18		R/W	0
1	CC_ACCUM_17		R/W	0
0	CC_ACCUM_16		R/W	0

2.13.8 FG_REG_07 Register

Table 233. FG_REG_07

Address	Dec 199, Hex C7		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description	Accumulated current value since last register reset(NRESPWRON pin low or CC_AUTOCLEAR bit set to logical 1)		
Type	R/W		

7	6	5	4	3	2	1	0
CC_ACCUM_31	CC_ACCUM_30	CC_ACCUM_29	CC_ACCUM_28	CC_ACCUM_27	CC_ACCUM_26	CC_ACCUM_25	CC_ACCUM_24

Bits	Field Name	Description	Type	Reset
7	CC_ACCUM_31	32-bit signed accumulator value 2's complement.	R/W	0
6	CC_ACCUM_30		R/W	0
5	CC_ACCUM_29		R/W	0
4	CC_ACCUM_28		R/W	0
3	CC_ACCUM_27		R/W	0
2	CC_ACCUM_26		R/W	0
1	CC_ACCUM_25		R/W	0
0	CC_ACCUM_24		R/W	0

Note:

- With a 14-bit measurement result and an 18 bit number of samples, selecting the 250-ms integration period mode, the accumulator can store up to 18 hours with a 6-A maximum current, which typically gives 108 Ah. Nevertheless, the maximum time is also limited by the 24-bit sample counter, which gives 48 days with a 250-ms integration period.

2.13.9 FG_REG_08 Register

Table 234. FG_REG_08

Address	Dec 200, Hex C8		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description	DC offset value measured during auto-calibration		
Type	R/W		

7	6	5	4	3	2	1	0
CC_OFFSET_07	CC_OFFSET_06	CC_OFFSET_05	CC_OFFSET_04	CC_OFFSET_03	CC_OFFSET_02	CC_OFFSET_01	CC_OFFSET_00

Bits	Field Name	Description	Type	Reset
7	CC_OFFSET_07	10-bit signed offset value 2's complement.	R/W	0
6	CC_OFFSET_06		R/W	0
5	CC_OFFSET_05		R/W	0
4	CC_OFFSET_04		R/W	0
3	CC_OFFSET_03		R/W	0
2	CC_OFFSET_02		R/W	0
1	CC_OFFSET_01		R/W	0
0	CC_OFFSET_00		R/W	0

2.13.10 FG_REG_09 Register

Table 235. FG_REG_09

Address	Dec 201, Hex C9		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description	DC offset value measured during auto-calibration		
Type	R/W		

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CC_OFFSET_09	CC_OFFSET_08

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R/W	0
6	RESERVED	Reserved	R/W	0
5	RESERVED	Reserved	R/W	0
4	RESERVED	Reserved	R/W	0
3	RESERVED	Reserved	R/W	0
2	RESERVED	Reserved	R/W	0
1	CC_OFFSET_09	10-bit signed offset value 2's complement.	R/W	0
0	CC_OFFSET_08		R/W	0

2.13.11 FG_REG_10 Register

Table 236. FG_REG_10

Address	Dec 202, Hex CA		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description	Result of the last gas gauge conversion		
Type	R/W		

7	6	5	4	3	2	1	0
CC_INTEG_07	CC_INTEG_06	CC_INTEG_05	CC_INTEG_04	CC_INTEG_03	CC_INTEG_02	CC_INTEG_01	CC_INTEG_00

Bits	Field Name	Description	Type	Reset
7	CC_INTEG_07	14-bit signed integrator value 2’s complement.	R/W	0
6	CC_INTEG_06		R/W	0
5	CC_INTEG_05		R/W	0
4	CC_INTEG_04		R/W	0
3	CC_INTEG_03		R/W	0
2	CC_INTEG_02		R/W	0
1	CC_INTEG_01		R/W	0
0	CC_INTEG_00		R/W	0

2.13.12 FG_REG_11 Register

Table 237. FG_REG_11

Address	Dec 203, Hex CB		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description	Result of the last gas gauge conversion		
Type	R/W		

7	6	5	4	3	2	1	0
Reserved	Reserved	CC_INTEG_13	CC_INTEG_12	CC_INTEG_11	CC_INTEG_10	CC_INTEG_09	CC_INTEG_08

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R/W	0
6	RESERVED	Reserved	R/W	0
5	CC_INTEG_13	14-bit signed integrator value 2’s complement.	R/W	0
4	CC_INTEG_12		R/W	0
3	CC_INTEG_11		R/W	0
2	CC_INTEG_10		R/W	0
1	CC_INTEG_09		R/W	0
0	CC_INTEG_08		R/W	0

2.14 General Purpose ADC

The GPADC channels are summarized in Table 238.

Table 238. GPADC CHANNELS

CHANNEL	TYPE	SCALAR	OPERATION
0	External	No	Battery type, resistor value
1	External	No	Battery temperature, NTC resistor value
2	External	1.875/1.25 V	Audio accessory/general purpose
3	External	No	Temperature with external diode/general purpose
4	External	No	Temperature measurement/general purpose
5	External	No	General purpose
6	External	No	General purpose
7	Internal	5/1.25 V or 6.25/1.25 V	System supply
8	Internal	6.25/1.25 V	Backup battery
9	Internal	11.25/1.25 V	External charger input
10	Internal	6.875/1.25 V	VBUS
11	Internal	1.875/1.25 V	VBUS DCDC output current (available only without power path)
12	Internal	No	Die temperature
13	Internal	No	Die temperature
14	Internal	6.875/1.25 V	USB ID line
15	Internal	6.25/1.25 V	Test network
16	Internal	4.75/1.25 V	Test network
17	Internal	7.8125 A/1.25 V	Battery charging current (1.5 A maximum current)
18	Internal	5/1.25 V or 6.25/1.25 V	Battery voltage

2.14.1 GPADC_CTRL Register

Table 239. GPADC_CTRL

Address	Dec 46, Hex 2E		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
GPADC_ISOURCE_EN	TMP2_EN_MONITOR	TMP1_EN_MONITOR	GPADC_SCALER_EN_CH11	VSYS_SCALER_DIV4	GPADC_SCALER_EN_CH2	reserved	GPADC_TEMP1_EN

Bits	Field Name	Description	Type	Reset
7	GPADC_ISOURCE_EN	Control the additionnal 15-µA current source connected to GPADC_IN0. 0: Current source Disabled 1: Current source Enabled The current source can be controlled only if OTP bit EN_BAT_DET = 1.	R/W	0
6	TMP2_EN_MONITOR	0: Thermal shutdown #2: GPADC monitoring feature disabled. 1: Thermal shutdown #2: GPADC monitoring feature enabled.	R/W	0
5	TMP1_EN_MONITOR	0: Thermal shutdown #1: GPADC monitoring feature disabled. 1: Thermal shutdown #1: GPADC monitoring feature enabled.	R/W	0
4	GPADC_SCALER_EN_CH11	Enable the 1.875/1.25 V divider on GPADC channel 11(mandatory to convert channel 11) 0: Divider disabled 1: Divider Enabled	R/W	0
3	VSYS_SCALER_DIV4	Divider selection for VBAT, GPADC channel 7. 0:DIV5(6.25/1.25 V) selected. 1:DIV4(5/1.25 V) selected.	R/W	0
2	GPADC_SCALER_EN_CH2	Enable the 1.875/1.25 V divider on GPADC channel 2(mandatory to convert channel 2) 0: Divider disabled 1: Divider Enabled	R/W	0
1	reserved	reserved	R	0
0	GPADC_TEMP1_EN	0: GPADC_IN1 temperature measurement feature disabled. 1: GPADC_IN1 temperature measurement feature enabled.	R/W	0

2.14.2 GPADC_CTRL2 Register

Table 240. GPADC_CTRL2

Address	Dec 47, Hex 2F		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	VBAT_SCALER_DIV4	GPADC_SCALER_EN_CH18	GPADC_REMSENSE_1	GPADC_REMSENSE_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	VBAT_SCALER_DIV4	0: VBAT DIV5 scaler selected 1: VBAT DIV4 scaler selected	R/W	0
2	GPADC_SCALER_EN_CH18	0: Scaler Disabled 1: Scaler Enabled	R/W	0
1	GPADC_REMSENSE_1	Select current source for GPADC_IN3 input: 00: 0 µA 01: 10 µA 10: 400 µA 11: 800 µA Note: The current source is enabled/disabled automatically during conversion.	R/W	0
0	GPADC_REMSENSE_0		R/W	0

2.14.3 RTSELECT_LSB Register

Table 241. RTSELECT_LSB

Address	Dec 50, Hex 32		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
CH_7	CH_6	CH_5	CH_4	CH_3	CH_2	CH_1	CH_0

Bits	Field Name	Description	Type	Reset
7	CH_7	These bits become read-only bits during real-time conversion. When the bit CH_ [i] is set, the GPADC channel i is inserted in the conversion sequence started by a real-time request through GPADC_START. The conversion sequence can include one or two channels. If more than two channels are selected, the two channels with lowest number are converted. See Table 238 for channels description	R/W	0
6	CH_6		R/W	0
5	CH_5		R/W	0
4	CH_4		R/W	0
3	CH_3		R/W	0
2	CH_2		R/W	0
1	CH_1		R/W	0
0	CH_0		R/W	0

2.14.4 RTSELECT_ISB Register

Table 242. RTSELECT_ISB

Address	Dec 51, Hex 33		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
CH_15	CH_14	CH_13	CH_12	CH_11	CH_10	CH_9	CH_8

Bits	Field Name	Description	Type	Reset
7	CH_15	These bits become read-only bits during real-time conversion.When the bit CH_ [i] is set, the GPADC channel i is inserted in the conversion sequence started by a real-time request through GPADC_START. The conversion sequence can include one or two channels. If more than two channels are selected, the two channels with lowest number are converted. See Table 238 for channels description	R/W	0
6	CH_14		R/W	0
5	CH_13		R/W	0
4	CH_12		R/W	0
3	CH_11		R/W	0
2	CH_10		R/W	0
1	CH_09		R/W	0
0	CH_08		R/W	0

2.14.5 RTSELECT_MSB Register

Table 243. RTSELECT_MSB

Address	Dec 52, Hex 34		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CH_18	CH_17	CH_16

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	CH_18	These bits become read-only bits during real-time conversion.When the bit CH_ [i] is set, the GPADC channel i is inserted in the conversion sequence started by a real-time request through GPADC_START. The conversion sequence can include one or two channels. If more than two channels are selected, the two channels with lowest number are converted. See Table 238 for channels description	R/W	0
1	CH_17		R/W	0
0	CH_16		R/W	0

2.14.6 CTRL_P1 Register

Table 244. CTRL_P1

Address	Dec 54, Hex 36		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	SP1	EOCRT	EOCP1	BUSY

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	SP1	**Start Process #1**: Toggle bit used by the processor (Process #1) to start a conversion. Writing logical 0 in this bit has no effect.	W	0
2	EOCRT	**End Of Conversion Real Time**: When this bit is set GPADC indicates that conversion with real time constraints required by the GPADC_START pin is terminated. An interrupt has been sent at the end of required conversion sequence to the interrupts controller. Default state is logic 1 indicating that the conversion is terminated. While associated conversion sequence is running this bit is at logical 0.	R	1
1	EOCP1	**End Of Conversion Process #1**: When this bit is set GPADC indicates that conversion required by the processor (Process #1) is terminated. An interrupt has been sent at the end of required conversion sequence to the interrupts controller. Default state is logic 1 indicating that the conversion is terminated. While associated conversion sequence is running this bit is at logical 0.	R	1
0	BUSY	When this bit is set to 1, the GPADC is running conversions.	R	0

2.14.7 GPSELECT_ISB Register

Table 245. GPSELECT_ISB

Address	Dec 53, Hex 35		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	BIT_4	These bits select the input channel for GP conversion: See Table 238 for channels description 00000: Channel 000001: Channel 1 ... 10001: Channel 17 10010: Channel 18 10011: No conversion ... 11111: No conversion	R/W	0
3	BIT_3		R/W	0
2	BIT_2		R/W	0
1	BIT_1		R/W	0
0	BIT_0		R/W	0

2.14.8 RTCH0_LSB Register

Table 246. RTCH0_LSB

Address	Dec 55, Hex 37		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0

Bits	Field Name	Description	Type	Reset
7	BIT_7	Conversion result of the lowest RTSELECT channel (8 LSBs). If COLLISION_RT bit is at 1 (that is, during a real-time conversion), the read value is 0x00.	R	0
6	BIT_6		R	0
5	BIT_5		R	0
4	BIT_4		R	0
3	BIT_3		R	0
2	BIT_2		R	0
1	BIT_1		R	0
0	BIT_0		R	0

2.14.9 RTCH0_MSB Register

Table 247. RTCH0_MSB

Address	Dec 56, Hex 38		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	COLLISION_RT	BIT_11	BIT_10	BIT_9	BIT_8

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	COLLISION_RT	**Collision Read Real Time**: This bit is set at 1 when a read operation occurs during an on going real-time sequence of conversions (EOCRT control bit at 0): If COLLISION_RT is at 1, the read value is 0x10.	R	0
3	BIT_11	Conversion result of the lowest RTSELECT channel (4 MSBs)	R	0
2	BIT_10		R	0
1	BIT_9		R	0
0	BIT_8		R	0

2.14.10 RTCH1_LSB Register

Table 248. RTCH1_LSB

Address	Dec 57, Hex 39		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0

Bits	Field Name	Description	Type	Reset
7	BIT_7	Conversion result of the second lowest RTSELECT channel (8 LSBs). If only one channels is selected, the register is not updated. If COLLISION_RT bit is at 1 (that is, during a real-time conversion), the read value is 0x00.	R	0
6	BIT_6		R	0
5	BIT_5		R	0
4	BIT_4		R	0
3	BIT_3		R	0
2	BIT_2		R	0
1	BIT_1		R	0
0	BIT_0		R	0

2.14.11 RTCH1_MSB Register

Table 249. RTCH1_MSB

Address	Dec 58, Hex 3A		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	COLLISION_RT	BIT_11	BIT_10	BIT_9	BIT_8

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	COLLISION_RT	**Collision Read Real Time**: This bit is set at 1 when a Read operation occurs during an on going real-time sequence of conversions (EOCRT control bit at 0): If COLLISION_RT is at 1, the read value is 0x10.	R	0
3	BIT_11	Conversion result of the second lowest RTSELECT channel (4 MSBs). If only one channels is selected, the register is not updated.	R	0
2	BIT_10		R	0
1	BIT_9		R	0
0	BIT_8		R	0

2.14.12 GPCH0_LSB Register

Table 250. GPCH0_LSB

Address	Dec 59, Hex 3B		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_1	BIT_0

Bits	Field Name	Description	Type	Reset
7	BIT_7	Conversion result of asynchronous conversion (8 LSBs). If COLLISION_GP bit is at 1, the read value is 0x00.	R	0
6	BIT_6		R	0
5	BIT_5		R	0
4	BIT_4		R	0
3	BIT_3		R	0
2	BIT_2		R	0
1	BIT_1		R	0
0	BIT_0		R	0

2.14.13 GPCH0_MSB Register

Table 251. GPCH0_MSB

Address	Dec 60, Hex 3C		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	COLLISION_GP	BIT_11	BIT_10	BIT_9	BIT_8

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	COLLISION_GP	**Collision Asynchronous**: This bit is set at 1 when a read operation occurs during an on going asynchronous conversions (EOCP1 control bit at 0): If COLLISION_GP is at 1, the read value is 0x10.	R	0
3	BIT_11	Conversion result of asynchronous conversion (4 MSBs).	R	0
2	BIT_10		R	0
1	BIT_9		R	0
0	BIT_8		R	0

2.15 SIM, MMC, and Battery Detection

2.15.1 SIMDEBOUNCING Register

Table 252. SIMDEBOUNCING

Address	Dec 235, Hex EB		
Physical Address	ID2 = 48h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
SIM_DEB_BYPASS	SINS_DEB_3	SINS_DEB_2	SINS_DEB_1	SINS_DEB_0	SEXT_DEB_2	SEXT_DEB_1	SEXT_DEB_0

Bits	Field Name	Description	Type	Reset
7	SIM_DEB_BYPASS	0: SIM debouncing enabled (duration selected by SINS/SEXT_DEB bits). 1: SIM debouncing bypassed (no debouncing).	R/W	0
6	SINS_DEB_3	SIM card insertion debouncing time: Code 0000: Debouncing time 0.5 ms (default state)	R/W	0
5	SINS_DEB_2	Code 0001: Debouncing time 1 ms	R/W	0
4	SINS_DEB_1	...	R/W	0
3	SINS_DEB_0	Code 1111: Debouncing time 8 ms **Note:** Insertion debouncing step is 0.5 ms	R/W	0
2	SEXT_DEB_2	SIM card extraction debouncing time Code 000: Debouncing time 31.25 µs (default state)	R/W	0
1	SEXT_DEB_1	Code 001: Debouncing time 62.50 µs Code 010: Debouncing time 93.75 µs	R/W	0
0	SEXT_DEB_0	... Code 111: Debouncing time 250.00 µs **Note**: Extraction debouncing step is 31.25 µs	R/W	0

Note:

- When software selects to bypass the debounce, it should first mask the interrupt.

2.15.2 SIMCTRL Register

Table 253. SIMCTRL

Address	Dec 236, Hex EC		
Physical Address	ID2 = 48h	**Instance**	State Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	LDO7_DEL	SIM_BATDET_1	SIM_BATDET_0	VSIM_AUTO_OFF	SW_FC	STS_BAT	STS_SIM

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	LDO7_DEL	When VSIM_AUTO_OFF = 1: 0: LDO7 is switched off after 125-µs delay 1: LDO7 is switched off after 416-µs delay	R/W	0
5	SIM_BATDET_1	00: BATREMOVAL pin state depends on battery detection or SIM detection. 01: BATREMOVAL pin state depends only of battery detection. 10: BATREMOVAL pin state depends only of SIM detection. 11: BATREMOVAL pin state depends on battery detection and SIM detection. The MSB can be masked by BATREMOVAL EPROM bit to allow only the two first options (00 and 01).	R/W	0
4	SIM_BATDET_0		R/W	1
3	VSIM_AUTO_OFF	0: When a card is extracted, there is no interaction on the regulator. 1: When a card is extracted, the regulator is automatically turned off.	R/W	1
2	SW_FC	SW_FC bit allows to configure the internal circuitry at the varying of the external SIM card receptacle mechanical contact: 0: Insertion corresponds to an open-state of the external mechanical contact. (SIM pin high) 1: Insertion corresponds to a close state of the external mechanical contact. (SIM pin low)	R/W	0
1	STS_BAT	0: Main battery is not present. 1: Main battery is present.	R	0
0	STS_SIM	0: SIM card is not present. 1: SIM card is present.	R	0

2.15.3 MMCDEBOUNCING Register

Table 254. MMCDEBOUNCING

Address	Dec 237, Hex ED		
Physical Address	ID2 = 48h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
MMC_DEB_BYPASS	MINS_DEB_3	MINS_DEB_2	MINS_DEB_1	MINS_DEB_0	MEXT_DEB_2	MEXT_DEB_1	MEXT_DEB_0

Bits	Field Name	Description	Type	Reset
7	MMC_DEB_BYPASS	0: MMC debouncing enabled (duration selected by MINS/MEXT_DEB bits). 1: MMC debouncing bypassed (no debouncing).	R/W	1
6	MINS_DEB_3	MMC card insertion debouncing time: Code 0000: Debouncing time 0.5 ms (default state)	R/W	0
5	MINS_DEB_2	Code 0001: Debouncing time 1 ms	R/W	0
4	MINS_DEB_1	...	R/W	0
3	MINS_DEB_0	Code 1111: Debouncing time 8 ms **Note :** Insertion debouncing step is 0.5 ms	R/W	0
2	MEXT_DEB_2	MMC card extraction debouncing time: Code 000: Debouncing time 31.25 µs (default state)	R/W	0
1	MEXT_DEB_1	Code 001: Debouncing time 62.50 µs Code 010: Debouncing time 93.75 µs	R/W	0
0	MEXT_DEB_0	... Code 111: Debouncing time 250.00 µs **Note**: Extraction debouncing step is 31.25 µs	R/W	0

Note:

- When software select to bypass the debounce, it should first mask the interrupt.

2.15.4 MMCCTRL Register

Table 255. MMCCTRL

Address	Dec 238, Hex EE		
Physical Address	ID2 = 48h	**Instance**	State Domain
Description			
Type			

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	LDO5_AUTO_OFF	SW_FC	RESERVED	STS_MMC

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	LDO5_AUTO_OFF	0: When a card is extracted, there is no interaction on the regulator. 1: When a card is extracted, the regulator is automatically turned off.	R/W	1
2	SW_FC	SW_FC bit allows to configure the internal circuitry at the varying of the external MMC card receptacle mechanical contact: 0: Insertion corresponds to an open-state of the external mechanical contact. (MMC pin high) 1: Insertion corresponds to a close state of the external mechanical contact. (MMC pin low)	R/W	0
1	RESERVED	Reserved	R	0
0	STS_MMC	0: MMC card is not present. 1: MMC card is present.	R	0

2.15.5 BATDEBOUNCING Register

Table 256. BATDEBOUNCING

Address	Dec 239, Hex EF		
Physical Address	ID2 = 48h	**Instance**	State Domain
Description			
Type	R/w		

7	6	5	4	3	2	1	0
BAT_DEB_BYPASS	BINS_DEB_3	BINS_DEB_2	BINS_DEB_1	BINS_DEB_0	BEXT_DEB_2	BEXT_DEB_1	BEXT_DEB_0

Bits	Field Name	Description	Type	Reset
7	BAT_DEB_BYPASS	0: Battery debouncing enabled (duration selected by BINS/BEXT_DEB bits). 1: Battery debouncing bypassed (no debouncing).	R/W	1
6	BINS_DEB_3	Battery insertion debouncing time: Code 0000: Debouncing time 0.5 ms (default state)	R/W	0
5	BINS_DEB_2	Code 0001: Debouncing time 1 ms	R/W	0
4	BINS_DEB_1	...	R/W	0
3	BINS_DEB_0	Code 1111: Debouncing time 8 ms **Note**: Insertion debouncing step is 0.5 ms	R/W	0
2	BEXT_DEB_2	Battery extraction debouncing time: Code 000: Debouncing time 31.25 µs (default state)	R/W	0
1	BEXT_DEB_1	Code 001: Debouncing time 62.50 µs	R/W	0
0	BEXT_DEB_0	... Code 111: Debouncing time 250.00 µs **Note**: Extraction debouncing step is 31.25 µs	R/W	0

Note:

- When software selects to bypass the debounce, it should first mask the interrupt.

2.16 Vibrator Driver and PWMs

2.16.1 VIBCTRL Register

Table 257. VIBCTRL

Address	Dec 155, Hex 9B		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	DSEL_1	DSEL_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	DSEL_1	Duty-cycle selection: 00: Duty-cycle = 100% (default mode) 01: Duty-cycle = 75% 10: Duty-cycle = 50% 11: Duty-cycle = 25%	R/W	0
0	DSEL_0		R/W	0

2.16.2 VIBMODE Register

Table 258. VIBMODE

Address	Dec 156, Hex 9C		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	FREQ_1	FREQ_0	RESERVED

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	FREQ_1	Vibrator frequency: x0: 4-Hz frequency, based on 32.768 kHz resynchronized on 6 MHz x1: 8-kHz frequency, based on 32.768 kHz resynchronized on 6 MHz	R/W	0
0	FREQ_0		R/W	0

2.16.3 PWM1ON Register

Table 259. PWM1ON

Address	Dec 186, Hex BA		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
PWM1_LENGTH	PWM1ON_6	PWM1ON_5	PWM1ON_4	PWM1ON_3	PWM1ON_2	PWM1ON_1	PWM1ON_0

Bits	Field Name	Description	Type	Reset
7	PWM1_LENGTH	Allow to select how many clock cycles are used in the PWM1 period: 128 (default value: bit at 0) or 64 (bit at 1)	R/W	0
6	PWM1ON_6	Number of periods PWM1 output turns on.	R/W	0
5	PWM1ON_5		R/W	0
4	PWM1ON_4		R/W	0
3	PWM1ON_3		R/W	0
2	PWM1ON_2		R/W	0
1	PWM1ON_1		R/W	0
0	PWM1ON_0		R/W	0

2.16.4 PWM1OFF Register

Table 260. PWM1OFF

Address	Dec 187, Hex BB		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	PWM1OFF_6	PWM1OFF_5	PWM1OFF_4	PWM1OFF_3	PWM1OFF_2	PWM1OFF_1	PWM1OFF_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	PWM1OFF_6	Number of periods PWM1 output turns off.	R/W	0
5	PWM1OFF_5		R/W	0
4	PWM1OFF_4		R/W	0
3	PWM1OFF_3		R/W	0
2	PWM1OFF_2		R/W	0
1	PWM1OFF_1		R/W	0
0	PWM1OFF_0		R/W	0

2.16.5 PWM2ON Register

Table 261. PWM2ON

Address	Dec 189, Hex BD		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
PWM2_LENGTH	PWM2ON_6	PWM2ON_5	PWM2ON_4	PWM2ON_3	PWM2ON_2	PWM2ON_1	PWM2ON_0

Bits	Field Name	Description	Type	Reset
7	PWM2_LENGTH	Allow to select how many clock cycles are used in the PWM1 period: 128 (default value: bit at 0) or 64 (bit at 1)	R/W	0
6	PWM2ON_6	Number of periods PWM2 output turns on.	R/W	0
5	PWM2ON_5		R/W	0
4	PWM2ON_4		R/W	0
3	PWM2ON_3		R/W	0
2	PWM2ON_2		R/W	0
1	PWM2ON_1		R/W	0
0	PWM2ON_0		R/W	0

2.16.6 PWM2OFF Register

Table 262. PWM2OFF

Address	Dec 190, Hex BE		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
RESERVED	PWM2OFF_6	PWM2OFF_5	PWM2OFF_4	PWM2OFF_3	PWM2OFF_2	PWM2OFF_1	PWM2OFF_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	PWM2OFF_6	Number of periods PWM2 output turns off.	R/W	0
5	PWM2OFF_5		R/W	0
4	PWM2OFF_4		R/W	0
3	PWM2OFF_3		R/W	0
2	PWM2OFF_2		R/W	0
1	PWM2OFF_1		R/W	0
0	PWM2OFF_0		R/W	0

2.17 Control Interface

The interrupts are summarized in Table 263.

Table 263. Interrupts Mapping

#	Reg	Section	Interrupt	Description
00	A0	PM	PWRON	PWRON detection: Power on button pressed and releasedDetection is performed on both falling and rising edgesInterrupt is sent in SLEEP or ACTIVE only, not in WAIT-ON
01	A1	PM	RPWRON	RPWRON detection: Remote power on signal changeInterrupt is sent in SLEEP or ACTIVE only, not in WAIT-ON
02	A2	PM	SYS_VLOW	System voltage low: System voltage decreasing and crossing V_{SYSMIN_HI}
03	A3	RTC	RTC_ALARM	RTC alarm event: Occurs at programmed determinate date and time
04	A4	RTC	RTC_PERIOD	RTC periodic event: Occurs at programmed regular period of time (every second or minute…)
05	A5	Thermal monitoring and shutdown	HOT_DIE	At least one of the two embedded thermal monitoring modules has detected a die temperature above the Hot-Die detection threshold
06	A6	SMPS/LDO	VXXX_SHORT	At least one of the following power resources has its output shorted:SMPS4, SMPS5, SMPS1, SMPS2, SMPS3, VANA, LDO2, LDO3, LDO4, LDO5, LDO6, LDO7, LDOLN, LDO1, LDOUSB
07	A7	PM	SPDURATION	PWRON short press duration.
08	B0	PM	WATCHDOG	Primary watchdog expires.
09	B1	Detection	BAT	Battery detection plug / unplug
10	B2	Detection	SIM	SIM card plug / unplug
11	B3	Detection	MMC	MMC card plug / unplug
12	B4	GPADC	GPADC_RT_EOC	End of conversion: Completion of a real-time conversion cycle; result available
13	B5	GPADC	GPADC_SW_EOC	End of conversion: Completion of a real time and a GP software 1 (SW1) conversion cycle, result available
14	B6	GasGauge	CC_EOC	End of conversion: Completion of gas gauge measurement (end of integration period); result available
15	B7	GasGauge	CC_AUTOCAL	Calibration procedure finished and the result are available in the register
16	C0	OTG	ID_WKUP	ID wake-up event (from WAIT-ON / SLEEP states)
17	C1	OTG	VBUS_WKUP	VBUS wake-up event (from WAIT-ON / SLEEP states)
18	C2	OTG	ID	ID event detection in SLEEP / ACTIVE states
19	C3	OTG	VBUS	VBUS event detection in SLEEP / ACTIVE states
20	C4	Charger	CHRG_CTRL	Charger controller Interrupt source can be: • Charger plug insertion and removal detection: – VAC_PLUG – VBUS_PLUG • Watchdogs 32mn / 32s interrupts: – FAULT_WDG • Battery interrupts: – BAT_REMOVED – BAT_TEMP_OVRANGE • Linear charger interrupt: – LINCH_GATED
21	C5	Charger	EXT_CHRG	External charger fault(CHRG_EXTCHRG_STATZ)

Table 263. Interrupts Mapping (continued)

#	Reg	Section	Interrupt	Description
22	C6	Charger	INT_CHRG	Internal USB charger fault Interrupt source can be: • CHARGERUSB_FAULT • CHARGERUSB_THMREG • CHARGERUSB_STAT • CURRENT_TERM • EN_LINCH
23	C7			Reserved

2.17.1 INT_STS_A Register

Table 264. INT_STS_A

Address	Dec 208, Hex D0		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
INT_STS_07	INT_STS_06	INT_STS_05	INT_STS_04	INT_STS_03	INT_STS_02	INT_STS_01	INT_STS_00

Bits	Field Name	Description	Type	Reset
7	INT_STS_07	Status of interrupt number 0 to 7. INT_STS [i] is set to 1 when the associated interrupt number i event is detected. All bits are cleared to 0 when a WRITE access (data 0 or 1) occurs on this register. See Table 263.	R/W	0
6	INT_STS_06		R/W	0
5	INT_STS_05		R/W	0
4	INT_STS_04		R/W	0
3	INT_STS_03		R/W	0
2	INT_STS_02		R/W	0
1	INT_STS_01		R/W	0
0	INT_STS_00		R/W	0

2.17.2 INT_STS_B Register

Table 265. INT_STS_B

Address	Dec 209, Hex D1		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
INT_STS_15	INT_STS_14	INT_STS_13	INT_STS_12	INT_STS_11	INT_STS_10	INT_STS_09	INT_STS_08

Bits	Field Name	Description	Type	Reset
7	INT_STS_15	Status of interrupt number 8 to 15. INT_STS [i] is set to 1 when the associated interrupt number i event is detected. All bits are cleared to 0 when a WRITE access (data 0 or 1) occurs on this register. See Table 263.	R/W	0
6	INT_STS_14		R/W	0
5	INT_STS_13		R/W	0
4	INT_STS_12		R/W	0
3	INT_STS_11		R/W	0
2	INT_STS_10		R/W	0
1	INT_STS_09		R/W	0
0	INT_STS_08		R/W	0

2.17.3 INT_STS_C Register

Table 266. INT_STS_C

Address	Dec 210, Hex D2		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
INT_STS_23	INT_STS_22	INT_STS_21	INT_STS_20	INT_STS_19	INT_STS_18	INT_STS_17	INT_STS_16

Bits	Field Name	Description	Type	Reset
7	INT_STS_23	Status of interrupt number 16 to 23. INT_STS [i] is set to 1 when the associated interrupt number i event is detected. All bits are cleared to 0 when a WRITE access (data 0 or 1) occurs on this register. See Table 263.	R/W	0
6	INT_STS_22		R/W	0
5	INT_STS_21		R/W	0
4	INT_STS_20		R/W	0
3	INT_STS_19		R/W	0
2	INT_STS_18		R/W	0
1	INT_STS_17		R/W	0
0	INT_STS_16		R/W	0

2.17.4 INT_MSK_LINE_A Register

Table 267. INT_MSK_LINE_A

Address	Dec 211, Hex D3		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
INT_MSK_LINE_07	INT_MSK_LINE_06	INT_MSK_LINE_05	INT_MSK_LINE_04	INT_MSK_LINE_03	INT_MSK_LINE_02	INT_MSK_LINE_01	INT_MSK_LINE_00

Bits	Field Name	Description	Type	Reset
7	INT_MSK_LINE_07	Line mask of interrupt number 0 to 7. When INT_MSK_LINE [i] is set to 1, the associated interrupt number i is INT line masked, which means that no interrupt is generated on the INT line. When INT_MSK_LINE [i] is set to 0, the associated interrupt number i is INT line enabled: An interrupt is generated on the INT line. In any case, the INT_STS [i] status bit may or may not be updated, only linked to the INT_MSK_STS [i] configuration register bit.	R/W	0
6	INT_MSK_LINE_06		R/W	0
5	INT_MSK_LINE_05		R/W	0
4	INT_MSK_LINE_04		R/W	0
3	INT_MSK_LINE_03		R/W	0
2	INT_MSK_LINE_02		R/W	0
1	INT_MSK_LINE_01		R/W	0
0	INT_MSK_LINE_00		R/W	0

2.17.5 INT_MSK_LINE_B Register

Table 268. INT_MSK_LINE_B

Address	Dec 212, Hex D4		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
INT_MSK_LINE_15	INT_MSK_LINE_14	INT_MSK_LINE_13	INT_MSK_LINE_12	INT_MSK_LINE_11	INT_MSK_LINE_10	INT_MSK_LINE_09	INT_MSK_LINE_08

Bits	Field Name	Description	Type	Reset
7	INT_MSK_LINE_15	Line mask of interrupt number 8 to 15. When INT_MSK_LINE [i] is set to 1, the associated interrupt number i is INT line masked, which means that no interrupt is generated on the INT line. When INT_MSK_LINE [i] is set to 0, the associated interrupt number i is INT line enabled: An interrupt is generated on the INT line. In any case, the INT_STS [i] status bit may or may not be updated, only linked to the INT_MSK_STS [i] configuration register bit.	R/W	0
6	INT_MSK_LINE_14		R/W	0
5	INT_MSK_LINE_13		R/W	0
4	INT_MSK_LINE_12		R/W	0
3	INT_MSK_LINE_11		R/W	0
2	INT_MSK_LINE_10		R/W	0
1	INT_MSK_LINE_09		R/W	0
0	INT_MSK_LINE_08		R/W	0

2.17.6 INT_MSK_LINE_C Register

Table 269. INT_MSK_LINE_C

Address	Dec 213, Hex D5		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
INT_MSK_LINE_23	INT_MSK_LINE_22	INT_MSK_LINE_21	INT_MSK_LINE_20	INT_MSK_LINE_19	INT_MSK_LINE_18	INT_MSK_LINE_17	INT_MSK_LINE_16

Bits	Field Name	Description	Type	Reset
7	INT_MSK_LINE_23	Line mask of interrupt number 16 to 23. When INT_MSK_LINE [i] is set to 1, the associated interrupt number i is INT line masked, which means that no interrupt is generated on the INT line. When INT_MSK_LINE [i] is set to 0, the associated interrupt number i is INT line enabled: An interrupt is generated on the INT line. In any case, the INT_STS [i] status bit may or may not be updated, only linked to the INT_MSK_STS [i] configuration register bit.	R/W	0
6	INT_MSK_LINE_22		R/W	0
5	INT_MSK_LINE_21		R/W	0
4	INT_MSK_LINE_20		R/W	0
3	INT_MSK_LINE_19		R/W	0
2	INT_MSK_LINE_18		R/W	0
1	INT_MSK_LINE_17		R/W	0
0	INT_MSK_LINE_16		R/W	0

2.17.7 INT_MSK_STS_A Register

Table 270. INT_MSK_STS_A

Address	Dec 214, Hex D6		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
INT_MSK_STS_07	INT_MSK_STS_06	INT_MSK_STS_05	INT_MSK_STS_04	INT_MSK_STS_03	INT_MSK_STS_02	INT_MSK_STS_01	INT_MSK_STS_00

Bits	Field Name	Description	Type	Reset
7	INT_MSK_STS_07	Status mask of interrupt number 0 to 7. When INT_MSK_STS [i] is set to 1, the associated interrupt number i is status masked, which means that no interrupt is stored in the INT_STS [i] status bit. Note that no interrupt number i is generated on the INT line, even if the INT_MSK_LINE [i] register bit is set to 0. When INT_MSK_STS [i] is set to 0, the associated interrupt number i is status enabled: An interrupt status is updated in the INT_STS [i] register. The interrupt may or may not be generated on the INT line, depending on the INT_MSK_LINE [i] configuration register bit.	R/W	0
6	INT_MSK_STS_06		R/W	0
5	INT_MSK_STS_05		R/W	0
4	INT_MSK_STS_04		R/W	0
3	INT_MSK_STS_03		R/W	0
2	INT_MSK_STS_02		R/W	0
1	INT_MSK_STS_01		R/W	0
0	INT_MSK_STS_00		R/W	0

2.17.8 INT_MSK_STS_B Register

Table 271. INT_MSK_STS_B

Address	Dec 215, Hex D7		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
INT_MSK_STS_15	INT_MSK_STS_14	INT_MSK_STS_13	INT_MSK_STS_12	INT_MSK_STS_11	INT_MSK_STS_10	INT_MSK_STS_09	INT_MSK_STS_08

Bits	Field Name	Description	Type	Reset
7	INT_MSK_STS_15	Status mask of interrupt number 8 to 15. When INT_MSK_STS [i] is set to 1, the associated interrupt number i is status masked, which means that no interrupt is stored in the INT_STS [i] status bit. Note that no interrupt number i is generated on the INT line, even if the INT_MSK_LINE [i] register bit is set to 0. When INT_MSK_STS [i] is set to 0, the associated interrupt number i is status enabled: An interrupt status is updated in the INT_STS [i] register. The interrupt may or may not be generated on the INT line, depending on the INT_MSK_LINE [i] configuration register bit.	R/W	0
6	INT_MSK_STS_14		R/W	0
5	INT_MSK_STS_13		R/W	0
4	INT_MSK_STS_12		R/W	0
3	INT_MSK_STS_11		R/W	0
2	INT_MSK_STS_10		R/W	0
1	INT_MSK_STS_09		R/W	0
0	INT_MSK_STS_08		R/W	0

2.17.9 INT_MSK_STS_C Register

Table 272. INT_MSK_STS_C

Address	Dec 216, Hex D8		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R/W		

7	6	5	4	3	2	1	0
INT_MSK_STS_23	INT_MSK_STS_22	INT_MSK_STS_21	INT_MSK_STS_20	INT_MSK_STS_19	INT_MSK_STS_18	INT_MSK_STS_17	INT_MSK_STS_16

Bits	Field Name	Description	Type	Reset
7	INT_MSK_STS_23	Status mask of interrupt number 16 to 23. When INT_MSK_STS [i] is set to 1, the associated interrupt number i is status masked, which means that no interrupt is stored in the INT_STS [i] status bit. Note that no interrupt number i is generated on the INT line, even if the INT_MSK_LINE [i] register bit is set to 0. When INT_MSK_STS [i] is set to 0, the associated interrupt number i is status enabled: An interrupt status is updated in the INT_STS [i] register. The interrupt may or may not be generated on the INT line, depending on the INT_MSK_LINE [i] configuration register bit.	R/W	0
6	INT_MSK_STS_22		R/W	0
5	INT_MSK_STS_21		R/W	0
4	INT_MSK_STS_20		R/W	0
3	INT_MSK_STS_19		R/W	0
2	INT_MSK_STS_18		R/W	0
1	INT_MSK_STS_17		R/W	0
0	INT_MSK_STS_16		R/W	0

Notes:

- All features not directly controlled by the power management FSM are managed by the TOGGLE and PWDNSTATUS registers.
- The TOGGLE registers include all those auxiliary features' enable and disable control bits.
- The PWDNSTATUS registers summarize the current activity status of each feature.
- Writing 1 in the S (Set) register bit enables the corresponding feature.
- Writing 1 in the R (Reset) register bit disables the corresponding feature.

2.17.10 TOGGLE1 Register

Table 273. TOGGLE1

Address	Dec 144, Hex 90		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	W		

7	6	5	4	3	2	1	0
FGDITHS	FGDITHR	FGS	FGR	GPADC_START_POLARITY	GPADC_SAMP_WINDOW	GPADCS	GPADCR

Bits	Field Name	Description	Type	Reset
7	FGDITHS	Writing 0: No effect Writing 1: FG DITH driver set signal (fuel gauge DITH digital enabled).	W	0
6	FGDITHR	Writing 0: No effect Writing 1: FG DITH driver reset signal (fuel gauge DITH digital disabled).	W	0
5	FGS	Writing 0: No effect Writing 1: FG driver set signal (fuel gauge digital enabled).	W	0
4	FGR	Writing 0: No effect Writing 1: FG driver reset signal (fuel gauge digital disabled).	W	0
3	GPADC_START_POLARITY	0: Start the GPADC RT conversion on a positive pulse (default). 1: Start the GPADC RT conversion on a negative pulse.	W	0
2	GPADC_SAMP_WINDOW	0: 3-µs sampling time window (default) 1: 450-µs sampling time window	W	0
1	GPADCS	Writing 0: No effect Writing 1: GPADC set signal (GPADC enabled).	W	0
0	GPADCR	Writing 0: No effect Writing 1: GPADC reset signal (GPADC disabled).	W	0

Note:

- GPADC_START is edge sensitive
- The FGHITHS bit is set to logical 1 to enable dithering in the ADC, which keeps idle tones from being generated with DC input value. Use the FGDITHR bit to disable the dithering. The dithering feature status is available in PWDNSTATUS1[5] .

2.17.11 TOGGLE2 Register

Table 274. TOGGLE2

Address	Dec 145, Hex 91		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type			

7	6	5	4	3	2	1	0
VIBS	VIBR	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7	VIBS	Writing 0: No effect Writing 1: Vibrator driver set signal (vibrator driver enabled).	W	0
6	VIBR	Writing 0: No effect Writing 1: Vibrator driver reset signal (vibrator driver disabled).	W	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	RESERVED	Reserved	R/W	0
0	RESERVED	Reserved	R/W	0

Notes:

- TOGGLE2 [1:0] are reserved bits with a R/W access.
- SW should not take care of the [1:0] returned bits values when reading this register.

2.17.12 TOGGLE3 Register

Table 275. TOGGLE3

Address	Dec 146, Hex 92		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	W		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	PWM2EN	PWM2S	PWM2R	PWM1EN	PWM1S	PWM1R

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	PWM2EN	0: PWM2 clock disabled 1: PWM2 clock enabled	W	0
4	PWM2S	Writing 0: No effect Writing 1: PWM2 set driver signal	W	0
3	PWM2R	Writing 0: No effect Writing 1: PWM2 reset driver signal	W	0
2	PWM1EN	0: PWM1 clock disabled 1: PWM1 clock enabled	W	0
1	PWM1S	Writing 0: No effect Writing 1: PWM1 set driver signal	W	0
0	PWM1R	Writing 0: No effect Writing 1: PWM1 reset driver signal	W	0

2.17.13 PWDNSTATUS1 Register

Table 276. PWDNSTATUS1

Address	Dec 147, Hex 93		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	FGDITH_EN	FG_EN	RESERVED	RESERVED	VIB_EN	GPADC_EN

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	FGDITH_EN	Fuel gauge dithering feature status 0: Dithering feature disabled 1: Dithering feature enabled	R	0
4	FG_EN	Fuel gauge status 0: Fuel gauge disabled 1: Fuel gauge enabled and running	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	VIB_EN	Vibrator driver status 0: Vibrator driver disabled 1: Vibrator driver enabled	R	0
0	GPADC_EN	GPADC status 0: GPADC disabled 1: GPADC enabled	R	0

Notes:

- PWDNSTATUS1 [2] is a reserved bit, not fixed at 0.
- SW should not take care of the [0] returned bit value when reading this register.

2.17.14 PWDNSTATUS2 Register

Table 277. PWDNSTATUS2

Address	Dec 148, Hex 94		
Physical Address	ID2 = 49h	**Instance**	State Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	START_POLARITY_STS	SAMP_WINDOW_STS	PWM2_CLK_EN	PWM2_STS	PWM1_CLK_EN	PWM1_STS

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	START_POLARITY_STS	0: Positive pulse (default), edge sensitive 1: Negative pulse, edge sensitive	R	0
4	SAMP_WINDOW_STS	0: 3-µs sampling time window (default) 1: 450-µs sampling time window	R	0
3	PWM2_CLK_EN	PWM2 clock driver enable status (active high)	R	0
2	PWM2_STS	PWM2 length (active high)	R	0
1	PWM1_CLK_EN	PWM1 clock driver enable status (active high)	R	0
0	PWM1_STS	PWM1 length (active high)	R	0

The following registers are located in the Memory Register Map section, Section 1.2.3.

2.17.15 VALIDITY0 Register

Table 278. VALIDITY0

Address	Dec 23, Hex 17		
Physical Address	ID2 = 48h	**Instance**	Backup Domain
Description	Secured (MSECURE) registers under backup domain to store sensitive data.		
Type	R/W		

7	6	5	4	3	2	1	0
BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_2	BIT_1

Bits	Field Name	Description	Type	Reset
7	BIT_7	Validity memory	R/W	0
6	BIT_6		R/W	0
5	BIT_5		R/W	0
4	BIT_4		R/W	0
3	BIT_3		R/W	0
2	BIT_2		R/W	0
1	BIT_1		R/W	0
0	BIT_0		R/W	0

2.17.16 VALIDITY1 Register

Table 279. VALIDITY1

Address	Dec 24, Hex 18		
Physical Address	ID2 = 48h	**Instance**	Backup Domain
Description	Secured (MSECURE) registers under backup domain to store sensitive data.		
Type	R/W		

7	6	5	4	3	2	1	0
BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_2	BIT_1

Bits	Field Name	Description	Type	Reset
7	BIT_7	Validity memory	R/W	0
6	BIT_6		R/W	0
5	BIT_5		R/W	0
4	BIT_4		R/W	0
3	BIT_3		R/W	0
2	BIT_2		R/W	0
1	BIT_1		R/W	0
0	BIT_0		R/W	0

2.17.17 VALIDITY2 Register

Table 280. VALIDITY2

Address	Dec 25, Hex 19		
Physical Address	ID2 = 48h	**Instance**	Backup Domain
Description	Secured (MSECURE) registers under backup domain to store sensitive data.		
Type	R/W		

7	6	5	4	3	2	1	0
BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_2	BIT_1

Bits	Field Name	Description	Type	Reset
7	BIT_7	Validity memory	R/W	0
6	BIT_6		R/W	0
5	BIT_5		R/W	0
4	BIT_4		R/W	0
3	BIT_3		R/W	0
2	BIT_2		R/W	0
1	BIT_1		R/W	0
0	BIT_0		R/W	0

2.17.18 VALIDITY3 Register

Table 281. VALIDITY3

Address	Dec 26, Hex 1A		
Physical Address	ID2 = 48h	**Instance**	Backup Domain
Description	Secured (MSECURE) registers under backup domain to store sensitive data.		
Type	R/W		

7	6	5	4	3	2	1	0
BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_2	BIT_1

Bits	Field Name	Description	Type	Reset
7	BIT_7	Validity memory	R/W	0
6	BIT_6		R/W	0
5	BIT_5		R/W	0
4	BIT_4		R/W	0
3	BIT_3		R/W	0
2	BIT_2		R/W	0
1	BIT_1		R/W	0
0	BIT_0		R/W	0

2.17.19 VALIDITY4 Register

Table 282. VALIDITY4

Address	Dec 27, Hex 1B		
Physical Address	ID2 = 48h	**Instance**	Backup Domain
Description	Secured (MSECURE) registers under backup domain to store sensitive data.		
Type	R/W		

7	6	5	4	3	2	1	0
BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_2	BIT_1

Bits	Field Name	Description	Type	Reset
7	BIT_7	Validity memory	R/W	0
6	BIT_6		R/W	0
5	BIT_5		R/W	0
4	BIT_4		R/W	0
3	BIT_3		R/W	0
2	BIT_2		R/W	0
1	BIT_1		R/W	0
0	BIT_0		R/W	0

2.17.20 VALIDITY5 Register

Table 283. VALIDITY5

Address	Dec 28, Hex 1C		
Physical Address	ID2 = 48h	**Instance**	Backup Domain
Description	Secured (MSECURE) registers under backup domain to store sensitive data.		
Type	R/W		

7	6	5	4	3	2	1	0
BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_2	BIT_1

Bits	Field Name	Description	Type	Reset
7	BIT_7	Validity memory	R/W	0
6	BIT_6		R/W	0
5	BIT_5		R/W	0
4	BIT_4		R/W	0
3	BIT_3		R/W	0
2	BIT_2		R/W	0
1	BIT_1		R/W	0
0	BIT_0		R/W	0

2.17.21 VALIDITY6 Register

Table 284. VALIDITY6

Address	Dec 29, Hex 1D		
Physical Address	ID2 = 48h	**Instance**	Backup Domain
Description	Secured (MSECURE) registers under backup domain to store sensitive data.		
Type	R/W		

7	6	5	4	3	2	1	0
BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_2	BIT_1

Bits	Field Name	Description	Type	Reset
7	BIT_7	Validity memory	R/W	0
6	BIT_6		R/W	0
5	BIT_5		R/W	0
4	BIT_4		R/W	0
3	BIT_3		R/W	0
2	BIT_2		R/W	0
1	BIT_1		R/W	0
0	BIT_0		R/W	0

2.17.22 VALIDITY7 Register

Table 285. VALIDITY7

Address	Dec 30, Hex 1E		
Physical Address	ID2 = 48h	**Instance**	Backup Domain
Description	Secured (MSECURE) registers under backup domain to store sensitive data.		
Type	R/W		

7	6	5	4	3	2	1	0
BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_2	BIT_1

Bits	Field Name	Description	Type	Reset
7	BIT_7	Validity memory	R/W	0
6	BIT_6		R/W	0
5	BIT_5		R/W	0
4	BIT_4		R/W	0
3	BIT_3		R/W	0
2	BIT_2		R/W	0
1	BIT_1		R/W	0
0	BIT_0		R/W	0

2.17.23 VALIDITY8 Register

Table 286. VALIDITY8

Address	Dec 53, Hex 35		
Physical Address	ID2 = 48h	**Instance**	Backup Domain
Description	Secured (MSECURE) registers under backup domain to store sensitive data.		
Type	R/W		

7	6	5	4	3	2	1	0
BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_2	BIT_1

Bits	Field Name	Description	Type	Reset
7	BIT_7	Validity memory	R/W	0
6	BIT_6		R/W	0
5	BIT_5		R/W	0
4	BIT_4		R/W	0
3	BIT_3		R/W	0
2	BIT_2		R/W	0
1	BIT_1		R/W	0
0	BIT_0		R/W	0

2.17.24 VALIDITY9 Register

Table 287. VALIDITY9

Address	Dec 54, Hex 36		
Physical Address	ID2 = 48h	**Instance**	Backup Domain
Description	Secured (MSECURE) registers under backup domain to store sensitive data.		
Type	R/W		

7	6	5	4	3	2	1	0
BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_2	BIT_1

Bits	Field Name	Description	Type	Reset
7	BIT_7	Validity memory	R/W	0
6	BIT_6		R/W	0
5	BIT_5		R/W	0
4	BIT_4		R/W	0
3	BIT_3		R/W	0
2	BIT_2		R/W	0
1	BIT_1		R/W	0
0	BIT_0		R/W	0

2.17.25 VALIDITY10 Register

Table 288. VALIDITY10

Address	Dec 55, Hex 37		
Physical Address	ID2 = 48h	**Instance**	Backup Domain
Description	Secured (MSECURE) registers under backup domain to store sensitive data.		
Type	R/W		

7	6	5	4	3	2	1	0
BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_2	BIT_1

Bits	Field Name	Description	Type	Reset
7	BIT_7	Validity memory	R/W	0
6	BIT_6		R/W	0
5	BIT_5		R/W	0
4	BIT_4		R/W	0
3	BIT_3		R/W	0
2	BIT_2		R/W	0
1	BIT_1		R/W	0
0	BIT_0		R/W	0

2.17.26 VALIDITY11 Register

Table 289. VALIDITY11

Address	Dec 56, Hex 38		
Physical Address	ID2 = 48h	**Instance**	Backup Domain
Description	Secured (MSECURE) registers under backup domain to store sensitive data.		
Type	R/W		

7	6	5	4	3	2	1	0
BIT_7	BIT_6	BIT_5	BIT_4	BIT_3	BIT_2	BIT_2	BIT_1

Bits	Field Name	Description	Type	Reset
7	BIT_7	Validity memory	R/W	0
6	BIT_6		R/W	0
5	BIT_5		R/W	0
4	BIT_4		R/W	0
3	BIT_3		R/W	0
2	BIT_2		R/W	0
1	BIT_1		R/W	0
0	BIT_0		R/W	0

2.18 Test

2.18.1 JTAGVERNUM Register

Table 290. JTAGVERNUM

Address	Dec 135, Hex 87		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	VERNUM_3	VERNUM_2	VERNUM_1	VERNUM_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	-	-
6	RESERVED	Reserved	-	-
5	RESERVED	Reserved	-	-
4	RESERVED	Reserved	-	-
3	VERNUM_3	Value depending on silicon version number 0000 - ES Revision 1.0 0001 - ES Revision 1.1 0010 - ES Revision 1.2	R	X
2	VERNUM_2		R	X
1	VERNUM_1		R	X
0	VERNUM_0		R	X

2.18.2 EPROM_REV Register

Table 291. EPROM_REV

Address	Dec 223, Hex DF		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
EPROM-REVISION_7	EPROM-REVISION_6	EPROM-REVISION_5	EPROM-REVISION_4	EPROM-REVISION_3	EPROM-REVISION_2	EPROM-REVISION_1	EPROM-REVISION_0

Bits	Field Name	Description	Type	Reset
7	EPROM-REVISION_7	Returned value is the EPROM revision number, corresponding to an EPROM name. LSB(EPROM-REVISION_[3:0]) corresponds to the EPROM name LSB MSB(EPROM-REVISION_[7:4]) is a coded register. MSB=2 corresponds to an EPROM named MSB=A, register MSB=3 correspond to an EPROM named MSB=B, ... Example: EPROM-REVISION_[7:0]=0x77 → EPROM name is F7	R	X
6	EPROM-REVISION_6		R	X
5	EPROM-REVISION_5		R	X
4	EPROM-REVISION_4		R	X
3	EPROM-REVISION_3		R	X
2	EPROM-REVISION_2		R	X
1	EPROM-REVISION_1		R	X
0	EPROM-REVISION_0		R	X

2.19 GPADC Trimming Bits™

2.19.1 GPADC_TRIM1 Register

Table 292. GPADC_TRIM1

Address	Dec 205, Hex CD		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	GPADC_TRIM1_2	GPADC_TRIM1_1	GPADC_TRIM1_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	GPADC_TRIM1_2	GPADC gain and offset compensation	R	EPROM
1	GPADC_TRIM1_1		R	EPROM
0	GPADC_TRIM1_0		R	EPROM

2.19.2 GPADC_TRIM2 Register

Table 293. GPADC_TRIM2

Address	Dec 206, Hex CE		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	GPADC_TRIM2_2	GPADC_TRIM2_1	GPADC_TRIM2_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	GPADC_TRIM2_2	GPADC gain and offset compensation	R	EPROM
1	GPADC_TRIM2_1		R	EPROM
0	GPADC_TRIM2_0		R	EPROM

2.19.3 GPADC_TRIM3 Register

Table 294. GPADC_TRIM3

Address	Dec 207, Hex CF		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	GPADC_TRIM3_4	GPADC_TRIM3_3	GPADC_TRIM3_2	GPADC_TRIM3_1	GPADC_TRIM3_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	GPADC_TRIM3_4	GPADC gain and offset compensation	R	EPROM
3	GPADC_TRIM3_3		R	EPROM
2	GPADC_TRIM3_2		R	EPROM
1	GPADC_TRIM3_1		R	EPROM
0	GPADC_TRIM3_0		R	EPROM

2.19.4 GPADC_TRIM4 Register

Table 295. GPADC_TRIM4

Address	Dec 208, Hex D0		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	GPADC_TRIM4_5	GPADC_TRIM4_4	GPADC_TRIM4_3	GPADC_TRIM4_2	GPADC_TRIM4_1	GPADC_TRIM4_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	GPADC_TRIM4_5	GPADC gain and offset compensation	R	EPROM
4	GPADC_TRIM4_4		R	EPROM
3	GPADC_TRIM4_3		R	EPROM
2	GPADC_TRIM4_2		R	EPROM
1	GPADC_TRIM4_1		R	EPROM
0	GPADC_TRIM4_0		R	EPROM

2.19.5 GPADC_TRIM5 Register

Table 296. GPADC_TRIM5

Address	Dec 209, Hex D1		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	GPADC_TRIM5_6	GPADC_TRIM5_5	GPADC_TRIM5_4	GPADC_TRIM5_3	GPADC_TRIM5_2	GPADC_TRIM5_1	GPADC_TRIM5_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	GPADC_TRIM5_6	GPADC gain and offset compensation	R	EPROM
5	GPADC_TRIM5_5		R	EPROM
4	GPADC_TRIM5_4		R	EPROM
3	GPADC_TRIM5_3		R	EPROM
2	GPADC_TRIM5_2		R	EPROM
1	GPADC_TRIM5_1		R	EPROM
0	GPADC_TRIM5_0		R	EPROM

2.19.6 GPADC_TRIM6 Register

Table 297. GPADC_TRIM6

Address	Dec 210, Hex D2		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	GPADC_TRIM6_6	GPADC_TRIM6_5	GPADC_TRIM6_4	GPADC_TRIM6_3	GPADC_TRIM6_2	GPADC_TRIM6_1	GPADC_TRIM6_0

Bits	Field Name	Description	Type	Reset
7	GPADC_TRIM6_7	GPADC gain and offset compensation	R	EPROM
6	GPADC_TRIM6_6		R	EPROM
5	GPADC_TRIM6_5		R	EPROM
4	GPADC_TRIM6_4		R	EPROM
3	GPADC_TRIM6_3		R	EPROM
2	GPADC_TRIM6_2		R	EPROM
1	GPADC_TRIM6_1		R	EPROM
0	GPADC_TRIM6_0		R	EPROM

2.19.7 GPADC_TRIM7 Register

Table 298. GPADC_TRIM7

Address	Dec 211, Hex D3		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	GPADC_TRIM7_4	GPADC_TRIM7_3	GPADC_TRIM7_2	GPADC_TRIM7_1	GPADC_TRIM7_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	GPADC_TRIM7_4	GPADC gain and offset compensation	R	EPROM
3	GPADC_TRIM7_3		R	EPROM
2	GPADC_TRIM7_2		R	EPROM
1	GPADC_TRIM7_1		R	EPROM
0	GPADC_TRIM7_0		R	EPROM

2.19.8 GPADC_TRIM8 Register

Table 299. GPADC_TRIM8

Address	Dec 212, Hex D4		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	GPADC_TRIM8_4	GPADC_TRIM8_3	GPADC_TRIM8_2	GPADC_TRIM8_1	GPADC_TRIM8_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	GPADC_TRIM8_4	GPADC gain and offset compensation	R	EPROM
3	GPADC_TRIM8_3		R	EPROM
2	GPADC_TRIM8_2		R	EPROM
1	GPADC_TRIM8_1		R	EPROM
0	GPADC_TRIM8_0		R	EPROM

2.19.9 GPADC_TRIM9 Register

Table 300. GPADC_TRIM9

Address	Dec 213, Hex D5		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	GPADC_TRIM9_3	GPADC_TRIM9_2	GPADC_TRIM9_1	GPADC_TRIM9_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	GRESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	GPADC_TRIM9_3	GPADC gain and offset compensation	R	EPROM
2	GPADC_TRIM9_2		R	EPROM
1	GPADC_TRIM9_1		R	EPROM
0	GPADC_TRIM9_0		R	EPROM

2.19.10 GPADC_TRIM10 Register

Table 301. GPADC_TRIM10

Address	Dec 214, Hex D6		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	GPADC_TRIM10_4	GPADC_TRIM10_3	GPADC_TRIM10_2	GPADC_TRIM10_1	GPADC_TRIM10_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	GPADC_TRIM10_4	GPADC gain and offset compensation	R	EPROM
3	GPADC_TRIM10_3		R	EPROM
2	GPADC_TRIM10_2		R	EPROM
1	GPADC_TRIM10_1		R	EPROM
0	GPADC_TRIM10_0		R	EPROM

2.19.11 GPADC_TRIM11 Register

Table 302. GPADC_TRIM11

Address	Dec 215, Hex D7		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	GPADC_TRIM11_3	GPADC_TRIM11_2	GPADC_TRIM11_1	GPADC_TRIM11_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	GRESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	GPADC_TRIM11_3	GPADC gain and offset compensation	R	EPROM
2	GPADC_TRIM11_2		R	EPROM
1	GPADC_TRIM11_1		R	EPROM
0	GPADC_TRIM11_0		R	EPROM

2.19.12 GPADC_TRIM12 Register

Table 303. GPADC_TRIM12

Address	Dec 216, Hex D8		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	GPADC_TRIM12_4	GPADC_TRIM12_3	GPADC_TRIM12_2	GPADC_TRIM12_1	GPADC_TRIM12_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	GPADC_TRIM12_4	GPADC gain and offset compensation	R	EPROM
3	GPADC_TRIM12_3		R	EPROM
2	GPADC_TRIM12_2		R	EPROM
1	GPADC_TRIM12_1		R	EPROM
0	GPADC_TRIM12_0		R	EPROM

2.19.13 GPADC_TRIM13 Register

Table 304. GPADC_TRIM13

Address	Dec 217, Hex D9		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	GPADC_TRIM13_3	GPADC_TRIM13_2	GPADC_TRIM13_1	GPADC_TRIM13_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	GRESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	GPADC_TRIM13_3	GPADC gain and offset compensation	R	EPROM
2	GPADC_TRIM13_2		R	EPROM
1	GPADC_TRIM13_1		R	EPROM
0	GPADC_TRIM13_0		R	EPROM

2.19.14 GPADC_TRIM14 Register

Table 305. GPADC_TRIM14

Address	Dec 218, Hex DA		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	GPADC_TRIM14_4	GPADC_TRIM14_3	GPADC_TRIM14_2	GPADC_TRIM14_1	GPADC_TRIM14_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	GPADC_TRIM14_4	GPADC gain and offset compensation	R	EPROM
3	GPADC_TRIM14_3		R	EPROM
2	GPADC_TRIM14_2		R	EPROM
1	GPADC_TRIM14_1		R	EPROM
0	GPADC_TRIM14_0		R	EPROM

2.19.15 GPADC_TRIM15 Register

Table 306. GPADC_TRIM15

Address	Dec 219, Hex DB		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	GPADC_TRIM15_3	GPADC_TRIM15_2	GPADC_TRIM15_1	GPADC_TRIM15_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	GRESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	GPADC_TRIM15_3	GPADC gain and offset compensation	R	EPROM
2	GPADC_TRIM15_2		R	EPROM
1	GPADC_TRIM15_1		R	EPROM
0	GPADC_TRIM15_0		R	EPROM

2.19.16 GPADC_TRIM16 Register

Table 307. GPADC_TRIM16

Address	Dec 220, Hex DC		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	GPADC_TRIM16_4	GPADC_TRIM16_3	GPADC_TRIM16_2	GPADC_TRIM16_1	GPADC_TRIM16_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	GPADC_TRIM16_4	GPADC gain and offset compensation	R	EPROM
3	GPADC_TRIM16_3		R	EPROM
2	GPADC_TRIM16_2		R	EPROM
1	GPADC_TRIM16_1		R	EPROM
0	GPADC_TRIM16_0		R	EPROM

2.19.17 GPADC_TRIM17 Register

Table 308. GPADC_TRIM17

Address	Dec 221, Hex DD		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RATIO_TLO_2	RATIO_TLO_1	RATIO_TLO_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RATIO_TLO_2	Battery temperature measurement: Low-temperature threshold ratio: 000: 0.2 x VREF 001: 0.3 x VREF	R	EPROM
1	RATIO_TLO_1	010: 0.4 x VREF 011: 0.5 x VREF (60°C) 100: 0.6 x VREF	R	EPROM
0	RATIO_TLO_0	101: 0.7 x VREF 110: 0.8 x VREF 111: 0.9 x VREF (0°C)	R	EPROM

2.19.18 GPADC_TRIM18 Register

Table 309. GPADC_TRIM18

Address	Dec 222, Hex DE		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RATIO_THI_2	RATIO_THI_1	RATIO_THI_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RATIO_THI_2	Battery temperature measurement: High-temperature threshold ratio: 000: 0.1 x VREF 001: 0.2 x VREF	R	EPROM
1	RATIO_THI_1	010: 0.3 x VREF 011: 0.4 x VREF (60°C) 100: 0.5 x VREF	R	EPROM
0	RATIO_THI_0	101: 0.6 x VREF 110: 0.7 x VREF 111: 0.8 x VREF (10°C)	R	EPROM

2.19.19 GPADC_TRIM19 Register

Table 310. GPADC_TRIM19

Address	Dec 253, Hex FD		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	GPADC_TRIM19_0

Bits	Field Name	Description	Type	Reset
7	RESERVED	Reserved	R	0
6	RESERVED	Reserved	R	0
5	RESERVED	Reserved	R	0
4	RESERVED	Reserved	R	0
3	RESERVED	Reserved	R	0
2	RESERVED	Reserved	R	0
1	RESERVED	Reserved	R	0
0	GPADC_TRIM19_0	GPADC gain and offset compensation	R	EPROM

2.19.20 GPADC_TRIM20 Register

Table 311. GPADC_TRIM20

Address	Dec 254, Hex FE		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
GPADC_TRIM20_7	GPADC_TRIM20_6	GPADC_TRIM20_5	GPADC_TRIM20_4	GPADC_TRIM20_3	GPADC_TRIM20_2	GPADC_TRIM20_1	GPADC_TRIM20_0

Bits	Field Name	Description	Type	Reset
7	GPADC_TRIM20_7	GPADC gain and offset compensation	R	EPROM
6	GPADC_TRIM20_6		R	EPROM
5	GPADC_TRIM20_5		R	EPROM
4	GPADC_TRIM20_4		R	EPROM
3	GPADC_TRIM20_3		R	EPROM
2	GPADC_TRIM20_2		R	EPROM
1	GPADC_TRIM20_1		R	EPROM
0	GPADC_TRIM20_0		R	EPROM

2.19.21 GPADC_TRIM21 Register

Table 312. GPADC_TRIM21

Address	Dec 255, Hex FF		
Physical Address	ID3 = 4Ah	**Instance**	Backup Domain
Description			
Type	R		

7	6	5	4	3	2	1	0
GPADC_TRIM21_7	GPADC_TRIM21_6	GPADC_TRIM21_5	GPADC_TRIM21_4	GPADC_TRIM21_3	GPADC_TRIM21_2	GPADC_TRIM21_1	GPADC_TRIM21_0

Bits	Field Name	Description	Type	Reset
7	GPADC_TRIM21_7	GPADC gain and offset compensation	R	EPROM
6	GPADC_TRIM21_6		R	EPROM
5	GPADC_TRIM21_5		R	EPROM
4	GPADC_TRIM21_4		R	EPROM
3	GPADC_TRIM21_3		R	EPROM
2	GPADC_TRIM21_2		R	EPROM
1	GPADC_TRIM21_1		R	EPROM
0	GPADC_TRIM21_0		R	EPROM

3 Revision History

The following table summarizes the TPS80032 ES1.1 and ES1.2 Register Map versions.

Note: Numbering may vary from previous verisons.

Version	Literature Number	Date	Notes
*	SWCU096	November 2011	See (1)
A	SWCU096A	February 2012	See (2)
B	SWCU096B	August 2012	See (3)
C	SWCU096C	November 2014	See (4)

(1) TPS80032 ES1.1 Register Map, (SWCU096) - initial release.

(2) TPS80032 ES1.1 Register Map, (SWCU096A):
- Section 2.15.1 and Section 2.15.3 - Update bit 3:0 description, code 000 is 31.25 µs
- Section 2.3.4 - Update FALLBACK bit description.
- Section 2.17.10 - Replace 16.5 µs by 3 µs in TOGGLE1[2] description
- Section 2.17.14 - Replace 16.5 µs by 3 µs in PWDNSTATUS2[4] description
- Section 2.17.13 - PWDNSTATUS1 bit 0 description updated.
- Table 263 - Update Interrupts Mapping table
- Table 2 and Section 2.5.7- Change SMPS5_CFG_VOLTAGE I2C address from ID1=48h to ID0=12h
- Section 2.11.5 - Add accurate descriptions in LINEAR_CHRG_STS register
- Table 25 and Section 2.11.22 - Change ANTICOLLAPSE_CTRL1 ID I2C address from ID1=48h to ID2=49h
- Section 2.15.2 - Update SIMCTRL SW_FC description
- Section 2.15.4 - Update MMCCTRL SW_FC description
- Section 2.3.5 - Change VSYSMIN_LO_THRESHOLD description
- Fix Tablenotes that were not under the correct table.

(3) TPS80032 ES1.1 and ES1.2 Register Map, (SWCU096B):
- Section 2.11.4-Fix register address issue
- Section 2.18.1- Add ES1.2 code
- Section 2.18.2- Update description
- Section 2.11.7- Add Table Note
- Section 2.11.16- Update BST_HW_PR_DIS description for ES1.2
- Section 2.11.16- Add GSMCAL_PRESET bit for ES1.2
- Section 2.11.22- Update BUCK_VTH_[2:0] Reset value for ES1.2
- Section 2.5- Remove Note
- Table 103Replace minimum value by typical value and add a table note for LDOUSB.

(4) TPS80032 ES1.1 and ES1.2 Register Map, (SWCU096C): Released to web.

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