Major Component Product Pages

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TI 66AK2L06 JESD Attach to Wideband ADCs and DACs

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Revision History

Revision	Notes
Rev 1.0	Initial revision release

Orderable: EVM_orderable	Designed for: Public Release	Mod. Date: 4/15/2015
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Number: TIDEP0034 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 1 of 35
Drawn By:	File: CoverSheet_01.SchDoc	Size: B
Engineer: a0271760	Contact: http://www.ti.com/support	

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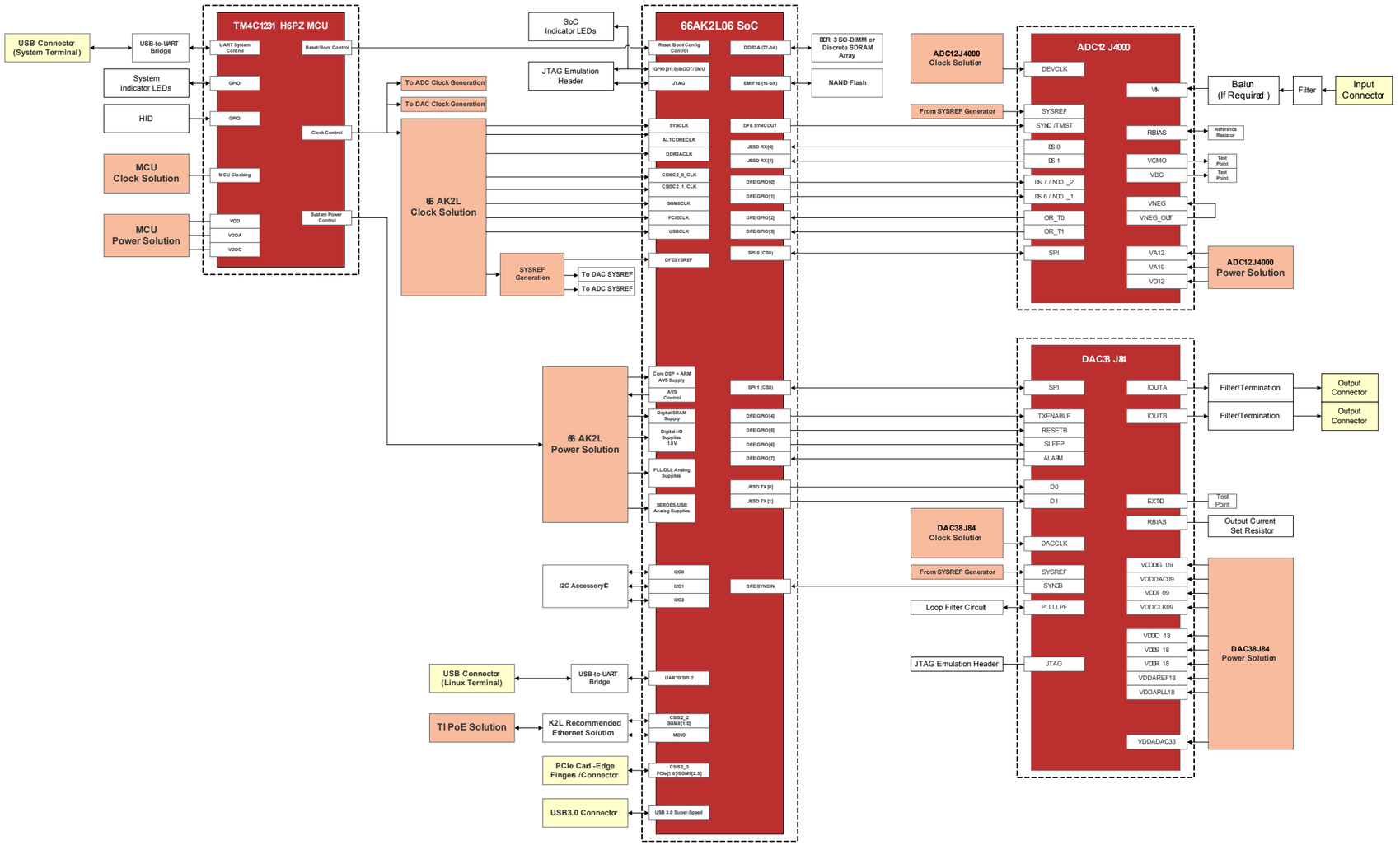

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Drawn By: a0271760		File: system_diagram.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

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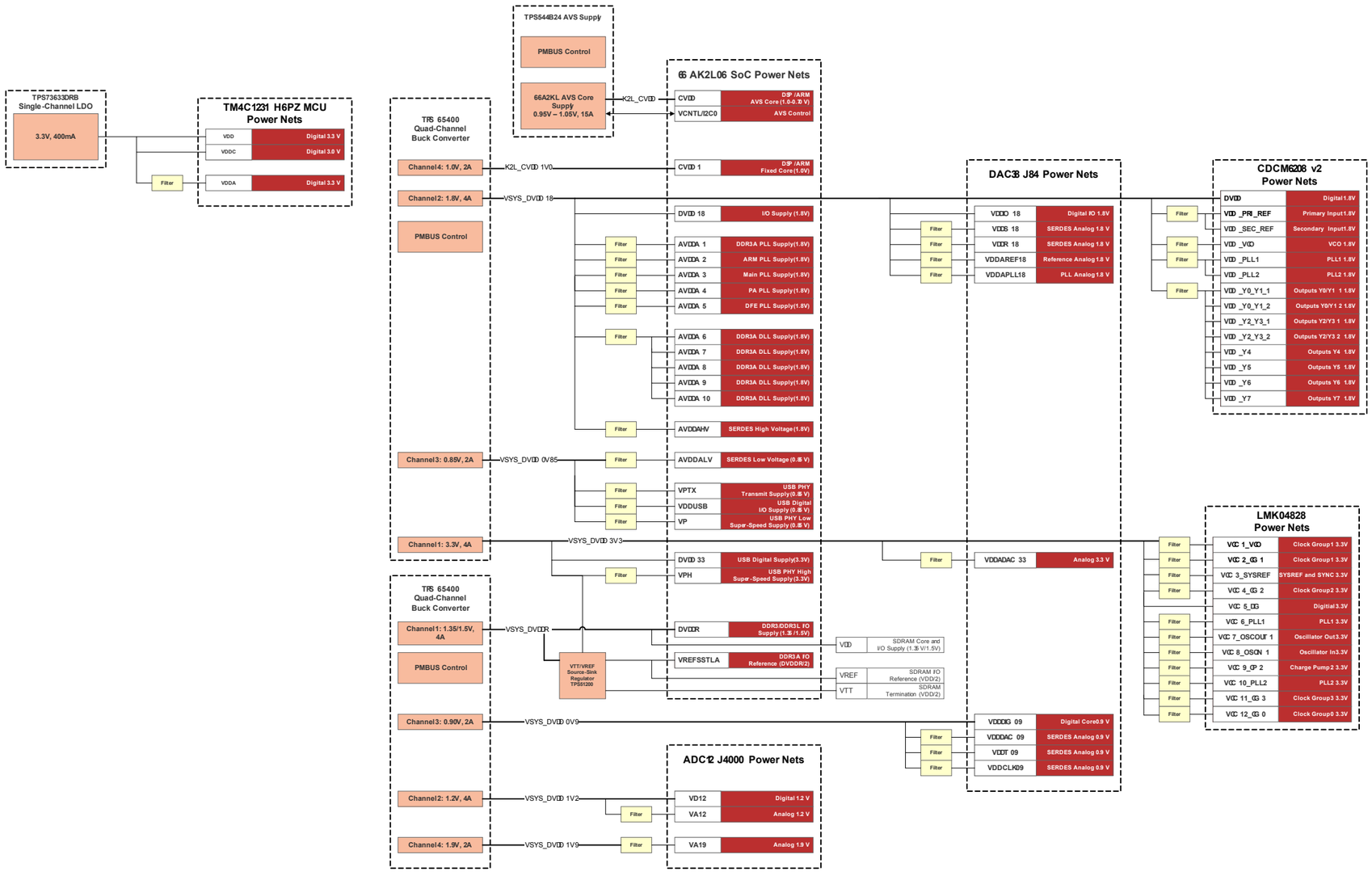

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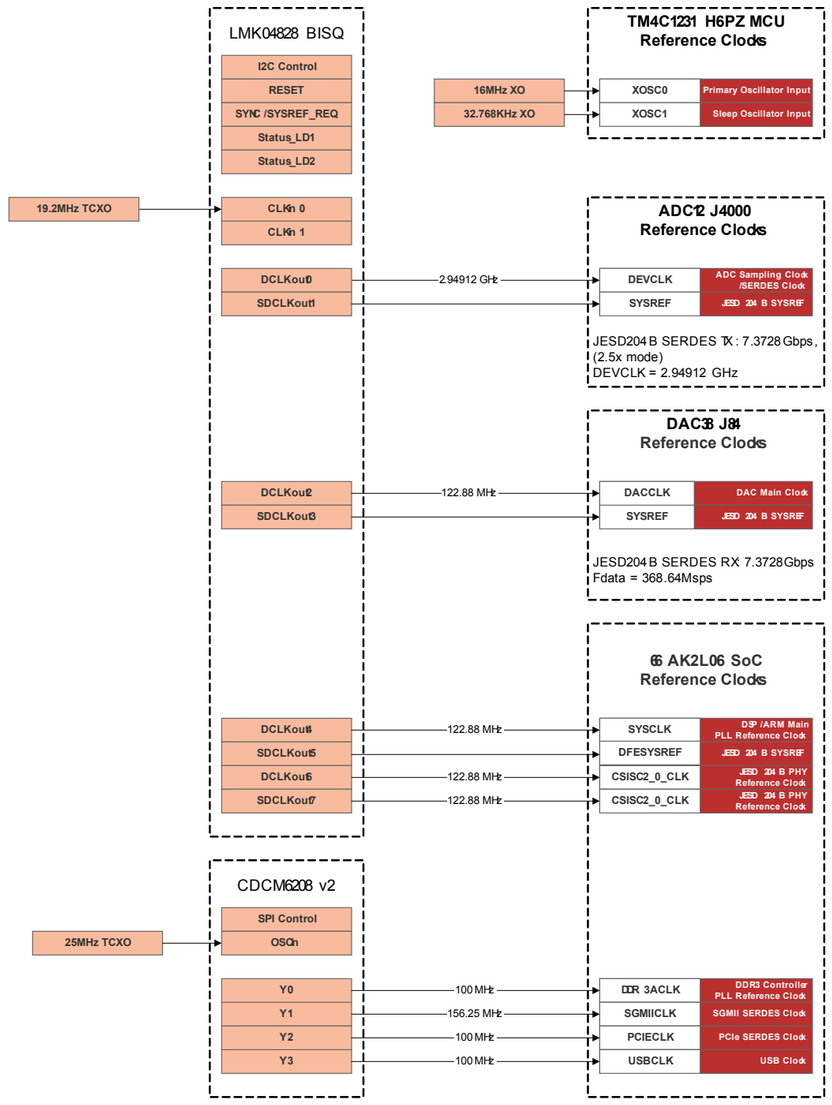
Engineer: a0271760		Contact: http://www.ti.com/support	



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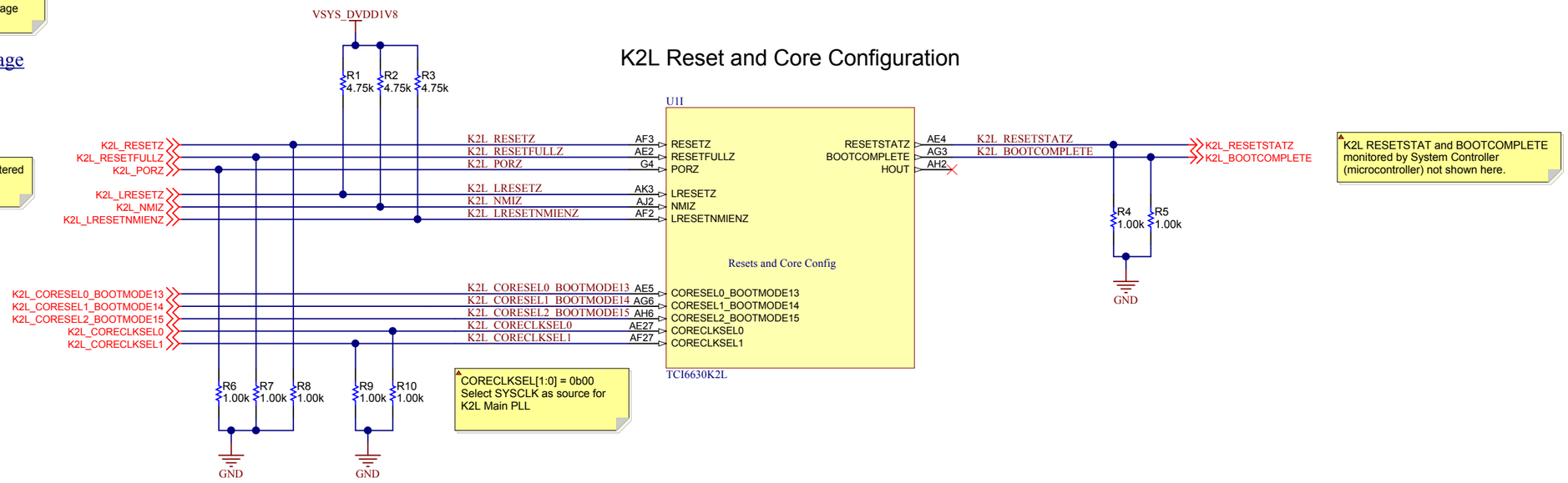
For schematic and layout recommendations and requirements see the K2L product page linked below.

TI 66AK2L06 Product Page

K2L BOOTMODE and RESET pins mastered by Board Mangement Controller (microcontroller) not shown here.

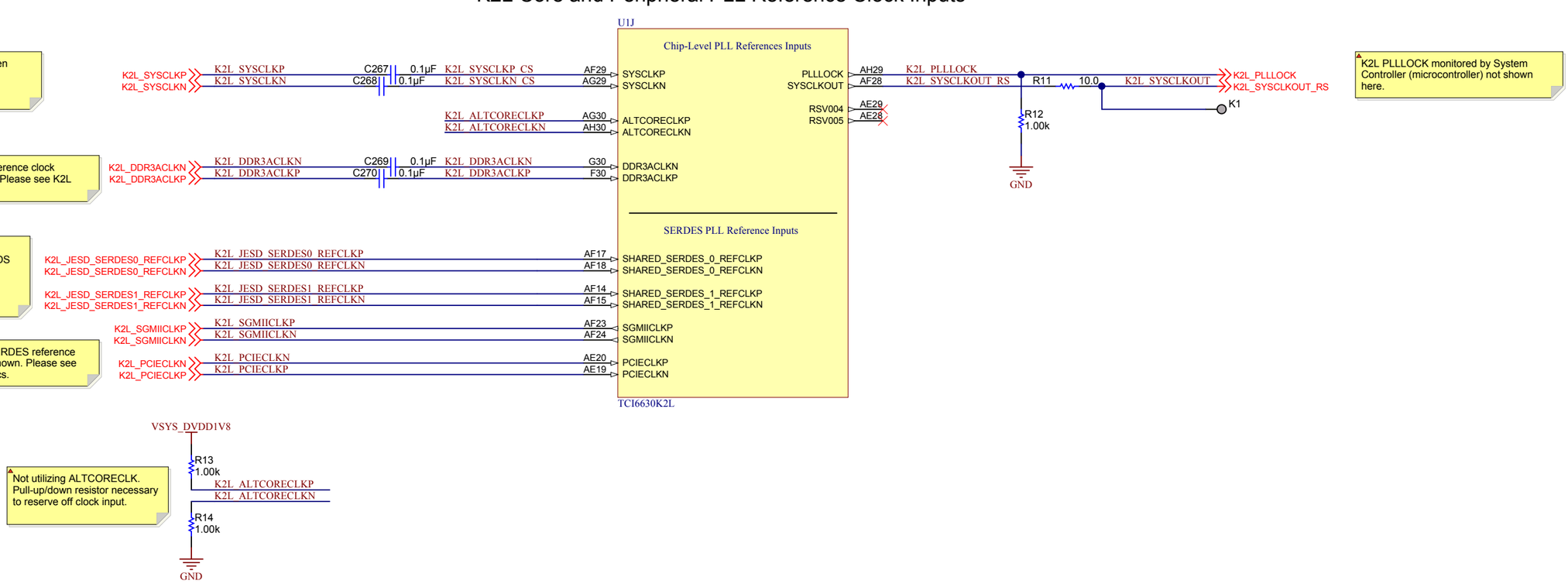
K2L Reset and Core Configuration



K2L RESETSTAT and BOOTCOMPLETE monitored by System Controller (microcontroller) not shown here.

CORECLKSEL[1:0] = 0b00
Select SYSCLK as source for K2L Main PLL

K2L Core and Peripheral PLL Reference Clock Inputs



K2L SYSCLK sourced my LMK04828. When utilizing LVDS outputs of LMK04828 only AC-coupling is necessary.

K2L PLLLOCK monitored by System Controller (microcontroller) not shown here.

DDR3 controller reference clock solution not shown. Please see K2L EVM schematics.

K2L JESD SERDES0/1 reference clock sourced my LMK04828. When utilizing LVDS outputs of LMK04828 no AC-coupling or external bias or termination network is necessary.

SGMII and PCIe SERDES reference clock solution not shown. Please see K2L EVM schematics.

Not utilizing ALTCORECLK. Pull-up/down resistor necessary to reserve off clock input.

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Engineer: a0271760	Contact: http://www.ti.com/support	

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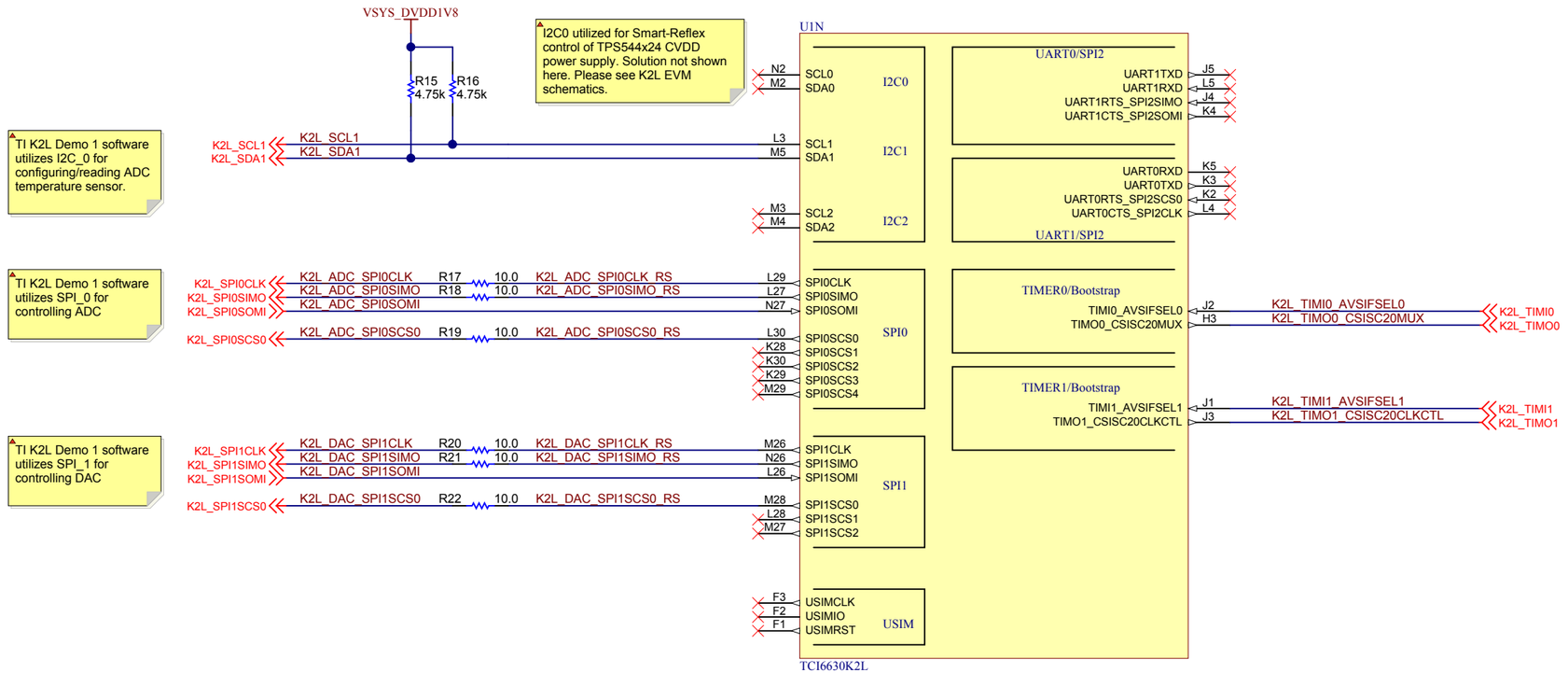
K2L Boot-Config, I2C, SPI, UART, Timer, and USIM



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Engineer: a0271760	Contact: http://www.ti.com/support	

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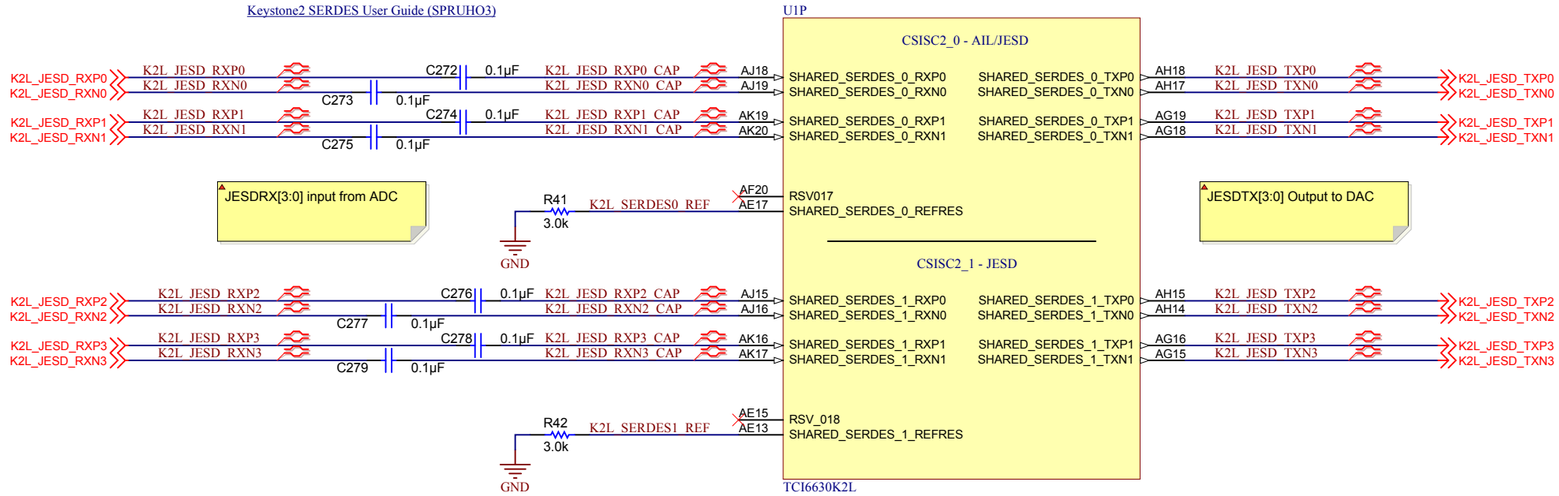
For schematic and layout recommendations and requirements see the K2L product page linked below.

TI 66AK2L06 Product Page

JESD204B SERDES shall be routed according to routing rules specified in the Keystone 2 SERDES User Guide (SPRUH03)

Keystone2 SERDES User Guide (SPRUHO3)

DFE JESD204B SERDES



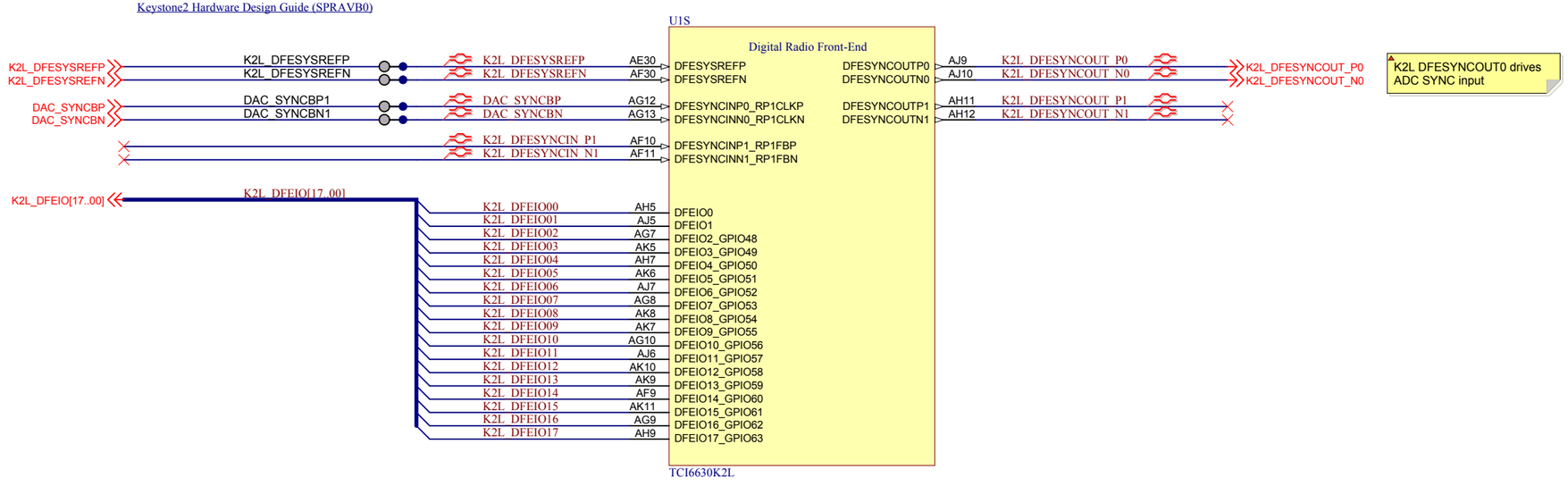
JESD204B SYSREF and SYNC shall be utilized according to DFE User Guide (SPRUHX8) and routed according to Keystone 2 Hardware Design Guide (SPRAVB0) DFE peripheral section.

Keystone2 Hardware Design Guide (SPRAVB0)

DFE JESD204B SYSREF, SYNCIN/OUT and DFE I/O

K2L SYSREF driven by LMK04828

K2L DFESYNCIN0 driven by DAC SYNC output



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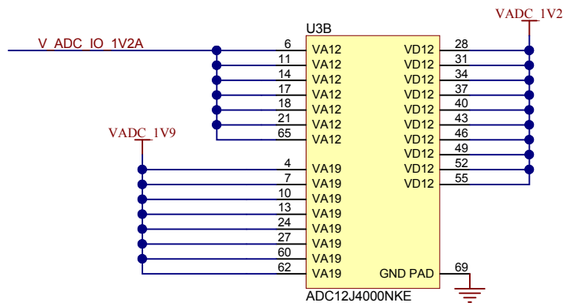
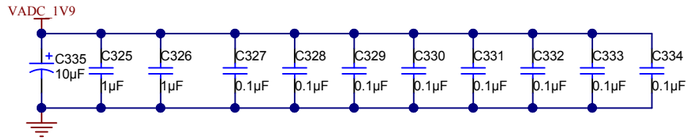
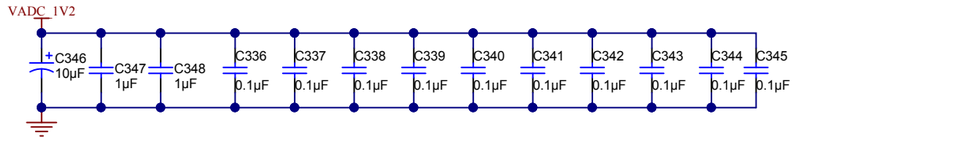
ADC Power Pins and Decoupling Capacitors

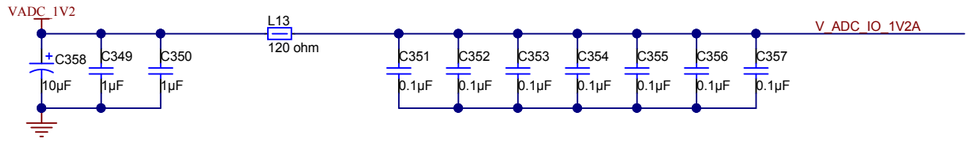


The ADC thermal pad is the only ground connection for this IC. Ensure good connection through multiple vias to the PCB ground planes.

Decoupling caps shall be placed as close to ADC power pins as possible.







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Engineer: a0271760	Contact: http://www.ti.com/support	

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ADC Input, JESD204B Interface, SPI and Discrete I/O Control

For schematic and layout recommendations and requirements see the ADC12J4000 product page linked below.

TI ADC12J4000 Product Page

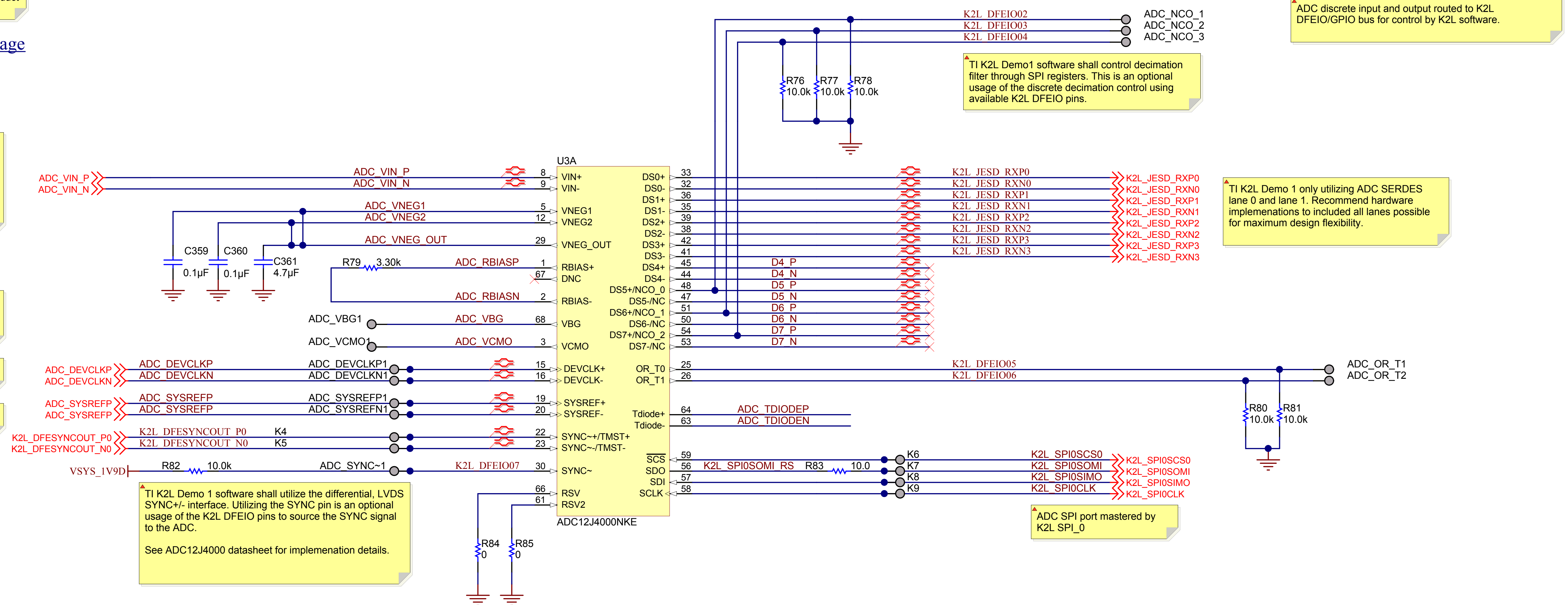
ADC input signal signal conditioning (bal-un, op-amps...etc) is not shown here.

The input circuit required is application and system specific. Please see ADC12J4000 datasheet, application notes and EVM design guide for specific recommendations.

ADC_DEVCLK is a 1GHz+ signal. It needs to be specially routed, and GND isolated in a similar manner to the JESD SERDES channels.

ADC DEVCLK driven by LMK04828

ADC SYSREF driven by LMK04828



K2L_DFEIO[17..00]
K2L_DFEIO02
K2L_DFEIO03
K2L_DFEIO04
ADC_NCO_1
ADC_NCO_2
ADC_NCO_3
R76 10.0k
R77 10.0k
R78 10.0k
U3A
ADC12J4000NKE
ADC_VIN_P
ADC_VIN_N
ADC_VNEG1
ADC_VNEG2
ADC_VNEG_OUT
C359 0.1µF
C360 0.1µF
C361 4.7µF
R79 3.30k
ADC_RBIASP
ADC_RBIASN
ADC_VBG1
ADC_VBG
ADC_VCMO1
ADC_VCMO
ADC_DEVCLKP
ADC_DEVCLKN
ADC_DEVCLKP1
ADC_DEVCLKN1
ADC_SYSREFP
ADC_SYSREFP1
ADC_SYSREFN1
K2L_DFESYNCOUT_P0
K2L_DFESYNCOUT_N0
K4
K5
VSYS_1V9D
R82 10.0k
ADC_SYNC~1
K2L_DFEIO07
VIN+
VIN-
VNEG1
VNEG2
VNEG_OUT
RBIAS+
DNC
RBIAS-
VBG
VCMO
DEVCLK+
DEVCLK-
SYSREF+
SYSREF-
SYNC~+/TMST+
SYNC~-/TMST-
SYNC~
RSV
RSV2
DS0+
DS0-
DS1+
DS1-
DS2+
DS2-
DS3+
DS3-
DS4+
DS4-
DS5+/NCO_0
DS5-/NC
DS6+/NCO_1
DS6-/NC
DS7+/NCO_2
DS7-/NC
OR_T0
OR_T1
Tdiode+
Tdiode-
SCS
SDO
SDI
SCLK
K2L_JESD_RXP0
K2L_JESD_RXN0
K2L_JESD_RXP1
K2L_JESD_RXN1
K2L_JESD_RXP2
K2L_JESD_RXN2
K2L_JESD_RXP3
K2L_JESD_RXN3
D4_P
D4_N
D5_P
D5_N
D6_P
D6_N
D7_P
D7_N
K2L_DFEIO05
K2L_DFEIO06
ADC_OR_T1
ADC_OR_T2
R80 10.0k
R81 10.0k
ADC_TDIODEP
ADC_TDIODEN
K2L_SPI0SOMI_RS
R83 10.0
K6
K7
K8
K9
K2L_SPI0SCS0
K2L_SPI0SOMI
K2L_SPI0SIMO
K2L_SPI0CLK
R84 0
R85 0

TI K2L Demo1 software shall control decimation filter through SPI registers. This is an optional usage of the discrete decimation control using available K2L DFEIO pins.

ADC discrete input and output routed to K2L DFEIO/GPIO bus for control by K2L software.

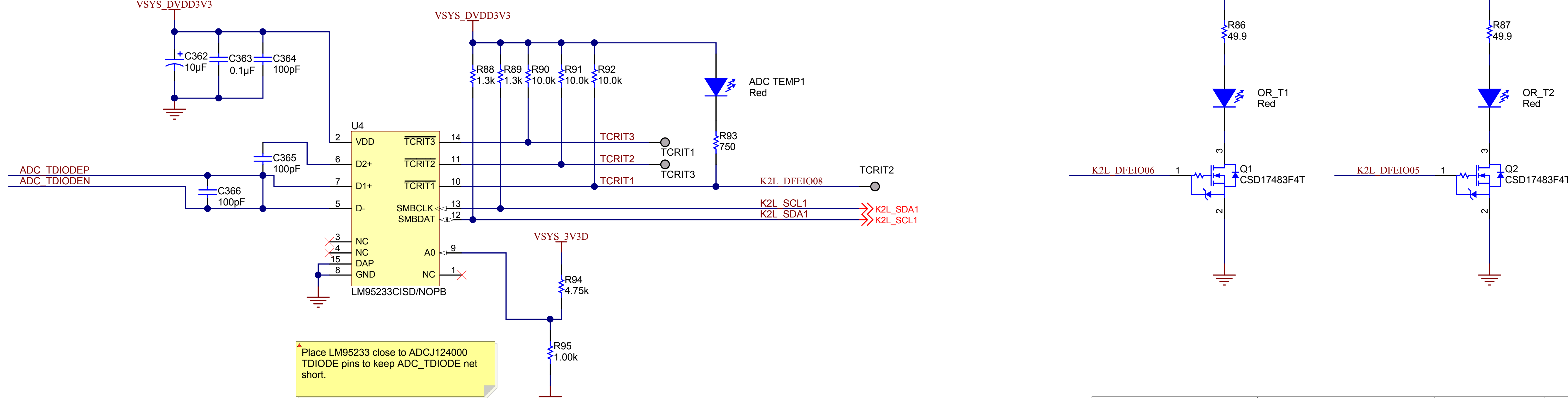
TI K2L Demo 1 only utilizing ADC SERDES lane 0 and lane 1. Recommend hardware implemenations to included all lanes possible for maximum design flexibility.

TI K2L Demo 1 software shall utilize the differential, LVDS SYNC+/- interface. Utilizing the SYNC pin is an optional usage of the K2L DFEIO pins to source the SYNC signal to the ADC.

See ADC12J4000 datasheet for implemenation details.

ADC SPI port mastered by K2L SPI_0

ADC Temperature Sensor



VSYS_DVDD3V3
C362 10µF
C363 0.1µF
C364 100pF
C365 100pF
C366 100pF
ADC_TDIODEP
ADC_TDIODEN
U4
LM95233CISD/NOPB
VDD
D2+
D1+
D-
NC
DAP
GND
TCRIT3
TCRIT2
TCRIT1
SMBCLK
SMBDAT
A0
R88 1.3k
R89 1.3k
R90 10.0k
R91 10.0k
R92 10.0k
ADC TEMP1 Red
R93 750
K2L_DFEIO08
K2L_SCL1
K2L_SDA1
VSYS_3V3D
R94 4.75k
R95 1.00k
R86 49.9
R87 49.9
OR_T1 Red
OR_T2 Red
K2L_DFEIO06
K2L_DFEIO05
Q1 CSD17483F4T
Q2 CSD17483F4T

Place LM95233 close to ADCJ124000 TDIODE pins to keep ADC_TDIODE net short.

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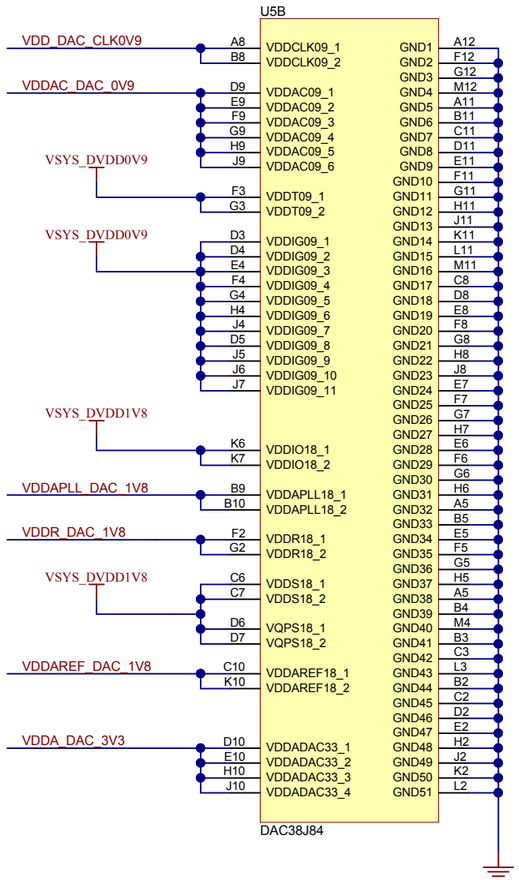
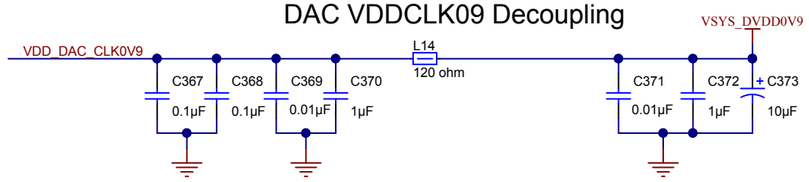
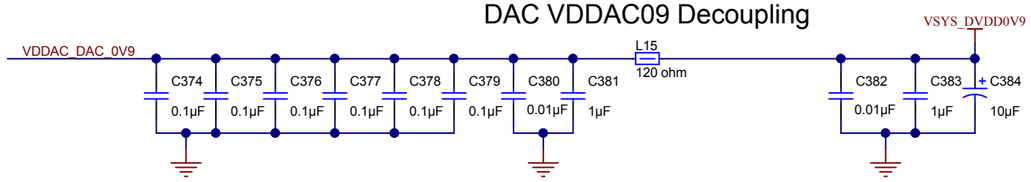


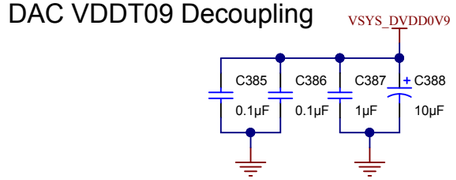
DAC VDDCLK09 Decoupling



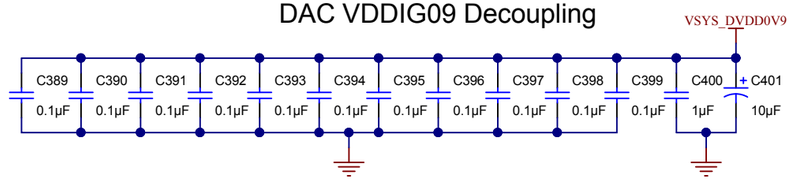
DAC VDDAC09 Decoupling



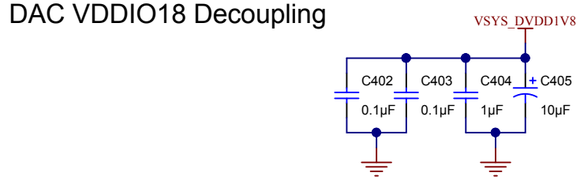
DAC VDDT09 Decoupling



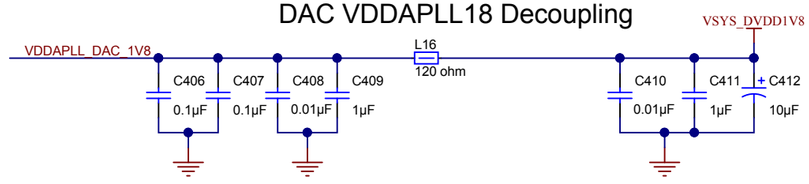
DAC VDDIG09 Decoupling



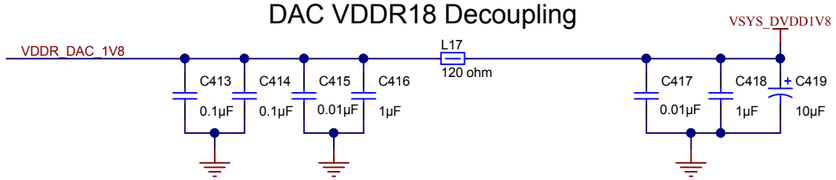
DAC VDDIO18 Decoupling



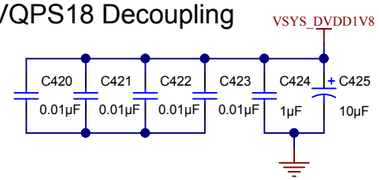
DAC VDDAPLL18 Decoupling



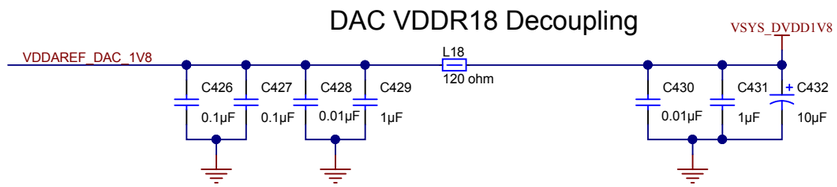
DAC VDDR18 Decoupling



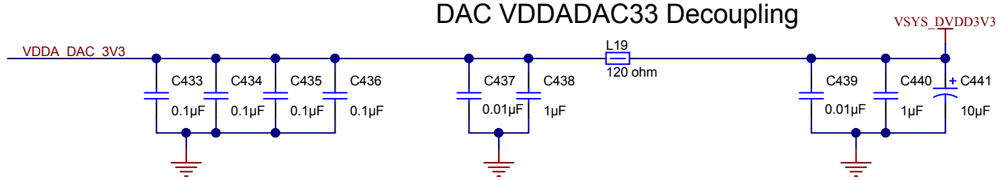
DAC VDDS18/VQPS18 Decoupling



DAC VDDR18 Decoupling



DAC VDDADAC33 Decoupling



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DAC Output, JESD204B Interface, SPI and Discrete I/O Control

For schematic and layout recommendations and requirements see the DAC38J84 product page linked below.

TI DAC38J84 Product Page

DAC DACCLK driven by LMK04828 LVPECL source.

DAC SYSREF driven by LMK04828 LVPECL source.

TI K2L Demo 1 only utilizing DAC SERDES lane 0 and lane 1. Recommend hardware implemenations to included all lanes possible for maximum design flexibility.

Optional external low-pass filter element. Shall be placed as close as possible to DAC BGA.

Please see DAC38J84 datasheet, application notes and EVM design guide for specific recommendations.

K2L_DFEIO[17..00] <<K2L_DFEIO[17..00]

DAC discrete input and output routed to K2L DFEIO/GPIO bus for control by K2L software.

DAC output signal signal conditioning (bal-un, op-amps...etc) is not shown here. The output circuit required is application and system specific. Please see DAC38J84 datasheet, application notes and EVM design guide for specific recommendations.

U5A

DAC_DACCLKP, DAC_DACCLKN → C443 0.1µF, C445 0.1µF → DAC_DACCLKP_CS, DAC_DACCLKN_CS → A10, A9 → DACCLKP, DACCLKN

DAC_SYSREFP, DAC_SYSREFN → C446 0.1µF, C447 0.1µF → DAC_SYSREFP_CS, DAC_SYSREFN_CS → A7, A6 → SYSREFP, SYSREFN

LPF C9 — R96 1.00k, C442 1000pF, R97 0, C444 0.1µF, GND

K2L_JESD_TXP3 / TXN3	C448 0.1µF, C449 0.1µF	DAC_JESD_TXP3_CS / TXN3_CS	M3, M2	RX3P, RX3N	
K2L_JESD_TXP2 / TXN2	C450 0.1µF, C451 0.1µF	DAC_JESD_TXP2_CS / TXN2_CS	L1, M1	RX2P, RX2N	
K2L_JESD_TXP1 / TXN1	C452 0.1µF, C453 0.1µF	DAC_JESD_TXP1_CS / TXN1_CS	K1, J1	RX1P, RX1N	
K2L_JESD_TXP0 / TXN0	C454 0.1µF, C455 0.1µF	DAC_JESD_TXP0_CS / TXN0_CS	G1, H1	RX0P, RX0N	

A3, A2 → RX7P, RX7N

B1, A1 → RX6P, RX6N

C1, D1 → RX5P, RX5N

F1, E1 → RX4P, RX4N

IOUTAP, IOUTAN	B12, C12	DAC_IOUTAP, DAC_IOUTAN
IOUTBP, IOUTBN	E12, D12	DAC_IOUTBP, DAC_IOUTBN
IOUTCP, IOUTCN	H12, J12	DAC_IOUTCP, DAC_IOUTCN
IOUTDP, IOUTDN	L12, K12	DAC_IOUTDP, DAC_IOUTDN

TXENABLE K5 — K2L_DFEIO09 — DAC_TXENABLE1 — R98 10.0k

EXTIO F10 — DAC_EXTIO — DAC_EXTIO1 C456 0.1µF, GND, GND

RBIAS G10 — DAC_RBIAS — R99 1.91k, GND

DAC_SYNCBP, DAC_SYNCBN → DAC_SYNCBP, DAC_SYNCBN → B7, B6 → SYNCBP, SYNCBN

DAC_AMUX1, DAC_AMUX2 → DAC_AMUX0, DAC_AMUX1 → H3, E3 → AMUX0, AMUX1

DAC38J84

Rbias controls the full-scale current output according to datasheet equation:

IOUTFS = (coarse_dac + 1) /16 x IBIAS x 64 = (coarse_dac + 1) /16 x VEXTIO / RBIAS x 64

U5C

DAC SPI port mastered by K2L SPI_1

K2L_SPI1SIMO, K2L_SPI1SCS0, K2L_SPI1CLK, K2L_SPI1SOMI → K2L_DAC_SPI1SIMO, K2L_DAC_SPI1SCS0, K2L_DAC_SPI1CLK, K2L_DAC_SPI1SOMI_RS (R100 10.0) → K10, K11, K12, K13 → L10, M9, L9, M10 → SDIO, SDENB, SCLK, SDO

IFORCE	C5	DAC_IFORCE → DAC_IFORCE1
VSENSE	C4	DAC_VSENSE → DAC_VSENSE1
ATEST	K9	DAC_ATEST → DAC_ATEST1
ALARM	L8	DAC_ALARM → DAC_ALARM1
TESTMODE	K3	DAC_TESTMODE → DAC_TESTMODE1

JTAG interface not utilized. JTAG subsystem held in reset per datasheet insuctions by TRSTB tied to GND.

K4, L5, M5, L4, J3 → TCLK, TDI, TDO, TMS, TRSTB

DAC_RESET1 → K2L_DFEIO10 → K8 → RESETB

DAC_SLEEP1 → K2L_DFEIO11 → M8 → SLEEP

R101 10.0k, R102 10.0k, R103 0, GND, GND, GND

SYNC_N_AB L6, SYNC_N_CD L7

NC3 M6, NC4 M7

DAC38J84

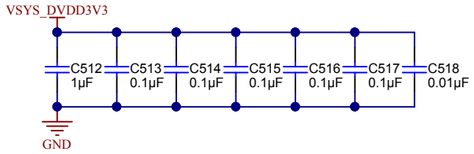
TI K2L Demo 1 software shall utilize the differential, LVDS SYNCBP/N interface. Utilizing the SYNC_AB and SYNC_CD pins is an optional usage of the K2L DFEIO pins to recieve the SYNC signal from the DAC.

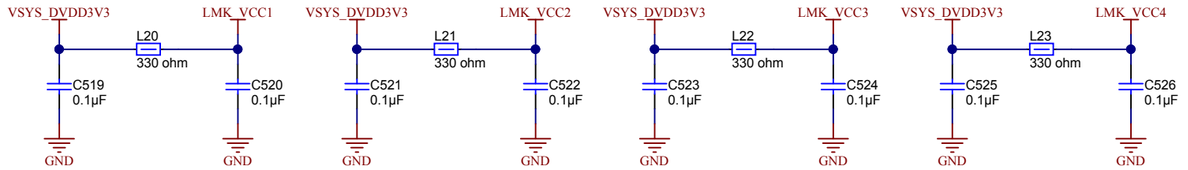
See DAC38J84 datasheet for implemenation details.

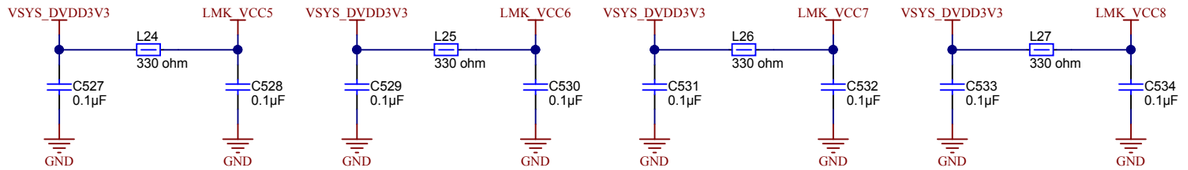
Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 4/14/2015
TID #: TIDEP0034		Project Title: TI 66AK2L06 JESD Attach to Wideband ADCs and I	
Number: TIDEP0034	Rev: E1	Sheet Title:	
SVN Rev: Version control disabled		Assembly Variant: [No Variations]	Sheet: 28 of 35
Drawn By:		File: dac38j84_02.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

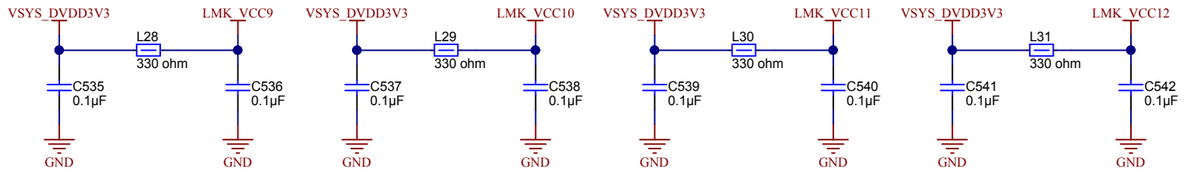
LMK04828 Decoupling Capacitors

LMK04828 decoupling shall be placed as close to the IC package as possible. See LMK04828 datasheet and EVM for example decoupling layout.









Orderable: EVM_orderable	Designed for: Public Release	Mod. Date: 4/14/2015
TID #: TIDEP0034	Project Title: TI 66AK2L06 JESD Attach to Wideband ADCs and I	
Number: TIDEP0034 Rev: E1	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 29 of 35
Drawn By:	File: lmk04828_01.SchDoc	Size: B
Engineer: a0271760	Contact: http://www.ti.com/support	

TEXAS INSTRUMENTS
http://www.ti.com

For schematic and layout recommendations and requirements see the LMK04828 product page linked below.

TI LMK04828 Product Page

LMK04828 RESET and SYNC mastered by System Controller (microcontroller) not shown here.

All unused pins shall be routed with short stubs to aid in solderability and mechanical robustness. Indicated by the LMK-xx unused pin nets names.

U11
LMK04828BISQ/NOPB

LMK04828 DCLKOUT0 used as the device clock for the ADC

LMK04828 SDCLKOUT0 used as the SYSREF for the ADC

LMK04828 DCLKOUT2 used as the device clock for the DAC

LMK04828 SDCLKOUT3 used as the SYSREF for the DAC

DAC DACCLK and SYSREF are LVPECL inputs which require LVPECL source biasing and AC-coupling as described in the DAC38J84 datasheet section 7.3.25

LMK04828 SPI port mastered by System Controller (microcontroller) not shown here.

LMK04828 SDCLKOUT5 used as the SYSREF for the K2L

LMK04828 DCLKOUT4 used as the SYSCLK for the K2L

LMK04828 DCLKOUT6 used as the JESD0 SERDES clock for the

LMK04828 SDCLKOUT7 used as the JESD1 SERDES clock for the

LMK04828 LD1 and LD2 monitored by System Controller (microcontroller) not shown here.

Optional external charge-pump filter element. Shall be placed as close as possible to LMK04828.

Please see LMK04828 datasheet, application notes and EVM design guide for specific recommendations.

Special care should be taken to GND isolate CLKIN0 signal.

19.2 MHz TCXO

LMK04828 LD1 and LD2 monitored by System Controller (microcontroller) not shown here.

Optional external charge-pump filter element. Shall be placed as close as possible to LMK04828.

Please see LMK04828 datasheet, application notes and EVM design guide for specific recommendations.

Orderable: EVM_orderable		Designed for: Public Release	Mod. Date: 4/14/2015
TID #: TIDEP0034		Project Title: TI 66AK2L06 JESD Attach to Wideband ADCs and D	
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SVN Rev: Version control disabled		Assembly Variant: [No Variations]	Sheet: 30 of 35
Drawn By:		File: lmk04828_02.SchDoc	Size: B
Engineer: a0271760		Contact: http://www.ti.com/support	

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