

TIDEP0042

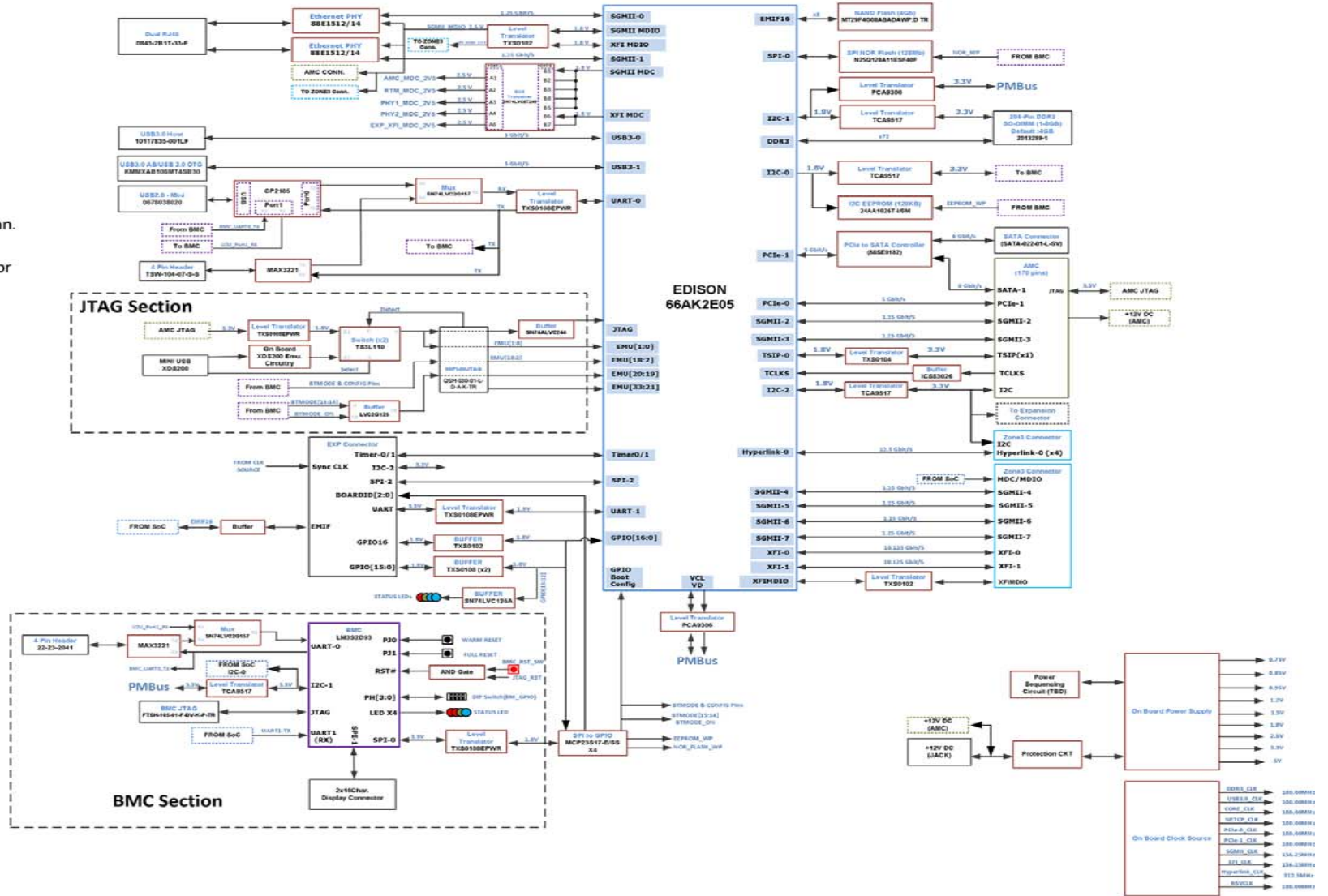
TI Design - Generating the AVS SmartReflex Core voltage for the K2E using the TPS544C25 and PMBus/I2C

Based on the XEVMK2EX design.
This schematic is a subset of the XEVMK2EX schematic.

Title		
TI Design Generating AVS with TPS544C25 and PMBus/I2C		
Size A	Document Number TIDEP0042	Rev A
Date:	Wednesday, August 12, 2015	Sheet 1 of 1

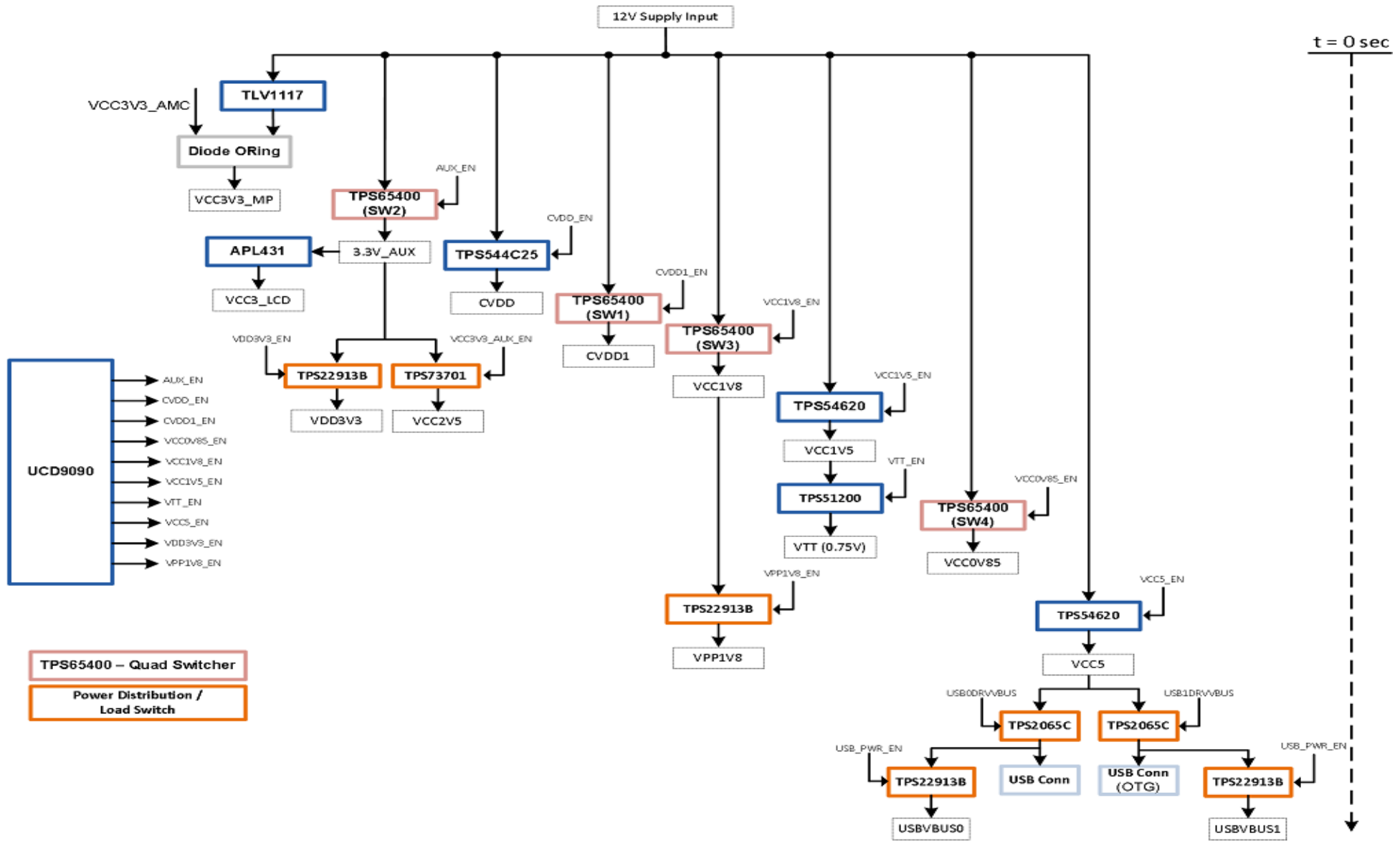
K2E EVM BLOCK DIAGRAM

- K2E SoC
- ICs
- Connectors
- Expansion Conn.
- AMC Connector
- BMC
- Zone 3 Conn.



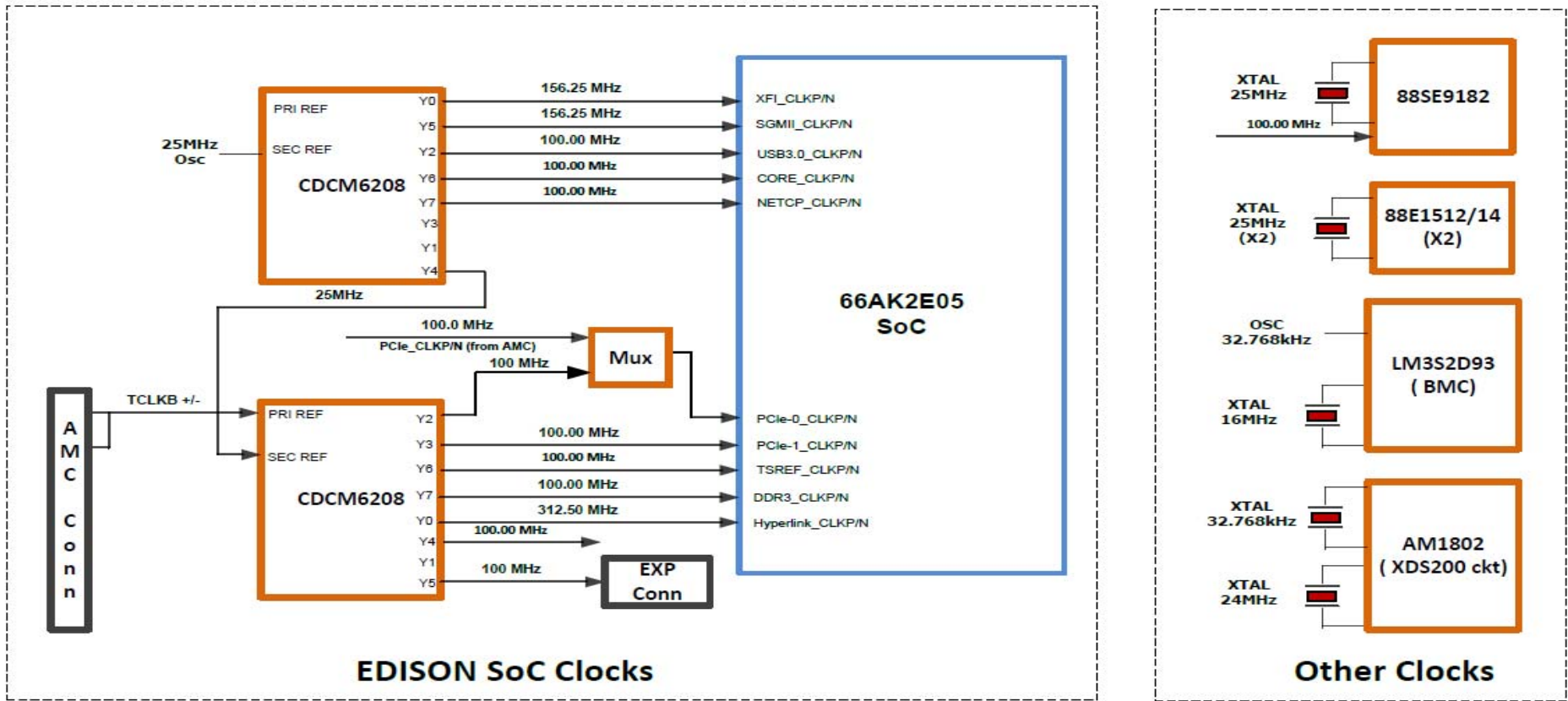
Project		K2E EVM		Designed for TI by elfnchips	
Title		SYSTEM BLOCKDIGRAM			
Size	Document Number	Rev			
C	16_00175_03	3.02			
Date: Monday, February 02, 2015			Sheet 3 of 37		

EDISON – Power Tree

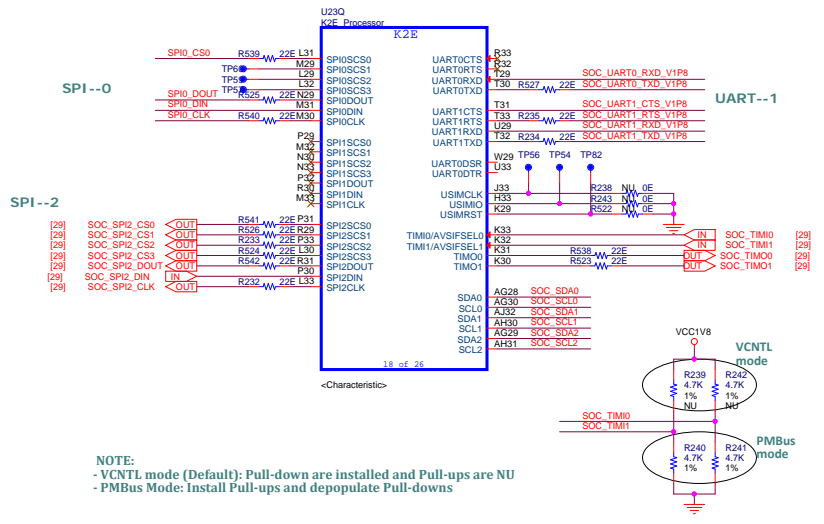


Project		K2E EVM		Designed for TI by elfnchips	
Title		POWER DISTRIBUTION			
Size	Document Number			Rev	
C	16_00175_03			3.02	
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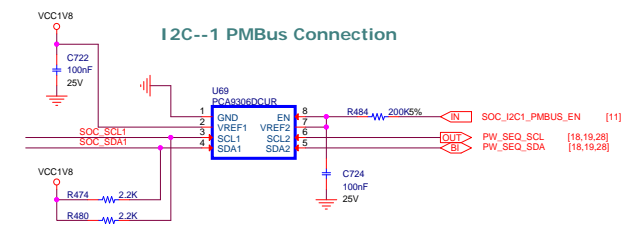
EDISON CLOCK GENERATION



Project K2E EVM		Designed for TI by elfochips	
Title CLOCK DIAGRAM			
Size C	Document Number 16_00175_03	Rev 3.02	
Date: Monday, February 02, 2015		Sheet 8 of 37	



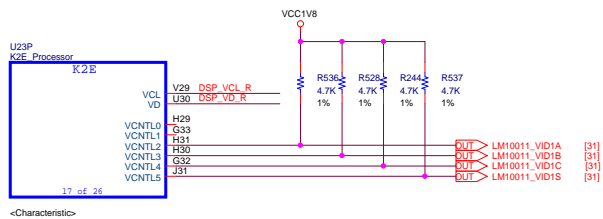
1.8V to 3.3V I2C voltage converter required for the connection to the TPS544C25




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Title		MISC			
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SMART REFLEX

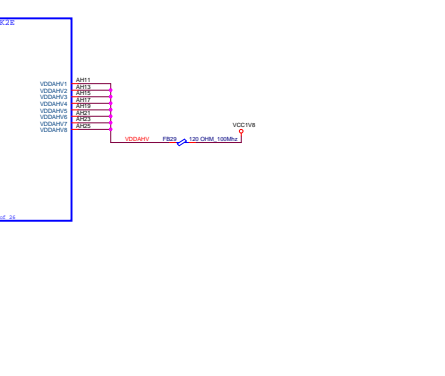
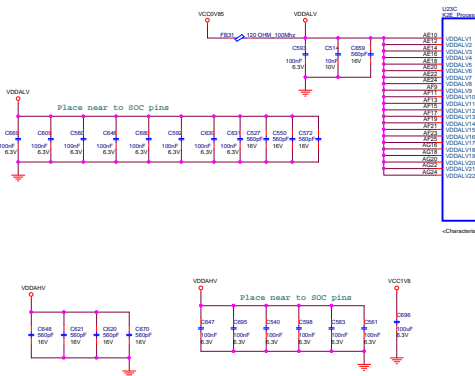
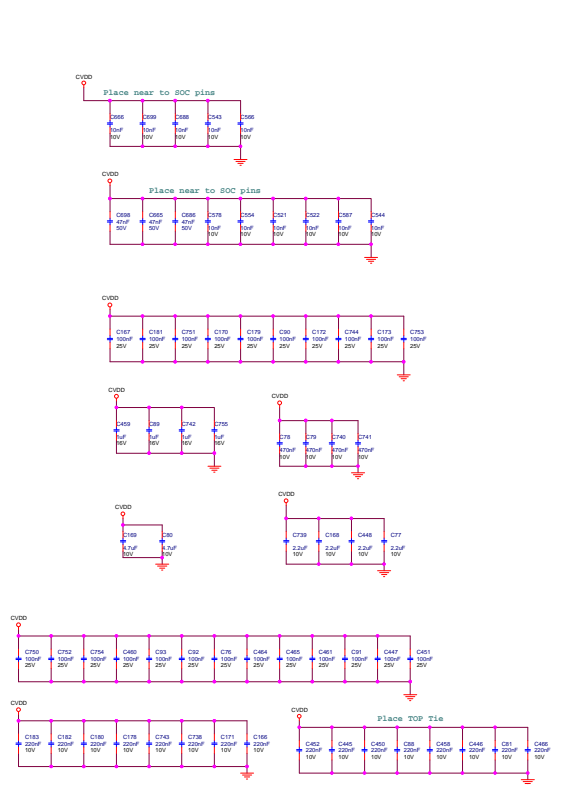
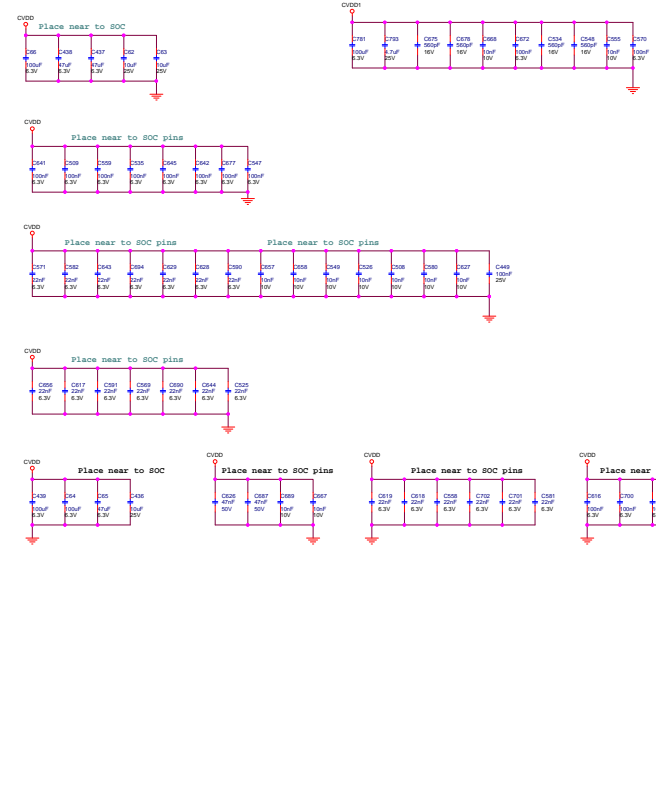
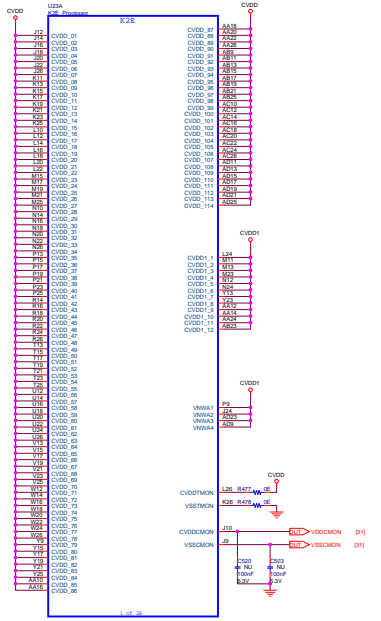
VCNTL interface included in schematic to allow the use of both LM10011 solution or the PMBus solution. VCNTL is not needed for PMBus solution. Refer to the users guide for more details.



Project K2E EVM		Designed for TI by elfochips	
Title CLOCK and SMART REFLEX			
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0.85V - 1.05V (CVDD) (Smart Reflex)

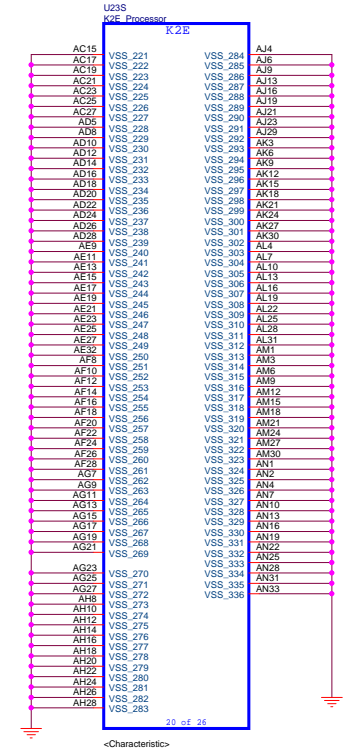
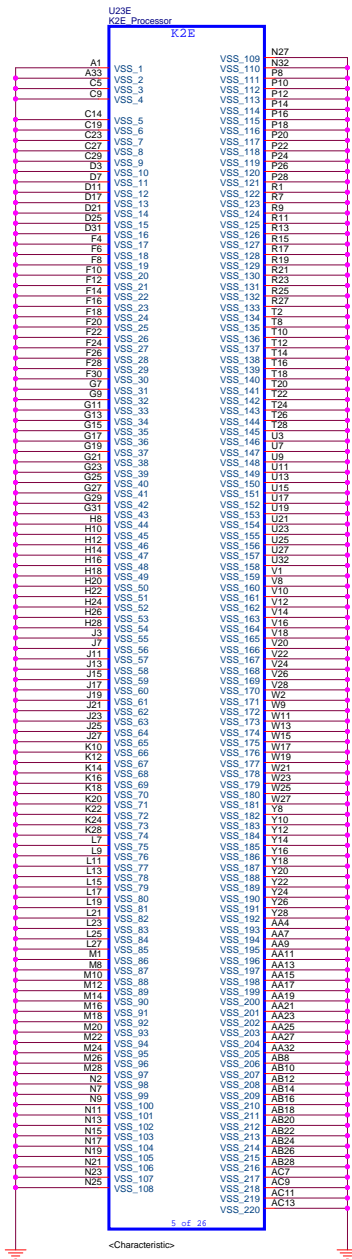
SOC POWER



THESE CAPS ARE ADDED FOR PROVISION ONLY. VALUES CAN BE CHANGED BASED ON PI ANALYSIS RESULT

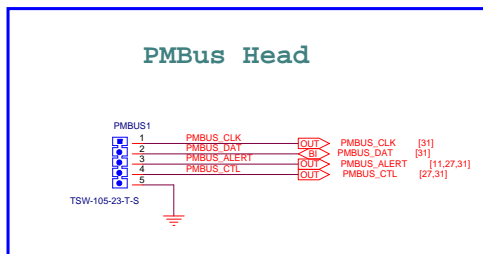
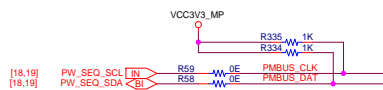
Project		K2E EVM		Designed for TI by infochips	
Title		SoC_POWERB			
Size	Document Number	16_00175_03		Rev	3.02
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SOC GROUND



Project		K2E EVM		Designed for TI by elfnchips	
Title		SoC Ground			
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Pull-up resistors and
 signa name change for the
 SOC I2C interface.



Project		K2E EVM		Designed for TI by elfochips	
Title		MCU_MISC			
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12V to CVDD Generation(TPS544C25)

LAYOUT NOTE:

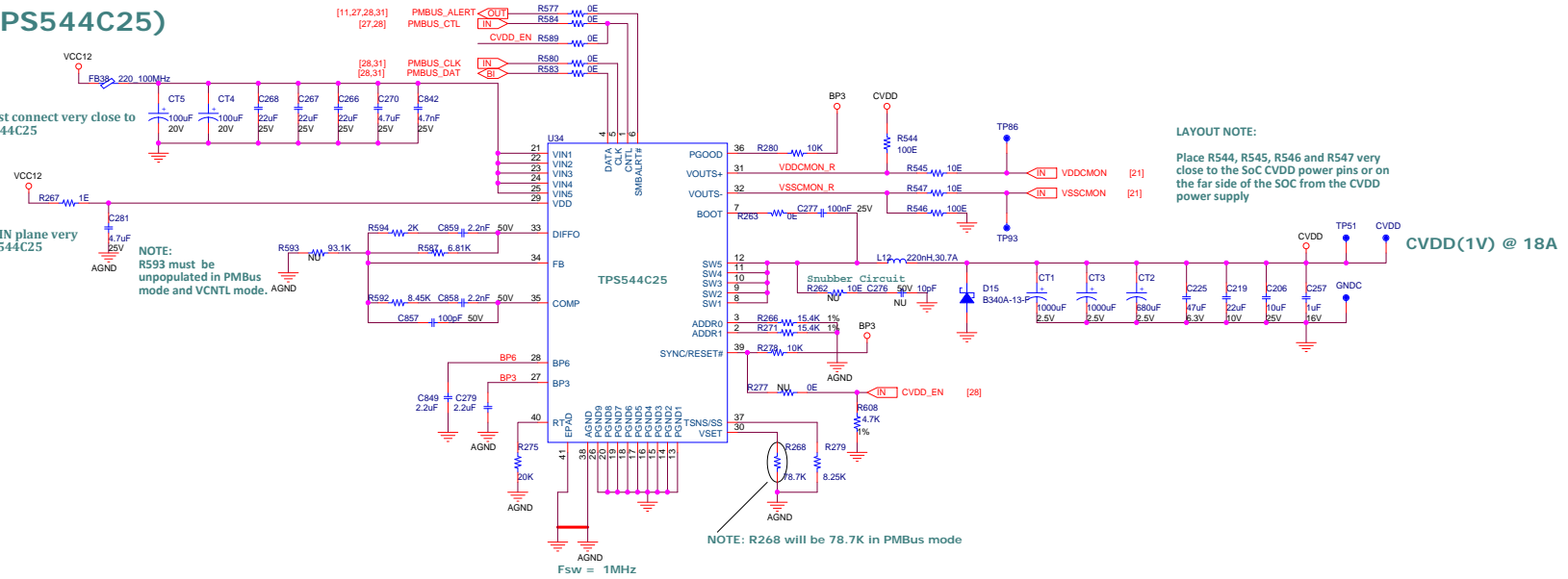
C842 (4.7nF) must connect very close to VIN pins of TPS544C25

LAYOUT NOTE:
R267 must connect to VIN plane very close to VIN pins of TPS544C25

NOTE:
R593 must be unpopulated in PMBus mode and VCNTL mode. AGND

LAYOUT NOTE:

Place R544, R545, R546 and R547 very close to the SoC CVDD power pins or on the far side of the SOC from the CVDD power supply



LAYOUT NOTE:

Currently, AGND and PGND are NOT shorted in schematic, to keep 2 separate grounds in layout design file. However, they should be shorted in layout design file ONLY at SINGLE point, i.e.: Pin 38 can be directly connected to Thermal Pad with thicker trace

LM10011 was removed the schematic. LM10011 is not needed for PMBus solution. Refer to the users guide for more details.

Project		K2E EVM		Designed for TI by elfochips	
Title		POWER SUPPLY--2			
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C	16_00175_03			3.02	
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