Test Report: PMP22760

Dual-Output Bias Power Supply Reference Design for Inverter and Motor Drive Applications

1 Description

This isolated primary-side regulated (PSR) flyback converter provides dual 15-V outputs at 100 mA each. It was designed to provide bias power for a rotor coil excitation gate-driver in motor and inverter applications. The isolated output voltage is sampled from the primary-side flyback voltage, eliminating the need for an optocoupler, voltage reference, or third winding from the transformer for output voltage regulation. It offers a high level of integration, low cost, and high efficiency in a compact form factor.

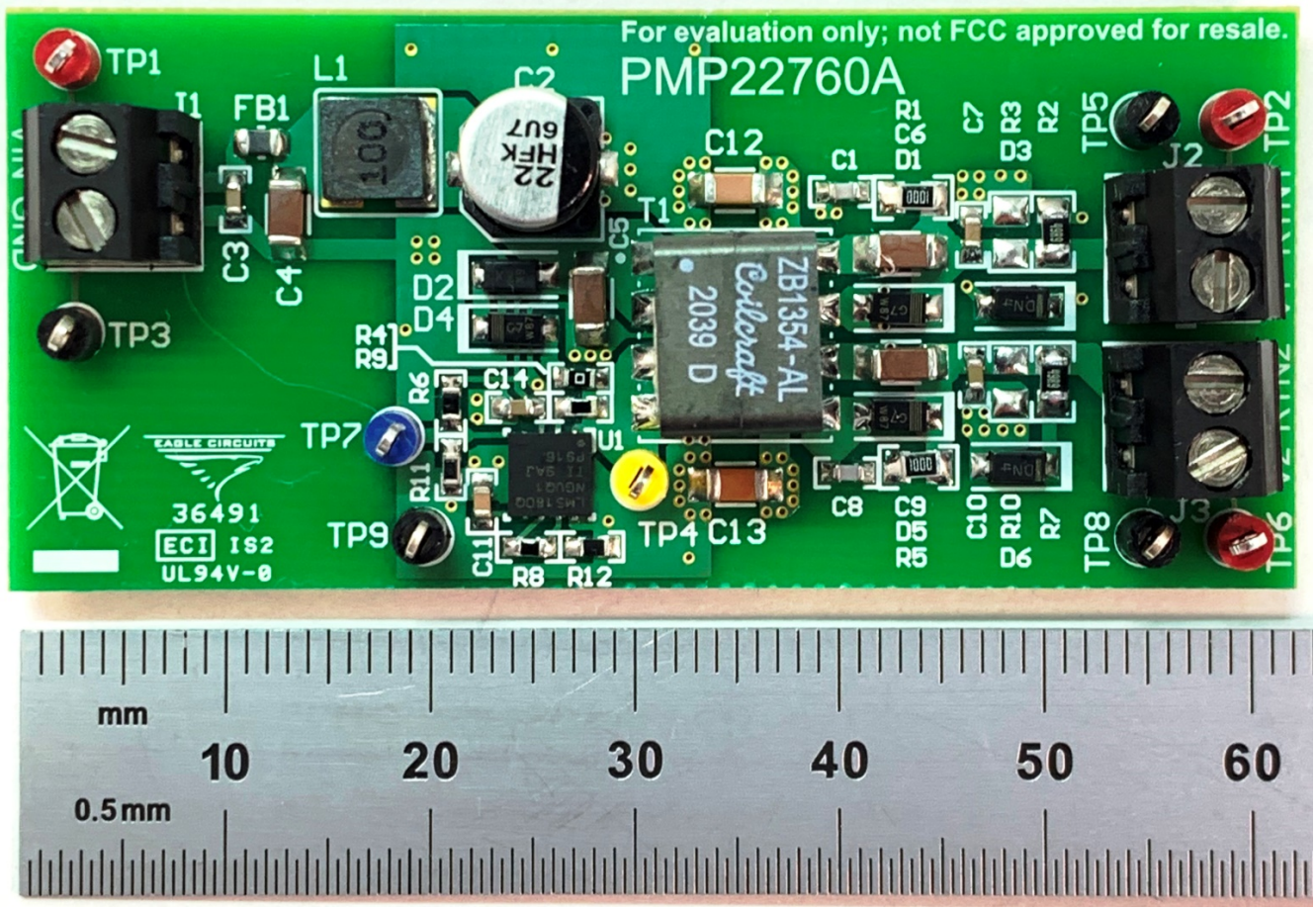


Figure 1-1. Top-Side Photo of PCB

2 Test Prerequisites

2.1 Voltage and Current Requirements

Table 2-1. Voltage and Current Requirements

Parameter	Specifications
Input voltage range	12 V–15 V
Output voltage and current	15 V and 100 mA maximum (2X)
Switching frequency	Variable, 350 kHz maximum
Isolation	1500 VAC (Pri - Secs), 750 VAC (Sec - Sec)
Topology	Flyback (FFM, DCM, BCM operating modes)

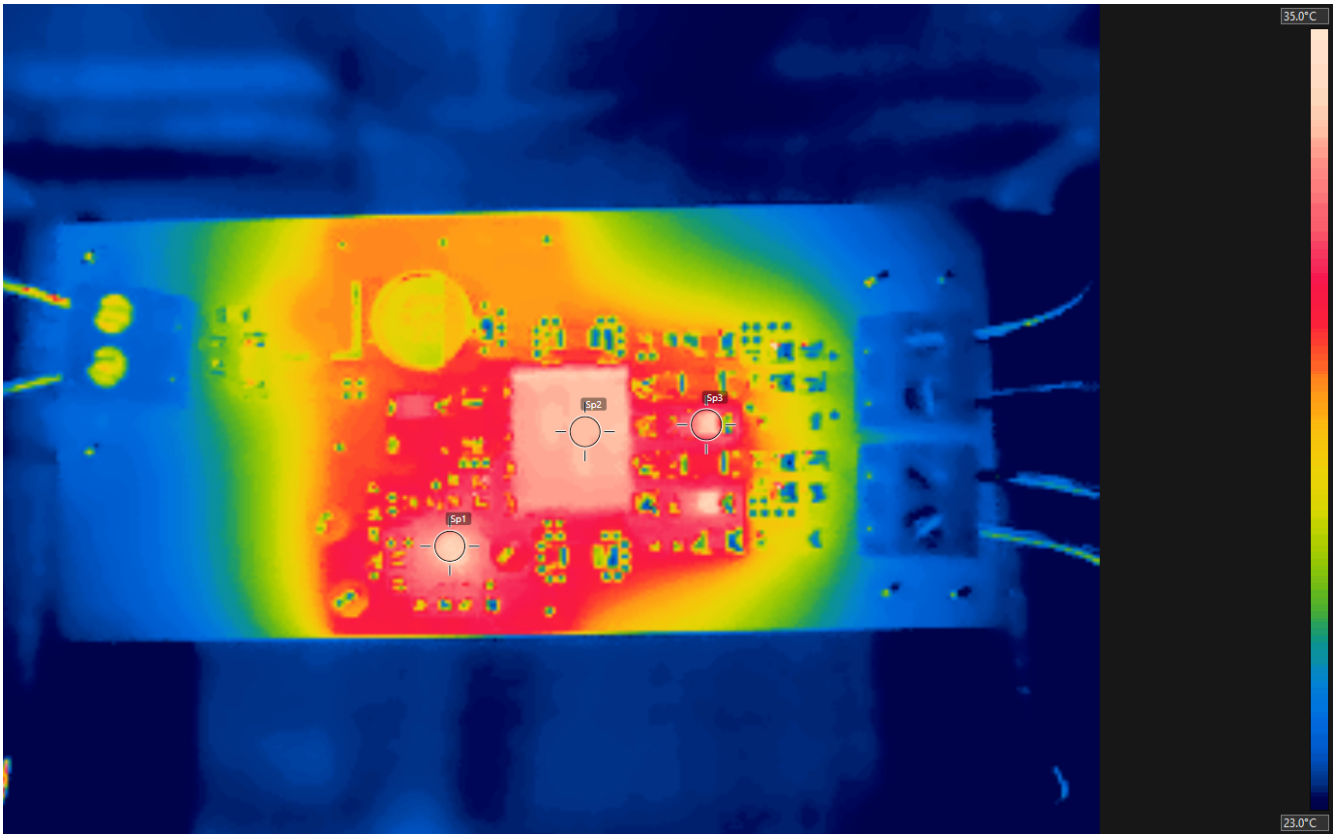
2.2 Required Equipment

- Resistive loads (resistor decade boxes), 1.5 W minimum each
- Power supply, variable, 15 V and 0.5 A minimum
- Oscilloscope and probes
- Digital multimeters

3 Testing and Results

3.1 Thermal Images

This thermal image shows the operating temperature of the top side of the board with 12-VDC input and both 15-V outputs loaded to 100 mA, while at room temperature and no air flow.



Measurement Location	Temperature (C)
Sp1	33.8
Sp2	33.5
Sp3	33.7

Figure 3-1. Top Side Thermal Image

3.2 Efficiency and Power Dissipation Graphs

This graph displays the efficiency and power dissipation of the converter with 12-VDC and 15-VDC input voltages.

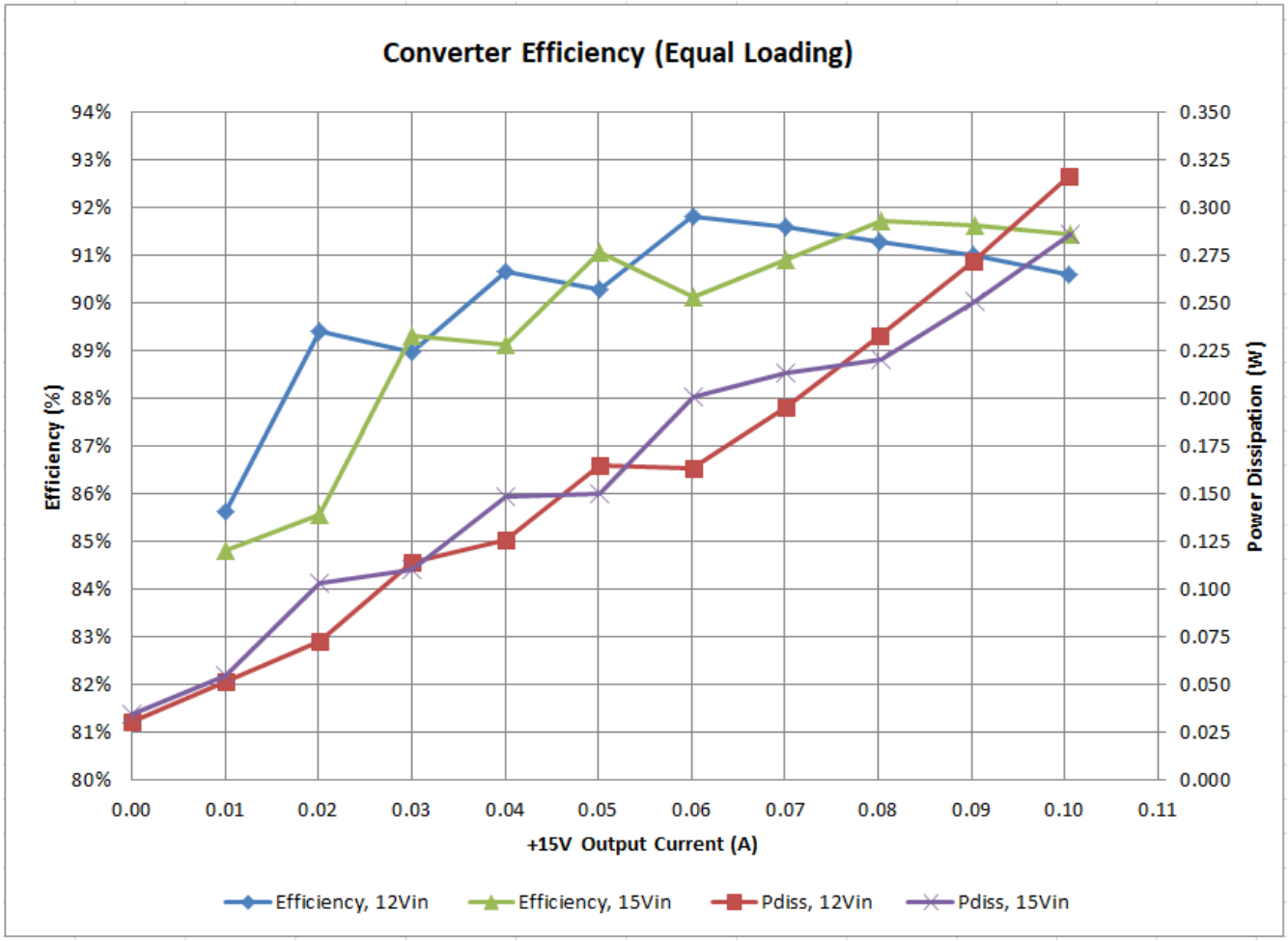


Figure 3-2. Efficiency Graph

3.3 Efficiency and Power Dissipation Data

Efficiency data with equal output loading is shown in the following tables.

Vin	Iin	Vout1	Iout1	Vout2	Iout2	Po	Pin	Efficiency	Pdiss (W)
12.025	0.0025	16.565	0.0000	16.428	0.00000	0.000	0.030	0.0%	0.030
12.022	0.0297	15.284	0.0100	15.284	0.00999	0.306	0.357	85.6%	0.051
12.020	0.0570	15.277	0.0201	15.278	0.02001	0.613	0.685	89.4%	0.073
12.018	0.0858	15.264	0.0301	15.264	0.03006	0.918	1.031	89.0%	0.114
12.016	0.1121	15.255	0.0400	15.255	0.04001	1.221	1.347	90.6%	0.126
12.013	0.1411	15.248	0.0502	15.249	0.05017	1.530	1.695	90.3%	0.165
12.011	0.1663	15.243	0.0601	15.244	0.06021	1.834	1.997	91.8%	0.164
12.009	0.1942	15.233	0.0700	15.234	0.07022	2.137	2.332	91.6%	0.196
12.007	0.2229	15.223	0.0802	15.223	0.08034	2.443	2.676	91.3%	0.233
12.005	0.2514	15.211	0.0902	15.212	0.09038	2.746	3.018	91.0%	0.272
12.002	0.2808	15.200	0.1004	15.201	0.10051	3.053	3.370	90.6%	0.317

Vin	Iin	Vout1	Iout1	Vout2	Iout2	Po	Pin	Efficiency	Pdiss (W)
15.035	0.0023	16.576	0.0000	16.440	0.00000	0.000	0.035	0.0%	0.035
15.033	0.0240	15.279	0.0100	15.279	0.01001	0.306	0.361	84.8%	0.055
15.031	0.0477	15.273	0.0201	15.274	0.02007	0.614	0.717	85.6%	0.103
15.032	0.0683	15.259	0.0300	15.260	0.03005	0.917	1.027	89.3%	0.110
15.028	0.0911	15.251	0.0400	15.251	0.04000	1.220	1.369	89.1%	0.149
15.026	0.1118	15.244	0.0502	15.245	0.05016	1.530	1.680	91.1%	0.150
15.024	0.1354	15.239	0.0601	15.240	0.06020	1.833	2.034	90.1%	0.201
15.023	0.1565	15.236	0.0701	15.237	0.07023	2.138	2.351	90.9%	0.214
15.021	0.1773	15.231	0.0804	15.233	0.08001	2.443	2.663	91.7%	0.221
15.019	0.2000	15.224	0.0904	15.225	0.09046	2.753	3.004	91.6%	0.251
15.017	0.2223	15.214	0.1006	15.216	0.10001	3.052	3.338	91.4%	0.286

3.4 Voltage Regulation Graphs

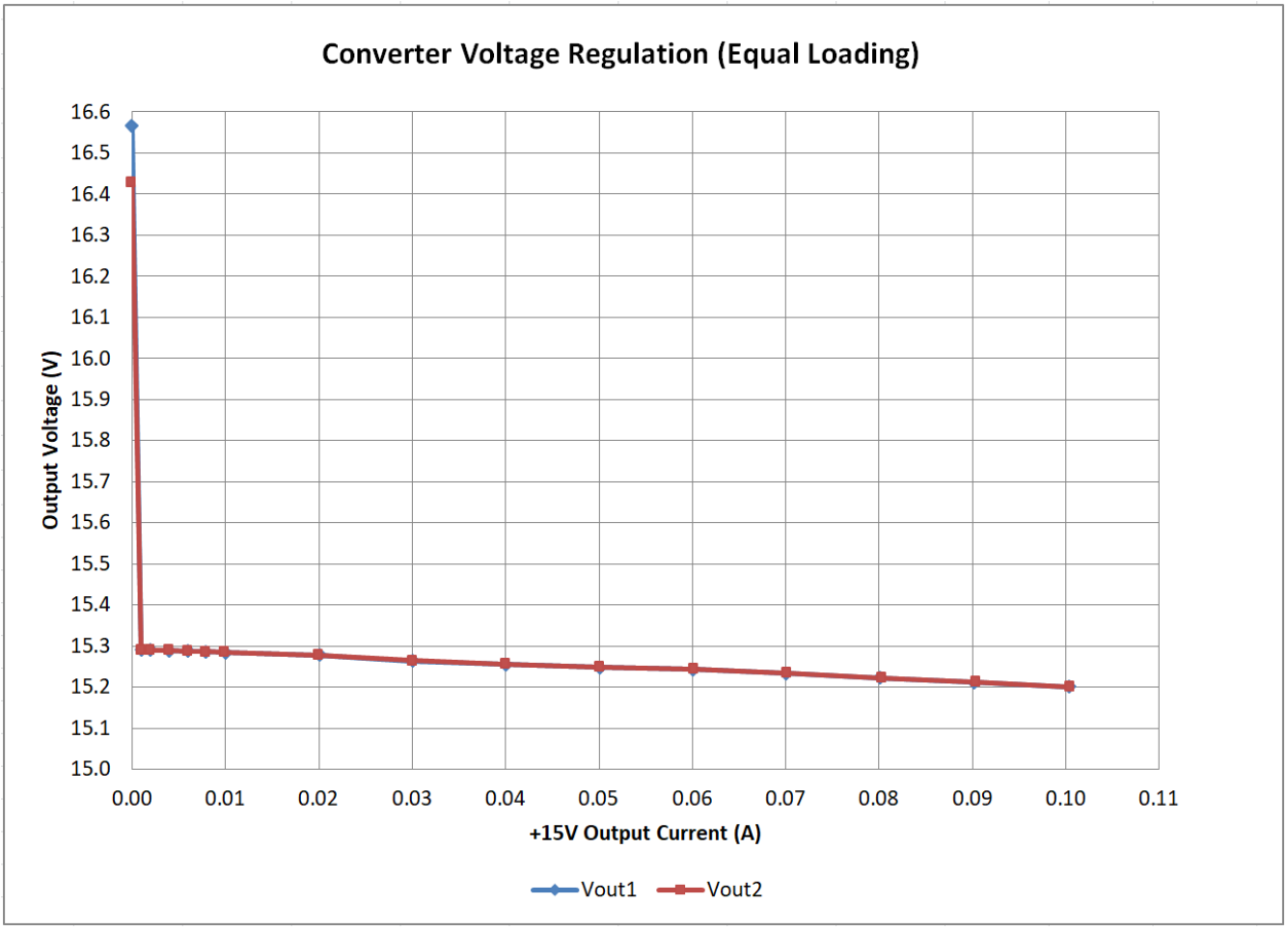


Figure 3-3. Output Voltage Regulation With Equal Loading

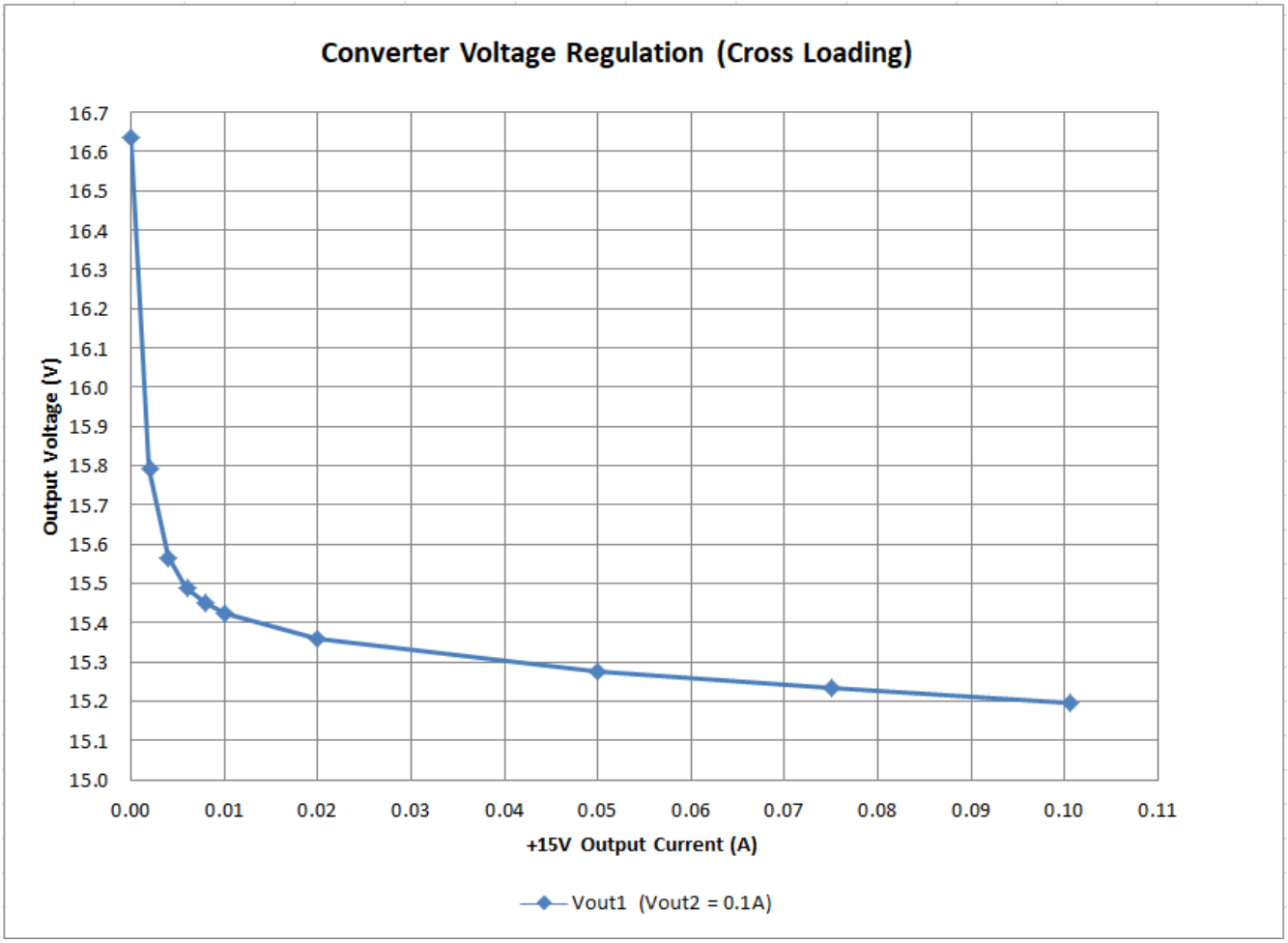


Figure 3-4. Output Voltage Regulation With Cross Loading

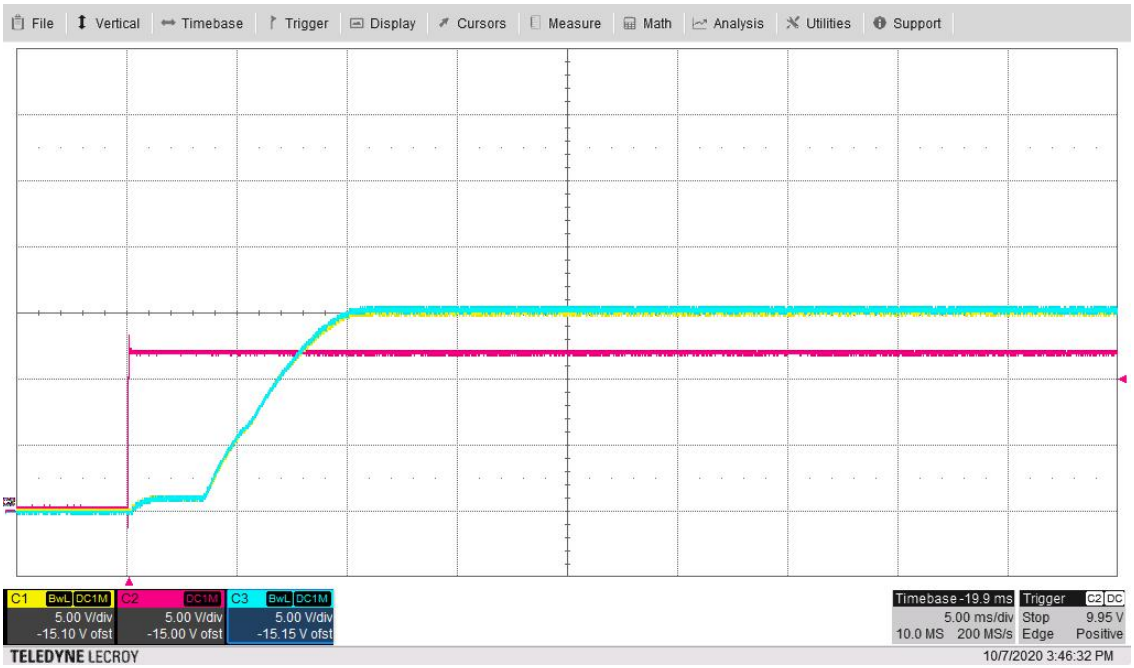
3.5 Cross-Load Voltage Regulation Data and Efficiency

Vin	Iin	Vout1	Iout1	Vout2	Iout2	Po	Pin	Efficiency	Pdiss (W)
12.025	0.1420	16.635	0.0000	15.188	0.10039	1.525	1.708	89.3%	0.183
12.024	0.1439	15.793	0.0020	15.188	0.10040	1.557	1.730	90.0%	0.174
12.024	0.1465	15.567	0.0040	15.188	0.10039	1.587	1.762	90.1%	0.175
12.023	0.1491	15.488	0.0060	15.187	0.10039	1.618	1.793	90.2%	0.175
12.023	0.1517	15.450	0.0080	15.187	0.10039	1.648	1.824	90.4%	0.176
12.023	0.1541	15.425	0.0100	15.187	0.10039	1.679	1.853	90.6%	0.174
12.022	0.1665	15.360	0.0200	15.188	0.10039	1.832	2.002	91.5%	0.169
12.018	0.2084	15.277	0.0500	15.189	0.10039	2.289	2.505	91.4%	0.216
12.015	0.2438	15.235	0.0750	15.194	0.10044	2.668	2.929	91.1%	0.261
12.012	0.2808	15.197	0.1005	15.197	0.10046	3.054	3.373	90.5%	0.319

4 Waveforms

4.1 Start-up Sequence

The following image shows the output voltage start-up waveforms (Vout1 in Blue, Vout2 in Yellow) after the application of 12-V input (Red) with each output loaded to 100 mA.



5 V/div, 5 ms/div

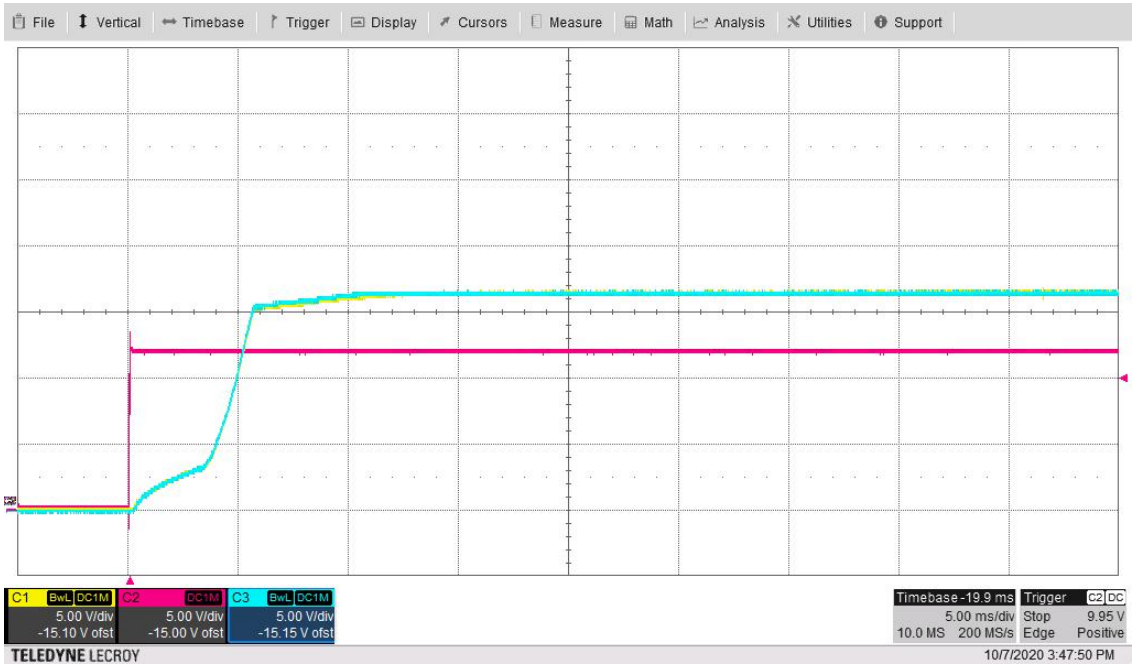
Figure 4-1. Output Voltage Start-up Waveforms

The following image shows the output voltage start-up waveforms (Vout1 in Blue, Vout2 in Yellow) after the application of 12-V input (Red) with each output loaded to 10 mA.

5 V/div, 5 ms/div

Figure 4-2. Output Voltage Start-up Waveforms

The following image shows the output voltage start-up waveforms (Vout1 in Blue, Vout2 in Yellow) after the application of 12-V input (Red) with each output loaded to 0 mA

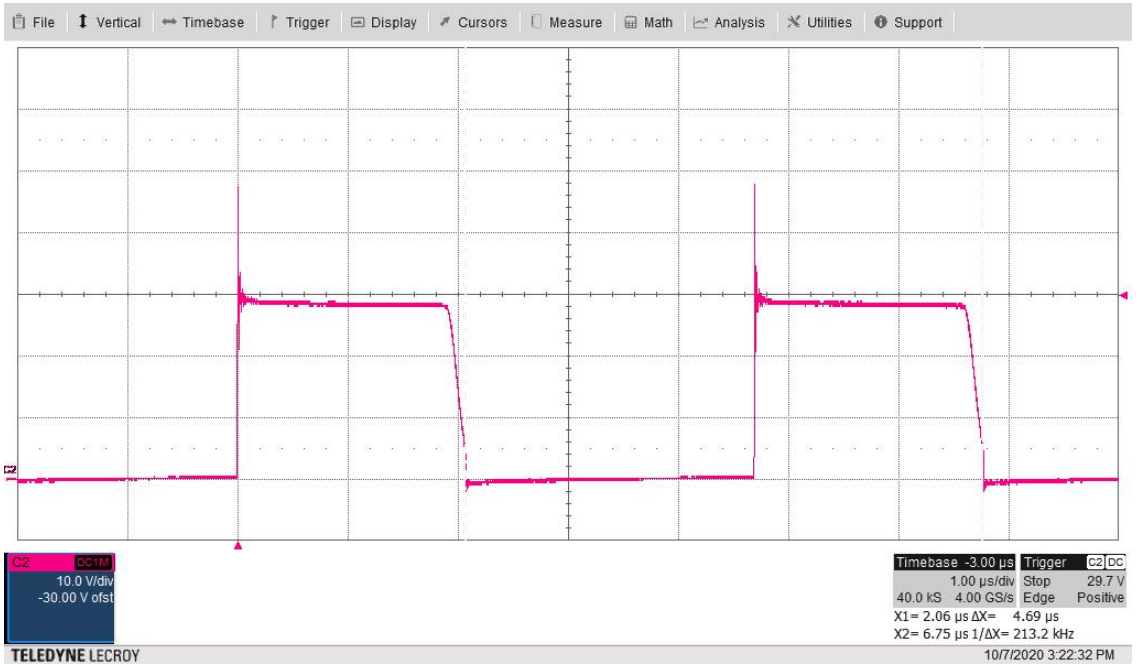


5 V/div, 5 ms/div

Figure 4-3. Output Voltage Start-up Waveform

4.2 Switch Node

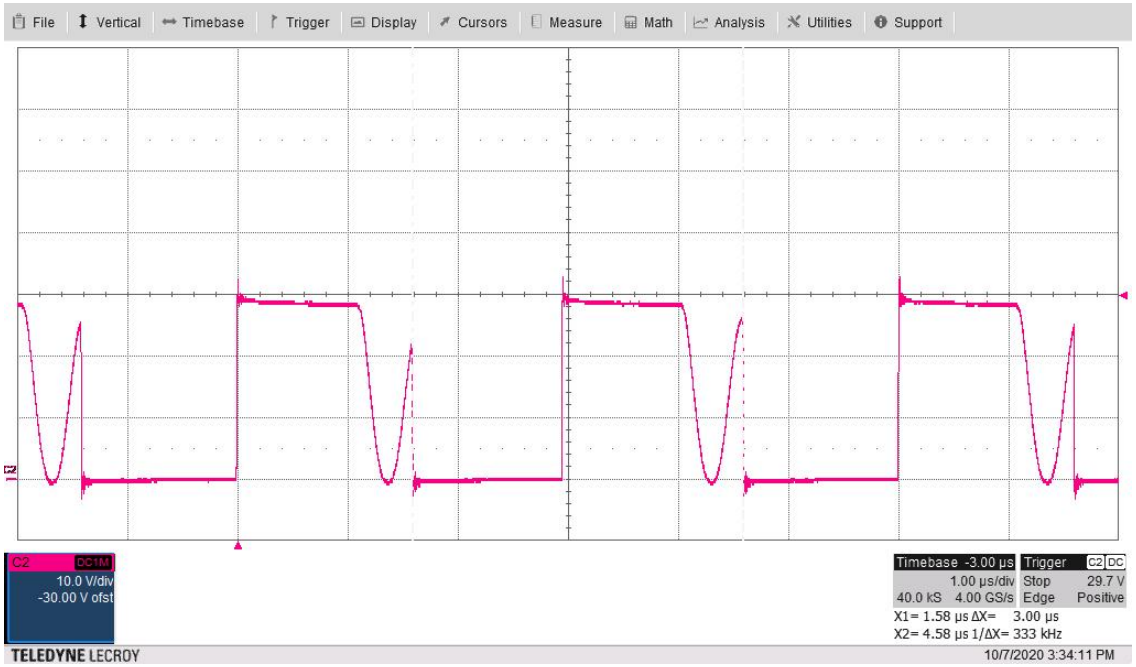
The following image shows the FET switch node voltage SW (Red) at TP4. The input voltage is 12 VDC and both 15-V outputs are loaded to 100 mA.



10 V/div, 1 µs/div

Figure 4-4. FET Switch Node Voltage SW

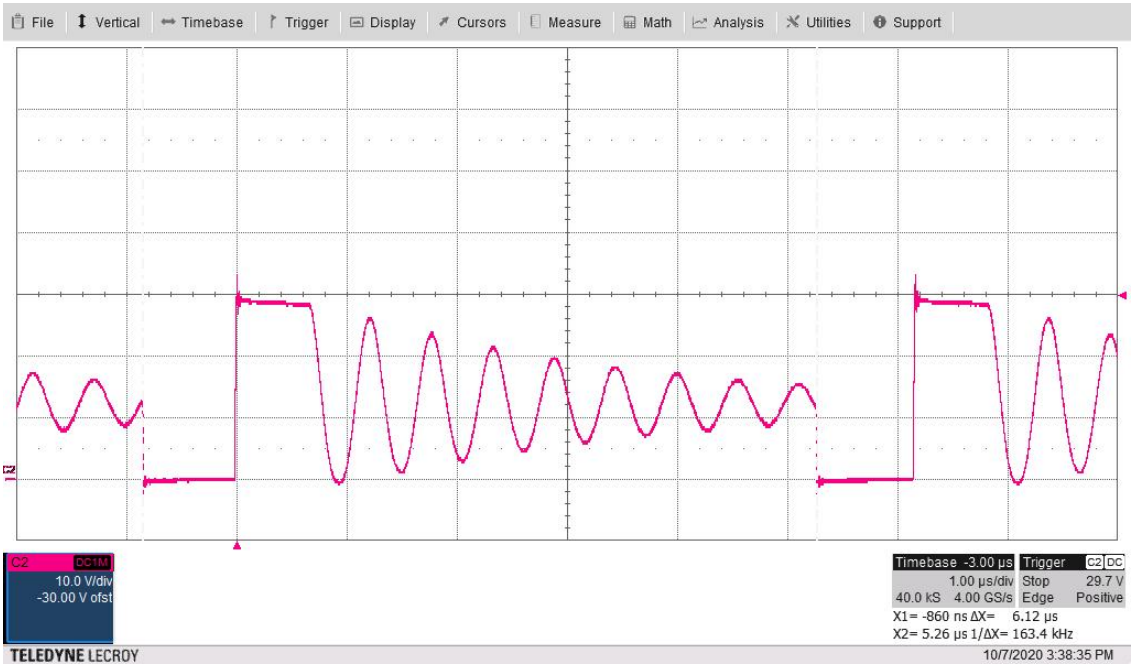
The following image shows the FET switch node voltage SW (Red) at TP4. The input voltage is 12 VDC and both 15-V outputs are loaded to 50 mA.



10 V/div, 1 µs/div

Figure 4-5. FET Switch Node Voltage SW

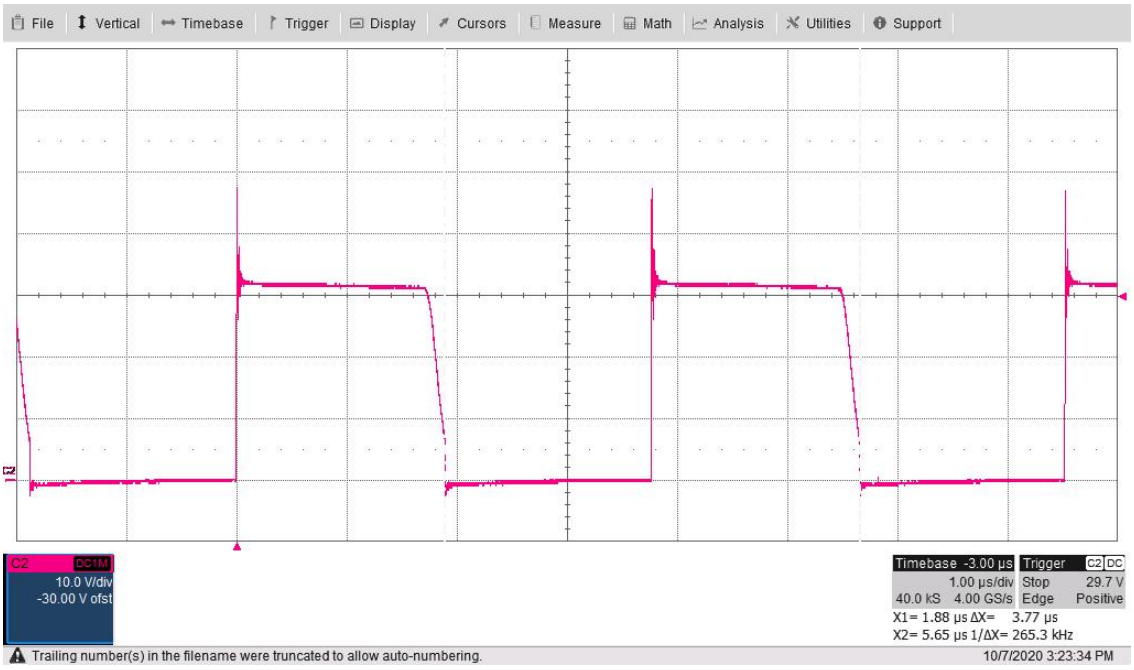
The following image shows the FET switch node voltage SW (Red) at TP4. The input voltage is 12 VDC and both 15-V outputs are loaded to 10 mA.



10 V/div, 1 µs/div

Figure 4-6. FET Switch Node Voltage SW

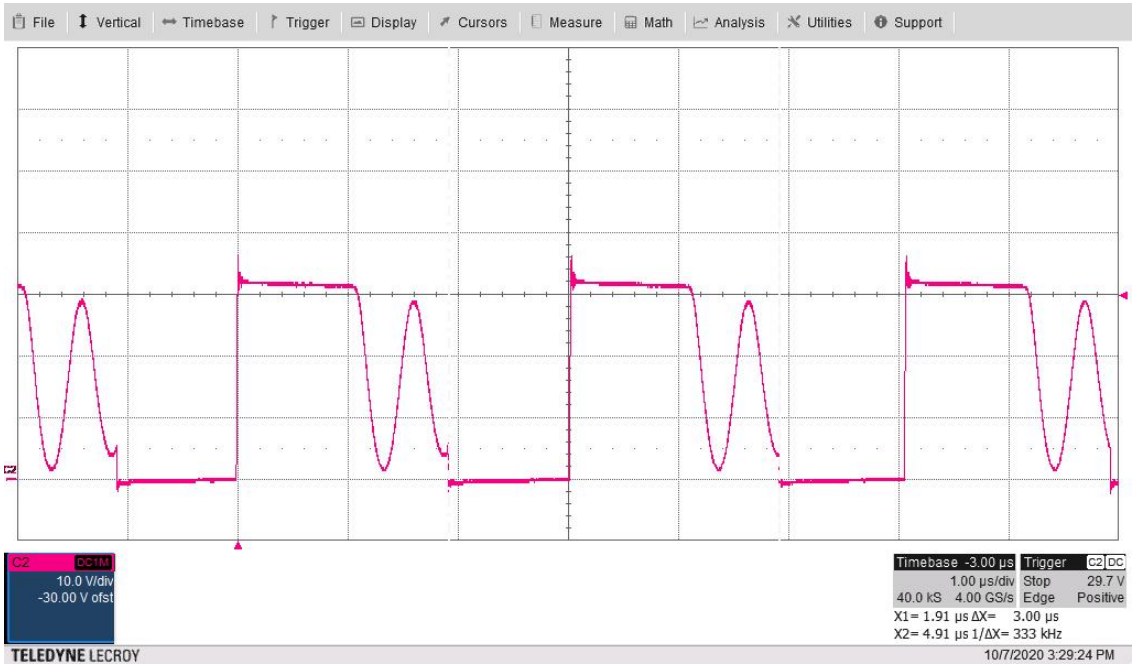
The following image shows the FET switch node voltage SW (Red) at TP4. The input voltage is 15 VDC and both 15-V outputs are loaded to 100 mA.



10 V/div, 1 µs/div

Figure 4-7. FET Switch Node Voltage SW

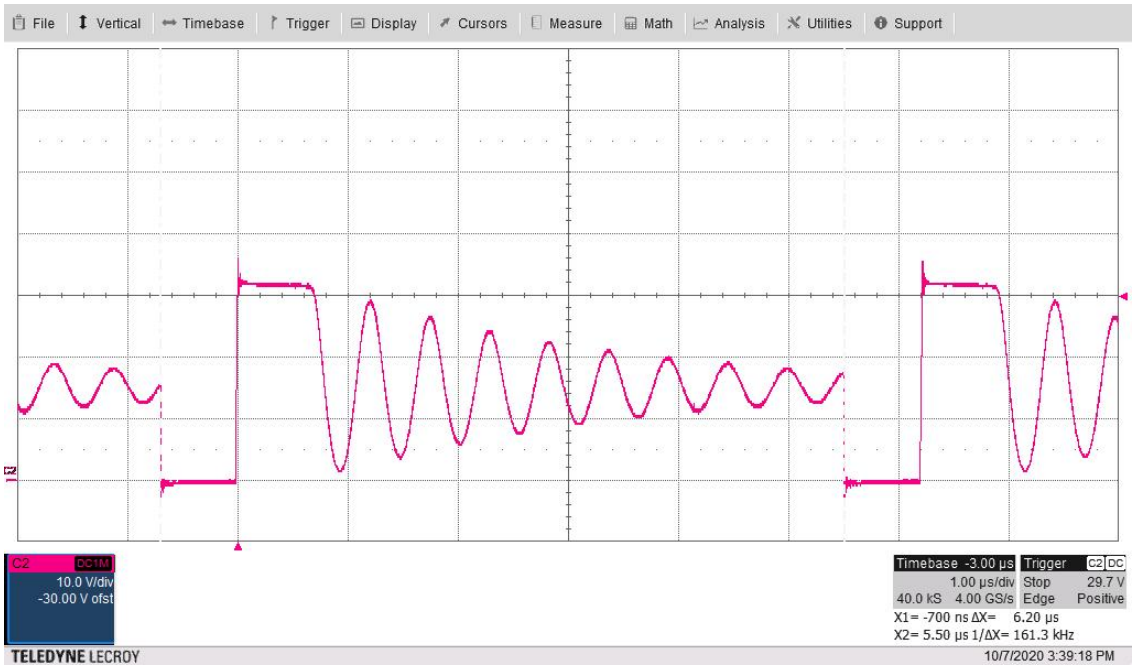
The following image shows the FET switch node voltage SW (Red) at TP4. The input voltage is 15 VDC and both 15-V outputs are loaded to 50 mA.



10 V/div, 1 µs/div

Figure 4-8. FET Switch Node Voltage SW

The following image shows the FET switch node voltage SW (Red) at TP4. The input voltage is 15 VDC and both 15-V outputs are loaded to 10 mA.



10 V/div, 1 µs/div

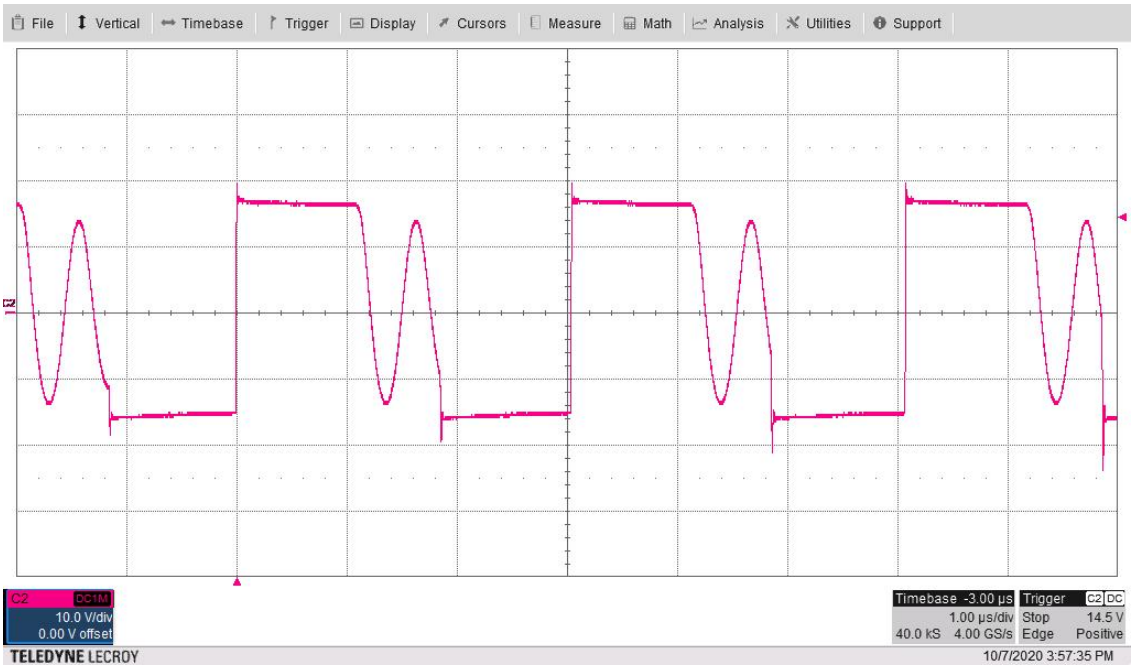
Figure 4-9. FET Switch Node Voltage SW

The following image shows the secondary winding voltage of the transformer at T1- pin 5 (Red) with respect to T1 – pin 6. The input voltage is 15 VDC and both 15-V outputs are loaded to 100 mA.

10 V/div, 1 µs/div

Figure 4-10. Secondary Winding Voltage of the Transformer

The following image shows the secondary winding voltage of the transformer at T1- pin 5 (Red) with respect to T1 – pin 6. The input voltage is 15 VDC and both 15-V outputs are loaded to 50 mA.

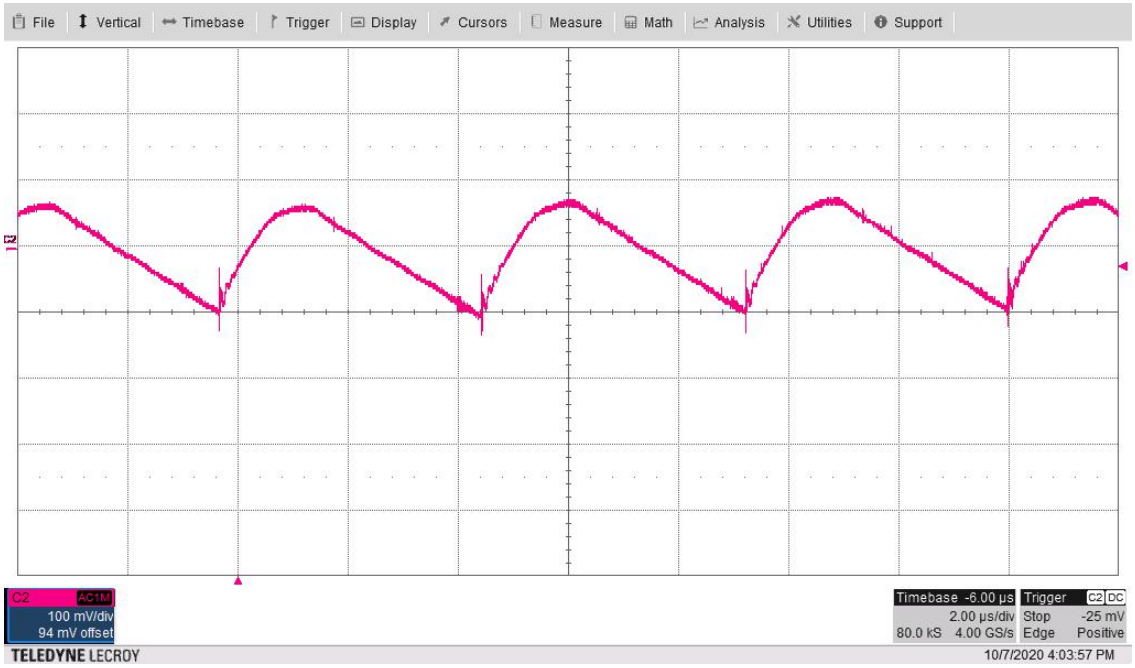


10 V/div, 1 µs/div

Figure 4-11. Secondary Winding Voltage of the Transformer

4.3 Output Voltage Ripple

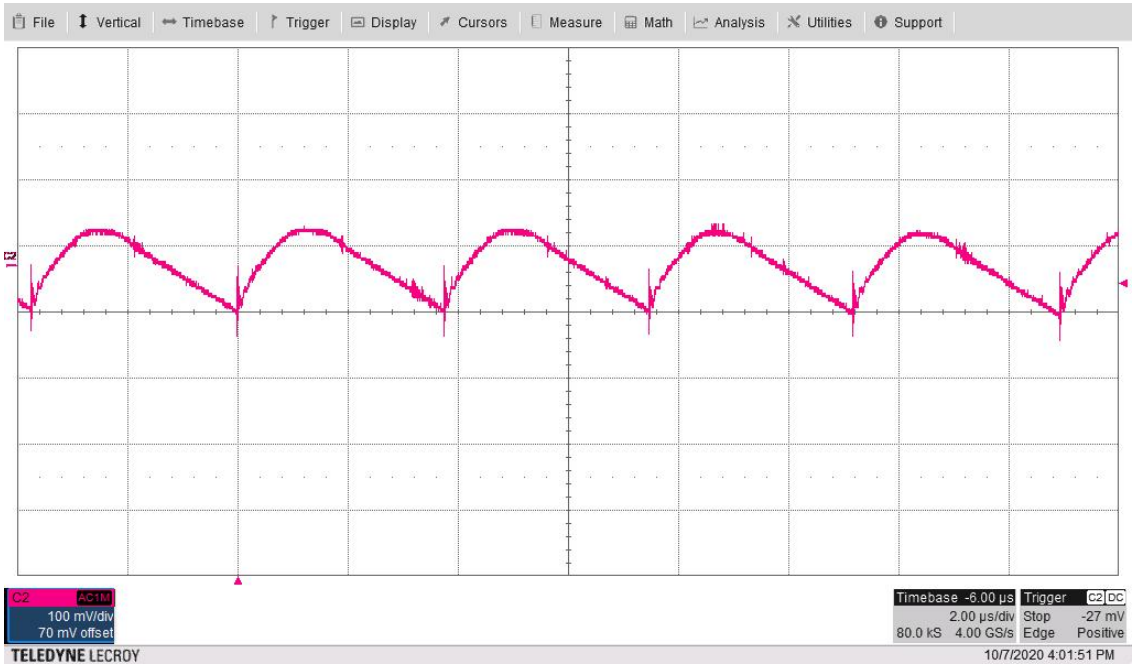
The following image shows the 15-V output ripple voltage (AC coupled). The input voltage is 12 VDC and both 15-V outputs are loaded to 100 mA.



100 mV/div, 2 µs/div

Figure 4-12. Ripple Voltage, 15-V Output

The following image shows the 15-V output ripple voltage (AC coupled). The input voltage is 15 VDC and both 15-V outputs are loaded to 100 mA.

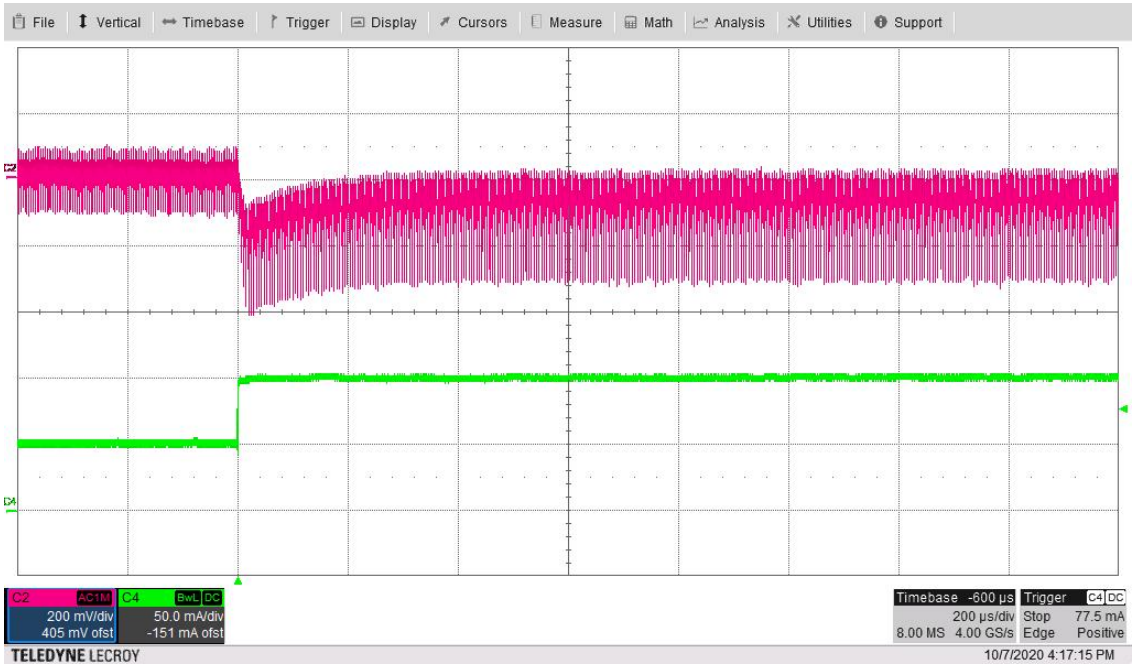


100 mV/div, 2 µs/div

Figure 4-13. Ripple Voltage, 15-V Output

4.4 Load Transients

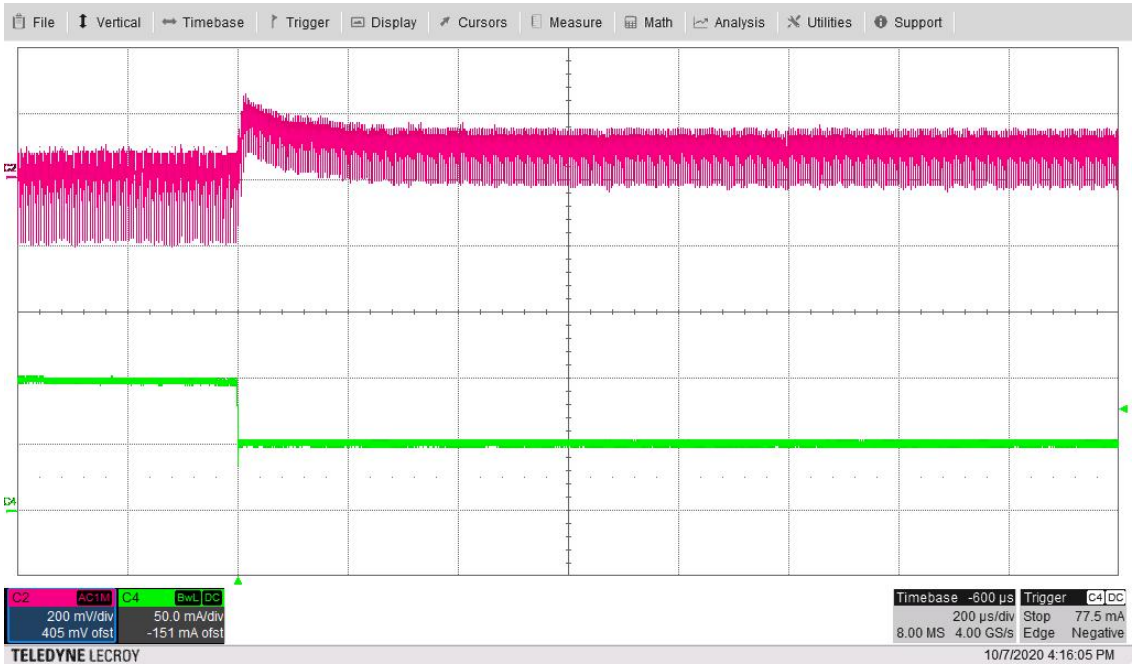
The following image shows the 15-V output voltage (AC coupled, Red) when the load current (Green) is stepped from 50 mA to 100 mA. The second output is loaded to 100 mA and the input voltage is 12 VDC.



200 mV/div, 50 mA/div, 200 µs/div

Figure 4-14. Load Transients, 15-V Output Voltage

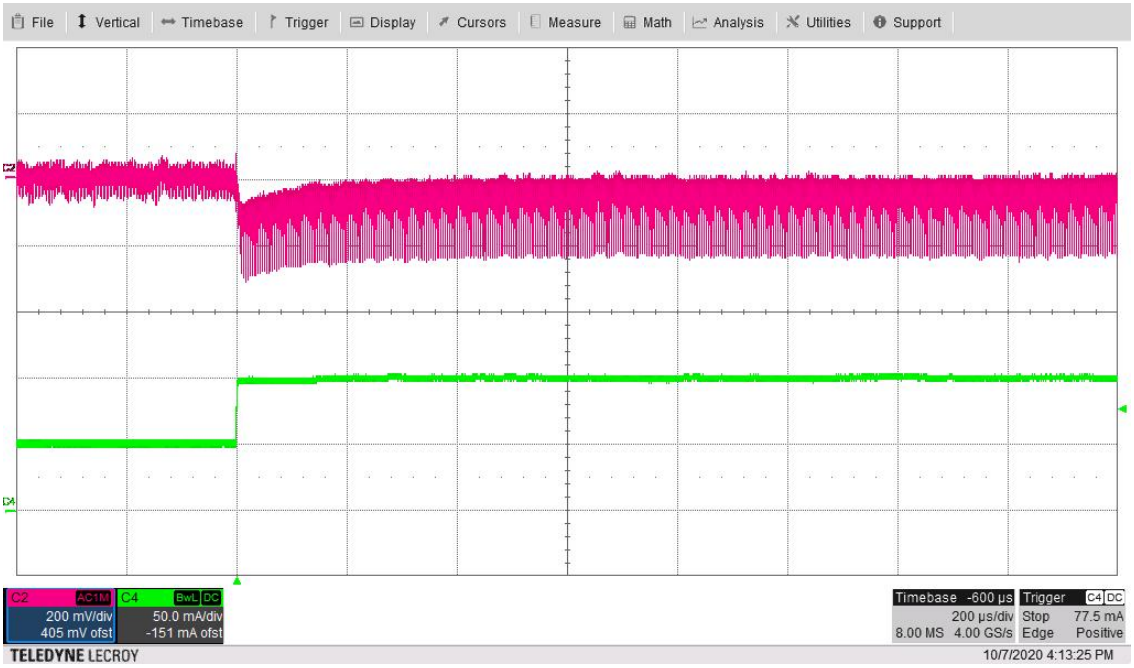
The following image shows the 15-V output voltage (AC coupled, Red) when the load current (Green) is stepped from 100 mA to 50 mA. The second output is loaded to 100 mA and the input voltage is 12 VDC.



200 mV/div, 50 mA/div, 200 µs/div

Figure 4-15. Load Transients, 15-V Output Voltage

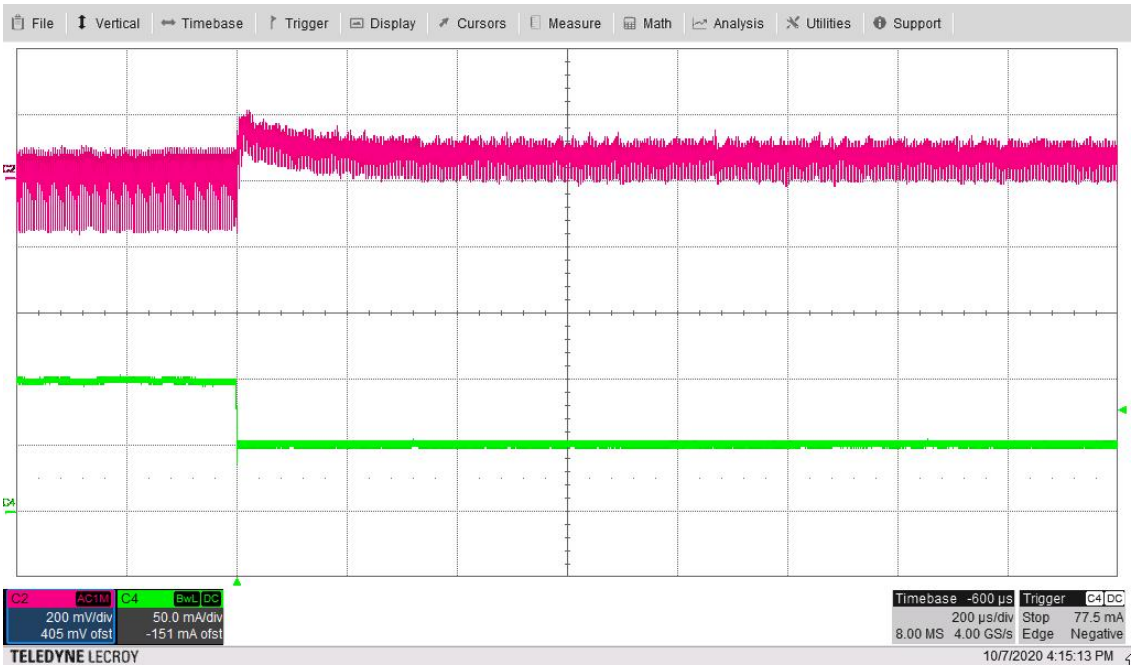
The following image shows the 15-V output voltage (AC coupled, Red) when the load current (Green) is stepped from 50 mA to 100 mA. The second output is loaded to 100 mA and the input voltage is 15 VDC.



200 mV/div, 50 mA/div, 200 µs/div

Figure 4-16. Load Transients, 15-V Output Voltage

The following image shows the 15-V output voltage (AC coupled, Red) when the load current (Green) is stepped from 100 mA to 50 mA. The second output is loaded to 100 mA and the input voltage is 15 VDC.



200 mV/div, 50 mA/div, 200 µs/div

Figure 4-17. Load Transients, 15-V Output Voltage

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