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TI Designs
RTD Temperature Transmitter for 2-Wire, 4 to 20-mA Current Loop Systems

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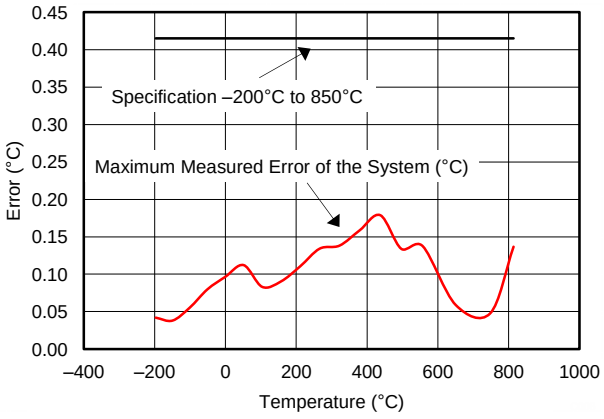
Design Resources

TIDA-0095	Tool Folder Containing Design Files
ADS1220	Product Folder
DAC161S997	Product Folder
MSP430G2513	Product Folder
TPS7A4901	Product Folder



Design Features

The RTD Temperature Transmitter is a 4 to 20-mA current-loop reference design that supports RTD probes.

- Input Compatible with 2, 3, and 4-wire RTD Probes
- 4 to 20-mA current-loop signal output
- Low power consumption of 1.4 mA (with RTD biasing currents) is ideal for loop powered systems
- Output resolution: 0.25 µA
- Maximum measured error 0.11°C (–200°C to 200°C), 0.17°C (–200°C to 850°C)
- Power-supply influence of 0.3 µA from 10-30 V
- Temperature range for RTD –200°C to 850°C
- IEC61000-4-2: ESD: Air Discharge: ±8 kV Class A
- IEC61000-4-4: EFT ±2 kV Class A

Featured Applications

- Factory Automation and Process Control
- Sensors and Field Transmitters
- Building Automation
- Portable Instrumentation

TI E2E™ Community

ASK Our Analog Experts
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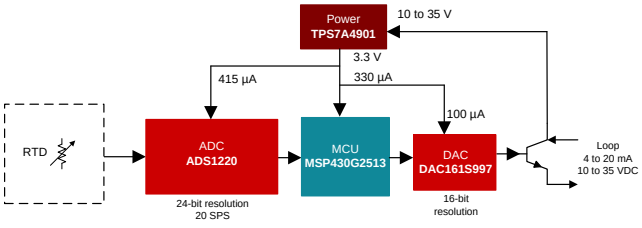

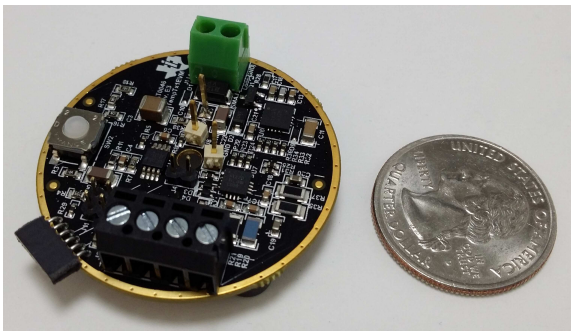

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1 Key System Specifications

Parameter	Specifications and Features		Details
Probe Type	2-wire, 3-wire, and 4-wire RTD MSP430 Firmware supports PT-100 RTD by default		See Section 5.3
Output Signal	4 to 20 mA		See Table 8
Temperature Range for RTD	–200°C to 850°C		See Figure 47
Power Supply Range	10 to 35-V DC		See Section 7
Error Current	Low: 3.375 mA (typical) High: 21.75 mA (typical)		See Figure 23
Loop Power Consumption	1.4 mA (typical) of DAC, ADC, MSP, and LDO including 500 µA of RTD biasing currents		See Section 6.9
Reverse Polarity on Input Power	Supported		See Section 4.9 and Section 6.8
Ambient Temperature	–40°C to 85°C		See Section 8
Input Resolution	0.029°C (noise free resolution of the analog front-end) ADS1220: PGA gain = 16, V_{REF} = 1.62 V Sampling rate: 20 samples per second (SPS)		See Section 6.2
Output Resolution	0.25 µA		See Section 6.4
System Accuracy or Maximum Measured Error	0.11°C (–200°C to 200°C) 0.17°C (–200°C to 850°C)		See Section 6.6
Power Supply Influence	Deviation of 0.3 µA from 10 V to 30 V		See Section 6.7
IEC ESD on Loop Power	IEC61000-4-2, ESD	Horizontal coupling plane	See Section 4.11 and Section 6.10
		Vertical coupling Plane: ±4 kV — Class A	
		Air discharge: ±8 kV — Class A	
IEC EFT on Loop Power	IEC61000-4-4	EFT: ±2 kV — Class A	
Calibration	ADC	Offset and gain calibration	See Section 4.6 and Section 4.7
	DAC		
RTD non-linearity	–200°C to 850°C lookup table with 1°C resolution implemented in the MSP430 Firmware to resolve non-linearity of RTD or the Callendar-Van Dusen relationship between resistance and temperature.		See Section 4.2
Connectivity Interface	UART, via a USB to UART dongle		See Figure 24
Form Factor	1.588-inch diameter, circular board		See Figure 61

2 System Description

This comprehensive design provides a complete system that measures and processes temperature signals inputs from 2-wire, 3-wire, and 4-wire resistance temperature detectors (RTDs) and outputs a 4 to 20-mA current-loop signal corresponding to the temperature processed from the RTD inputs (see Figure 1). The reference design is intended for process measurement applications in factory automation, field transmitters, and building automation. With less-than 0.17°C maximum measured error over –200°C to 850°C, extremely low loop power consumption 1.4 mA (typical) including RTD biasing currents and IEC61000 pre compliance testing, this design significantly reduces the design time for development of high-accuracy temperature transmitter systems. This design also addresses system-level calibration, both offset and gain calibration, to improve ADC and DAC accuracy. Linear interpolation is also included in this design to address the non-linearity of the RTD element. The reference design provides a complete design guide for the hardware and firmware design of a temperature transmitter with a 4 to 20-mA current output in a small industrial form factor (see Figure 57). The design files include schematics, Bill of Materials (BOM), layer plots, Altium files, Gerber Files, and MSP430 Firmware.

The overall system-level requirements for this design were: the system must perform precise ratiometric RTD measurements with 4 to 20-mA current loop accuracy to meet the overall system-error specification, the maximum measured error of the system must be below approximately 0.4°C between –200°C and 850°C, low quiescent current of the system must meet system alarm requirements of less than 3.5 mA, small overall form factor, low-cost and low-power processor capable of performing gain and offset calibration of the ADC and DAC and linear interpolation using a RTD lookup table. To translate the above requirements to sub-system level, the requirements of ADC, DAC, processor, and power management are listed.

ADC

- ADC with current excitation and buffered reference inputs for implementing a ratiometric measurement
- Low power to meet the loop power requirements
- Low noise high input impedance PGA
- Small package to fit in the form factor of the design
- Simultaneous 50-Hz and 60-Hz rejection to filter the noise from power mains
- Target resolution of 10 times lower than the overall system accuracy of 0.4°C at –200°C and 850°C

  The ADS1220 device, with 24-bit sigma-delta ADC was selected because the device meets the listed requirements for the ADC subsystem.

DAC

- Digital input to analog output that supports 4 to 20-mA current loop
- Target resolution of 10 times lower than the overall system accuracy of 0.4°C at –200°C and 850°C
- Small package to fit in the form factor of the design
- Similar interface for MCU control as ADC

  The DAC161S997 device, with a 16-bit resolution was selected because the device meets the listed requirements for the DAC subsystem.

Processor

- Floating point math to implement all the calculations involving gain and offset calibration
- 16k Flash to support floating point math as well as the PT-100 lookup table
- UART interface for COM port communication for debug purposes
- SPI interface or equivalent to communicate to ADC and DAC
- Low cost and low power

  The value-line MSP430 device was selected for overall low-cost design. The 16k flash option was selected to meet the listed requirements for the processor.

Power Management

- Generates 3.3 V nominal from 10 to 35-V supply
- High PSRR, low noise to keep the power supply influence on the system accuracy low
- Small form factor

- Low θ_{JA}, in case of low-dropout regulator (LDO) selection, to ensure that the junction temperature is not exceeded in the application

  The TPS7A4901 device (LDO) was selected because the device meets the listed requirements of the power management.

The highly-integrated devices in this design deliver a 4-chip system solution. The analog-to-digital converter (ADC) from Texas Instruments, the ADS1220 device (see Figure 2), interfaces with a 2-wire, 3-wire, or 4-wire RTD probe and the MSP430™ microcontroller (see Figure 4). The microcontroller (MCU) runs the application firmware including the algorithms for system calibration (see Section 4.6, Section 4.7, and Section 4.2). The output is controlled by a DAC from TI, the DAC161S997 device (see Figure 3), that interfaces with the MSP430 and delivers a 4 to 20-mA output current proportional to the RTD temperature reading (see Figure 45). TI's low dropout regulator (LDO), the TPS7A4901 device, supplies the system with power (See Figure 5). The TPS7A4901 device has an input-voltage range of 3 to 36-V, very low noise (15.4 μV_{RMS}, 72-dB PSRR), and high thermal performance. The design also incorporates reverse-polarity protection capability as well as IEC61000-4-2 and IEC61000-4-4 protection on the loop power input.

2.1 ADS1220

The ADS1220 device (also referred to as the ADC) is a precision, 24-bit, analog-to-digital converter (ADC) that offers many integrated features to reduce system cost and component count in applications measuring small sensor signals. The device features two differential or four single-ended inputs through a flexible input multiplexer (mux), a low-noise programmable gain amplifier (PGA), two programmable excitation current sources, a voltage reference, an oscillator, a low-side switch, and a precision temperature sensor.

The device performs conversions at data rates of up to 2000 samples-per-second (SPS) with single-cycle settling. At 20 SPS the digital filter offers simultaneous 50-Hz and 60-Hz rejection for noisy industrial applications. The internal PGA offers gains of up to 128 V/V. This PGA makes the ADS1220 ideally-suited for applications measuring small sensor signals, such as resistance temperature detectors (RTDs), thermocouples, thermistors, and bridge sensors. The device supports measurements of pseudo-differential or fully-differential signals when using the PGA. Alternatively, the device can be configured to bypass the internal PGA while still providing high input impedance and gains of up to 4 V/V, allowing for single-ended measurements.

The power consumption is as low as 120 µA when operating in duty-cycle mode with the PGA disabled. Communication to the device is established through a Mode 1 SPI-compatible interface. The ADS1220 device is offered in a leadless QFN-16 or a TSSOP-16 package and specified over a temperature range of –40°C to 125°C. For the ADS1220 block diagram, see Figure 2.

2.2 DAC161S997

The DAC161S997 device (also referred to as the DAC) is a very low power 16-bit ΣΔ digital-to-analog converter (DAC) for transmitting an analog output current over an industry standard 4 to 20-mA current loop. The DAC161S997 device has a simple 4-wire SPI for data transfer and configuration of the DAC functions. To reduce power and component count in compact loop-powered applications, the DAC161S997 device contains an internal ultra-low power voltage reference and an internal oscillator. The low power consumption of the DAC161S997 device results in additional current being available for the remaining portion of the system. The loop drive of the DAC161S997 device interfaces to a Highway Addressable Remote Transducer (HART) modulator, allowing injection of FSK modulated digital data into the 4 to 20-mA current loop. This combination of specifications and features makes the DAC161S997 device ideal for 2- and 4-wire industrial transmitters. The DAC161S997 is available in a 16-pin 4 mm × 4 mm WQFN package and is specified over the extended industrial temperature range of –40°C to 105°C. For the DAC161S997 block diagram, see Figure 3.

2.3 MSP430G2513

The Texas Instruments MSP430 family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 µs.

The MSP430G2513 device is an ultra-low-power mixed signal microcontroller with built-in 16-bit timers, built-in communication capability using the universal serial communication interface support as well as a versatile analog comparator.

Typical applications include low-cost sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system. For the MSP430G2513 block diagram, see Figure 4.

2.4 TPS7A4901

The TPS7A4901 device (also referred to as the LDO) is a positive, high-voltage (36 V), ultralow noise (15.4 μV_{RMS}, 72 dB PSRR) linear regulators capable of sourcing a load of 150 mA.

These linear regulators include a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other features available include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A49xx family is designed using bipolar technology, and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This design makes it an excellent choice to power operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry.

In addition, the TPS7A49xx family of linear regulators is suitable for post dc/dc converter regulation. By filtering out the output voltage ripple inherent to dc/dc switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications. For the TPS7A4901 block diagram, see Figure 5.

3 Block Diagram

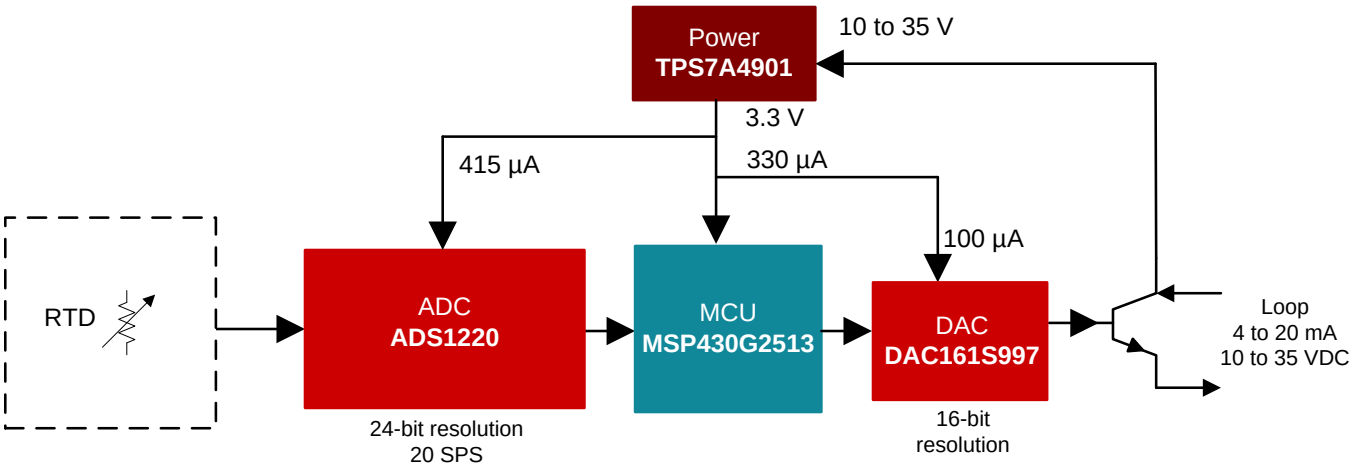


Figure 1. Temperature Transmitter System Block Diagram

3.1 Highlighted Products

The RTD Temperature Transmitter Reference Design features the following devices:

- ADS1220
  - Low-power, low-noise, 24-bit, analog-to-digital converter for small-signal sensors
- DAC161S997
  - SPI 16-bit precision DAC for 4 to 20-mA loops
- MSP430G2513
  - MSP4302513 mixed-signal microcontroller
- TPS7A4901
  - V_I 3-V to 36-V, 150-mA, ultra-low noise, high PSRR, low-dropout linear regulator

For more information on each of these devices, see the respective product folders at www.TI.com.

3.1.1 ADS1220

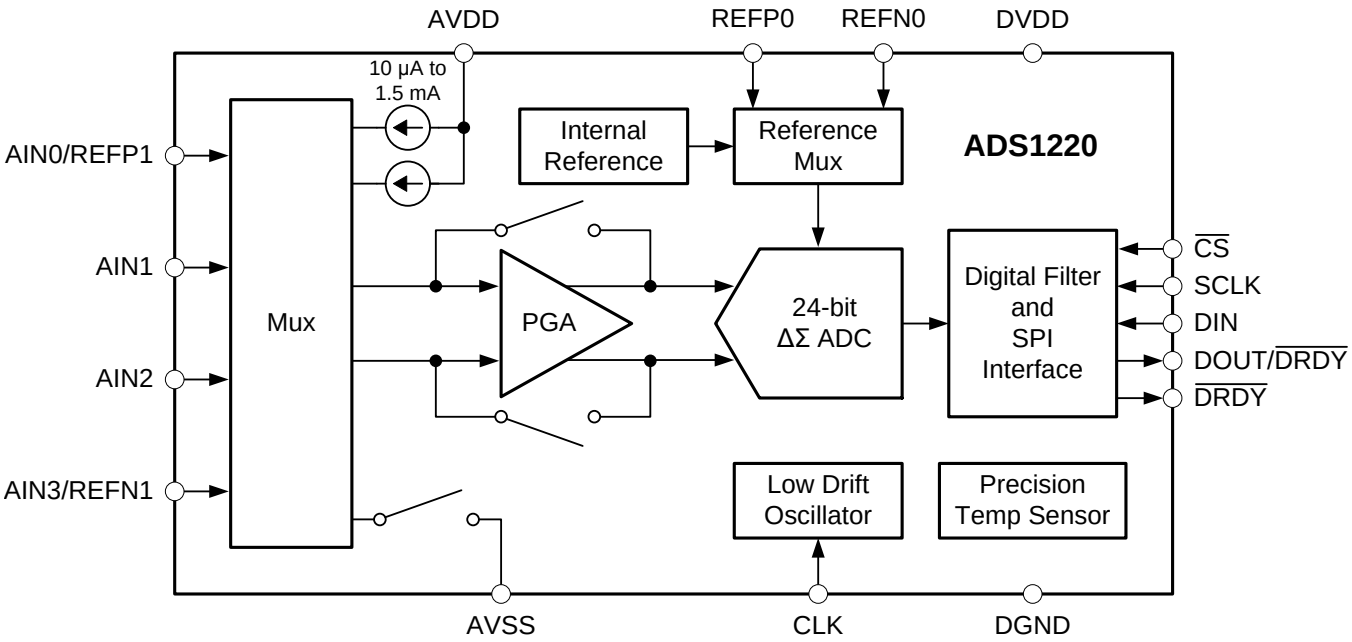


Figure 2. ADS1220 Block Diagram

- Low current consumption:
  - Duty-cycle mode: 120 µA
  - Normal mode: 415 µA
- Wide supply range: 2.3 V to 5.5 V
- Programmable gain: 1 V/V to 128 V/V
- Programmable data rates: Up to 2 kSPS
- Simultaneous 50-Hz and 60-Hz rejection at 20 SPS with a single-cycle settling digital filter
- Low-noise PGA: 90 nV_{RMS} at 20 SPS
- Dual-matched programmable current-sources: 10 µA to 1500 µA
- Internal 2.048-V reference: 5 ppm/°C (typical) drift
- Internal Oscillator: 2% (maximum) Accuracy
- Internal temperature sensor
- Two differential or four single-ended inputs
- SPI™-compatible interface
- Package: 3,5 mm × 3,5 mm × 0,9 mm QFN

3.1.2 DAC161S997

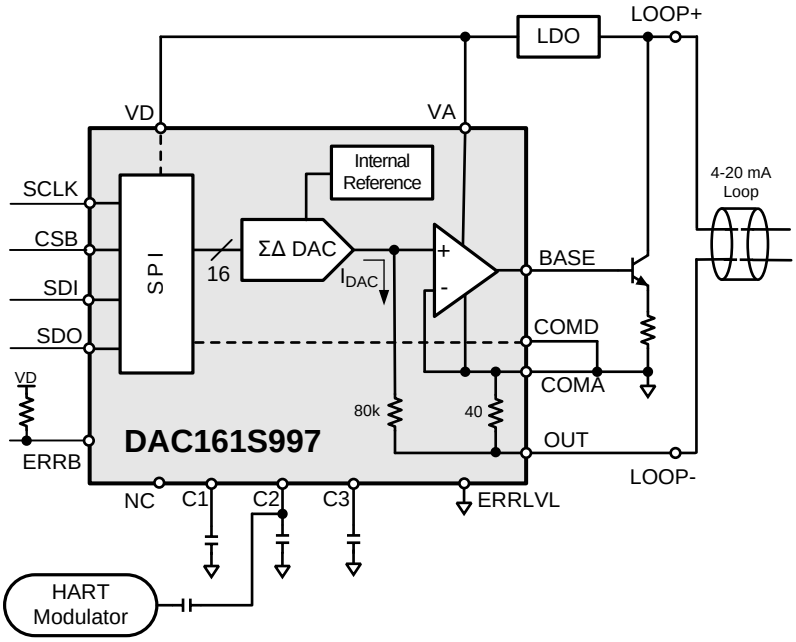


Figure 3. DAC161S997 Block Diagram

- 16-bit resolution
- Very-low supply current of 100 µA
- 5 ppmFS/°C gain error
- Pin-programmable power-up condition
- Loop-error detection and reporting
- Programmable output-current error levels
- Simple HART modulator interfacing
- Highly integrated feature set in a small-footprint WQFN-16 (4 × 4 mm, 0,5 mm pitch)

3.1.3 MSP430G2513

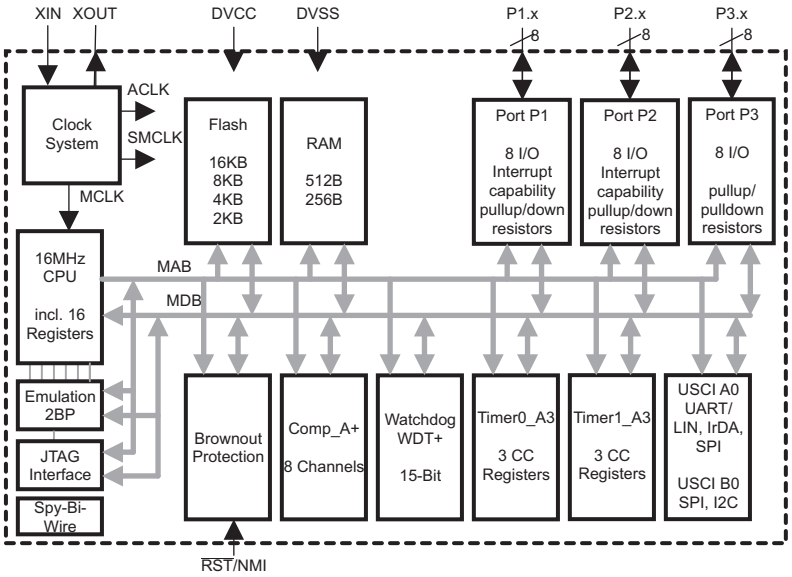


Figure 4. MSP430G2513 Block Diagram

- Low supply-voltage range: 1.8 V to 3.6 V
- Ultra-low power consumption
  - Active mode: 230 µA at 1 MHz, 2.2 V
  - Standby mode: 0.5 µA
  - Off mode (RAM retention): 0.1 µA
- Five power-saving modes
- Ultra-fast wake-up from standby mode in less than 1 µs
- 16-Bit RISC architecture, 62.5-ns instruction cycle time
- Basic clock module configurations
  - Internal frequencies up to 16 MHz with four calibrated frequency
  - Internal very-low-power low-frequency (LF) oscillator
  - 32-kHz crystal
  - External digital clock source
- Two 16-Bit Timer_A with three capture and compare registers
- Up to 24 capacitive-touch enabled I/O pins
- Universal serial communication interface (USCI)
  - Enhanced UART supporting auto baud-rate detection (LIN)
  - IrDA encoder and decoder
  - Synchronous SPI
  - I^2C
- On-chip comparator for analog signal-compare function or slope analog-to-digital (A-D) conversion
- 10-Bit 200-ksps analog-to-digital (A-D) converter with internal reference, sample-and-hold, and autoscan
- Brownout detector
- Serial onboard programming, no external programming voltage needed, programmable code protection by Security Fuse
- On-chip emulation logic with Spy-Bi-Wire interface
- Package options:

  - TSSOP: 20 Pin, 28 Pin
  - PDIP: 20 Pin
  - QFN: 32 Pin
- For complete module descriptions, see the *MSP430x2xx Family User's Guide* (SLAU144)

3.1.4 TPS7A4901

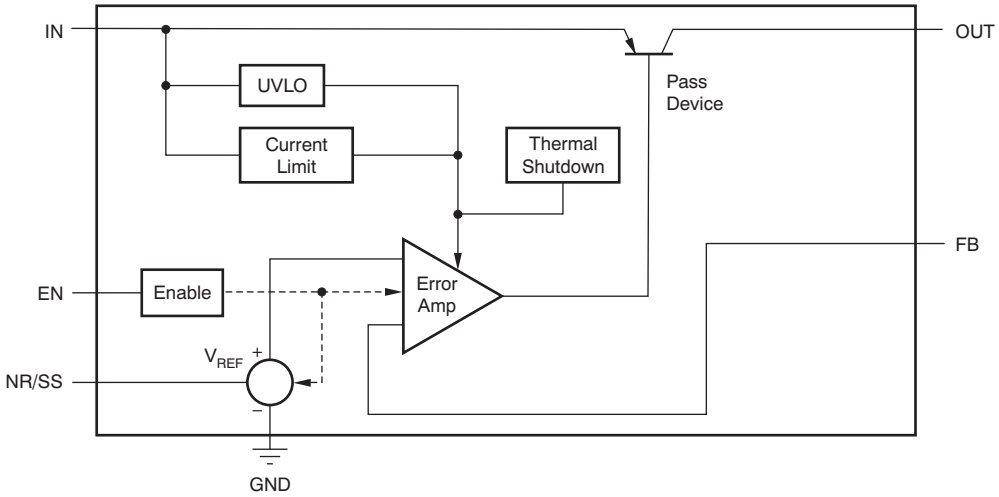


Figure 5. TPS7A4901 Block Diagram

- Input-voltage range: 3 V to 36 V
- Noise:
  - 12.7 μV_{RMS} (20 Hz to 20 kHz)
  - 15.4 μV_{RMS} (10 Hz to 100 kHz)
- Power-supply ripple rejection:
  - 72 dB (120 Hz)
  - ≥ 52 dB (10 Hz to 400 kHz)
- Adjustable output: 1.194 V to 33 V
- Output current: 150 mA
- Dropout voltage: 260 mV at 100 mA
- Stable with ceramic capacitors ≥ 2.2 µF
- CMOS logic-level-compatible Enable pin
- Built-in, fixed, current-limit and thermal shutdown protection
- Available in high thermal performance MSOP-8 PowerPAD™ package
- Operating temperature range: –40°C to 125°C

4 System Design Theory

4.1 RTD Overview

A resistance temperature detector (RTD) is a sensing element made of a metal with predictable resistance characteristics over temperature. The temperature of an RTD is therefore calculated by measuring the resistance. RTD sensors offer wide temperature ranges, good linearity, and excellent long-term stability and repeatability which makes RTD sensors suitable for many precision applications.

The relationship between the resistance and temperature of an RTD is defined by the Callendar-Van Dusen (CVD) equations (see Section 4.2).

Most RTD applications use a current source as excitation for the RTD element. By driving a known current through the RTD, a voltage potential is developed that is proportional to the resistance of the RTD and the excitation current. This voltage potential is amplified and then fed to the inputs of an ADC, which converts the voltage into a digital output code that can be used to calculate the RTD resistance.

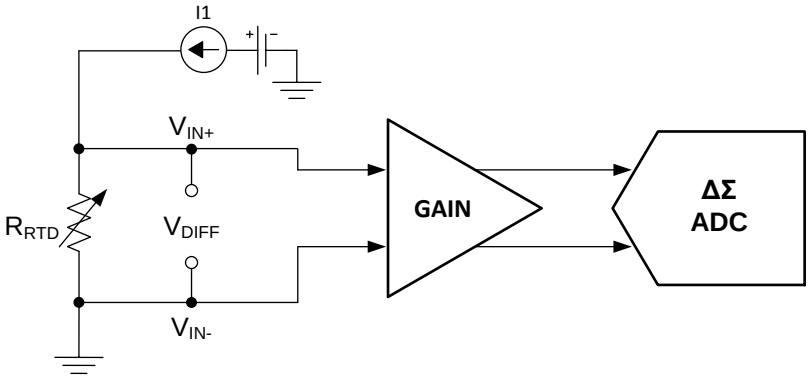


Figure 6. Simplified RTD Application

4.2 Callendar-Van Dusen Equations

4.2.1 PT-100 RTD Information

The PT-100 RTD is a platinum-based RTD sensor. Platinum is a noble metal and offers excellent performance over a wide temperature range. Platinum also features the highest resistivity of commonly used RTD materials, requiring less material to create desirable resistance values. The PT-100 RTD has an impedance of 100 Ω at 0°C and approximately 0.385 Ω of resistance change per 1°C change in temperature. This impedance results in 18.52 Ω at –200°C and 390.481 Ω at 850°C. Higher-valued resistance sensors, such as PT-1000 or PT-5000, can be used for increased sensitivity and resolution.

Class-A RTDs are a good choice for this application to provide good pre-calibration accuracy and long-term stability. A Class-A RTD has less than 0.5°C of error at 100°C without calibration and the long-term stability makes accurate infrequent calibration possible. Table 1 displays the tolerance, initial accuracy, and resulting error at 100°C for the five main classes of RTDs.

Table 1. RTD Class Tolerance Information

Tolerance Class (DIN-IEC 60751)	Tolerance Values (°C)	Resistance at 0°C (Ω)	Error at 100°C (°C)
AAA(1)	± (0.03 + 0.0005 × T)	100 ± 0.012	± 0.08
AA	± (0.01 + 0.0017 × T)	100 ± 0.04	± 0.27
A	± (0.15 + 0.002 × T)	100 ± 0.06	± 0.35
B	± (0.3 + 0.005 × T)	100 ± 0.12	± 0.8
C	± (0.6 + 0.01 × T)	100 ± 0.24	± 1.6

(1) AAA is not included in the DIN-IEC 60751 specification but is an industry accepted tolerance for performance demanding applications.

For positive temperatures the CVD equation is a second-order polynomial as shown in Equation 1.

$$RTD(T) = R_0 \times [1 + A(T) + B(T)^2] \quad (1)$$

For negative temperatures from –200°C to 0°C, the CVD equation expands to a fourth-order polynomial shown in Equation 2.

$$RTD(T) = R_0 \times [1 + A(T) + B(T)^2 + C(T)^3 \times (T - 100)] \quad (2)$$

The coefficients in the Callendar-Van Dusen equations are defined by the IEC-60751 standard. R_0 is the resistance of the RTD at 0°C. For a PT-100 RTD with an alpha (α) of 0.00385, the coefficients are shown in Equation 3.

$$R_0 = 100\ \Omega$$

$$\begin{aligned} A &= 3.9083 \times 10^{-3}\,°C \\ B &= -5.775 \times 10^{-7}\,°C \\ C &= -4.183 \times 10^{-12}\,°C \end{aligned} \quad (3)$$

The change in resistance of a PT-100 RTD from –200°C to 850°C is shown in Figure 7.

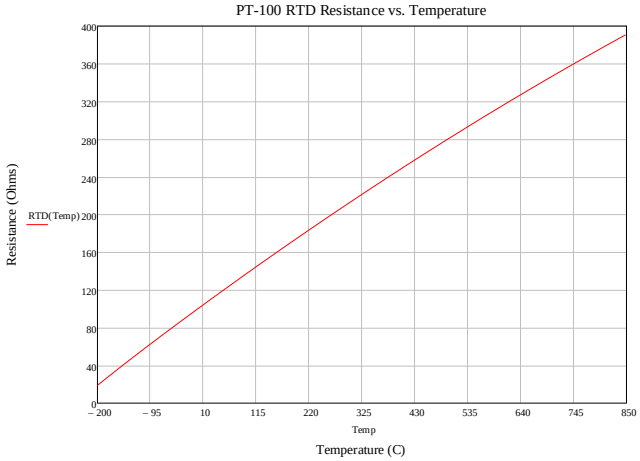


Figure 7. PT-100 RTD Resistance from –200°C to 850°C

While the change in RTD resistance is fairly linear over small temperature ranges, Figure 8 shows the resulting non-linearity if an end-point fit is made to the curve shown in Figure 7. The results show approximately 0.375% non-linearity and illustrate the necessity for digital calibration.

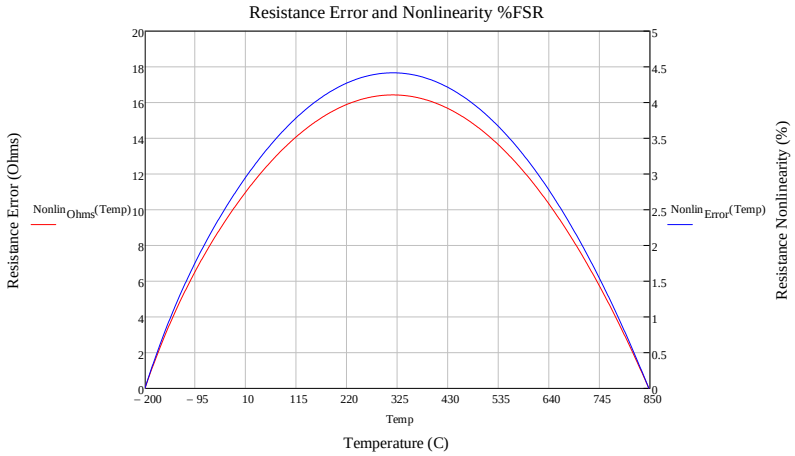


Figure 8. PT-100 RTD Non-Linearity from –200°C to 850°C

In this reference design, a lookup table for the PT-100 (see Figure 32 and Figure 33) with a resolution of 1°C is used for linear interpolation. The RTD value is computed after offset and gain calibration. Then this RTD value is used in linear interpolation of the line segment involving two surrounding points in the PT-100 table. If additional accuracy is desired, a table with more points with less than 1°C or more accurate curve fit can be stored as a look up reference table.

4.3 ADC RTD Measurement

The ADS1220 device integrates all required features (such as dual-matched programmable current sources, buffered reference inputs, and PGA) to ease the implementation of ratiometric 2-wire, 3-wire, and 4-wire RTD measurements.

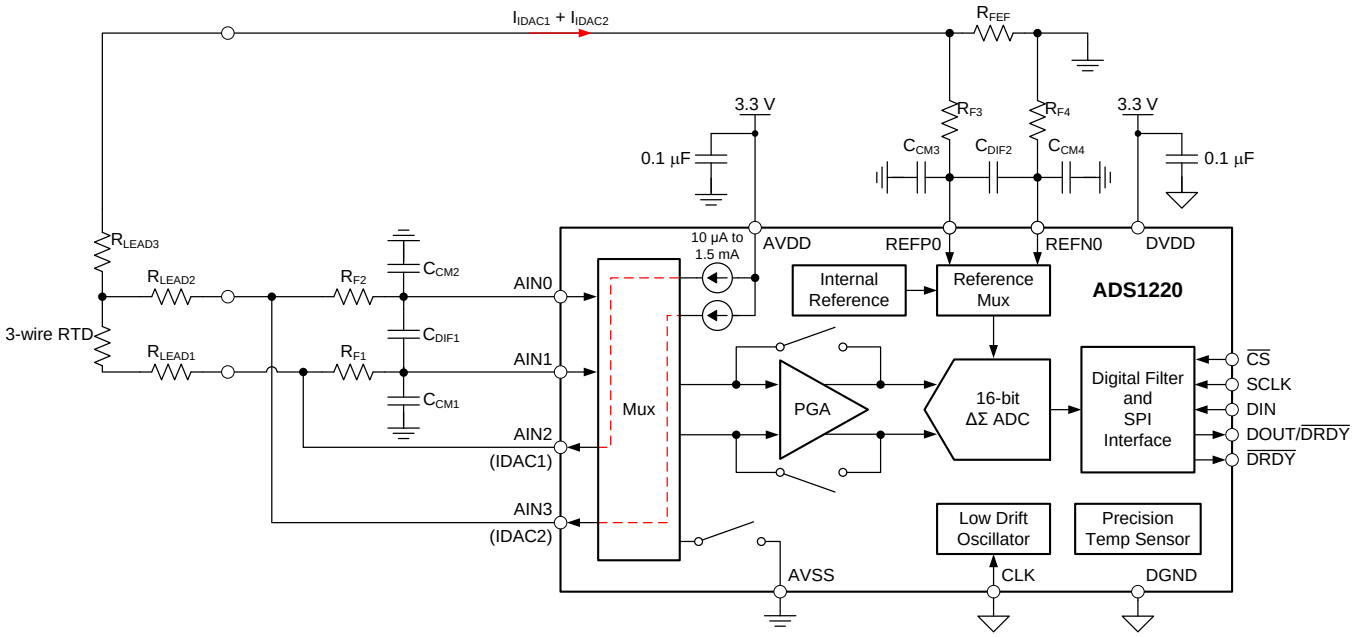


Figure 9. 3-Wire RTD Measurement

The circuit in Figure 9 employs a ratiometric measurement approach. In other words, the sensor signal (the voltage across the RTD) and the reference voltage for the ADC are derived from the same excitation source. Therefore, errors resulting from temperature drift or noise cancel out because these errors are common to both the sensor signal and the reference.

In order to implement a ratiometric 3-wire RTD measurement using the ADS1220 device, IDAC1 is routed to one of the excitation leads of the RTD while IDAC2 is routed to the second excitation lead. Both currents have the same value, which is programmable by bits IDAC[2:0] in the configuration register. The design of the ADS1220 device ensures that both IDAC values are closely matched, even across temperature. The sum of both currents flows through a low-drift reference resistor, R_{REF}. The voltage, V_{REF}, generated across the reference resistor is shown in Equation 4. Because IDAC1 = IDAC2, Equation 5 is then used as the ADC reference voltage.

$$V_{REF} = (I_{DAC1} + I_{DAC2}) \times R_{REF} \quad (4)$$

$$V_{REF} = 2 \times I_{DAC1} \times R_{REF}$$

- I_{DAC1} and I_{DAC2} based on default firmware: 250 µA, R_{REF} = 3.24 kΩ
- V_{REF} = 1.62 V (5)

Equation 6 assumes for the moment that the individual lead resistance values of the RTD (R_{LEADx}) are zero. Only IDAC1 excites the RTD to produce a voltage V_{RTD}, which is proportional to the temperature dependable RTD value and the IDAC1 value.

$$V_{RTD} = R_{RTD}\,(\text{Temperature}) \times I_{IDAC1} \quad (6)$$

The ADS1220 device internally amplifies the voltage across the RTD using the PGA and compares the resulting voltage against the reference voltage to produce a digital output code, which is proportional to Equation 7 and Equation 9.

$$\text{Code} \propto V_{RTD} \times PGA / V_{REF} \quad (7)$$

$$\text{Code} \propto (R_{RTD}\,[\text{Temperature}] \times I_{IDAC1} \times PGA) / (2 \times IDAC1 \times R_{REF}) \quad (8)$$

$$\text{Code} \propto (R_{RTD}\,[\text{Temperature}] \times PGA) / (2 \times R_{REF}) \quad (9)$$

As shown in Equation 9, the output code depends only on the value of the RTD, the PGA gain and the reference resistor (R_{REF}), but not on the IDAC1 value. The absolute accuracy and temperature drift of the excitation current therefore does not matter. However, because the value of the reference resistor directly impacts the measurement result, choosing a reference resistor with a very low temperature coefficient is important to limit errors introduced by the temperature drift of R_{REF}.

The second IDAC2 is used to compensate for errors introduced by the voltage drop across the lead resistance of the RTD. All three leads of a 3-wire RTD typically have the same length and, thus, the same lead resistance. Also, IDAC1 and IDAC2 have the same value. Consequently, the differential voltage (V_{IN}) across the ADC inputs, AIN0 and AIN1, is as shown in Equation 10.

$$V_{IN} = V_{AIN0} - V_{AIN1} = I_{IDAC1} \times (R_{RTD} + R_{LEAD1}) - I_{IDAC2} \times R_{LEAD2} \quad (10)$$

When $R_{LEAD1} = R_{LEAD2}$ and $I_{IDAC1} = I_{IDAC2}$, Equation 10 reduces to Equation 11.

$$V_{IN} = I_{IDAC1} \times R_{RTD} \quad (11)$$

In other words, the measurement error resulting from the voltage drop across the RTD lead resistance is compensated for, as long as the lead resistance values and the IDAC values are well matched.

Implementing a 2-wire or 4-wire RTD measurement is very similar to the 3-wire RTD measurement shown in Section 4.3 except that only one IDAC is required. See Figure 34 for the ADC Code to RTD Conversion as implemented in MSP430 Firmware.

4.4 ADC Input and Reference Low Pass Filter

Using differential and common-mode low-pass filters at the input and reference paths improves the cancellation of excitation and environment noise.

NOTE: The corner frequency of the two differential filters must be well matched.

For example: For the selected ADS1220 sampling rate of 20 SPS results in a –3 dB bandwidth of 14.8 Hz. Therefore, the filter –3 dB corner frequency must be set at a decade greater than the bandwidth of the ADS1220.

$$C_{I\_DIFF} = \frac{1}{2 \times \pi \times F_{-3\,dB} \times \left(R_{I1} + R_{I2} + R_{RTD}\right)} \quad (12)$$

$$C_{R\_DIFF} = \frac{1}{2 \times \pi \times F_{-3\,dB} \times \left(R_{REF} + R_{R1} + R_{R2}\right)} \quad (13)$$

To ensure that mismatch of the common-mode filtering capacitors is not translated to a differential voltage, the common-mode capacitors (C_{I_CM1} and C_{I_CM2}) were chosen to be ten-times smaller than the differential capacitor.

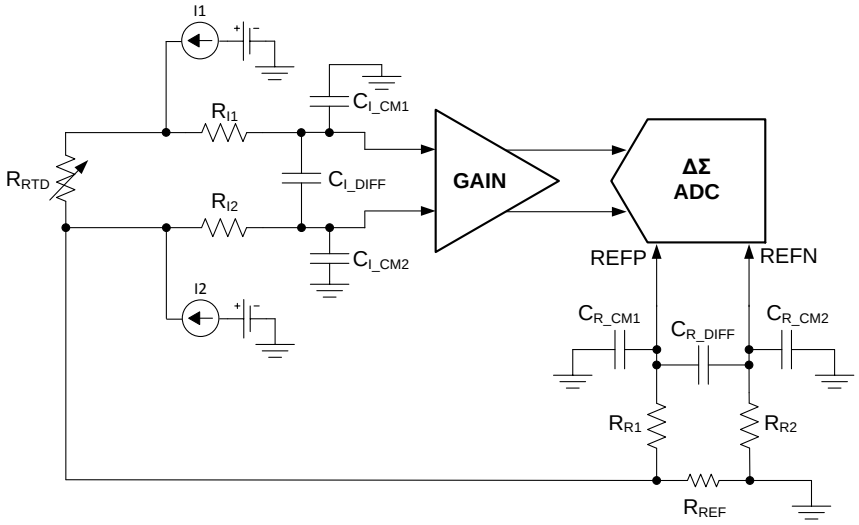


Figure 10. Input and Reference Low-Pass Filtering

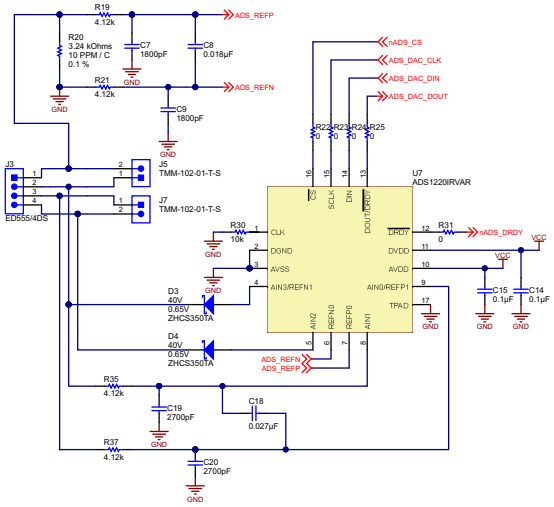


Figure 11. Low Pass Filtering on ADS1220 inputs as implemented in this Design

The cut off frequency chosen for this design is higher to account for faster sampling rate.

4.5 DAC Theory of Operation

The DAC converts the 16-bit input code in the DACCODE registers to an equivalent current output. The ΣΔ DAC output is a current pulse which is then filtered by a third-order RC lowpass filter and boosted to produce the loop current (I_{LOOP}) at the device OUT pin.

Figure 12 shows the principle of operation of the DAC161S997 in the loop-powered transmitter.

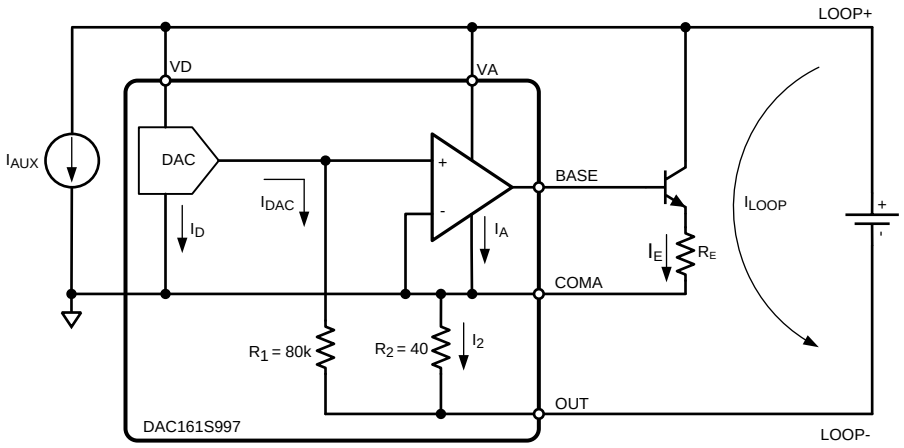


Figure 12. Loop-Powered Transmitter

In Figure 12, I_D and I_A represent supply (quiescent) currents of the internal digital and analog blocks. I_{AUX} represents supply (quiescent) current of companion devices present in the system, such as the voltage regulator and the digital interface. Because both the control loop formed by the amplifier and the bipolar transitor force the voltage across R_1 and R_2 to be equal, under normal conditions, the I_{LOOP} is dependent only on I_{DAC} through the following relationship (see Equation 14 and Figure 13).

$$I_{Loop} = (1 + R_1 / R_2)\, I_{DAC}$$

where

- $I_{DAC} = f(\text{DACCODE})$ (14)

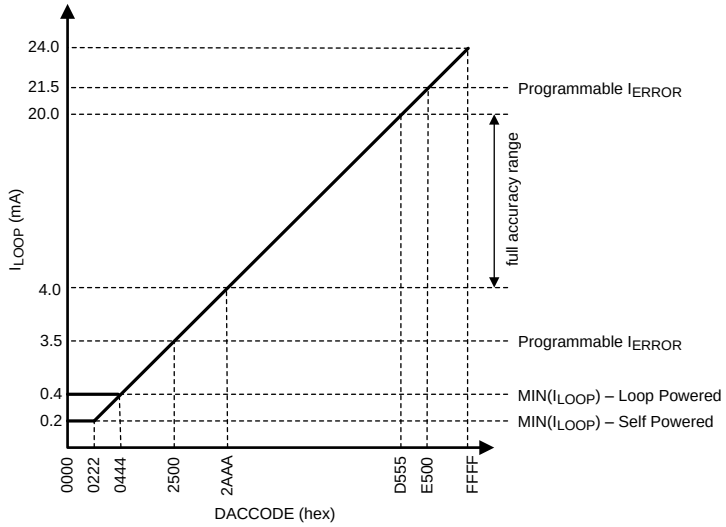


Figure 13. DAC-DC Transfer Function

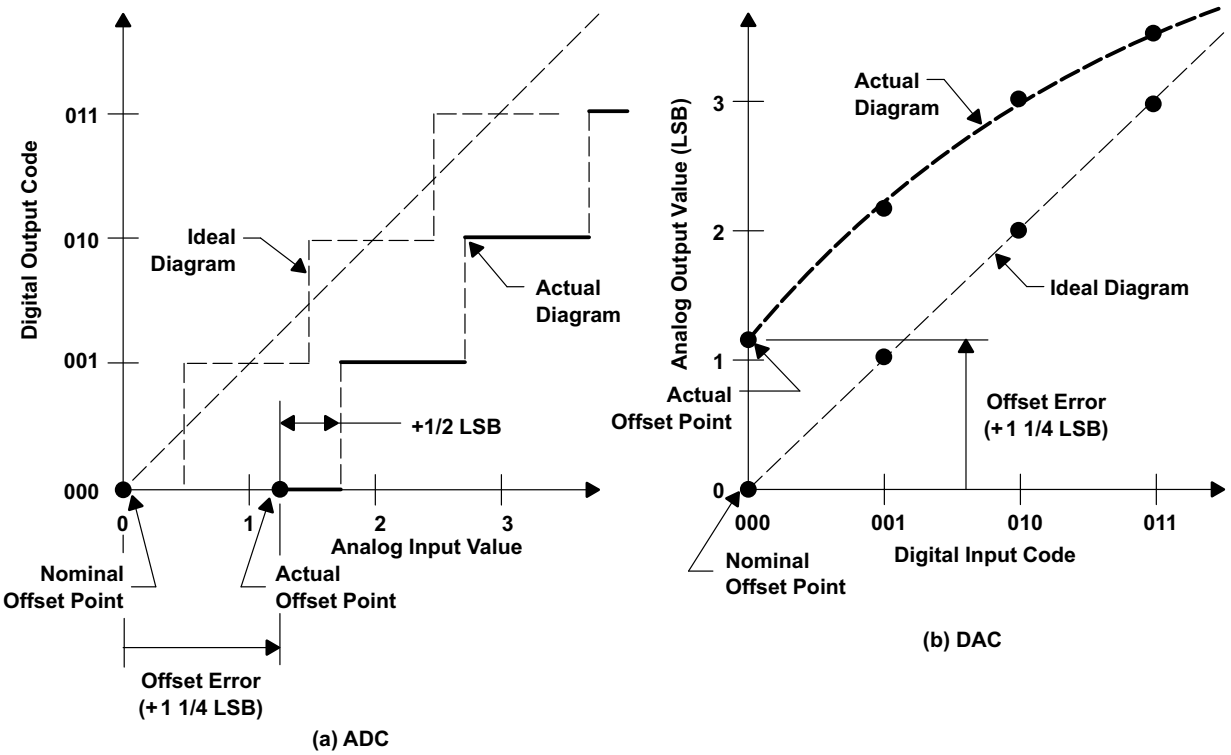
The DAC161S997 cannot directly interface to the typical 4 to 20-mA loop because of the high supply voltage. The loop interface has to provide the means of stepping down the LOOP Supply to approximately 3.3 V. The second component of the loop interface is the external NPN transistor (BJT). This device is part of the control circuit that regulates the transmitter's output current (I_{LOOP}). Since the BJT operates over the wide current range, spanning at least 4 to 20 mA, degenerating the emitter in order to stabilize transconductance (gm) of the transistor is not necessary. The degeneration resistor of 20 Ω is suggested in typical applications.

In this system, the default firmware supports temperature range from –200°C to 850°C. Thus a theoretical DAC error of 1 µA would lead to 0.065°C error in the system. See Figure 35 for temperature to current conversion as implemented in the MSP430 Firmware.

4.6 Offset Error

The offset error as shown in Figure 14 is defined as the difference between the nominal and actual offset points. For an ADC, the offset point is the midstep value when the digital output is zero, and for a DAC it is the step value when the digital input is zero. This error affects all codes by the same amount and can usually be compensated for by a trimming process. If trimming is not possible, this error is referred to as the zero-scale error.

In this design, offset error correction for ADC is shown in Figure 31. In this algorithm, the ADC input pins inside the ADS1220 device are shorted and a given number of measurements are averaged to determine an offset error correction that is applied to all functional measurements. For DAC offset error correction, see Section 6.5. The offset correction required for the DAC was not as significant as the gain correction as shown in Figure 44. The firmware does not implement a DAC offset correction. However, a simple algorithm can be implemented if offset correction is needed.



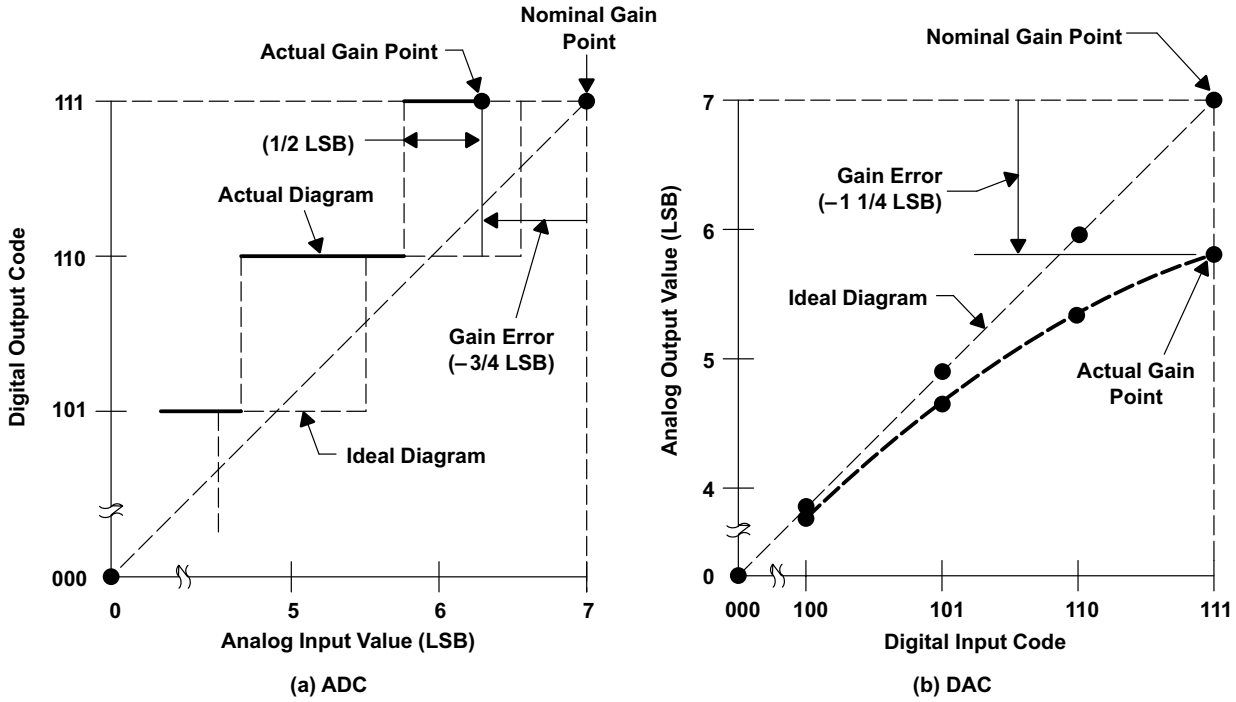
Offset error of a Linear 3-Bit Natural Binary Code Converter (Specified at Step 000)

Figure 14. Offset Error

4.7 Gain Error

The gain error shown in Figure 15 is defined as the difference between the nominal and actual gain points on the transfer function after the offset error has been corrected to zero. For an ADC, the gain point is the midstep value when the digital output is full scale, and for a DAC it is the step value when the digital input is full scale. This error represents a difference in the slope of the actual and ideal transfer functions and as such corresponds to the same percentage error in each step. This error can also usually be adjusted to zero by trimming.

In this design, gain error correction for ADC is shown in Section 6.3. For DAC gain correction, see Section 6.5. A simple 2 point calibration was implemented to overcome the gain error as shown in Section 6.5. Note that this is an example code of how to implement gain correction on the DAC. The gain correction factor is stored in Figure 30. Customers can perform the DAC gain calibration measurement on a given system by removing the *#DAC_test* and recompiling the firmware and then use SW 1 (see Figure 55) which outputs 4 to 20 mA in 2-mA steps for each button push. Using these values, a new *DACErrorCorrection* value as shown in Figure 30 can be determined. For a higher precision a gain error correction using multiple points lookup can be implemented.



Gain Error of a Linear 3-Bit Natural Binary Code Converter (Specified at Step 111), After Correction of the Offset Error

Figure 15. Gain Error

NOTE: In this reference design, the firmware implements the offset and gain calibration for ADC by default. For DAC offset and gain calibration procedures described in Section 6.5 can be used to implement such corrections.

4.8 Power Design

The input voltage range for the temperature transmitter system is approximately 8 to 35 V. For this input range, the desired output for the on board system power is approximately 3.3 V. An LDO that has a high power-supply ripple rejection is required for a high precision design. A low junction-to-ambient thermal resistance is also required to ensure that the extra unused energy from the input supply can dissipate within the package of the LDO.

The TPS7A4901 device comes from a series of high-voltage, ultra-low noise LDOs that are ideal for precision applications. A resistor divider at the LDO output sets the output voltage (V_{LDO_OUT}) proportional to the internal reference voltage of the LDO (V_{LDO_REF}). For this device, V_{LDO_REF} = 1.194 V. In order to set V_{LDO_OUT} to the desired 3.3 V, the resistor divider components are calculated in Equation 15.

$$V_{LDO\_OUT} = V_{LDO\_REF} \times \left(1 + \frac{R1}{R2}\right) \quad (15)$$

where

- R1 = 21 kΩ
- R2 = 12 kΩ

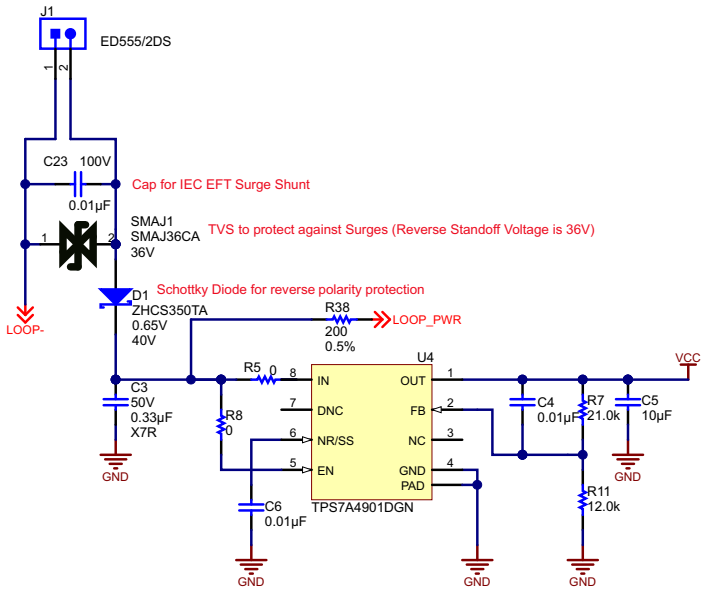


Figure 16. LDO Section

The TPS7A4901 device supports up to 36 V of input voltage and has an ultra-low noise of 15.4 μV_{RMS} and 72 dB PSRR.

Equation 16 calculates the maximum power dissipation requirements for the TPS7A4901 device.

$$(V_I - V_O) \times I_O \quad (16)$$

where

- V_I is 35 V, V_O is 3.3 V, I_O is approximately 24 mA (max)

From Equation 16 the power dissipated in the LDO package is approximately 0.76W

The junction-to-ambient thermal resistance, θ_{JA}, of the TPS7A4901 device is 55.09°C/W (see Equation 17).

$$\theta_{JA} \times \text{Power Dissipation} + T_A\text{max} < 150°C\ (T_J\text{max}) \quad (17)$$

The maximum junction temperature before the TPS7A4901 device shuts down is 150°C. From Equation 17, the worst case temperature of TPS7A4901 device is approximately 126°C assuming that ambient temperature of 85°C. Therefore, a sufficient thermal-operating margin is available with the TPS7A4901 device, even accounting for the worse case power dissipation.

4.9 Reverse Polarity Protection

To protect the system from accidently connecting the power to ground and ground to power, reverse polarity protection diodes are placed both in the path of Loop+ and Loop– as shown in Figure 17 and Figure 18.

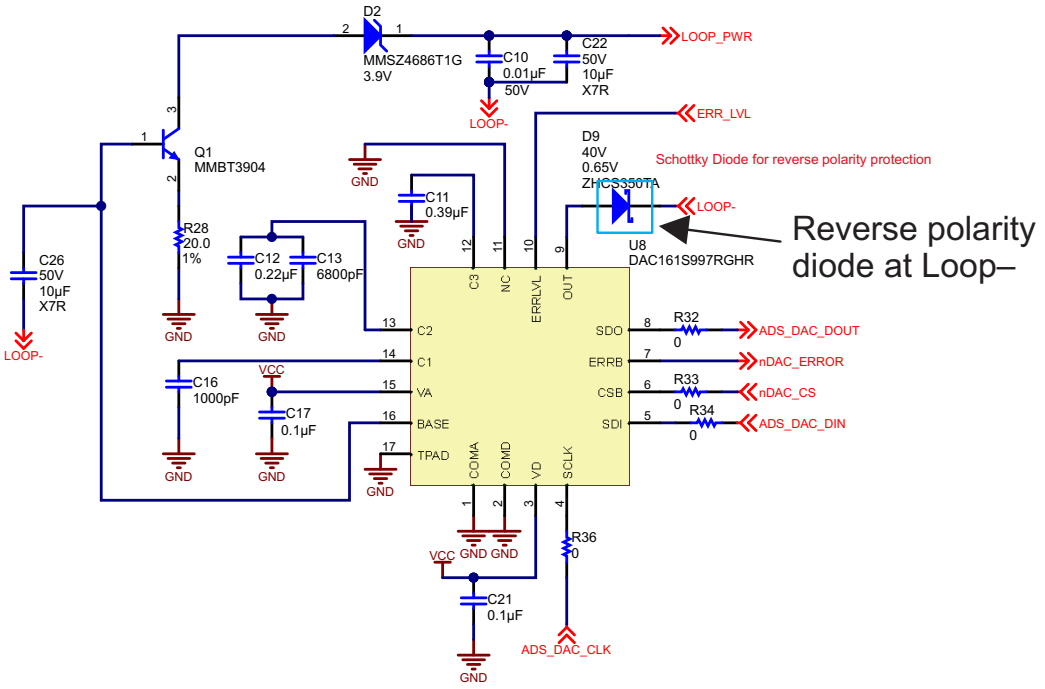


Figure 17. Reverse Polarity Diode at Loop–

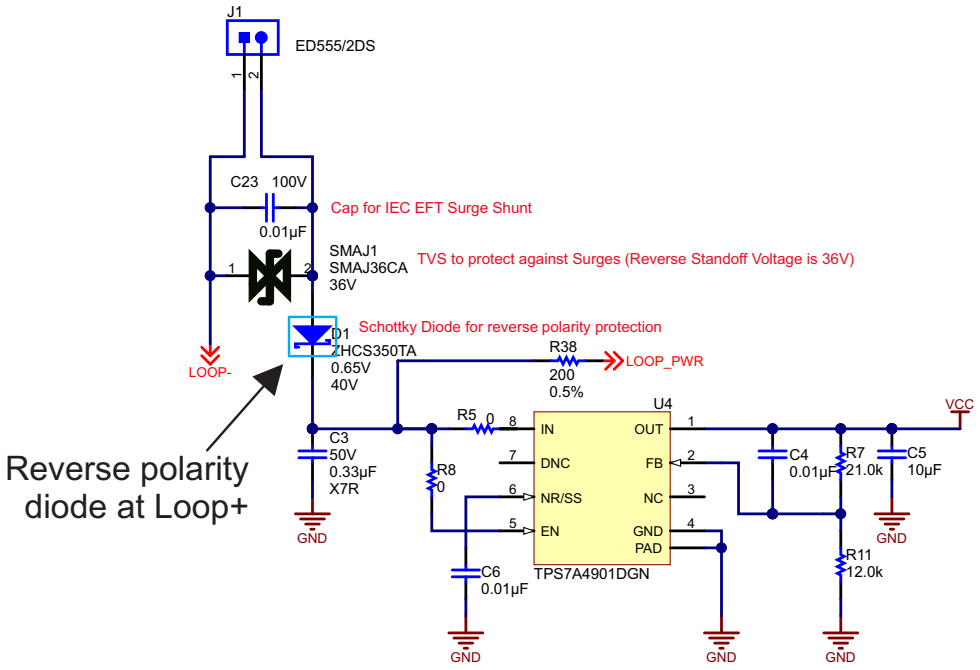


Figure 18. Reverse Polarity Diode at Loop+

4.10 Power Supply Sequencing

To ensure that the LDO can provide 3.3 V to the DAC before the loop power is applied to the DAC output, the size of the capacitors is chosen such that:

$$C3 \ll C22, C26 \quad (18)$$

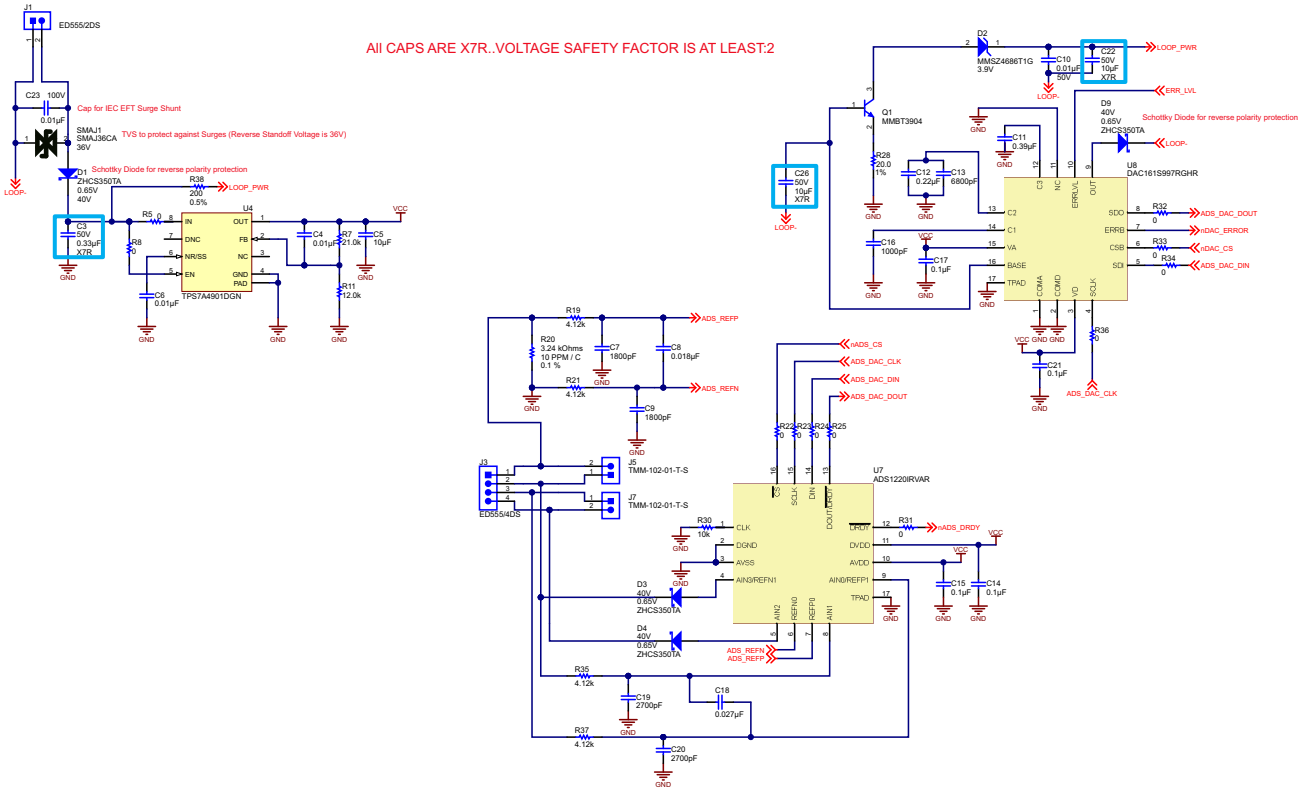


Figure 19. Power Supply Sequencing

4.11 IEC61000-4-2 and IEC61000-4-4 Protection

For IEC61000-4-2 and IEC61000-4-4 protection a TVS diode as well as a capacitor is placed as close as possible to the input power connector J1. See Figure 20 for the schematic and corresponding layout. Ensure that both the TVS and the capacitor are placed as close as possible to the input power connector (J1) as shown in Figure 20. The TVS diode is mounted on the top side near the J1 connector. The shunt capacitor is placed on the bottom side as close to the J1 connector as possible.

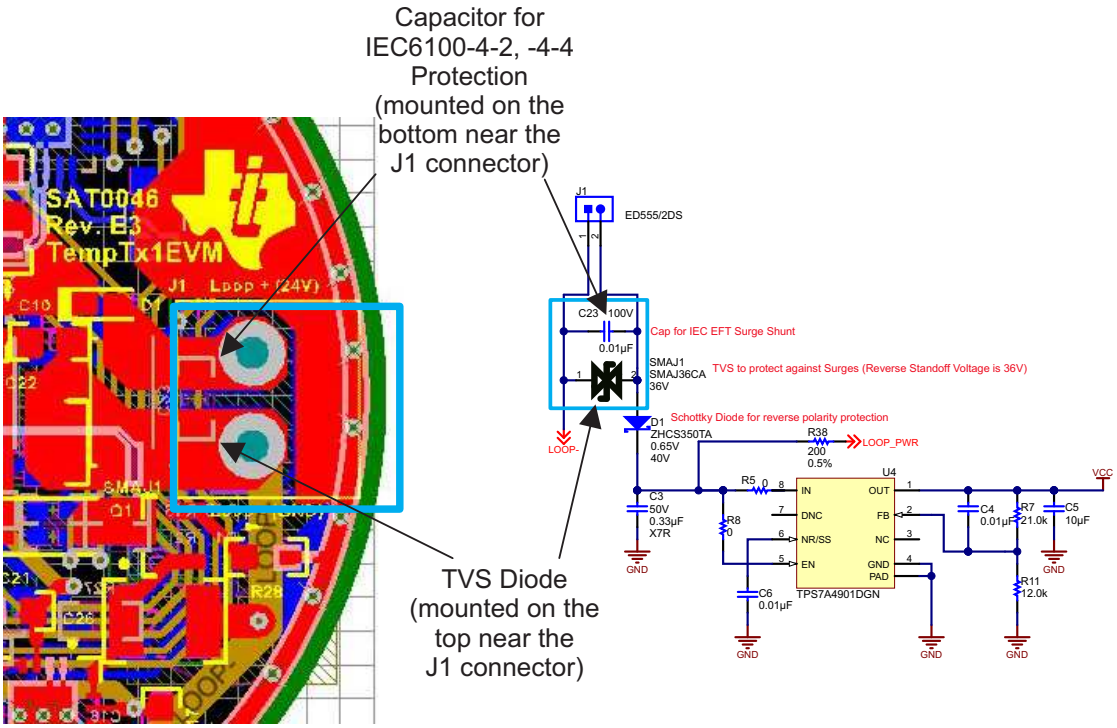


Figure 20. TVS and a Shunt Capacitor for IEC61000-4-2 and IEC61000-4-4 Protection

4.12 MSP430

The MSP430 device interfaces with ADC and DAC through SPI interface. SPI interface is shared between the ADC and DAC. The MSP430 device interfaces to a PC COM port through the UART port. A USB to UART dongle is required.

The MSP430 device records the raw ADC code from the ADS1220 device that corresponds to the temperature reading, applies offset and gain calibration, converts the ADC code to a resistance value, performs linear interpolation to overcome the non-linearity of the RTD, converts the given temperature from the lookup table to the DAC current and after correcting for DAC gain and offset correction, and applies that equivalent code corresponding to loop current to the DAC161S997 device through SPI. See Section 5.4 for details.

NOTE: In this reference design, the firmware implements the offset and gain calibration for ADC by default. For DAC offset and gain calibration procedures described in Section 6.5 can be used to implement such corrections.

4.13 Complete System Theory

- The input-voltage range of 10 to 35 V converts to 3.3 V through an LDO, the TPS7A4901 device.
- The system has protection for IEC61000-4-2 and IEC61000-4-4 for input power (loop power) as well as reverse polarity protection incorporated.
- The ADS1220 device is a 24-bit sigma delta ADC that interfaces with RTD probes and converts resistance measurement to a raw ADC code.
- The MSP430 device records the raw ADC code from ADS1220 that corresponds to the temperature reading, applies offset and gain calibration, converts the ADC code to a resistance value, performs linear interpolation to overcome the non-linearity of the RTD.
- The MSP430 device converts the given temperature from the lookup table to the DAC equivalent current code. The DAC offset and gain calibration can be applied at this step.
- The MSP430 device uses the same SPI interface to interface both to the ADS1220 device and the DAC161S997 device.

NOTE: The MSP430 device shares the same SPI between the ADS1220 device and the DAC161S997 device. External buffering is not required because both of TI's devices, the ADS1220 device and the DAC161S997 device, go hi-Z when not addressed.

NOTE: The system design requirements listed in Section 2 were met as described in Section 4.

5 Getting Started

5.1 Hardware Overview

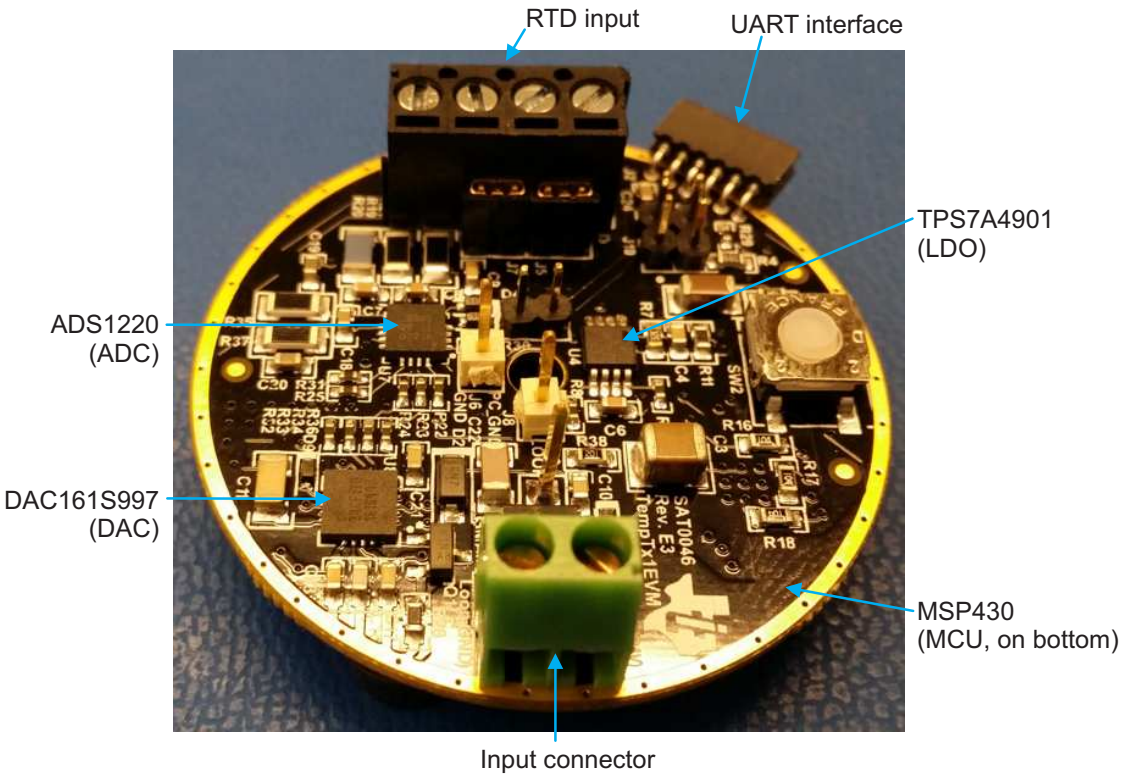


Figure 21. System Hardware Description

5.2 Getting Started Steps

1. A power supply with 20 to 24-V (typical) range can power the system as shown in Figure 22.
2. The current-limit of the power supply is set to 40 mA as recommended. 24 mA is the theoretical maximum that the system should draw from the power supply.
3. Connect a precision multimeter in series with the power supply as shown in Figure 22. A 6.5-digit precision multimeter is recommended as shown in Figure 22.

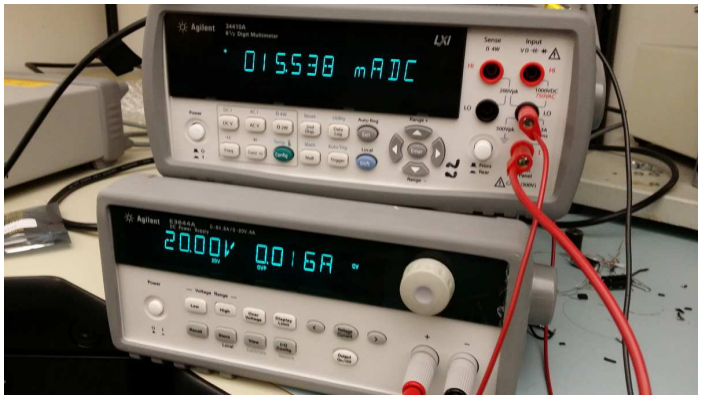


Figure 22. Power Supply and Multimeter Connected in Series

NOTE: For basic functionality testing, a 6.5-digit multimeter is sufficient. For DAC characterization, a 8.5-digit multimeter is recommended

4. If there is no firmware loaded into the MSP430 flash the default current consumed by the system is approximately 3.37 mA. This consumed current does not reflect the power consumed by the system. The consumed current reflects the error low condition as indicated by the DAC161S997 as shown in Figure 23.

	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
IERRL	LOW ERROR current	ERR_LOW = default	3.36	3.375	3.39	mA
IERRH	HIGH ERROR current	ERR_HIGH = default	21.7	21.75	21.82	mA

Figure 23. Default Current Drawn by the System When the Firmware is Not Programmed

5. Figure 24 shows the basic setup to program the system. Note that a USB to UART dongle is needed to program the system. A capacitor is connected to the input power-supply terminals primarily for ease of power supply lead connectivity. If the capacitors are polarized then reverse polarity can damage these capacitors. A precision resistor (0.01%) connected to the RTD inputs emulate a 2-wire RTD connection (jumpers J5 and J7 are installed). For programming setup Jumpers J4, J10, and J11 are installed. These jumpers ensure that the connectivity from the MSP430 programming pins is available and that the PC GND is shorted to the system ground (see Figure 55).

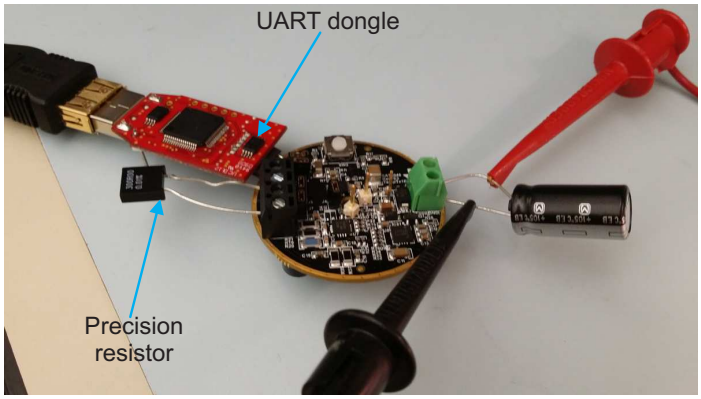


Figure 24. System Hardware Setup for MSP430 Firmware programming

6. Figure 27 shows the basic setup in functional mode. Note that the jumpers J4, J10, and J11 are not required. UART pins between the PC and the MSP430 device are isolated through ISO7421 see Figure 25, which ensures that the PC GND does not interfere with the system or the loop ground. In this setup, the connection is a 3-wire RTD and therefore J7 is installed and J5 is not installed as listed in Figure 27

NOTE: The load switch in this design can turn off the isolation section as needed by the end application (see Figure 26).

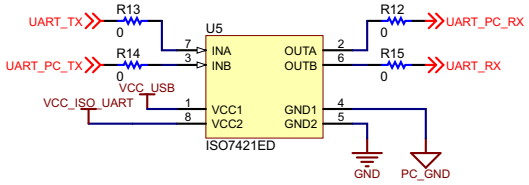


Figure 25. Digital Isolation for UART

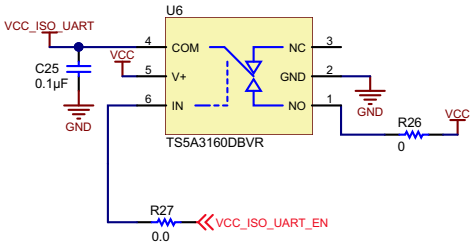


Figure 26. Load Switch to Turn Off and On Isolation

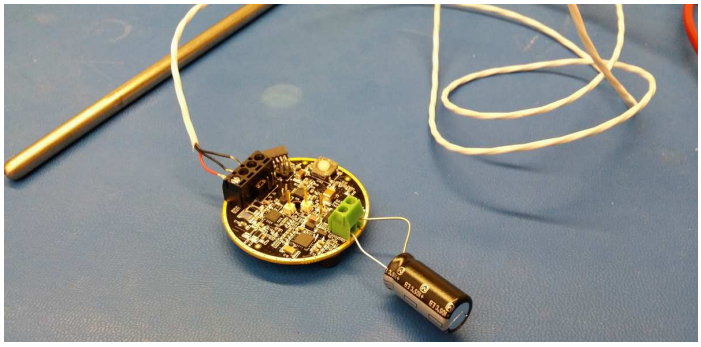


Figure 27. Basic Setup

5.3 Support for 2-Wire, 3-Wire, and 4-Wire RTD

The system supports both 2-wire, 3-wire, and 4-wire RTD. Table 2 lists the jumper configurations as shown in Figure 28.

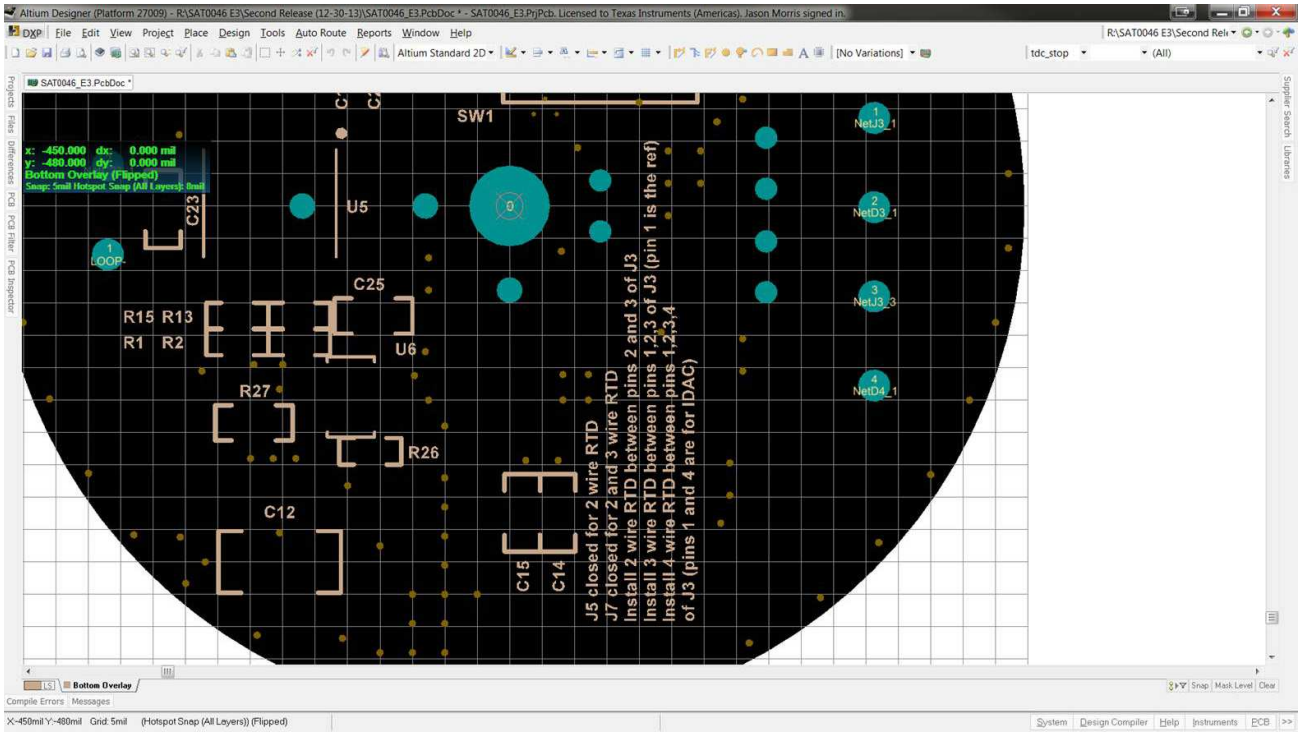


Figure 28. 2-Wire, 3-Wire, and 4-Wire RTD Support Shown on the Bottom Silkscreen

Table 2. 2-Wire, 3-Wire, and 4-Wire RTD Support

SETUP	CONNECTORS		RTD LOCATION
	INSTALLED	NOT INSTALLED	
2 wire	J5 and J7		2-wire RTD is installed between pins 2 and 3 of J3
3 wire	J7	J5	3-wire RTD is installed between pins 1, 2, and 3 of J3
4 wire		J5 and J7	4-wire RTD is installed between pins 1, 2, 3, and 4 of J3

5.4 Firmware

For MSP430 Firmware updates, code composer is recommended. Also a USB-to-UART dongle is required as shown in Figure 24. For programming setup, jumpers J4, J10, and J11 are installed. These jumpers ensure that the connectivity from the MSP430 programming pins is available as well as the PC GND is shorted to the system ground (see Figure 55).

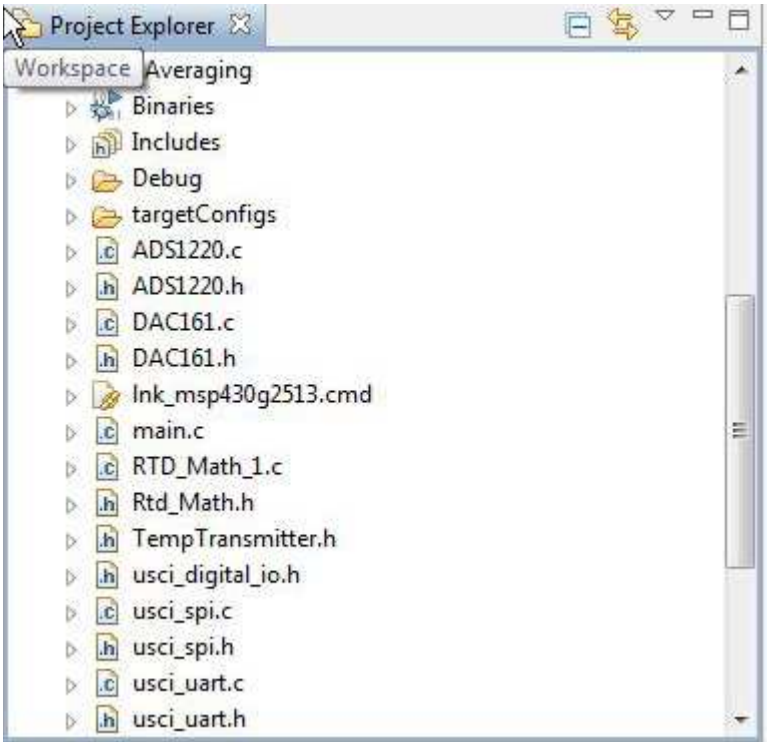


Figure 29. Firmware Project Files

```
47 float Rref = 3240.0;
48
49 // Setting the DacErrorCorrection to 1.0 and turning on the DAC_TEST will allow the user to measure the
50 //  output of the DAC161 at 2mA intervals to determine the DacErrorCorrection for there specific device.
51 //#define DAC_TEST 1
52 float DacErrorCorrection = 0.99945;
53
54 // If the following #define is enabled, the system will perform Gain Calibration when the user pushes
55 // the button on the top of the device. The user MUST have modified the code to place the expected
56 // results into the MeasuredGainCodeValue. The user is expected to place a known resistor value in
57 // place of the RTD and push the top button to determine the system level gain correction.
58 // This correction value will be stored into flash memory for future use.
59 //
60 // To prevent the user from accidentally modifying the Gain Correction setting, this #define is left
61 // commented out for normal operations
62 //#define GAIN_CAL
63
64 // To calculate expected result, take the expected answer from the precision multimeter reading and
65 //   Code = RTDmeas * PgaGainLevel * (2^23 - 1) / (Rref * 2)
66 float MeasuredGainCodeValue = 7868944.1883;
67
68
```

Figure 30. Key Variables

The key variables, such as R_{REF}, the reference resistor for the ADC, the DAC gain-calibration factor, or the ADC gain factor are brought out as variables (see Section 4.7, Section 6.3, and Section 6.5).

ADS1220.c

```
/*****************************************************************************************************************************************************
*  ADS1220_Offset_Calibrate_Data
*****************************************************************************************************************************************************/
/*!
* @brief Performs a calibration step from data collected by the ADS1220.
*
* In order to perform a calibration, the ADS1220 AIN lines are shorted together (using the Setup_ADS1220() function). A number of conversion are
* then performed and the conversion data is sent to this function.
*
* This function will take the conversion data and average the results which will be used in the ADS1220_Get_Conversion_Data_Calibrated() function
* to return a calibrated conversion result.
*
* @param[in]    *tempData        Pointer to raw conversion data that will be included in calibration calculations.
*
* @return  None
*
* @sa Setup_ADS1220()
* @sa ADS1220_Get_Conversion_Data_Calibrated()
*****************************************************************************************************************************************************/
void ADS1220_Offset_Calibrate_Data (unsigned char *tempData)
{
    long temp;

    temp = tempData[0];
    temp <<= 8;
    temp |= tempData[1];
    temp <<= 8;
    temp |= tempData[2];

    // Was temp negative?
    if (tempData[0] & 0x80)
        temp |= ((long)0xff << 24);              // Sign extend

    OffsetCalibrateData += temp;
    OffsetCalibrateCount++;
    OffsetCalibrateValue = OffsetCalibrateData / OffsetCalibrateCount;

}
```

Figure 31. ADC-Offset Calibration Routine

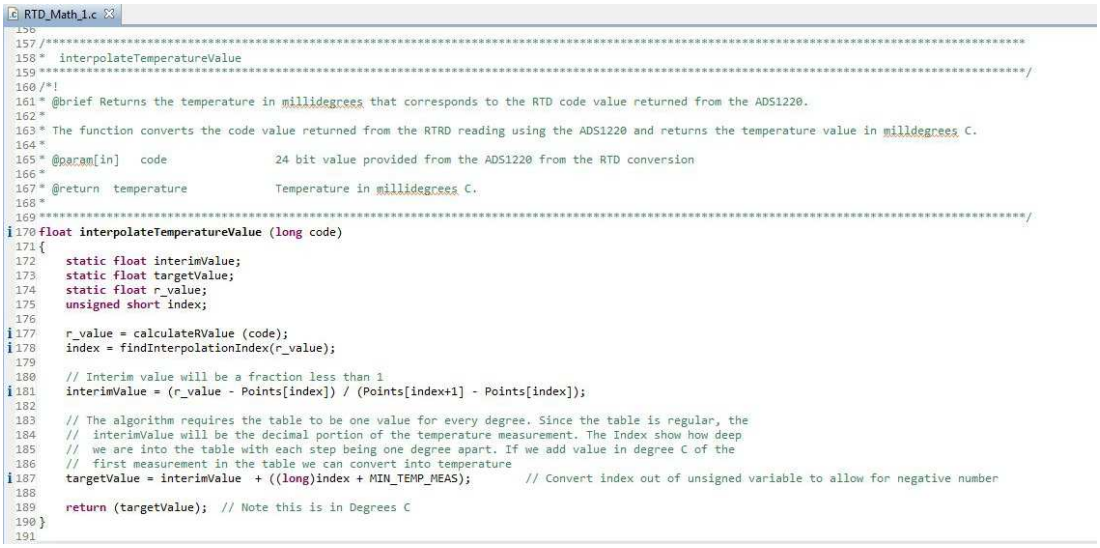
Section 4.6 shows the ADC-offset calibration as implemented in this firmware.

RTD_Math_1.c

```
// This particular table has measurements at every degree C from -200 to 851 inclusive (1052 points).
// It is used to perform a linear interpolation between two points that surround the measurement. In this case, those points are 1 degree apart.
//
// Other tables can be used with more or less points, at the impact of changing the accuracy of the measurement. These is no requirement for the measurements to be evenly
// spaced. The table can have fewer points at areas that are nearly linear, and more points at areas that are less linear with no change required to the algorithm.
//
//
const float Points[] =
{
        18.520, 18.952, 19.384, 19.815, 20.247, 20.677, 21.108, 21.538, 21.967, 22.397,
        22.825, 23.254, 23.682, 24.110, 24.538, 24.965, 25.392, 25.819, 26.245, 26.671,
        27.096, 27.522, 27.947, 28.371, 28.796, 29.220, 29.643, 30.067, 30.490, 30.913,
        31.335, 31.757, 32.179, 32.601, 33.022, 33.443, 33.864, 34.284, 34.704, 35.124,
        35.543, 35.963, 36.382, 36.800, 37.219, 37.637, 38.055, 38.472, 38.889, 39.306,
        39.723, 40.140, 40.556, 40.972, 41.388, 41.803, 42.218, 42.633, 43.048, 43.462,
        43.876, 44.290, 44.704, 45.117, 45.531, 45.944, 46.356, 46.769, 47.181, 47.593,
        48.005, 48.416, 48.828, 49.239, 49.649, 50.060, 50.470, 50.881, 51.291, 51.700,
        52.110, 52.519, 52.928, 53.337, 53.746, 54.154, 54.562, 54.970, 55.378, 55.786,
        56.193, 56.600, 57.007, 57.414, 57.821, 58.227, 58.633, 59.039, 59.445, 59.850,
        60.256, 60.661, 61.066, 61.471, 61.876, 62.280, 62.684, 63.088, 63.492, 63.896,
        64.300, 64.703, 65.106, 65.509, 65.912, 66.315, 66.717, 67.120, 67.522, 67.924,
        68.325, 68.727, 69.129, 69.530, 69.931, 70.332, 70.733, 71.134, 71.534, 71.934,
        72.335, 72.735, 73.134, 73.534, 73.934, 74.333, 74.732, 75.131, 75.530, 75.929,
        76.328, 76.726, 77.125, 77.523, 77.921, 78.319, 78.717, 79.114, 79.512, 79.909,
        80.306, 80.703, 81.100, 81.497, 81.894, 82.290, 82.687, 83.083, 83.479, 83.875,
        84.271, 84.666, 85.062, 85.457, 85.853, 86.248, 86.643, 87.038, 87.432, 87.827,
        88.222, 88.616, 89.010, 89.404, 89.798, 90.192, 90.586, 90.980, 91.373, 91.767,
        92.160, 92.553, 92.946, 93.339, 93.732, 94.124, 94.517, 94.909, 95.302, 95.694,
        96.086, 96.478, 96.870, 97.261, 97.653, 98.044, 98.436, 98.827, 99.218, 99.609,
        100.000, 100.391, 100.781, 101.172, 101.562, 101.953, 102.343, 102.733, 103.123, 103.513,
        103.903, 104.292, 104.682, 105.071, 105.460, 105.849, 106.238, 106.627, 107.016, 107.405,
        107.794, 108.182, 108.570, 108.959, 109.347, 109.735, 110.123, 110.510, 110.898, 111.286,
        111.673, 112.060, 112.447, 112.835, 113.221, 113.608, 113.995, 114.382, 114.768, 115.155,
        115.541, 115.927, 116.313, 116.699, 117.085, 117.470, 117.856, 118.241, 118.627, 119.012,
        119.397, 119.782, 120.167, 120.552, 120.936, 121.321, 121.705, 122.090, 122.474, 122.858,
        123.242, 123.626, 124.009, 124.393, 124.777, 125.160, 125.543, 125.926, 126.309, 126.692,
        127.075, 127.458, 127.840, 128.223, 128.605, 128.987, 129.370, 129.752, 130.133, 130.515,
        130.897, 131.278, 131.660, 132.041, 132.422, 132.803, 133.184, 133.565, 133.946, 134.326,
        134.707, 135.087, 135.468, 135.848, 136.228, 136.608, 136.987, 137.367, 137.747, 138.126,
        138.506, 138.885, 139.264, 139.643, 140.022, 140.400, 140.779, 141.158, 141.536, 141.914,
        142.293, 142.671, 143.049, 143.426, 143.804, 144.182, 144.559, 144.937, 145.314, 145.691,
        146.068, 146.445, 146.822, 147.198, 147.575, 147.951, 148.328, 148.704, 149.080, 149.456,
        149.832, 150.208, 150.583, 150.959, 151.334, 151.710, 152.085, 152.460, 152.835, 153.210,
        153.584, 153.959, 154.333, 154.708, 155.082, 155.456, 155.830, 156.204, 156.578, 156.952,
        157.325, 157.699, 158.072, 158.445, 158.818, 159.191, 159.564, 159.937, 160.309, 160.682,
        161.054, 161.427, 161.799, 162.171, 162.543, 162.915, 163.286, 163.658, 164.030, 164.401,
        164.772, 165.143, 165.514, 165.885, 166.256, 166.627, 166.997, 167.368, 167.738, 168.108,
```

Figure 32. Lookup Table for Linear Interpolation

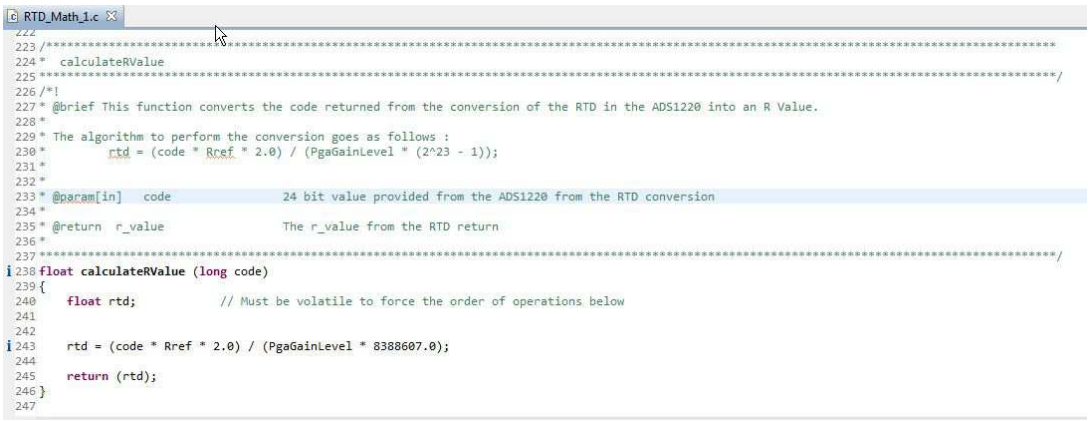
This lookup table is stored in the MSP430 Firmware for the linear interpolation to address the non-linearity of the RTD as shown in the Section 4.2.



```
RTD_Math_1.c
/*****************************************************************************************************************************************************
*  interpolateTemperatureValue
*****************************************************************************************************************************************************/
/*!
* @brief Returns the temperature in millidegrees that corresponds to the RTD code value returned from the ADS1220.
*
* The function converts the code value returned from the RTRD reading using the ADS1220 and returns the temperature value in milldegrees C.
*
* @param[in]   code                24 bit value provided from the ADS1220 from the RTD conversion
*
* @return  temperature             Temperature in millidegrees C.
*
*****************************************************************************************************************************************************/
float interpolateTemperatureValue (long code)
{
    static float interimValue;
    static float targetValue;
    static float r_value;
    unsigned short index;

    r_value = calculateRValue (code);
    index = findInterpolationIndex(r_value);

    // Interim value will be a fraction less than 1
    interimValue = (r_value - Points[index]) / (Points[index+1] - Points[index]);

    // The algorithm requires the table to be one value for every degree. Since the table is regular, the
    //  interimValue will be the decimal portion of the temperature measurement. The Index show how deep
    //  we are into the table with each step being one degree apart. If we add value in degree C of the
    //  first measurement in the table we can convert into temperature
    targetValue = interimValue  + ((long)index + MIN_TEMP_MEAS);        // Convert index out of unsigned variable to allow for negative number

    return (targetValue);  // Note this is in Degrees C
}
```

Figure 33. Algorithm for Linear Interpolation

The algorithm for the linear interpolation addresses the non-linearity of the RTD as shown in Section 4.2.



```
RTD_Math_1.c
/*****************************************************************************************************************************************************
*  calculateRValue
*****************************************************************************************************************************************************/
/*!
* @brief This function converts the code returned from the conversion of the RTD in the ADS1220 into an R Value.
*
* The algorithm to perform the conversion goes as follows :
*         rtd = (code * Rref * 2.0) / (PgaGainLevel * (2^23 - 1));
*
*
* @param[in]   code                24 bit value provided from the ADS1220 from the RTD conversion
*
* @return  r_value                 The r_value from the RTD return
*
*****************************************************************************************************************************************************/
float calculateRValue (long code)
{
    float rtd;            // Must be volatile to force the order of operations below


    rtd = (code * Rref * 2.0) / (PgaGainLevel * 8388607.0);

    return (rtd);
}
```

Figure 34. Convert ADC Code to Resistance

The code in Figure 34 converts the ADC code, after offset and gain calibration, to resistance.

main.c

```
137
138 /*****************************************************************************************************************************************************
139 *  ConvertTemp2uAmps
140 *****************************************************************************************************************************************************/
141 /*!
142 * @brief Converts a temperature in the range of -200 to +850 degrees C into a 4-20mAmp value.
143 *
144 * This function is called to convert the temperature (scaled into degrees C * 1000) into an Amp setting to send on the 4-20mA line.
145 * -200 degrees will correspond to 4.000 mA. +850 degrees C will correspond to 20mA.
146 *
147 * @param[in]      temperature in degrees C * 1000; from -200000 to +850000
148 *
149 * @return  uAmp value       Input temperature converted in MicroAmps (mA * 1000).
150 *****************************************************************************************************************************************************/
151 unsigned long ConvertTemp2uAmps (long temperature)
152 {
153     float uAmps;
154
155     // Here is where we need to convert the 3 bytes received from the ADS1220 into a uAmp value that will be placed into the DAC
156     // -200 to +850 C measured in 1000 * C is  -200000 to 850000 or a range of 1050000 1000*C.
157     // Add 200000 to the temperature to convert it into a range between 0 and 1050000. Divide by 1050000 to get the percentage of the temperature scale.
158     //
159     // 4 to 20mA output is measured in uAmps and therefore is 4000 to 20000 uAms or a range of 16000 uAmps.
160     // Multiply the results above by 16000 to get the percentage on the uAmp scale that ranges from 0 - 16000.
161     // Adjust the results so that -200 degrees C (which comes out to 0 uAmps) is represented by 4000 uAmps by adding 4000
162     //
163     // uAmps = ((temperature + 200000) * 16000 / 1050000) + 4000  --  Divide top and bottom by 1000 and we get
164     //         ((temperature + 200000) * 16 / 1050) + 4000
165     //
166     uAmps = (((temperature + 200000) * 16.0) / 1050.0) + 4000.0;
167     uAmps = uAmps * DacErrorCorrection;
168     return ((unsigned long)uAmps);
169 }
170
```

Figure 35. Convert Temperature to DAC current

The code in Figure 35 converts the temperature to DAC current.

6 Test Data

NOTE: The test data in the following sections was measured with the system at room temperature unless otherwise noted.

NOTE: All of the measurements in this section were measured with calibrated lab equipment.

6.1 Overview

As the overall system performance is governed by the ADC accuracy, DAC accuracy, and resolution. Section 6.2 characterizes the ADC for both resolution and error (adjusted for offset and gain calibration). The DAC is then characterized for both resolution and error (adjusted for offset and gain calibration). Finally, a full-system characterization is performed for maximum measured error of the complete system.

6.2 ADC Input Referred Noise

Approximately 1000 raw ADC values are captured by the MSP430 device. To capture these values, the MSP430 device communicates to a COM Port through the USB to UART dongle as shown in Figure 36 (see step 5 in the Getting Started Steps section for more information). A precision resistor of 300 Ω is connected to the RTD as shown in Figure 36.

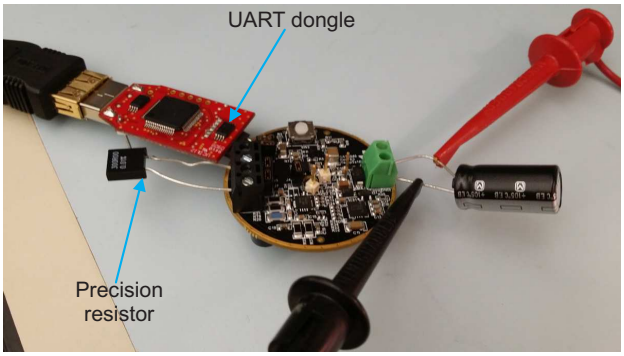


Figure 36. Input Referred Noise Measurement Setup

Figure 37 shows the plotted raw ADC values without any offset calibration or gain calibration.

The standard deviation is **approximately 43 codes** and the spread of the codes, MAX(code) to MIN(code), is **approximately 239**.

$$\text{LSB weight} = \left[\frac{\frac{V_{REF} \times 2}{\text{PGA Gain}}}{2^{24} - 1} \right] \quad (19)$$

here

- V_{REF} = 1.62 V
- PGA gain = 16, note that the sample rate is 20 SPS

$$\text{Input Referred Noise (pp)} = \left[\text{spread of RAW ADC codes} \times \text{LSB}\right] = 239 \times 12.06\ \text{nV} = 2.8\ \mu\text{V},\ 0.029°\text{C} \quad (20)$$

$$\frac{\text{ppNoise}}{(\text{PT-100\_Sensitivity} \times \text{IDAC})} = \frac{2.8\ \mu\text{Vpp}}{(0.385\ \Omega/°\text{C} \times 250\ \mu\text{A})} = 0.029°\text{C} \quad (21)$$

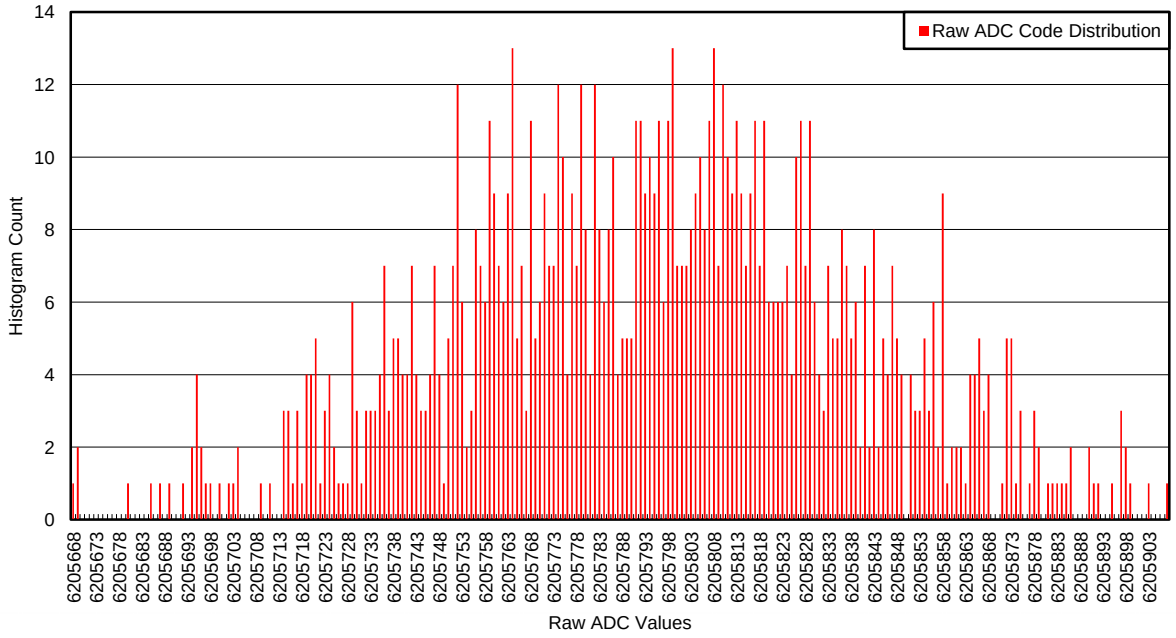


Figure 37. Raw ADC Code Distribution

6.3 ADS1220 Error Characterization Including Offset and Gain Calibration

As shown in Figure 38, the following equipment was used in this test setup.

- A power supply provides 24 V (current-limit set to 40 mA).
- A precision 6.5-digit multimeter in series to the power supply measures loop current.
- Another 8.5 digit precision multimeter precisely measures the precision resistors used in this test.
- For this test, precision resistors with a 0.01% tolerance were used to emulate the RTD probes (see Figure 39).

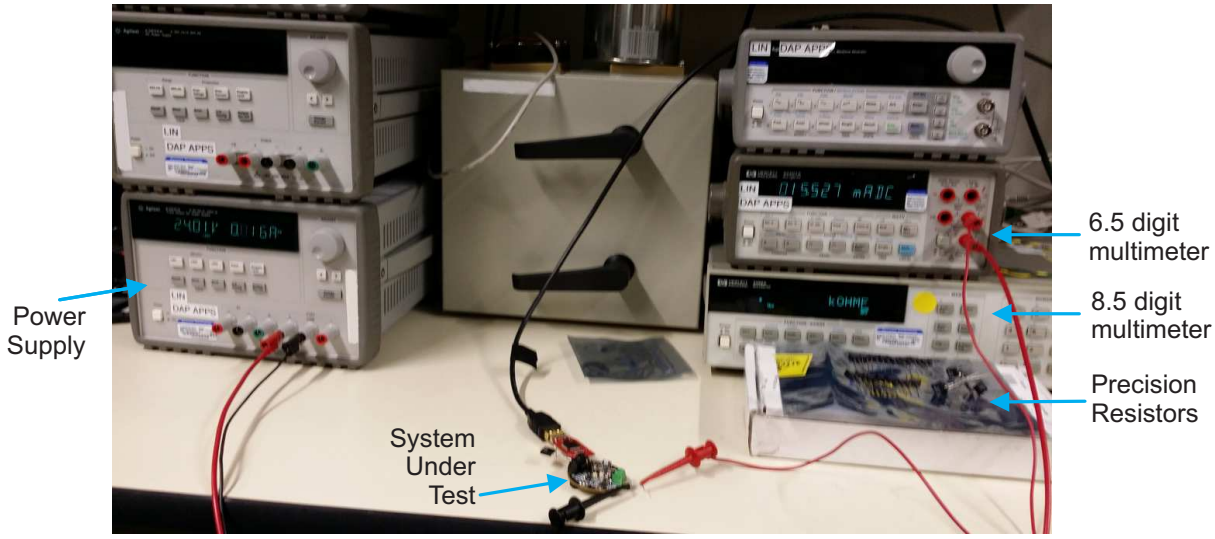


Figure 38. Setup for ADC Characterization

Figure 39. Precision Resistors 0.01% Tolerance Used for ADC Characterization

- In the typical data collection for this test, a precision resistor (for example 20 Ω) is connected to RTD inputs 1 and 3 of the J3 connector with jumpers J5 and J7 shorted (see Figure 38).
- The MSP430 device collects the RAW ADC value, applies offset calibration (one time) see Section 4.6, and collects the ADC value including the offset calibration. These values are sent to to a communication (COM) port on the PC through the USB to UART dongle.
- Once the data is measured, the precision resistor is immediately measured with the 8.5-digit precision multimeter (see Figure 40).

NOTE: To ensure that the resistance measurement is not altered by human contact, tongs were used to remove the precision resistor from the J3 connector and immediately connect to the Kelvin probes of the 8.5-digit multimeter.

- Gain calibration occurs (see Section 4.7) by connecting a 380-Ω resistor (correspond to approximately 814°C) to the RTD inputs, pin 1 and pin 3. The measured ADC value after offset correction is compared with the ideal expected ADC value based on the 8.5-digit multimeter measurement of the 380-Ω resistor. Finally, this gain calibration factor is applied to all the resistor measurements across the temperature range (see Table 4).

NOTE: **Gain Calibration for ADC** The MSP430 Firmware algorithm averages a given number of measurements with offset correction applied to an expected result with a 380-Ω resistor connected to determine the gain calibration factor.

To execute the algorithm, SW2 (see Figure 55) must be pressed with a 380-Ω resistor in place.

If there is no previously stored gain calibration factor, a new one will be determined and stored in flash.

To overwrite an existing gain calibration factor value, the first 4 bytes of *InfoC* memory in the MSP430 must be set to 0xFF.

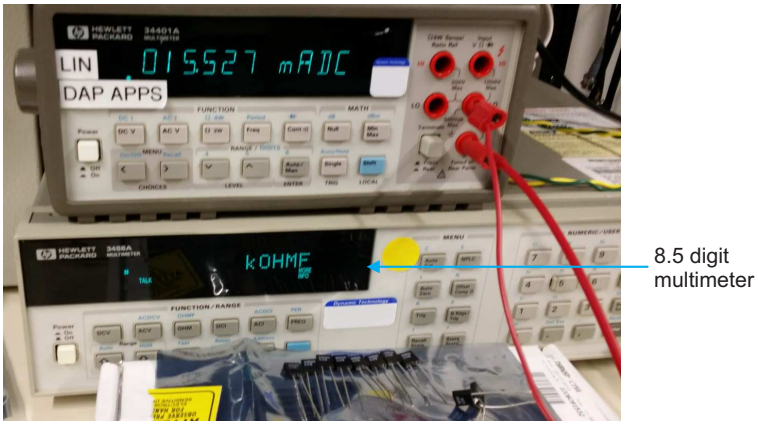


Figure 40. Precision Resistors and an 8.5-digit Multimeter

Table 3. Precision Resistors Corresponding Temperature Values

Precision Resistor Value as Measured by 8.5-digit Multimeter (Ω)	Reference Temperature Based on Measured Precision Resistor, Calculated With Callendar-Van Dusen Equations (see Section 4.2)
20.0007	–196.570346
40.0014	–149.332074
59.9921	–100.650615
79.9980	–50.776173
100.0024	0.00614
119.9960	51.555661
139.9950	103.92953
159.9918	157.147496
180.0046	211.301704
200.0006	266.349859
219.9999	322.397013
239.9789	379.431081
259.9875	437.656
280.0035	497.077256
300.0007	557.690044
329.9275	650.910269
359.9782	747.831551
379.9108	814.135104

Table 4. Raw ADC Code, ADC Code After Gain and Offset Calibration

Raw ADC Code (DEC)	ADC Code After Offset Calibration (DEC)	ADC Code After Offset and Gain Calibration (DEC)
413631	413758	414150
827425	827552	828336
1241010	1241137	1242314
1654817	1654944	1656513
2068676	2068803	2070765
2482330	2482457	2484811
2896130	2896257	2899003
3309865	3309992	3313131
3723824	3723951	3727482
4137619	4137746	4141670
4551351	4551478	4555794
4964771	4964898	4969606
5378777	5378904	5384005
5792921	5793048	5798542
6206693	6206820	6212706
6826873	6827000	6833474
7447941	7448068	7455131
7861347	7861474	7868929

Table 5. ADC Error After Gain and Offset Calibration

RTD calculation Based on ADC Code After Gain and Offset Calibration (Ω) (see Figure 34)	Temperature Reading running Linearization After Offset & Gain Calibration (°C) (see Figure 32 and Figure 33)	Reference Temperature Based on Measured Precision Resistor, Calculated with Callendar-Van Dusen Equations (see Section 4.2)	Measured Error of the ADC
19.99506593	–196.5848571	–196.570346	**0.01451**
39.99186993	–149.3556911	–149.332074	**0.02362**
59.97863173	–100.684719	–100.650615	**0.03410**
79.97606337	–50.82998014	–50.776173	**0.05381**
99.97605383	–0.06062601	0.00614	**0.06677**
119.9660987	51.47993397	51.555661	**0.07573**
139.9631923	103.8452168	103.92953	**0.08431**
159.9571961	157.0532523	157.147496	**0.09424**
179.9619663	211.1874151	211.301704	**0.11429**
199.9588668	266.2337681	266.349859	**0.11609**
219.9526775	322.2618586	322.397013	**0.13515**
239.9314248	379.2930855	379.431081	**0.13800**
259.9385124	437.5102093	437.656	**0.14579**
279.9522626	496.9460531	497.077256	**0.13120**
299.9480045	557.5494406	557.690044	**0.14060**
329.9185395	650.9059074	650.910269	**0.00436**
359.9319953	747.7075864	747.831551	**0.12396**
379.9100667	814.1344287	814.135104	**0.00068**

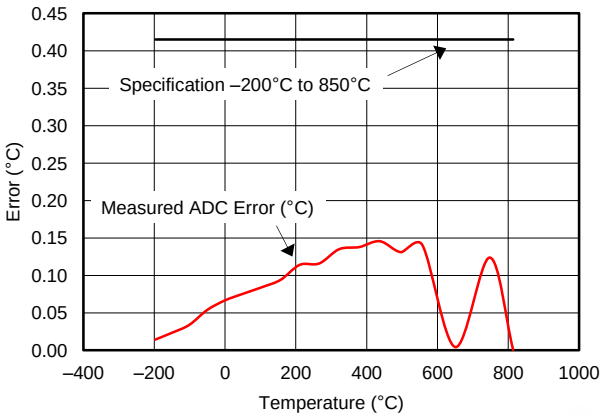


Figure 41. Measured ADC Error

NOTE: The measured ADC error is after gain and offset calibration. The measured ADC error includes the error associated with the linear interpolation of the lookup table that is used to overcome the non-linearity of RTD (see Section 4.2).

6.4 Output Resolution

For this test, the DAC output was programmed for 4 mA and multiple values were recorded over time using an 8.5-digit multimeter as shown in Figure 42. The minimum and maximum currents recorded were 3.99754 and 3.99779 mA (respectively) and thus the output resolution was 0.25 µA.

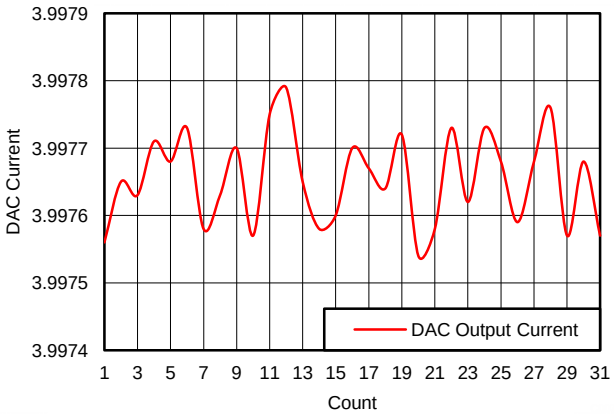


Figure 42. Output Resolution

6.5 DAC Characterization

In this setup, an 8.5-digit multimeter was used as shown in Figure 43. The MSP430 was programmed at fixed 4, 6, 8, 10, 12, 14, 16, 18, and 20 mA to the DAC and the corresponding loop current was measured using an 8.5-digit multimeter.

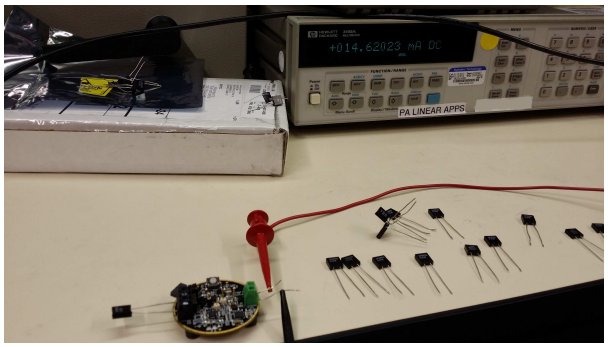


Figure 43. DAC Characterization Setup

Table 6. DAC Current With and Without Gain Calibration

DAC Value Applied (mA)	Loop Current Measured (mA)	
	Before Gain Calibration	After Gain Calibration
4	4.00126	3.99901
6	6.00200	5.99873
8	8.00285	7.99875
10	10.00372	9.99857
12	12.00464	11.99832
14	14.00577	13.99823
16	16.00685	15.99861
18	18.00798	17.99862
20	20.00948	19.99901

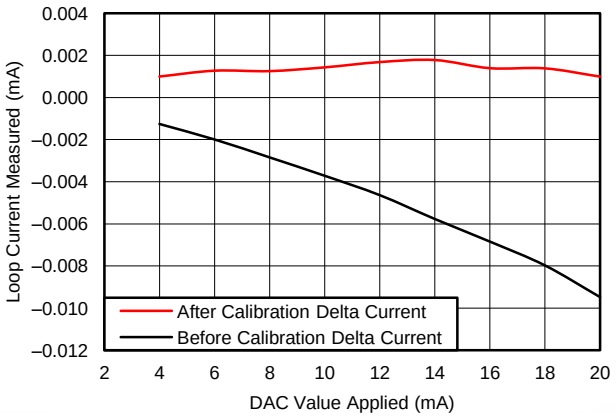


Figure 44. DAC Gain and Offset Calibration

As shown in Figure 44, without gain calibration an error is seen in the loop current. This error increases linearly with loop current. A simple gain calibration (see Section 4.7) implemented in the MSP430 fixes this error as shown in Figure 44. to increase DAC accuracy, the MSP430 MCU can also further reduce the remaining error which is offset in nature.

For reference, the distribution of the precision resistor connected to RTD input terminals versus the corresponding ideal loop current forced by the DAC is listed in Table 7.

Table 7. Ideal DAC Loop Current Versus Temperature Range

Reference Temperature Based on Measured Precision Resistor	Ideal DAC Value based on precision resistor (mA)
–196.570346	4.05226
–149.332074	4.77208
–100.650615	5.51390
–50.776173	6.27389
0.00614	7.04771
51.555661	7.83323
103.92953	8.63131
157.147496	9.44225
211.301704	10.26745
266.349859	11.10628
322.397013	11.96034
379.431081	12.82943
437.656	13.71666
497.077256	14.62213
557.690044	15.54575
650.910269	16.96625
747.831551	18.44315
814.135104	19.45349

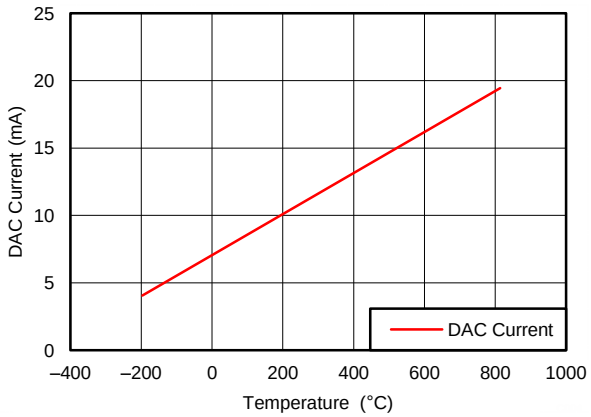


Figure 45. Ideal DAC Loop Current vs Temperature Range

6.6 Complete System Maximum Measured Error

After correcting the ADC and the DAC for gain and offset calibration, a complete system characterization was performed for maximum measured error (see Figure 46). In this setup, a power supply and 8.5-digit multimeter was used for loop current measurement. As shown in Figure 45, multiple precision resistor values covering –200°C to 850°C similar to those used in Figure 39.

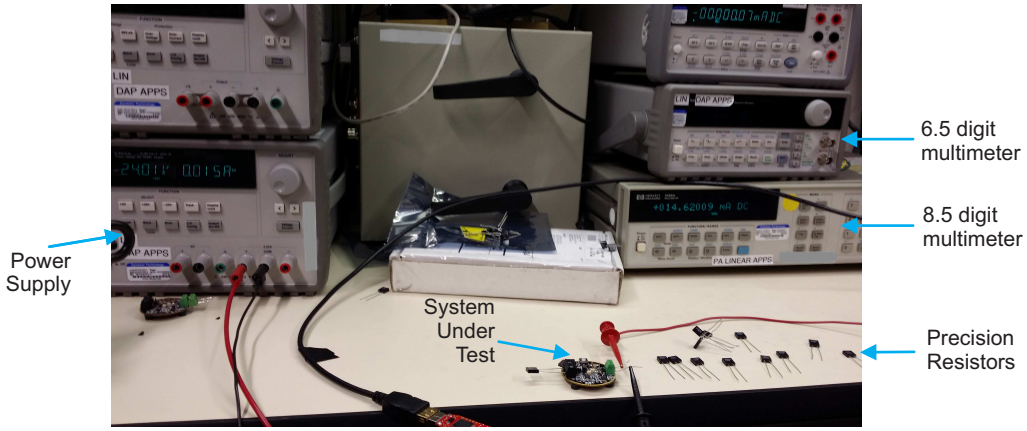


Figure 46. Complete System Characterization Setup

Table 8. Maximum Measured Error of the System

Reference Temperature Based on Measured Precision Resistor	Ideal DAC Value based on precision resistor (mA)	Measured Loop Current Value of the System (mA)
–196.570346	4.05226	4.05162
–149.332074	4.77208	4.7715
–100.650615	5.51390	5.51305
–50.776173	6.27389	6.27267
0.00614	7.04771	7.04624
51.555661	7.83323	7.83152
103.92953	8.63131	8.63004
157.147496	9.44225	9.44087
211.301704	10.26745	10.26577
266.349859	11.10628	11.10424
322.397013	11.96034	11.95823
379.431081	12.82943	12.82701
437.656	13.71666	13.71394
497.077256	14.62213	14.62009
557.690044	15.54575	15.54366
650.910269	16.96625	16.96715
747.831551	18.44315	18.44242
814.135104	19.45349	19.45557

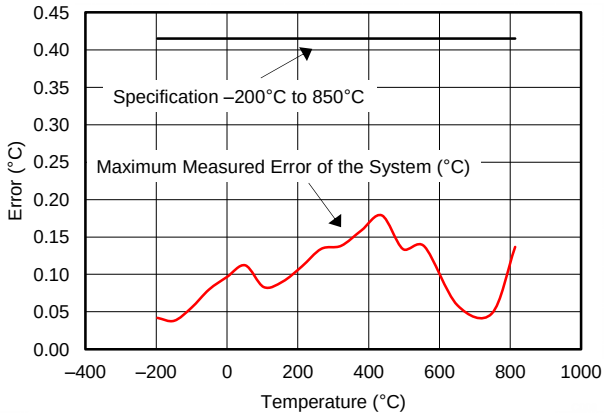


Figure 47. Maximum Measured Error of the Complete System Across –200°C to 850°C

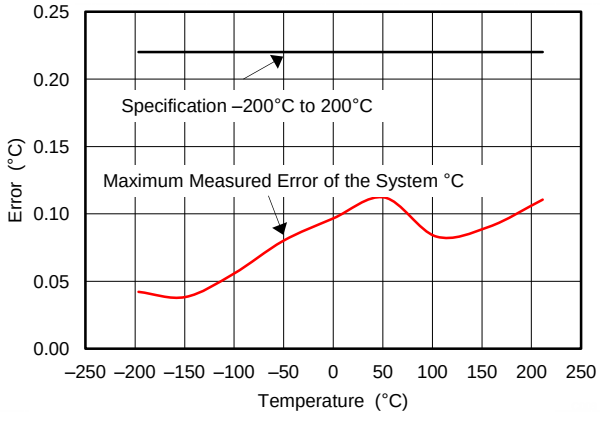


Figure 48. Maximum Measured Error of the Complete System Across –200°C to 200°C

6.7 Power Supply Influence

For the power-supply influence test, the power supply was vetted from 10 V to 30 V and the corresponding loop-current change was recorded. A 100-Ω precision resistor was connected to the RTD inputs for this measurement (see Figure 46). The total deviation of loop current across the power supply range was less than 0.30 µA.

6.8 Reverse Polarity Test

For the reverse polarity test, the power leads are connected to J1 without any polarized capacitor as shown in Figure 49.

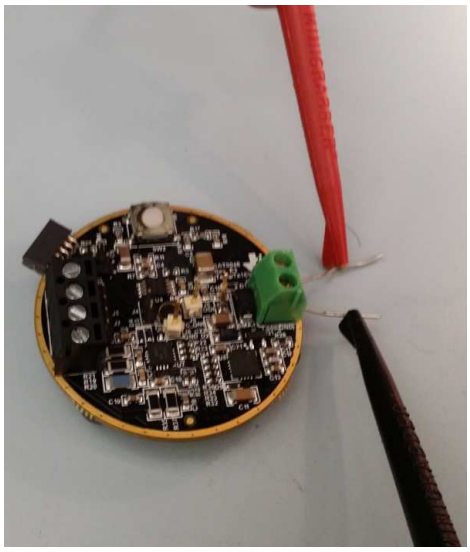


Figure 49. Reverse Polarity Test Setup

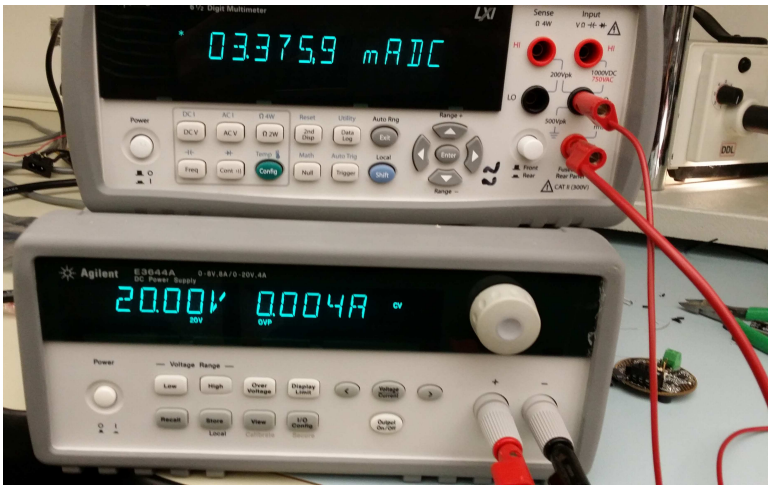


Figure 50. Reverse Polarity Setup With Correct Polarity

By default, an unprogrammed system draws 3.37 mA.

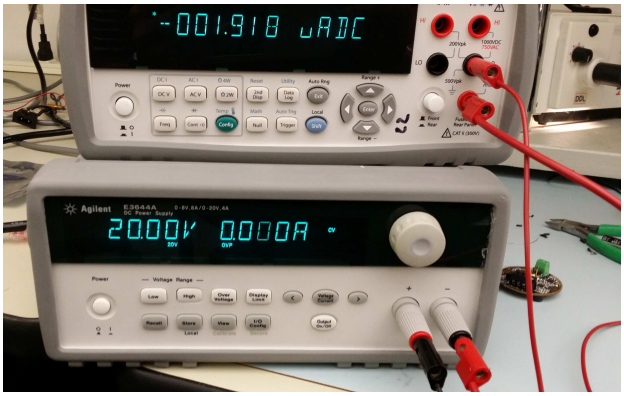


Figure 51. Reverse Polarity Measurement With Inverted Polarity

The leakage current of the system is only approximately 2 µA with reverse polarity applied.

6.9 Loop Power Consumption

The total loop power consumed by the design is 1.435 mA. Table 9 lists the total current consumed by each device.

Table 9. Loop Power Consumption

DEVICE	CURRENT
ADS1220	340 µA + 75 µA + 500 µA (biasing currents) = 915 µA (PGA 16, normal mode, sample rate of 20 SPS)
DAC161S997	100 µA
MSP430G2513	360 µA (Active Mode Current at 1 MHz, 3.3 V))
TPS7A4901	60 µA

For a loop powered system, having a low power consumption of approximately 1.4 mA ensures that the remainder of the budget (approximately [3.3 mA – 1.4 mA] = approximately 1.9 mA) can be used for system-level functions such as HART modem implementation.

6.10 IEC 61000-4-4 and IEC61000-4-2 Protection

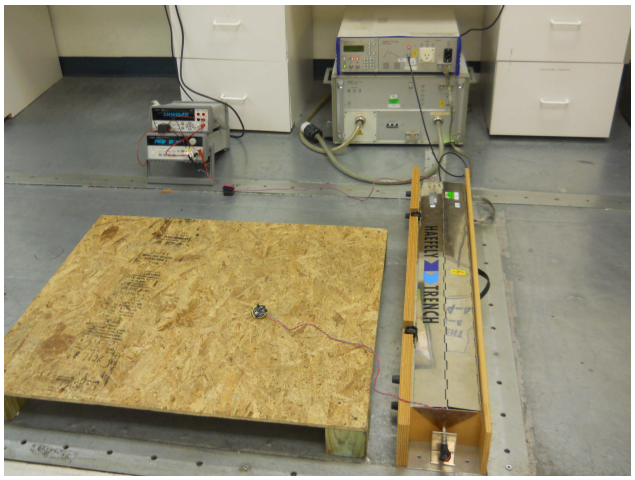


Figure 52. IEC61000-4-4 EFT Setup

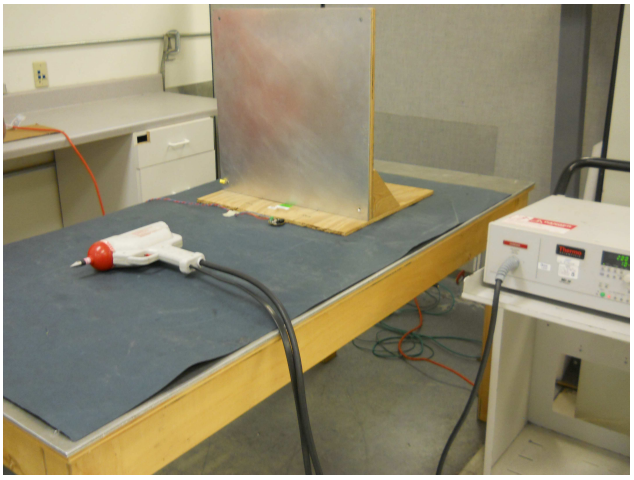


Figure 53. IEC61000-4-2 ESD Setup

For both IEC61000-4-4 and IEC61000-4-2 tests, the system was powered and loop current was measured before, during, and after the strike. In both the tests, the maximum deviation of the loop current measured was less than 3.5 µA which corresponds to 0.21°C (see Figure 47).

NOTE: IEC61000 tests were only performed on loop power inputs or the J1 connector.

Table 10. IEC61000 Test Data

IEC61000 TEST	RESULTS
IEC ESD on Loop Power	IEC61000-4-2, ESD: Horizontal Coupling Plane. Vertical Coupling Plane: ±4 kV — Class A
	IEC61000-4-2, ESD: Air Discharge: ±8 kV — Class A
IEC EFT on Loop Power	IEC61000-4-4: EFT ±2 kV — Class A

7 Schematics

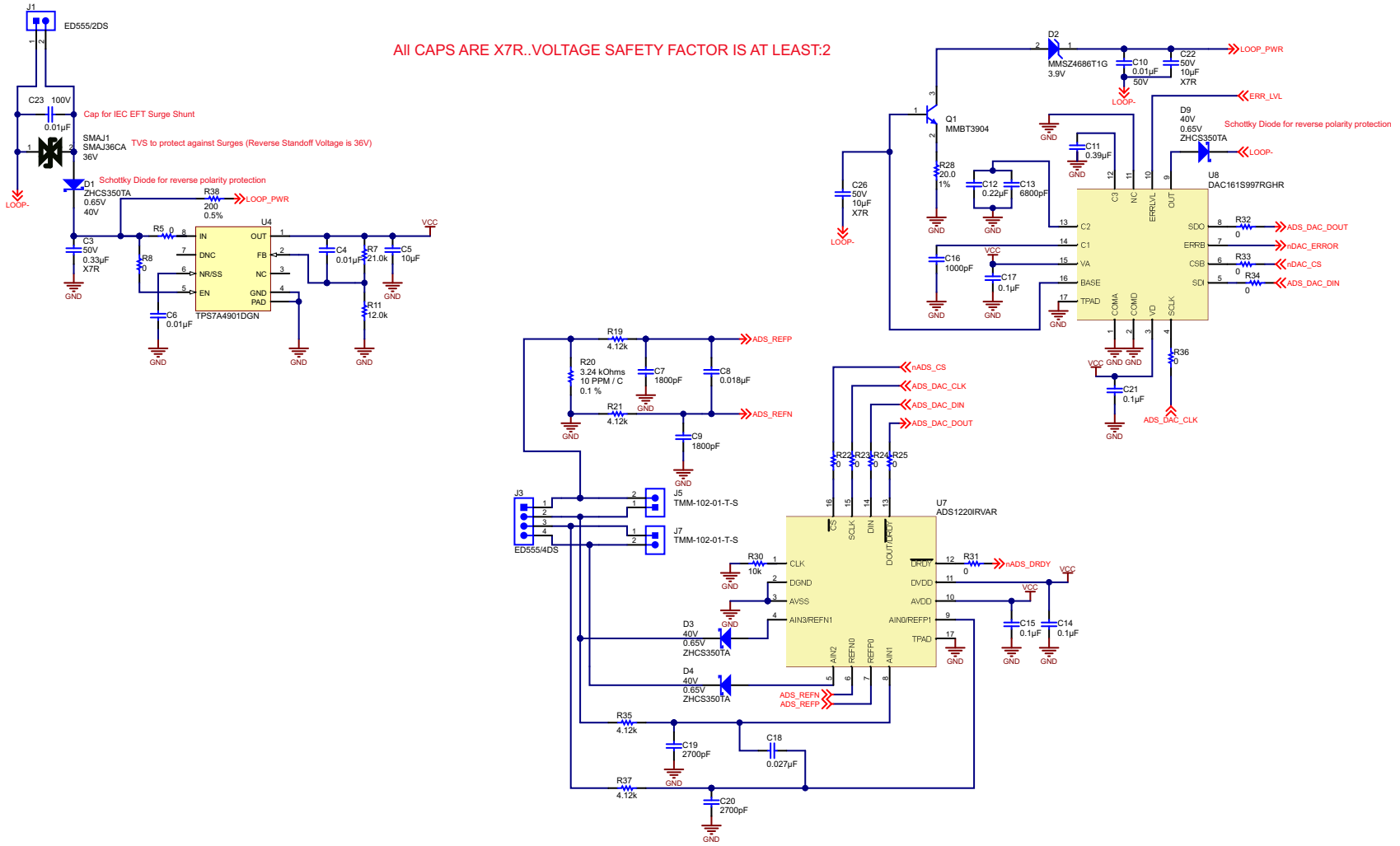


Figure 54. ADS1220, DAC161S997, Power Section

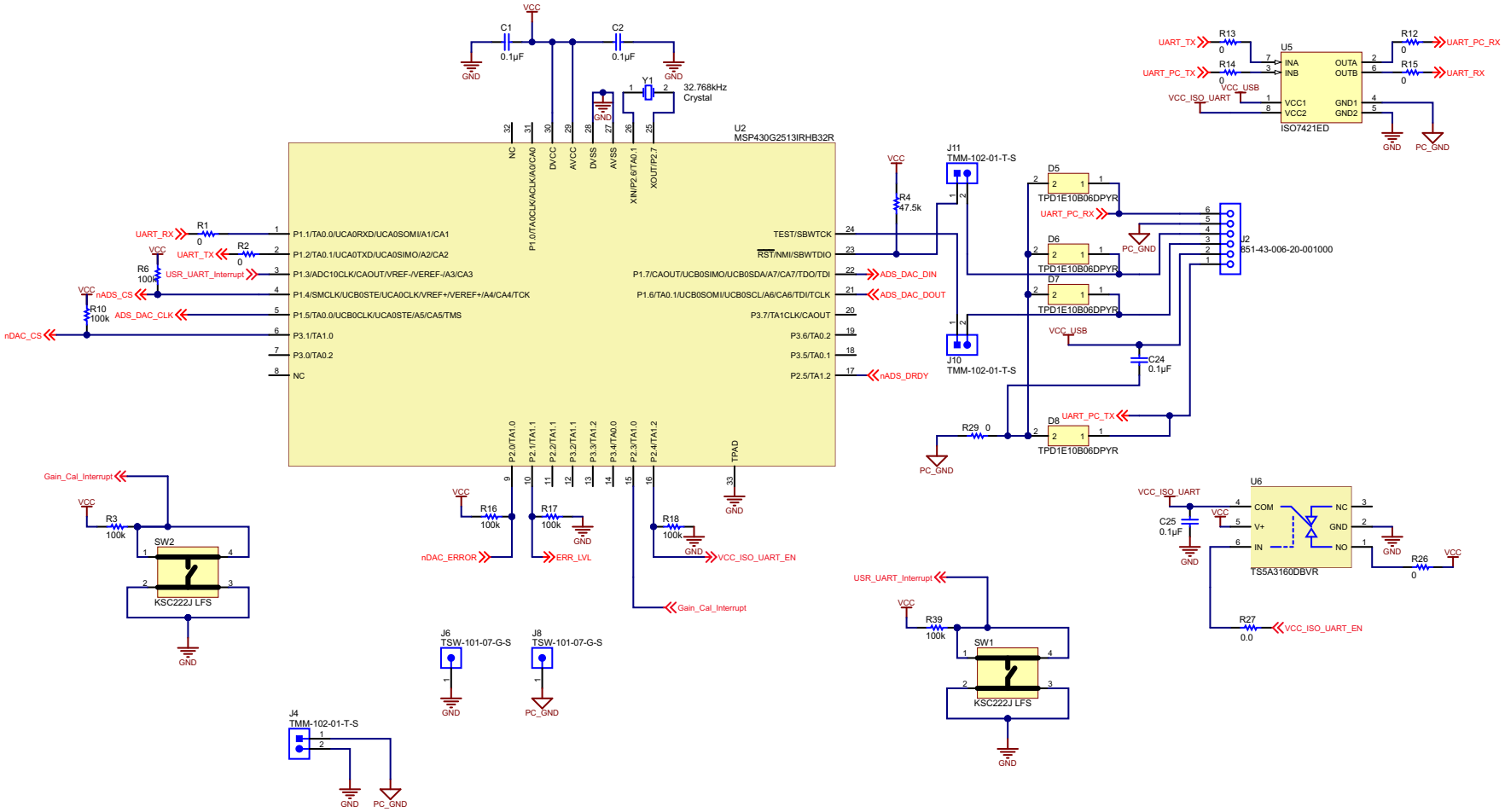


Figure 55. MSP430 Section

8 Bill of Materials

To download the bill of materials (BOM) for each board, see the design files at www.ti.com/tool/TIDA-0095. Table 11 lists the BOM.

Table 11. BOM

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
!PCB1	1		Printed Circuit Board		SAT0046	Any
C1, C2, C14, C15, C17, C21, C24, C25	8	0.1 µF	CAP, CERM, 0.1 µF, 16 V, ±10%, X7R, 0603	0603	C0603X104K4RACTU	Kemet
C3	1	0.33 µF	CAP, CERM, 0.33 µF, 50 V, ±10%, X7R, 1206	1206	12065C334KAT2A	AVX
C4, C6, C10	3	0.01 µF	CAP, CERM, 0.01 µF, 50 V, ±5%, X7R, 0603	0603	C0603C103J5RACTU	Kemet
C5	1	10 µF	CAP, CERM, 10 µF, 16 V, ±10%, X7R, 1206	1206	GRM31CR71C106KAC7L	MuRata
C7, C9	2	1800 pF	CAP CER 1800PF 100 V 10% X7R 0603	eg: 0603, used in PnP report	Used in BOM report	Used in BOM report
C8	1	0.018 µF	CAP, CERM, 0.018 µF, 100 V, ±10%, X7R, 0603	0603	C0603C183K1RACTU	Kemet
C11	1	0.39 µF	CAP, CERM, 0.39 µF, 50V, ±10%, X7R, 1206	1206	GRM31MR71H394KA01L	MuRata
C12	1	0.22 µF	CAP, CERM, 0.22 µF, 50V, ±5%, X7R, 1206	1206	C1206C224J5RACTU	Kemet
C13	1	6800 pF	CAP, CERM, 6800pF, 50V, ±5%, X7R, 0603	0603	C0603C682J5RACTU	Kemet
C16	1	1000 pF	CAP, CERM, 1000pF, 50V, ±5%, X7R, 0603	0603	C0603C102J5RACTU	Kemet
C18	1	0.027 µF	CAP, CERM, 0.027 µF, 100V, ±10%, X7R, 0603	0603	C0603C273K1RACTU	Kemet
C19, C20	2	2700 pF	CAP CER 2700PF 100V 10% X7R 0603	eg: 0603, used in PnP report	Used in BOM report	Used in BOM report
C22, C26	2	10 µF	CAP, CERM, 10 µF, 50V, ±10%, X7R, 1210	1210	GRM32ER71H106KA12L	MuRata
C23	1	0.01 µF	CAP, CERM, 0.01 µF, 100V, ±10%, X7R, 0603	0603	C1608X7R2A103K	TDK
D1, D3, D4, D9	4	0.65 V	Diode, Schottky, 40V, 0.35A, SOD-523	SOD-523	ZHCS350TA	Diodes Inc.
D2	1	3.9 V	Diode, Zener, 3.9V, 500mW, SOD-123	SOD-123	MMSZ4686T1G	ON Semiconductor
D5, D6, D7, D8	4		ESD in 0402 Package with 10 pF Capacitance and 6 V Breakdown, 1 Channel, –40°C to 125°C, 2-pin X2SON (DPY), Green (RoHS and no Sb/Br)	DPY0002A	TPD1E10B06DPYR	Texas Instruments
FID1, FID2, FID3, FID4, FID5, FID6	6		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
H1, H2, H3	3		Bumpon, Cylindrical, 0.312 X 0.200, Black	Black Bumpon	SJ61A1	3M
J1	1		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
J2	1		Receptacle, 50mil, 6x1, R/A, TH	Receptacle, 6x1, 50mil pitch, R/A	851-43-006-20-001000	Mill-Max
J3	1		Terminal Block, 6A, 3.5mm Pitch, 4-Pos, TH	14x8.2x6.5mm	ED555/4DS	On-Shore Technology
J4, J5, J7, J10, J11	5		Header, 2mm, 2x1, Tin, TH	Header, 2mm, 2x1	TMM-102-01-T-S	Samtec

Table 11. BOM (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer
J6, J8	2		Header, TH, 100mil, 1pos, Gold plated, 230 mil above insulator	Testpoint	TSW-101-07-G-S	Samtec
Q1	1	0.2 V	Transistor, NPN, 40V, 0.2A, SOT-23	SOT-23	MMBT3904	Fairchild Semiconductor
R1, R2, R5, R8, R12, R13, R14, R15, R22, R23, R24, R25, R26, R29, R31, R32, R33, R34, R36	19	0	RES, 0 ohm, 5%, 0.063W, 0402	0402	CRCW04020000Z0ED	Vishay-Dale
R3, R6, R10, R16, R17, R18, R39	7	100k	RES, 100 kΩ, 0.1%, 0.1W, 0603	0603	RT0603BRD07100KL	Yageo America
R4	1	47.5k	RES, 47.5 kΩ, 0.1%, 0.1W, 0603	0603	RG1608P-4752-B-T5	Susumu Co Ltd
R7	1	21.0k	RES, 21.0 kΩ, 1%, 0.1W, 0603	0603	RC0603FR-0721KL	Yageo America
R11	1	12.0k	RES, 12.0 kΩ, 1%, 0.1W, 0603	0603	RC0603FR-0712KL	Yageo America
R19, R21, R35, R37	4	4.12k	RES 4.12 kΩ 1/4W .1% 1206 SMD	1206 (3216 Metric)	ERA-8AEB4121V	Panasonic Electronic Components
R20	1	3.24 kΩ	Thin Film Resistors - SMD 3.24K .1% 10ppm	1206 (3216 metric)	PFC-W1206R-12-3241-B	IRC / TT electronics
R27	1	0.0	RES 0.0 OHM 1/10W JUMP 0603 SMD	0603 (1608 Metric)	ERJ-3GEY0R00V	Panasonic Electronic Components
R28	1	20.0	RES, 20.0 ohm, 1%, 0.1W, 0603	0603	CRCW060320R0FKEA	Vishay-Dale
R30	1	10k	RES, xxx ohm, x%, xW, [PackageReference]	0402 (1005 Metric)	CRCW040210K0FKEDHP	Vishay Dale
R38	1	200	RES, 200 ohm, 0.5%, 0.1W, 0603	0603	RT0603DRE07200RL	Yageo America
SMAJ1	1		DIODE TVS 36V 400W BI 5% SMD	DO-214AC, SMA	SMAJ36CA	Bourns Inc.
SW1, SW2	2		SWITCH TACTILE SPST-NO 0.05A 32V		KSC222J LFS	C&K Components
U2	1		IC MCU 16BIT 16KB FLASH 32QFN	32-VFQFN Exposed Pad	MSP430G2513IRHB32R	Texas Instruments
U4	1		+36V, +150mA, Ultralow-Noise, Positive LINEAR REGULATOR, DGN0008D	DGN0008D	TPS7A4901DGN	Texas Instruments
U5	1		50 Mbps Low-Power Dual Channels Digital Isolator, 3.3 V / 5 V, -40 to +125 degC, 8-pin SOIC (D), Green (RoHS and no Sb/Br)	D0008A	ISO7421ED	Texas Instruments
U6	1		IC SWITCH SPDT SOT23-6		TS5A3160DBVR	Texas Instruments
U7	1		Low-Power, Low-Noise, 24-Bit, Analog-to-Digital Converter for Small-Signal Sensors		ADS1220IRVAR	Texas Instrumetns
U8	1		IC DAC 16BIT SPI/SRL 16WQFN	16-WFQFN Exposed Pad	DAC161S997RGHR	Texas Instruments
Y1	1		Crystal, 32.768kHz, 12.5pF, SMD	2-SMD	NX3215SA-32.768K-STD-MUS-2	NDK

9 Layer Plots

To download the layer plots for each board, see the design files at www.ti.com/tool/TIDA-0095. Figure 56 shows the layer plots.

Figure 56. Layer Plot

10 Altium Project

To download the Altium project files for each board, see the design files at www.ti.com/tool/TIDA-0095. Figure 57, Figure 58, Figure 59, Figure 60, and Figure 61 show the layout.

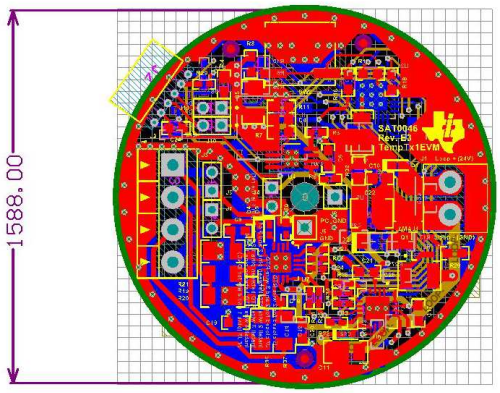


Figure 57. All Layers

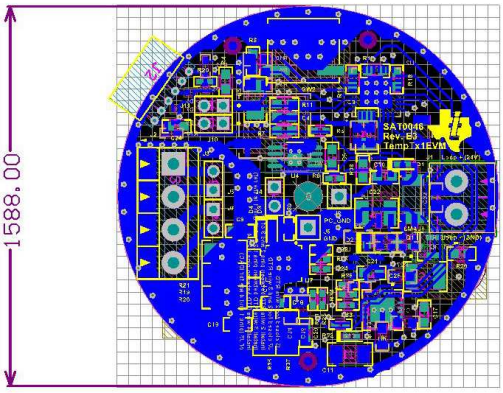


Figure 58. Bottom Layer

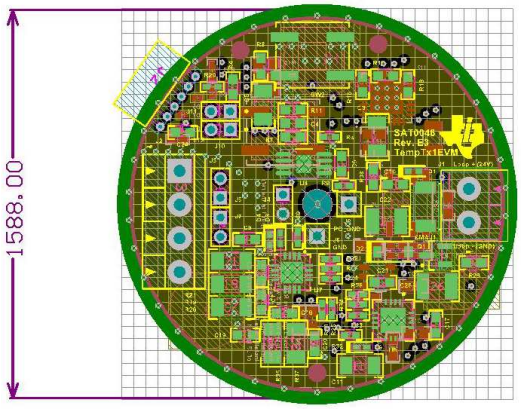


Figure 59. Ground Layer

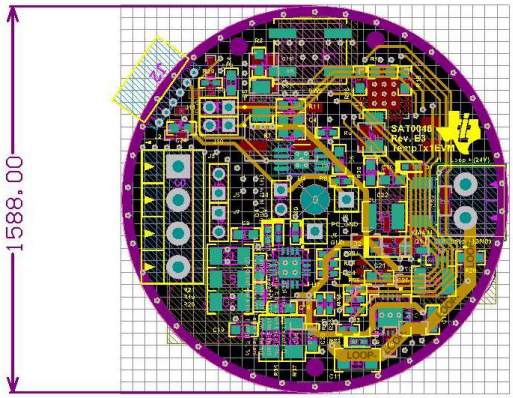


Figure 60. Inner Layer

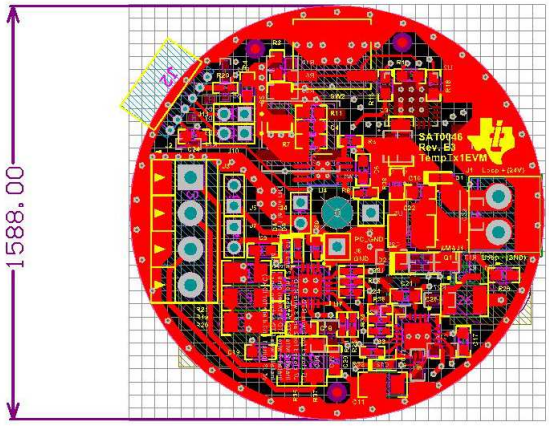


Figure 61. Top Layer

11 Layout Guidelines

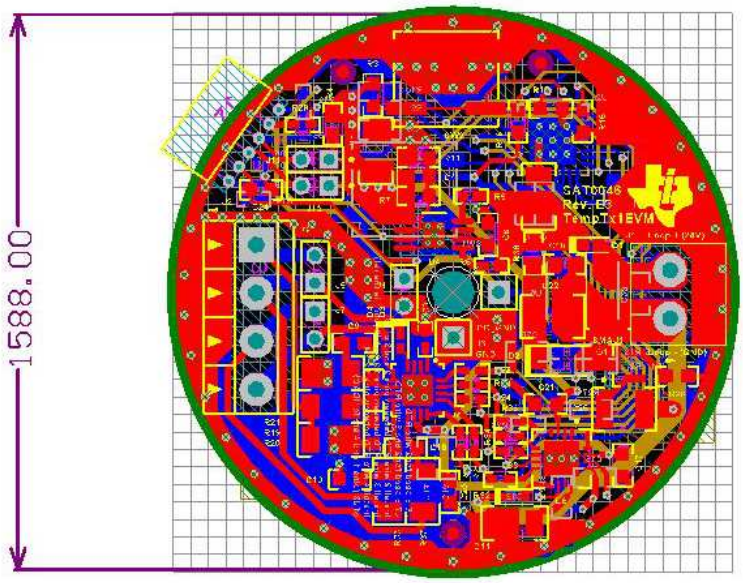


Figure 62. Via Stitching

To ensure high performance analog design, the ADS1220 device and the RTD inputs are isolated from the rest of the design through extensive ground via stitching. Any unused planes were stitched with ground vias as well.

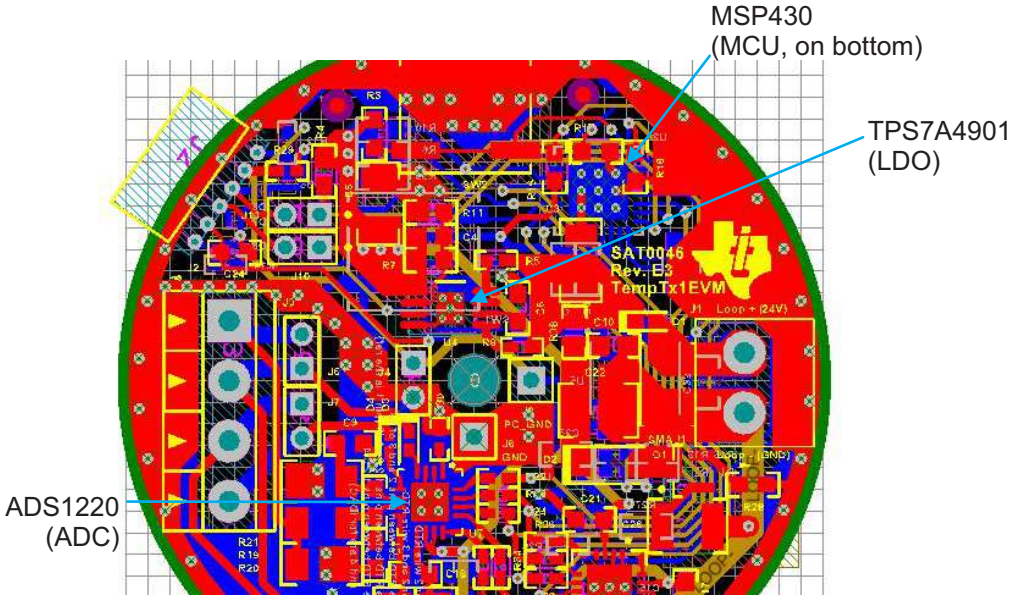


Figure 63. MSP430 and LDO With Respect to Analog Section

The MSP430 MCU and the LDO were placed as far as possible away from the ADS1220 device with no digital routes in the ADS1220 section.

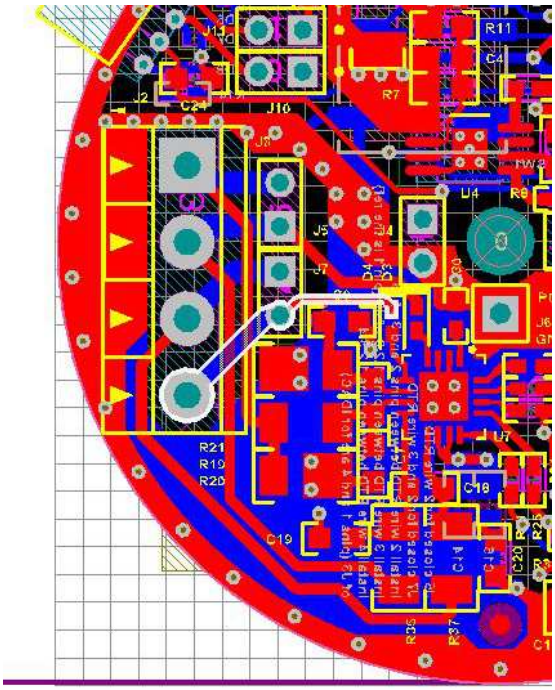


Figure 64. RTD Inputs

RTD inputs were routed without any vias other than the through-hole jumpers.

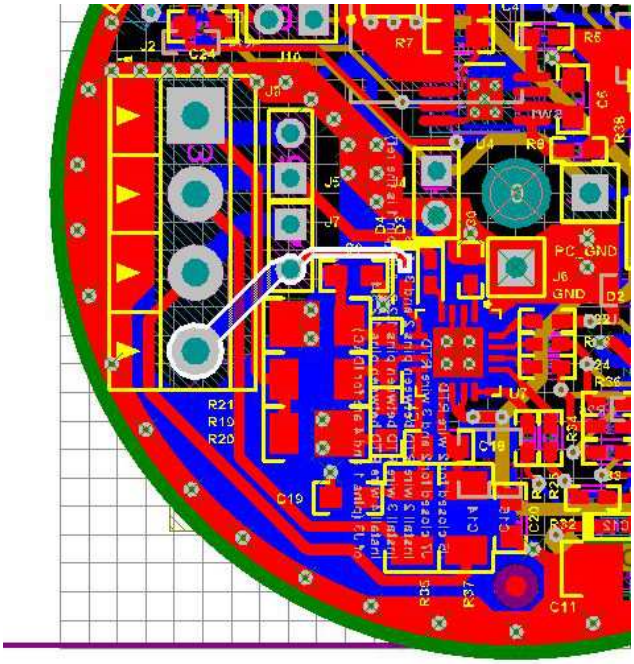


Figure 65. ADS1220 Section

No digital routes in the ADS1220 section.

12 Gerber Files

To download the Gerber files for each board, see the design files at www.ti.com/tool/TIDA-0095.

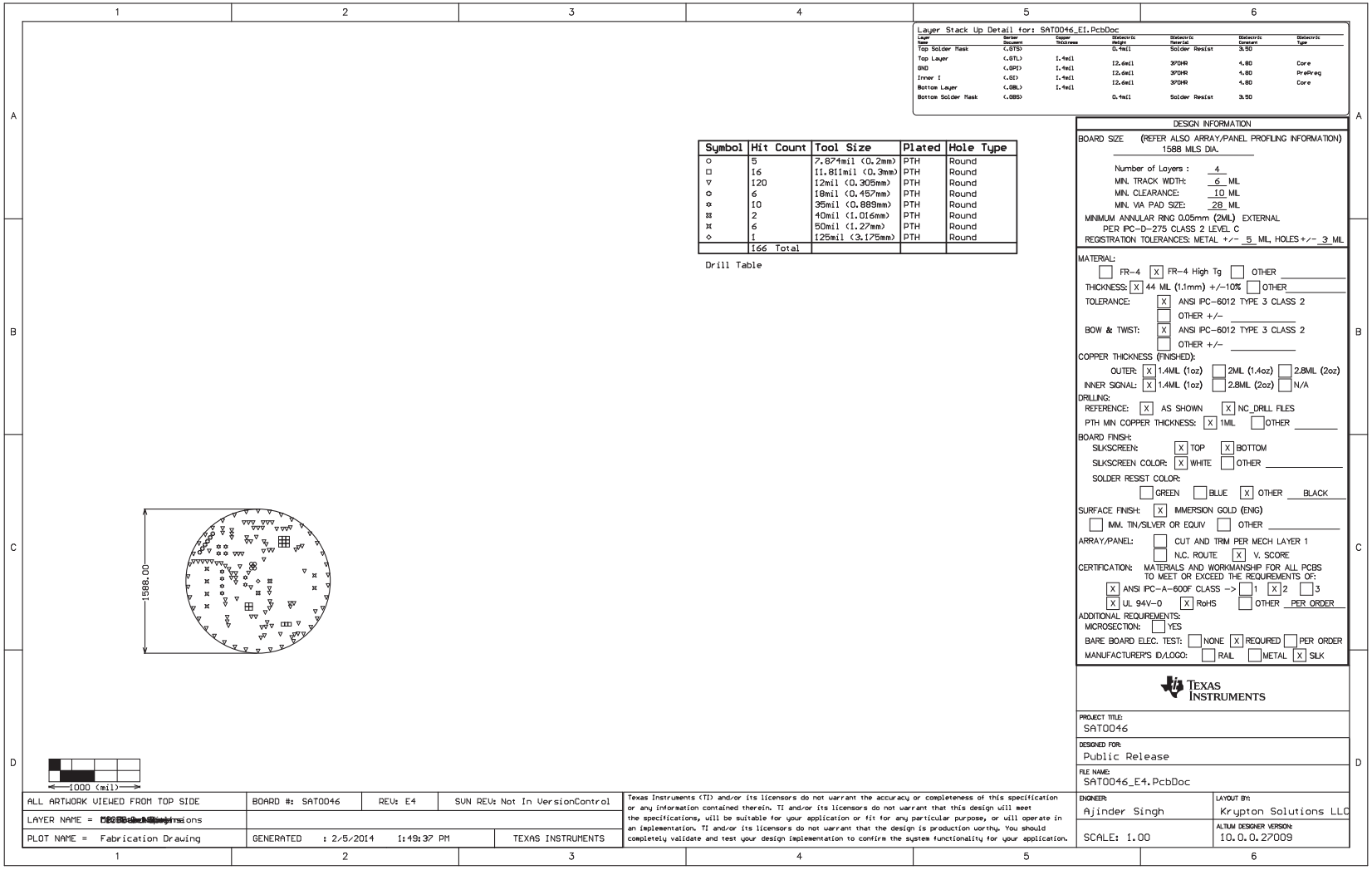


Figure 66. Fab Drawing

13 Assembly Drawings

To download the assembly drawings for the reference design, see the design files at www.ti.com/tool/TIDA-0095..

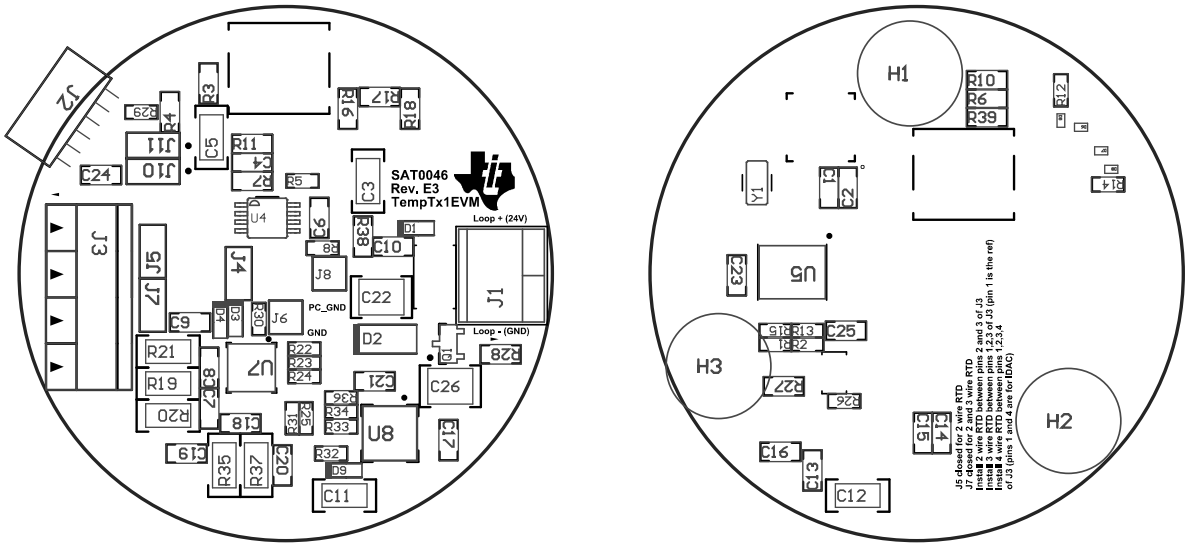


Figure 67. Assembly Drawings

14 Software Files

To download the software files for the reference design, see the design files at www.ti.com/tool/TIDA-0095.

15 References

For additional references, see the following:

1. Application Report, *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*, SBAA201
2. TI Precision Design Guide, *0-1A, Single-Supply, Low-Side, Current Sensing Solution*, TIDU040
3. TI Precision Design Guide, *Hardware-Compensated Ratiometric 3-Wire RTD System, 0°C – 100°C, 0.005°C Error*, TIDU045
4. ADS1220 Data Sheet, SBAS501
5. DAC161S997 Data Sheet, SNAS621
6. MSP430G2513 Data Sheet, SLAS735
7. TPS7A4901 Data Sheet, SBVS121

16 About the Author

AJINDER PAL SINGH is a Systems Architect at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Ajinder brings to this role his extensive experience in high-speed digital, low-noise analog and RF system-level design expertise. Ajinder earned his Master of Science in Electrical Engineering (MSEE) from Texas Tech University in Lubbock, TX. Ajinder is a member of the Institute of Electrical and Electronics Engineers (IEEE).

Revision History

Changes from Original (January 2014) to A Revision **Page**

- Changed schematic in Figure 16 for board revision to E4 19
- Changed schematic in Figure 17 for board revision to E4 20
- Changed schematic in Figure 18 for board revision to E4 20
- Added the *Power Supply Sequencing* section and schematic image showing capacitors C3, C22, and C26 21
- Changed schematic and board layout in Figure 20 for board revision to E4 22
- Changed schematic images Figure 54 and Figure 55 for board revision to E4 44
- Changed BOM in Table 11 for board revision to E4 46
- Changed layer plot images in Figure 56 for board revision to E4. Added two new layer plot images. 48
- Changed Altium layout images in Figure 57, Figure 58, Figure 59, Figure 60, and Figure 61 for board revision to E4 .. 49
- Changed the fab drawing in Figure 66 for board revision to E4 52
- Added the assembly drawings in Figure 67 for board revision to E4 53

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of EVMs for RF Products in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
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EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM’s electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI’s recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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