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Reinforced Isolated IGBT Gate-Drive Flyback Power Supply With Eight Outputs

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Design Resources

TIDA-00182	Design Page
UCC28701	Product Folder
CSD19533Q5A	Product Folder

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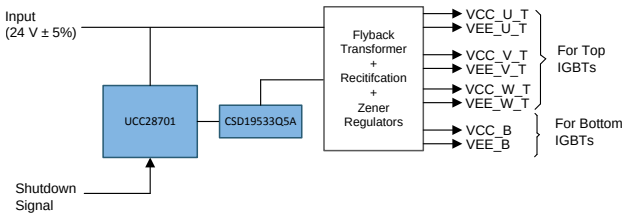
Design Features

- Reinforced Isolated Power Supply for IGBT Gate Drive
- Supports Six IGBT Gate Drivers for Three-Phase Inverter (Each Arm in Half-Bridge Configuration)
- Two Low-Ripple (<200 mV) Outputs for Each IGBT of Three-Phase Inverter: 16 V (×2) and –8.2 V (×2)
- Operates with Unregulated 24-V Input
- Output power: 2 W per IGBT
- Scalable to Support Higher Power IGBTs
- Output Capacitors Rated to Support up to 6-A Peak Gate Drive Current
- Option to Shut Down the Power Supply to Facilitate Safe Torque Off (STO) Feature
- Designed to Comply with IEC61800-5

Featured Applications

- Variable Speed AC/DC Drives
- Industrial and Solar Inverters
- UPS Systems
- Servo Drives
- IGBT-Based HVDC Systems



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1 System Description

This reference design provides reinforced isolated positive and negative voltage rails required for insulated-gate bipolar transistor (IGBT) gate drivers from a single 24-V DC input supply. IGBTs are used in three-phase inverters for variable-frequency drives to control the speed of AC motors. This reference design uses a flyback topology and provides isolation compliant with IEC61800-5 and is intended to operate from a pre-regulated 24-V DC input. With a regulated input source (within 5%), a primary side regulated controller can regulate the line and load well.

This reference design uses a single transformer for generating power rails for all three arms of the three-phase inverter. The voltage rails for all the top IGBTs are isolated whereas the voltage rails for all bottom IGBTs are combined. Larger IGBTs for higher power drives sometimes require more gate drive current than what is provided by a typical IGBT gate driver; designers often use additional transistors for gate current boosting. This reference design provides 16 V on the positive outputs and –8.2 V on the negative outputs to compensate for the added voltage drops in these transistors.

Three-phase inverters are used for variable-frequency drives to control the speed of AC motors and for high power applications such as a high-voltage, direct current (HVDC) power transmission. The typical application of a three-phase inverter using six isolated gate drivers is shown in Figure 1. Note that each phase uses a high-side and a low-side IGBT switch to apply positive and negative HVDC pulses to the motor coils in an alternating mode.

High-power IGBTs require isolated gate drivers to control their operations. Each IGBT is driven by a single isolated gate driver that galvanically isolates the high-voltage output from the low-voltage controlled inputs. The emitter of the top IGBT floats, which necessitates using an isolated gate-driver. In order to isolate the high-voltage circuit with a low-voltage control circuit, isolated gate drivers are used to control the bottom IGBTs.

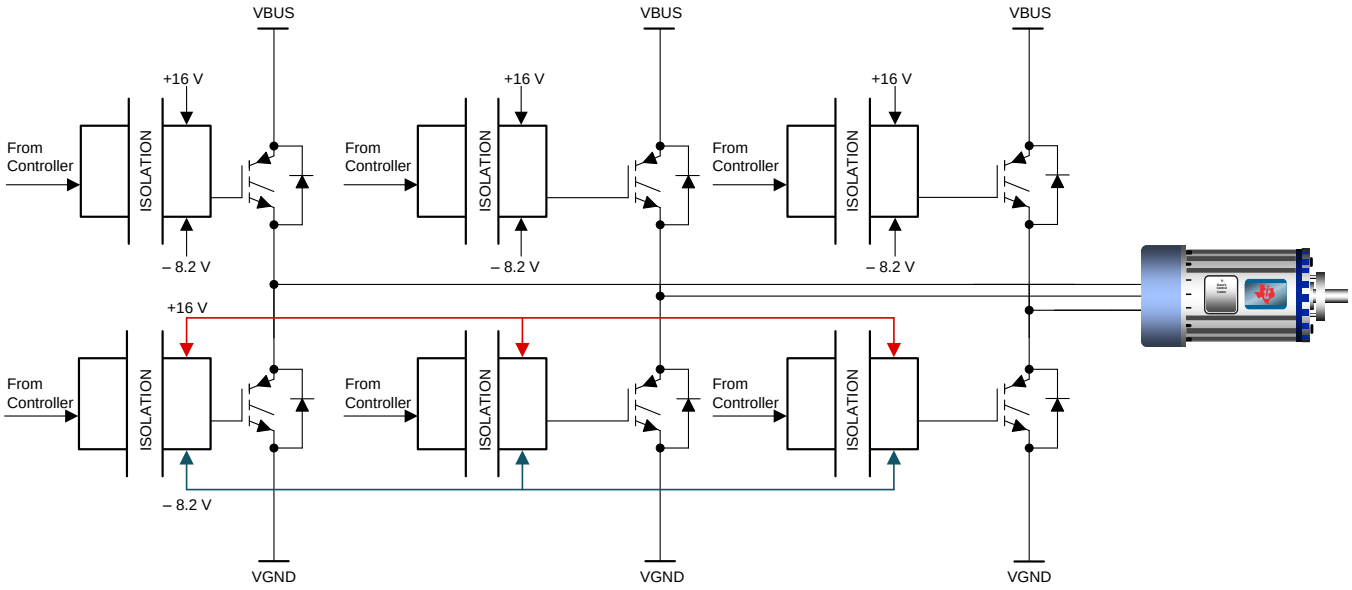


Figure 1. Three-Phase Inverter with Isolated Gate Drive

1.1 Requirements of a Gate Drive Supply

To reduce conduction losses, the gates of the IGBTs are supplied with a much higher voltage than the actual gate-threshold voltages. Typically, 15 to 18 V are applied at the gate to reduce the $V_{CE(on)}$.

The IGBT is a minority carrier device with a high-input impedance and has a large, bipolar current-carrying capability. The switching characteristics of an IGBT are very much similar to that of a power MOSFET. Assuming identical conditions, IGBTs and MOSFETs behave identically when turned on, and both have similar current rise and voltage fall times. However, the waveforms of the switched current are different when turned off.

At the end of the switching event, the IGBT has a *tail current*, which does not exist for the MOSFET. This tail is caused by minority carriers trapped in the base of the bipolar output section of the IGBT, which causes the device to remain turned on. Unlike a bipolar transistor, the IGBT cannot extract these carriers to speed up switching as there is no external connection to the base, so the device remains turned on until the carriers recombine.

This *tail current* increases the turn-off losses and requires an increase in the dead time between the conduction of two devices in a half-bridge circuit. To reduce the turn-off time, have a negative voltage (–5 to –10 V) at the gate.

When activated, an IGBT generates some voltage spikes on the gate terminal due to the high dv/dt and parasitic capacitance between the gate and emitter. The voltage spikes can cause a false turn-on of the bottom IGBT. A negative voltage at the gate helps to avoid this false turn-on trigger.

Usually, 16 V is applied to the gate for turn-on and –8 V for turn-off.

Next, decide on the power requirement to drive the IGBT. Equation 1 calculates the gate drive power requirement for different power ratings of variable speed drives:

$$P_{gate} = P_{driver} + \left(Q_{gate} \times f_{sw} \times \Delta V_{gate}\right) + \left(C_{ge} \times f_{sw} \times \Delta V_{gate}^{2}\right) \quad (1)$$

where

- Q_{gate} = Total gate charge
- f_{sw} = Switching frequency
- ΔV_{gate} = Gate driver output voltage swing

Note that the second term in Equation 1 reflects power requirement for IGBT gate capacitance and the third term reflects the power requirement for additional external capacitance as shown in Figure 2.

As noted earlier, an isolated gate driver is used to turn the IGBT on and off. In this process, power is dissipated by the driver IC, IGBT gate, and by any RC circuits in the gate drive path (see Figure 2).

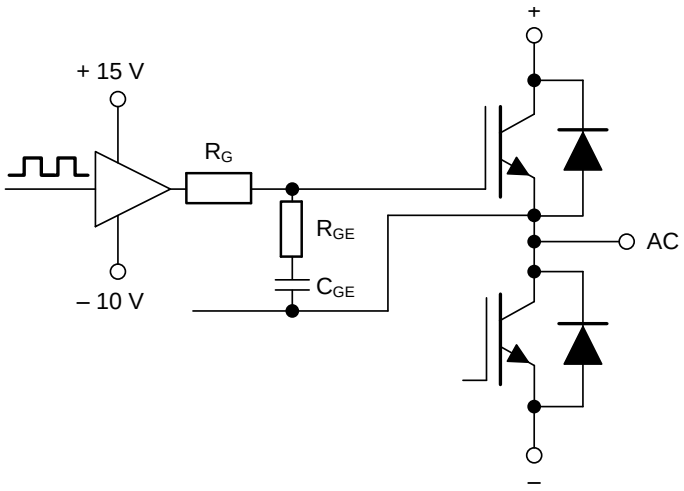


Figure 2. IGBTs with Gate Drive Circuitry for Gate Power Calculation

Considering the following example:

- An IGBT module with 1200 V/200 A capacity (appropriate for <100 kW drives) having Q_{gate} = 1.65 µC.
- A switching frequency of 16 kHz, considered high for typical high-power drives.
- A gate voltage, swinging from –15 to 15 V. These values are a worst case condition since IGBTs are typically driven with 15 V and either –5 or –8 V.
- Gate-to-Emitter capacitance (C_{ge}) = 20 nF (typical value ranges between 1 and 20 nF)
- Gate driver total power consumption (P_{driver}) = approximately 600 mW. This value is estimated using the typical data sheet of an isolated IGBT gate-driver.

Using the values above,

$$P_{gate} = 0.6\,W + 0.792\,W + 0.288\,W = 1.68\,W \quad (2)$$

With de-rating, Equation 2 comes to 2 W per IGBT.

The current output of a gate-driver may or may not be sufficient to drive the IGBT, so designers use transistors for current boosting. This reference design is designed for 16 V on positive output and –8.2 V on the negative output, which ultimately takes care of the appproimate 1-V drop in the transistors.

2 Design Features

The primary objective of this design is to replace the discrete components used in a power supply design with that of a PWM controller-based gate drive power supply. Replacing these components leads to a reduced bill of materials (BOM) and an increased reliability and performance.

2.1 Design Requirements

The system-level requirements for this design include:

- A PWM controller and a topology that helps scale the output power while driving high-power IGBTs
- Isolated positive and negative rails (16 and –8 V) to power the isolated gate driver and the gates of the IGBTs
- Continuous output power of 2 W to drive each IGBT
- Support up to a 6-A peak current, with an output voltage ripple of less than 200 mV
- The ability to shut down the power supply to support the STO feature to comply with safety-relatedIEC61800-5-1 standards

2.2 Topology Selection

This reference design is intended to operate with an unregulated 24-V input. To save costs, have one transformer generate all the isolated rails to feed the gate driver and avoid any use of opto-based feedback. Flyback topology with primary-side regulation meets these requirements. The requirements of the PWM controller, MOSFETs, and transformer are listed here:

- PWM Controller
  - Should support flyback topology
  - Should support primary-side regulation
  - Shutdown feature to incorporate STO functionality
  - Operate from a 24-V supply
- Power MOSFETs
  - Should have a rated VDS ≥100 V to support a 24-V input supply
  - Should support 3-A drain current (minimum)
- Transformer specifications (as per IEC61800-5-1)
  - Four isolated outputs: Vout1 = 25 V at 150 mA, Vout2 = 25 V at 150 mA, Vout3 = 25 V at 150 mA, and Vout4 = 25 V at 450 mA
  - Switching frequency = 100kHz
  - Primary to secondary isolation = 7.4 kV for 1.2/50-µs impulse voltage
  - Type test voltage:
    - Primary to Secondary = 3.6 kV_{RMS}
    - Secondary1 to Secondary2 = 1.8 kV_{RMS}
    - Secondary2 to Secondary3 = 1.8 kV_{RMS}
    - Secondary3 to Secondary4 = 1.8 kV_{RMS}
  - Spacings:
    - Primary to Secondary clearance = 8 mm
    - Secondary1 to Secondary2 clearance = 5.5 mm
    - Secondary2 to Secondary3 clearance = 5.5 mm
    - Secondary3 to Secondary4 clearance = 5.5 mm
    - Creepage distance = 9.2 mm
  - Functional isolation primary and secondaries = 1.5-kV DC
  - DC isolation between secondaries = 1.5-kV DC

The aforementioned spacing, creepage, and impulse test voltage are met by considering reinforced isolation. If the drive architecture requires only basic or functional isolation, the transformer can be redesigned. Lower levels of spacing and creepage values significantly reduces the size of the transformer.

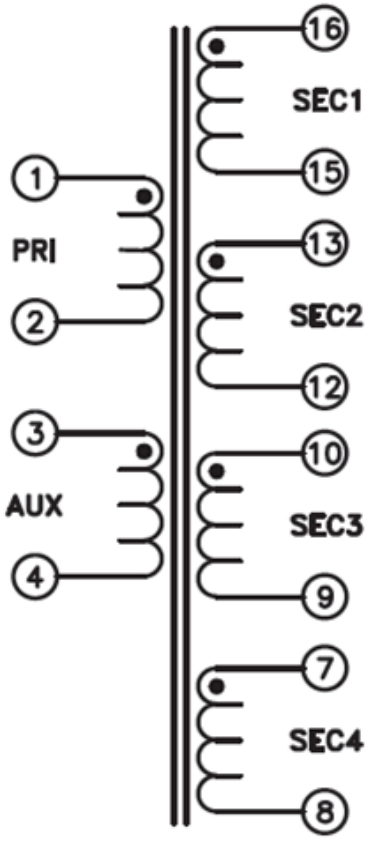


Figure 3. Flyback Transformer Symbol for TIDA-00182

3 Block Diagram

This reference design is intended for motor control, industrial inverters, and many other applications that use IGBT drivers and should help to reduce design time significantly while meeting all of the design requirements. The design files include schematics, bill of materials (BOM), layer plots, Altium files, Gerber files, and test results.

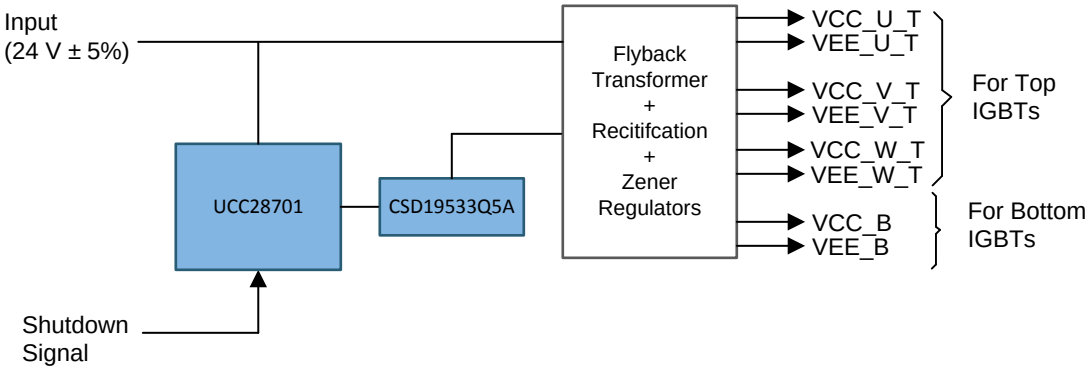


Figure 4. System Block Diagram

4 Highlighted Products

This reference design features the following devices, which were selected based on their specifications:

- UCC28701 Constant-Voltage, Constant-Current PWM Controller with Primary-Side Regulation
- CSD19533 NexFET™ power MOSFET

For more information on each of these devices, see the respective product folders at www.ti.com or click on the links for the product folders on the first page of this reference design (Design Resources).

4.1 Component Selection

The following components were selected based on their specifications.

4.1.1 UCC28701

The UCC28700 is a flyback power supply controller that provides accurate voltage and constant current regulation with primary-side feedback, eliminating the need for optocoupler feedback circuits. The controller operates in discontinuous conduction mode with valley switching to minimize switching losses. The modulation scheme is a combination of frequency and primary peak current modulation to provide high conversion efficiency across the load range. The controller has a maximum switching frequency of 130 kHz and allows for a shutdown operation using the NTC pin.

4.1.2 CSD19533

This 100-V, 7.8-mΩ, SON 5 × 6-mm NexFET™ power MOSFET minimizes losses in power conversion applications. The maximum drain current capability is much higher than the 3-A design requirement.

4.2 Circuit Design

4.2.1 Powering Up UCC28701

The VDD pin of UCC28701 is connected to a bypass capacitor to ground and a start-up resistance to the input bulk capacitor positive terminal. The VDD turn-on UVLO threshold is 21 V and turn-off UVLO threshold is 8.1 V, with an available operating range up to 35 V. The wide VDD range provides the advantage of selecting a relatively small VDD capacitor and high-value start-up resistance to minimize no-load standby power loss in the start-up resistor. Because the input voltage for this reference design is 24 V, a smaller value (10 kΩ) of a start-up resistor is used along with a VDD capacitor of 2.2 µF. After applying the input voltage to the converter, the start-up resistor connected to VDD from the bulk capacitor voltage charges the VDD capacitor. When charging the VDD capacitor, the device bias supply current is less than 1.5 µA. When VDD reaches the 21-V UVLO turn-on threshold, the controller is enabled and the converter starts switching. The initial three cycles are limited to $I_{PP(min)}$, which allows sensing any initial input or output faults with minimal power delivery. After the initial three cycles at minimum $I_{PP(min)}$, the controller responds to the condition dictated by the control law. The converter remains in discontinuous mode while charging the output capacitors, maintaining a constant output current until the output voltage regulates.

NOTE: The minimum voltage on the 24-V input rail that can guarantee start-up has to be >23 V because of the UCC28701 $V_{VDD(on)(max)}$ specifications.

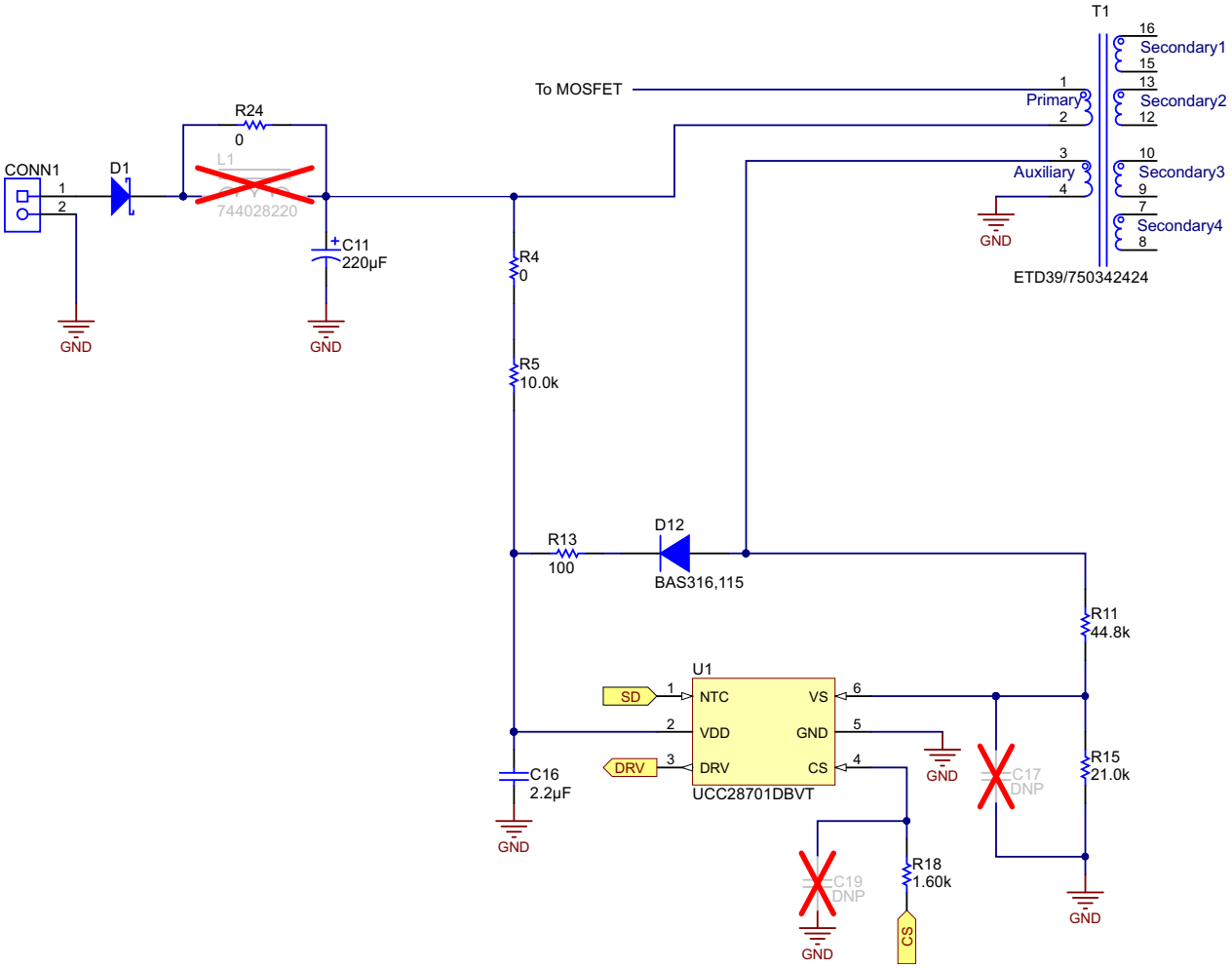


Figure 5. Powering Up UCC28701

4.2.2 Transformer Design

For designing the transformer, important parameters are primary-to-secondary turns ratio, auxiliary-to-secondary turns ratio, and primary winding inductance. The maximum primary-to-secondary turns ratio can be determined by the target maximum switching frequency at full load, the minimum input capacitor bulk voltage, and the estimated discontinuous conduction mode (DCM) quasi-resonant time. Before calculating the transformer parameters, determine the maximum available total duty cycle of the on-time and secondary conduction time based on target switching frequency and DCM resonant time. D_{MAGCC} is defined as the secondary diode conduction duty cycle during constant-current (CC) operation, which is set internally by the UCC28701 at 0.425. For the transition mode operation limit, the period required from the end of secondary current conduction to the first valley of the V_{DS} is half of the DCM resonant period. D_{MAX} can be determined using Equation 3:

$$D_{MAX} = 1 - \left(\frac{T_R}{2} \times f_{MAX} \right) - D_{MAGCC} \quad (3)$$

where

- D_{MAX}: MOSFET on-time duty cycle
- T_R: Resonant frequency during the DCM time, assuming T_R = 2 uS for resonant frequency of 500 kHz
- f_{MAX}: Target full-load maximum switching frequency of the converter
- D_{MAGCC}: Secondary diode conduction duty cycle in CC, (equal to 0.425 for UCC28701)

For this reference design, f_{MAX} is 100 kHz, which calculates D_{MAX} = 0.475

Once D_{MAX} is known, the maximum turns-ratio of the primary to secondary can be determined with Equation 4. Determine the total voltage on the secondary winding, which is the sum of V_{OCV} and the secondary rectifier V_F.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times (V_{OCV} + V_F)} \quad (4)$$

where

- N_{PS}: Transformer primary-to-secondary turns ratio.
- D_{MAX}: MOSFET on-time duty cycle
- $V_{BULK(min)}$: Minimum voltage on input bulk capacitor at full power
- D_{MAGCC}: Secondary diode conduction duty cycle in CC (equal to 0.425 for UCC28701)
- V_{OCV}: Regulated output voltage of the converter
- V_F: Secondary rectifier forward voltage drop at near-zero current

UCC28701 has UVLO threshold of 21 V, so keep $V_{BULK(min)}$ equal to 21 V. The outputs are required to provide 16 and –8 V at the same time, so select V_{OCV} equal to 25 V. Use a schottky diode as a secondary rectifier having forward voltage drop equal to 0.3 V. With all these values, the calculated value of $N_{PS(max)}$ is 0.92, and N_{PS} is finalized as 0.9.

The UCC28701 controller CC regulation is achieved by maintaining a maximum D_{MAG} duty cycle of 0.425 at the maximum primary current setting. The transformer turns ratio and CC-regulating voltage determine the current sense resistor for a target constant current (Equation 5). Because not all of the energy stored in the transformer is transferred to the secondary, a transformer efficiency term is included. This efficiency number includes the core and winding losses, leakage inductance ratio, and bias power ratio to rated output power.

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 I_{OCC}} \times \eta_{XFMR} \quad (5)$$

where

- R_{CS}: Primary current programming resistance
- V_{CCR}: CC-regulating voltage constant (equals 319 mV, typical from UCC28701 datasheet)
- N_{PS}: Transformer primary-to-secondary turns ratio
- η_{XFMR}: Transformer primary-to-secondary power transfer efficiency, assume η_{XFMR} = 0.8
- I_{OCC}: Converter output CC target

The total output current from the reference design is 0.5 A. Keeping some margin, take I_{OCC} equal to 0.55 A. Using these values, the calculated value of R_{CS} is 0.2 Ω.

The transformer primary current is simply the maximum current sense threshold divided by the current sense resistance (Equation 6):

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}}$$

where

- $I_{PP(max)}$: Maximum transformer primary current.
- $V_{CST(max)}$: CS pin maximum current-sense threshold (equals 750 mV, typical from UCC28701 datasheet)
- R_{CS}: Primary current programming resistance. (6)

With R_{CS} equal to 0.2 Ω, the maximum transformer primary current equals 3.75 A.

Calculate the primary transformer inductance using the standard energy storage equation for flyback transformers. The primary current, maximum switching frequency, and output and transformer power losses are included in Equation 7:

$$L_P = \frac{2\left(V_{OCV} + V_F\right) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(max)}^{2} \times f_{MAX}}$$

where

- L_P: Transformer primary inductance
- V_{OCV}: Regulated output voltage of the converter
- V_F: Secondary rectifier forward voltage drop at near-zero current
- I_{OCC}: Converter output CC target
- η_{XFMR}: Transformer primary-to-secondary power transfer efficiency
- $I_{PP(max)}$: Maximum transformer primary current
- f_{MAX}: Target full-load maximum switching frequency of the converter (7)

With V_{OCV} = 25 V, V_F = 0.3 V, I_{OCC} = 0.55 A, η_{XFMR} = 0.8, $I_{PP(max)}$ = 3.75 and f_{MAX} = 100 kHz, the calculated value of L_P is 24 uH.

The secondary winding to auxiliary winding transformer turns ratio is determined by the lowest target operating output voltage in constant-current regulation and the V_{DD} UVLO of the UCC28701. The transformer leakage inductance energy supplies additional energy to V_{DD}, which allows a lower turns ratio to be used, if required. Equation 8 calculates for the same:

$$N_{AS} = \frac{V_{DD(off)} + V_{FA}}{V_{OCC} + V_F}$$

where

- N_{AS}: Transformer auxiliary-to-secondary turns ratio
- $V_{DD(off)}$: UVLO turn-off voltage (equals 8.1 V, typical from UCC28701 datasheet)
- V_{FA}: Auxiliary rectifier forward voltage drop
- V_{OCC}: Target lowest converter output voltage in CC regulation
- V_F: Secondary rectifier forward voltage drop at near-zero current (8)

For a 5% regulation, V_{OCC} is 23.75 V, and assuming secondary rectifier diode and auxiliary rectifier diode have the same forward voltage drop of 0.3 V, the calculated value of N_{AS} is 0.35. This design uses an N_{AS} of 0.5.

4.2.3 Transformer Parameter Verification

The transformer turns ratio selected affects the MOSFET VDS and secondary rectifier reverse voltage, so review these aspects. The UCC28701 controller requires a minimum on time of the MOSFET (T_{ON}) and minimum DMAG time (T_{DMAG}) of the secondary rectifier in the high line, minimum load condition. The selection of f_{MAX}, L_P and R_{CS} affects the minimum T_{ON} and T_{DMAG}. The secondary rectifier and MOSFET voltage stress can be determined by Equation 9.

$$V_{REV} = \frac{V_{IN(max)}}{N_{PS}} + V_{OCV}$$

where

- V_{REV}: Peak reverse voltage on the secondary rectifier
- $V_{IN(max)}$: Maximum input voltage to the converter
- V_{OCV}: Regulated output voltage of the converter
- N_{PS}: Transformer primary-to-secondary turns ratio (9)

With $V_{IN(max)}$ = 25.2 V (5% higher than 24 V), the calculated value of V_{REV} = 53.3 V. This reference design uses secondary rectifier diodes with V_{REV} equal to 100 V.

For the MOSFET VDS voltage stress, include an estimated leakage inductance voltage spike (V_{LK}). Equation 10 calculates the MOSFET VDS voltage stress.

$$V_{DSPK} = \left(V_{IN(max)}\right) + \left(V_{OCV} + V_F\right) \times N_{PS} + V_{LK}$$

where

- V_{DSPK}: Peak MOSFET drain-to-source voltage at high line
- $V_{IN(max)}$: Maximum input voltage to the converter
- V_{OCV}: Regulated output voltage of the converter
- V_F: Secondary rectifier forward voltage drop at near-zero current
- V_{LK}: Estimated leakage inductance energy reset voltage
- N_{PS}: Transformer primary-to-secondary turns ratio (10)

Assuming V_{LK} = 25 V, the peak drain-to-source voltage V_{DSPK} equals 73 V. This reference design uses MOSFET with $V_{DS(max)}$ equal to 100 V.

Equation 11 and Equation 12 are used to determine if the minimum T_{ON} target of 300 ns and minimum T_{DMAG} target of 1.1 µs are achieved. These values are required by UCC28701 for proper sensing, valley switching, and operation of the device.

$$T_{ON(min)} = \frac{L_P}{V_{IN(max)}} \times \frac{I_{PP(max)} \times V_{CST(min)}}{V_{CST(max)}}$$

where

- $T_{ON(min)}$: Minimum MOSFET on time
- L_P: Transformer primary inductance
- $I_{PP(max)}$: Maximum transformer primary current
- $V_{CST(min)}$: CS-pin minimum current-sense threshold (equals 250 mV, typical from UCC28701 datasheet)
- $V_{IN(max)}$: Maximum input voltage to the converter
- $V_{CST(max)}$: CS pin maximum current-sense threshold (equals 750 mV, typical from UCC28701 datasheet) (11)

The calculated value of $T_{ON(min)}$ is 1.2 us, which is higher than the target of 300 ns.

$$T_{DMAG(min)} = \frac{T_{ON(min)} \times V_{IN(max)}}{N_{PS} \times (V_{OCV} + V_F)}$$

where

- $T_{DMAG(min)}$: Minimum secondary rectifier conduction time
- $T_{ON(min)}$: Minimum MOSFET on time
- N_{PS}: Transformer primary-to-secondary turns ratio
- V_{OCV}: Regulated output voltage of the converter
- V_F: Secondary rectifier forward voltage drop at near-zero current (12)

The calculated value of $T_{DMAG(min)}$ is 1.33 us, which is higher than the target of 1.1 us.

4.2.4 Primary Side Regulation

In primary-side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. To accurately represent the secondary output voltage on the auxiliary winding, the discriminator (inside UCC28701) reliably blocks the leakage inductance reset and ringing, continuously samples the auxiliary voltage during the down slope after the ringing is diminished, and captures the error signal at the time the secondary winding reaches zero current. The internal reference on VS is 4.05 V, and it is connected to a resistor divider from the auxiliary winding to ground. The output-voltage feedback information is sampled at the end of the transformer secondary current demagnetization time to provide an accurate representation of the output voltage. Timing information to achieve valley-switching and to control the duty cycle of the secondary transformer current is determined by the waveform on the VS pin. Do not place a filter capacitor on this input, which would interfere with accurate sensing of this waveform. The values for the auxiliary voltage divider upper-resistor R_{S1} and lower-resistor R_{S2} can be determined by Equation 13 and Equation 14:

$$R_{S1} = \frac{V_{IN(run)}}{N_{PA} \times I_{VSL(run)}} \quad (13)$$

where

- N_{PA}: Transformer primary-to-auxiliary turns ratio
- $V_{IN(run)}$: Converter input start-up (run) voltage
- $I_{VSL(run)}$: The run-threshold for the current pulled out of the VS pin during the MOSFET on-time (equal to 260 uA, maximum from UCC28701 datasheet)

If N_{PS} = 0.9 and N_{AS} = 0.5, then N_{PA} = 1.8. The controller starts working at $V_{IN(run)}$ = 21 V. With these values, the calculated value of R_{S1} is 44.8 kΩ.

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSR}} \quad (14)$$

where

- V_{OCV}: regulated output voltage of the converter
- V_F: secondary rectifier forward voltage drop at near-zero current
- N_{AS}: transformer auxiliary-to-secondary turns ratio
- R_{S1}: the VS divider high-side resistance
- V_{VSR}: CV regulating level at the VS input (equal to 4.05 V, typical from UCC28701 datasheet)

With R_{S1} = 44.8 kΩ, the calculated value of R_{S2} is 21.09 kΩ.

4.2.5 MOSFET Gate Drive and Current Sensing

The DRV pin of UCC28701 is connected to the MOSFET gate pin, usually through a series resistor. The gate driver provides a gate drive signal limited to 14 V. The turn-on characteristic of the driver is a 25-mA current source, which limits the turn-on dv/dt of the MOSFET drain and reduces the leading-edge current spike but still provides the gate drive current to overcome the Miller plateau. The gate drive turn-off current is determined by the low-side driver $R_{DS(on)}$ and any external gate drive resistance. The current-sense (CS) pin is connected through a series resistor (R_{LC}) to the current-sense resistor (R_{CS}). The CS threshold is 0.75 V for $I_{PP(max)}$ and 0.25 V for $I_{PP(min)}$. The series resistor R_{LC} provides the function of feed-forward line compensation to eliminate change in I_{PP} due to change in di/dt and the propagation delay of the internal comparator and MOSFET turn-off time. There is an internal leading-edge blanking time of 235 ns to eliminate sensitivity to the MOSFET turn-on current spike. The value of R_{CS} is determined by the target output current in CC regulation. The values of R_{CS} and R_{LC} can be determined by Equation 5 and Equation 15:

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times T_D \times N_{PA}}{L_P} \quad (15)$$

where

- R_{LC}: Line compensation resistor
- R_{S1}: VS pin high-side resistor value
- R_{CS}: CS resistor value
- T_D: CS delay including MOSFET turn-off delay; add 50 ns to MOSFET delay
- N_{PA}: Transformer primary-to-auxiliary turns ratio
- L_P: Transformer primary inductance
- K_{LC}: Current-scaling constant (equal to 25 A/A, from datasheet of UCC28701)

The calculated value for RLC is 1.68 kΩ.

Figure 6 shows the section of schematic with MOSFET gate drive and current sense circuit.

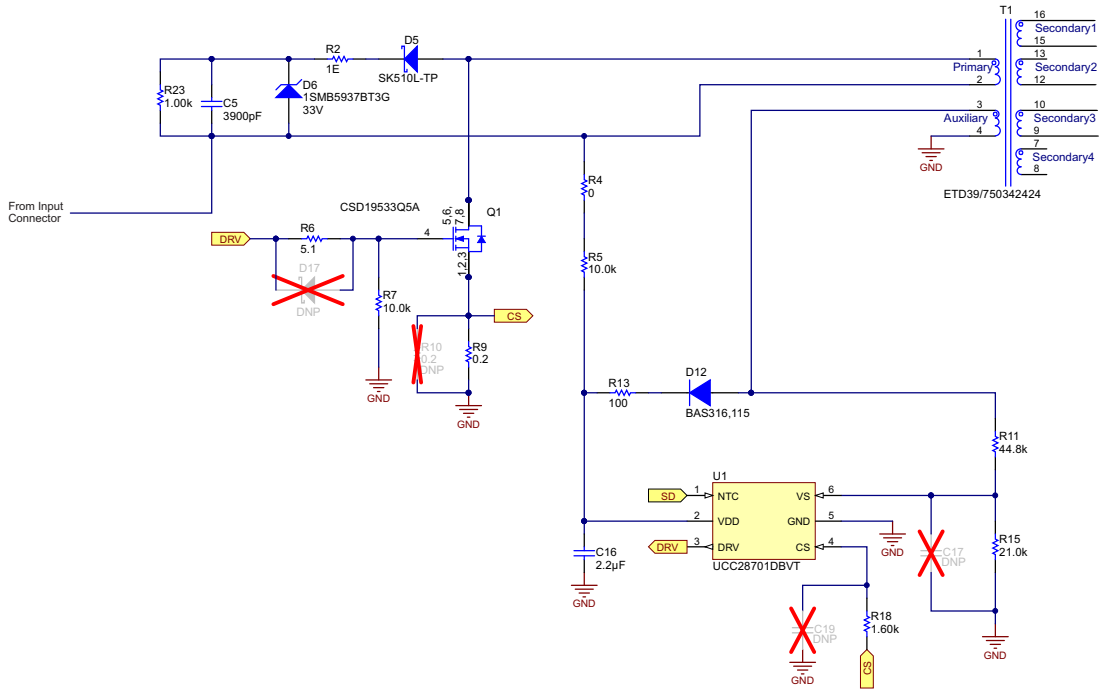


Figure 6. MOSFET Gate Drive and Current Sense Circuit

Table 1 shows the mapping of the component designators (in Section 4.2.2 to Section 4.2.5) with the component designators and values used in the schematic design.

Table 1. Calculated and Schematic Component Mapping

DESIGN DESIGNATOR	CALCULATED VALUE	SCHEMATIC DESIGNATOR	SCHEMATIC VALUE
R_{CS}	0.2 Ω	R9	0.2 Ω
R_{S1}	44.8 kΩ	R11	44.8 kΩ
R_{S2}	21.09 kΩ	R15	21 kΩ
R_{LC}	1.68 kΩ	R18	1.6 kΩ

4.2.6 Shutdown Operation of PWM Controller

The UCC28701 has an NTC pin that can be used for an external NTC thermistor to allow a user-programmable external thermal shutdown. The shutdown threshold is 0.95 V with an internal 105-µA current source, which results in a 9.05-kΩ thermistor shutdown threshold. This reference design uses this pin for a shutdown operation of the PWM controller to facilitate STO feature. The STO function is the most common and basic drive-integrated safety function. The STO features ensure that no torque-generating energy can continue to act upon a motor and prevent unintentional starting. As shown in Figure 7, a BJT (Q2) is used as a switch to facilitate the STO feature in this reference design. Once an active-high shutdown signal is given on CONN2, the BJT (Q2) turns on and pulls the NTC pin of UCC28701 low, which ultimately stops the switching of UCC28701. The STO functionality is shown tested and the waveforms are shown in Figure 11.

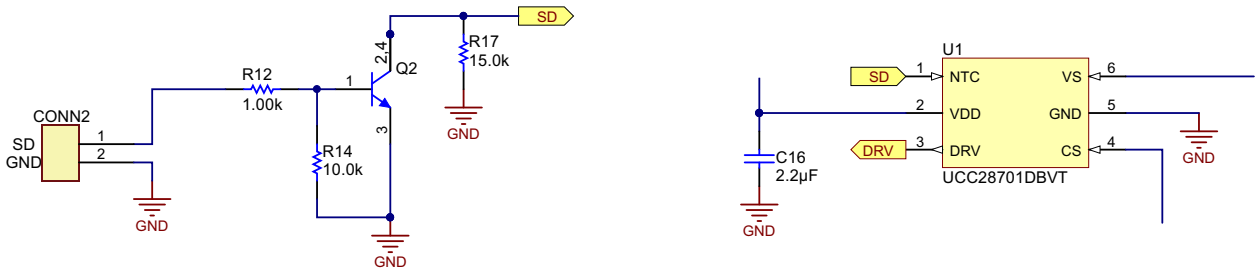


Figure 7. Shutdown Mechanism

4.2.7 Positive and Negative Outputs for Gate Driver

Each secondary outputs of the transformer is rectified and given to zener regulators. In Figure 8, LEDs on each output indicate the availability of the output. The positive (16 V) and negative (–8.2 V) outputs are generated using two zener diodes on each output followed by bulk capacitors for the large current ripples (as explained in Section 5.5).

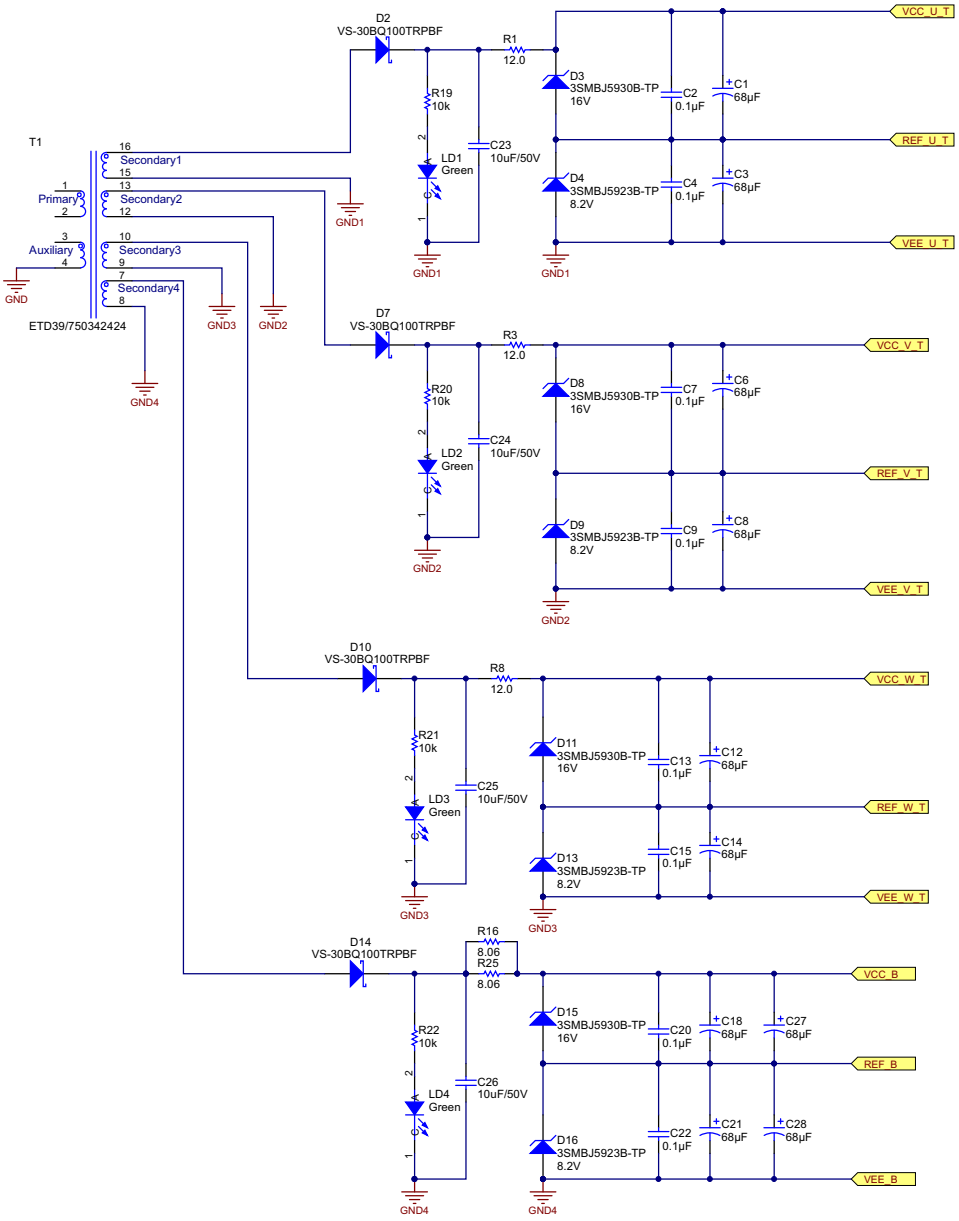


Figure 8. Positive and Negative Outputs on Each Secondary

4.2.8 Single Transformer for Powering All Three IGBT Arms

The selected flyback topology uses only one transformer to power all three arms (U, V, and W) of the three-phase inverter. The outputs are as shown in Table 2:

Table 2. Outputs for Top and Bottom IGBTs (for All Three Arms)

PHASE	FOR TOP IGBT	FOR BOTTOM IGBT
U	VCC_U_T	VCC_B
	VEE_U_T	VEE_B
	REF_U_T	REF_B
V	VCC_V_T	VCC_B
	VEE_V_T	VEE_B
	REF_V_T	REF_B
W	VCC_W_T	VCC_B
	VEE_W_T	VEE_B
	REF_W_T	REF_B

4.2.9 Scalability Option for Higher Power Industrial Drives

This design is intended to be used with IGBT modules with ratings of 1200 V/200 A. If higher power IGBT modules are to be powered, the same reference design can scale up to a higher power by changing the transformer design. The existing transformers have secondary output current ratings of 150 mA each. This rating can be increased to meet the requirement for higher power Industrial drives.

5 Test Setup and Test Results

5.1 Functional Test Results for UCC28701

Figure 9 and Figure 10 show the Gate drive signal, MOSFET Drain voltage and voltage across resistor R_{CS} under no-load condition as well as full-load condition respectively.

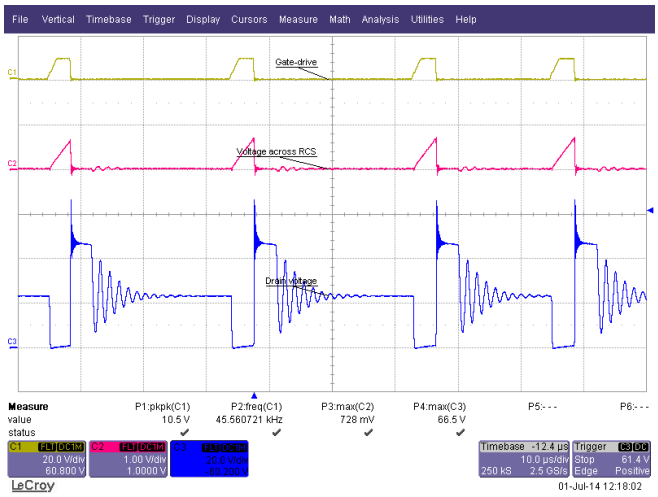


Figure 9. Gate Drive Signal, MOSFET Drain Voltage, and Voltage Across RCS (for No Load Condition)

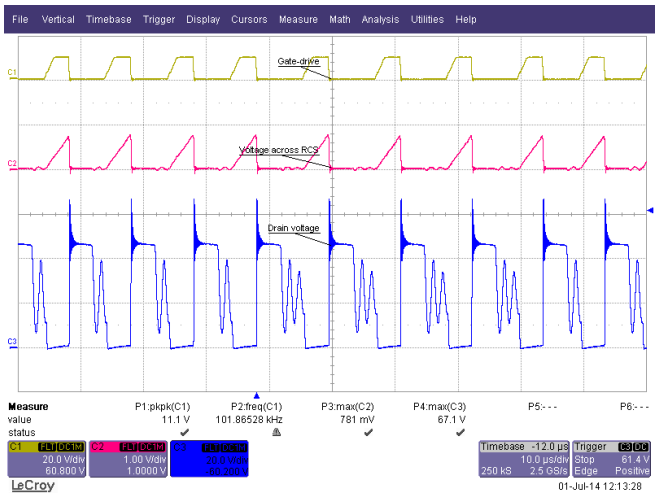


Figure 10. Gate Drive Signal, MOSFET Drain Voltage, and Voltage Across RCS (for Full Load Condition)

A BJT is used as a switch to facilitate the STO feature in this reference design. UCC28701's NTC pin can be used for achieving this functionality. The same has been tested and the waveform in Figure 11 shows the shutdown signal along with the outputs going to zero.

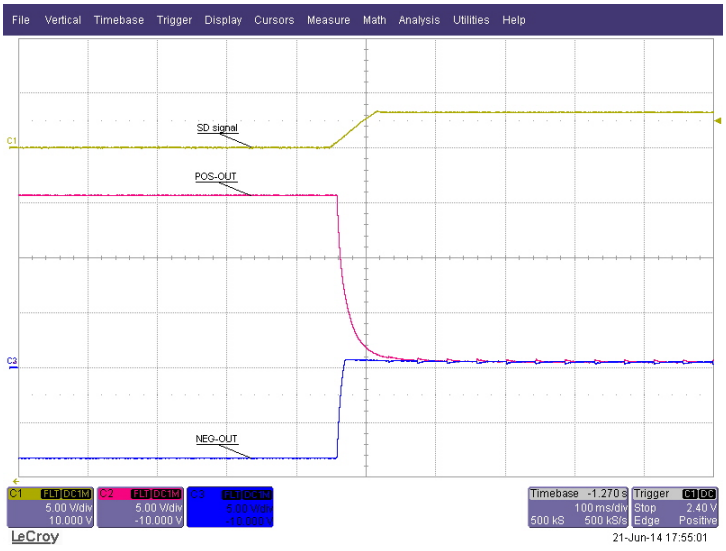


Figure 11. Shutting Down UCC28701 Using External Signals

5.2 Output Ripple Measurement

With all the outputs loaded with 2 W of output power, the ripple at the 16-V output and –8.2-V outputs are captured. On the 16-V output and –8.2-V output, the peak-to-peak ripple voltages are 23 mV and 22.4 mV, respectively. Figure 12 and Figure 13 show the waveforms for the same.

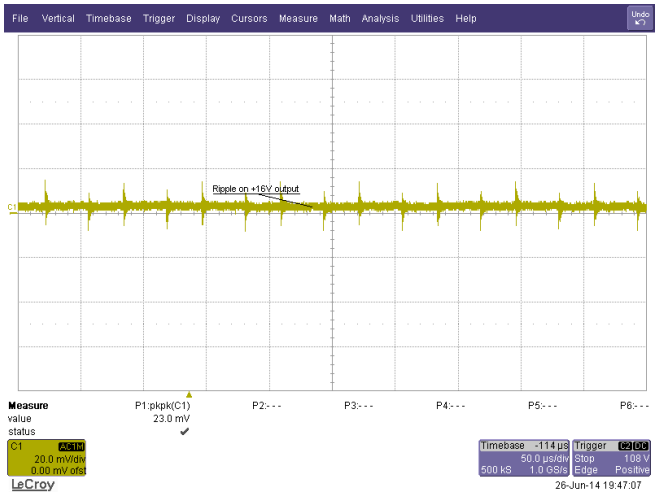


Figure 12. Ripple Voltage on 16-V Output (at Full Load)

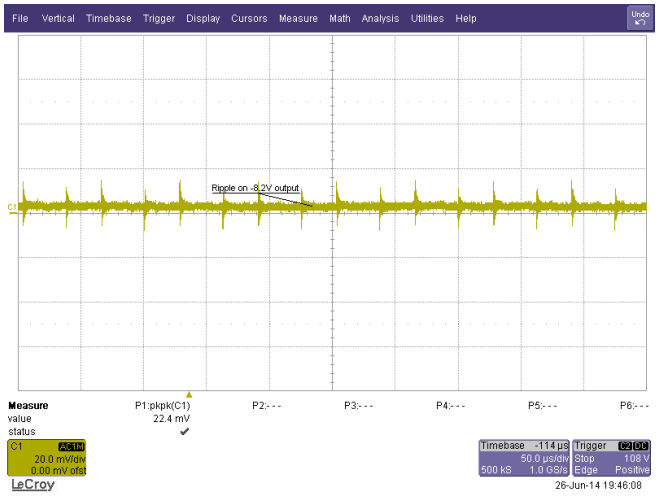


Figure 13. Ripple Voltage on –8.2-V Output (at Full Load)

5.3 Efficiency and Output Voltage Regulation

The efficiency is measured with all the outputs loaded with equal loads. When all the outputs were loaded with a 2-W load each, the efficiency is around 76% as shown in Figure 14:

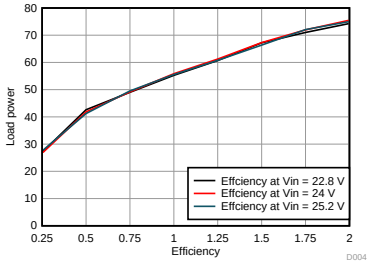


Figure 14. Efficiency at Different Vin Values

The regulation data is captured at different Vin values as shown in Figure 15 through Figure 17. While measuring the regulation, the VCC and VEE for bottom IGBTs are loaded with three times the load of each VCC and VEE for top IGBTs. For example, if the VCC and VEE for top IGBTs are loaded with 0.25 W each, then the VCC and VEE for bottom IGBTs are loaded with 0.75 W.

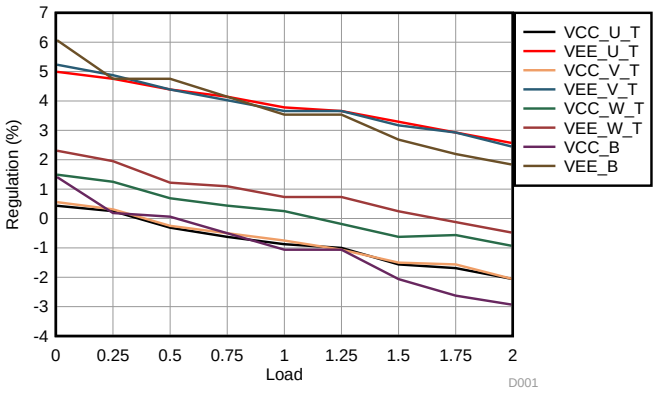


Figure 15. Output Voltage Regulation at Vin = 22.8 V

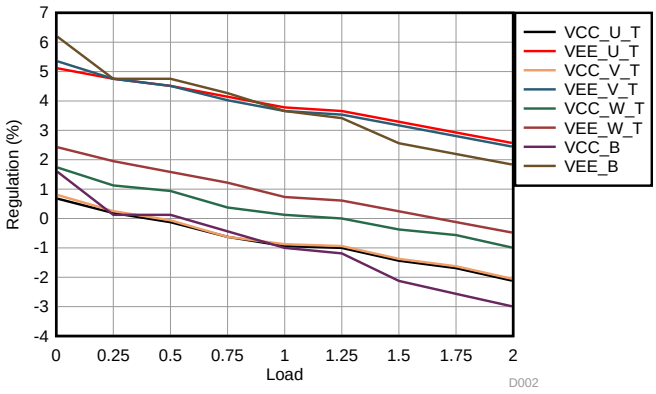


Figure 16. Output Voltage Regulation at Vin = 24 V

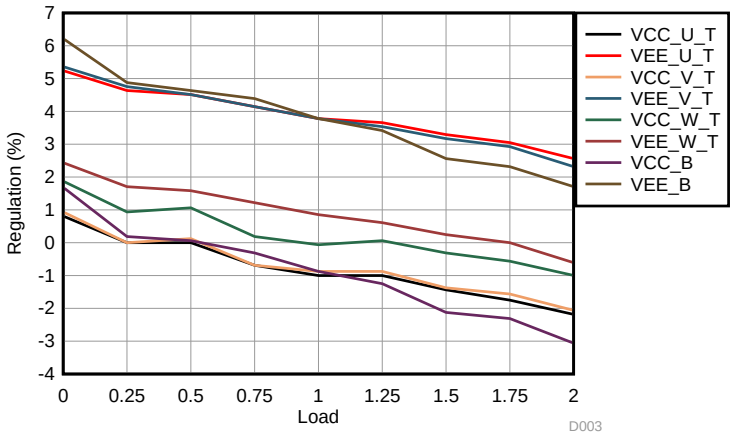


Figure 17. Output Voltage Regulation at Vin = 25.2 V

5.4 Isolation Test Results

The design is tested for and successfully passes the 7-kV impulse test (for 1.2/50 us pulse). The design also passes the type-test isolation voltage tests as per the design specifications.

5.5 Testing with ISO5500 and IGBTs

To duplicate the actual drive testing, this reference design is tested with TI's ISO5500 EVMs along with 1200-V IGBTs. Two 16-kHz complementary PWM signals for IGBT gate driving are generated using Piccolo™ LaunchPAD™ from TI. The signals are fed to two ISO5500 (each connected to one 1200-V IGBT). The IGBTs are connected in half-bridge form as shown in Figure 18 with 1-kΩ load connected at the output. The image of the setup with all boards is also shown in Figure 19.

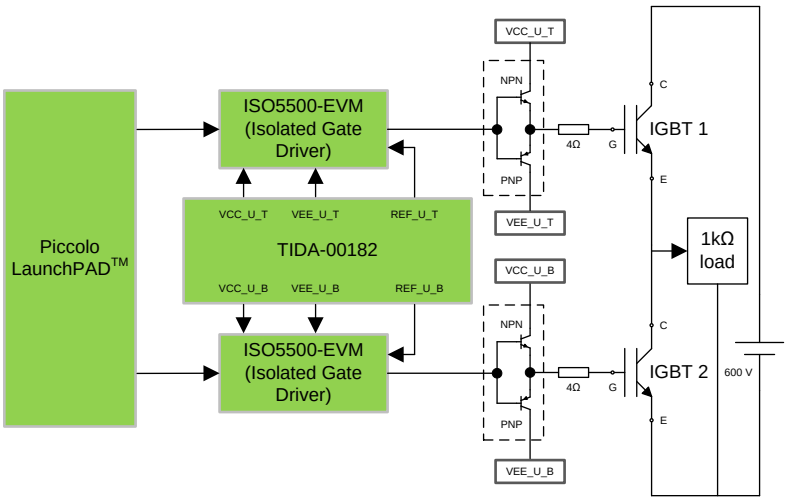


Figure 18. Setup for Testing TIDA-00182 Design With TI's ISO5500 and IGBTs

Figure 19. Image of the Setup

With 600 V applied to the IGBT arm, and both the ISO5500s applied with power supply from TIDA-00182, the ripple is measured. Figure 20 and Figure 21 show the output ripple voltage waveforms that meet the specification of the reference design.

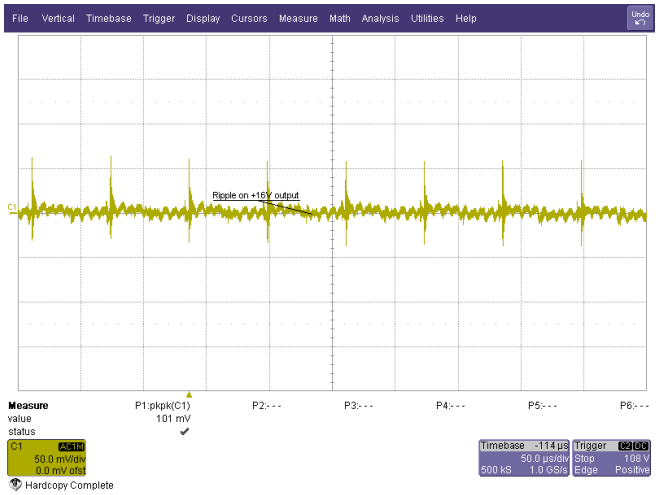


Figure 20. Ripple on 16-V Output (for dv/dt = 11.4*E9 on the Output Load)

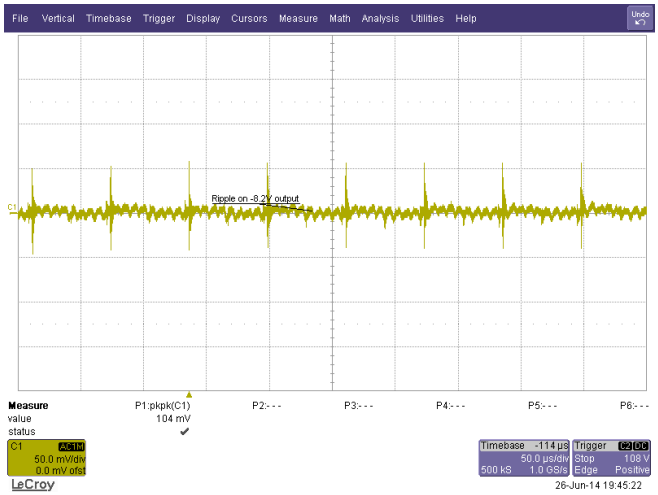


Figure 21. Ripple on –8.2-V Output (for dv/dt = 11.4*E9 on the Output Load)

The current boost transistors (NPN and PNP) are used to boost the output current of the ISO5500 to drive the IGBTs. With a 6-A peak current while charging the internal capacitance of IGBTs, the ripple on the VCC and VEE outputs of power supply are also measured (see Figure 22 and Figure 23 show the same.

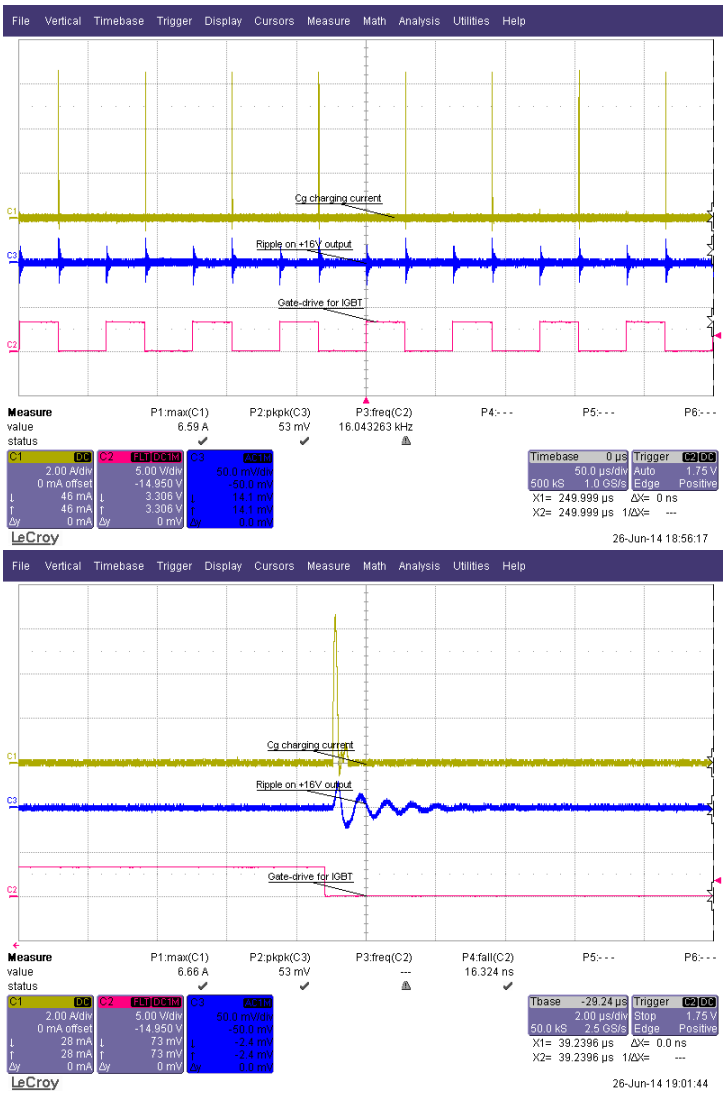


Figure 22. (Top) Ripple on 16-V Output for 6-A Peak Load Current with IGBTs (Bottom) Zoomed Waveforms

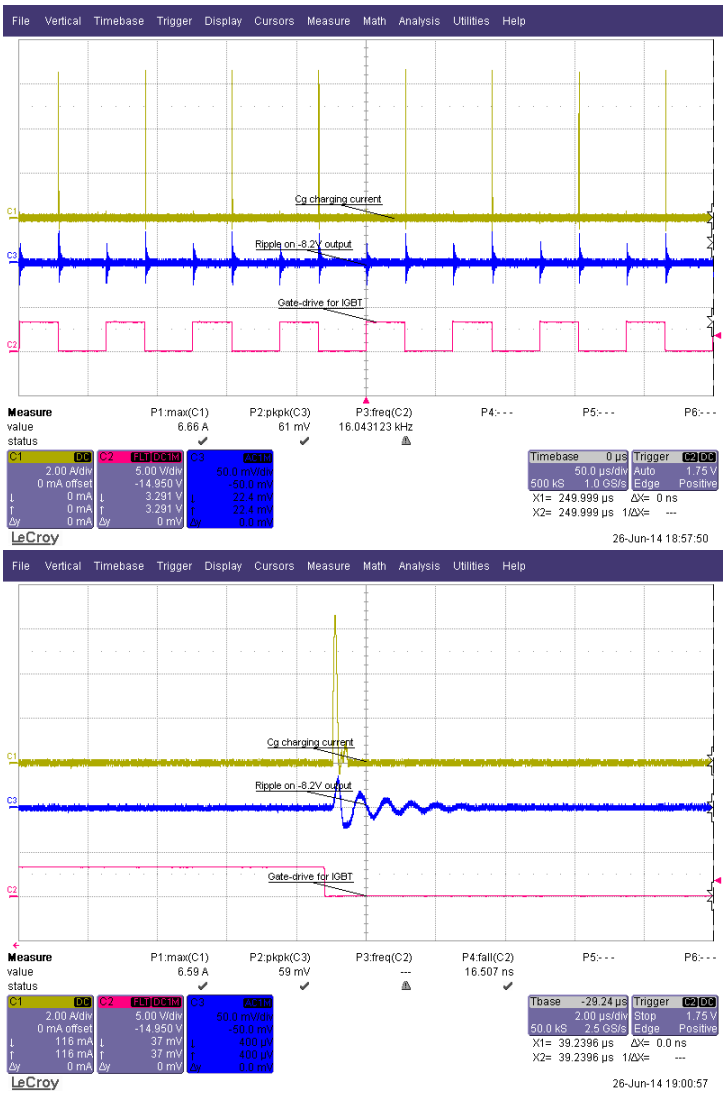


Figure 23. (Top) Ripple on –8.2-V Output for 6-A Peak Load Current with IGBTs (Bottom) Zoomed Waveforms

5.6 Temperature Measurement

The temperature of the power MOSFET (Q1) is about 60°C at room temperature. The thermal resistance from case to ambient can be improved further by having more copper and connecting to the plane. Also explore other packages that lessens thermal resistance from junction to ambient.

6 Design Files

6.1 Schematics

To download the schematics, see the design files at TIDA-00182.

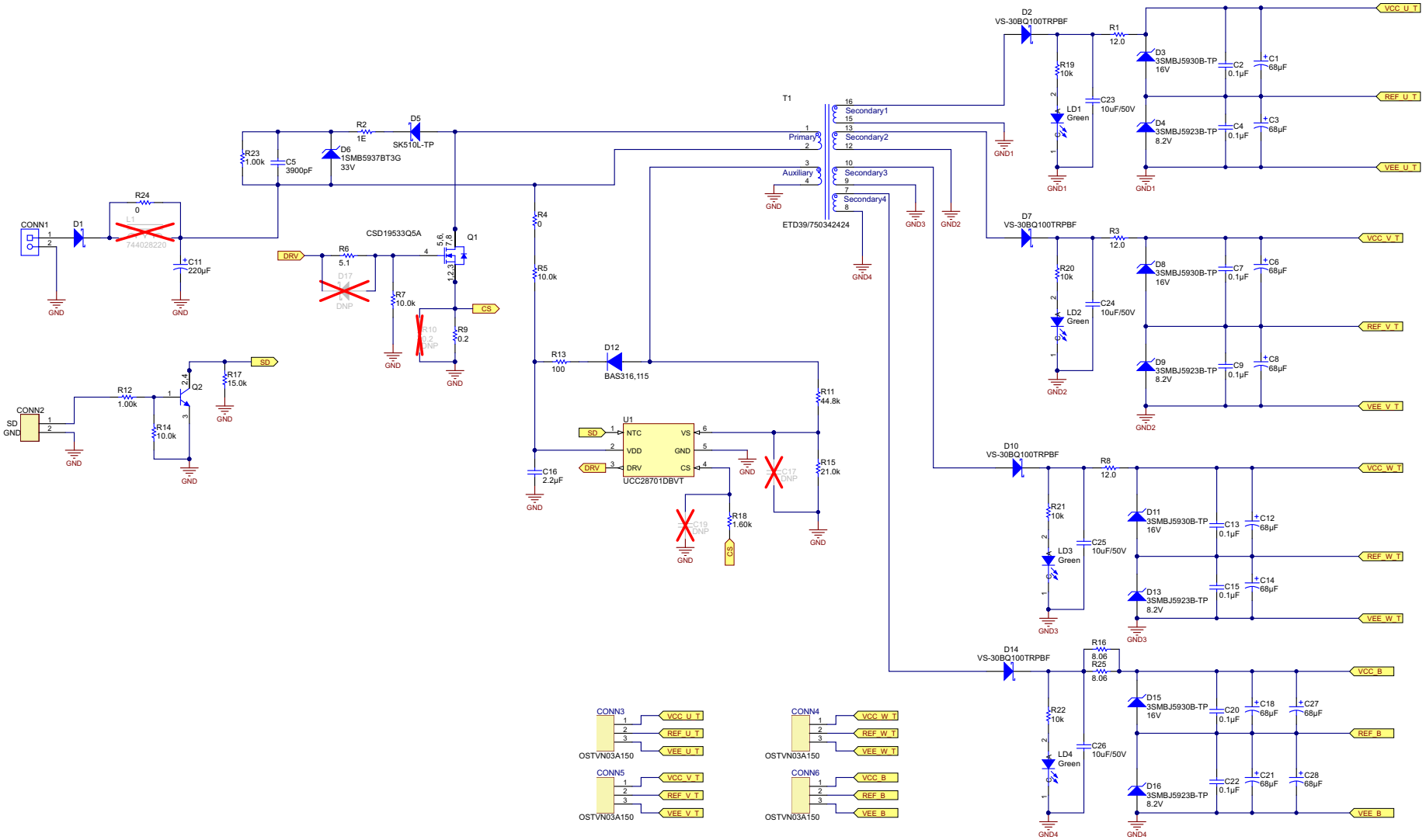


Figure 24. Main Schematic

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00182.

Table 3. BOM

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER PARTNUMBER	MANUFACTURER	PCB FOOTPRINT
1	1	C11	CAP, AL, 220 µF, 35 V, ±20%, 0.16 Ω, SMD	EEE-FK1V221P	Panasonic	SMT Radial F
2	1	C16	CAP, CERM, 2.2 µF, 50 V, ±10%, X5R, 0805	C2012X5R1H225K125AB	TDK	0805
3	1	C5	CAP, CERM, 3900 pF, 100 V, ±10%, X7R, 0805	GRM219R72A392KA01D	MuRata	0805
4	1	CONN1	Terminal Block, 2×1, 5.08 mm, TH	282841-2	TE Connectivity	10.16 × 15.2 × 9 mm
5	1	CONN2	Terminal Block, 4×1, 2.54 mm, TH	OSTVN02A150	On Shore Technology Inc	TERM_BLK, 2pos, 2.54 mm
6	1	D1	Diode, Schottky, 60 V, 2 A, SMA	B260A-13-F	Diodes Inc.	SMA
7	1	D12	Diode, Ultrafast, 100 V, 0.25 A, SOD-323	BAS316,115	NXP Semiconductor	SOD-323
8	1	D5	Diode Schottky 100 V, 5 A, DO214AB	SK510L-TP	Micro Commercial Co	DO-214AB, (SMC)
9	1	D6	Diode, Zener, 33 V, 550 mW, SMB	1SMB5937BT3G	ON Semiconductor	SMB
10	1	LBL1	Thermal Transfer Printable Labels, 0.650" W × 0.200" H - 10,000 per roll	THT-14-423-10	Brady	PCB Label 0.650"H × 0.200"W
11	1	Q1	MOSFET, N-CH, 100 V, 13 A, SON 5×6 mm	CSD19533Q5A	Texas Instruments	SON 5 × 6 mm
12	1	Q2	Transistor, NPN, 32 V, 1 A, SOT-89	2DD1664R-13	Diodes Inc.	SOT-89
13	1	R11	RES, 44.8 kΩ, 0.1%, 0.125 W, 0805	RT0805BRD0744K8L	Yageo America	0805
14	1	R12	RES, 1.00 kΩ, 1%, 0.125 W, 0805	CRCW08051K00FKEA	Vishay-Dale	0805
15	1	R13	RES, 100 Ω, 1%, 0.125W, 0805	CRCW0805100RFKEA	Vishay-Dale	0805
16	1	R15	RES, 21.0 kΩ, 1%, 0.125 W, 0805	CRCW080521K0FKEA	Vishay-Dale	0805
17	1	R17	RES, 15.0 kΩ, 0.1%, 0.125 W, 0805	RG2012P-153-B-T5	Susumu Co Ltd	0805
18	1	R18	RES, 1.60 kΩ, 0.5%, 0.1 W, 0805	RR1220P-162-D	Susumu Co Ltd	0805
19	1	R2	RES, 1.00 Ω, 1%, 0.25 W, 1206	CRCW12061K00FKEA	Vishay-Dale	1206
20	1	R23	RES, 1.00 kΩ, 1%, 0.25 W, 1206	RC1206FR-071KL	Yageo America	1206
21	1	R5	RES, 10.0 kΩ, 1%, 0.25 W, 1206	ERJ-8ENF1002V	Panasonic	1206
22	1	R6	RES, 5.1 Ω, 5%, 0.125 W, 0805	CRCW08055R10JNEA	Vishay-Dale	0805
23	1	R9	RES, 0.2 Ω, 1%, 0.5 W, 1206	CSR1206FKR200	Stackpole Electronics Inc	1206
24	1	T1	Transformer, TH	ETD39/750342424	Würth Elektronik	
25	1	U1	IC, Constant Voltage, Constant Current PWM with Primary Side Regulation	UCC28701DBVT	Texas Instruments	SOT-23-6
26	10	C1, C3, C6, C8, C12, C14, C18, C21, C27, C28	CAP ALUM 68 µF 35 V 20% SMD	EEH-ZA1V680XP	Panasonic Electronic Components	6.60 × 6.60 mm
27	2	R16, R25	RES, 8.06 Ω, 1%, 0.25 W, 1206	CRCW12068R06FKEA	Vishay-Dale	1206

Table 3. BOM (continued)

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER PARTNUMBER	MANUFACTURER	PCB FOOTPRINT
28	2	R4, R24	RES, 0 Ω, 5%, 0.25 W, 1206	RC1206JR-070RL	Yageo America	1206
29	2	R7, R14	RES, 10.0 kΩ, 0.1%, 0.125 W, 0805	RG2012P-103-B-T5	Susumu Co Ltd	0805
30	3	R1, R3, R8	RES, 12.0 Ω, 1%, 0.25 W, 1206	RC1206FR-0712RL	NXP Semiconductor	SOD-323
31	1	D6	Diode, Zener, 33 V, 550 mW, SMB	1SMB5937BT3G	ON Semiconductor	SMB
32	1	D5	Diode Schottky 100 V, 5 A, DO214AB	SK510L-TP	Micro Commercial Co	DO-214AB, (SMC)
33	4	D4, D9, D13, D16	Diode Zener 8.2 V, 3 W, DO214AA	3SMBJ5923B-TP	Micro Commercial Co	DO214AA/SMB
34	4	D3, D8, D11, D15	Diode Zener 16 V, 3 W DO214AA	3SMBJ5930B-TP	Micro Commercial Co	DO214AA/SMB
35	4	D2, D7, D10, D14	Diode, Schottky, 100V, 3A, SMC	VS-30BQ100TRPBF	Vishay-Semiconductor	SMC
36	1	D1	Diode, Schottky, 60 V, 2 A, SMA	B260A-13-F	Diodes Inc.	SMA
37	4	CONN3, CONN4, CONN5, CONN6	CONN Term Block 2.54-mm 3POS PCB	OSTVN03A150	On Shore Technology Inc	TERM_BLK, 3pos, 2.54 mm
38	1	CONN2	Terminal Block, 4×1, 2.54 mm, TH	OSTVN02A150	On Shore Technology Inc	TERM_BLK, 2pos, 2.54 mm
39	1	CONN1	Terminal Block, 2×1, 5.08 mm, TH	282841-2	TE Connectivity	10.16 × 15.2 × 9 mm
40	4	C23, C24, C25, C26	CAP, CERM, 10 µF, 50 V, ±10%, X5R, 1206_190	CGA5L3X5R1H106K160AB	TDK	1206_190
41	0	C19	CAP, CERM, 1000 pF, 50 V, ±10%, X7R, 0805	C2012X7R1H102K	TDK	0805
42	0	C17	CAP, CERM, 0.33 µF, 25 V, ±10%, X5R, 0805	08053D334KAT2A	AVX	0805
43	1	C16	CAP, CERM, 2.2 µF, 50 V, ±10%, X5R, 0805	C2012X5R1H225K125AB	TDK	0805
44	1	C5	CAP, CERM, 3900 pF, 100 V, ±10%, X7R, 0805	GRM219R72A392KA01D	MuRata	0805
45	8	C2, C4, C7, C9, C13, C15, C20, C22	CAP, CERM, 0.1 µF, 50 V, ±5%, X7R, 0805	08055C104JAT2A	AVX	0805
46	10	C1, C3, C6, C8, C12, C14, C18, C21, C27, C28	CAP ALUM 68 µF, 35 V, 20% SMD	EEH-ZA1V680XP	Panasonic Electronic Components	6.60 × 6.60mm

6.3 Layer Plots

To download the layer plots, see the design files at TIDA-00182.

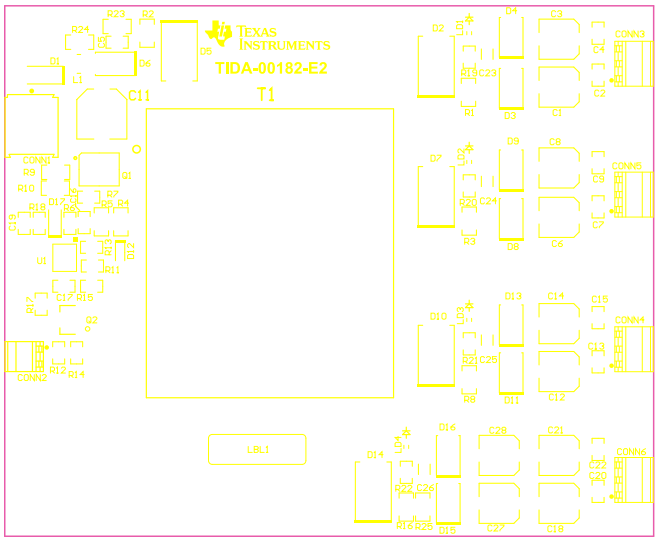


Figure 25. Top Overlay

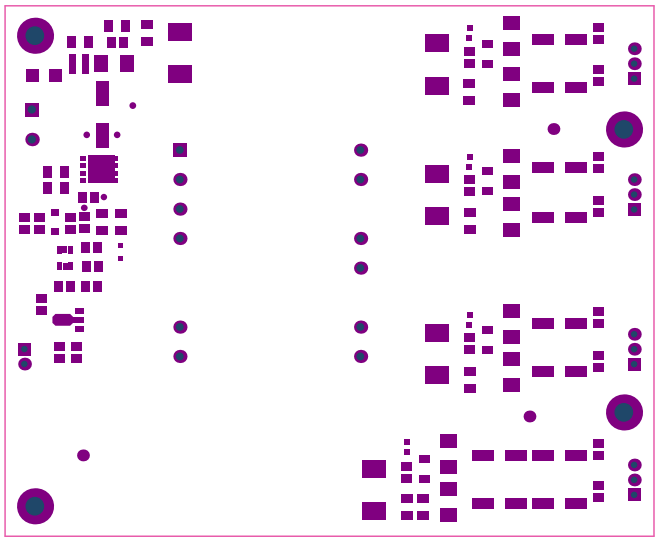


Figure 26. Top Solder Mask

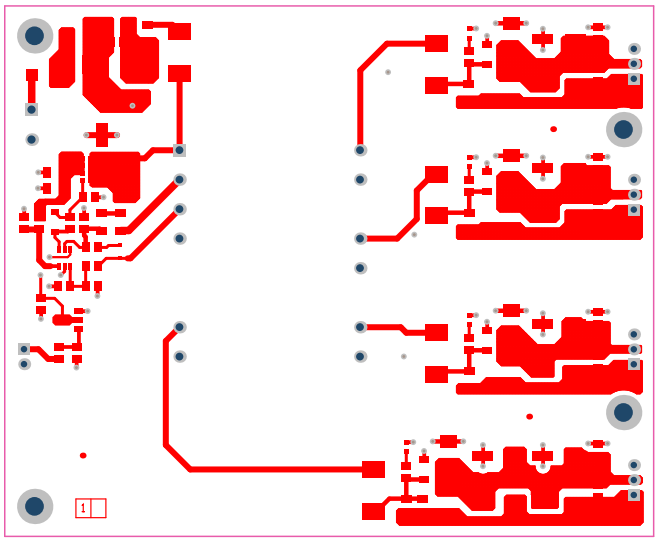


Figure 27. Top Layer

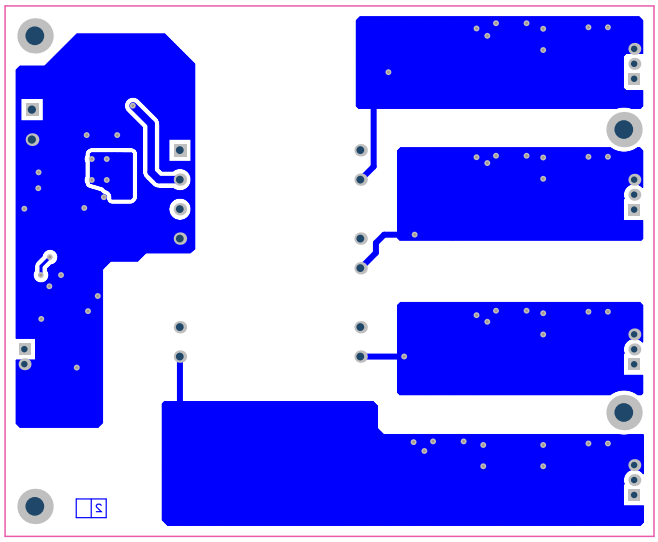


Figure 28. Bottom Layer

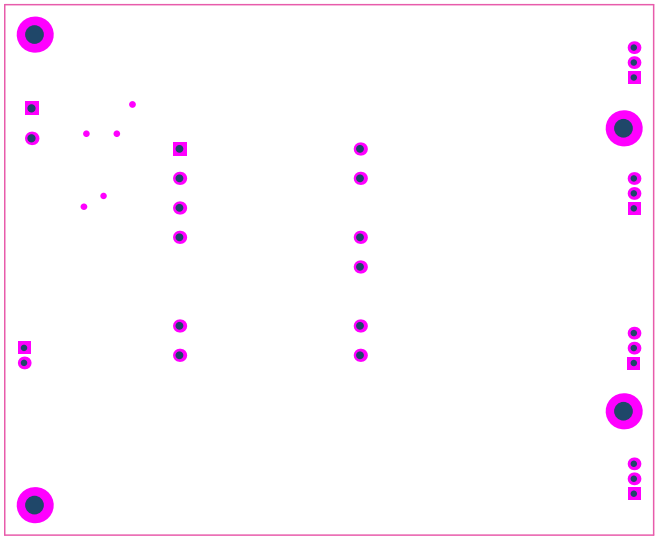


Figure 29. Bottom Solder Mask

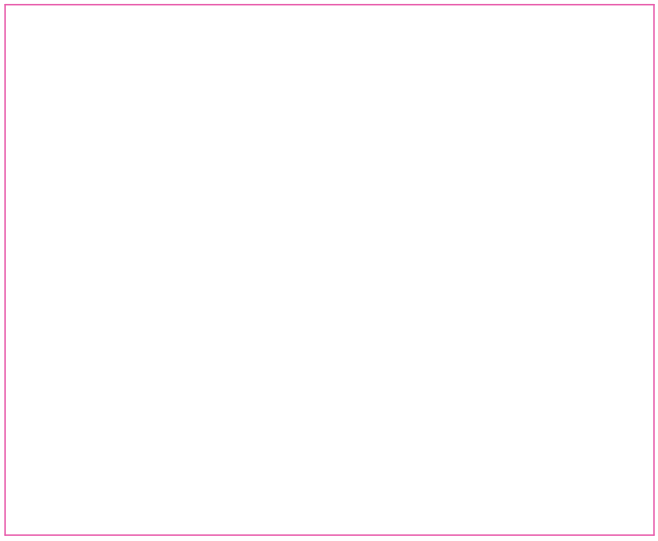
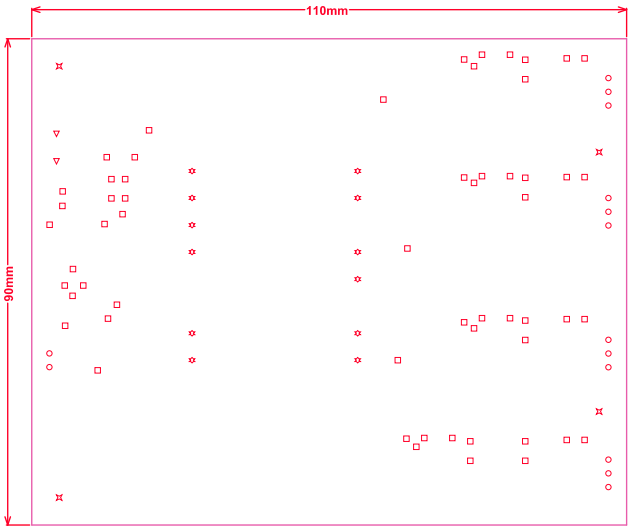


Figure 30. Bottom Overlay



Symbol	Hit Count	Tool Size	Plated	Hole Type
□	57	20mil (0.508mm)	PTH	Round
○	14	44mil (1.118mm)	PTH	Round
✡	12	53mil (1.346mm)	PTH	Round
▽	2	55.118mil (1.4mm)	PTH	Round
⌑	4	125.984mil (3.2mm)	PTH	Round
	89 Total			

Drill Table
DRILL TOLERANCE
FOR PTH +/- 3MIL

Figure 31. Drill Drawing

6.4 Altium Project

To download the Altium project files, see the design files at TIDA-00182.

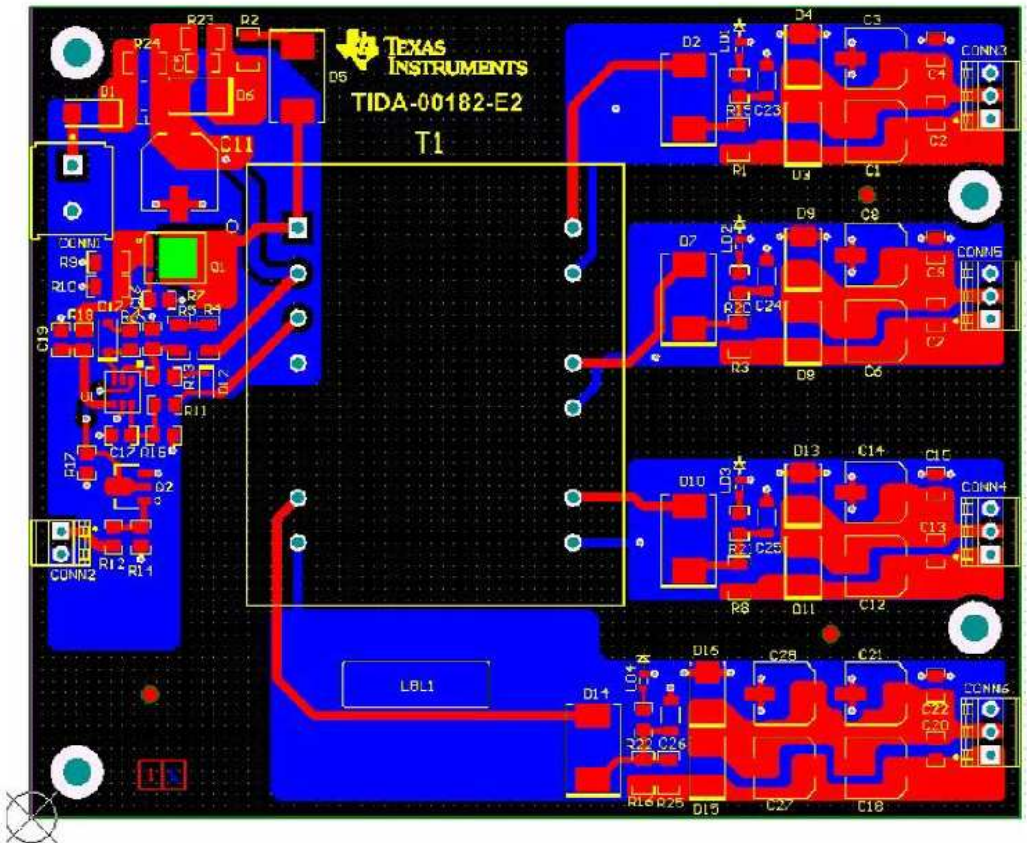


Figure 32. All Layers

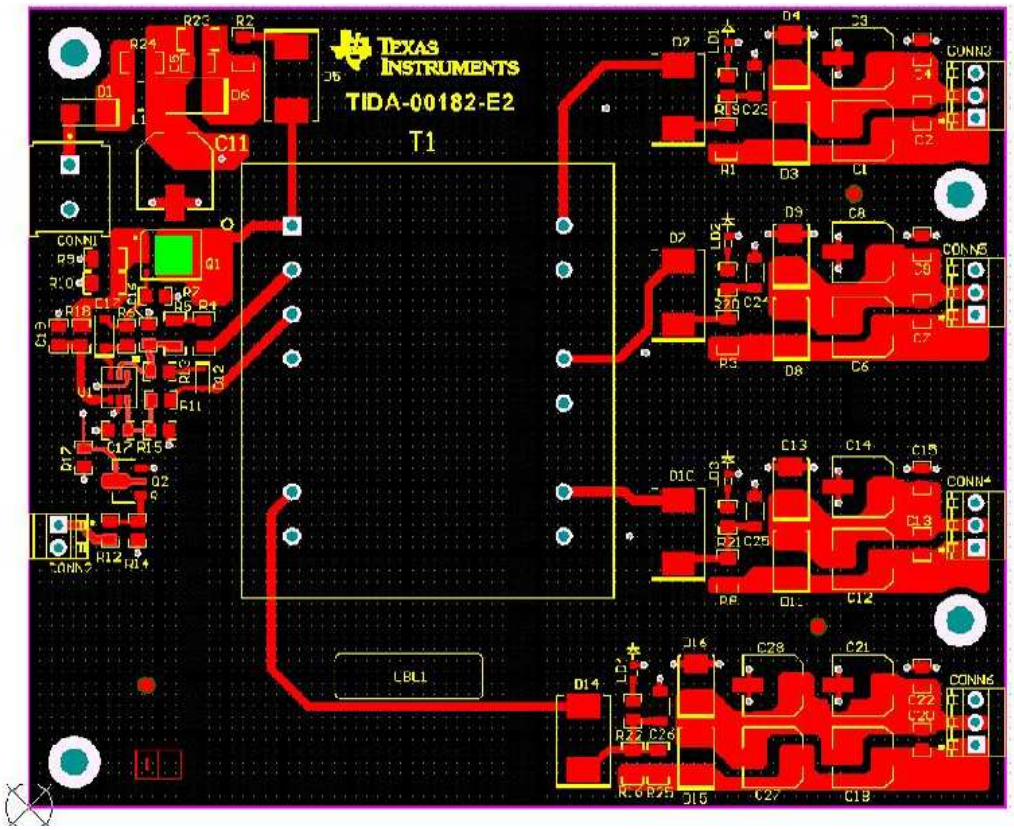


Figure 33. Top Layer

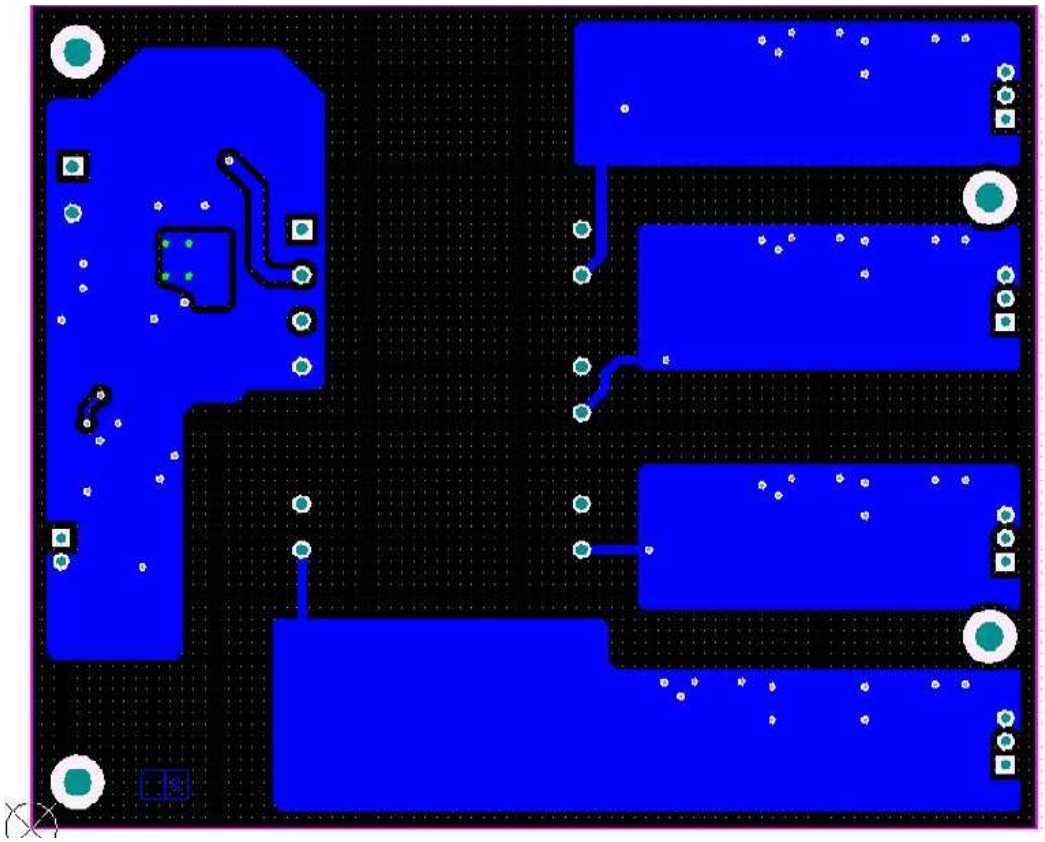


Figure 34. Bottom Layer

6.5 Layout Guidelines

The VDD pin is connected to a bypass capacitor to ground and a start-up resistance to the input bulk capacitor (+) terminal. The GND pin (Pin 5) is a single ground reference external to the device for the gate drive current and analog signal reference. Place the VDD bypass capacitor close to GND and VDD with short traces to minimize noise on the VS and CS signal pins.

The VS pin is connected to a resistor divider from the auxiliary winding to ground. Information on the output voltage feedback is sampled at the end of the transformer secondary current demagnetization to accurately represent the output voltage. Timing information to achieve valley-switching and to control the duty cycle of the secondary transformer current is determined by the waveform on the VS pin. Avoid placing a filter capacitor on this input, which would interfere with accurately sensing this waveform.

The CS pin is connected through a series resistor (R_{LC}) to the CS resistor (R_{CS}). The CS threshold is 0.75 V for $I_{PP(max)}$ and 0.25 V for $I_{PP(min)}$. R_{LC} provides the function of feed-forward line compensation to eliminate change in I_{PP} due to a change in di/dt and the propagation delay of the internal comparator and MOSFET turn-off time. There is an internal leading-edge blanking time of 235 ns to eliminate sensitivity to the MOSFET turn-on current spike. A bypass capacitor on the CS pin is not necessary. The value of R_{CS} is determined by the target output current in CC regulation.

6.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00182.

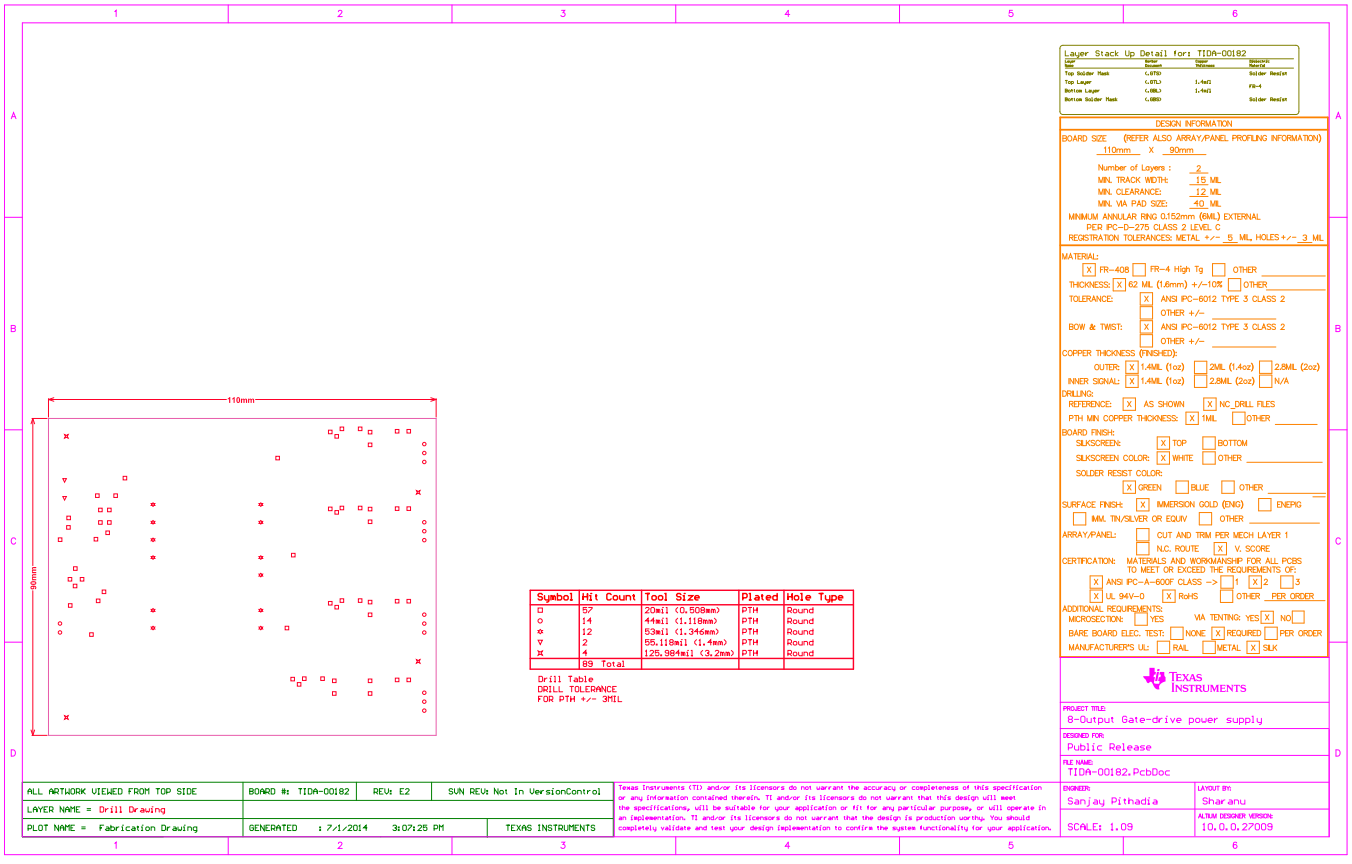


Figure 35. FAB Drawing

6.7 Assembly Drawings

To download the assembly files, see the design files at TIDA-00182.

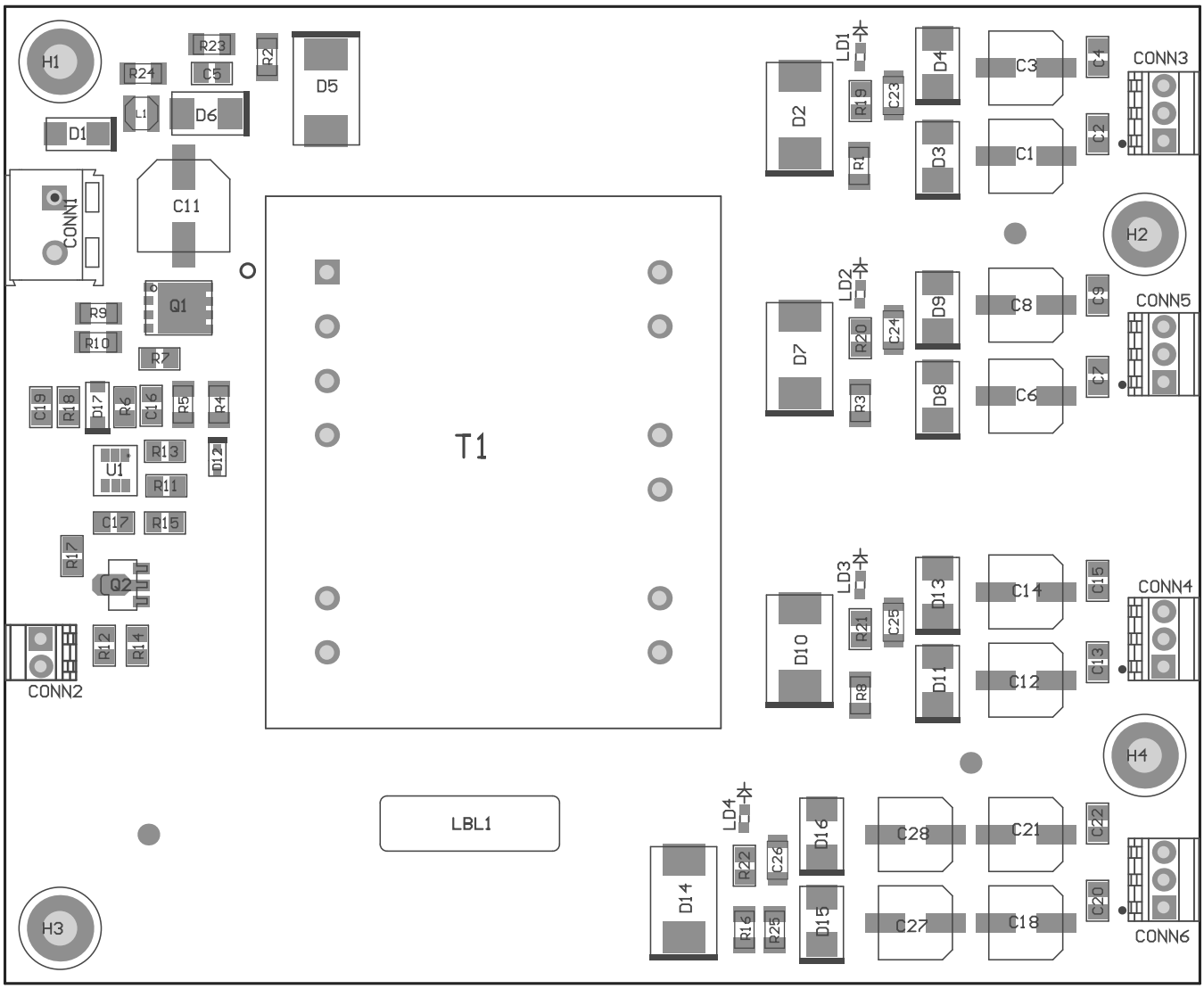


Figure 36. Assembly Drawing

7 References

1. Power Tip #6: Accurately Measuring Power Supply Ripple (Link)
2. UCC28700 EVAL board (SLUU968)
3. ISO5500EVM User's Guide (SLLU136A)
4. C2000 Piccolo LaunchPAD (Folder)

8 About the Author

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