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Cynthia Sosa

TI Designs
Adding an LDO for Increased Standby Mode Efficiency

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Circuit Description

This regulation topology is designed to increase the efficiency of a DC/DC buck converter by disabling the converter during light-load operation and providing a regulated output voltage with a low-Iq LDO. During no-load or light-load conditions, the LDO allows for low-noise, low-Iq output voltage regulation while the DC/DC is disabled. Once the load is engaged, the DC/DC converter can provide high efficiency at high load currents, thereby combining the benefits of both devices.

Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
TPS54331	Product Folder
TPS709	Product Folder

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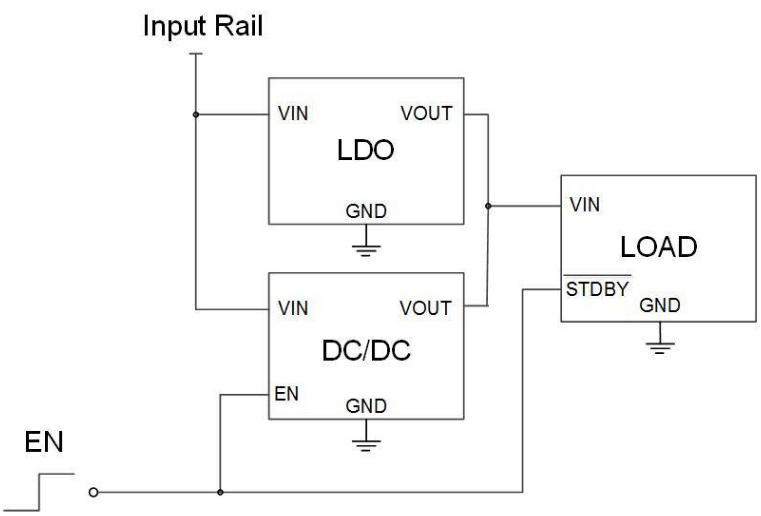

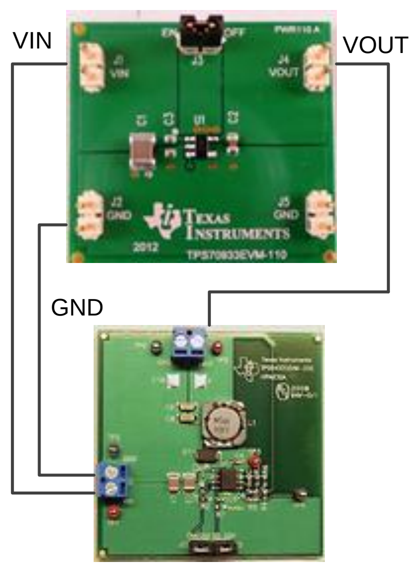

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1 Design Summary

The design requirements are as follows:

- Input Voltage: 12 V ± 10 %
- Output Voltage: 3.3V ± 10 %
- Current Consumption during Standby Mode: < 15 µA
- Conversion Efficiency at 3 A: > 80%
- Delay required from Standby to Full Load Output Regulation: < 5 msec

Table1. Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Simulated	Measured
Standby Mode Current	<15 uA	<1 mA	<15 uA
Efficiency @ 3 A	>80%		85%
Standby Mode Delay to Full Load	<5 ms	4 ms	~0.6372 ms
DC Output Voltage Load Regulation, DC/DC Enabled (0A to 3A)	3.3 ± 10 %		3.462 (0 A) – 3.466 (3 A)
DC Output Voltage Load Regulation, DC/DC disabled (0 A to 150 mA)	3.3 ± 10 %		3.3035 (0 mA) – 3.290 (150 mA)

2 Theory of Operation

Many automotive and industrial applications require efficient 12-V or 24-V buck power conversions from the main supply down to the point-of-load (POL) voltage at full load, but also need very low current consumption when the device is in an idle, or shutdown state. In order to achieve such low current, you can easily use a Low Dropout Regulator (LDO) in parallel with a buck converter to achieve minimal current draw from the battery when the system enters a light-load/no-load state.

Ultimately, the ideal situation to prolong battery life in the system would be to disable every possible device from the input supply. In some cases though, a sub-regulated voltage is still necessary for certain components within the system to allow communication with other system blocks during the shutdown state (i.e. a CAN bus transceiver in an automotive application). DC/DC converters that are not specifically designed for light-load efficiency can consume several milliamps with no load. Additionally, converters that do exhibit high light-load efficiency will utilize frequency-foldback schemes and discontinuous mode operation, resulting in noisy output voltages and excessive EMI emissions. An LDO is ideal for light load situations because they can be designed to consume very low currents while maintaining a low noise output voltage. The no-load current into the input (also called “ground current”) can be on the order of a few micro amps or lower. Combining the performance of both converter and LDO, therefore, has obvious benefits.

2.1 Approach

The approach selected in this reference design uses an enable pin to enable the DC/DC converter when the load is high (full load), and disable the DC/DC converter when the load is minimal. High voltage applications generally require good DC/DC converter efficiency across the load spectrum, however, the efficiency will naturally decrease as the load is decreased. In the light load region, a low-Iq LDO will exhibit higher efficiency than most DC/DC converters. Figure 1 shows a general example of LDO efficiency vs. DC/DC converter efficiency.

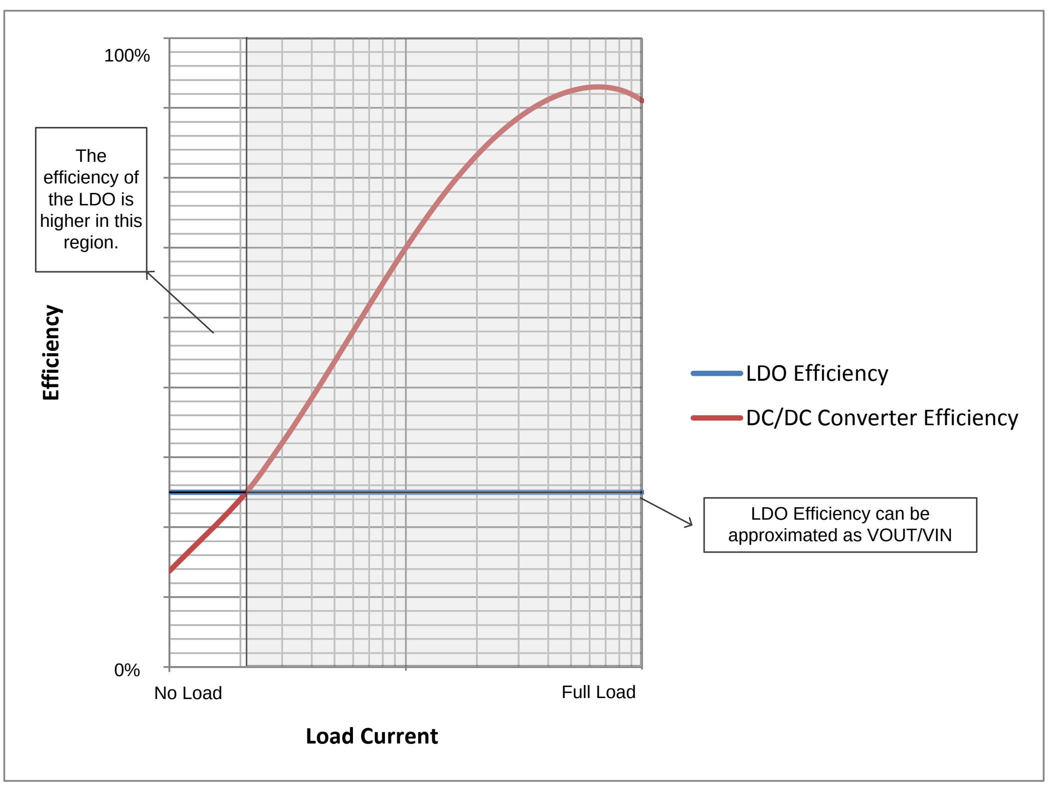

Figure 1: Efficiency vs. load current for a DC/DC Converter (Red) and an LDO (Blue)

Implementing this design requires that the converter output is set at a higher voltage than the maximum LDO output voltage. In normal operation, when the converter is enabled, the converter will regulate the output voltage and provide the current to the load. Most LDOs are unable to sink current, relying on load current sourced out of the pass device to regulate the output. Pulling the output voltage of the LDO above its nominal voltage will force the LDO into an unregulated state where current will not flow from the input to the output, and the DC/DC converter will effectively operate as if the LDO was not connected.

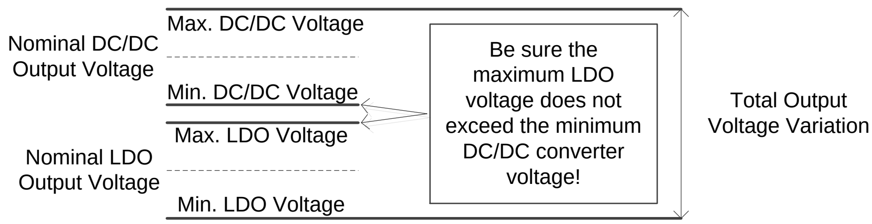

Figure 2: Maximum/Minimum Voltages for LDO and DC/DC Converter

Once the DC/DC converter is disabled, it will stop switching and the output voltage will decrease until the LDO begins to regulate the output. Upon enabling again, the DC/DC converter will start up in a pre-biased condition (a positive voltage existing on the output during startup is called “pre-biased”). The converter will begin its startup procedure without sinking any current from the output node, eventually pulling the voltage at the output above the nominal LDO voltage, and regaining control of the output.

3 Component Selection

3.1 DC/DC Converter

The requirements for the DC/DC converter, in addition to ability to support the maximum/minimum VIN and IOUT, are listed below:

1) Adjustable Output. The DC/DC output voltage must be adjusted sufficiently above the LDO voltage to ensure the LDO does not get loaded under heavy loads. Equation 1 below gives the necessary calculation.

$$V_{REFMIN} \times \left[\frac{R_{FBTOPMIN}}{R_{FBBOTMAX}} + 1\right] - V_{LINE,LOAD\ ERR} > V_{LDOMAX}$$

Where

V_{REFMIN} = Minimum DC/DC converter reference voltage

$R_{FBTOPMIN}$ = Minimum value of top feedback resistor (From VOUT to VFB)

$R_{FBBOTMAX}$ = Maximum value of bottom feedback resistor (From VFB to GND)

$V_{LINE,\ LOAD\ ERR}$ = Total Line Regulation and Load Regulation Error of DC/DC converter

V_{LDOMAX} = Maximum LDO voltage across load, line and temperature

Equation 1

2) Pre-biased Startup Capability. The DC/DC converter must not sink current when it starts up into an existing output voltage. This is commonly referred to as pre-biased startup.

3) Enable. The device must be able to be enabled and disabled.

3.2 Low Drop Out Regulator

The requirements for the LDO, in addition to be able to support the maximum VIN, are listed below:

1) The LDO's maximum output voltage must be lower than the converter's minimum. For an adjustable LDO, the error from the feedback resistors must be taken into account, as well as the line and load regulation error.

2) The LDO must have sufficient power dissipation to ensure it does not exceed the maximum junction temperature when the DC/DC converter is disabled.

3) The output and input capacitance requirements of the LDO must match the DC/DC converter. Generally, the converter will require higher capacitance values than the LDO. The LDO must be stable with the necessary converter capacitance.

3.3 Load Delay Circuit

The DC/DC converter requires several milliseconds to reach the steady-state output voltage. If a heavy load is drawn from the LDO before the DC/DC converter has reached steady-state, the LDO could go into current limit and the regulation voltage can drop below the desired levels. To prevent this, the load should be not be switched to the converter until after the converter is enabled; this will allow for the converter to start up and be able to carry the load without experiencing an exaggerated dip in the output voltage. For this design, a simple RC delay was used between the load and the enable signal. To slow the load enough to allow the DC/DC converter to reach steady-state, a 1-kOhm resister and a 1-µF capacitor were used; a Schottky diode was also placed in parallel with the resistor to remove the delay on the falling edge.

4 Simulation

The bill of materials can be found in the Appendix.

4.1 Simulation

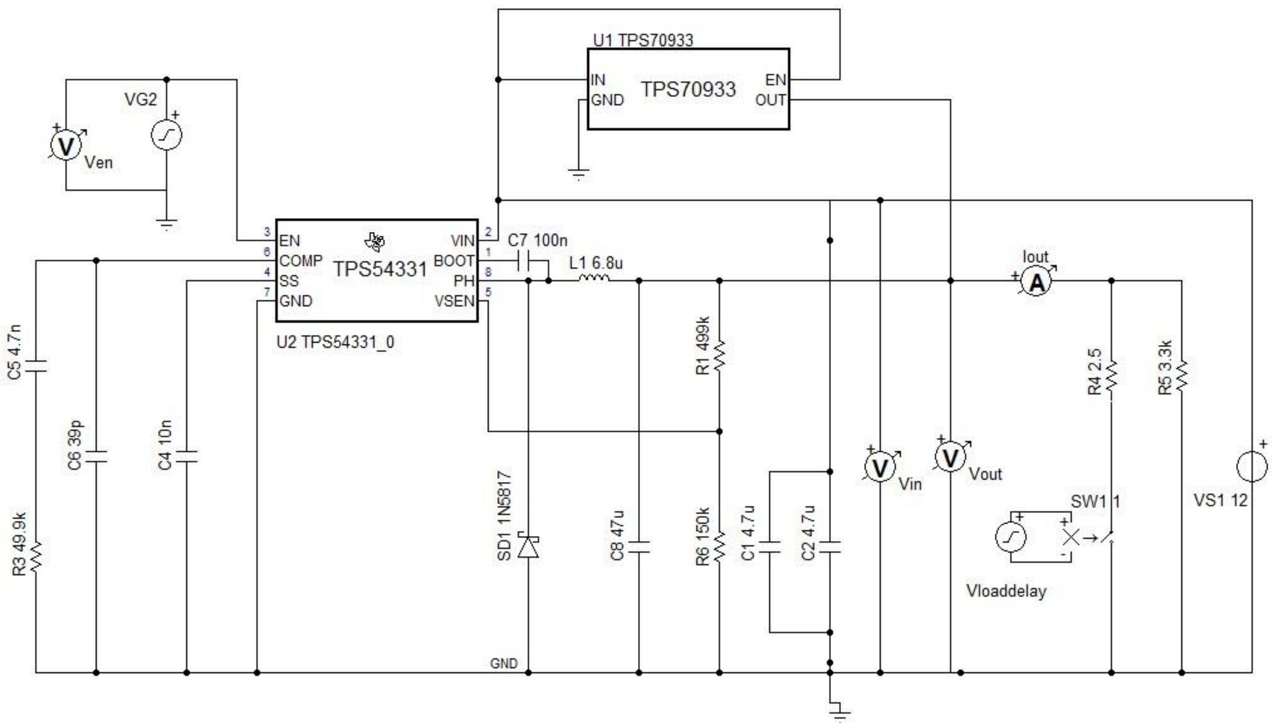

Figure 3: TINA-TI™ Simulation Circuit

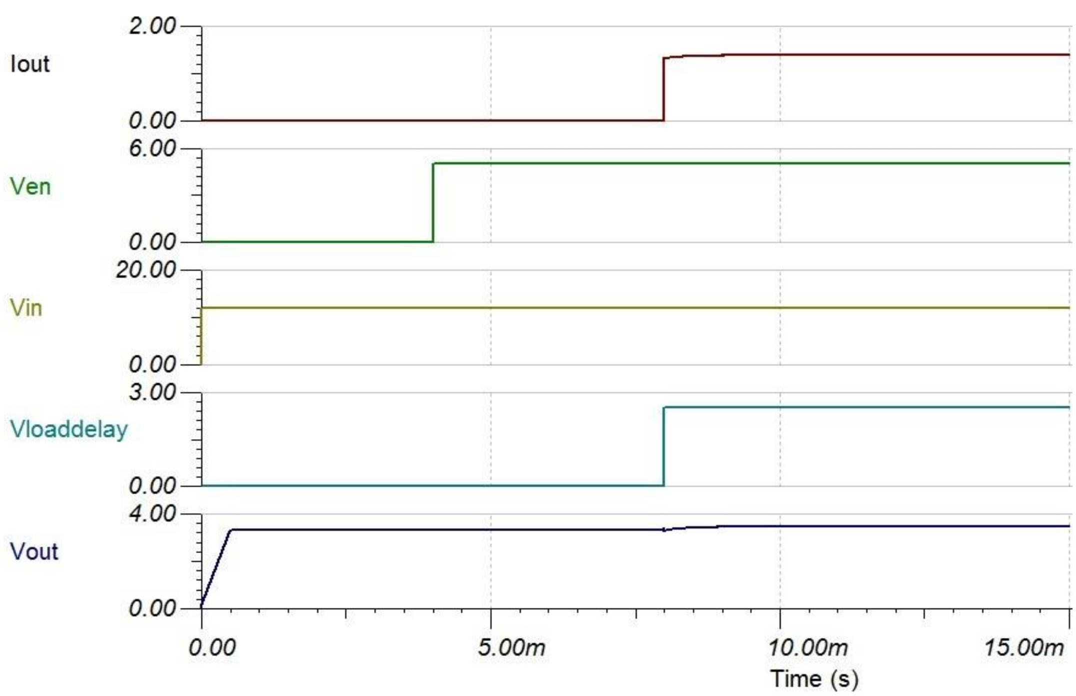

Figure 4: Simulated Startup with Enable and load delay

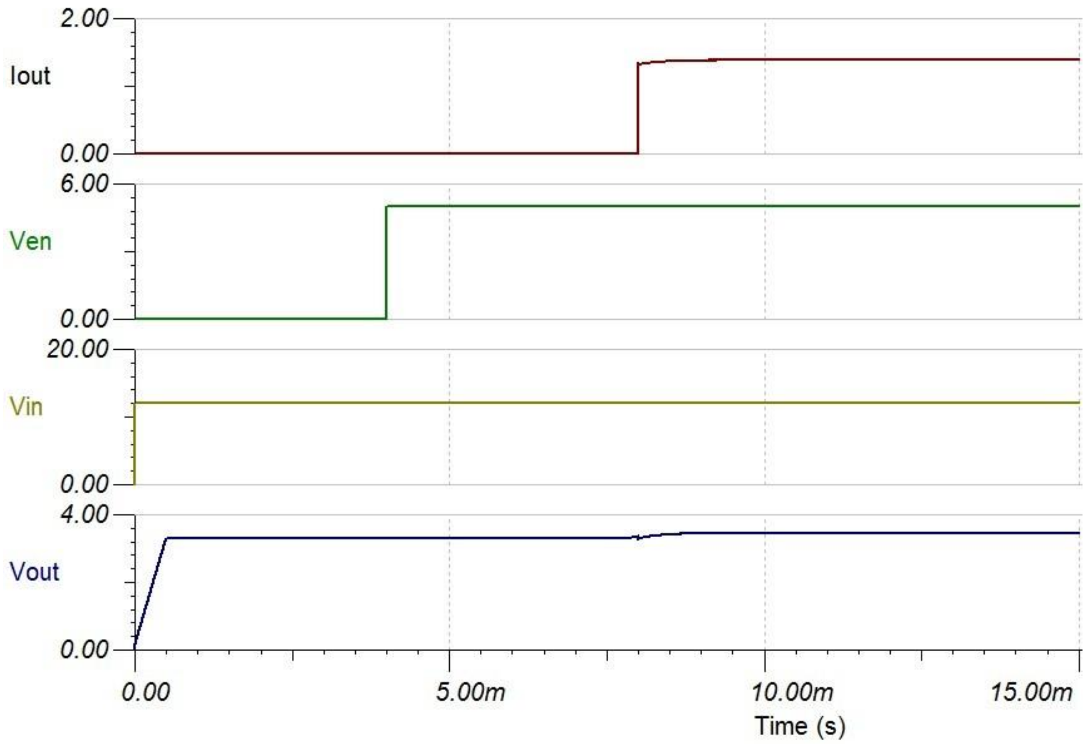

Figure 5: Simulated Startup with Enable

5 Verification & Measured Performance

The design schematic can be seen in Figure 6. The TPS709 was selected for the LDO for ultra-low Iq, and the TPS54331 was selected for the DC/DC converter for high efficiency across loads.

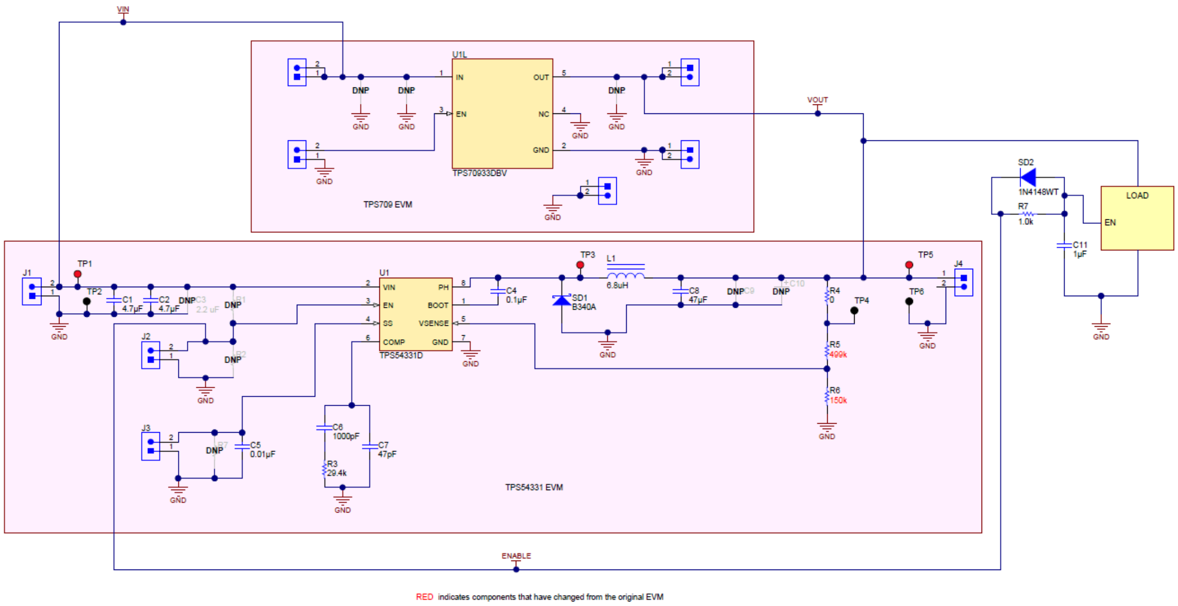

Figure 6: Schematic

5.1 Efficiency measurements

Figure 7 shows the load at which the efficiency is higher for the DC/DC converter versus the LDO, around 250 µA.

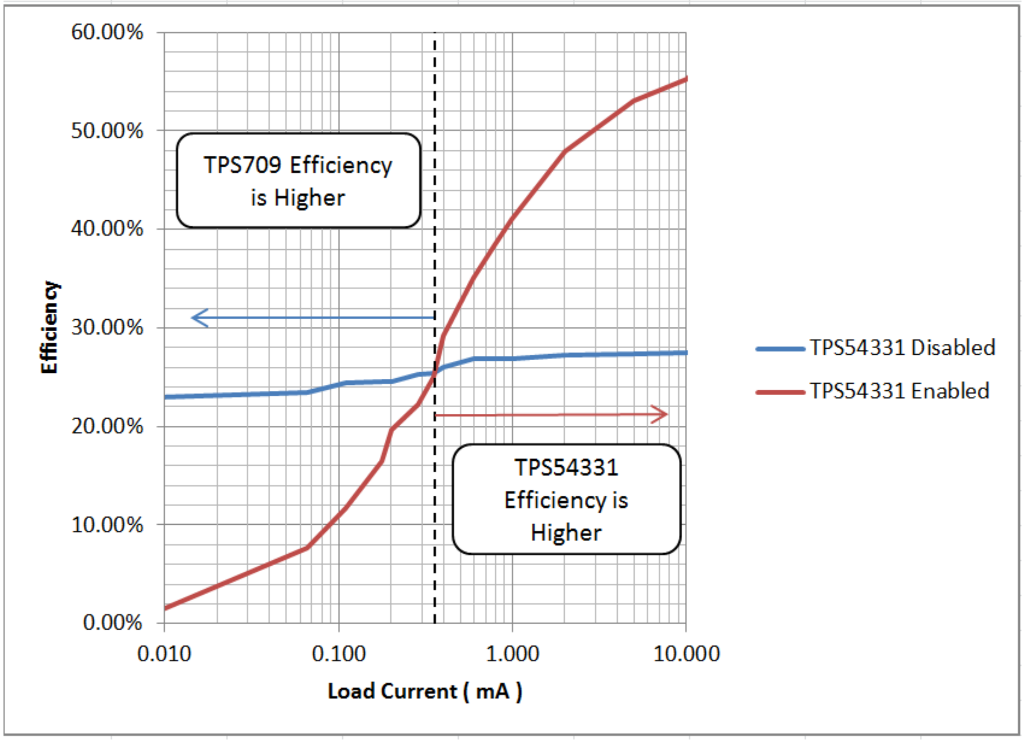

Figure 7. Efficiency of TPS54331 compared to TPS70933 (TPS54331 disabled)

5.2 Start up

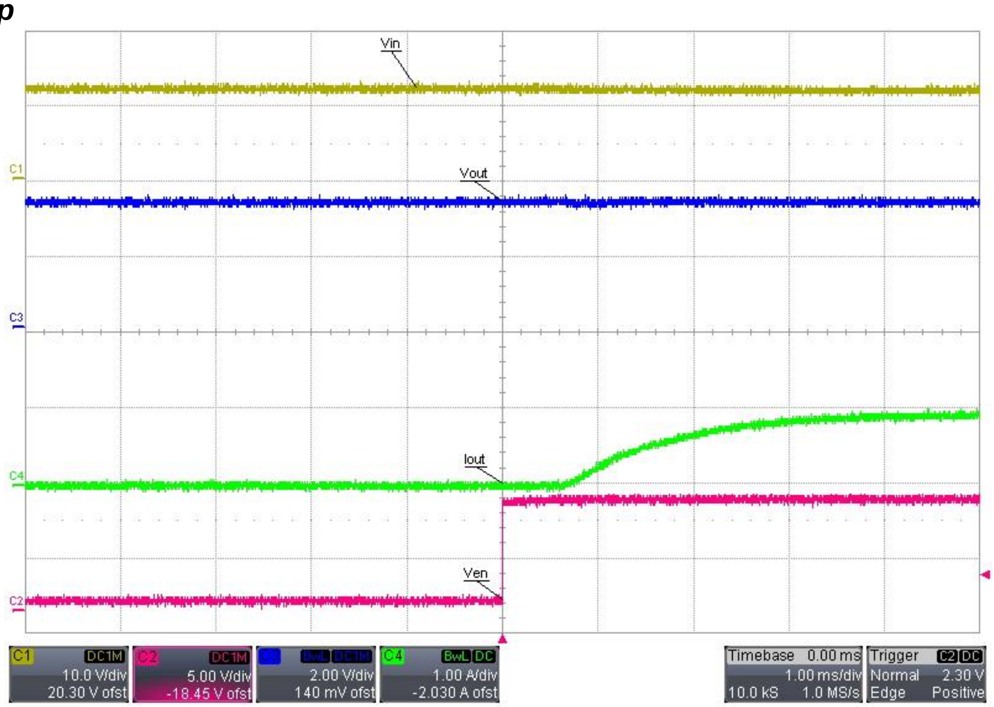

Figure 8: Enable transition low to high, load delay

5.3 Converter Enable Switching

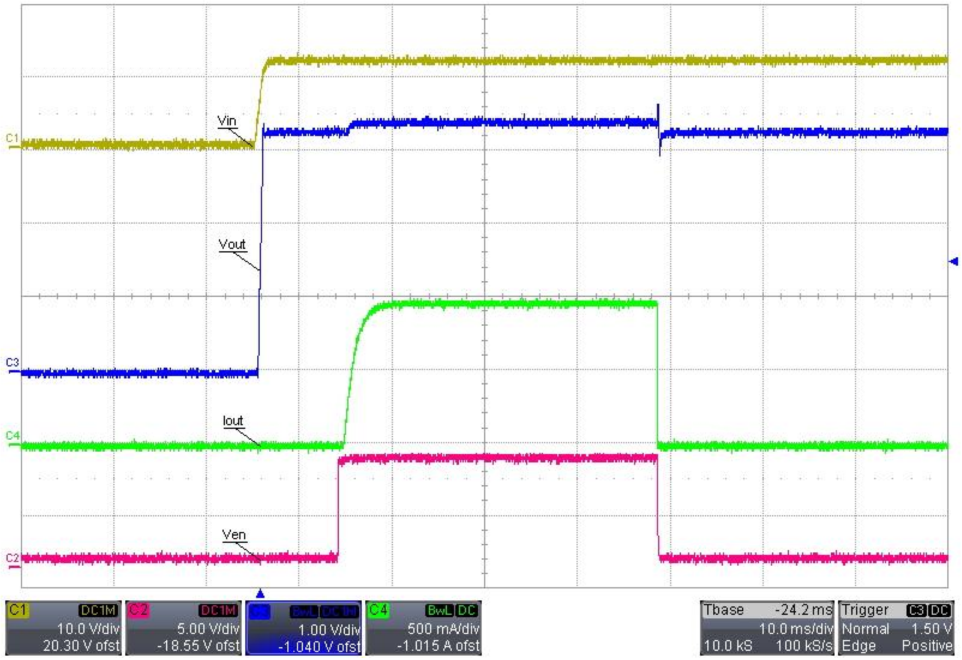

Figure 9: Start up followed by Enable and load pulse

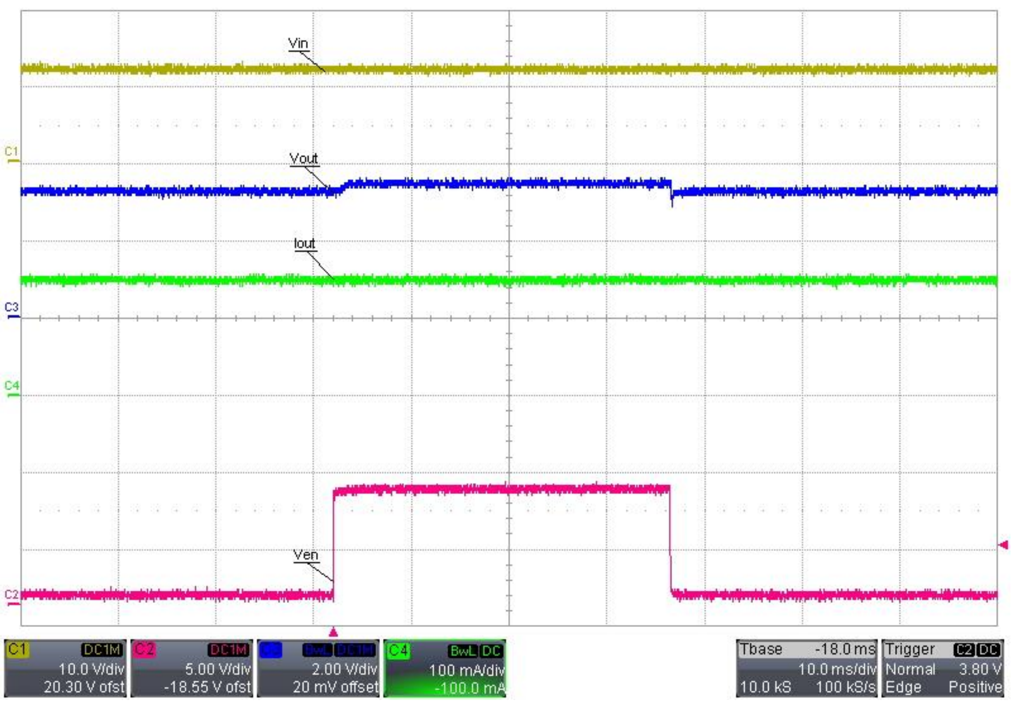

Figure 10: Output voltage variation from Enable pulse, 150 mA load

5.4 Power Down

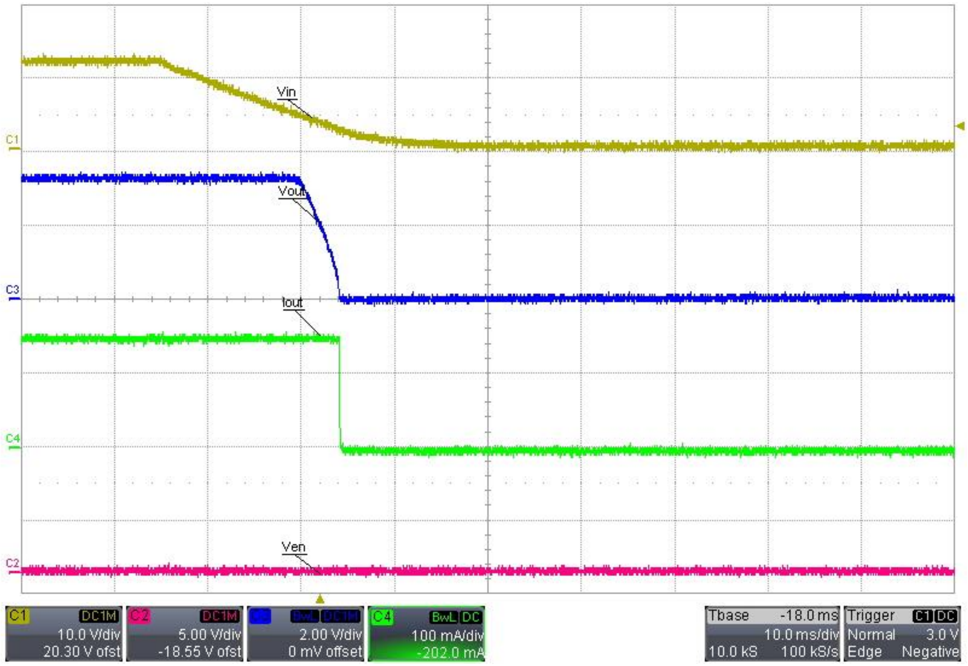

Figure 11: Shut down of circuit with Enable signal low.

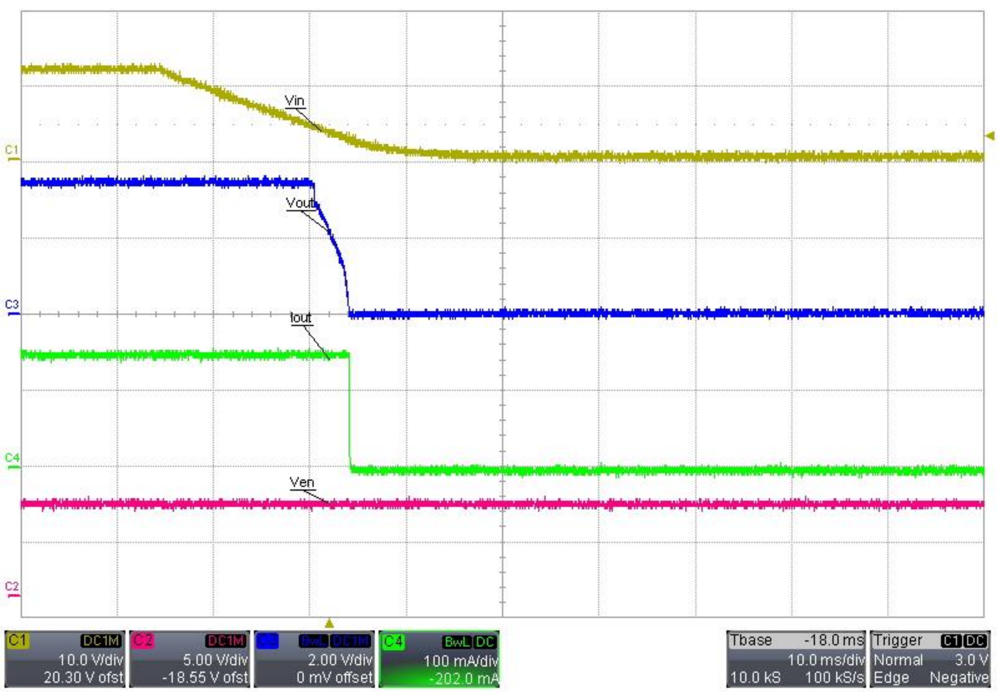

Figure 12: Shut down of circuit with enable signal high.

6 About the Author

Mike Hartshorne is an applications engineer in the Linear Power business unit. He has worked as an applications engineer in various power product lines, and previously in Analog-to-Digital Converter product lines. Mike received a BSEE from the University of San Diego and an M. Eng. from the University of Arizona.

Cynthia Sosa is an applications engineer in the Linear Power business unit. She received her BSEE from the University of Texas at El Paso in 2014. She joined TI in 2015.

7 Acknowledgements & References

1. *TPS709 Datasheet*

2. *TPS54331 Datasheet*

3. *How to improve buck converter light load efficiency with LDO -Part1*

4. *How to improve buck converter light load efficiency with an LDO -Part2*

Appendix A.

A.1 Simulations and Measurements

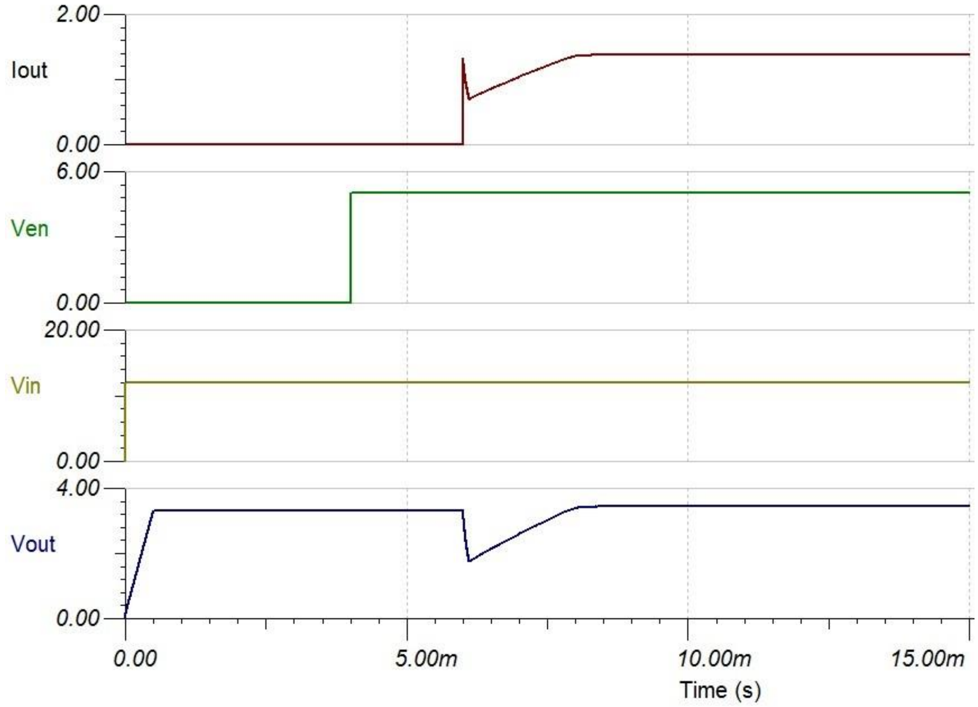

Figure A-1: Simulation of insufficient load delay

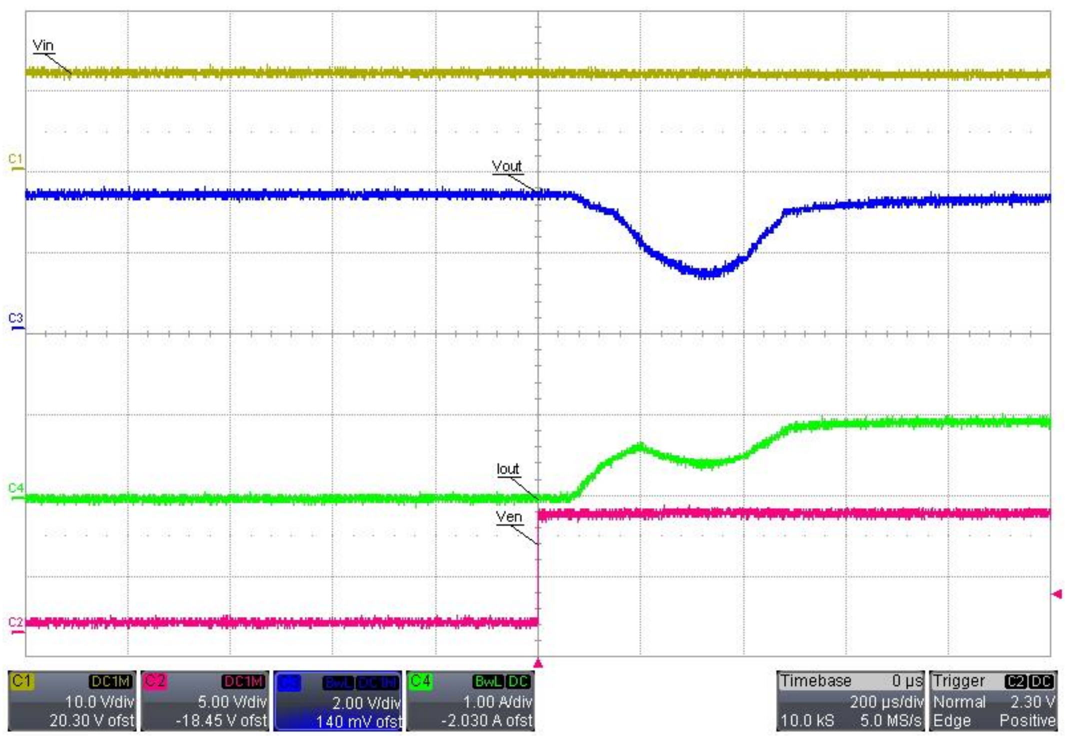

Figure A-2: VOUT drop when load delay is insufficient

A.2 Bill of Materials

Item	Qty	Reference	Value	Part Description	Manufacturer	Manufacturer Part Number	Alternate Part	PCB Footprint
1	2	C1, C2	4.7uF	Capacitor, Ceramic, 50V, X7R, 20%	STD	STD		1210
2	1	C4	100nF	Capacitor, Ceramic, 50V, X7R, 20%	STD	STD		0603
3	1	C5	10nF	Capacitor, Ceramic, 50V, X7R, 20%	STD	STD		0603
4	1	C6	1nF	Capacitor, Ceramic, 50V, X7R, 20%	STD	STD		0603
5	1	C7	47pF	Capacitor, Ceramic, 50V, X7R, 20%	STD	STD		0603
6	1	C8	47uF	Capacitor, Ceramic, 6.3, X5R, 20%	TDK	C3216X5R0J476MT		1206
7	1	C11	1 uF	Capacitor, Ceramic, 6.3, X5R, 20%	TDK	STD		0603
8	1	L1	6.8uH	Inductor, SMT, 3.84A, 35 mW	Sumida	CDRH103RNP-6R8		0.406 x 0.409
9	1	SD1	B340A	Diode, Schottky, 3A, 40V	Diodes Inc	B340A		SMA
10	1	SD2	1N4148	Diode Rectifier	Powerex Inc	1N4148		SMA
11	1	R3	29.4kΩ	Resistor, Chip, 1/16W, 1%	STD	STD		0603
12	1	R4	0Ω	Resistor, Chip, 1/16W, 1%	STD	STD		0603
13	1	R5	499kΩ	Resistor, Chip, 1/16W, 1%	STD	STD		0603
14	1	R6	150kΩ	Resistor, Chip, 1/16W, 1%	STD	STD		0603
15	1	R7	1kΩ	Resistor, Chip, 1/16W, 1%	STD	STD		0603
16	1	U2	TPS54331	IC, DC-DC Converter, 28V, 3A	TI	TPS54331D		SO-8
17	1	U1	TPS70933	IC, 150 mA, ultra-low IQ, 1-μA LDO reg	TI	TPS70933DBV		SOT-23

Figure A-2: Bill of Materials, all Designators are in reference to Figure 6.

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