TI Designs: TIDA-00530

Automotive Power Reference Design for Low-Power TDA3x Based Systems

Description

The TIDA-00530 design is an integrated, size-optimized power design for advanced driver assistance system (ADAS) applications using the TDA3x system on chip (SoC) off of an automotive battery input. By targeting only applications with lower processing needs, these devices and components are smaller compared to systems using higher performance processors.

Resources

TIDA-00530	Design Folder
LM53603-Q1	Product Folder
TPS54116-Q1	Product Folder
LP8731-Q1	Product Folder
LM74610-Q1	Product Folder
LM3880-Q1	Product Folder
TPS61240-Q1	Product Folder
TPS3808-Q1	Product Folder

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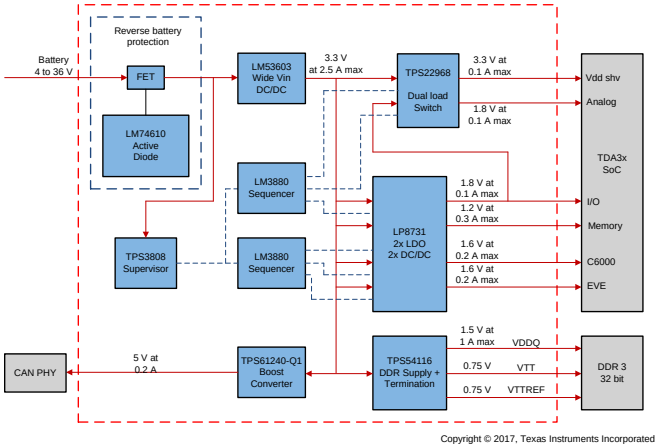
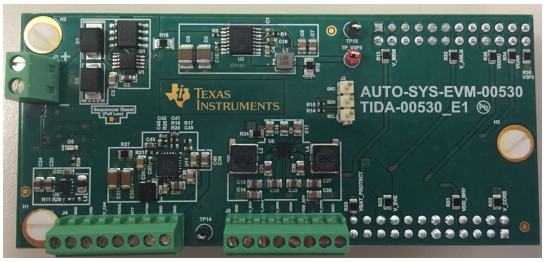
Features

- Complete TDA3x, DDRx, and CAN Power Solution
- Highly-Integrated, Size-Optimized Design
- Off-Battery Operation
- Full Power-up and Power-Down Sequencing
- Designed to ISO 7637-2:2004 Pulse 1, 2a, and 5b (Clamped Load Dump)

Applications

- Rear Camera
- Mono Front Camera
- Multi-Mode Radar (SRR and MRR)





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1 System Description

This system is designed to be a complete power solution for low-power TDA3x ADAS processor applications, including key peripheral power (CAN PHY, DDR). This TI Design was created with the following points in mind:

- Satisfy power requirements for the TDA3x applications processor's single DSP at 700 MHz and EVE co-processor at 650 MHz use case
- Provide power for CAN PHY and DDR3 memory
- Implement a compliant sequencing (both power up and power down) scheme for the system per the TDA3x requirements
- Operate over the full range of battery conditions (3.5 to 42 V)
- Survive and continue operation through ISO 7637-2:2004 pulses 1, 2a, and 5b (clamped load dump)
- Optimize the individual blocks for smallest possible solution size
- Provide flexible board interface to either mate with the TDA3x EVM, or jumper to custom board through screw terminals

This solution is sufficient for low-power TDA3x processing applications. Example applications include smart rear view cameras, low-end mono front cameras, and multi-mode radar (SRR and MRR) systems. Figure 1 shows an example of a TDA3x-based mono front camera system:

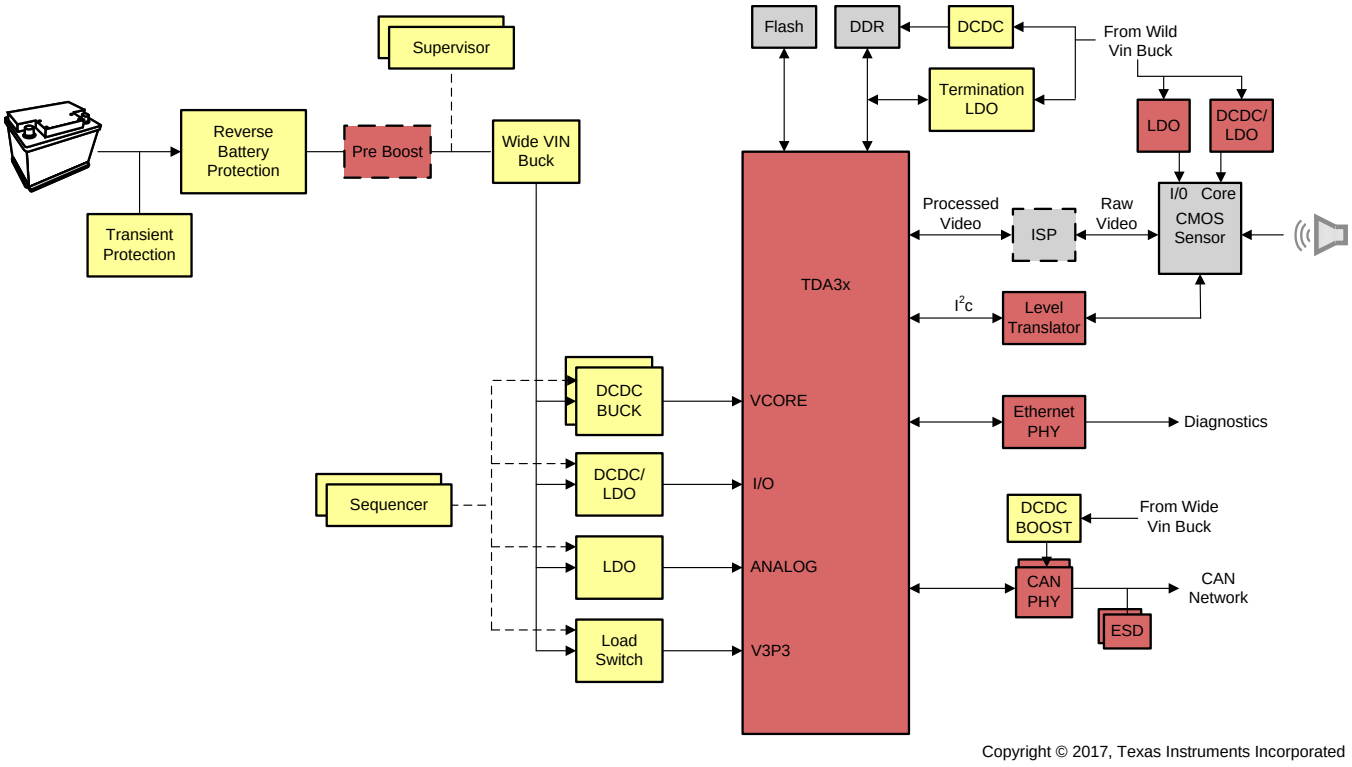


Figure 1. Example TDA3x-Based Mono Front Camera Block Diagram

The yellow blocks are all components found on the TIDA-00530 board, covering nearly all monitoring, sequencing, and power requirements of the example system (as this TI Design is not application-specific, power for a CMOS imaging sensor or other application-specific blocks is not included).

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
SYSTEM INPUT						
V_{IN}	Input voltage	Battery voltage range (DC)	3.5	13	36.0	V
I_{IN}	Input current	All rails at full load	—	—	2.2	A
V_{CLAMP+}	Positive clamping voltage	Positive input protection TVS clamping range	28.9	—	42.1	V
$V_{CLAMP–}$	Negative clamping voltage	Negative input protection TVS clamping range	15.6	—	25.8	V
P_{PK}	Peak pulse power dissipation	Maximum TVS power dissipation	—	600	—	W
OUTPUT VOLTAGES						
V_{OUT}	V_CORE	TDA3x DSP core supply	1.039	1.06	1.081	V
	V_EVE	TDA3x EVE coprocessor core supply	1.039	1.06	1.081	V
	V_ANLG	TDA3x analog supply	1.746	1.80	1.854	V
	V_MEM	TDA3x memory supply	1.164	1.20	1.236	V
	VDDIO	TDA3x I/O supply	1.746	1.80	1.854	V
	VDD_SHV	TDA3x auxiliary supply	3.247	3.30	3.380	V
	V_CAN	CAN PHY supply	4.900	5.00	5.100	V
	VDDQ	DDR3 supply	1.485	1.50	1.515	V
	VTT_REF	DDR buffered reference	VDDQ × 0.49	VDDQ × 0.5	VDDQ × 0.51	V
	VTT	DDR termination supply	—	VTT_REF	—	V
OUTPUT CURRENTS						
I_{OUT}	V_CORE	TDA3x DSP core supply	—	—	1.2	A
	V_EVE	TDA3x EVE coprocessor core supply	—	—	1.2	A
	V_ANLG	TDA3x analog supply	—	—	0.1	A
	V_MEM	TDA3x memory supply	—	—	0.3	A
	VDDIO	TDA3x I/O supply	—	—	0.2	A
	VDD_SHV	TDA3x auxiliary supply	—	—	0.1	A
	V_CAN	CAN PHY supply	—	—	0.2	A
	VDDQ	DDR3 supply	—	—	1.0	A
	VTT	DDR termination supply	—	—	1.0	A

2 System Overview

2.1 Block Diagram

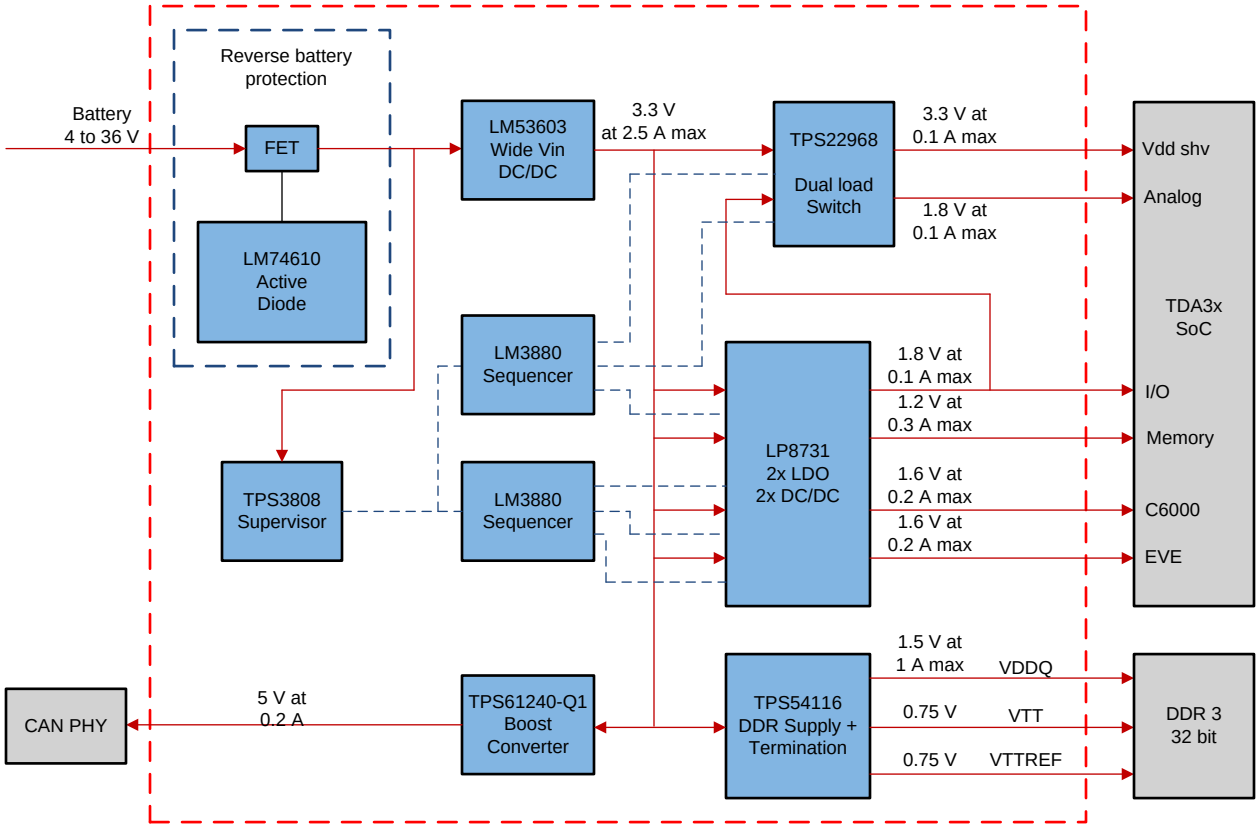


Figure 2. Power Solution for TDA3x Based Systems

2.2 Highlighted Products

This TI Design uses the following TI products:

- The LM53603-Q1 is a 2.1-MHz synchronous buck converter with a wide input voltage range from 3.5 to 36 V (42-V transients), enabling the device to work directly from an automotive battery
- The LP8731-Q1 is a highly integrated multi-output power management device containing two buck converters and two low-dropout regulators (LDOs) in a single package with internal sequencing
- The TPS54116-Q1 is an integrated buck regulator and LDO for memory and DDR applications.
- The TPS61240-Q1 is a highly compact boost converter intended for use with 5-V CAN PHYs
- The LM74610-Q1 "Smart Diode Controller" is a high-side N-FET controller intended for reverse-battery protection
- The LM3880-Q1 is a three-channel, cascadable sequencer

Find more information on each device and why it was chosen for this application in the following subsections.

2.2.1 LM53603-Q1

Because this TI Design uses about 2.1 A, the device maximum of 3 A provides a healthy amount of headroom. This device nominally switches at 2.1 MHz in PWM mode. In automotive designs, DC-DC converters must switch at a frequency outside the AM radio band. Staying above this band allows the user to shrink the external components to optimize the size of the board. To stay above the AM band, force the device into PWM mode. This is achieved by setting the FPWM pin high. Without this forced PWM mode feature, the device could fall into discontinuous conduction or PFM mode at light load conditions. Here, the switching the frequency would be in the AM band. However, because of the minimum on-time limitations at high voltages and minimum off-time limitations at voltages lower than 6 V, the switching frequency will be reduced to overcome these limitations. Temperature variation also enhances these effects.

Integrated FETs with a synchronous rectifier provides a more efficient approach than asynchronous devices, and makes forced PWM mode possible. Though not used in this TI Design, external clock synchronization can be used to avoid beat frequencies between multiple converters or to allow a master to dither the clock signal. This can be a very useful feature for optimizing systems for EMI performance.

To operate straight off of the battery, a wide input voltage range is required. Many safety-critical ADAS systems must also withstand load dump as well as cold-crank and start-stop conditions. This device meets these requirements as well with the 3.5- to 36-V, 42-V transient input voltage range.

2.2.2 LP8731-Q1

In applications that are space constrained, it is crucial for devices to have a high level of integration. The LP8731-Q1 has two bucks and two LDOs in a 2.5×2.5-mm BGA package. The part further reduces solution size by integrated compensation components and eliminates the need for feedback resistors by operating at fixed voltages (configurable through I^2C). The buck regulators in the device operate at a fixed frequency of 2.1 MHz, meeting the requirement to stay above the AM band.

Although this TI Design uses external sequencing, the device has internal sequencing, which allows for some systems to eliminate the need for external sequencer ICs, further reducing the solution footprint.

2.2.3 TPS54116-Q1

The TPS54116-Q1 contains an integrated buck regulator for DDR memory applications and an integrated LDO VTT termination regulator greatly reducing the total solution size when compared to a discrete approach.

Loads current up to 4 A, can be drawn from the buck regulator at a 2 MHz switching frequency allowing for up to 4 GB of DDR3 memory to be supported. This TI Design makes use of only 1 GB of DDR3 memory which is sufficient for the low-end processing applications targeted and provides more than sufficient headroom for all tasks at just 1 A of current draw..

2.2.4 TPS61240-Q1

This fixed 5-V boost converter for CAN PHY reduces external component count and switches well above the AM band at 3.5 MHz. Because 5 V at 200 mA is required for most CAN PHYs, this device is optimized for this application. The package is a very small 2×2-mm WSON. The only required external components are the I/O capacitors and inductor.

2.2.5 LM74610-Q1

The LM74610-Q1 Smart Diode Controller satisfies the requirement for reverse-battery protection on all electrical subsystems. This device controls an external N-FET in series with the battery supply input to act as an ideal diode, reducing the voltage drop and power loss as opposed to a discrete diode solution. When a reverse-battery condition is detected, the device quickly turns off the FET isolating and protecting downstream circuitry.

Because the voltage drop across the FET is negligibly small, this provides more input voltage headroom for the wide input voltage buck converter, allowing it to operate at even lower battery input voltages. For example, a cold-crank scenario could see the battery voltage temporarily drop to as low as 3.5 V at the input of the system. With a diode solution, the buck converter would see 3.5 V minus the typical diode drop of 0.7 V, or 2.8 V, and would not be able to maintain the 3.3-V system voltage. With the smart diode solution, the buck will still see close to 3.5 V during this condition and continue to operate.

Because the part has no ground reference, the quiescent current is virtually zero, which helps the subsystem draw less standby current from the battery. Many OEMs have very small quiescent current budgets.

2.2.6 LM3880-Q1

The LM3880-Q1 is a three-channel sequencer with open-drain outputs. The open-drain output is compatible with the active-high enable signals of all devices used in this system, so additional inverters are required. This part can be cascaded with some external logic to expand to more than three channels. This is required for the application to control the sequencing of five separate outputs.

Different orderable part numbers for various power-up and power-down sequences and delay lengths are available. This allows configurability without the need for programming or external components.

2.3 System Design Theory

2.3.1 PCB and Form Factor

The goals for the board geometry are two-fold:

1. Provide compatibility with the TDA3x 15×15 Validation Board.
2. Provide the ability to evaluate the solution standalone without the validation board.

Another design target is providing the smallest board possible. Because the board needs to mate with the TDA3x Validation Board, there is the possibility of collision with validation board components or interference with switches or interfaces on the main PCB. The validation board provides an area specifically for a power management daughterboard. The daughterboard area on the PCB is circled in Figure 3:

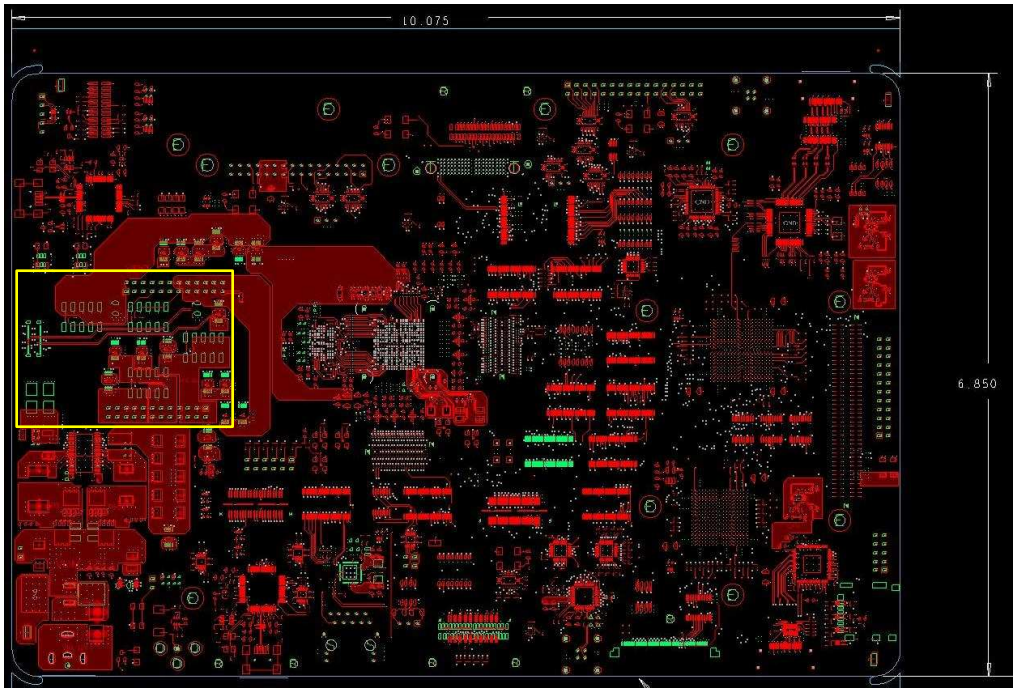


Figure 3. TDA3x Validation Board (Power Management Daughter Board Highlighted)

Because the area is on the edge of the board, one could simply create an extension for the board and allow the bulk of the solution to extend outside of the validation board outline to the left. The mating headers are on the right side of the board.

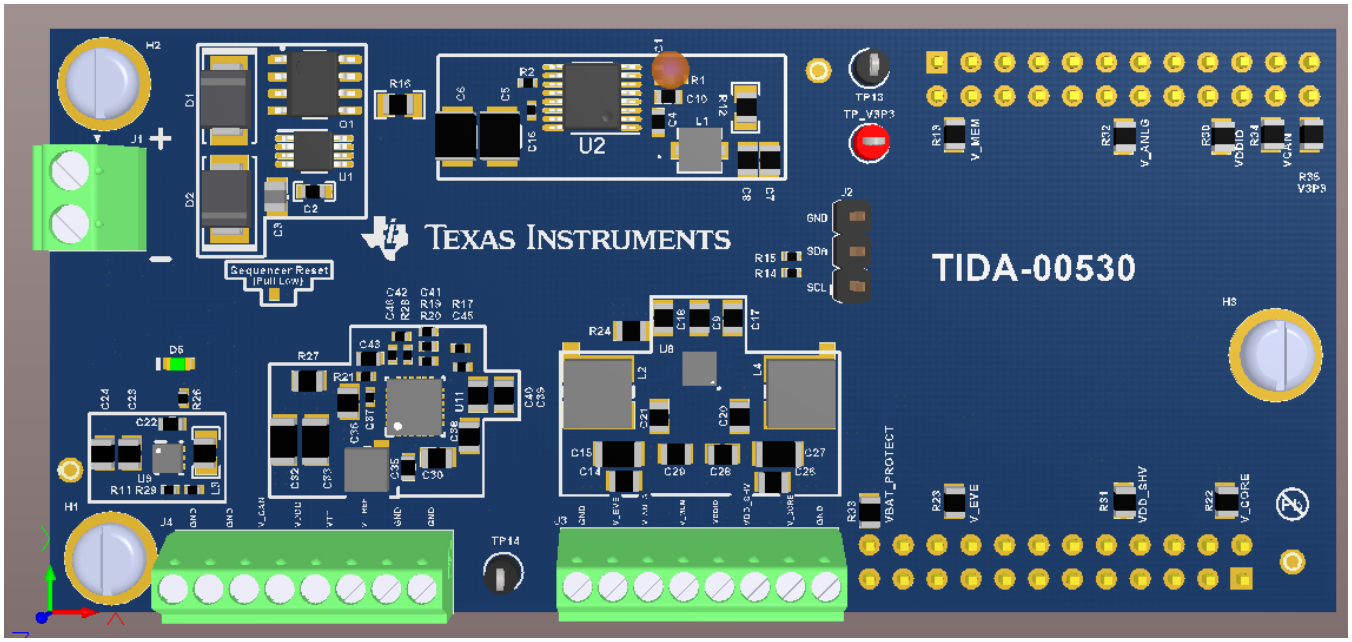


Figure 4. TIDA-00530 PCB Render

This frees the user to use as much length in the x-axis in Figure 4 for the solution.

2.3.2 Input Protection and Wide-V_{IN} DC-DC

2.3.2.1 Reverse Battery Protection

Reverse battery protection is required in nearly every electronic subsystem of a vehicle, both by OEM standards as well as ISO 16750-2, an international standard pertaining to supply quality.

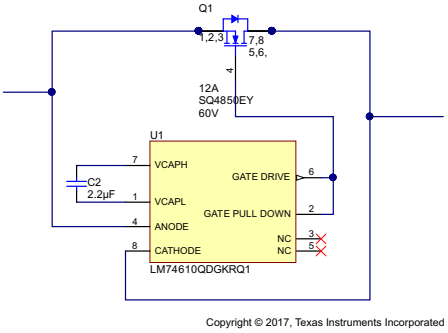


Figure 5. Reverse Battery Input Protection

Rather than use the traditional diode rectifier solution for reverse battery protection, this implementation uses an N-channel MOSFET driven by the LM74610-Q1 Smart Diode Controller. The diode solutions power dissipation can be significant due to the typically 600- to 700-mV forward drop, whereas using this solution only results in the loss due to the $R_{DS(ON)}$ of the FET, which can be significantly lower resulting in greater efficiency and less required thermal dissipation.

The LM74610 team provides recommendations as well as a tool to help select a FET for an application. Here are the important considerations:

- Ensure that the continuous current rating is sufficient for the application.
- The V_{GS} threshold must be 2.5 V at maximum.
- V_{SD} must be at least 0.48 V at 2 A and 125°C.

For this TI Design, the FET needs to be rated at least as high as the clamped input voltage; a 40-V FET would be acceptable, but this TI Design uses a 60-V for additional headroom.

2.3.2.2 TVS Diodes

Transient voltage suppression (TVS) diodes are required on the supply input of the system to protect against both positive and negative going transients. The transients to be concerned with are detailed in ISO 7637-2:2004, pulses 1 and 2a. Many systems in a car can simply shut down during these transients until the condition passes, but many ADAS applications are required to continue operation. For this reason, shunt the transients instead of using an overvoltage shutdown scheme.

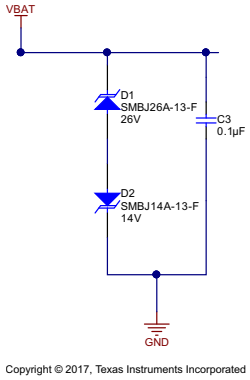


Figure 6. Input Transient Protection

Choose the diode breakdown voltages such that transients are clamped at voltages that will protect the MOSFET and, as follows, the rest of the system. The positive clamping device must clamp above double-battery (jump-start) and clamped load dump voltages, but lower than the maximum operating voltage of the downstream devices. In this case, this means starting to clamp around 28 V, but having a maximum clamping voltage below 40 V. Ideally, the best choice is somewhere around 36 V as the maximum clamping voltage.

The reverse clamping device must clamp all negative voltages greater than the battery voltage so that it does not short out during a reverse-battery condition.

Due to the energy of the pulses, SMD-sized TVS diodes with 600-W instantaneous peak power ratings are the minimum required.

2.3.2.3 Input Capacitors Exposed to Battery Inputs

The final consideration for the front-end protection is the input capacitor. Due to flexion of the PCB or other means, it is possible for a ceramic capacitor to mechanically fail short; if this happens to an input capacitor connected directly to the battery, this could cause a hard short at the battery terminals. To avoid this short, typically two ceramic capacitors are used in series and aligned at 90° with respect to each other in the layout. These capacitors give a good chance that a flexion in one direction may only affect the capacitor aligned in that direction; if one fails, there is still another to avoid a short. This solution instead uses a capacitor designed specifically for this application, which effectively includes two capacitors previously described into a single SMD package.

2.3.2.4 Wide Input Voltage Buck Converter

The LM53603-Q1 is an AECQ100 qualified, wide input voltage buck regulator used as a front-end supply to provide a 3.3-V system voltage. With an input voltage range of 3.5 to 36 V nominally, and transients up to 42 V, the device can continue operation through most battery conditions such as start-stop, cold-crank, and load dump.

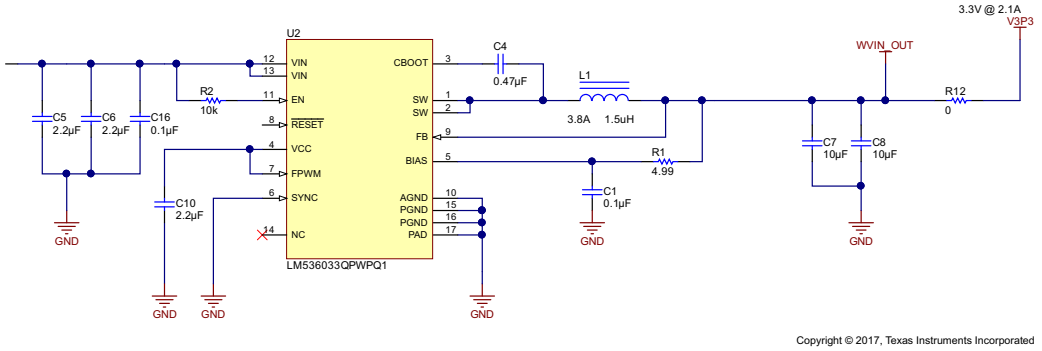


Figure 7. LM53603-Q1 Wide Input Voltage Buck

The LM53603-Q1 can automatically transition from PWM to PFM mode to achieve light load efficiency. However, because the goal is to ensure that the effective switching frequency does not drop into the AM band, this feature needs to be disabled by pulling the FPWM pin high. Pay attention to the absolute maximum of this pin. Because it can only handle 5.5 V, tying it to VIN may exceed this maximum in certain conditions and potentially damage the device. It is recommended to pull it up to VCC, which is a 3.3-V supply generated internally by the device. However, it is also acceptable if there is another 3.3-V, or similar, auxiliary supply available on the board that comes up before the LM53603-Q1.

2.3.2.5 Sequencing and Voltage Supervision

The solution for sequencing uses two cascaded LM3880-Q1 three-channel sequencers in conjunction with some logic and a battery supply supervisor. The order in which the LM3880-Q1 sequencers enable and disable its outputs, and the delays associated with the power-up and power-down, is different between several orderable part numbers. In this case, thee sequence goes up 1, 2, 3, and down 3, 2, 1, with a 10-ms delay between each. The solution requires external logic to properly execute power-down sequencing.

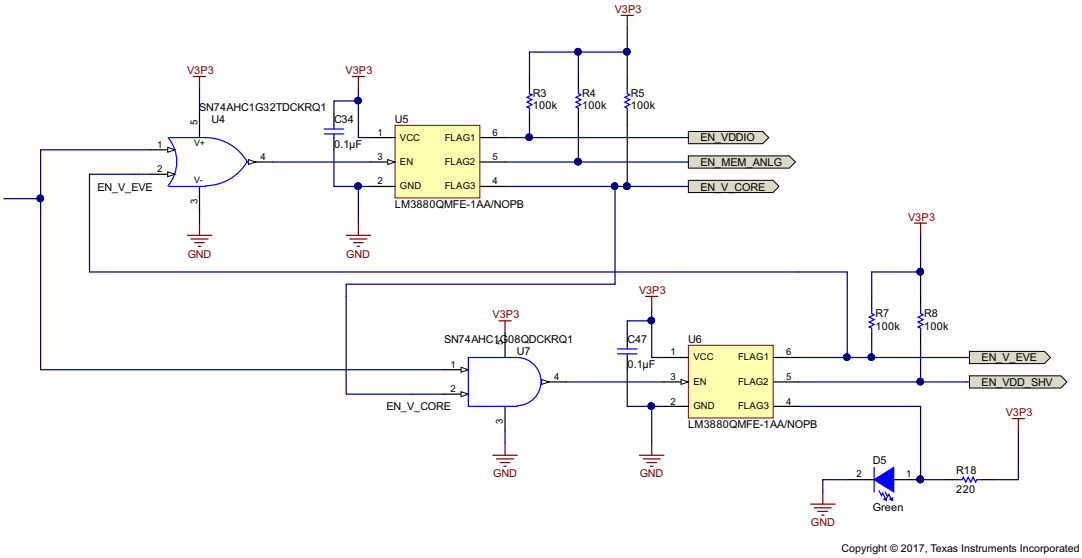


Figure 8. Cascaded LM3880-Q1 Sequencers With External Logic for Power-Down Sequencing

The TPS3808-Q1 supply supervisor is used to detect a rising or falling battery voltage and kick off the power-up and power-down sequences, respectively. The supervisor must monitor the battery voltage before the reverse polarity protection. The LM74610-Q1's "hiccup" behavior will the voltage ahead of it to drop by 0.6 to 0.7 V every few seconds, which could lead to a false early shutdown.

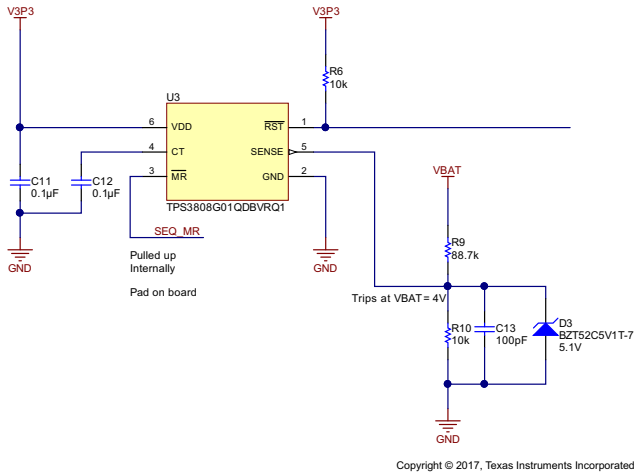


Figure 9. TPS3808-Q1 Voltage Supervisor

Sometimes, there are multiple power rails in a system that have the same voltage, but need to be sequenced or controlled separately. A load switch allows one to use the same LDO or DC-DC for both rails while having independent control over each. In this case, for instance, VDDIO and V_ANLG are both 1.8-V rails sourced from the same LDO, but can be independently sequenced.

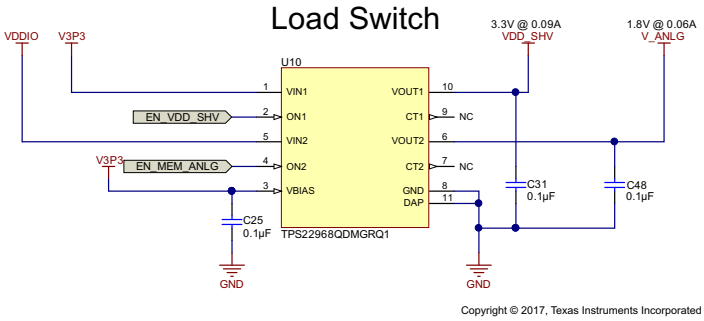


Figure 10. Load Switch Schematic

An alternate solution here is to use the internal power-up and power-down sequencing of the LP8731-Q1. The sequence is configurable through I^2C and be used for its four outputs. For this solution, this TI Design uses a discrete solution, but if using the internal sequencing, one LM3880-Q1 could be removed.

2.3.2.6 General Power Supply Design Considerations

For this power supply, choose inductors such that:

- The ripple current is between 20% to 40% of the load current I_{LOAD} with the given switching frequency, input voltage, and output voltage. This TI Design uses 40% was used.
- The temperature ratings are appropriate for automotive applications, typically –40°C tp 125°C for ADAS applications.
- Saturation current is chosen per Equation 1 for peak current, plus additional margin:

$$I_{SAT}(I_{LOAD} + 0.5 \times I_{RIPPLE}) \times 1.2 \quad (1)$$

For ADAS applications, it is recommended that all ceramic capacitors use X7R dielectric material, which ensures minimum capacitance variation over the full temperature range. The voltage rating of the capacitors must be greater than the maximum voltage they could see and twice the typical voltage seen to avoid DC bias effects. The amount of output capacitance used depends on output ripple and transient response requirements, and there are many equations and tools available online to help estimate these. Supplies in this solution were designed for a ±2.5% total transient response. Low ESR ceramic capacitors were used exclusively to reduce ripple. For internally compensated supplies, see device specific datasheets as they may have limitations on acceptable LC output filter values.

ICs must always be qualified per AECQ100. TI parts that are qualified will typically end their part numbers with '-Q1'.

For improved accuracy, all feedback resistor dividers should use components with 1% or better tolerance.

0-Ω resistors are used at the input and output of all the supplies for testing purposes only and could be removed if need in a production board.

2.3.2.7 LP8731-Q1 I²C Interface

The LP8731-Q1 integrates two DC-DC converters and two LDOs, and is used to generate the core voltages for the DSP and EVE co-processor onboard the TDA3x as well as two lower power rails. The device is optimized for size, eliminating most external components. Rather than using external resistor dividers to set output voltages, the device comes with pre-set values, which are then adjustable through an I²C interface. The default values are 1.06 V for the DC-DCs, 2.8 V for LDO1, and 3.3 V for LDO2.

Unfortunately, the LDO voltages do not match what is needed in this design, and must be programmed after power (see the LP8731-Q1 product page for a configuration GUI). However, customers wishing to order this part in volume can work with TI to order parts with custom voltage settings for their application at no extra cost, as this is simply controlled by OTP settings and not a change to silicon.

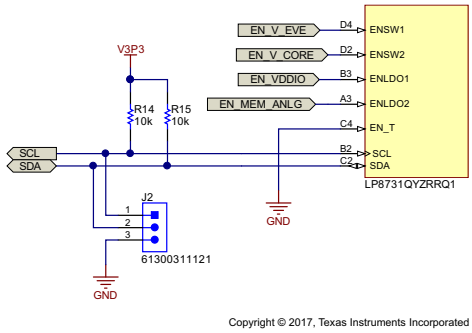


Figure 11. LP8731-Q1 I²C Interface

2.4 TPS54116-Q1 VDDQ DDR Regulator

The TPS54116 was chosen for this design for its ease of implementation and small package size that integrates a complete automotive qualified DDR Memory solution including the VTT Source/Sink Termination LDO. A 1GB, DDR3 solution is need for the design, setting VDDQ = 1.5 V and 1 A while VTT = 0.75 V.

During the design, the switching frequency was set to 2 MHz which reduces the size of the VDDQ rail inductor and keeps the total solution size small. The current mode architecture of the IC simplifies the regulator compensation, cutting down on design time and requiring fewer external components than voltage mode regulators. A current mode scheme also provides fast transient response with minimal output capacitance; requiring only two 22 uF capacitors for the VDDQ rail. Additionally, over current, over voltage, under voltage, and over temperature protections ensure that the TPS54116 and load remain protected in a harsh automotive environment.

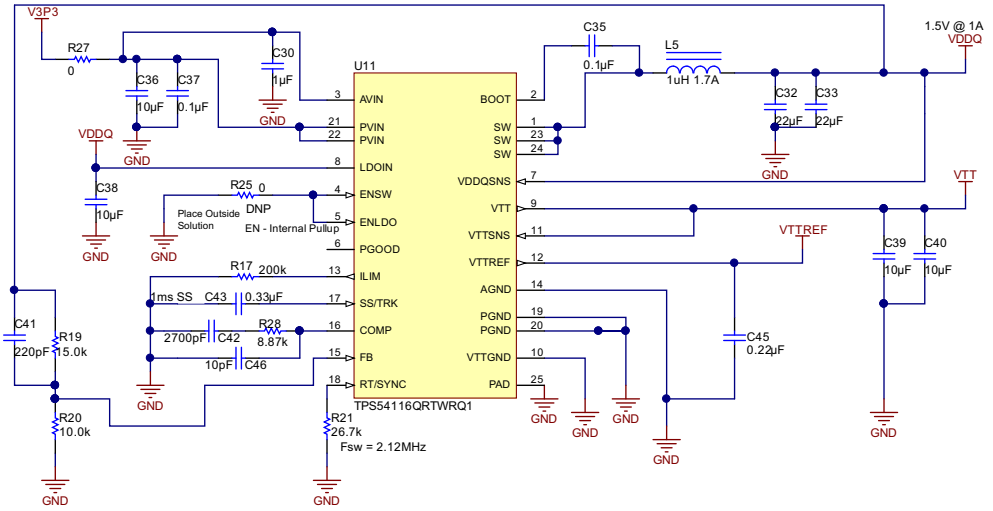


Figure 12. TPS54116-Q1 VDDQ DDR Regulator

3 Getting Started Hardware and Software

3.1 Getting Started Hardware

To get started with the TIDA-00530 board, simply connect leads (recommended using at least 15 AWG) to the two-port screw terminal on the left side of the board. The screw terminals are labeled + and – to indicate the proper polarity of the supply:

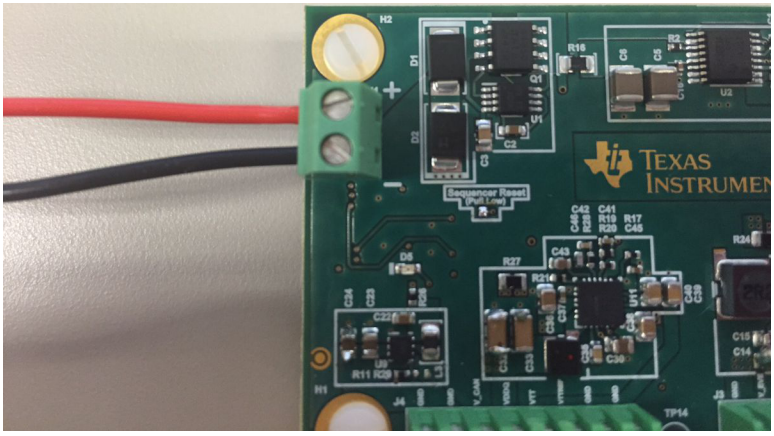


Figure 13. Board Input Terminal

Connect a power supply capable of at least 12 V and 2 A to the leads, and turn it on. After a moment, LED D5 should light up (green), indicating the rails have completed sequencing.

Connect a USB2ANY or other I²C sniffer to the I²C header in the center of the board and see Section 4 for instructions on how to properly set the output voltages of the LP8731-Q1.

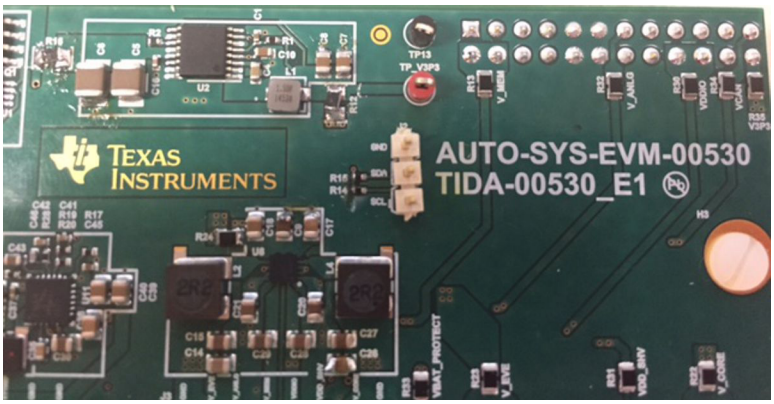


Figure 14. I²C Header

Verify that all output voltages are correct with a multi-meter before connecting to another board. Loads can be connected to each output through the screw terminals along the bottom of the board, which are labeled accordingly:

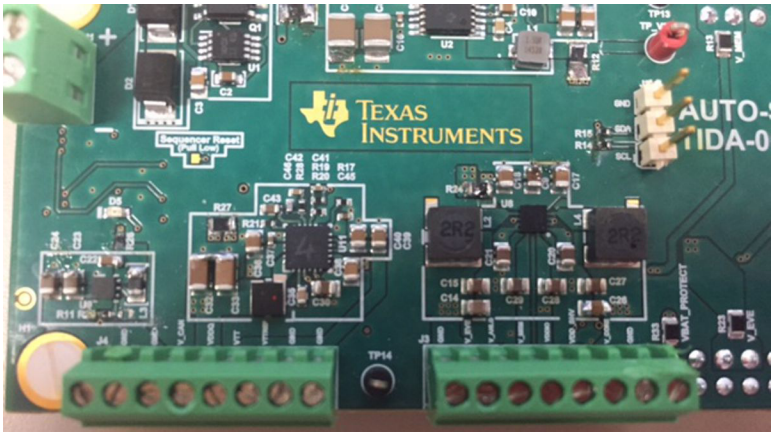


Figure 15. Screw Terminals for Supply Outputs

0-Ω resistors are available on the board to isolate individual devices if that is desired, such as for efficiency measurements. See Section 5 for more details on the schematic and layout of this TI Design. Locations of the 0-Ω resistors are highlighted in yellow in Figure 16:

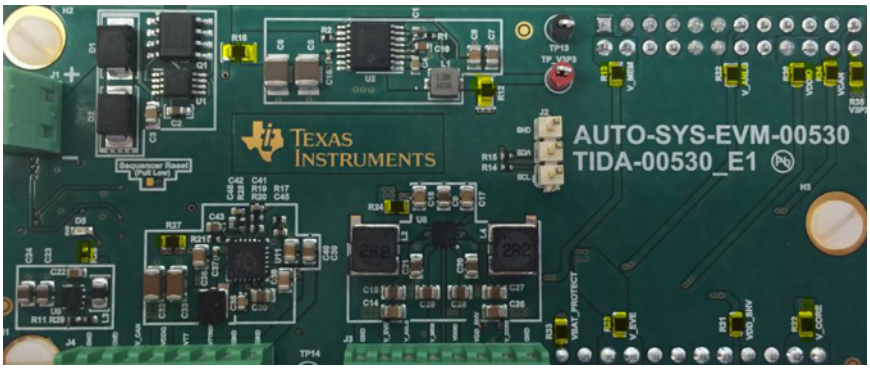


Figure 16. 0-Ω Resistors for Isolating Supplies

3.2 Getting Start Software

The only software required to work with the TIDA-00530 board is the LP8731Q1 Evaluation Program (see Section 6).

Once the system is powered up, connect the USB2ANY's I^2C interface onto the TIDA-00530 I^2C header in the center of the board. Start the LP8731Q1 Evaluation Program:

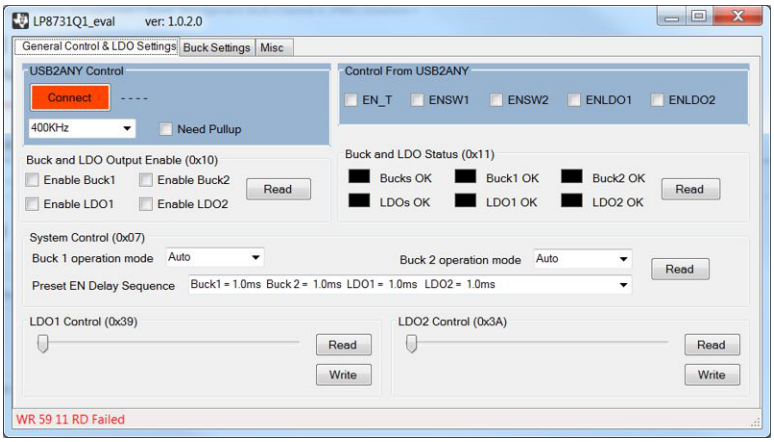


Figure 17. LP8731-Q1 Evaluation Software

The *Connect* button in the top left should turn green after a moment. If not, try clicking *Connect*. If it still fails to connect to the board, ensure that "400 kHz" is selected, and verify physical connections.

Use the software to set the correct output voltages for the LP8731 as well as other settings. The voltages of the LDO voltages can be set using the sliders along the bottom of the first tab, and the DC-DCs can be set on the second tab, "Buck Settings":

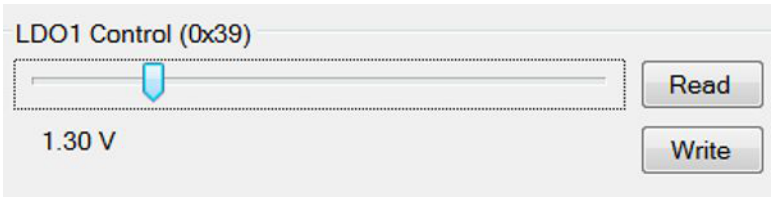


Figure 18. LDO Settings

Figure 19. Buck Settings

Set each supply to the proper voltage and click *Write* to execute the change. Use the following settings:

- LDO1: 1.8 V
- LDO2: 1.2 V
- Buck1: 1.0625 V
- Buck2: 1.0625 V

4 Testing and Results

The following diagrams show how to set up for various tests.

4.1 Ripple and Thermal Image Setup

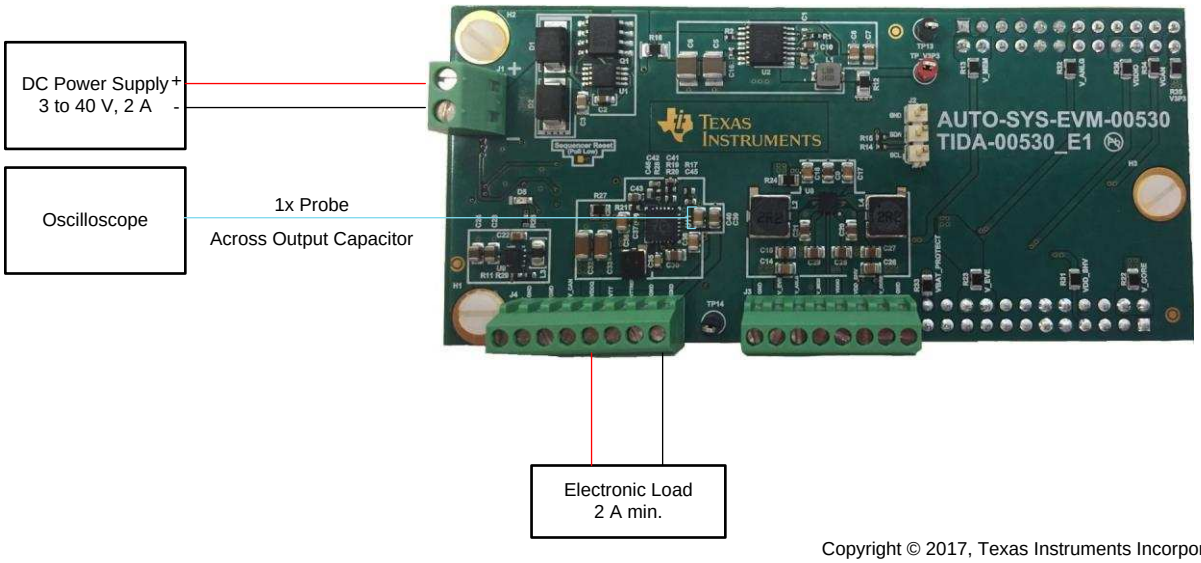


Figure 20. DC-DC Converter Output Voltage Ripple and Thermal Measurement Setup

4.2 Load Transient Setup

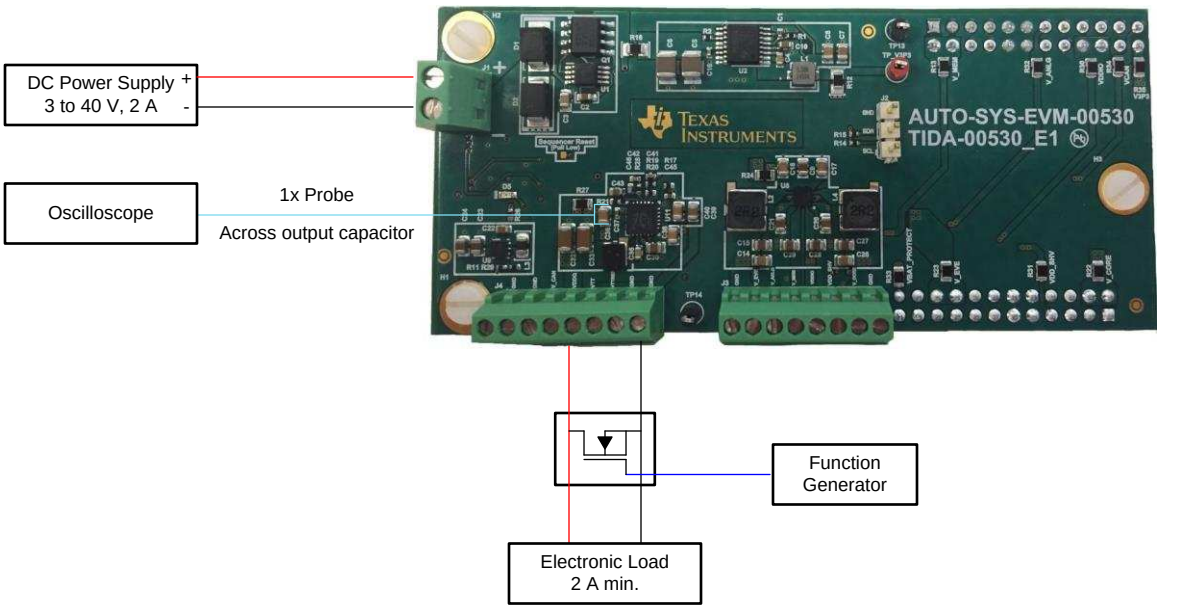


Figure 21. Setup for Load Transient Tests

4.3 Efficiency Setup

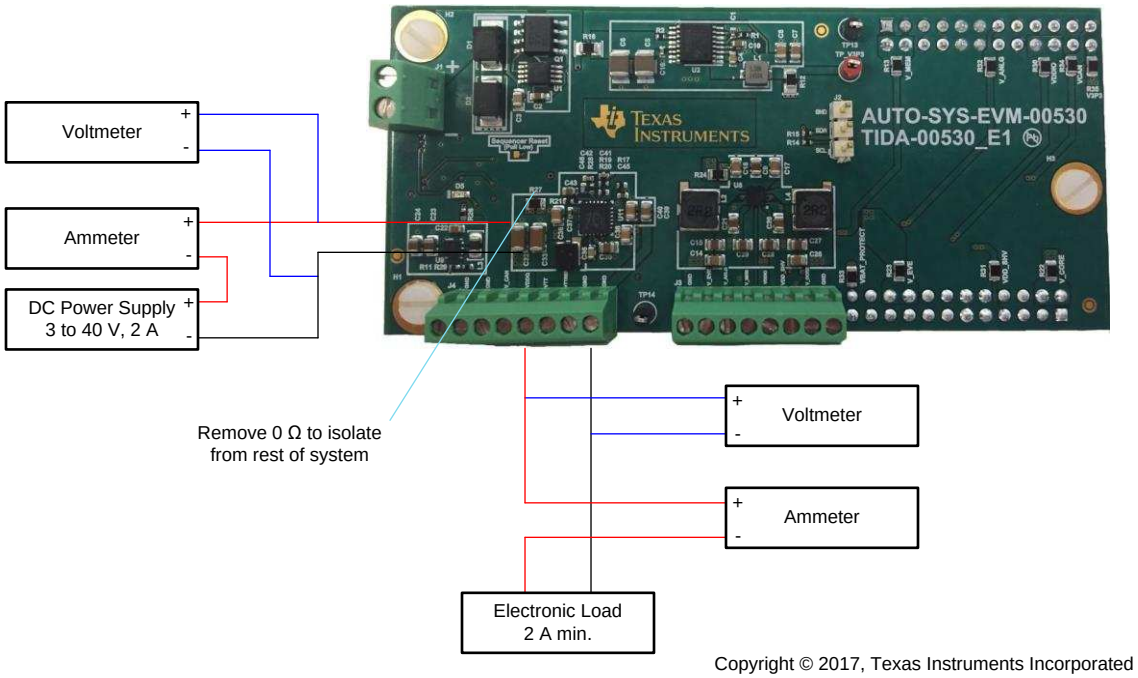


Figure 22. DC-DC Efficiency Measurement Setup

4.4 Load Regulation Setup

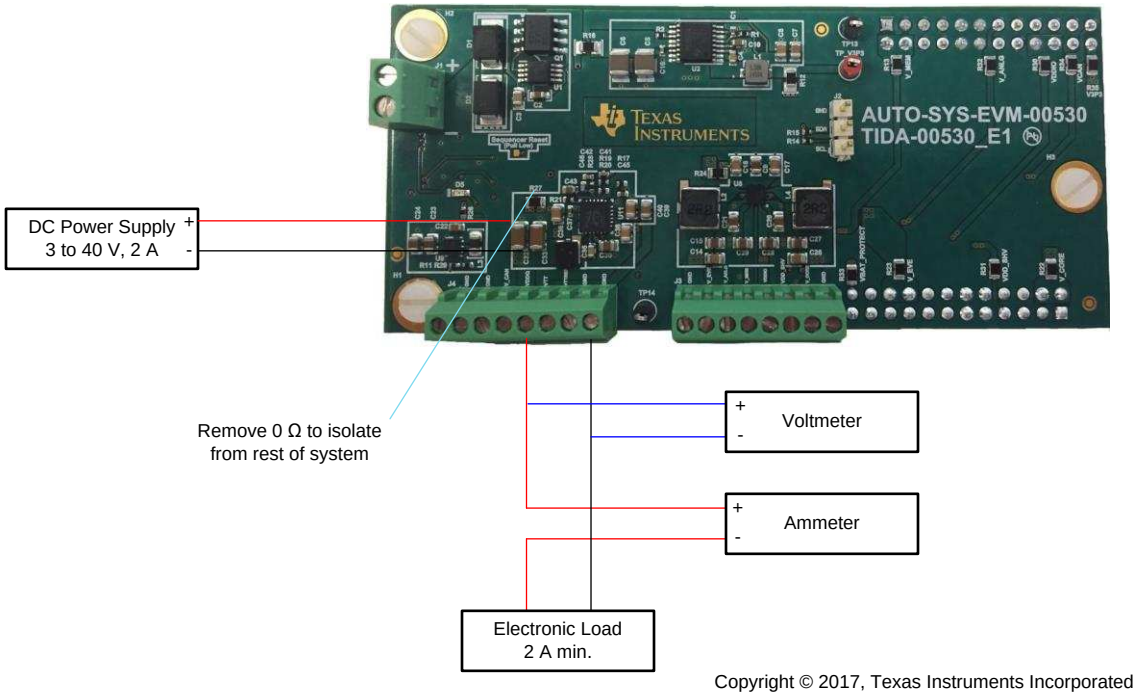


Figure 23. Load Regulation Measurement Setup

4.5 Input Transient Setup

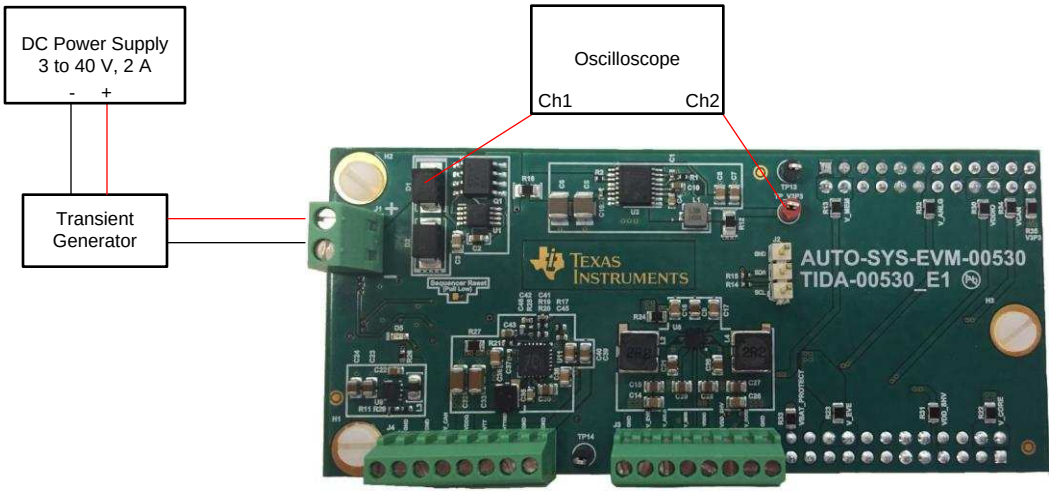


Figure 24. Electrical Transient Setup (NSG 550 Used for Transient Generator)

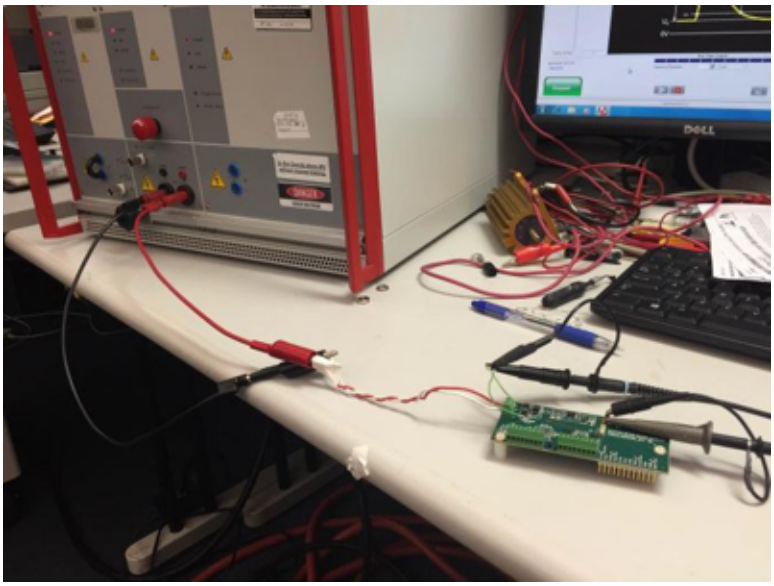


Figure 25. Picture of Setup for Transient Tests

To work with the NSG 5500, also use the Teseq AutoStar software, which has pre-defined pulses that the user can tweak to meet specific requirements. Figure 26 shows an example:

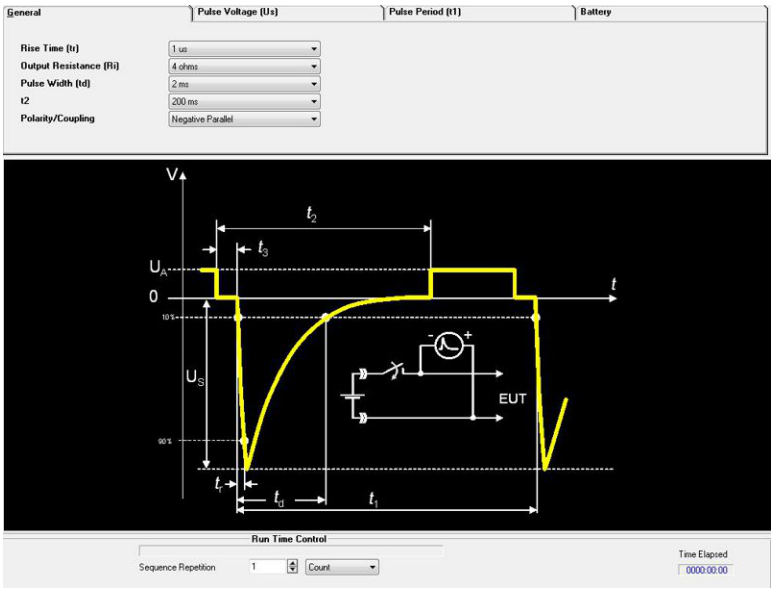


Figure 26. AutoStar Setup for Pulse 1

4.6 Test Data

The following sections show the test data from characterizing the switching power supplies in the system.

4.6.1 DC-DC Efficiency

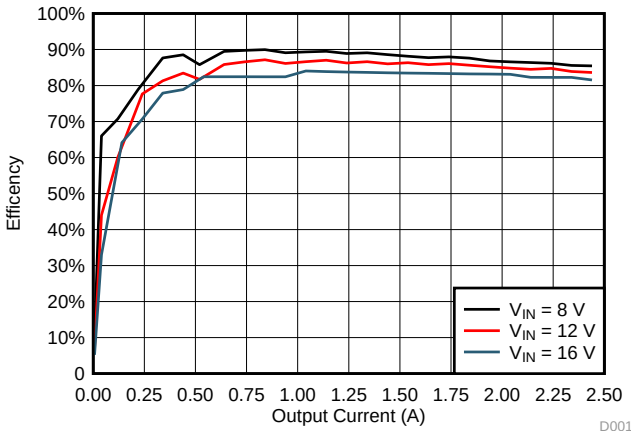


Figure 27. V3P3 Efficiency

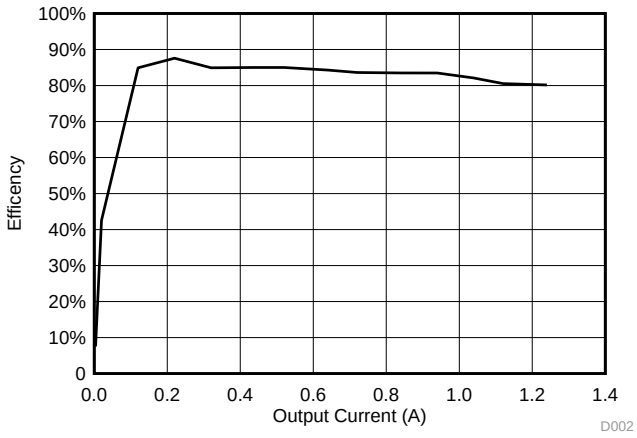


Figure 28. VEVE Efficiency (V_{IN} = 3.3 V)

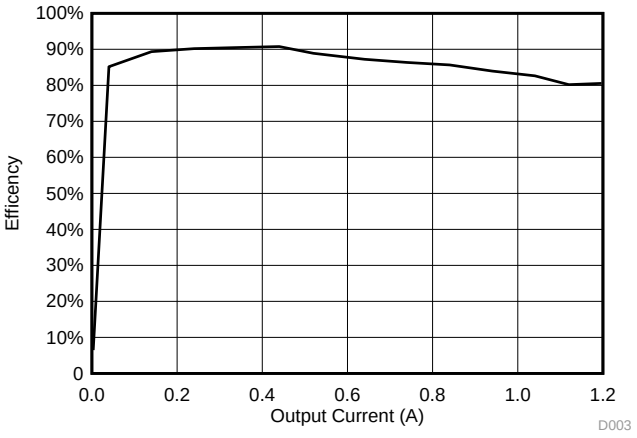


Figure 29. VCORE Efficiency (V_{IN} = 3.3 V)

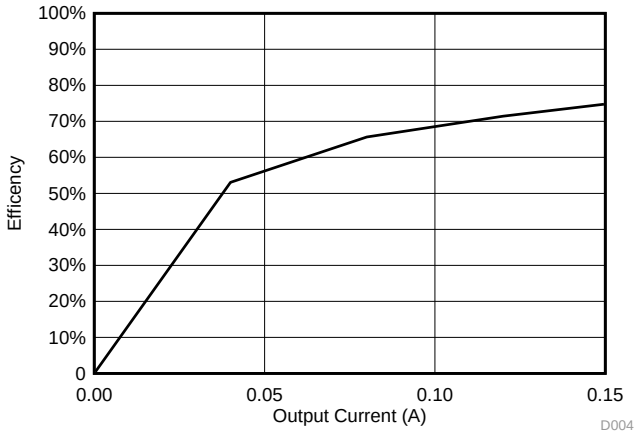


Figure 30. VCAN Efficiency (V_{IN} = 3.3 V)

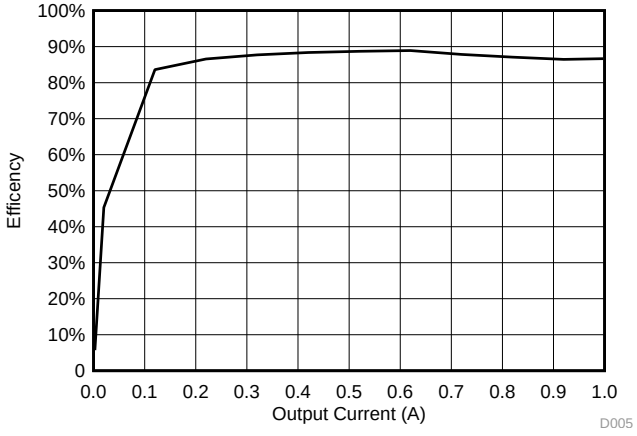


Figure 31. VDDQ Efficiency (V_{IN} = 3.3 V)

4.6.2 Load Regulation

The following results show the percent deviation from nominal output voltage as a function of output current.

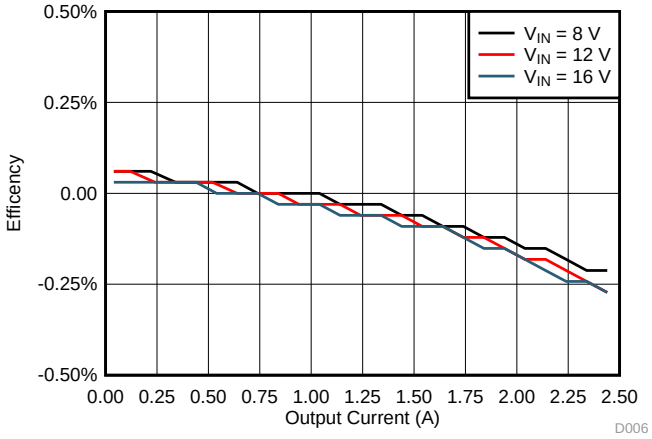


Figure 32. V3PV Load Regulation 0 to 2.5 A, 8 to 16 V_{IN}

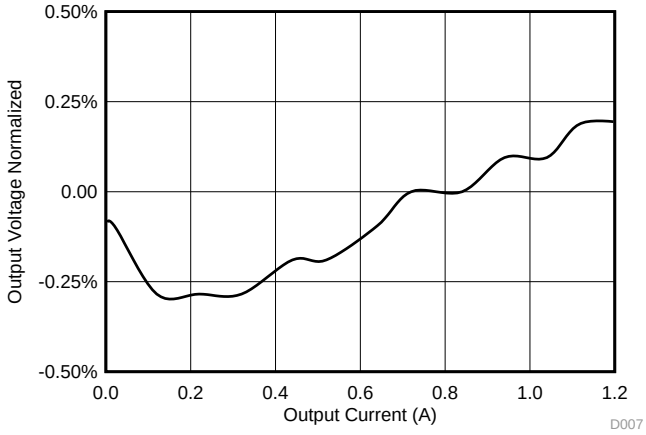


Figure 33. VEVE Load Regulation 0 to 1.2 A (V_{IN} = 3.3 V)

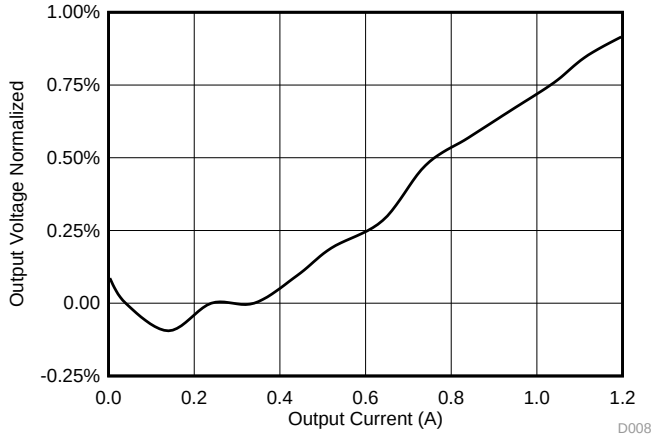


Figure 34. VCORE Load Regulation 0 to 1.2 A (V_{IN} = 3.3 V)

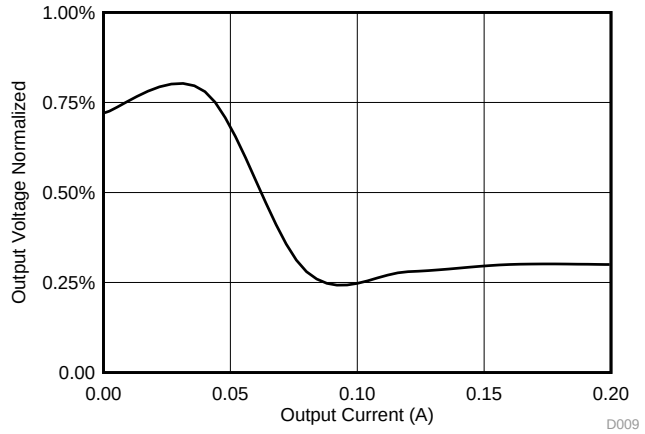


Figure 35. VCAN Load Regulation 0 to 0.2 A (V_{IN} = 3.3 V)

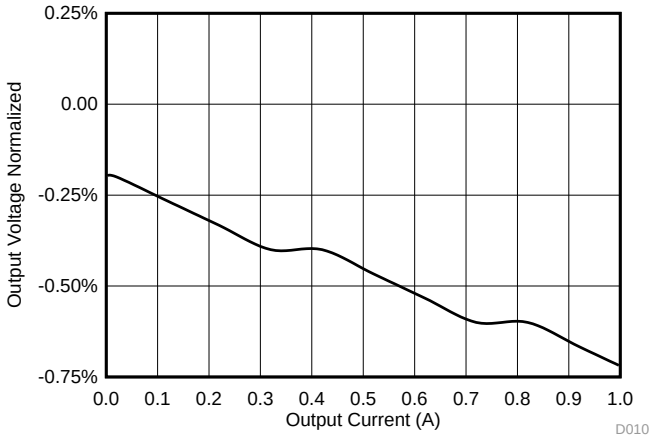


Figure 36. VDDQ Load Regulation 0 to 1 A (V_{IN} = 3.3 V)

4.6.3 Start-up Sequencing Waveforms

The following images show the sequencing of relevant supplies during power-up.

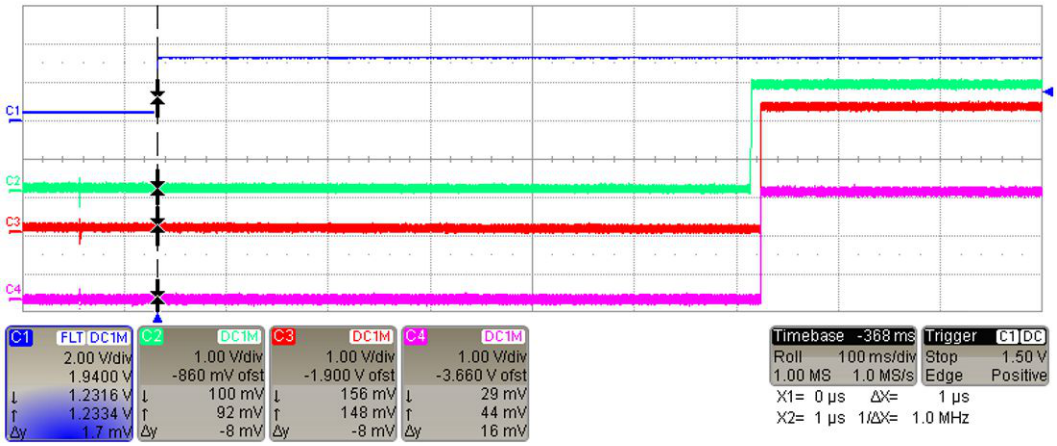


Figure 37. Startup Waveform 1

CH1: V3P3

CH2: VDDIO

CH3: VDDQ

CH4: V_ANLG

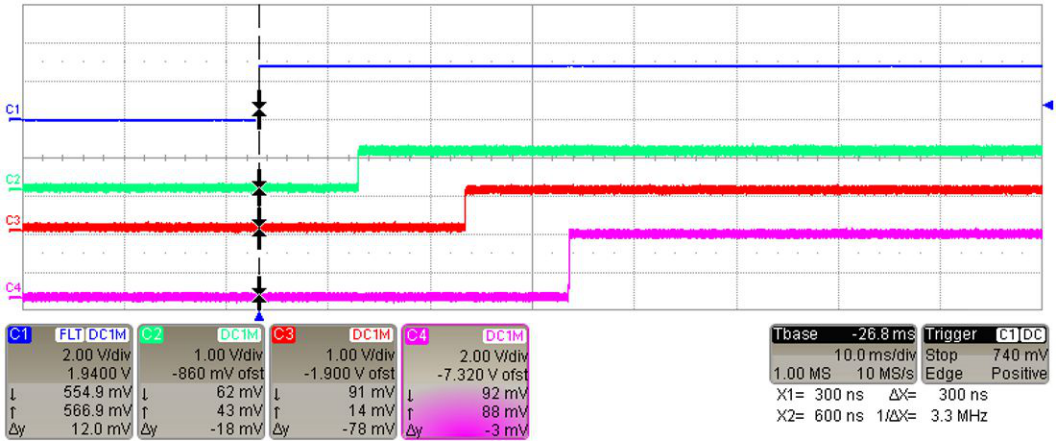


Figure 38. Startup Waveform 2

CH1: V_ANLG

CH2: V_CORE

CH3: V_EVE

CH4: VDD_SHV

4.6.4 Power-Down Sequencing Waveforms

The following images show the sequencing of relevant supplies during power down.

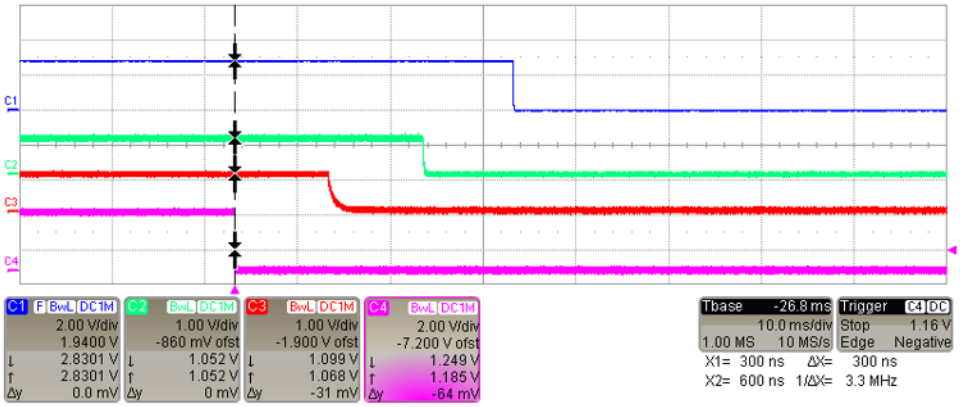


Figure 39. Shutdown Waveform 1

CH1: VDD_SHV

CH2: V_EVE

CH3: V_CORE

CH4: V_ANLG

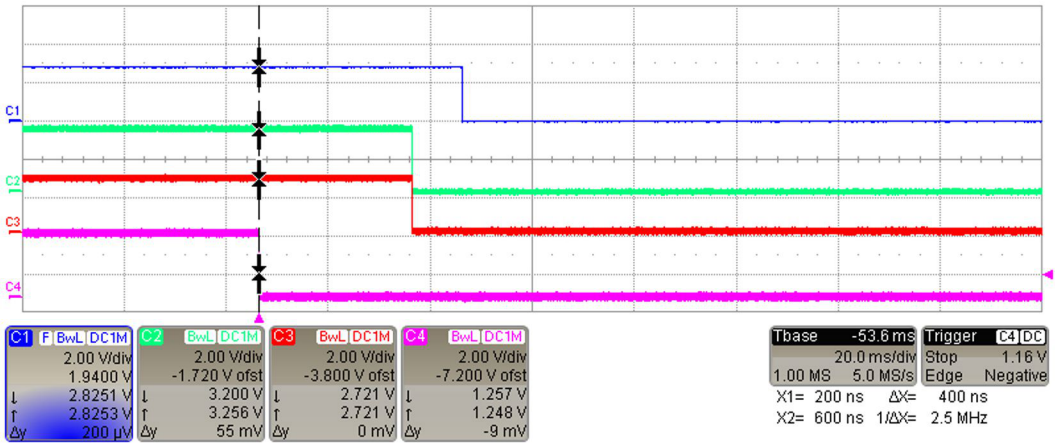


Figure 40. Shutdown Waveform 2

CH1: V_CORE

CH2: V_ANLG

CH3: VDDQ

CH4: VDDIO

4.6.5 DC-DC Output Voltage Ripple

The following images show the output voltage ripple at full load of each DC-DC converter. Where possible, the switch node is also shown (V_{IN} = 12 V).

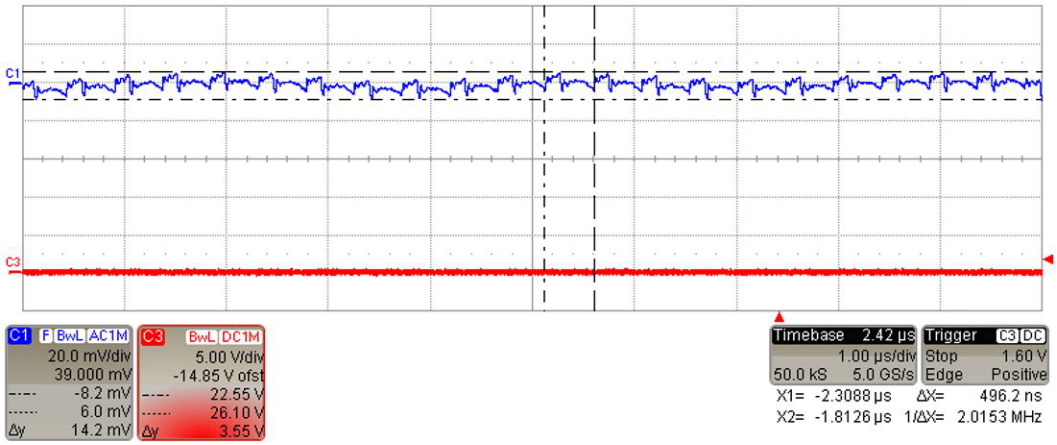


Figure 41. V3P3, VOUT = 3.3V, IOUT = 2.5A

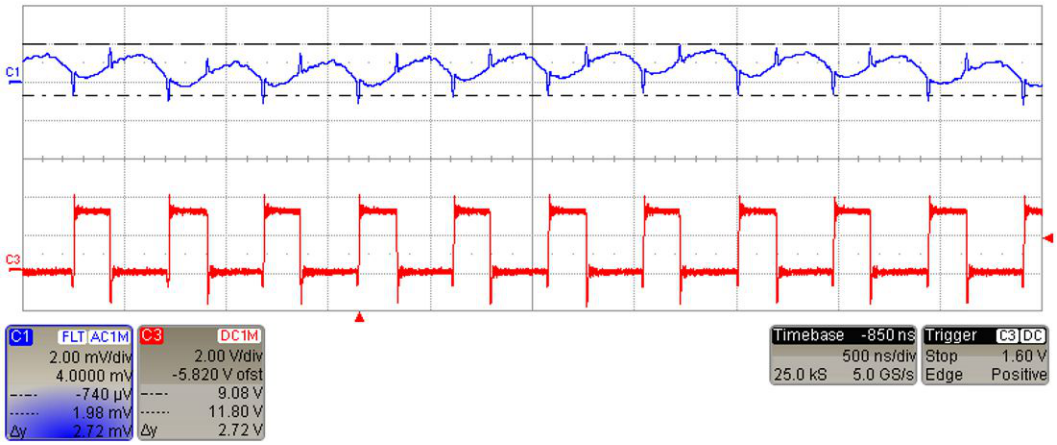


Figure 42. V_EVE, VOUT = 1.06V, IOUT = 1.2A

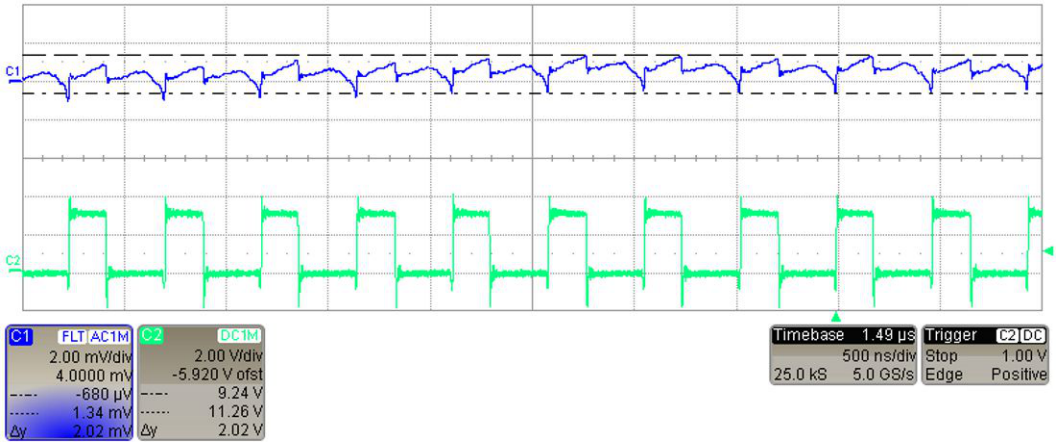


Figure 43. V_CORE, VOUT = 1.06V, IOUT = 1.2A

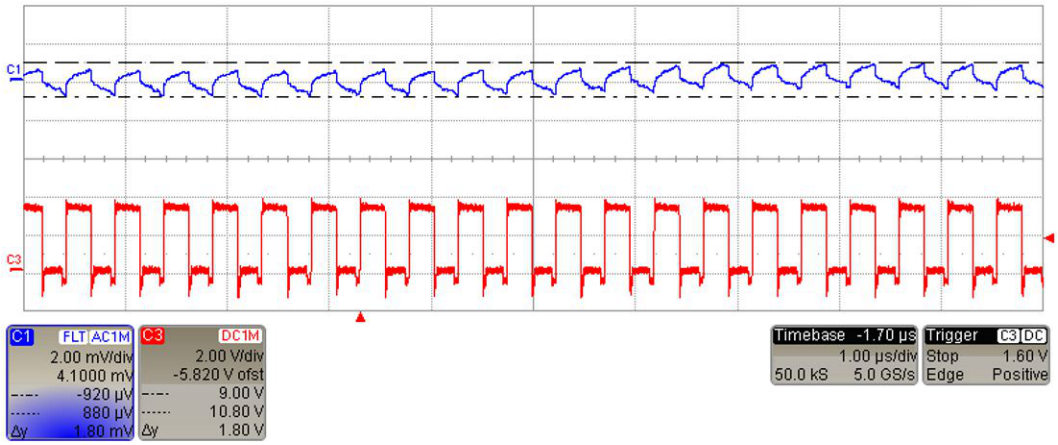


Figure 44. VDDQ, VOUT = 1.5V, IOUT = 1A

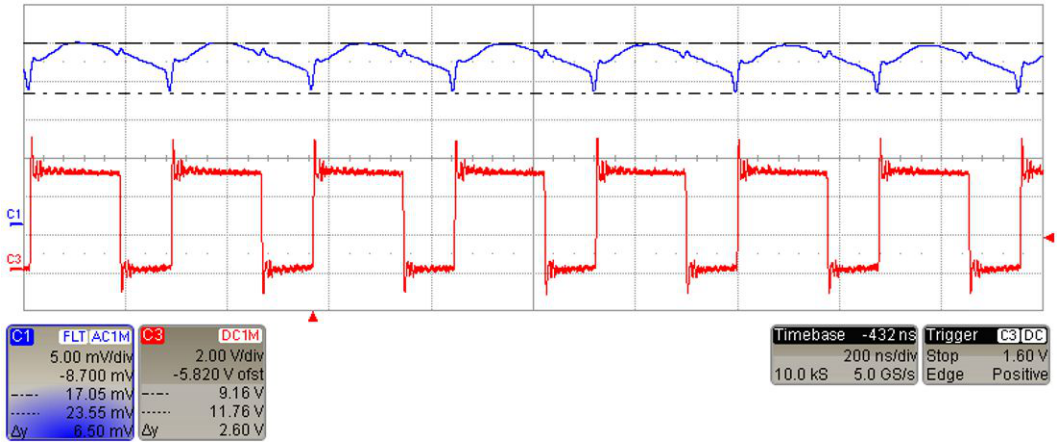


Figure 45. V_CAN, VOUT = 5V, IOUT = 200mA

4.6.6 DC-DC Load Transients

The following images show the transient response for both load step and release at 25% of full load.

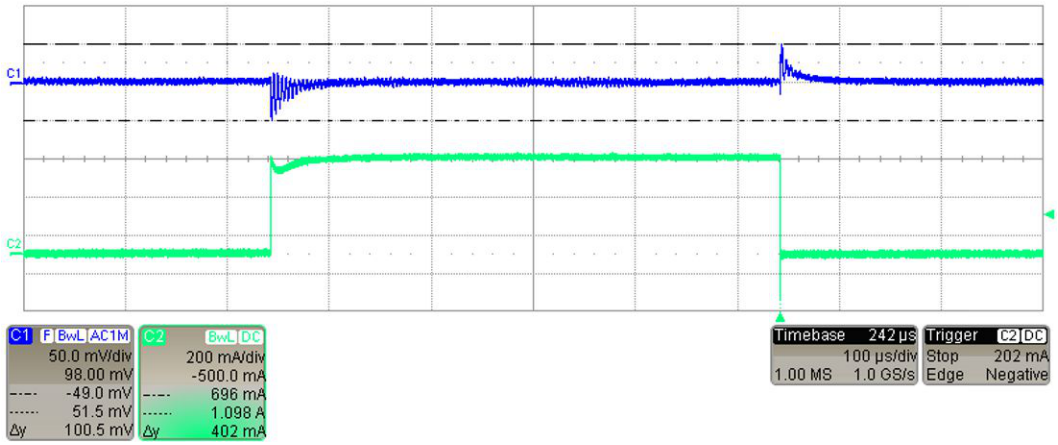


Figure 46. V3P3, VOUT = 3.3 V, IOUT_STEP = 500 mA

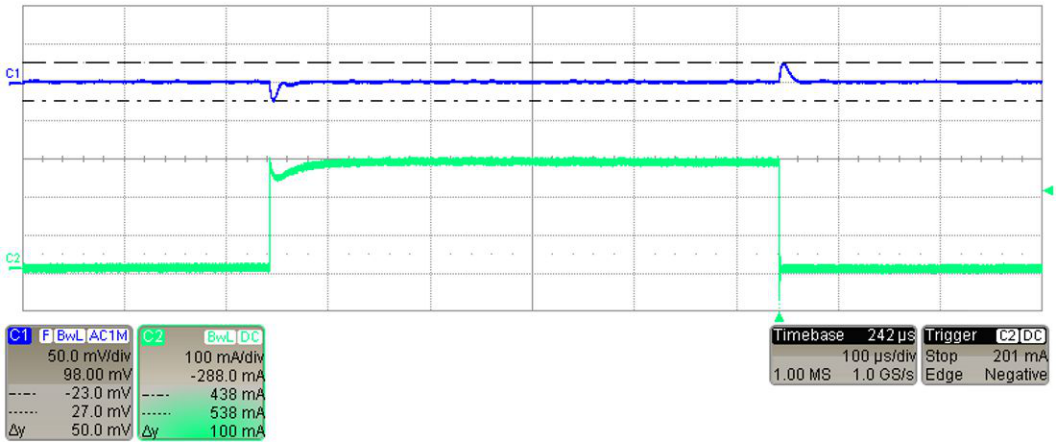


Figure 47. V_EVE, VOUT = 1.06 V, IOUT_STEP = 300 mA

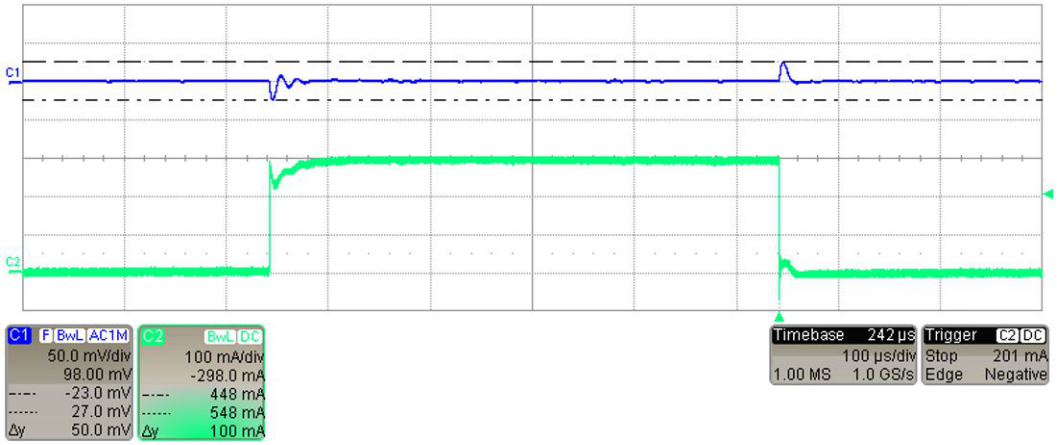


Figure 48. V_CORE, VOUT = 1.06 V, IOUT_STEP = 300 mA

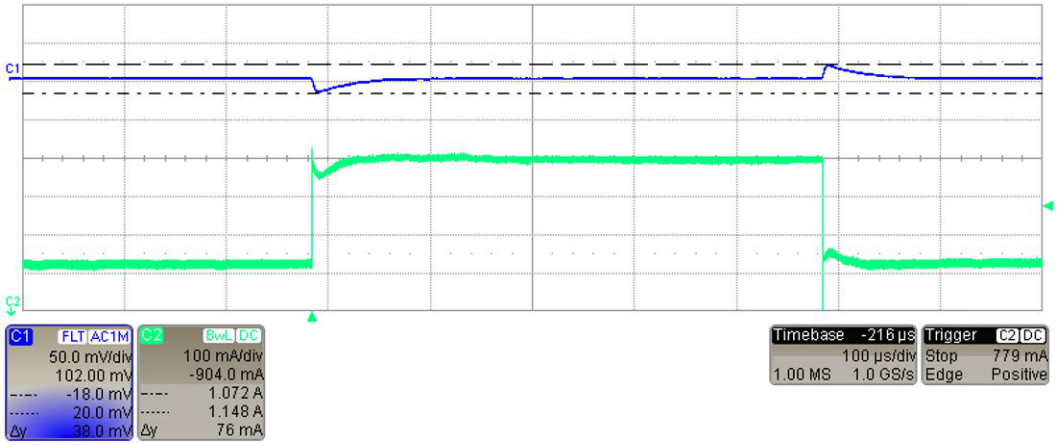


Figure 49. VDDQ, VOUT = 1.5 V, IOUT_STEP = 250 mA

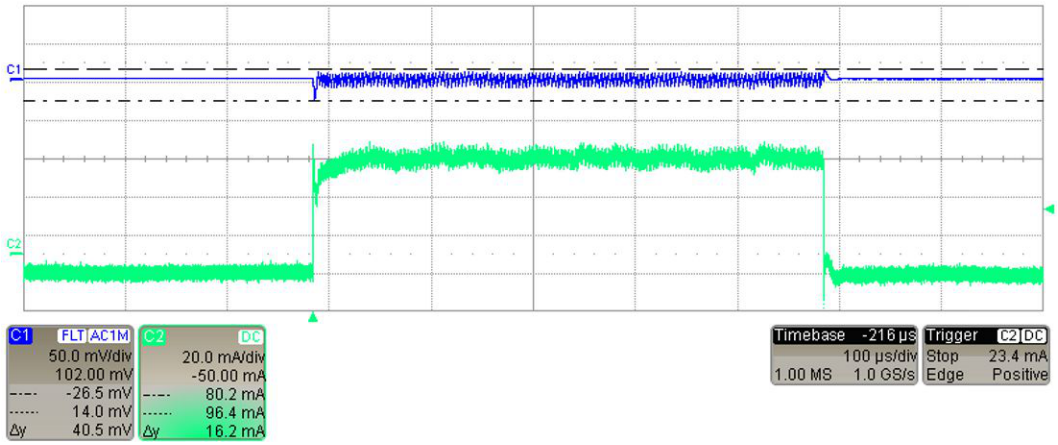


Figure 50. V_CAN, VOUT = 5 V, IOUT_STEP = 50 mA

4.6.7 Thermal Images

The following images show the temperature rise of the different components on the board under various load conditions.

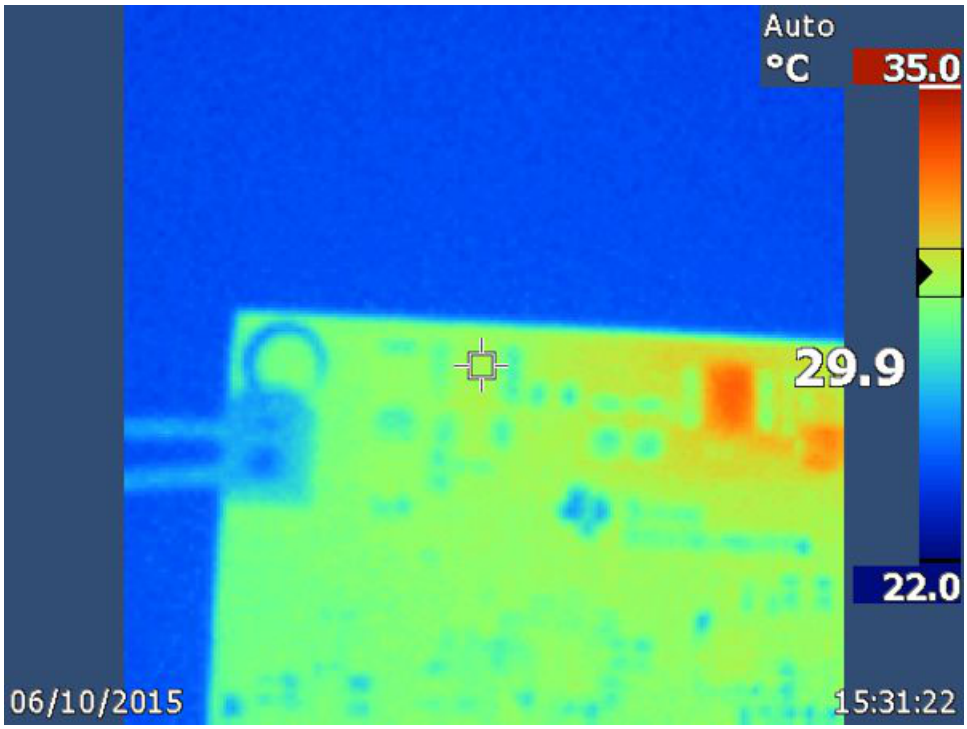


Figure 51. LM74610 (Reverse Polarity Protection) FET, No Load, Steady State

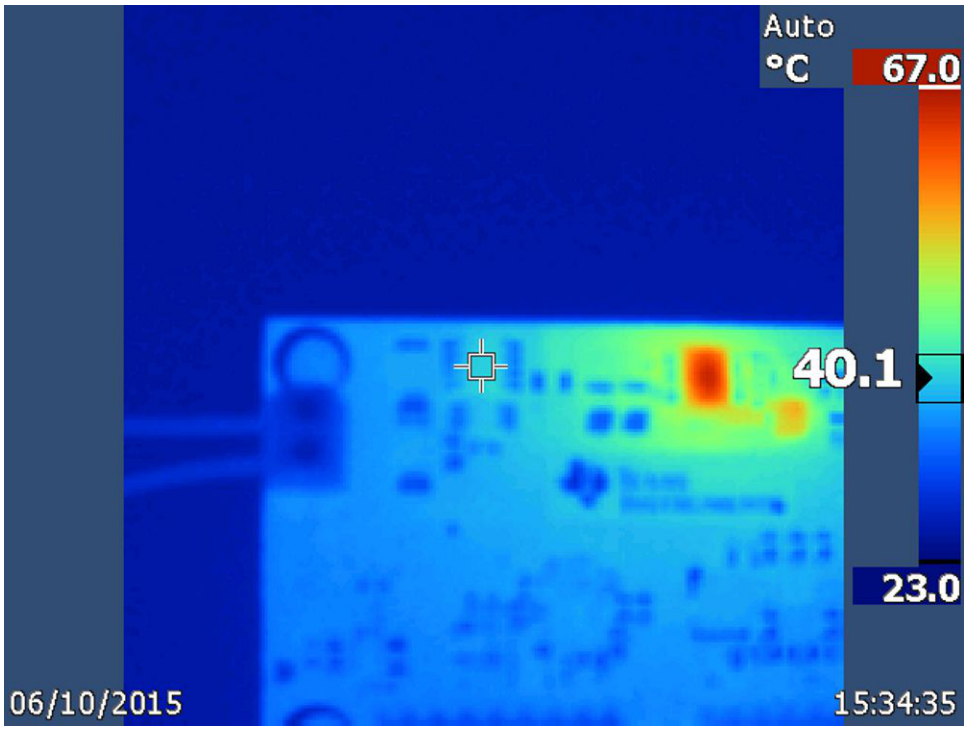


Figure 52. LM74610 (Reverse Polarity Protection) FET, Full Board Load, Steady State

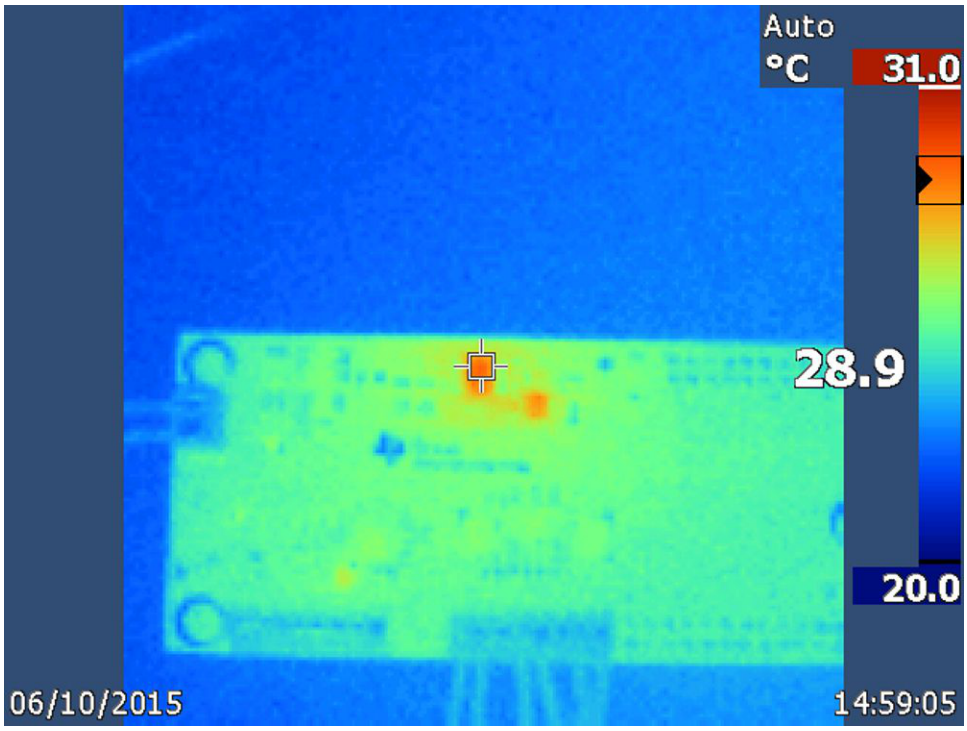


Figure 53. LM53603 (Wide-VIN Buck) IC, No Load, Steady State

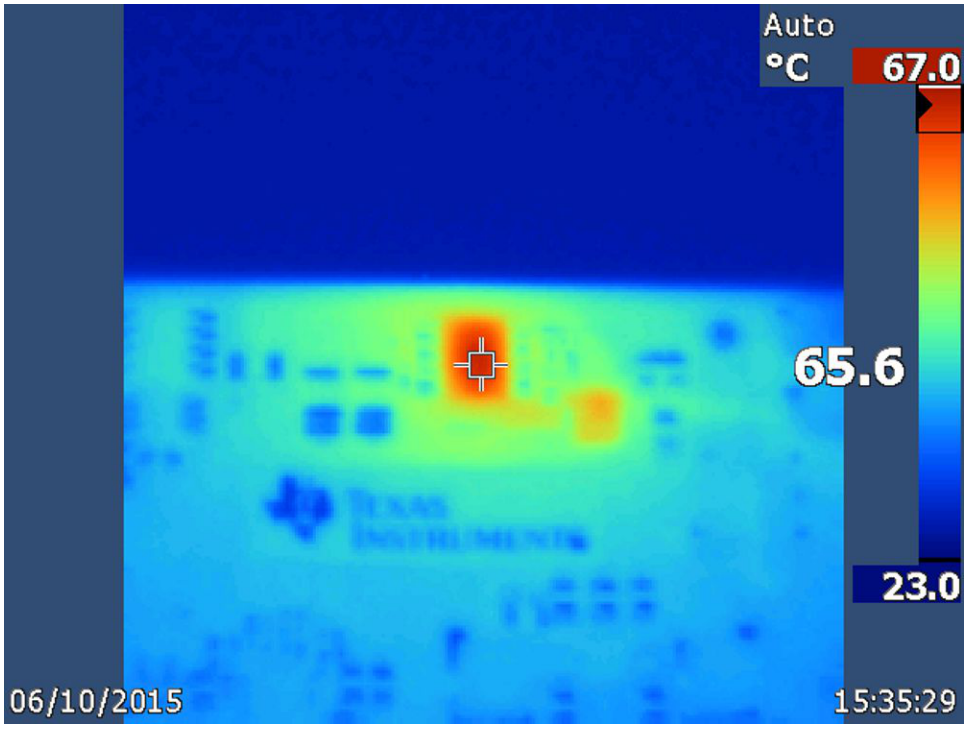


Figure 54. LM53603 (Wide-VIN Buck) IC, Full Load, Steady State

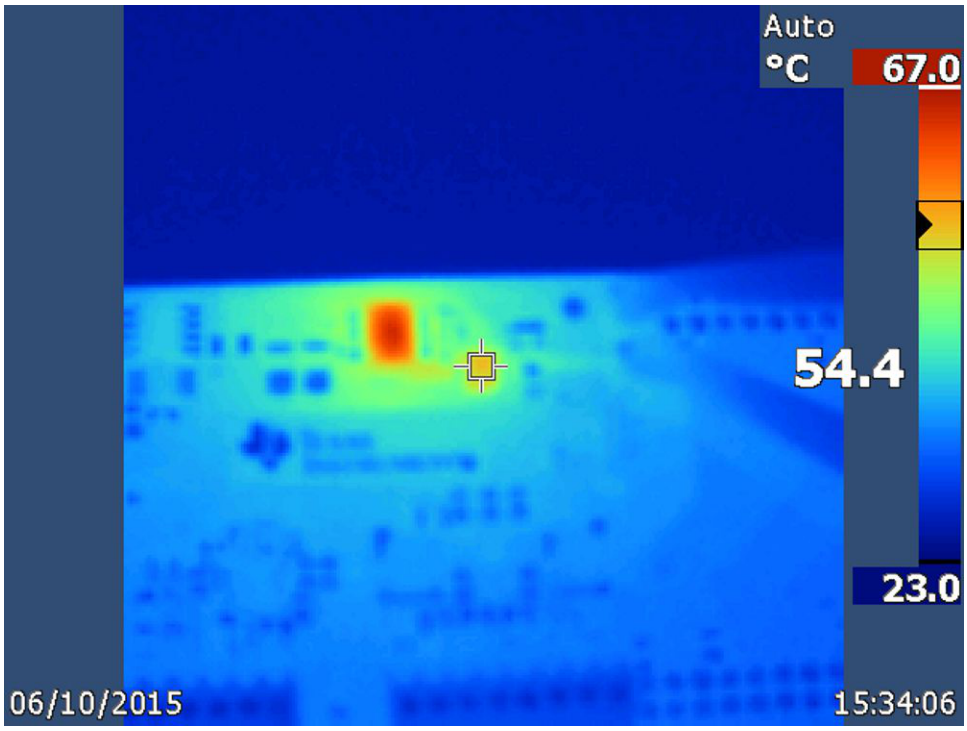


Figure 55. LM53603 (Wide-VIN Buck) Inductor, Full Load, Steady State

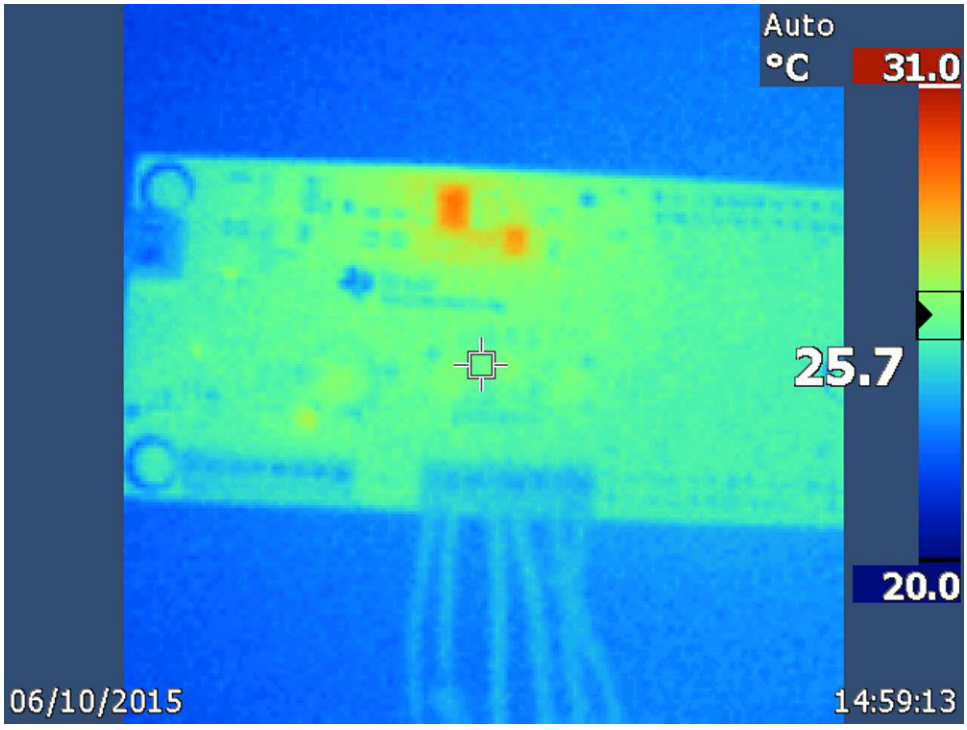


Figure 56. LP8731 IC, No Load, Steady State

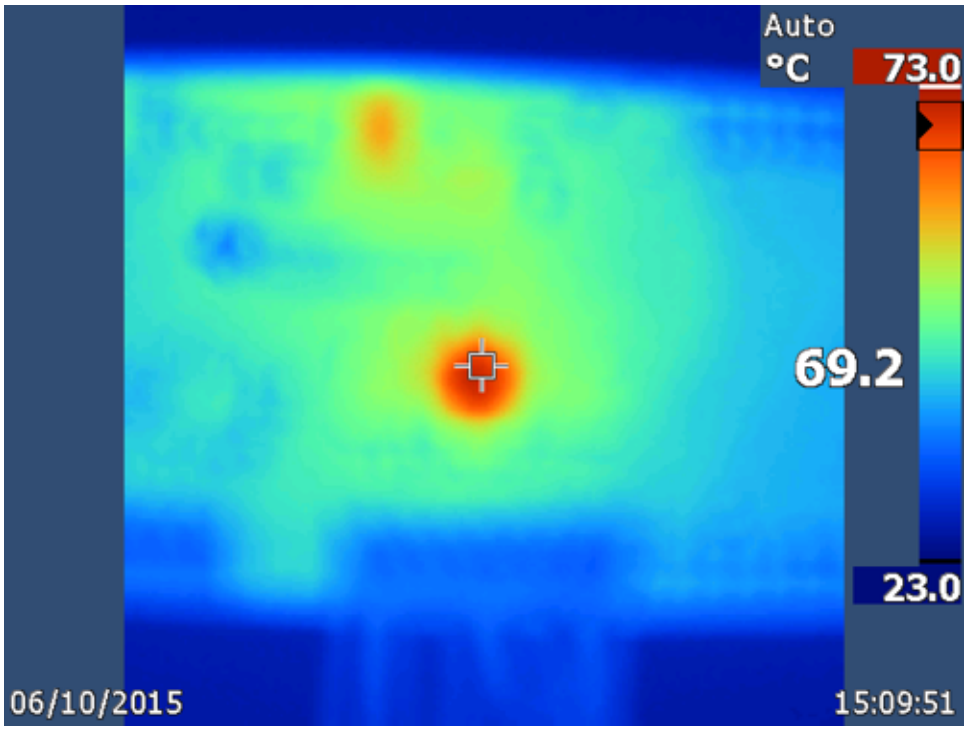


Figure 57. LP8731 IC, All Four Rails Full Load, Steady State

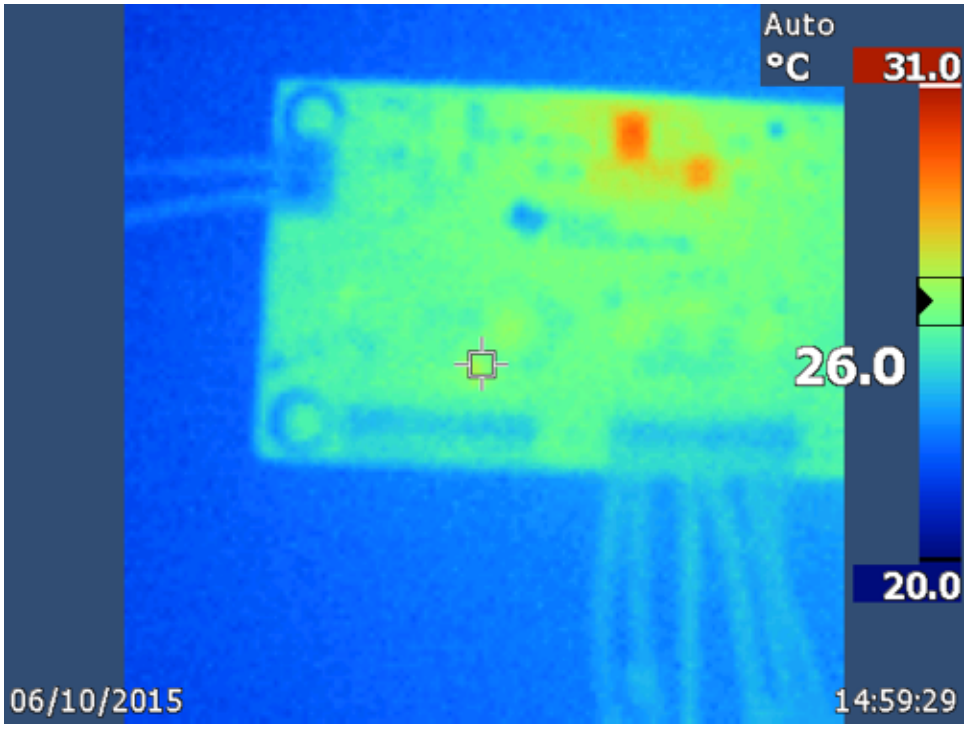


Figure 58. TPS54116-Q1 IC, No Load, Steady State

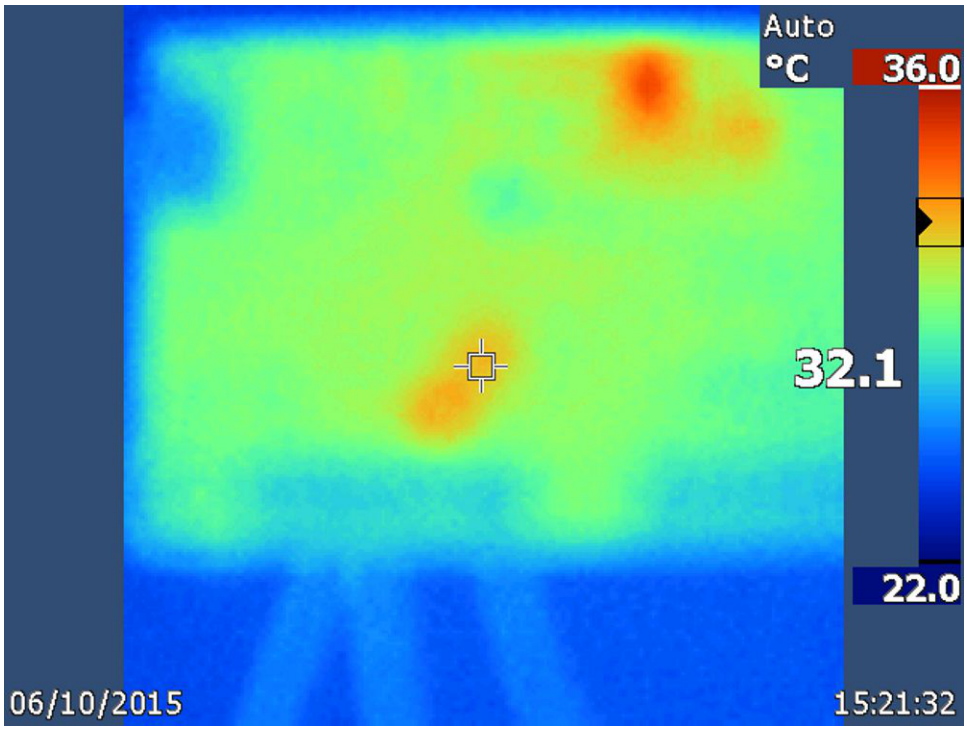


Figure 59. TPS54116-Q1 IC, Full Load, Steady State

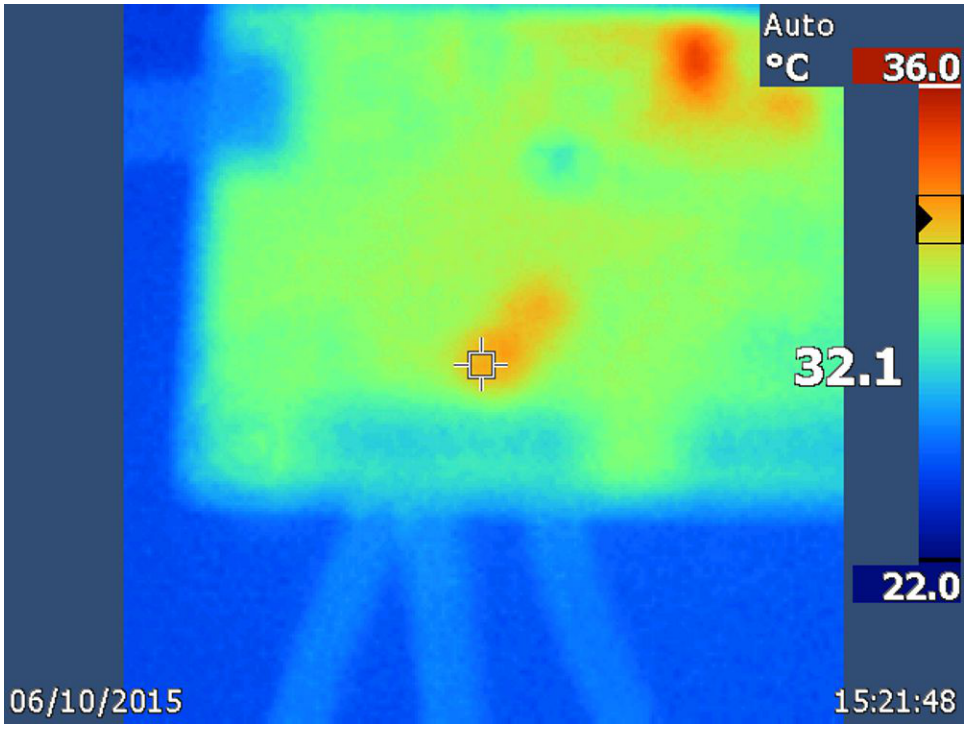


Figure 60. TPS54116-Q1 Inductor, Full Load, Steady State

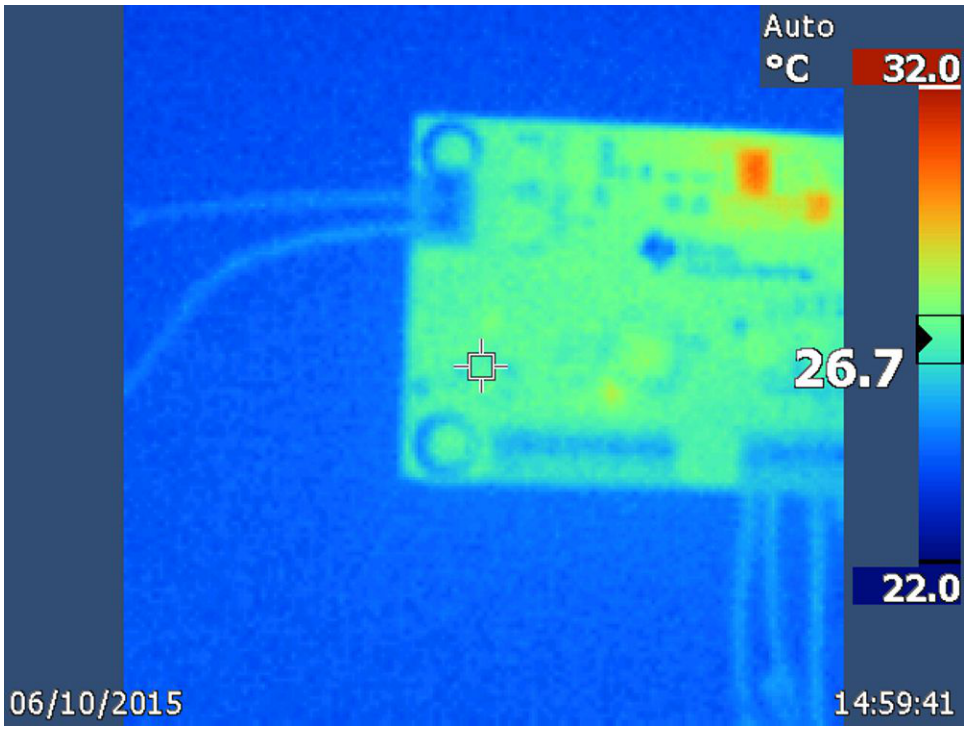


Figure 61. VCAN IC, No Load, Steady State

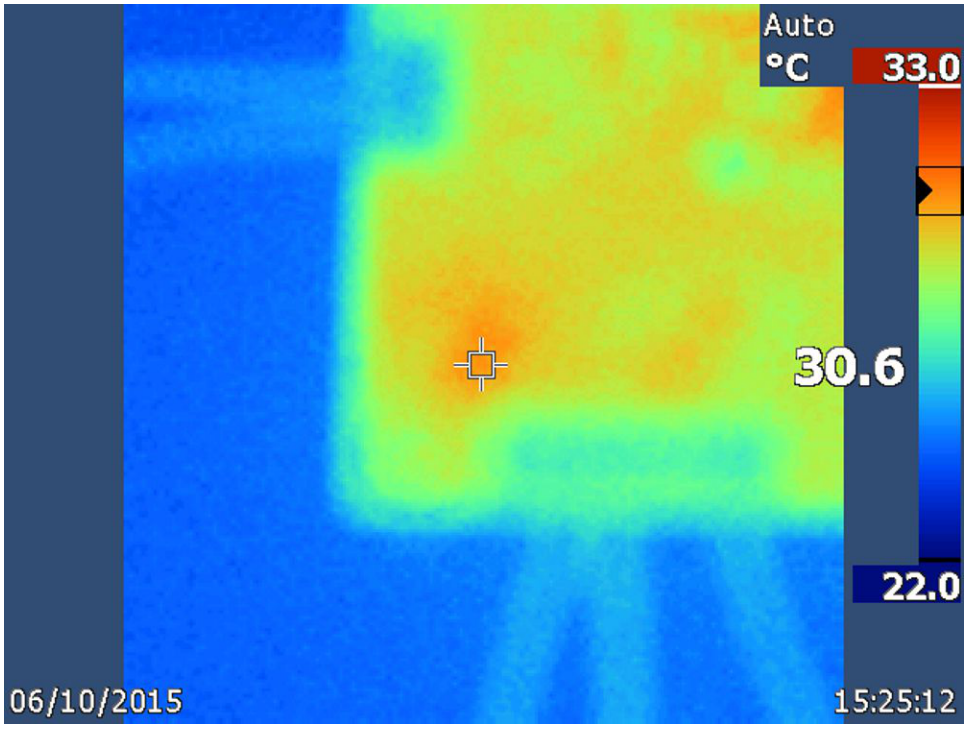


Figure 62. VCAN IC, Full Load, Steady State

4.6.8 Electrical Transient Testing

Three electrical transient test pulses were applied to verify the transient suppression scheme: ISO 7637-2:2004 Pulse 1, 2a, and 5b (clamped or suppressed load dump). A battery DC voltage of 13.5 V is used for all tests. All yellow traces are pulse inputs, and all blue traces are the output of the wide V_{IN} buck converter (LM53603).

4.6.8.1 ISO Pulse 1

Figure 63. Pulse 1 Test Pulse

The pulse was first verified as open circuit using the following parameters:

- V_{MIN} = –100 V (–99.2 V achieved)
- R_{SOURCE} = 4 Ω
- T_{RISE} = 1 µs
- $T_{DURATION}$ = 2 ms

The circuit was then subjected to the ISO 1 pulse while the disturbance to the output of the Wide V_{IN} buck was measured.

Figure 64. TVS Circuit Clamps the Negative Voltage to –20.4 V

Although not shown here, the LM74610 disconnects the circuit from the input within a few µs of the pulse, and the output is sustained by the input capacitors until the supply voltage recovers.

Figure 65. Max Overshoot = 4.2 V Protects Circuits Downstream

Figure 66. Max Undershoot = 2.2 V may be too low for some downstream converters to maintain regulation. Additional hold-up capacitors can be added to those converter inputs in this case.

NOTE: 2.2 V may be too low for some downstream converters to maintain regulation. In this case, additional hold-up capacitors can be added to those converter inputs.

Note that 2.2 V may be too low for some downstream converters to maintain regulation. In this case, additional hold-up capacitors can be added to those converter inputs.

4.6.8.2 ISO Pulse 2a

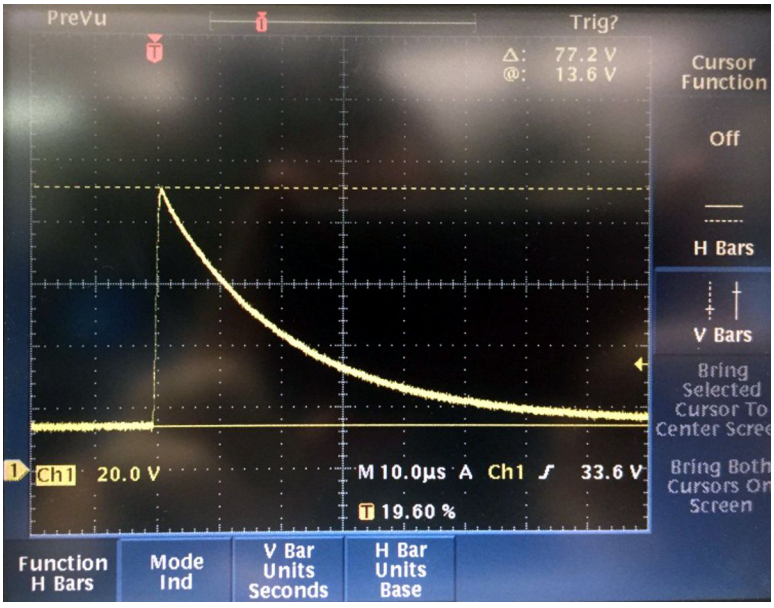


Figure 67. Pulse 2a Test Pulse

This pulse was first verified as open circuit using the following parameters:

- V_{PULSE} = 75 V (77.2 V achieved), superimposed on 13.5-V DC (90.7 V max)
- R_{SOURCE} = 4 Ω
- T_{RISE} = 1 µs
- $T_{DURATION}$ = 2 ms

The circuit was then subjected to the ISO 2a pulse while the disturbance to the output of the wide V_{IN} buck was measured.

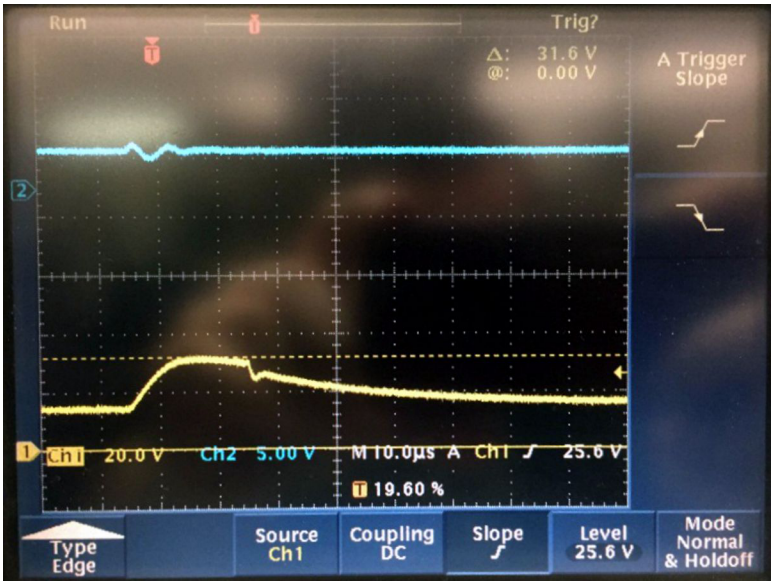


Figure 68. TVS Circuit Clamps Voltage to 31.6 V

The wide V_{IN} buck converter has a maximum transient voltage standoff of 42 V and is protected by the clamp.

Figure 69. Max Overshoot = 4 V Protects Circuits Downstream

Although not shown here with markers, the maximum undershoot is ≈ 2.5 V, which may be too low for some downstream converters to maintain regulation. In this case, additional hold-up capacitors can be added to those converter inputs.

4.6.8.3 ISO Pulse 5b (Clamped Load Dump)

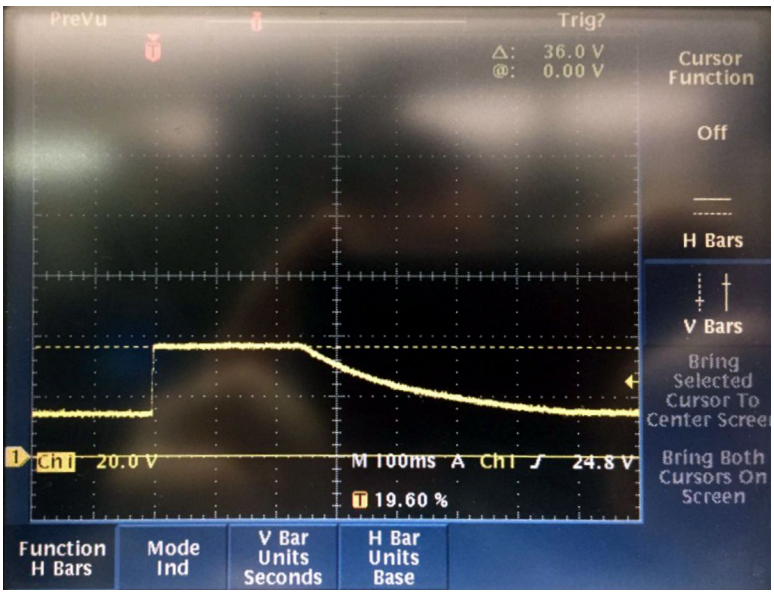


Figure 70. Pulse 5b (Clamped Load Dump) Test Pulse

This pulse was first verified as open circuit using the following parameters:

- V_{PULSE} = 36 V, (22.5 V superimposed on 13.5-V DC)
- R_{SOURCE} = 0.5 Ω
- T_{RISE} = 10 ms
- $T_{DURATION}$ = 400 ms

The circuit was then subjected to the ISO 2a pulse while the disturbance to the output of the wide V_{IN} buck was measured.

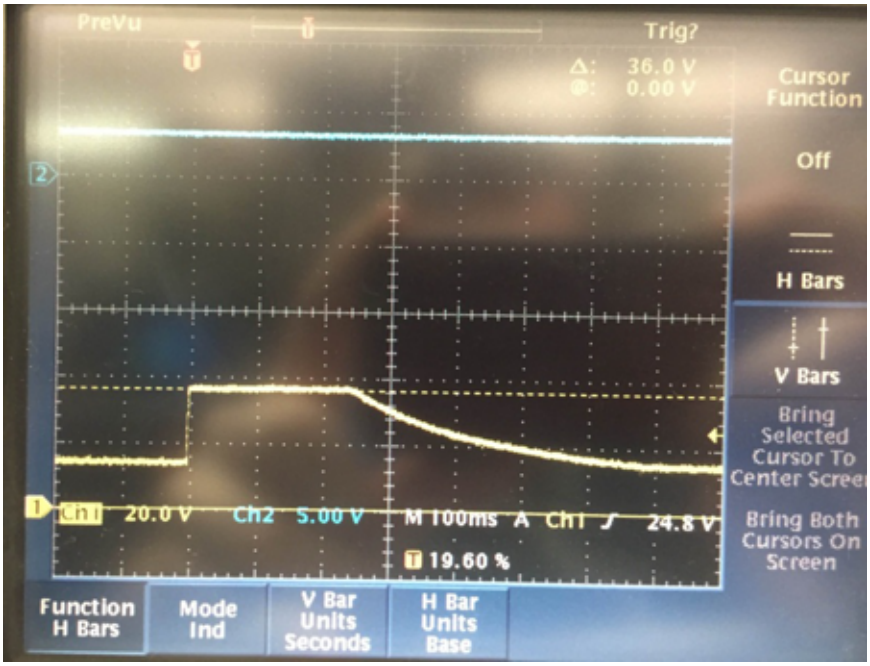


Figure 71. Wide V_{IN} Output Undisturbed During Load Dump Pulse

Although the load dump pulse is quite energetic, it is slow enough that it does not cause any significant line transient effects on the output of the LM53603 because the control loop is quick enough to respond to the rising input voltage. The TVS protection circuit also does not need to clamp this pulse as it is low enough in magnitude not to damage downstream devices.

5 Design Files

To download the design files for this TI Design including the schematic, bill of materials, layer plots, Gerber files, and Altium files, see the TIDA-00530 product page.

5.1 PCB Layout Recommendations

5.1.1 Noise Sensitive Traces and Components

Route voltage feedback (FB) traces away from other noisy traces or components, such as I^2C clock lines. Avoid routing things under the switch node of a power inductor altogether if possible:

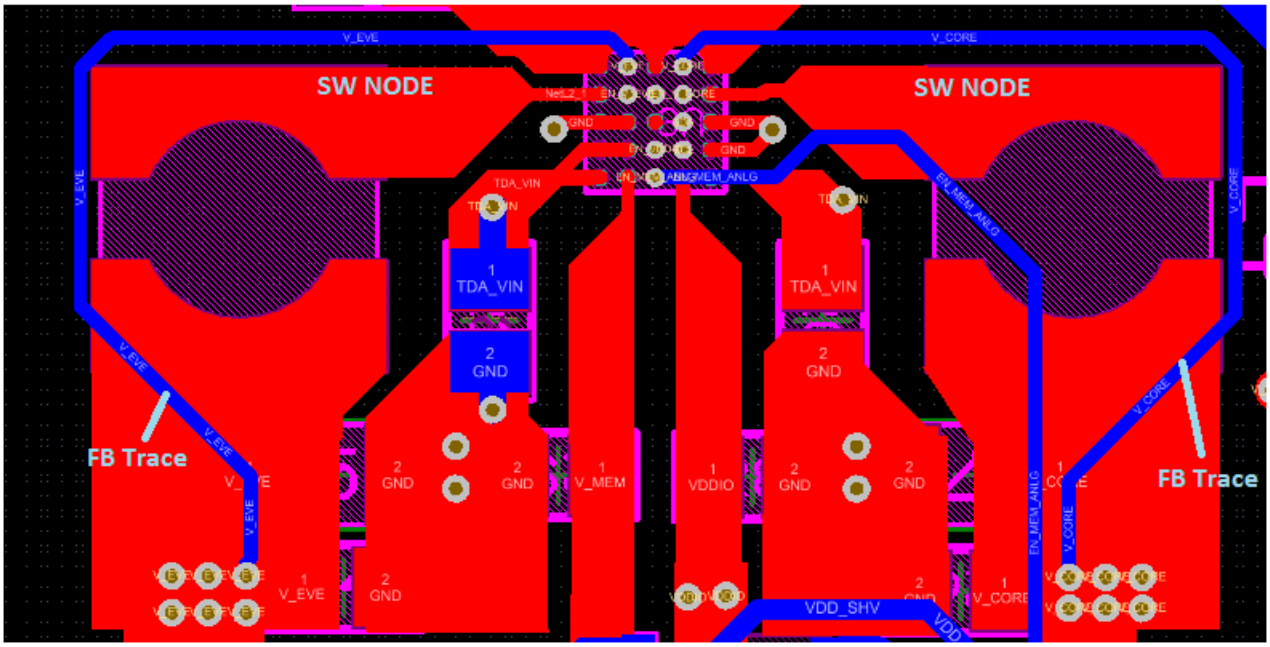


Figure 72. Routing Feedback Traces Around Switch Nodes

FB nodes are high-impedance lines, which are quite sensitive to disturbances. The switch node can radiate a significant amount of energy and could couple noise into FB traces or other sensitive lines. Placing these traces on the other side of the board (with ground planes between them) helps mitigate ill effects as well. I^2C traces should also be routed away from switching nodes.

It is critical that analog and control loop components be placed such that their trace lengths back to the IC are minimized. Figure 73 shows an example of the compensation and feedback components for the DDR supply DC-DC converter:

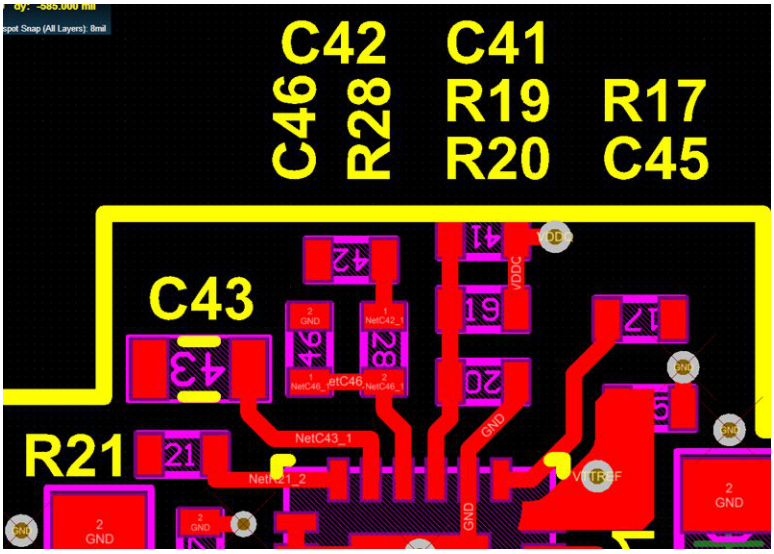
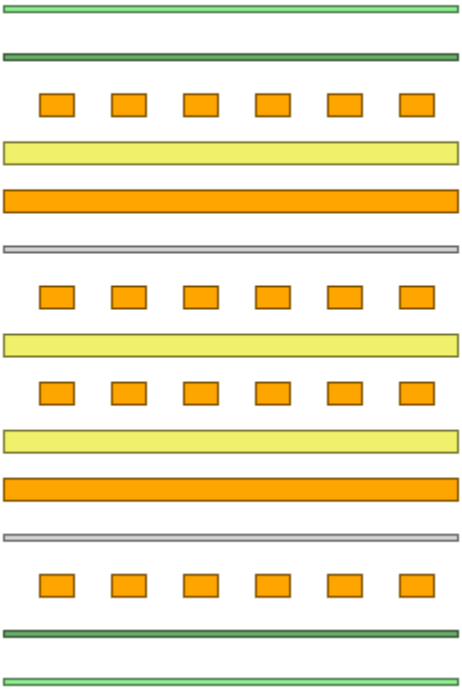


Figure 73. Compensation and Feedback Components Placed Close to IC

The FB and COMP nodes are especially high impedance and thus susceptible to picking up noise emitted from switching nodes. As these nodes are critical to operate the device's control loop, poor placement and routing of these components or traces can affect the performance of the device by introducing unwanted parasitic inductances and capacitances.

5.1.2 PCB Layering Recommendations

If using a six-layer board (as in this TI Design), make layers 2 and 5 ground planes to shield the internal signal layers from outside noise sources as well as the switch nodes found on the top layer. If using a four-layer board, layer 2 should be a ground plane. Figure 74 shows the stack-up used in this TI Design.



Layer Name	Type	Material	Thickness (mil)
Top Overlay	Overlay		
Top Solder	Solder Mask/...	Surface Mat...	0.4
Top Layer	Signal	Copper	1.4
Dielectric1	Dielectric	Core	14.3
GND1	Internal Plane	Copper	1.417
Dielectric 5	Dielectric	Prepreg	5
VSYS	Signal	Copper	1.417
Dielectric 4	Dielectric	Core	14.3
Signal	Signal	Copper	1.417
Dielectric 2	Dielectric	Core	14.3
GND2	Internal Plane	Copper	1.417
Dielectric 3	Dielectric	Prepreg	5
Bottom Layer	Signal	Copper	1.4
Bottom Solder	Solder Mask/...	Surface Mat...	0.4
Bottom Over...	Overlay		

Figure 74. Layer Stack-up With GND Planes Separating Signal Layers

Keep power traces and pours on the same layer as much as routing requirements allow. This grouping minimizes the inductance of the path and reduces noise coupling between planes. Unfortunately, due to the high number of rails in this TI Design and the routing requirements needed to get signals to the EVM connectors, sticking to this rule is not totally possible.

5.1.3 General Power Supply Considerations

- Input capacitors should be placed as close to the IC as possible to reduce the parasitic series inductance from the capacitor to the device it is supplying. This is especially important for DC-DC converters as the inductance from the capacitor to the high-side switching FET can cause high voltage spikes and ringing on the switch node, which can be damaging to components and cause problems for EMI.
- Place the input capacitors in order of descending size/value, with the smallest being closest to the device input pin. Contrastingly, place the output capacitors in order of increasing size/value, with the largest being closest to the device's output pins/power inductor.
- Use wide copper traces for routing the outputs of converters to the connectors or loads. This reduces the IR drop along the power path and thus improves load regulation.
- The resistance of a trace drops as the width of the trace increases($R \propto 1/W$). If not using DC-DC or linear regulators capable of differential remote sensing, care must be taken that the voltage drop from the location of regulation (close to the converter) to the load is not significant. While there isn't a maximum limit on this, there is a minimum. PCB traces, like wires, are rated for current ranges based on their cross-sectional area. This depends not only on the width but also on the thickness of the trace. Calculators are available online for calculating minimum trace width.

- Minimize the loop area and series path inductance of the return switching current in a DC-DC converter. It is preferable that this be on the same layer and can be achieved by careful placement of the components, as can be seen below with the grounds of the input and output capacitors very close to each other.
- Since it is not always convenient to guarantee a good return path on the same layer, ground vias can be dropped to an internal plane to provide a more direct return path. The figure below shows the use of these ground vias where it was not possible to create a small loop on the top layer.
- Power inductors should be placed close to the switch node pins of the ICs, minimizing the distance from the pin to the inductor, while maintaining large area as much as possible to handle the load currents expected. The goal is to minimize both the parasitic inductance, as well as reduce the radiated emissions from the node. If a boot-strap capacitor is needed it should be placed close to the inductor and IC to minimize loop inductance.

5.1.4 Protection Circuitry

Place input protection circuitry as close to the battery terminal inputs as possible, rather than close to the downstream circuit it is protecting, to reduce the inductance of the path. This allows the TVS diodes to react as quick as possible to any transients. Close placement provides a tight loop for the return path back to the battery terminals while the TVS diodes shunt a transient event. In the event of a reverse polarity event, the FET Q1 will shut off quickly, possibly causing inductive kicks due to the interrupted current flow. The severity of this kick is a function of the inductance (and therefore the length/width) of the power path.

6 Software Files

To download the I^2C programming GUI for the LP8731-Q1, go to http://www.ti.com/product/LP8731-Q1/toolssoftware.

7 Related Documentation

1. Texas Instruments, *3.5 V to 36 V Wide-VIN Synchronous 2.1 MHz Step-Down Converters*, LM53603-Q1 Datasheet (SNVSAR0)
2. Texas Instruments, *Dual High-Current Step-Down DC-DC And Dual Linear Regulators with I^2C Interface*, LP8731-Q1 Datasheet (SNVSA28)
3. Texas Instruments, *3.5-MHz High Efficiency Step-Up Converter*, TPS61240-Q1 Datasheet (SLVSAO4)
4. Texas Instruments, *Zero IQ Reverse Polarity Protection Smart Diode Controller*, LM74610-Q1 Datasheet (SNOSCZ1)
5. Texas Instruments, *Simple Power Sequencer*, LM3880-Q1 Datasheet (SNVS451)
6. Texas Instruments, *2.95-V to 6-V Input, 4-A Step-Down Converter and 1-A Source/Sink DDR Termination Regulator* , TPS54116-Q1 Datasheet (SLVSCO3B)
7. International Organization for Standardization, ISO 7637-2:2004 Road vehicles – Electrical disturbances from conduction and coupling – Part 2: Electrical transient conduction along supply lines only, Section 5.6
8. International Organization for Standardization, ISO 16750-2:2010 Road vehicles – Environmental conditions and testing for electrical and electronic equipment – Part 2: Electrical loads, Section 4.6
9. Texas Instruments, *USB Interface Adapter EVM*, USB-TO-GPIO Tool Folder (http://www.ti.com/tool/usb-to-gpio)

7.1 Trademarks

Revision B History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (May 2017) to B Revision	Page
• Changed bottom LM53603 device in block diagram to TPS61240-Q1	1

Revision A History

Changes from Original (November 2015) to A Revision	Page
• Changed from preview draft	1

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