TI Designs

Multi-Protocol Digital Position Encoder Master Interface Reference Design With AM437x on PRU-ICSS

TEXAS INSTRUMENTS

TI Designs

TI provides the system solution for industrial communication on Sitara™ processors. This TI Design describes the integrated multi-protocol digital position encoder master interface support:
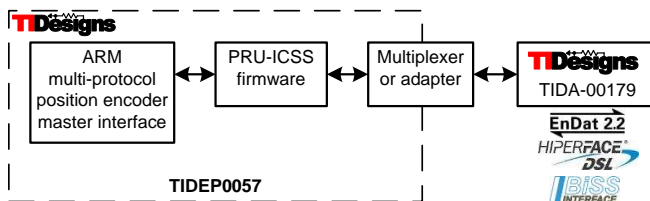
- Multi-protocol digital position encoder master interface for EnDat 2.2, BiSS C, and HIPERFACE® DSL
- For integrated single-chip drives, servo drives, and remote position encoder master devices
- Supported by the PRU-ICSS peripheral within the Sitara AM437x processor
- No external FPGA or ASIC for position encoder protocol required

Design Resources

|	
TIDEP0057	Design Folder
AM4376	Product Folder
SN65HVD78	Product Folder
TMDSIDK437X	Tools Folder
TIDA-00179	Tools Folder

ASK Our E2E Experts

Design Features

- Supports Master Protocol of the Following Digital Position Encoders:
  - EnDat 2.2 (Heidenhain)
  - HIPERFACE DSL (SICK STEGMANN)
  - BiSS C (iC Haus)
- Example Multi-Protocol Selector Application for ARM in Source Code to Enable Customization
- Getting Started Guide for AM437x Industrial Development Kit
- Featured at SPS/IPC/Drive 2015 Trade Show: https://www.youtube.com/watch?v=6PYky6Rx9aw

Featured Applications

- Integrated Servo Drives
- Remote Position Encoder Master Devices
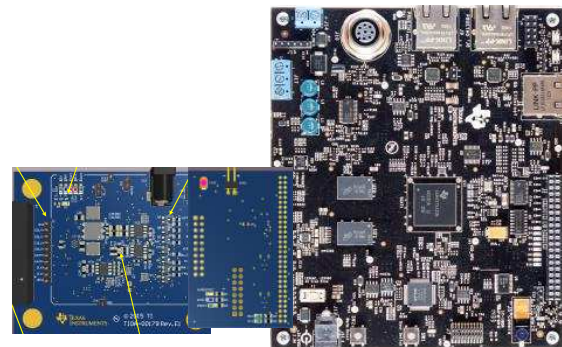
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1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION	DETAILS
Digital position encoder	EnDat 2.2 encoder	Heidenhain
	HIPERFACE DSL encoder	Sick
	BiSS C encoder	Wachendorf

2 System Description

Digital position encoders measure the angle or distance of a rotary or linear shaft and output a digital code. There are two types of position encoders: absolute and incremental position encoders. The absolute encoder does not require any calibration of the zero point and outputs the true position. The incremental encoder typically requires a calibration after power up and provides motion information, which can be processed into speed, distance, and position.

Position encoders are used inside integrated motor or servo drives and stand-alone position feedback installments. Position encoders report the current position (angle or distance) of the motor towards a position encoder master and can be analog or digital. The integrated servo drive contains the position encoder master, inverter stage, motor control module, and fieldbus interface.

This TI Design targets the digital position encoder master interface, specifically about the position encoder communication protocols EnDat 2.2, HIPERFACE DSL, and BiCC C.
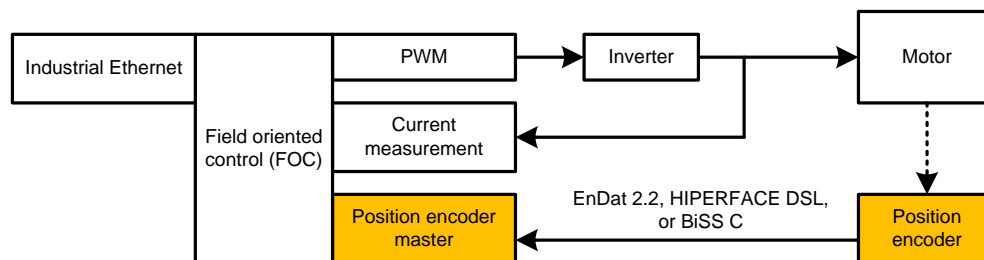
Figure 1. Integrated Servo Drive With Position Encoder Master Interface

Each digital position encoder communication protocol requires a specific hardware implementation in terms of FPGA, PLD, or ASIC. This TI Design implements all those three communication protocols with one Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS), which is a peripheral on many TI Sitara processors. Furthermore, the PRU-ICSS can support another communication protocol by changing the firmware on the PRU. This TI Design is based on the TMDSIDK437x industrial development kit (IDK).

2.1 Absolute Digital Position Encoder

Absolute digital position encoders report back the "true" position in terms of angle or distance without any kind of calibration after power up. On the other side, relative position encoders require calibration of a reference position after power up. In addition to the angle, absolute position encoders can also measure whole rounds of turns.

This TI Design's PRU-ICSS currently supports the following digital encoder protocols: EnDat 2.2, HIPERFACE DSL, and BiSS. It is possible for customers using PRU-ICSS to implement additional position encoder communication protocols.

The following sections describe an overview of the digital position encoder protocol used in this TI Design.

2.2   EnDat 2.2

The EnDat interface was developed by the German company HEIDENHAIN [5]. The initial version of EnDat used analog interface signals. With EnDat 2.2, the encoder interface became a digital, bidirectional interface for incremental and absolute encoders. It uses the RS-485 standard for differential signal transmission.

The EnDAT uses two differential signals to transmit the position data: CLOCK (unidirectional) and DATA (bidirectional). The power supply has six wires required to establish communication between the EnDat master and the EnDat slave (see Figure 2).
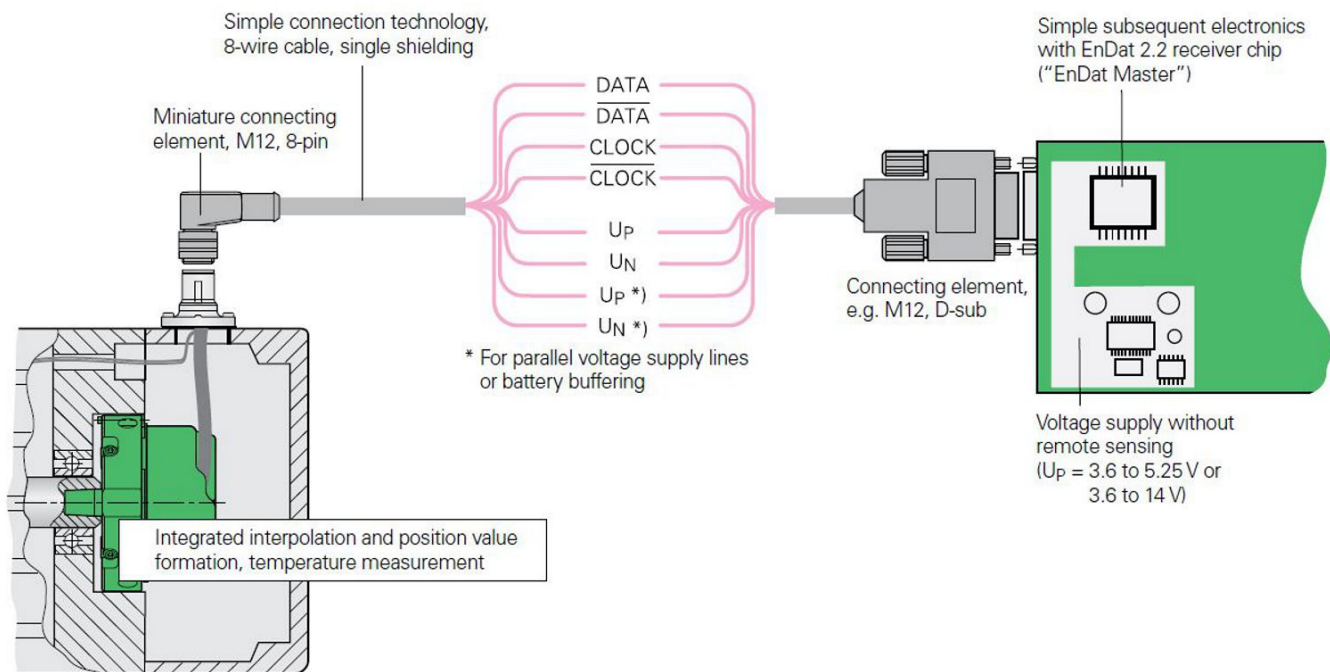
Figure 2. EnDat 2.2 Master Slave Architecture

EnDat 2.2 supports operating frequencies between 100 kHz and 16 MHz. At higher frequencies—starting at 2 MHz—the master has to support signal propagation delay compensation. EnDat supports cable length of up to 100 m. The startup of an EnDat master-to-slave communication is getting trained at a lower frequency, where also the cable propagation delay is measured. After this initial startup, the EnDat can operate at higher frequencies.

The EnDat slave reports the position back to the master with the position request frame. Additional information like diagnostic data, calibration, and parameter data can be also included in the position request frame; therefore, no additional frame has to be exchanged between the master and slave.

EnDat supports various kinds of encoder types, including

- Incremental linear encoder
- Absolute linear encoder
- Rotational incremental single-turn encoder
- Rotational absolute single-turn encoder
- Multi-turn rotary encoder
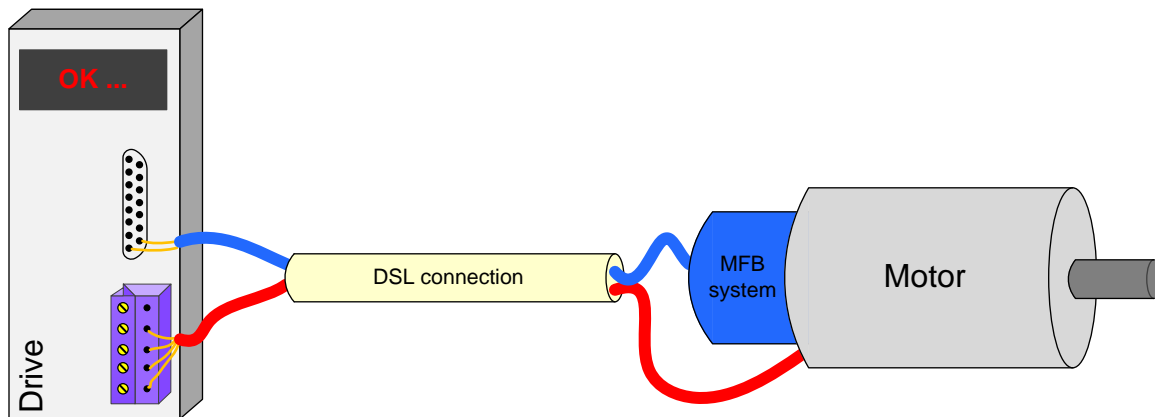- Multi-turn rotary encoder with battery buffer

The PRU-ICSS has a dedicated hardware IP block to support the command message format and compensation delay for EnDat 2.2. One PRU can support up to three EnDat 2.2 channels. See TIDEP0050 for further information.

2.3 *HIPERFACE DSL*

The **HI**gh **PER**formance Inter**FACE D**igital **S**ervo **L**ink (HIPERFACE DSL) encoder protocol has been developed by SICK STEGMANN. It also uses the RS-485 standard for differential signal transmission. It operates at a fixed frequency of 9.375 MHz and supports cables up to 100 m.

The advantage of HIPERFACE DSL is the two-wire interface with bidirectional communication between the HIPERFACE DSL master and HIPERFACE DSL slave. These two wires are also transporting the encoder power supply; therefore, only two wires in total need to be wired between the master and the slave, which extremely reduces the wiring cost.

There is a continuous stream of position requests between the master and the slave and no on-demand position requests. To synchronize the motor control loop to the encoder position request, the HIPERFACE DSL master can synchronize the position requests of the control loop to the HIPERFACE DSL slave.

Figure 3. HIPERFACE DSL System

The PRU-ICSS has a dedicated hardware IP block to support the command message format and compensation delay for the HIPERFACE DSL. One PRU can support one HIPERFACE DLS channels (one PRU-ICSS has two PRUs, hence support for two HIPERFACE DSL is possible).

2.4 BiSS C

The bidirectional BiSS interface has been developed by iC-Haus in 2002 and has been published as open source. The BiSS interface is compatible with the unidirectional serial synchronous interface (SSI). BiSS C protocol refers to continuous mode. It supports a maximum of 10 MHz with the RS-485 interface.

The BiSS C standard supports point-to-point between master and slave, but it also allows multiple sensors and actuator buses that are connected to one master. The interface consists of a shared clock and control data (MA+/MA–) signal from the master to the slave. In return, from the slaves to the master there is the shared sensor data and control data (SL+/SL–) signal.

The control data is embedded as one additional bit in each BiSS C message transfer. The master and slave need to collect the control data over multiple BiSS C messages in order to build up the control request or control response.

Overall, the BiSS C interface requires four signal data lines and two power supply lines between the master and the sensor (see Figure 4).
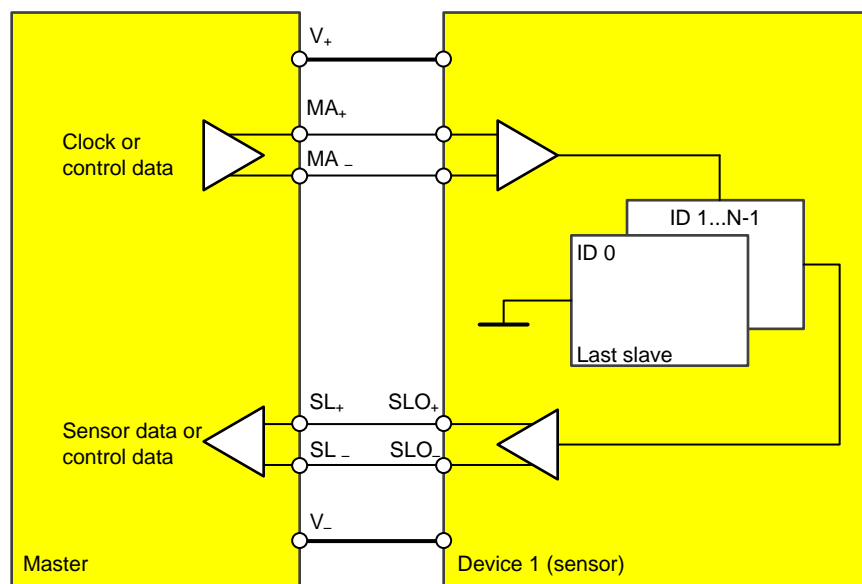

Figure 4. BiSS C System

The master performs line delay compensation by detecting the start bit sequence in the slave's responds message. Therefore, the BiSS C standard can support cable signal path delay of up to 100 m. The position measurement request is triggered on request by the master.

The PRU-ICSS has a dedicated hardware IP block to support the message format and compensation delay for BiCC C. One PRU can support one HIPERFACE DLS channels (one PRU-ICSS has two PRUs, hence support for two HIPERFACE DSL is possible).

2.5   Multi-Protocol Encoder With PRU-ICSS

The AM437x application processor has two instances of PRU-ICSS. Each PRU-ICSS has two PRUs (see Figure 5). A PRU is a programmable 32-bit RISC processor with no instruction pipeline; therefore, the PRU executes each instruction in 5 ns, which allows real-time programming of interfaces.
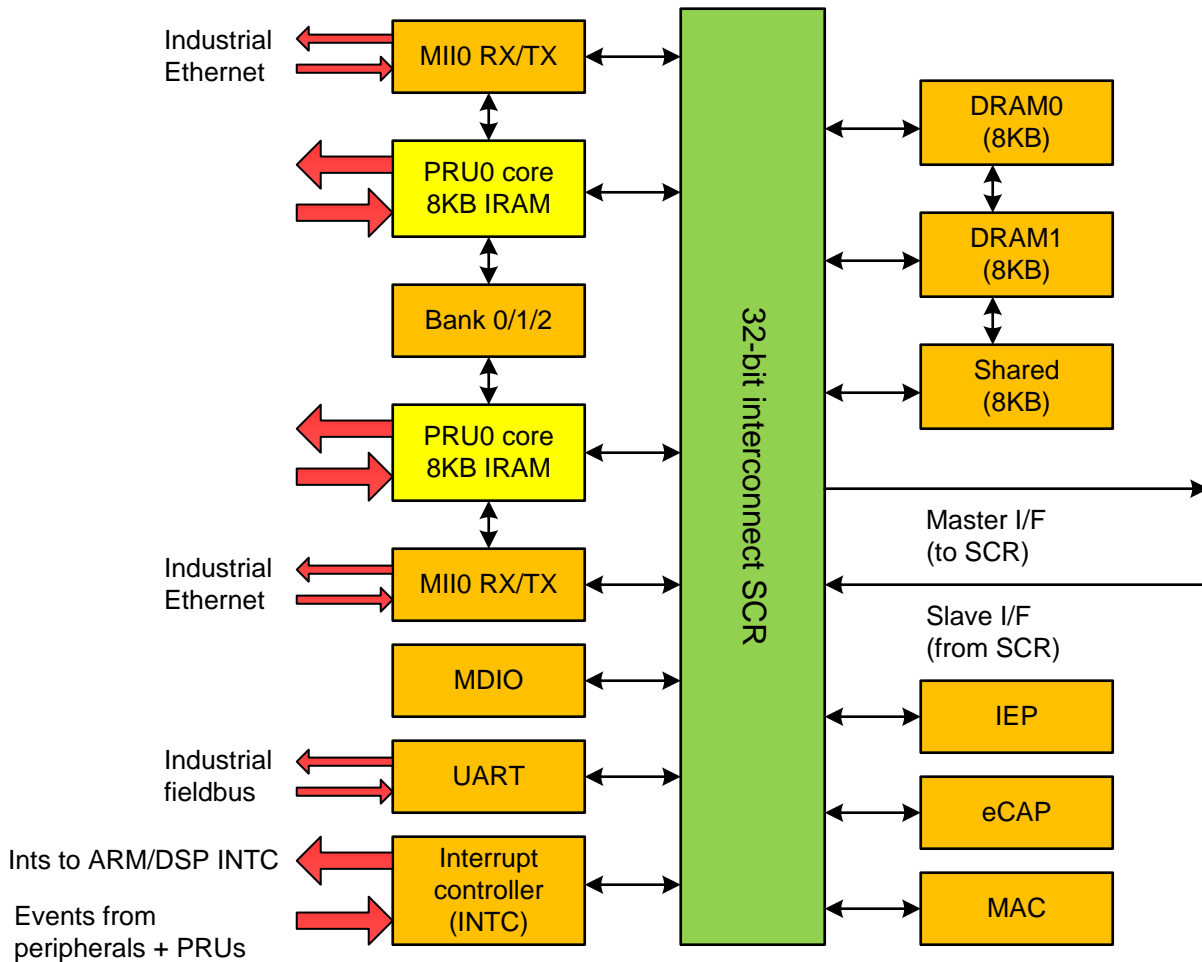
Figure 5. PRU-ICSS System Architecture

The PRU-ICSS has integrated hardware support for digital position encoder interfaces. It has dedicated position encoder hardware that is directly used to interface EnDat 2.2 and HIPERFACE DSL. The peripheral supports signal line delay compensation and serial bit-stream transmission and reception.

One PRU can support up to three channels for EnDat, one channel for HIPERFACE DSL, or one channel for BiSS C.
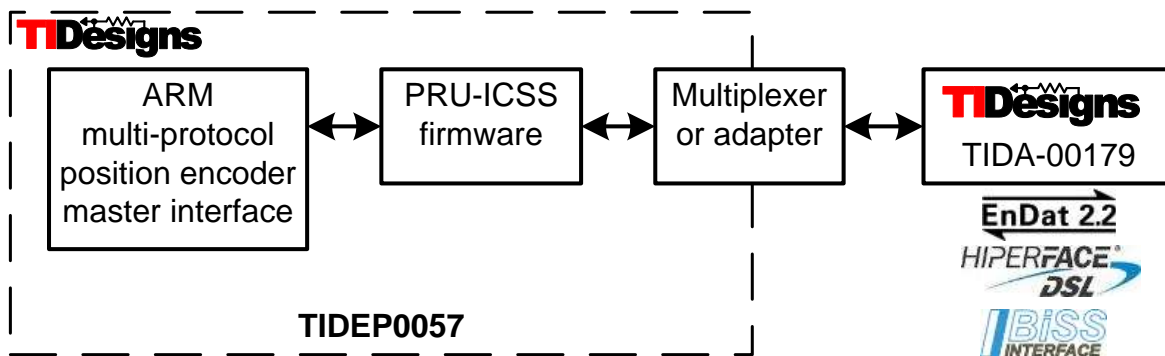
3   Block Diagram

Figure 6. System Block Diagram

3.1   *Highlighted Products*

3.1.1   AM4379 Processor

Up to 1-GHz Sitara ARM® Cortex®-A9 32-bit RISC processor:

- NEON™ SIMD coprocessor and ARM Vector Floating Point (VFPv3) coprocessor
- 32KB of L1 instruction and 32KB of data cache
- 256KB of L2 Cache or L3 RAM
- 256KB of on-chip boot ROM
- 64KB of dedicated RAM
- Emulation and debug – JTAG
- Interrupt controller

PRU-ICSS:

- Supports protocols such as EtherCAT®, PROFIBUS, PROFINET, EtherNet/IP™, EnDat 2.2, and more
- Two PRU subsystems with two PRU cores each
- 32-bit load and store RISC processor capable of running at 200 MHz
- 12KB (PRU-ICSS1), 4KB (PRU-ICSS0) of instruction RAM with single-error detection (parity)
- 8KB (PRU-ICSS1), 4KB (PRU-ICSS0) of data RAM with single-error detection (parity)
- Single-cycle 32-bit multiplier with 64-bit accumulator
- Enhanced GPIO module provides shift-in or shift-out support and parallel latch on external signal
- 12KB (PRU-ICSS1 only) of shared RAM with single-error detection (parity)
- Three 120-byte register banks accessible by each PRU
- Local interconnect bus for connecting internal and external masters to the resources inside the PRU-ICSS
- Peripherals inside the PRU-ICSS:
    - One UART port with flow control pins, supports up to 12 Mbps
    - One enhanced capture (eCAP) module
    - Two MII Ethernet ports that support industrial Ethernet, such as EtherCAT
    - One MDIO port
- On-chip memory (shared L3 RAM)
- 256KB of general-purpose on-chip memory controller (OCMC) RAM
- Accessible to all masters

External memory interfaces (EMIF):

- DDR controllers:
  - LPDDR2: 266-MHz clock (LPDDR2-533 data rate)
  - DDR3 and DDR3L: 400-MHz clock (DDR-800 data rate)
  - 32-bit data bus
  - 2GB of total addressable space
  - Supports one x32, two x16, or four x8 memory device configurations
- General purpose memory controller (GPMC)
  - Flexible 8-bit and 16-bit asynchronous memory interface with up to seven chip selects (NAND, NOR, Muxed-NOR, SRAM)
  - Uses BCH code to support 4-, 8-, or 16-bit ECC
  - Uses hamming code to support 1-bit ECC

See the AM4379 datasheet for a complete list of features [3].

3.1.2 AM437X IDK EVM Hardware Specification

Features

- AM4379 ARM Cortex-A9
- 1GB DDR3, QSPI-NOR flash
- Discrete power solution
- EnDat connectivity for motor feedback control
- 24-V power supply
- USB cable for JTAG interface and serial console

Software and tools

- SYS/BIOS real-time operating system (OS)
- StarterWare base port
- TI Code Composer Studio™ (CCS) integrated development environment (IDE)
- Application stack for industrial communication protocols
- Sample industrial applications

Connectivity

- PROFIBUS interface
- CANOpen
- EtherCAT
- EtherNet/IP
- PROFINET
- Sercos III
- IEC61850
- PWM
- Motor axis position feedback
- Up to 3-phase motor drive connector
- Sigma delta decimation filter
- Digital inputs and outputs (I/O)
- SPI
- UART
- JTAG

See the AM437X IDK tool folder for a complete list of features and design resources:
http://www.ti.com/tool/tmdsidk437x

3.1.3 SN65HVD78 3.3-V Supply RS-485 With IEC ESD Protection

Features

- Small-size VSSOP packages save board space or SOIC for drop-in compatibility
- Bus I/O protection
  - \>±15-kV HBM protection
  - \>±12-kV IEC 61000-4-2 contact discharge
  - \>±4-kV IEC 61000-4-4 fast transient burst
- Extended industrial temperature range –40°C to 125°C
- Large receiver hysteresis (80 mV) for noise rejection
- Low unit loading allows over 200 connected nodes
- Low power consumption
  - Low standby supply current: < 2 µA
  - I_{CC} < 1-mA quiescent during operation
- 5-V tolerant logic inputs compatible with 3.3-V or 5-V controllers
- Signaling rate options optimized for 250 kbps, 20 Mbps, and 50 Mbps

See the SN65HVD78 datasheet for a complete list of features: http://www.ti.com/product/SN65HVD78

4 System Design Theory

The Multi-Protocol Encoder Master Support for AM437x design checks for a valid communication connection to BiSS C, HIPERFACE DSL, and EnDat 2.2 encoder type. It consists of an ARM application and corresponding encoder PRU firmware binaries.

The ARM application configures the hardware boards for a specific protocol and loads the PRU firmware. After the encoder startup time, the ARM application tests if the encoder reports back a valid position. If there is no valid position after some time (typically less than one second), the ARM reconfigures the hardware and PRU for the next encoder protocol. This sequence is repeated by the ARM application until a valid position is reported. The ARM application displays the position through the UART console.

Once the ARM detects a stale or invalid position—which occurs if the encoder gets disconnected—it will repeat this sequence.

4.1 Required Hardware Function

This TI Design has been validated with the following three hardware boards:

- AM437x IDK (TMDSIDK437X): This is the reference design with the AM437X application processor and power management. Expansion connector J16 routes out all the required encoder signals for BiSS, HIPERFACE DSL, and EnDat 2.2. This TI Design uses EnDAT Channel 2 signals for the interface with EnDat 2.2 and HIPERFACE DSL encoder. BiSS C is interfaced through the serial shift register signals pr0_pru0_r31[0] for SENSOR-DATA and pr0_pru0_r30[x] for CLK.

- Adapter interface board: This board is described in Section 9. The adapter interface board multiplexes the EnDat Channel 2 and serial capture signals towards the TIDA-00179 board. It also indicates with LEDs which interface has been enabled.

- TIDA-00179 board: The board hosts the RS-485 transceiver and power supply for EnDat 2.2, HIPERFACE DSL, and BiSS interface. See the TIDA-00179 TI design guide for more information (TIDUAN5).

To select the signal path for a specific encoder protocol, the ARM sets four processor GPIOs. The GPIOs select a specific pinmux on the adapter interface board and also enable an encoder-specific power supply to generate on the TIDA-00179 board. Table 2 shows the GPIO pinmux signals and the encoder signals.

Table 2. GPIO Pinmux and Encoder Signals

| AM437x SIGNAL		OFFSET	MODE	J16	ADAPTER BOARD	EnDAT	BiSS	HIPERFACE DSL	COMMENT
GPIO_12		0x08b8	7, output	49	MUX_DIS	"0"	"0"	"0"	Enables nOE on U2 on the adapter board
GPIO_13		0x0834	7, output	48	HIPERFACE	"0"	"0"	"1"	Routed to TIDA-00179 for muxing
GPIO_14		0x0838	7, output	42	ENDAT/nBISS	"1"	"0"	"1"	
GPIO_26		0x08f0				EnDat mode	GPIO "0"	EnDat mode	Need to pinmux for BiSS as GPIO and for EnDat and HIPERFACE PRU EnDat mode
pr0_pru0_gpo6		0x9a8	5, output	52	ENDAT2_CLK	pr0_pru0_mux_sel=01			
pr0_pru0_gpo7			5, output	54	ENDAT2_OUT or DSL_OUT	pr0_pru0_mux_sel=01		pr0_pru0_mux_sel=01	
pr0_pru0_gpo8	mmc0_dat3	0x08f0	5, output	56	ENDAT2_OUTEN or DSL_EN	pr0_pru0_mux_sel=01	gpio2_26 (set to 0)	pr0_pru0_mux_sel=01	
pr0_pru0_gpi11	mmc0_dat0	0x8fc	6, output	58	ENDAT2_IN or DSL_IN	pr0_pru0_mux_sel=01		pr0_pru0_mux_sel=01	
pr0_pru0_gpi0			6, output	31	BISS_IN		pr0_pru0_mux_sel=00		
pr0_pru0_gpo1			5, output	33	BISS_CLK		pr0_pru0_mux_sel=00		

4.2 ARM Multi-Protocol Software

The ARM application performs the following tasks after program start (see Figure 7):

1. Initialize a generic IDK board
2. Start the multi-protocol encoder task MPEncoderTask()
3. Initialize the PRU-ICSS subsystem
4. Initialize a generic encoder

Once the generic initialization has been applied, the ARM application operates in a round robin mode. In the round robin mode, the MPEncoderTaks() is calling the three different encoder functions:

• MPEncoderHiperfaceDSL()
• MPEncoderBiSS()
• MPEncoderEnDat22()

Each encoder function is configuring the device's internal peripherals and external signal paths, loading the PRU encoder firmware, and communicating with the encoder. If the encoder function cannot communicate with the encoder after some timeout, the encoder function returns back to the round robin mode.
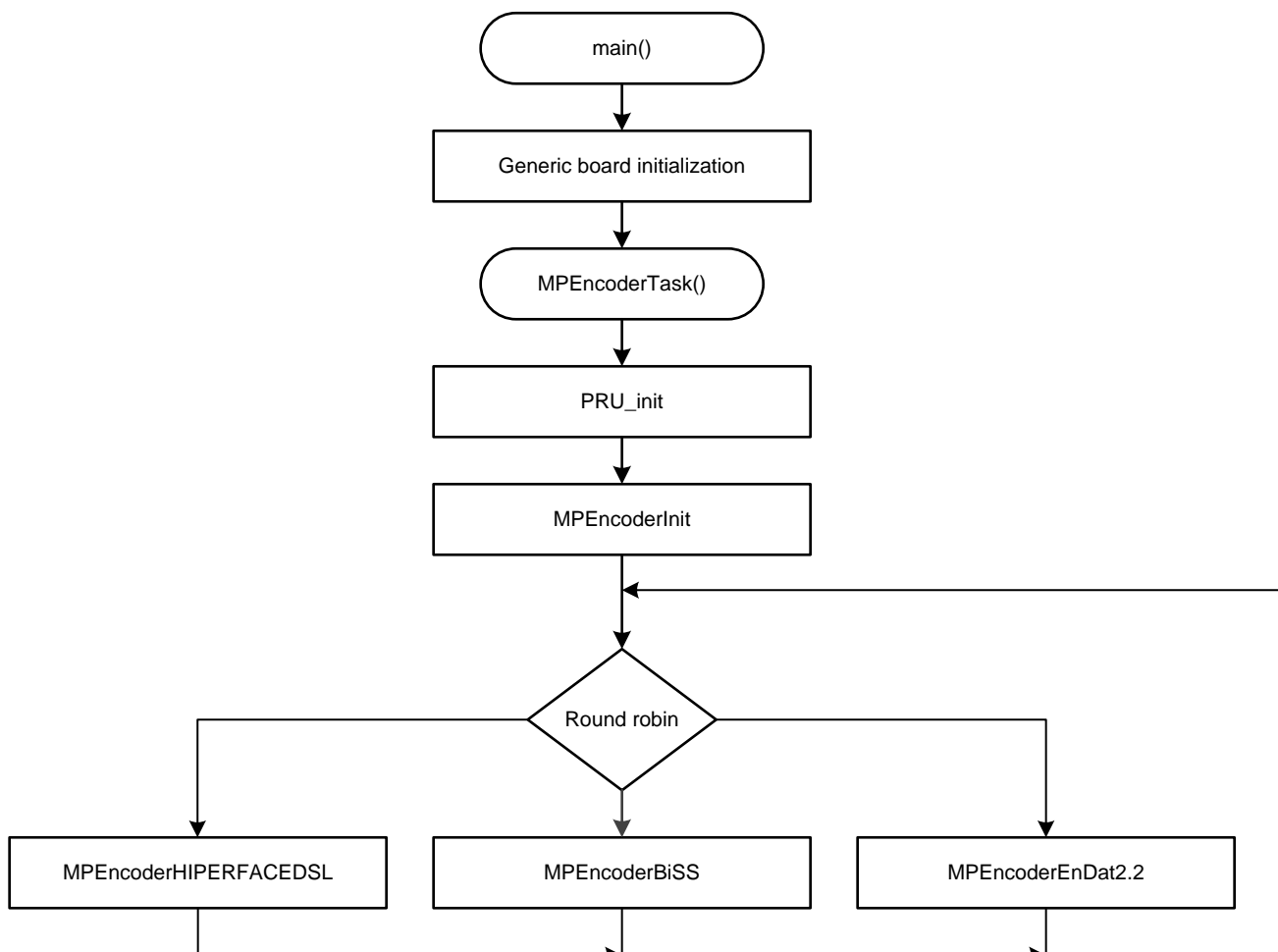
Figure 7. Multi-Protocol Software Flowchart

If there is no position decoder detected after a defined time (typically less than a second), the encoder function returns and the next encoder function is called.

If there is an encoder detected, the encoder information (type of encoder or position) is shown on the UART console output.

5 Getting Started Hardware

This TI Design has been developed with the following hardware.

5.1 TMDSIDK437x IDK

The TMDSIDK437X IDK must be modified to enable encoder signals on J16. Remove R541 to disable the outputs of the QEP driver U58, which would otherwise interfere with the encoder signals.
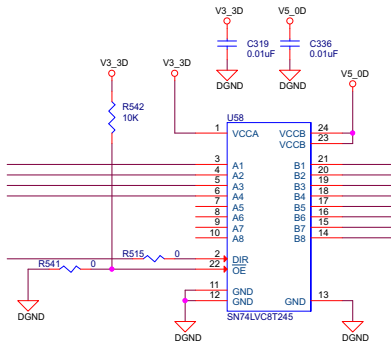

Figure 8. R541 in TMDSIDK437x IDK Schematic

5.2 Multiplexer Adapter

The multiplex adapter schematics are part of this TI Design (see Section 9.1). The multiplex adapter is an interface between the IDK board and the TIDA-00179. It also routes the encoder signals, depending to the selected encoder protocol.

Connect J2 of the multiplex adapter to J16 of the IDK board. The IDK provides power for the multiplex adapter.

5.3 TIDA-00179

The TIDA-00179 board is the Universal Digital Interface to Absolute Position Encoders reference design. For more information, see http://www.ti.com/tool/tida-00179.

6 Getting Started Software

The following software components are required:

- CCS version 6.1.0.00104
- SYS/BIOS 6.41.4.54 Real-Time OS
- XDC Tool 3.31.2.28_core
- Compiler GNU v4.8.4 (Linaro)
- Serial console terminal application (like Tera Term, minicom, or HyperTerminal)

The following hardware components are required:

- The three hardware boards described in Section 5
- microSD card

6.1 Import MPE Project With CCS

Import the AM437xMpe project into CCS: File → Import. After the import, the project can be seen on Project Explorer (see Figure 9).
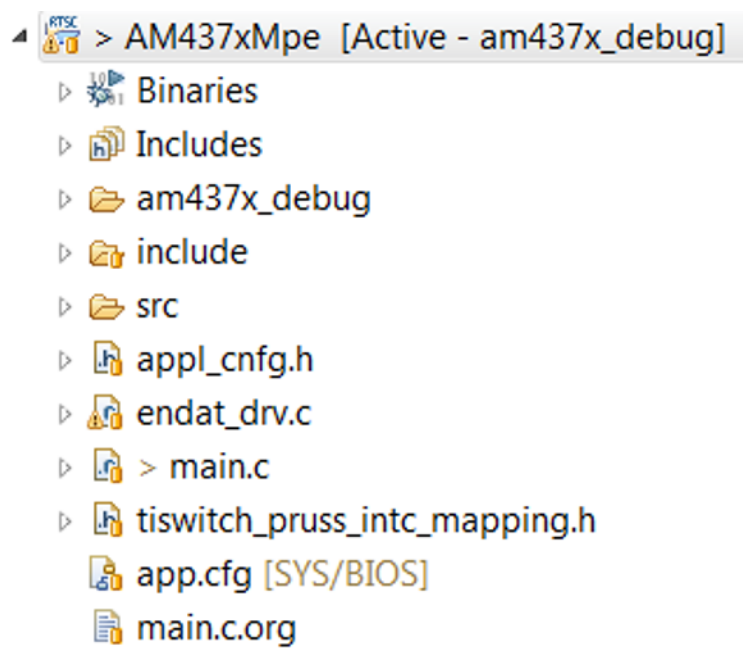
Figure 9. AM437xMpe Project View in CCS

6.2 Build Project

Build the project: Project → Build Project. This generates the files AM437xMPE.out, AM437xMPE_ti.bin, and AM437xMPE.bin (see Figure 10).

```
▲ 🗁 am437x_debug
    ▷ 🗁 configPkg
    ▷ ⏵ AM437xMpe.out - [ARM/le]
    ▷ 🔢 endat_drv.o - [ARM/le]
    ▷ 🔢 main.o - [ARM/le]
       📄 AM437xMpe_ti.bin
       📄 AM437xMpe.bin
       📄 AM437xMpe.map
       📄 ccsObjs.opt
       📄 endat_drv.d
       📄 main.d
       📄 makefile
       📄 objects.mk
       📄 sources.mk
       📄 subdir_rules.mk
       📄 subdir_vars.mk
```
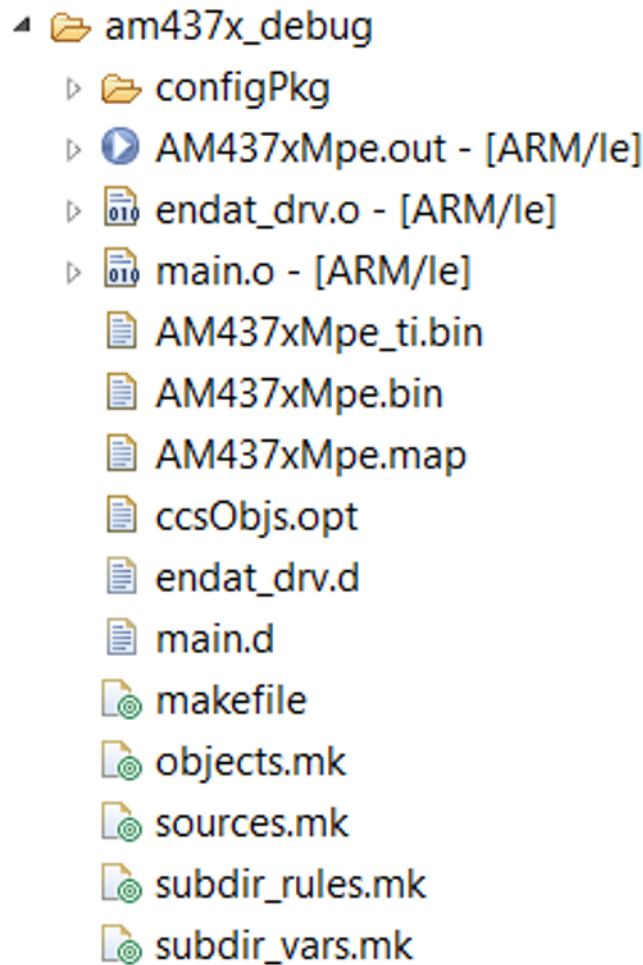
Figure 10. am437x_debug Folder

6.3 Getting Started Using microSD Card

To start the application through a microSD card, perform the following steps:
1. Copy the file AM437xMPE_ti.bin to the microSD card.
2. Rename the file AM437xMPE_ti.bin to app.
3. Place the microSD card into the microSD card slot of the TMDSIDK437X board.
4. Power up the TMDSIDK437X board; the image is getting started by the bootloader.
5. Connect with a serial terminal console and observe the output.

6.4 *Getting Started Through CCS and JTAG*

To start the application through CCS and JTAG connection, perform the following steps:

1. Create a target configuration file for the TMDSIDK437X board (use the EVM GEL script provided by the industrial SDK).
2. Launch the created target configuration in CCS (see Figure 11).
3. Connect though JTAG to the CortexA9 processor.
4. Initialize the board with the AM437x IDK GEL script.
5. Download the AM437xMPE.out file.
6. Start the application.
7. Connect with a serial terminal console and observe the output.
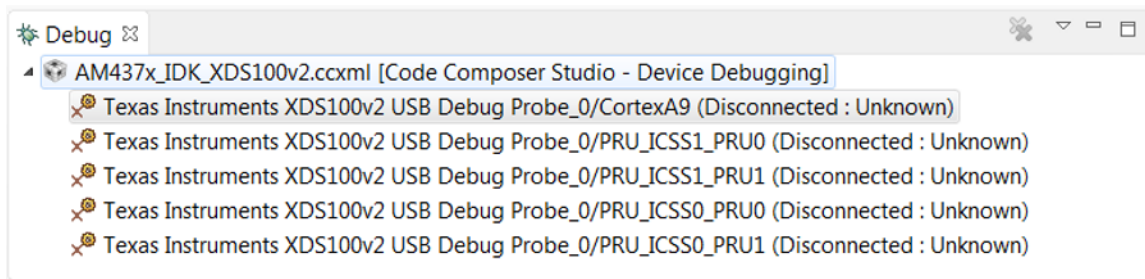
Figure 11. CCS Debug Window

7   Test Setup

The board test setup is mounted into a hexagon (see Figure 12). Between the TIDEP0057 and the encoder is a cable connection, which can be attached to the three different encoders.
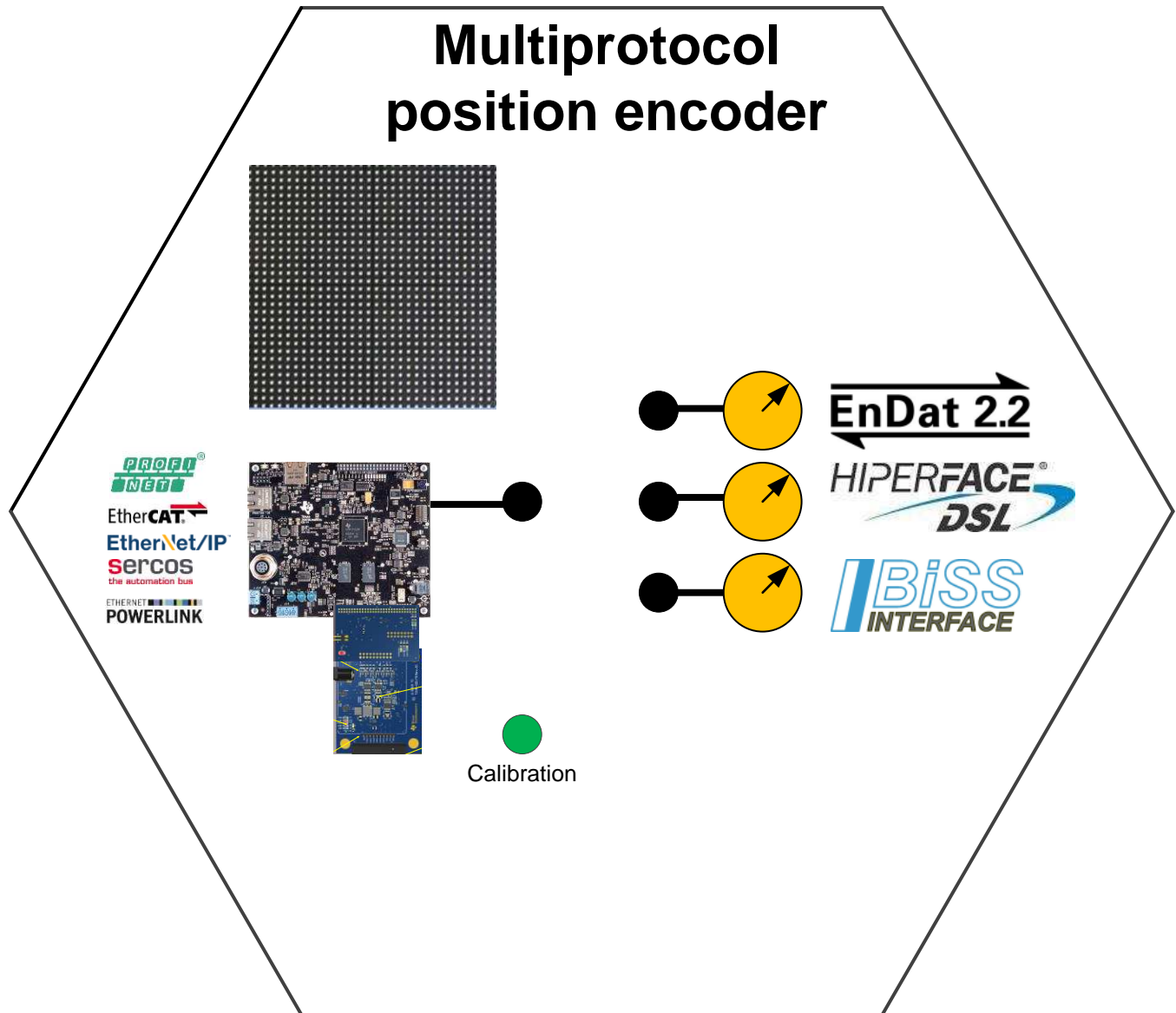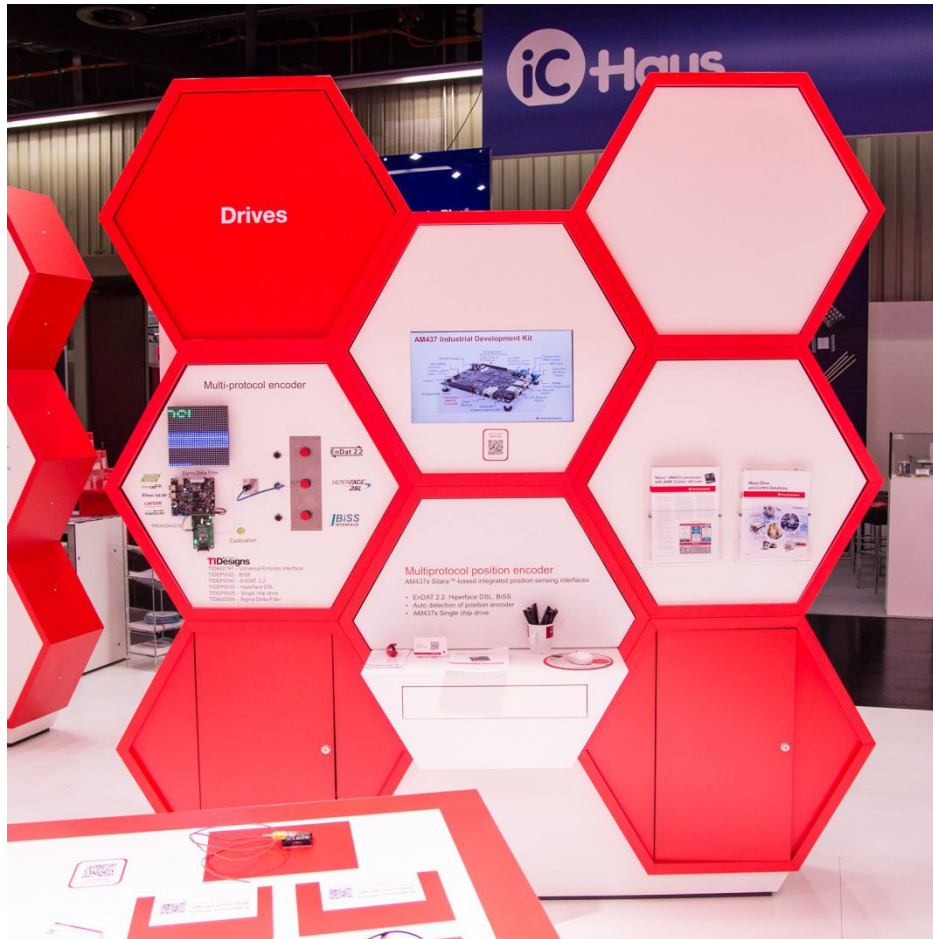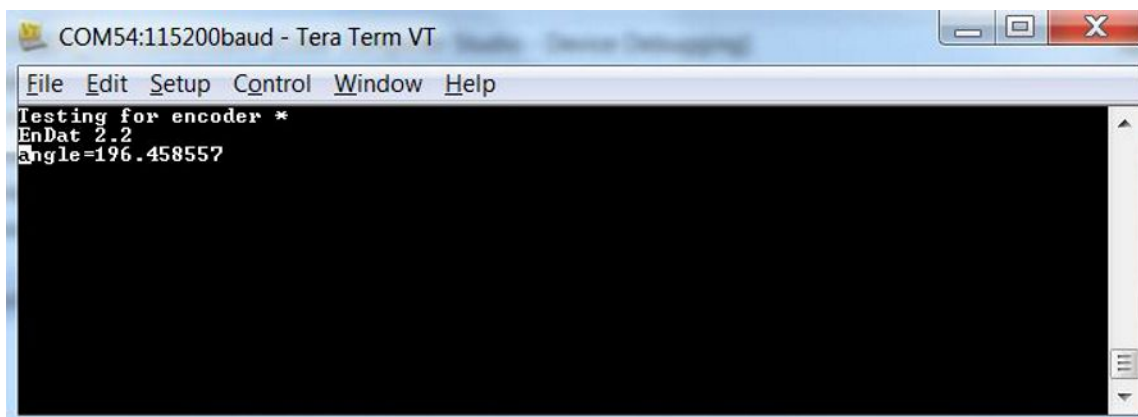

Figure 12. Test Setup

8 Test Data

The multi-protocol encoder has been verified on the setup seen in Figure 13.

Figure 13. Hexagon Test Setup at SPS/IPC/Drives 2015

8.1 *EnDat 2.2*

Connecting an EnDat 2.2 encoder provides the position output in the serial console terminal application as seen in Figure 14.

Figure 14. EnDat 2.2 Serial Terminal Output

8.2 HIPERFACE DSL

Connecting a HIPERFACE DSL encoder provides the position output in the serial console terminal application as seen in Figure 15.
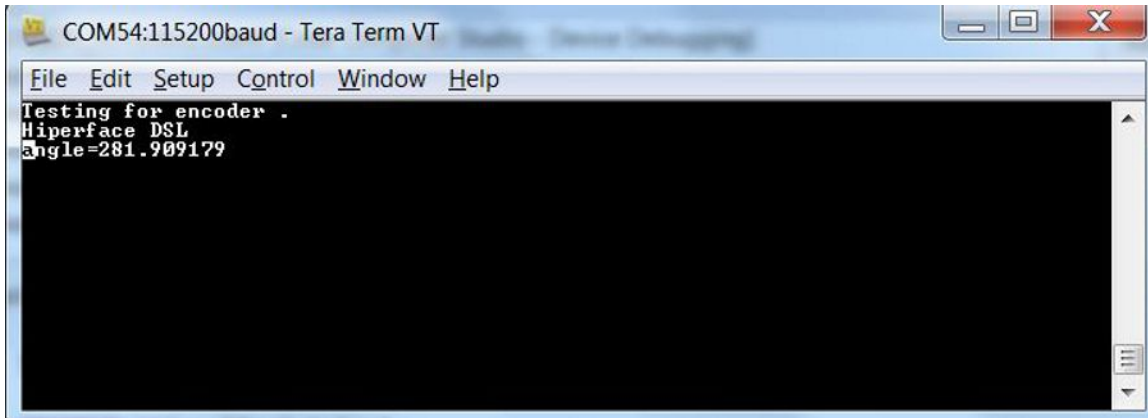

Figure 15. HIPERFACE DSL Serial Terminal Output

8.3 BiSS C

Connecting an EnDat 2.2 encoder provides the position output in the serial console terminal application as seen in Figure 16.
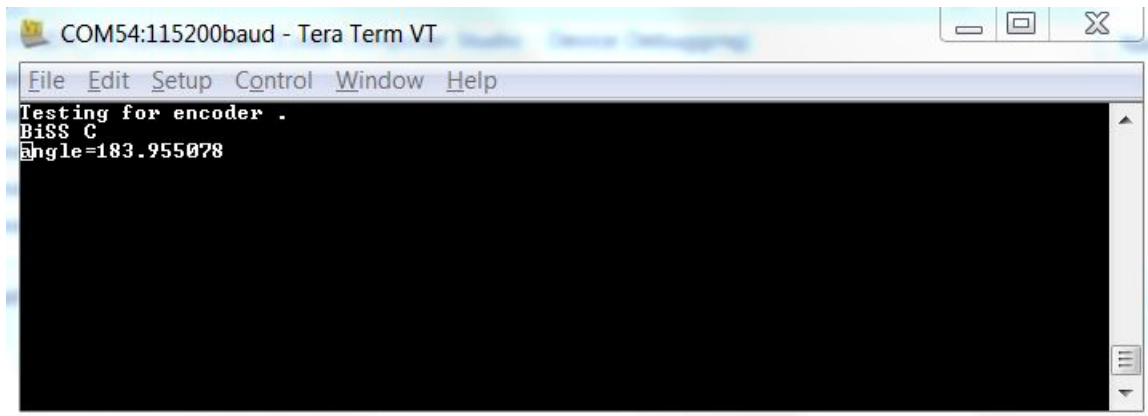

Figure 16. BiSS C Serial Terminal Output

9 Design Files

9.1 Schematics

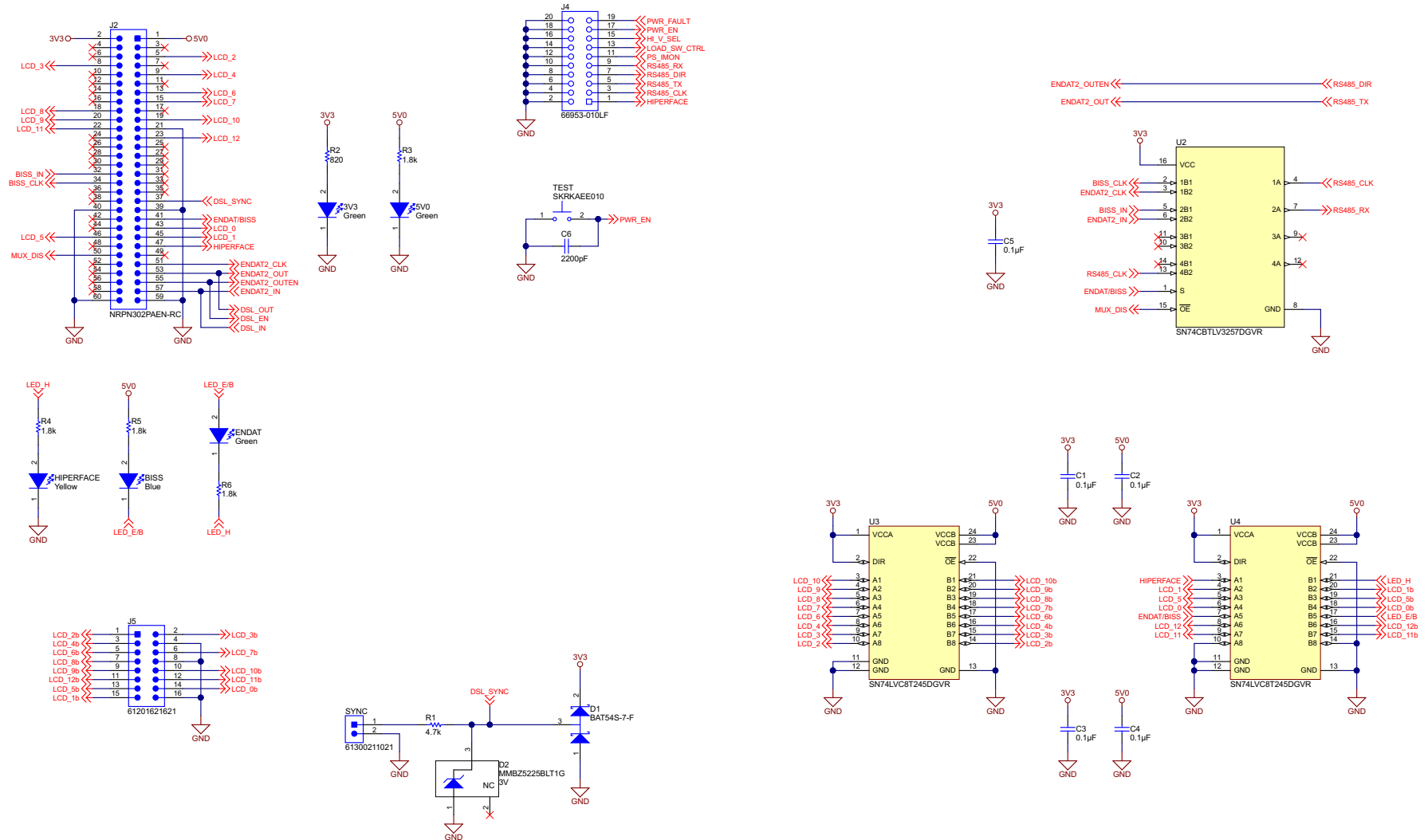To download the schematics, see the design files at [TIDEP0057](#).

Figure 17. Schematic of Adapter Board

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDEP0057.

Table 3. BOM

ITEM	DESIGNATOR	QTY	VALUE	PARTNUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
1	3V3, 5V0, ENDAT	3	Green	150060GS75000	Wurth Elektronik	LED, Green, SMD	LED_0603
2	BISS	1	Blue	150060BS75000	Wurth Elektronik	LED, Blue, SMD	LED_0603
3	C1, C2, C3, C4, C5	5	0.1uF	8.85012E+11	Wurth Elektronik	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0603_095	0603_095
4	C6	1	2200pF	8.85012E+11	Wurth Elektronik	CAP, CERM, 2200 pF, 16 V, +/- 10%, X7R, 0603_095	0603_095
5	D1	1	30V	BAT54S-7-F	Diodes Inc.	Diode, Schottky, 30 V, 0.2 A, SOT-23	SOT-23
6	D2	1	3V	MMBZ5225BLT1G	ON Semiconductor	Diode, Zener, 3 V, 225 mW, SOT-23	SOT-23
7	HIPERFACE	1	Yellow	150060YS75000	Wurth Elektronik	LED, Yellow, SMD	LED_0603
8	J2	1		NRPN302PAEN-RC	Sullins Connector Solutions	Header, 2 mm, 30x2, Gold, SMT	Header, 2 mm, 30x2, Vertical, SMT
9	J4	1		66953-010LF	FCI	Receptacle, 100mil, 10X2, Tin, TH	Receptacle, 100mil, 10x2, TH
10	J5	1		61201621621	Wurth Elektronik	Header(Shrouded), 2.54mm, 8x2, Gold, TH	Header, 2.54mm, 8X2, TH
11	R1	1	4.7k	CRCW06034K70JNEA	Vishay-Dale	RES, 4.7 k, 5%, 0.1 W, 0603	603
12	R2	1	820	RC0603JR-07820RL	Yageo America	RES, 820, 5%, 0.1 W, 0603	603
13	R3, R4, R5, R6	4	1.8k	RC0603JR-071K8L	Yageo America	RES, 1.8 k, 5%, 0.1 W, 0603	603
14	SYNC	1		61300211021	Wurth Elektronik	Header, 2.54 mm, 2x1, Gold, R/A, TH	Header, 2.54 mm, 2x1, R/A, TH
15	TEST	1		SKRKAEE010	Alps	Switch, Push Button, SMD	2.9x2x3.9mm SMD
16	U2	1		SN74CBTLV3257DGVR	Texas Instruments	Low-Voltage 4-Bit 1-of-2 FET Multiplexer / Demultiplexer, DGV0016A	DGV0016A
17	U3, U4	2		SN74LVC8T245DGVR	Texas Instruments	8-BIT DUAL-SUPPLY BUS TRANSCEIVER with CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUT, DGV0024A	DGV0024A

9.3 Layout Prints

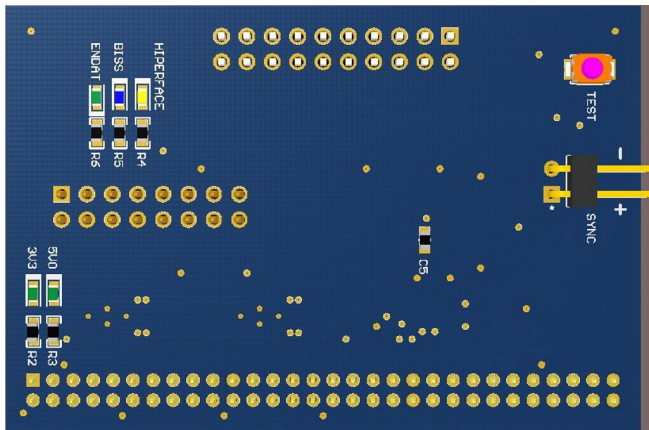To download the layout prints, see the design files at TIDEP0057.
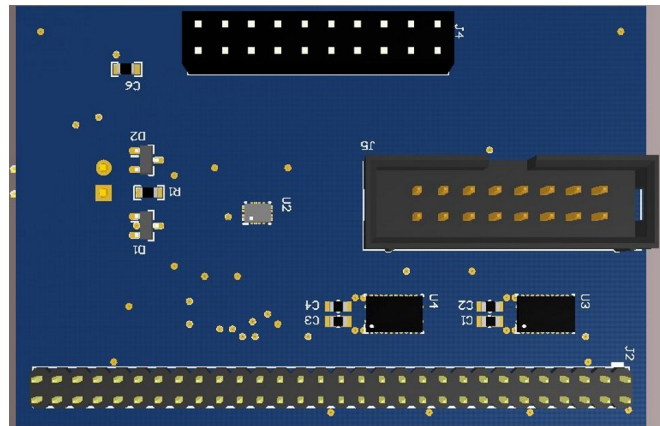

Figure 18. Top Layer

Figure 19. Bottom Layer

9.4 Altium Project

To download the Altium project files, see the design files at TIDEP0057.

9.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDEP0057.

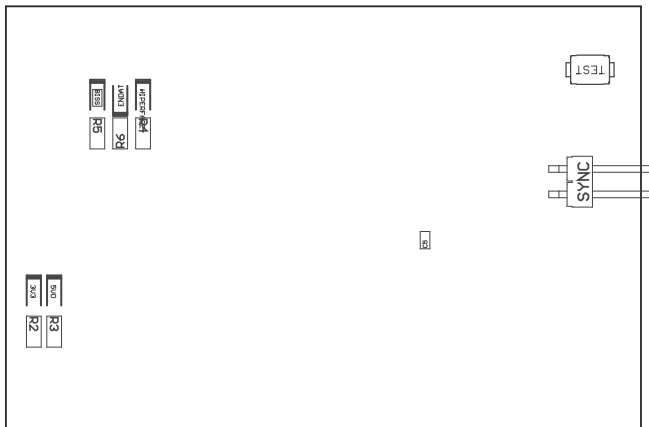**Figure 20. Top Assembly Drawing**

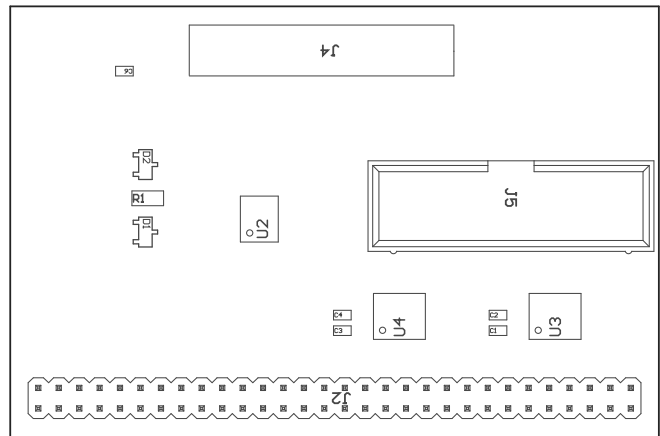**Figure 21. Bottom Assembly Drawing**

10 Software Files

To download the software files, see the design files at TIDEP0057.

11 References

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12 Terminology

ASIC— Application Specific Integrated Circuit

CCS— Code Composer Studio

FPGA— Field Programmable Gate Array

ICSS— Industrial Communication Subsystem

MPE— Multi-Protocol-Encoder

PRU— Programmable Real-time Unit

13 About the Authors

THOMAS MAUER is a System Engineer in the Factory Automation and Control Team at Texas Instruments Freising, where he is responsible for developing reference design solutions for the industrial segment. Thomas brings to this role his extensive experience in industrial communications like Industrial Ethernet, fieldbuses, and industrial applications. Thomas earned his electrical engineering degree (Dipl. Ing. (FH)) at the University of Applied Sciences in Wiesbaden, Germany.

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