TI Designs

Combined Voltage and Current Output With Surge Protection Reference Design

Description

This TI Design provides a universal analog output (AO) for industrial sensors and transmitters. The design is based on a 16-bit DAC and uses a single output. This common output is user configurable for 0 V to 10 V or for 4 mA to 20 mA. The design implements a dedicated protection circuitry for use in harsh industrial environments and has been designed to withstand differential mode surge pulses up to 1 kV at 40 Ω, according to the IEC61000-4-5 standard. The use of an isolated digital interface simplifies board configuration and evaluation.

Resources

TIDA-00559	Design Folder
DAC8760	Product Folder
TPS7A1601	Product Folder
OPA170	Product Folder
ISO7641FC	Product Folder
TIPD153	Tool Folder

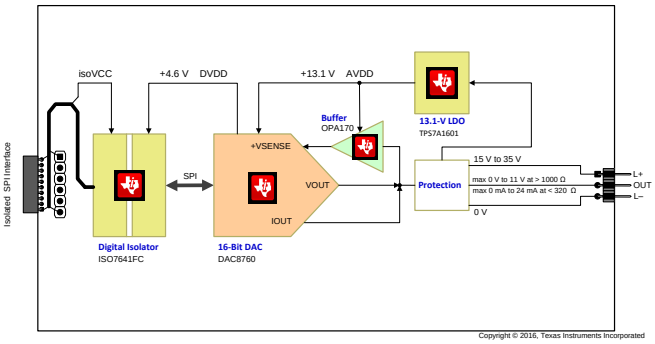
TI E2E™ Community — ASK Our E2E Experts

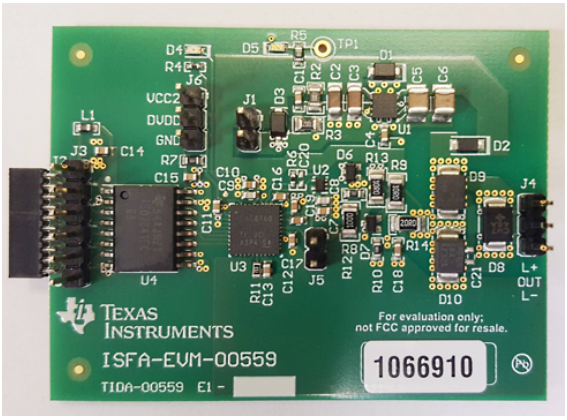
Features

- Analog Output Sensor Interface
  - Based on 16-Bit DAC
- Common Output Pin, Selectable as Voltage or Current Output
  - 0 V to 10 V (Plus 10% Overrange), Minimum Load ≥ 1kΩ
  - 4 mA to 20 mA (0 mA to 24 mA), Maximum Load ≤ 320 Ω
- Designed to Meet EN 61000-4-5
  - ±1 kV, 40 Ω, 8/20 µs, DM
- Configuration and Evaluation Interface
  - Isolated Four-Wire SPI
- Power Input: 15 V to 35 V
  - Reverse Polarity Protection

Applications

- Factory Automation
- Process Control
- Field Transmitter With Analog Output
- Analog Outputs of PLC Modules





An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Overview

1.1 System Description

This combined voltage and current analog output (AO) design addresses the following specific requirements to consider when designing industrial sensors and field transmitters:

- Flexible configurability
- Simplicity
- Accuracy
- Ruggedness

The TIDA-00559 TI Design has a unipolar (0 V to 10 V, plus 10% overrange) target specification for its voltage output. This specification enables the use of a unipolar, positive power on the board. This feature is in contrast to other designs that use a bipolar positive and negative onboard power. The TIDA-00559 also contains a dedicated protection against high-energy overvoltage transients (surge) as a feature that differentiates this design from other similar designs.

The dominating output interfaces used in industrial sensors and transmitters are current outputs and voltage outputs. One trend is to offer sensors containing both output types to allow universal use of a sensor. This type of output interface also includes the simultaneous usage of the two types of outputs by feeding them simultaneously into two separate programmable logic controller (PLC) analog inputs of the respective type. This requires a field transmitter to have a separate output pin for each of the two different output signals.

In contrast to the latter type of usage, the combined voltage and current output of this TIDA-00559 design targets use cases where the end customer does not intend to use the two different types of outputs simultaneously. As a result of this design specification, both outputs share a common output pin (OUT), as Figure 1 shows.

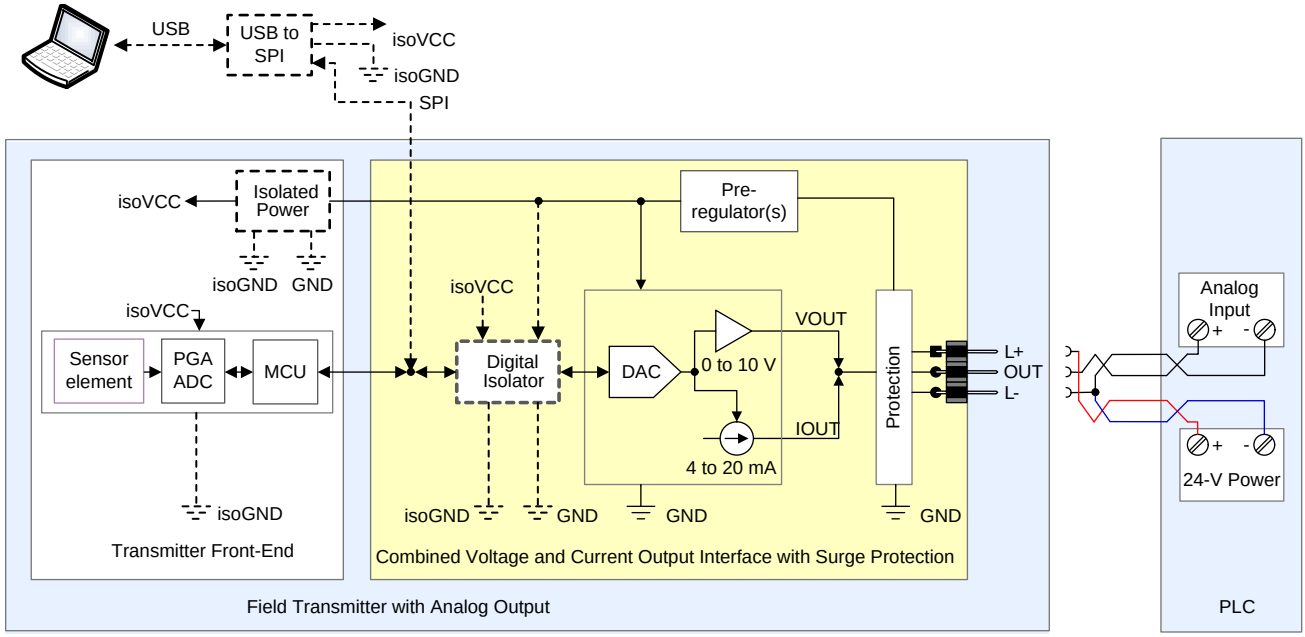


Figure 1. System Diagram—Exemplary Use of Combined Voltage and Current Output Interface With Surge Protection in Complete Transmitter and PLC System

The user must decide which of the two output types are optimal for use in a design application. The options for output use are either voltage output (VOUT) or current output (IOUT). The user can select the output type through software configuration, which allows a large degree of flexibility. The system example in Figure 1 uses an optional personal computer (PC) for this purpose. In addition to configuring the output type, the user can also set other parameters, such as output ranges, dynamic behavior, calibration, and error handling with ease using this method. In a real application, the voltage or current output interface is controlled from the analog front end, which sends the configuration and digital data to the digital-to-analog converter (DAC).

The TIDA-00559 design uses a 16-bit DAC to provide the level of accuracy required for such current or voltage outputs. The DAC uses a four-wire serial peripheral interface (SPI) for communication with the transmitter front end or with the optional PC. The SPI has been galvanically isolated to break potential ground loops and enable a trouble-free evaluation of the design. The isolation can be considered as optional. In real systems it needs to be decided case–by-case whether the isolation is required.

One unique challenge to consider for all sensor interfaces is their protection against overvoltage from switching and lightning transients (surge). This TIDA-00559 TI Design contains dedicated protection circuitry that has been designed to fulfill the IEC61000-4-5 requirements for such overvoltage conditions. The combined voltage and current output provide~~!~s~~ a significant advantage in that they both share a common protection block. This advantage significantly reduces the required effort for the surge protection of the complete design. This protection feature is not the only way this design distinguishes itself from the already existing combined voltage or current output designs [4]. The TIDA-00559 differs from all other existing designs that use this type of DAC by the method with which the design powers the analog part of the used DAC. Other designs with the same DAC focus on bipolar output voltage ranges (–5 V to +5 V and –10 V to +10 V), which requires a bipolar supply of the DAC; however, this TIDA-00559 design clearly targets a unipolar 0- to 10-V output range (plus 10% overrange) for the voltage output. With these design specifications, a unipolar, positive analog VDD (AVDD) supply is used to power the DAC.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
ANALOG OUTPUT SIDE		
Power		
Operating supply voltage (L+ to L–)	15- to 35-V DC	See Table 7
Reverse polarity protection	Yes	See Section 1.5.2.9
Power good indicator	Green indicator LED	See Section 1.5.4
Voltage Output		
Output voltage range	0 V to 5 V, 0 V to 10 V	See [2]
Overrange	0 V to 5.5 V, 0 V to 11 V	
Minimum load resistance	1 kΩ	See Table 7
Current Output		
Maximum load resistance	320 Ω	See Table 7
Output current range	4 mA to 20 mA, 0 mA to 20 mA, 0 mA to 24 mA	See [2]
Software Configurable Features	Calibration (gain and zero), frame error checking, watchdog timer, software reset, voltage output ranges, current output ranges, overrange, and slew rate control	
Alarm		
Alarm indicator	Red indicator LED	See [2]
General alarm events	SPI watchdog timer timeout, SPI frame error, and overtemperature	
Current output alarm events	Output open circuit, maximum load resistance violation	
Transient overvoltage protection	Designed to meet IEC61000-4-5, ±1 kV, coupled as differential mode signal through 40 Ω between L+/L–, L+/OUT, and OUT/L–	See Section 1.5.2
ISOLATED SPI		
Power		See [1]
Operating voltage (isoVCC – isoGND)	3- to 5.5-V DC	
Others		
Reverse polarity protection	No	
Rated isolation	Determined by ISO7641FC, board construction, test condition and isolation standard applied, see [1]	
Input threshold	Based on used digital isolator ISO7641FC	
High-level output voltage		
Low-level output voltage		
ENVIRONMENT		
Ambient temperature	–40°C to 85°C	See Section 1.5.2

1.3 Block Diagram

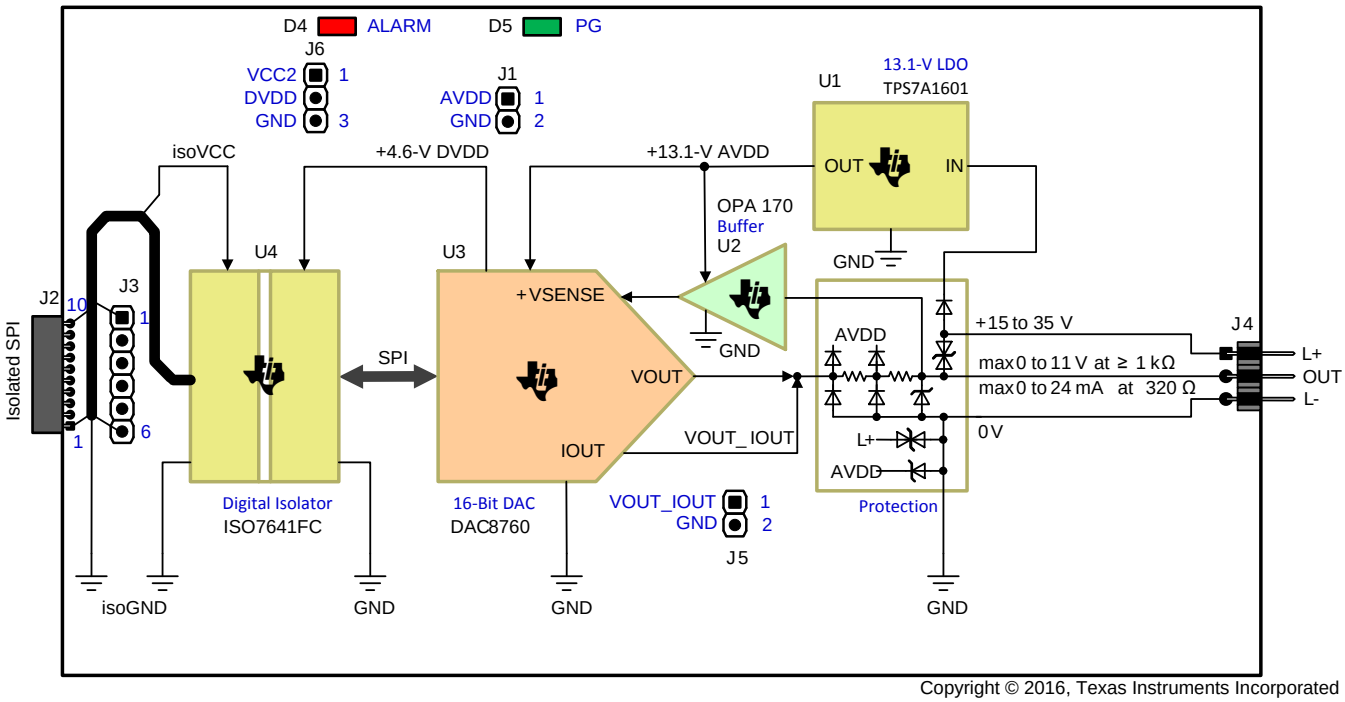


Figure 2. TIDA-00559 Detailed Block Diagram—Combined Voltage and Current Output With Surge Protection

1.3.1 Isolated Serial Peripheral Interface (SPI)

The isolated SPI (serial peripheral interface) available on J2 and J3 is the digital input interface of the design. This interface is used to configure the DAC and to write and read data into and from the internal registers of the DAC.

The feature of isolation is used to avoid potential issues during testing, evaluation, or in real use cases. Such issues can be caused by ground loops or leakage currents across isolation. Such issues may build up in external systems during testing or in a real transmitter application when the sensor element has made direct contact to grounded systems or a connection to any other voltage rail.

In addition to configuration and data communication, the interface on J2 and J3 is used to power the isolated side of the digital isolator U4 with isoVCC and isoGND.

The isolated supply voltage (isoVCC) and the associated ground (isoGND) in Figure 1 and Figure 2 can be provided in one of two ways:

- Connection to a PC through TI's SM-USB DIG Platform [5] with the dedicated 10-pin receptacle J2 of the isolated SPI
- Connection with a transmitter front end connected to the 6-pin header J3 of this interface

Using other test systems instead of these two approaches is also feasible if such test systems provide the isoVCC and isoGND for U4 and provided that the voltage and logic levels match the specifications for U4 as given in its data sheet.

The DAC U3 provides the 4.6-V DVDD and this 4.6-V DVDD powers the non-isolated side of the digital isolator U4.

1.3.2 Protection

The protection circuit block connects directly to connector J4 of the TIDA-00559 design, which connects the design with the analog input of a PLC and a 24-V power supply. The purpose of the protection block is to make the design more robust against transient overvoltages resulting from switching and lightning transients (surge) as well as to provide reverse polarity protection for the low-dropout regulator (LDO) U1.

The circuit has been designed to fulfill the requirements of IEC61000-4-5, considering a differential mode surge of up to ±1 kV coupled by 40 Ω. This protection has been achieved by clamping the overvoltage with transient voltage suppressor (TVS) diodes directly on any pair of two pins of J4. Protecting the DAC (U3) outputs (VOUT and IOUT) requires additional measures. In addition to the clamping with diodes, these outputs are also protected by a cascaded network of current limiting resistors and diodes, which steer the current to GND or AVDD. Because a current steering to AVDD causes the voltage on this rail to rise, an additional clamp is used on AVDD.

A small diode in series with the LDO input provides reverse protection of the LDO U1 power input (IN), which blocks any current when the external 24 V on the L+ and L– pins of J4 have been applied in the reverse direction.

1.3.3 16-Bit DAC and Buffer

The 16-bit DAC U3 is the heart of the TIDA-00559 TI Design. The device performs the conversion of the digital input data into its analog equivalents as voltage (VOUT) or current (IOUT) outputs. Both type of output signals are connected together and are represented by VOUT_IOUT. The configuration of the DAC specifies the specific type of output used, as well as the specific output range.

The output current on the IOUT of U3 equals the current on the OUT-pin of J4 when the DAC has been configured as current output and when neither the clamping diodes nor the steering diodes in the protection block are conducting current. The output current is not influenced by the current limiting resistors inside the protection block under these conditions.

This setup contrasts to the scenario of configuring U3 as the voltage output, where any current flow through the current limiting resistors inside the protection block causes a voltage drop across those resistors. This fluctuation causes the voltage on the OUT pin of J4 to deviate from the voltage on the VOUT pin of U3. The use of remote sensing for the voltage on the J4 OUT pin compensates for this voltage drop resulting from the load current. The sensed voltage on the J4 OUT pin is then fed into the +VSENSE pin of U3 for that purpose. The use of an additional op amp (U2) buffers the voltage measured on the OUT pin of J4.

The specific device which has been selected for U3 has an internal LDO to generate a 4.6-V rail. This internal LDO of U3 is used to power the non-isolated side of the digital isolator U4, which connects directly to the SPI of the DAC.

1.3.4 13.1-V LDO

The 13.1-V LDO (U1) is used to power the analog supply rail AVDD of the DAC (U3) with a low-noise voltage just high enough to support the targeted output voltage range of the TIDA-00559 design. The specific AVDD voltage level accounts for the voltage drop across the current limiting resistors of the protection block and also factors in the U3 compliance voltage and headroom voltage.

Table 1 and Table 7 provide the maximum voltage on the OUT pin of J4 with an 11-V specification when configuring the design as a voltage output with 10% overrange for a standard 0- to 10-V output.

When setting the design configuration as a current output, the OUT pin of J4 must be able to support voltages up to almost 7.7 V. This support requirement is based on the given specification for a 0- to 24-mA output current range for a current output and a load resistance of 320 Ω.

1.4 Highlighted Products

The following subsections detail each circuit block in the TIDA-00559 block diagram in further detail. For more information on each of these devices, see their respective product folders at www.ti.com.

1.4.1 ISO76x1 Low-Power Triple and Quad-Channel Digital Isolators

Description:

The ISO7631F and ISO7641F devices provide galvanic isolation up to 4242 V_{PK} per VDE. The ISO7631F device has three channels, two of which operate in the forward direction and one which operates in the reverse direction. The ISO7641F device has four channels, three of which operate in the forward direction and one of which operates in the reverse direction. Suffix F indicates that output defaults to low-state in fail-safe conditions. M-Grade devices are high-speed isolators capable of up to 150-Mbps data rates with fast propagation delays, whereas C-Grade devices are capable of up to 25-Mbps data rates with low power consumption and integrated filters for noise-prone applications. C-Grade devices are recommended for lower-speed applications where input noise pulses of less than 6 ns duration must be suppressed, or when low-power consumption is critical.

Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. The devices have TTL input thresholds and can operate from 2.7-V (M-Grade), 3.3-V and 5-V supplies. All inputs are 5-V tolerant when supplied from 3.3-V or 2.7-V supplies.

Features:

- Signaling rate: 150 Mbps (M-grade), 25 Mbps (C-grade)
- Robust design with integrated noise filter (C-grade)
- Low power consumption, typical I_{CC} per channel (3.3-V supplies):
  - ISO7631FM: 2 mA at 10 Mbps
  - ISO7631FC: 1.5 mA at 10 Mbps
  - ISO7641FC: 1.3 mA at 10 Mbps
- Extremely-low $I_{CC\_disable}$ (C-grade)
- Low Propagation delay: 7 ns typical (M-grade)
- Output defaults to low-state in fail-safe mode
- Wide temperature range: –40°C to 125°C
- 50 KV/µs transient immunity, typical
- Long life with SiO_2 isolation barrier
- Operates from 2.7-V (M-grade), 3.3-V and 5-V supply and logic levels
- 2.7-V (M-grade), 3.3-V and 5-V level translation
- Wide body SOIC-16 package
- Safety and regulatory approvals
  - 2500-V_{RMS} isolation for 1 min per UL 1577
  - 4242-V_{PK} basic insulation per DIN V VDE V 0884-10 and DIN EN 61010-1
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 End Equipment Standards
  - CQC Certification per GB4943.1-2011
  - TUV-3000 V_{RMS} reinforced insulation according to EN/UL/CSA 60950-1 and EN/UL/CSA 61010-1

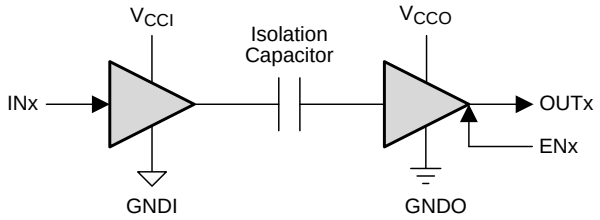


Figure 3. ISO76x1 Simplified Schematic

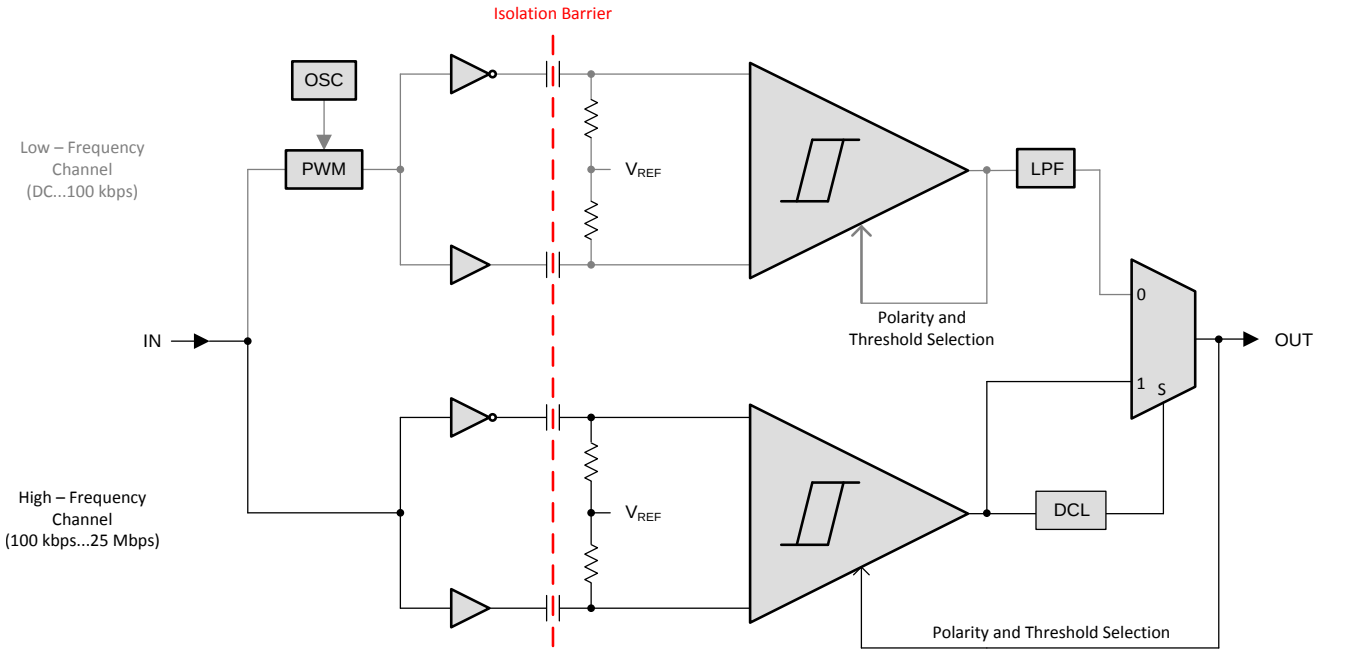


Figure 4. ISO7631FC and ISO7641FC Conceptual Block Diagram

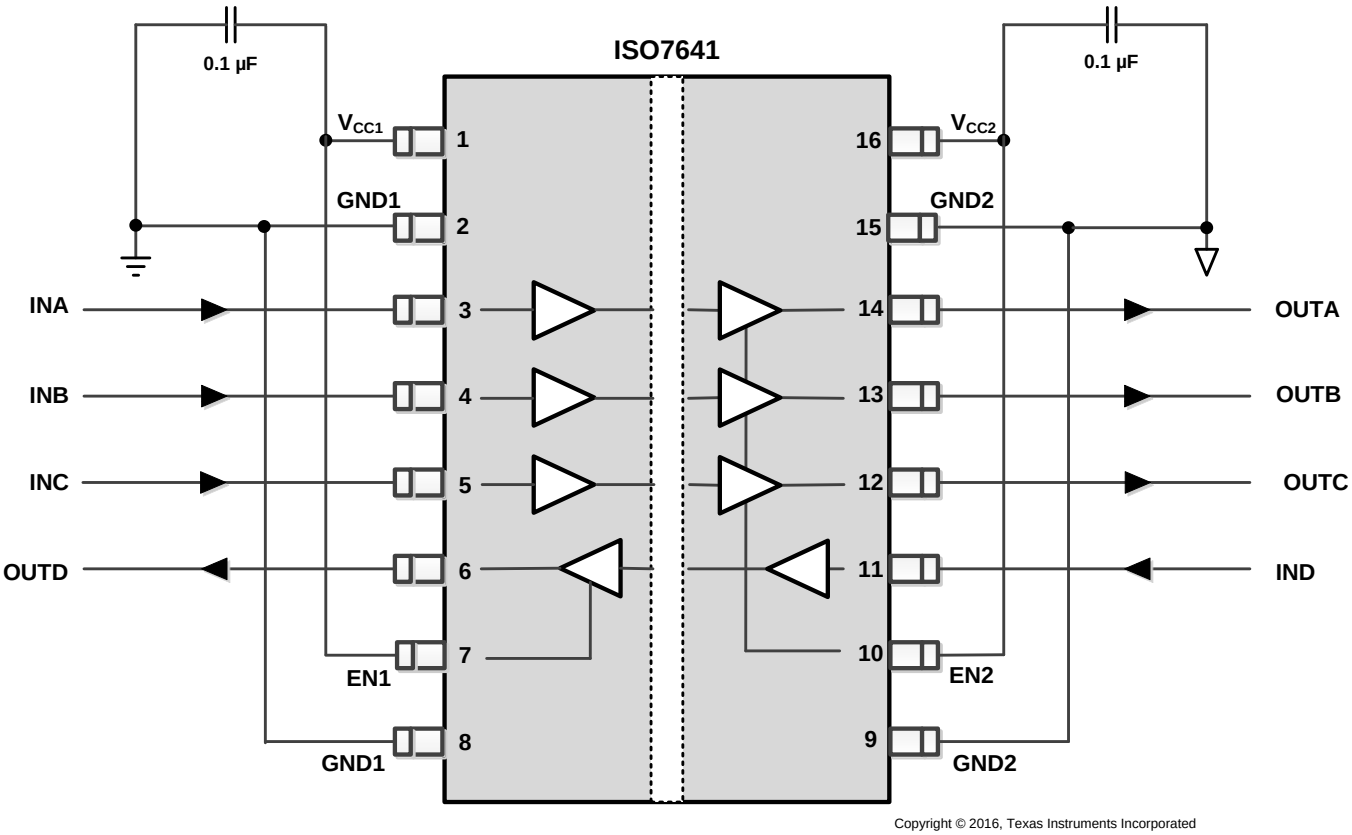


Figure 5. Typical ISO7641FC Circuit Hookup

1.4.2 Single-Channel, 12- and 16-Bit Programmable Current Output and Voltage Output DACs for 4-mA to 20-mA Current Loop Applications

Description:

The DAC7760 and DAC8760 are low-cost, precision, fully-integrated, 12-bit and 16-bit digital-to-analog converters (DACs) designed to meet the requirements of industrial process-control applications. These devices can be programmed as a current output with a range of 4 mA to 20 mA, 0 mA to 20 mA, or 0 mA to 24 mA; or as a voltage output with a range of 0 V to 5 V, 0 V to 10 V, ±5 V, or ±10 V with a 10% overrange (0 V to 5.5 V, 0 V to 11 V, ±5.5 V, or ±11 V). Both current and voltage outputs can be simultaneously enabled while being controlled by a single data register.

These devices include a power-on-reset function to ensure powering up in a known state (both IOUT and VOUT are disabled and in a Hi-Z state). The CLR and CLR-SEL pins set the voltage outputs to zero-scale or midscale, and the current output to the low end of the range, if the output is enabled. Zero and gain registers can be programmed to digitally calibrate the device in the end system. The output slew rate is also programmable by register. These devices can superimpose an external HART® signal on the current output and can operate with either a single 10-V to 36-V supply, or dual supplies of up to ±18 V. All versions are available in both 6-mm × 6-mm 40-pin VQFN and 24-pin HTSSOP packages.

Features:

- Current output: 4 mA to 20 mA;
  0 mA to 20 mA; 0 mA to 24 mA
- Voltage output:
  - 0 V to 5 V; 0 V to 10 V; ±5 V; ±10 V
  - 0 V to 5.5 V; 0 V to 11 V; ±5.5 V; ±11 V
    (10% overrange)
- ±0.1% FSR total unadjusted error (TUE) maximum
- DNL: ±1 LSB maximum
- Simultaneous voltage and current output
- Internal 5-V reference (10 ppm/°C, maximum)
- Internal 4.6-V power-supply output
- Reliability features:
  - CRC check and watchdog timer
  - Thermal alarm
  - Open alarm, short current limit
- Wide temperature range: –40°C to 125°C
- 6-mm × 6-mm 40-pin VQFN and 24-pin HTSSOP packages

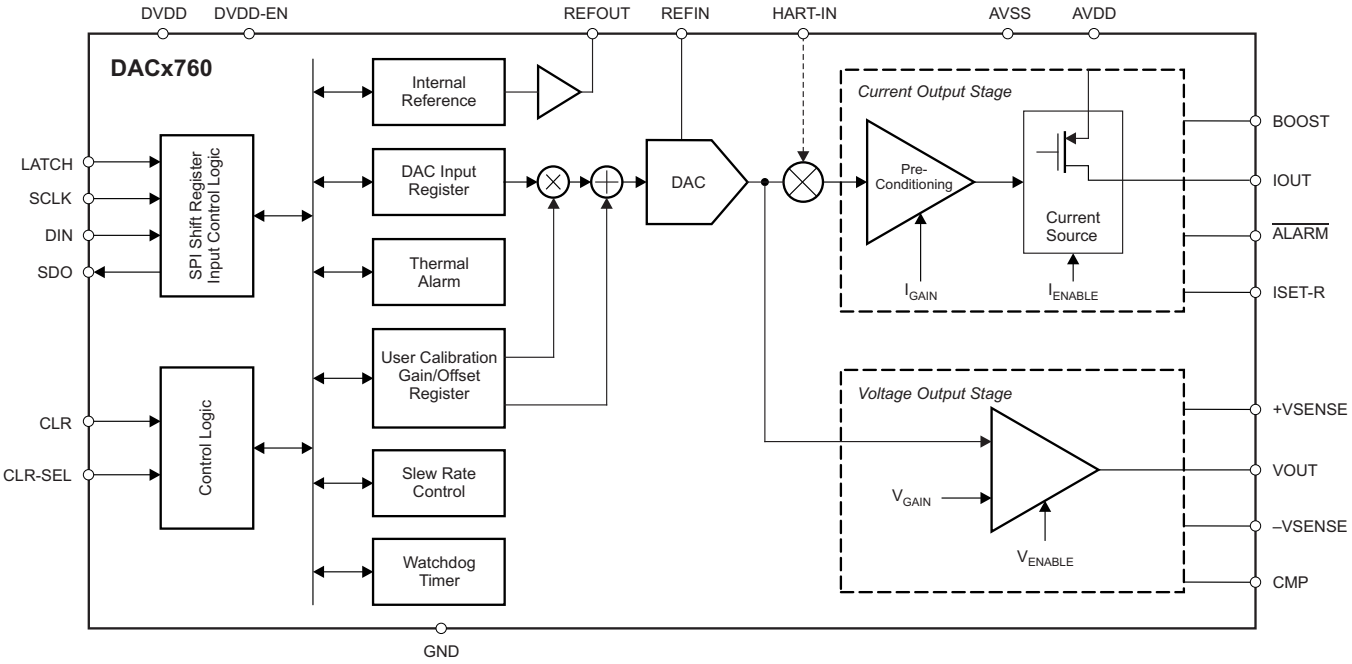


Figure 6. DACx760 Block Diagram

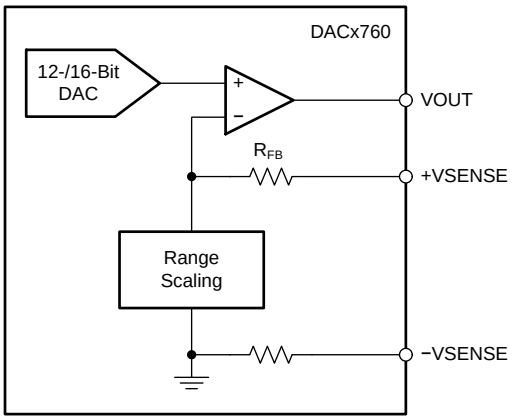


Figure 7. Voltage Output Mode

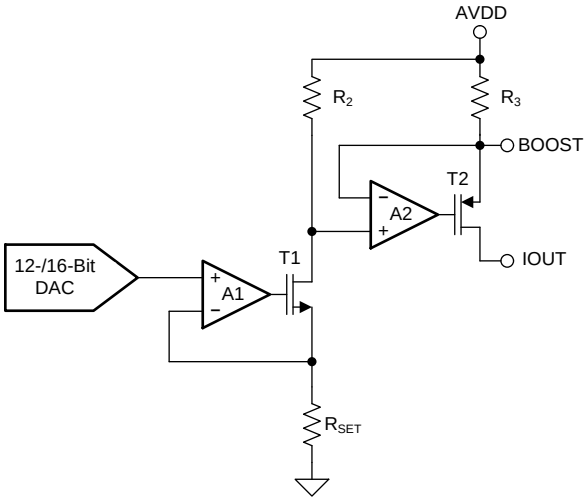


Figure 8. Current Output Mode

1.4.3 36-V, Single-Supply, SOT553, Low-Power Op-Amp Value Line Series

Description:

The OPA170, OPA2170, and OPA4170 devices (OPAx170) are a family of 36-V, single-supply, low-noise operational amplifiers that feature micro packages with the ability to operate on supplies ranging from 2.7 V (±1.35 V) to 36 V (±18 V). They offer good offset, drift, and bandwidth with low quiescent current. The single, dual, and quad versions all have identical specifications for maximum design flexibility.

Unlike most operational amplifiers, which are specified at only one supply voltage, the OPAx170 family of operational amplifiers is specified from 2.7 V to 36 V. Input signals beyond the supply rails do not cause phase reversal. The OPAx170 family is stable with capacitive loads up to 300 pF. The input can operate 100 mV below the negative rail and within 2 V of the positive rail for normal operation. Note that these devices can operate with full rail-to-rail input 100 mV beyond the positive rail, but with reduced performance within 2 V of the positive rail. The OPAx170 operational amplifiers are specified from –40°C to 125°C.

Features:

- Supply range: 2.7 V to 36 V, ±1.35 V to ±18 V
- Low noise: 19 nV/$\sqrt{\text{Hz}}$
- RFI filtered inputs
- Input range includes the negative supply
- Input range operates to positive supply
- Rail-to-rail output
- Gain bandwidth: 1.2 MHz
- Low quiescent current: 110 µA per amplifier
- High common-mode rejection: 120 dB
- Low bias current: 15 pA (maximum)
- Industry-standard packages:
  - 8-pin SOIC
  - 8-pin MSOP (VSSOP)
  - 14-pin TSSOP
- *micro*Packages
  - Single in 5-pin SOT553
  - Dual in 8-pin VSSOP

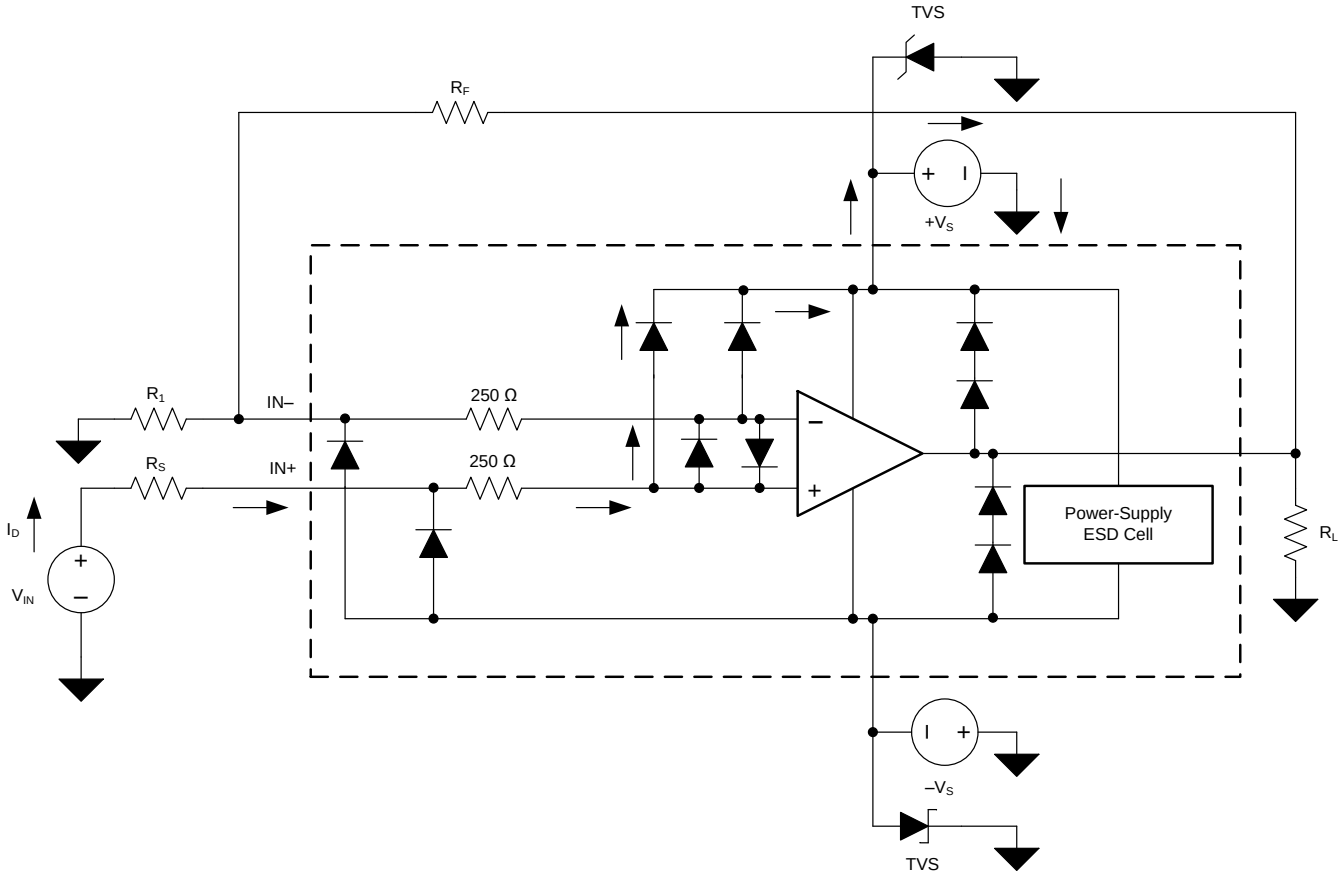


Figure 9. Electrical Overstress—Equivalent Internal ESD Circuitry Relative to Typical Circuit Application

1.4.4 TPS7A16 60-V, 5-µA I_Q, 100-mA, Low-Dropout Voltage Regulator With Enable and Power-Good

Description:

The TPS7A16 family of ultralow power, low-dropout (LDO) voltage regulators offers the benefits of ultra-low quiescent current, high input voltage and miniaturized, high thermal-performance packaging.

The TPS7A16 family is designed for continuous or sporadic (power backup) battery-powered applications where ultralow quiescent current is critical to extending system battery life.

The TPS7A16 family offers an enable pin (EN) compatible with standard CMOS logic and an integrated open drain active-high power good output (PG) with a user-programmable delay. These pins are intended for use in microcontroller-based, battery-powered applications where power-rail sequencing is required.

In addition, the TPS7A16 is ideal for generating a low-voltage supply from multicell solutions ranging from high cell-count power-tool packs to automotive applications; not only can this device supply a well-regulated voltage rail, but it can also withstand and maintain regulation during voltage transients. These features translate to simpler and more cost-effective, electrical surge-protection circuitry.

Features:

- Wide input voltage range: 3 V to 60 V
- Ultralow quiescent current: 5 µA
- Quiescent current at shutdown: 1 µA
- Output current: 100 mA
- Low dropout voltage: 60 mV at 20 mA
- Accuracy: 2%
- Available in:
  - Fixed output voltage: 3.3 V, 5 V
  - Adjustable version from 1.2 V to 18.5 V
- Power-good with programmable delay
- Current limit and thermal shutdown protections
- Stable with ceramic output capacitors: ≥ 2.2 µF
- Packages: high thermal performance MSOP-8 and SON-8 PowerPAD™
- Operating temperature range: –40°C to 125°C

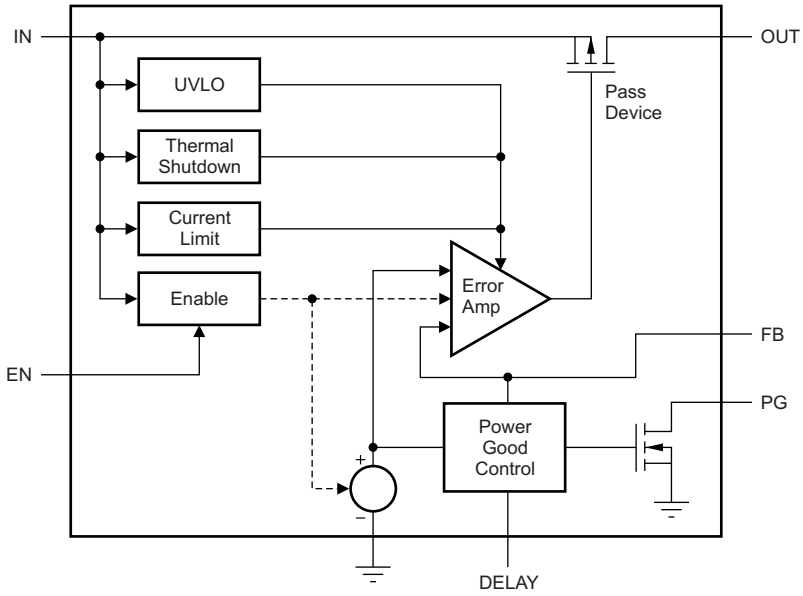


Figure 10. TPS7A16 Block Diagram

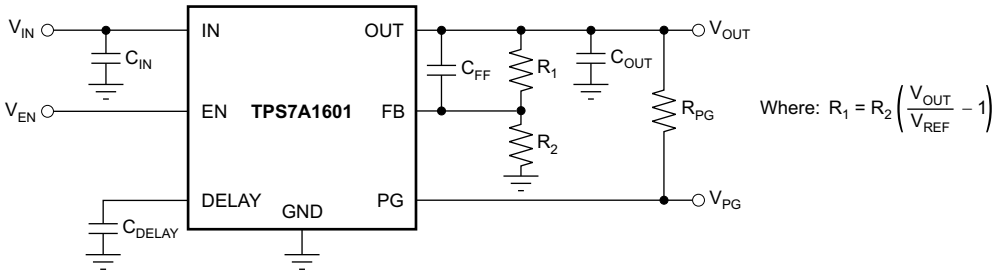


Figure 11. TPS7A1601 Circuit as Adjustable Regulator Schematic

1.5 Design Considerations

The following subsections describe the specific design considerations which have been applied to the design of each of circuit blocks addressed in previous subsections as well as their interactions in the context of the complete system. The circuit design relies heavily on the components selected (see Section 1.4) and vice versa.

1.5.1 Isolated SPI

Figure 12 shows the implementation of the isolated SPI.

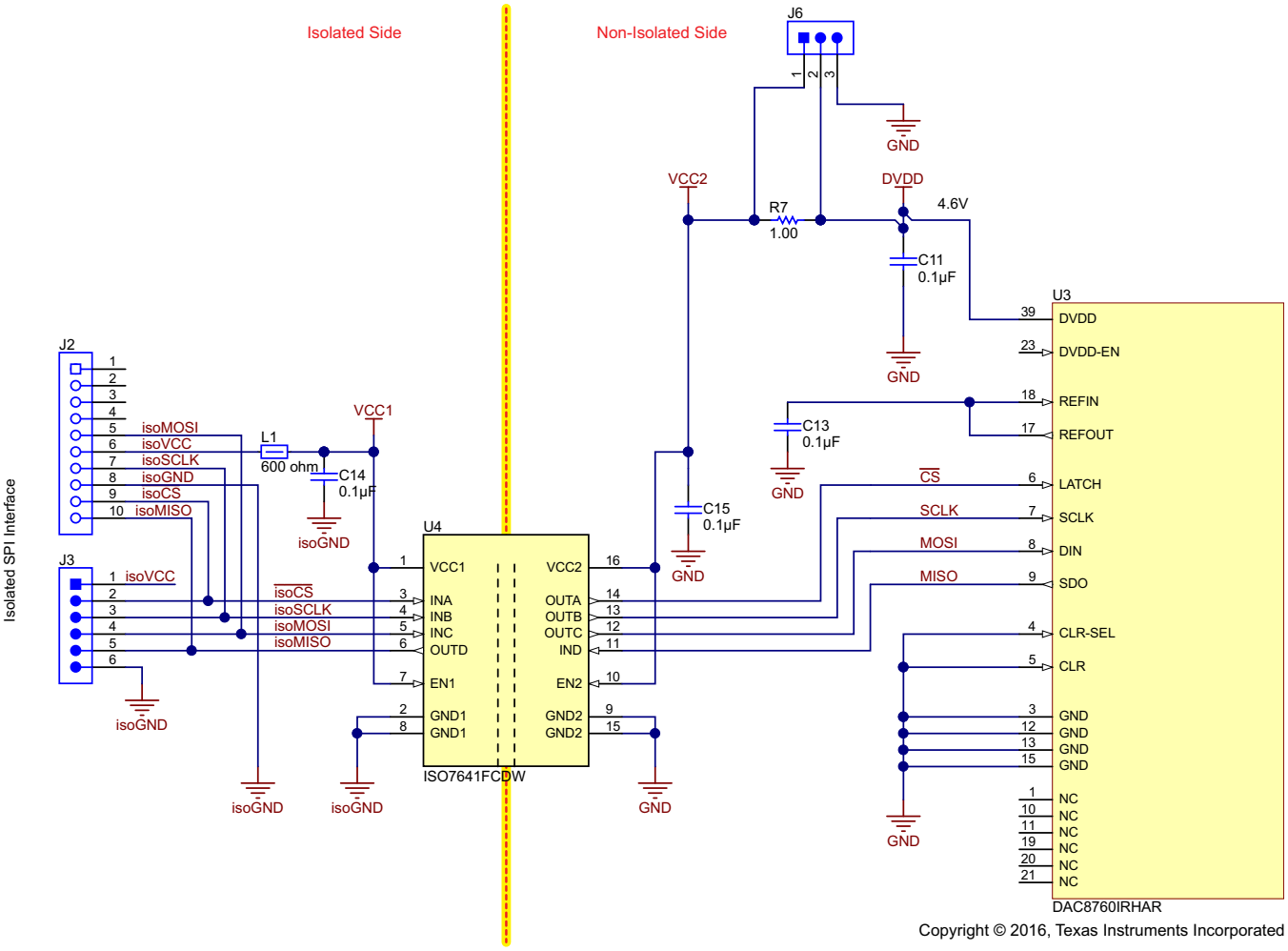


Figure 12. Implementation of Isolated SPI

An ISO7641FC [1] quad-channel digital isolator has been used to link the four logic SPI signals from the isolated SPI (connectors J2 and J3) in an isolated manner to the non-isolated SPI of the 16-bit DAC U3, as Table 2 shows.

One note of importance is that the power rails and the respective grounds on the isolated side and the non-isolated side are not related to each other. Different sources power these sides and they can even be powered with different voltage levels on the isolated and non-isolated side provided that these voltage levels fulfill the requirements as specified in the ISO7641FC data sheet [1].

The level of isolation on this TIDA-00559 TI Design depends on the board construction and layout as well as the used digital isolator U4. The datasheet of the ISO7641FC specifies different isolation and insulation levels and ratings for the device, depending on which standard and test conditions had been applied.

The fixed 4.6-V DVDD generated from the internal linear DVDD regulator of U3 powers the VCC2 on the non-isolated side.

The isolated SPI powers the VCC1 on the isolated side by either using the SM-USB-DIG Platform from TI [5] connected to the 10-pin receptacle J2 or by using a transmitter front end connected to the 6-pin header J3. The user can implement any other system or approach instead of a transmitter front end; however, such an alternative system must be able to provide the isolated power rails isoVCC and isoGND to power the isolated side of U4, as well as to provide the required signals to control the U3 DAC.

VCC1 and VCC2 are bypassed by 100-nF multi-layer ceramic capacitors (MLCCs) and decoupled by a ferrite bead (L1) on the isolated side and a 1-Ω resistor (R7) on the non-isolated side.

R7 also serves as a current shunt to enable measuring the current consumption of VCC2 using the header J6 (pin 2 referred to pin 1). This measurement can be used to ensure that the output current of the U3 DVDD regulator is below its 10-mA limit. J6 also enables a voltage measurement for DVDD between its pin 2 and pin 3.

Table 2. SPI—Signal and Pin Assignment

ISOLATED SIDE						NON-ISOLATED SIDE		
SM-USB-DIG						TIDA-00559		
CONNECTOR H2			CONNECTORS J2 AND J3			DAC8760 U3		
SIGNAL[1]	DESCRIPTION	PIN[1]	SIGNAL	J2 PIN	J3 PIN	SIGNAL[2]	DESCRIPTION	PIN[2]
VDUT	Switchable DUT power supply: +3.3 V, +5 V, or Hi-Z (disconnected)[3]	6	isoVCC[4]	6	1	DVDD44[4]	Digital power supply	39
SPI_CS1	SPI chip select signal ($\overline{CS}$)	9	isoCS	9	2	LATCH	Load DAC registers input. A rising edge on this pin loads the input shift register data into the DAC data and control registers and updates the DAC outputs.	6
SPI_CLK	SPI clock signal (SCLK)	7	isoSCLK	7	3	SCLK	Serial clock input	7
SPI_DOUT 1	SPI data output (MOSI)	5	isoMOSI	5	4	DIN	Serial data input. Data are clocked into the 24-bit input shift register on the rising edge of the serial clock input.	8
SPI_DIN1	SPI data input (MISO)	10	isoMISO	10	5	SDO	Serial data output. Data are valid on the rising edge of SCLK	9
GND[5]	Power return (GND) of SPI-Master	8	isoGND[4]	8	6	GND[4][5]	Ground reference point for all digital circuitry of the device.	3

(1) Signal names and pin numbers as used in SM-USB-DIG Platform User's Guide [5]
(2) Signal names as used in the DAC8760 data sheet of [2]; pin numbers are given for the QFN-40 package
(3) When VDUT is Hi-Z, all digital I/O are Hi-Z as well
(4) Signals are completely independent from each other
(5) Signal names are determined by the documents from which they derive. Although the same signal names (GND) are used, both signals are not identical but completely independent from each other.

1.5.2 Protection

One of the main goals of this TIDA-00559 TI Design is to show how the sensitive voltage and current output pins of the DAC (U3) can be protected against transient overvoltages caused by switching and lightning transients (surge). This level of protection differentiates this design from other existing designs, which focus on protection against electrostatic discharge (ESD) and electrical fast transients (EFTs), but do not cover the topic of surge protection.

Addressing the challenges that surges pose required making certain concessions to the TIDA-00559 circuit design to make it more robust against differential mode (DM) surges of up to ±1 kV coupled by 40 Ω. Protection against DM surges is not an explicit requirement by all applicable standards; however, it is good design practice. Additionally, any common-mode (CM) surge which has been applied to J4 turns into DM overvoltage transients as a result of any imbalance in the circuitry.

Figure 13 shows an exemplary test setup based on the *IEC 61000-4-x Test for TI's Protection Devices* application report [10]. Switch S1 must be in any of the DM x position and switch S2 must be in any position other than the same DM x position of S1.

Switch S1 must be in the CM position for CM surge testing. The mechanical construction of the case and the mounting of the board inside the case have a major impact on the CM surge susceptibility; therefore, the protection against CM surges is not covered by this design.

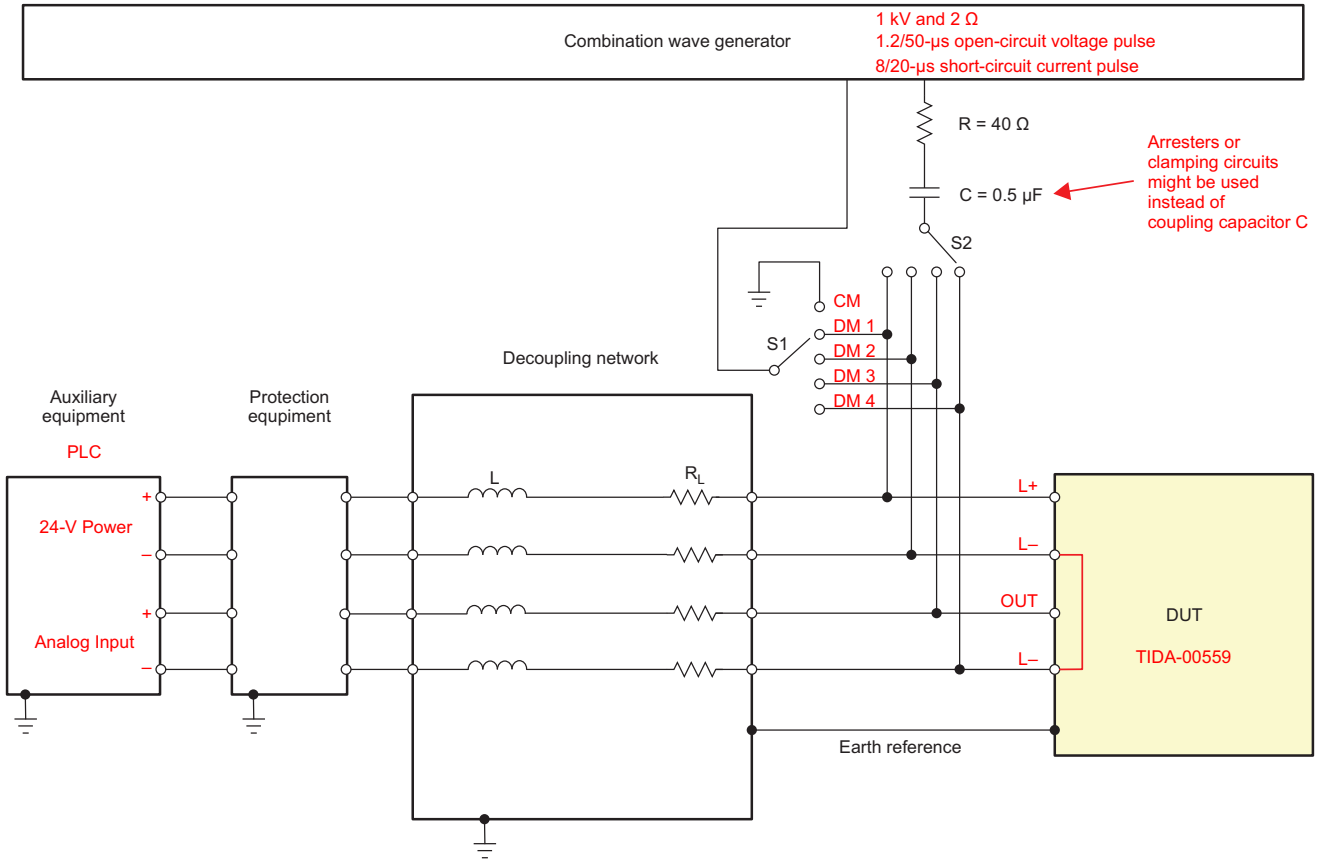


Figure 13. Exemplary Test Setup for Surge Testing TIDA-00559

1.5.2.1 General Considerations for Selection of Protection Components

Including the measures for circuit protection generally makes the design more robust. However, in other situations, some side effects may inadvertently influence or even degrade the system performance and system parameters on the other side. To avoid such side effects, be sure to carefully consider the specific protection approach and selection of protection components.

Some of the primary concerns when selecting the protection approach and protection components are:

1. Effectiveness over the complete specified operating temperature range of the application:
   The majority of clamping voltages, forward voltages, leakage currents, and other parameters do have a distinct temperature dependency, which is often not very well specified. A proper margin must be factored in to counterbalance for imperfect, or missing device specifications.
2. Effectiveness of the protection under different operating conditions:
   This must include operation when powered with voltages over their full operating voltage range as well as non-powered conditions. Under non-powered conditions, the current through steering diodes can be larger and devices can possibly be powered from (clamped) voltages appearing on their outputs, which causes internal protection diodes to conduct this voltage from its output to the power input of the device.
3. Effectiveness even in conjunction with internal protection circuits inside the sensitive devices to be protected:
   The internal protection is often not strong enough to cover full surge protection. When selecting the added protection, the user must ensure that the internal protection actually becomes disburdened.
4. The effect of leakage current of clamping devices at or below their standoff voltage must be negligible. This consideration is especially critical for a current output.
5. The effect of voltage drops caused by current limiting devices (resistors) must be negligible. This consideration is especially critical for voltage output.
6. The power dissipation caused by the maximum value of the operating voltage and resulting leakage or breakdown current through a clamping device must be insignificant.
7. Proper clamping of voltage at the application specific peak pulse current
8. Proper clamping of voltage rails to which current is steered:
   The use of steering diodes steers current either to a voltage rail or to ground. Current steering to a voltage rail causes the voltage of this rail to rise and can violate recommended operating conditions or absolute maximum ratings of devices connected to that voltage rail.
9. Capability of clamping devices, steering devices, and current limiting components to handle the surge currents for the given timing of the surge pulses:
   This consideration is not only a topic for the selection of clamping diodes and steering diodes, but also for current limiting resistors in the current path.

1.5.2.2 Voltage Clamping on Interface Connector J4

The ±1-kV surge voltage is much larger than any voltage level which the used devices (DAC, LDO, op amp, and the digital isolator) are able to withstand. The combination wave generator (CWG) outputs a 1.2/50-µs open-circuit voltage pulse, which leads to an 8/20-µs short-circuit current pulse. The width of these pulses may appear short, but is long and severe enough to cause even catastrophic failure of any of the devices in use. The peak surge current is limited by the impedance of the path in which the surge flows, which is in total 42 Ω. This 42 Ω is the sum of the 2-Ω internal impedance of the combination wave generator plus the 40-Ω resistance, which the coupling network adds externally. Equation 1 calculates the resulting surge current:

$$I_{SURGE} = \frac{V_{Surge}}{Z_{Total}} = \frac{\pm 1\ kV}{40\ \Omega + 2\ \Omega} \approx \pm 23.8\ A \quad (1)$$

where:

- I_{SURGE} is the surge current at a specific impedance Z_{Total} of the path where the surge current flows
- V_{Surge} is the open circuit surge voltage generated by the combination wave generator (CWG)
- Z_{Total} is the sum of the CWGs internal 2 Ω and any external impedance in the path where the surge current flows.

To protect the design against this high surge voltage, any incoming differential surge voltage is clamped directly on the interface connector J4. The TVS diodes D8, D9, and D10 have been purposed for clamping between any two pins of J4 in this design, as Figure 14 shows.

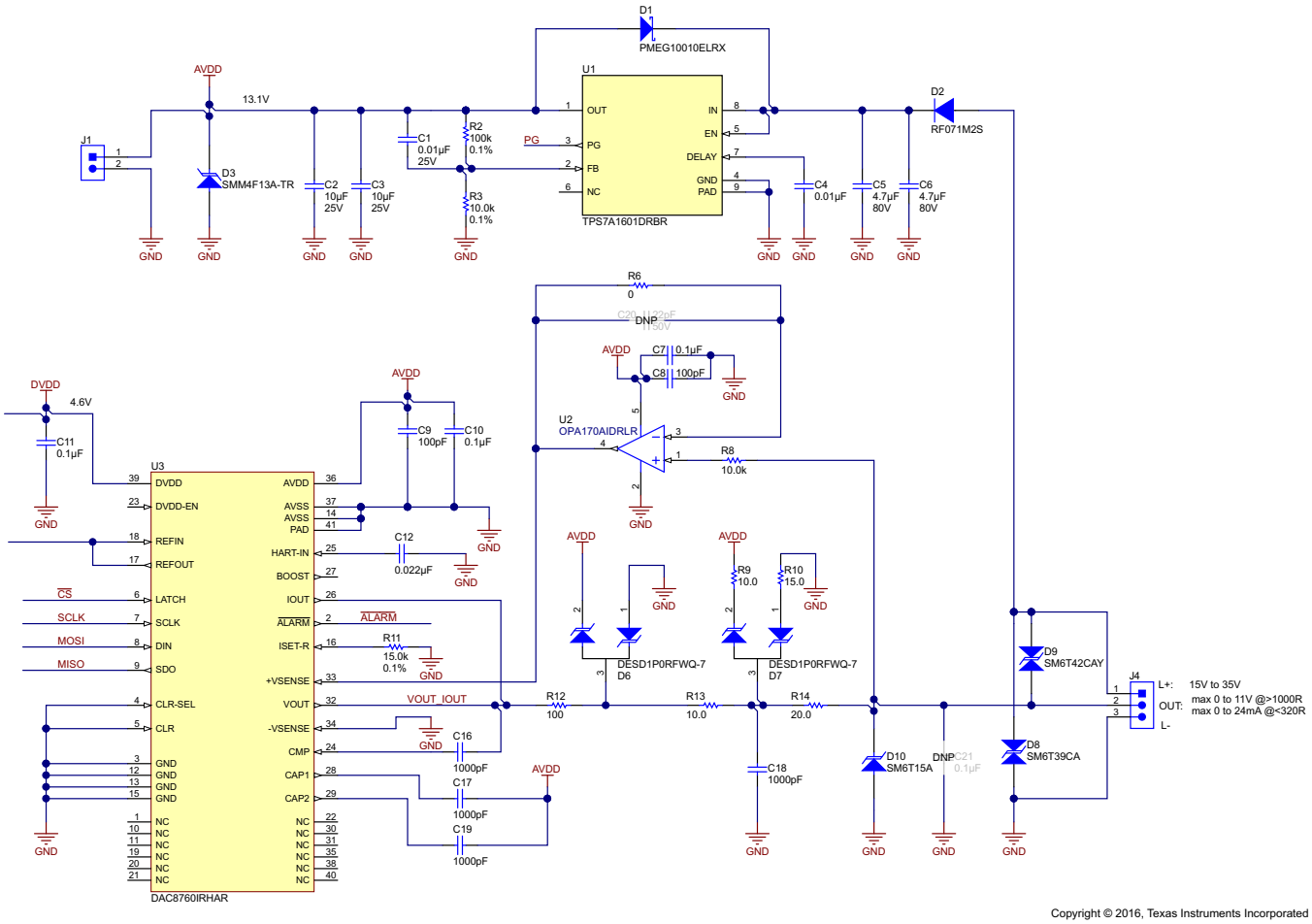


Figure 14. Protection Circuitry With Protected Devices

The following subsection outlines the dedicated considerations for the selection of protection components and their specific implementation into the TIDA-00559 design.

1.5.2.3 D8—Voltage Clamping Between L+ and L–

The diode D8 provides the basic clamping of the nominal 24-V supply voltage of the design. This design uses the SM6T39CA transient voltage suppressor diode (TVS) from the SM6T family [8] and with specifications as follows in Table 3.

Table 3. SM6T39CA Parameters—D8

ITEM	PARAMETER	DESCRIPTION	CONDITIONS	VALUES
1	Type of diode	—	—	Bidirectional TVS
2	I_{RM} max at V_{RM}	Maximum leakage current at standoff voltage	T = 85°C; V_{RM} = 33.3 V	Max 1 µA
3	V_{BR} min, typ, and max at I_R	Minimum, typical, and maximum breakdown voltage at reverse current	T = 25°C; I_R = 1 mA	Min 37.1 V, Typ 39 V, Max 41 V
4	V_{CL} max at I_{PP} and 8/20 µs	Maximum clamping voltage at peak pulse current and 8/20-µs current pulse waveform	T = 25°C; I_{P-P} =57 A, 8/20 µs	Max 69.7 V
5	P_{PP} max at 8/20 µs	Peak pulse power at 8/20-µs current pulse waveform	8/20 µs	Max 4 kW
6	R_D at 8/20 µs	Dynamic resistance at 8/20-µs current pulse waveform	T = 25°C, 8/20 µs	0.504 Ω
7	αT max	Maximum voltage temperature coefficient	T = 25°C	10×10^{-4}/°C
8	$R_{th(j-a)}$	Thermal resistance junction-to ambient	Recommended pad layout	100°C/W

The parameters in the preceding Table 3 vary in importance for the specific application purpose of D8.

Item 1 relates to one of the most important questions when selecting a TVS diode, which is whether to select the unidirectional or bidirectional type. A bidirectional TVS has been selected for this design to protect against any damage to the TVS in any situation where the 15- to 35-V supply voltage of the design has been applied in the reverse direction. D2 is inserted into the path between D8 and the LDO U1 to provide finally the reverse protection for the LDO.

If the designer selects a unidirectional TVS diode, the diode clamps the 15- to 35-V supply voltage after having been reversely applied to the forward voltage level of the TVS diode. This forward voltage is in the range of approximately 500 mV to 3 V and is determined by the forward current, which is equal to the current that the sourcing power supply is able to provide. This sort of condition damages unidirectional TVS diodes, which is an obvious conclusion.

Item 2 is the leakage current and is of little concern because it slightly increases the current consumption of the design but does not add any additional error to the voltage or current output of the design.

Item 3 is important and relates of to the continuous operation of the design at the maximum of the nominal operating voltage range of the design (35 V). The designer must ensure that the power dissipation of D8 is insignificant at this point. Operation of the TVS D8 at its typical breakdown voltage V_{BR} and the respective reverse current I_R = 1 mA results in a power dissipation, P_d, as the following Equation 2 shows:

$$P_d = V_{BR} \times I_R = 39\ V \times 1\ mA = 39\ mW \quad (2)$$

This power dissipation increases the junction temperature Tj in the following Equation 3 by:

$$\Delta T_j = P_d \times R_{th(j-a)} = 39\ mW \times 100\,°C / W = 3.9\,°C \quad (3)$$

where:

- P_d is the power dissipation
- V_{BR} is the breakdown voltage at a given reverse current I_R
- I_R is the reverse current
- ΔT_j is the change in junction temperature
- $R_{th(j-a)}$ is the thermal resistance junction to ambient

The resulting temperature increase of 3.9°C can be considered to be negligible. Considering the typical breakdown voltage and operation at the 35-V maximum operation voltage and at 25°C, the power dissipation in D8 is less. The power dissipation is almost zero because the 35-V maximum operation voltage is much less than the typical 39-V breakdown voltage. Nevertheless, the designer must note that the breakdown voltage has a tolerance range, as well. Even this tolerance range does not change the 0-mW power dissipation statement, because the 35-V maximum operation voltage is much less than the minimum breakdown voltage of 37.1 V at 25°C, too. Operation at temperatures less than 25°C requires to factor in the positive temperature coefficient (Item 7 of Table 3) of the breakdown voltage of D8

According to the D8 diode data sheet [9], the following Equation 4 calculates the breakdown voltage at a specific junction temperature:

$$V_{BR} \text{ at } T_j = V_{BR} \text{ at } 25°C \times \left(1 + \alpha T \left(T_j - 25°C\right)\right) \tag{4}$$

Applying this Equation 4 for the calculation of the worst-case, minimum breakdown voltage leads to the following Equation 5:

$$V_{BR\_min} \text{ at } -40°C = V_{BR\_min} \text{ at } 25°C \times \left(1 + \alpha T \left(-40°C - 25°C\right)\right)$$
$$= 37.1\ V \times \left(1 + 10 \times \frac{10^{-4}}{°C} \times \left(-40°C - 25°C\right)\right)$$
$$= 37.1\ V \times \left(1 + \frac{-0.065°C}{°C}\right) \cong 34.69\ V \tag{5}$$

where:

- αT is the temperature coefficient of the breakdown voltage
- T_j is the junction temperature
- V_{BR_min} is the minimum breakdown voltage.

The resulting 34.69-V worst-case minimum breakdown voltage calculated in Equation 5 is 0.31 V less than the 35-V maximum operation voltage. As a result, the reverse current is to be larger than the 1 mA, which leads to a higher power dissipation than the 39 mW calculated in Equation 2. To roughly approximate further details of this potential issue, the breakdown of D8 was simulated using TINA-TI™ simulation software. Figure 15 shows the respective TINA-TI schematic for this simulation, which shows the behavior at room temperature.

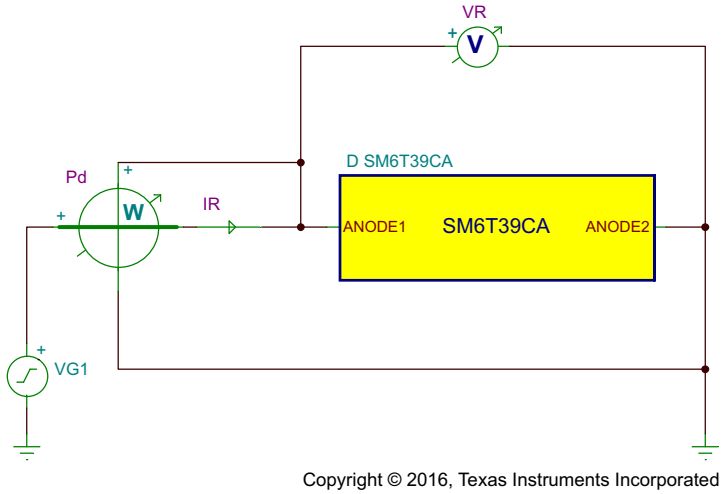


Figure 15. TINA-TI™ Schematic for Simulating Breakdown Behavior of D8

Figure 16 shows the simulation results, which clearly show a significant increase of the reverse current from 1 mA to 177 mA when the voltage across the diode has been increased from its breakdown voltage V_{BR} to V_{BR} + 311 mV.

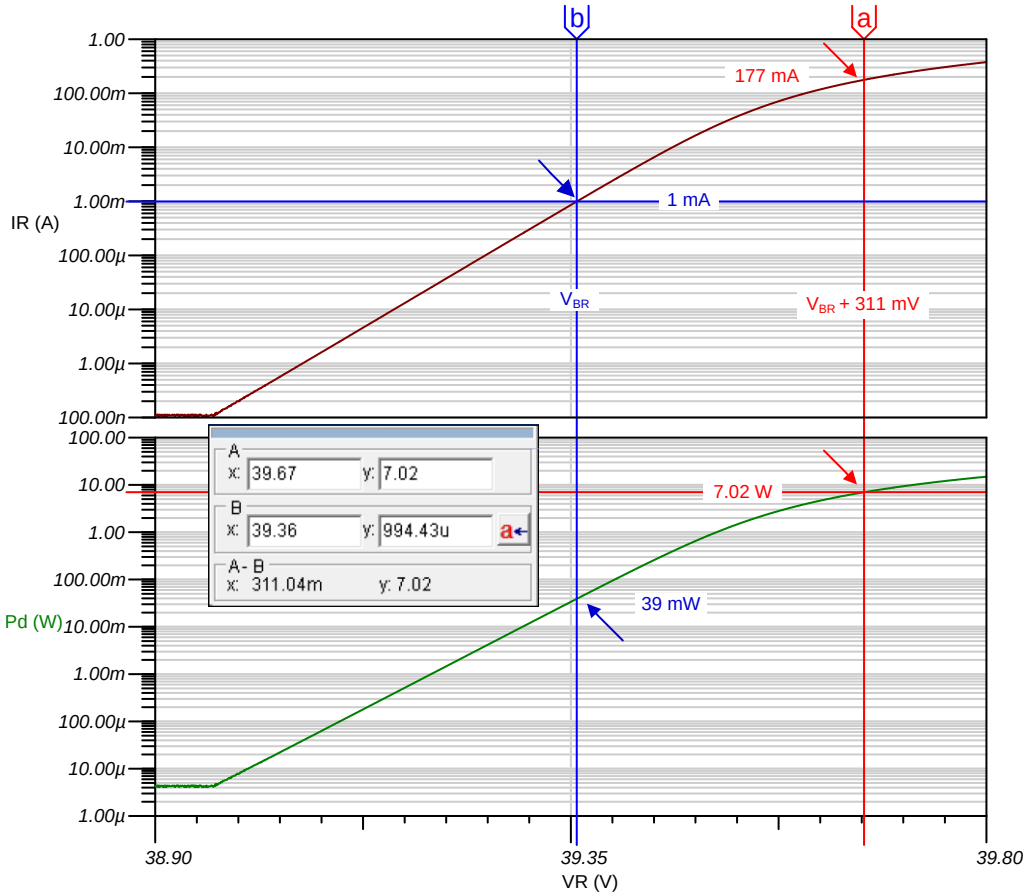


Figure 16. Breakdown of D8—Simulation Results for Reverse Current and Power Dissipation at Specified V_{BR} and Applied Voltage (311 mV Larger than V_{BR})

As a result of the reverse current increase, the power dissipation in D8 increases from the roughly 39 mW stated before to more than 7 W. Expect similar results during operation at –40°C when the maximum operating voltage of 35 V has been applied while the minimum VBR at –40°C is expected to be approximately 34.69 V (see Equation 5). Assuming such a condition to be a continuous operating condition, consider that the D8 is not capable for use because of a resulting continuous 7-W power dissipation, which leads to an increase in junction temperature of 702°C, as Equation 6 calculates:

$$\Delta T_j = P_d \times R_{th(j-a)} = 7.02\ W \times 100^{\circ}C/W = 702^{\circ}C \quad (6)$$

Fortunately, the positive temperature coefficient αT (Item 7) of the breakdown voltage V_{BR} does help and counteracts this impasse. The underlying theory is that any power dissipation in D8 increases its junction temperature. Because of the positive αT of the V_{BR} (at which the reverse current equals 1 mA, per definition), the V_{BR} rises according to Equation 4.

Rearranging this Equation 4 to find the junction temperature at which the worst-case minimum breakdown voltage of D8 equals the maximum operating voltage of the design (35 V) leads to the calculations in the following Equation 7, Equation 8, and Equation 9.

$$T_j = \frac{V_{BR} \text{ at } T_j - V_{BR} \text{ at } 25°C}{V_{BR} \text{ at } 25°C \times \alpha T} + 25°C \tag{7}$$

$$V_{BR} \text{ at } T_j = V_{L+\_max} \tag{8}$$

$$T_j = \frac{V_{L+\_max} - V_{BR} \text{ at } 25°C}{V_{BR} \text{ at } 25°C \times \alpha T} + 25°C = \frac{35 \text{ V} - 37.1 \text{ V}}{37.1 \text{ V} \times 10 \times \frac{10^{-4}}{°C}} + 25°C = \frac{-2.1 \text{ V}}{37.1 \text{ V} \times 10 \times \frac{10^{-4}}{°C}} + 25°C$$

$$T_j = -56.6°C + 25°C = -31.6°C \tag{9}$$

The result given by Equation 9 shows that the minimum breakdown voltage is 35 V at a junction temperature of D8 of –31.6°C. This temperature is far from the room temperature of 25°C, which means there is a sufficient margin.

Thee three calculations from the preceding Equation 7, Equation 8, and Equation 9 are first approximations only but show the principle of using a TVS with a breakdown voltage that is at the minimum operating temperature of a specific design that is slightly less than the maximum operating voltage of said design. A positive temperature coefficient of the breakdown voltage is a major prerequisite for such a use case.

Item 4 and Item 5 are the product of the maximum clamping voltage, V_{CL_max}, and the corresponding peak pulse current, I_{PP}, equals the maximum peak pulse power dissipation, P_{PP}, which D8 can handle at a given initial temperature and at a given current pulse waveform (see Equation 10).

$$P_{PP} = V_{CL\_max} \times I_{PP} = 69.7 \text{ V} \times 57 \text{ A} \approx 3973 \text{ W} \tag{10}$$

The 4-kW peak pulse power given in Item 5 is a good match to the 3973-W P_{PP} value calculated in Equation 10.

The 4-kW peak pulse power is important because it requires constant checking to confirm whether or not it has been exceeded in the case of the specific application.

This step requires knowing the application-specific peak pulse current I_{PP_appl}. The surge current calculated in Equation 1 as 23.8 A can be used instead as a good approximation (see Equation 11).

$$I_{PP\_appl\_max} \approx I_{Surge} \approx 23.8 \text{ A} \tag{11}$$

where:

- $I_{PP\_appl\_max}$ is the maximum peak pulse current in the specific application.

Based on the $I_{PP\_appl\_max}$, the maximum clamping voltage can be calculated, which occurs at the maximum junction temperature because of the positive temperature coefficient of the D8 breakdown voltage.

According to the data sheet for D8 [9], the maximum clamping voltage at other surge levels (other than what the *Electrical Characteristics* table shows) can be calculated using the formula in Equation 12:

$$V_{CL} = R_D \times I_{PP} + V_{BR\_max} \tag{12}$$

To approximate the maximum clamping voltage at the maximum temperature, the temperature coefficient, αT must also be factored in, as Equation 13 shows.

$$V_{CL\_max} \text{ at } 125°C \approx \left(I_{PP\_appl\_max} \times R_D + V_{BR\_max} \text{ at } 25°C\right) \times \left(1 + \alpha T \times \left(125°C - 25°C\right)\right)$$

$$V_{CL\_max} \text{ at } 125°C \approx \left(23.8 \text{ A} \times 0.504 \ \Omega + 41 \text{ V}\right) \times \left(1 + 10 \times \frac{10^{-4}}{°C} \times \left(125°C - 25°C\right)\right) \approx 58.3 \text{ V} \tag{13}$$

where

- V_{CL_max} is the maximum clamping voltage at the peak pulse current in the specific application
- $I_{PP\_appl\_max}$ is the maximum peak pulse current in the specific application
- R_D is the dynamic resistance at the specific current pulse waveform (8/20 μs)

- V_{BR_max} is the maximum breakdown voltage.

As the results from the preceding Equation 13 show, the worst-case voltage that all components connected in parallel to D8 must be capable of withstanding is in the range of 60 V.

With the calculated maximum clamping voltage from Equation 13, the maximum peak pulse power in the specific application can be calculated, as the following Equation 14 shows:

$$P_{PP\_appl\_max} = V_{CL\_max} \times I_{PP\_appl\_max} = 58.3\ V \times 23.8\ A \cong 1387\ W \quad (14)$$

where

- $P_{PP\_appl\_max}$ is the maximum peak pulse power in the specific application.

The calculation of 1387 W is much less than the 4 kW for which D8 is rated. The selected TVS is a good selection, even when factoring in a marginal power derating (less than –5%) for an initial junction temperature of +125°C, which the SM6T series data sheet provides [8].

1.5.2.4 D10—Voltage Clamping Between OUT and L–

D10 provides the basic clamping of incoming transients between the OUT and L– pins of the connector J4. The clamping that D10 provides is the first level of protection for the combined VOUT and IOUT pins of the DAC U3. The other components in the path between D10 and the VOUT and IOUT pins of U3 (steering diodes, resistors, and capacitor), provide further protection. The SM6T15A device from the SM6T family [8] has been chosen for this design with the specifications as listed in Table 4.

Table 4. SM6T15A Parameters—D10

ITEM	PARAMETERS	DESCRIPTION	CONDITIONS	VALUES
9	Type of diode	—	—	Unidirectional TVS
10	I_{RM} max at V_{RM}	Maximum leakage current at standoff voltage	T = 85°C; V_{RM} = 12.8 V	Max 1 µA
11	V_{BR} min, typ, max at I_R	Minimum, typical, and maximum breakdown voltage at reverse current	T = 25°C; I_R = 1 mA	Min 14.3 V, typ 15 V, max 15.8 V
12	V_{CL_max} at I_{PP} and 8/20 µs	Maximum clamping voltage at peak pulse current and 8/20-µs current pulse waveform	T = 25°C; I_{PP} = 147 A, 8/20 µs	Max 27.2 V
13	P_{PP_max} at 8/20 µs	Peak pulse power at 8/20-µs current pulse waveform	8/20 µs	Max 4 kW
14	R_D at 8/20 µs	Dynamic resistance at 8/20-µs current pulse waveform	T = 25°C, 8/20 µs	0.078 Ω
15	αT max	Maximum voltage temperature coefficient	T = 25°C	8.4×10^{-4}/°C
16	$R_{th(j-a)}$	Thermal resistance junction-to-ambient	Recommended pad layout	100°C/W

Item 9: A unidirectional TVS has been selected for this particular item. The purpose of D10 is to clamp transient overvoltages, but not to provide protection against overvoltage applied for longer pulse waveforms nor for continuously applied overvoltage. The positive transients on this pin must be clamped to a voltage level slightly larger than the nominal voltages expected on the VOUT and IOUT pins of U3. The negative transients on the J4 OUT-pin can be directly clamped to GND (which is identical to L–), because of the positive unipolar output range on the OUT-pin that is expected.

Item 10: The leakage current is very critical when the design has been configured as a current output. Any leakage current through D10 cannot be sensed by the internal current sense of the DAC U3, which therefore causes an error and a mismatch between the output current controlled by the DAC and the current sensed by the analog input of a connected PLC (see Figure 1). Operation at a high temperature is especially critical because this generally causes increased leakage. The SM6T family of TVS diodes specifies the leakage current even for temperatures of 85°C, which simplifies the selection process.

Equation 15 calculates the maximum nominal voltage across D10 when the design has been configured as a current output:

$$V_{D10\_IOUT\_max} \le R_{Load\_max} \times I_{OUT\_max} = 320\ \Omega \times 24\ mA = 7.68\ V \quad (15)$$

where:

- $V_{D10\_IOUT\_max}$ is the maximum voltage across D10 when the design is configured as current output
- R_{Load_max} is the maximum load resistance
- I_{OUT_max} is the maximum output current (equals the loop current)

The maximum nominal voltage across D10 with the design configured as a voltage output equals the maximum value of the overrange voltage range, which is 11 V.

With a 12.8-V standoff voltage at 1-uA leakage and at 85°C, enough margin exists to stay in normal operation below the 1-uA leakage current at even higher temperatures than 85°C. This relationship exists because the maximum nominal voltage (7.68 V when configured as current output or 11 V when configured as voltage output) applied to D10 is less than its 12.8-V standoff voltage.

Item 11: The minimum breakdown voltage of 14.3 V is larger than the worst-case maximum voltage that the DAC U3 is capable of providing when the design has been configured as a current output and when operating without any load. This maximum voltage equals the AVDD, which is the 13.1-V output voltage generated by the LDO U1.

The worst-case operating condition is to operate at the minimum temperature (–40°C), at which the minimum breakdown voltage of D10 can decrease according to the following calculation in Equation 16:

$$V_{BR\_min}\ \text{at}\ -40°C = V_{BR\_min}\ \text{at}\ 25°C \times \left(1 + \alpha T \times (-40°C - 25°C)\right) = 14.3\ V \times \left(1 + 8.4 \times \frac{10^{-4}}{°C} \times (-40°C - 25°C)\right)$$

$$V_{BR\_min}\ \text{at}\ -40°C = 14.3\ V \times \left(1 + \frac{-0.0546°C}{°C}\right) = 13.52\ V \quad (16)$$

However, this value is still larger than the 13.1-V AVDD-voltage and therefore ensures that the reverse current through D10 stays below the 1-mA level.

Item 12: Knowing the maximum clamping voltage at the surge current is especially important. The worst-case maximum V_{CL} occurs at the maximum temperature, which the following Equation 17 calculates:

$$V_{CL\_max}\ \text{at}\ 125°C \cong \left(IPP\_appl\_max \times R_D + VBR\_max\ \text{at}\ 25°C\right) \times \left(1 + \alpha T \times (125°C - 25°C)\right)$$

$$= \left(23.8\ A \times 0.078\ \Omega + 15.8\ V\right) \times \left(1 + 8.4 \times \frac{10^{-4}}{°C} \times (125°C - 25°C)\right) = 19.14\ V \quad (17)$$

Item 13: After calculating the maximum clamping voltage, the maximum peak pulse power in the specific application can be calculated (see Equation 18):

$$P_{PP\_appl\_max} = V_{CL\_max} \times I_{PP\_appl\_max} = 19.14\ V \times 23.8\ A \approx 455.5\ W \quad (18)$$

This 455-W power dissipation is much less than the maximum 4-kW peak pulse power for which D10 is specified. A less powerful and even smaller TVS may seem to be a reasonable choice at first; however, remember that a less powerful and smaller TVS yields a larger dynamic resistance, which leads to a higher clamping voltage. Such a higher clamping voltage requires an increased resistance in the current steering network between the D10 diode and VOUT_IOUT signal of the DAC U3. The higher resistance leads to higher voltage drops, which then requires a larger AVDD to compensate for the larger drop. The design goal is to enable operation of the design with a supply voltage (on L+) as low as possible (15 V is the specification from Table 1 for the operating supply voltage). This minimum operating voltage must be larger than 15 V if the AVDD voltage requires an increase.

1.5.2.5 D9—Voltage Clamping Between OUT and L+

The D9 diode provides the basic clamping of incoming transients between the OUT and L+ pins of the connector J4. The SM6T42CAY device from the SM6TY family[9] has been chosen for this design with the specifications as listed in Table 5.

Table 5. SM6T42CAY Parameters—D9

ITEM	PARAMETERS	DESCRIPTION	CONDITIONS	VALUES
17	Type of diode	—	—	Bidirectional TVS
18	I_{RM} max at V_{RM}	Maximum leakage current at standoff voltage	T = 85°C; V_{RM} = 36 V	Max 1 µA
19	V_{BR} min, typ, max at I_R	Minimum, typical, and maximum breakdown voltage at reverse current	T = 25°C; I_R = 1 mA	Min 40 V, typ 42.1 V, max 44.2 V
20	V_{CL} max at I_{PP} and 8/20 µs	Maximum clamping voltage at peak pulse current and 8/20 µs current pulse waveform	T = 25°C; I_{PP} = 52 A, 8/20 µs	Max 76 V
21	P_{PP} max at 8/20 µs	Peak pulse power at 8/20-µs current pulse waveform	8/20 µs	Max 4 kW
22	R_D at 8/20µs	Dynamic resistance at 8/20-µs current pulse waveform	T = 25°C, 8/20 µs	0.611 Ω
23	αT max	Maximum voltage temperature coefficient	T = 25°C	10×10^{-4}/°C

Item 17: Item 17 requires a bidirectional TVS. The series connection of D9 and D10 connects in parallel to the D8 TVS. A unipolar D9, with the D9 anode connected to the D10 cathode, results in a unipolar clamping of D8, too. However, as Item 1 details, a bipolar characteristic is required for D8. Using a unipolar D9, but with the D9 cathode connected to the D10 cathode, also does not work. In such a case, the OUT of J4 is always pulled up to L+ by D9.

Item 18: The leakage current of D9 is very critical, when the design has been configured as a current output. Any leakage current through D9 cannot be sensed by the internal current sense of the DAC U3, which therefore causes an error and a mismatch between the output current controlled by the DAC and the current sensed by the analog input of a connected PLC (see Figure 1). Operation at a high temperature is especially critical because this generally causes increased leakage currents. The SM6TY family of TVS diodes provides the leakage current even for temperatures of 85°C, which simplifies the selection process.

Equation 19 calculates the maximum nominal voltage across D9 when the design has been configured as a current output:

$$V_{D9\_IOUT\_max} \le V_{L+\_max} - \left(R_{Load\_min} \times I_{OUT\_min}\right) = 35\ V - \left(0\ \Omega \times 0\ mA\right) = 35\ V \quad (19)$$

where:

- $V_{D9\_IOUT\_max}$ is the maximum voltage across D9 when the design has been configured as a current output
- R_{Load_min} is the minimum load resistance; Table 1 does not provide any minimum limit, even an ammeter with very low internal shunt can be used; therefore, assume 0 Ω
- I_{OUT_min} is the minimum output current (equals the loop current), 0 mA in case of a 0- to 24-mA output.

The standoff voltage of the selected TVS must be ≥ 35 V, as calculated in Equation 19, to ensure that the leakage current is small enough to ignore. In comparison to the SM6T39CA with a 33.3-V standoff voltage, which was selected for D8, D9 requires a different TVS with a standoff voltage that is greater or equal to the specified 35 V. The SM6T42CAY has been selected for this design. The SM6T42CAY is a TVS from a family of devices very similar to the SM6T but it offers a verison with a standoff voltage of 36 V, which is not available in the SM6T family.

Item 19: Equation 20 calculates the minimum breakdown voltage at –40°C. The calculated 37.4 V is greater than the maximum 35-V operating voltage of the design; therefore, the selected diode is a good fit.

$$V_{BR\_min} \text{ at } -40\,^{\circ}C = V_{BR\_min} \text{ at } 25\,^{\circ}C \times \left(1 + \alpha T \times \left(-40\,^{\circ}C - 25\,^{\circ}C\right)\right) = 40 \text{ V} \times \left(1 + 10 \times \frac{10^{-4}}{^{\circ}C} \times \left(-40\,^{\circ}C - 25\,^{\circ}C\right)\right)$$

$$V_{BR\_min} \text{ at } -40\,^{\circ}C = 40 \text{ V} \times \left(1 + \frac{-0.065\,^{\circ}C}{^{\circ}C}\right) = 37.4 \text{ V} \tag{20}$$

Item 20: Knowing the maximum clamping voltage at the surge current is especially important. The worst-case maximum V_{CL} occurs at the maximum temperature, which the following equations calculate:

$$V_{CL\_max} \text{ at } 125\,^{\circ}C \approx \left(I_{PP\_appl\_max} \times V_{BR\_max} \text{ at } 25\,^{\circ}C\right) \times \left(1 + \alpha T \times \left(125\,^{\circ}C - 25\,^{\circ}C\right)\right)$$

$$V_{CL\_max} \text{ at } 125\,^{\circ}C \approx \left(23.8 \text{ A} \times 0.611\ \Omega + 44.2 \text{ V}\right) \times \left(1 + 10 \times \frac{10^{-4}}{^{\circ}C} \times \left(125\,^{\circ}C - 25\,^{\circ}C\right)\right) \approx 64.62 \text{ V} \tag{21}$$

Item 21: After calculating the maximum clamping voltage, the maximum peak pulse power in the specific application can be calculated (see Equation 22):

$$P_{PP\_appl\_max} = V_{CL\_max} \times I_{PP\_appl\_max} = 64.62 \text{ V} \times 23.8 \text{ A} \cong 1538 \text{ W} \tag{22}$$

This 1538 W is much less than the maximum 4-kW peak pulse power for which D10 is specified. The selected TVS is a good fit, even when factoring in the marginal power derating (less than – 5%) for an initial junction temperature of 125°C, as provided in the SM6TY data sheet [10].

1.5.2.6 D3—Voltage Clamping of AVDD

D3 provides the basic clamping of the AVDD voltage rail to prevent the AVDD rail from rising in an uncontrollable manner during positive overvoltage transients on the OUT-pin of J4. Under such a condition, D10 clamps the OUT-pin of J4 to a maximum of about 20 V, as the preceding Equation 17 shows. In addition, a current steers through D6 and D7 to the AVDD-rail because the 20-V V_{CL} across D10 is larger than the nominal 13.1-V AVDD. This current charges the output capacitors C2 and C3 of the LDO U1. A SMM4F13A out of the SMM4F family [10] was selected for its capability to clamp the AVDD-rail, which avoids violating the 18.5-V maximum output voltage range of the LDO. Table 6 summarizes the important specifications of D3.

Table 6. SMM4F13A Parameters—D3

ITEM	PARAMETER	DESCRIPTION	CONDITIONS	VALUES
24	Type of diode	—	—	Undirectional TVS
25	I_{RM} max at V_{RM}	Maximum leakage current at standoff voltage	T = 85°C; V_{RM} = 13 V	Max 1 µA
26	V_{BR} min, typ, and max at I_R	Minimum, typical, and maximum breakdown voltage at reverse current	T = 25°C; I_R = 1 mA	Min 14.3 V, typ 15 V, max 15.8 V
27	V_{CL} max at I_{PP} and 8/20 µs	Maximum clamping voltage at peak pulse current and 8/20-µs current pulse waveform	T = 25°C; I_{PP} = 85 A, 8/20 µs	Max 27.2 V
28	P_{PP} max at 8/20 µs	Peak pulse power at 8/20-µs current pulse waveform	8/20 µs	Max 2.4 kW
29	R_D at 8/20 µs	Dynamic resistance at 8/20-µs current pulse waveform	T = 25°C, 8/20 µs	0.13 Ω
30	αT max	Maximum voltage temperature coefficient	T = 25°C	8.4 x 10^{-4}/°C

Item 24: A unidirectional TVS is sufficient.

Item 25 and Item 26: No significant leakage current of D3 occurs, although the standoff voltage (13 V) of D3 is slightly less than the max value of the AVDD-rail (13.41 V). Even the maximum reverse current is expected to be less than 1 mA. This value is because the maximum AVDD-rail voltage is even less than the 13.52 V calculated as the worst-case minimum breakdown voltage (at 1-mA reverse current and at –40°C), as Equation 23 shows. The selected diode is therefore a good fit.

$$V_{BR\_min} \text{ at } -40°C = V_{BR\_min} \text{ at } 25°C \times \left(1 + \alpha T \times (-40°C - 25°C)\right) = 14.3 \text{ V} \times \left(1 + 8.4 \times \frac{10^{-4}}{°C} \times (-40°C - 25°C)\right)$$

$$V_{BR\_min} \text{ at } -40°C = 14.3 \text{ V} \times \left(1 + \frac{-0.0546°C}{°C}\right) = 13.52 \text{ V} \tag{23}$$

Item 27: Knowing the maximum clamping voltage at the surge current is especially important. This maximum clamping voltage must be less than the 18.5-V maximum output voltage range of the LDO U1.Obtaining the maximum clamping voltage requires knowing the application-specific peak pulse current, I_{PP_appl} (see Equation 24).

$$I_{PP\_appl\_max} \cong I_{D7\_AVDD} + I_{D6\_AVDD} \leq 1 \text{ A} \tag{24}$$

where:

- I_{D7_AVDD} is the peak pulse current through D7 steered to the AVDD-rail
- I_{D6_AVDD} is the peak pulse current through D6 steered to the AVDD-rail

Both currents through the steering diodes D6 and D7 are expected to be less than 300 mA to 400 mA. In theory, the current that flows through the ESD protection diode of the DAC U3 must be added. This current is expected to be less than 10 mA. A maximum of 1 A can be used as an reasonable worst-case approximation for $I_{PP\_appl\_max}$.

With this value, the worst-case maximum V_{CL} (at the maximum temperature) can be calculated using the following Equation 25:

$$V_{CL\_max} \text{ at } 125°C \approx \left(I_{PP\_appl\_max} \times R_D + V_{BR\_max} \text{ at } 25°C\right) \times \left(1\_\alpha T \times (125°C - 25°C)\right)$$

$$V_{CL\_max} \text{ at } 125°C \approx \left(1 \text{ A} \times 0.13\ \Omega + 15.8 \text{ V}\right) \times \left(1 + 8.4 \times \frac{10^{-4}}{°C} \times (+125°C - 25°C)\right) \approx 17.27 \text{ V} \tag{25}$$

Item 28: With the before calculated maximum clamping voltage, the maximum peak pulse power in the specific application can now be calculated, as Equation 26 shows:

$$P_{PP\_appl\_max} = V_{CL\_max} \times I_{PP\_appl\_max} = 17.27 \text{ V} \times 1 \text{ A} \cong 17.3 \text{ W} \tag{26}$$

This 17.3-W power dissipation is much less than the maximum 2.4-kW peak pulse power for which D3 is specified. A less powerful and even smaller TVS may appear to be a reasonable choice at a first glance. However, be mindful that a less powerful and smaller TVS has a larger dynamic resistance, which leads to a higher clamping voltage. Such a higher clamping voltage may violate the LDOs U1 maximum output voltage range.

1.5.2.7 Current Steering Network Between D10 and VOUT_IOUT of DAC U3

The D10 diode has been selected in such a way as to not influence the voltage or current output accuracy of the design, even during operation over the full-temperature range. As Section 1.5.2.4 shows, an adequate margin has been factored in to this range. This factoring in was achieved by choosing a TVS with a maximum high temperature leakage current of less than 1 μA at the 12.8-V standoff voltage of that TVS (see Item 10 in Section 1.5.2.4). Alternatively, it is important to note that the maximum high temperature clamping voltage of D10 is almost 20 V (see Equation 17). This large 20-V under surge condition across D10 violates the maximum voltage rating for the VOUT and IOUT pins of the DAC U3.

Therefore, an additional network between D10 and the VOUT_IOUT signal of the DAC is required, as Figure 17 shows.

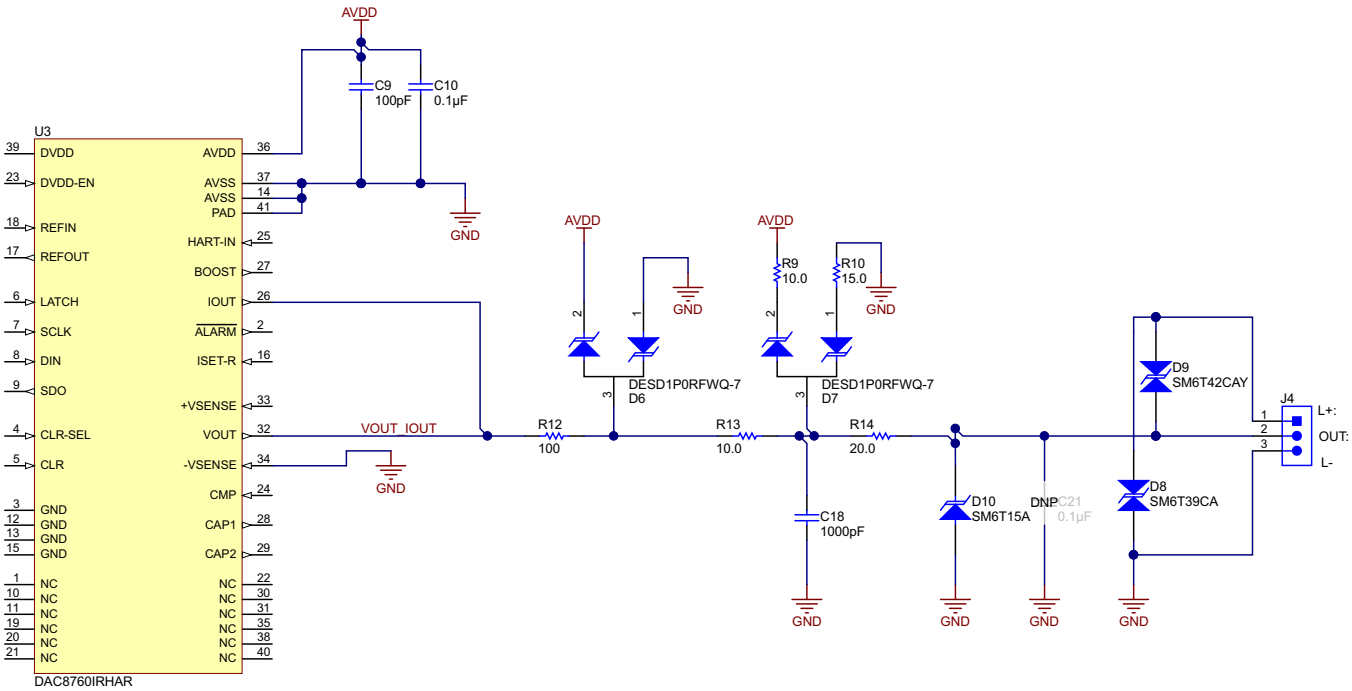


Figure 17. Current Steering Network Between D10 and VOUT_IOUT Signal of DAC U3

The design goal is to keep the VOUT and the IOUT pins at a level within GND – 300 mV and AVDD + 300 mV so as not to damage the internal protection circuitry of the DAC, nor to degrade the DAC performance. In addition, the current through the internal protection circuitry of the DAC should be limited to less than 10 mA.

To achieve this goal, a network has been used consisting of a cascade of two dual-current steering diodes (D6 and D7), three current-limiting resistors (R12, R13, and R14), two balancing resistors (R9 and R10), and one filter capacitor (C18). This network reduces and balances the current from the large surge current (±23.8 A) through the clamping diode D10 down to a much lower current (less than 10 mA) through the internal protection circuit of the DAC.

The DESD1P0RFWQ-7 diodes have been selected as steering diodes [11]. These diodes steer any positive surge to AVDD and any negative surge to GND. The diodes are rated for a 15-A peak pulse current (8/20 μs) and show typical reverse currents of roughly 320 nA at 75°C and 5 μA at 125°C, both at a 20-V reverse voltage.

Simulations with TINA-TI have been conducted to show the performance, peak currents, and peak voltages. A DC analysis has also been performed. The results as provided in the following Figure 18 and Figure 19 show that the current through the internal protection circuitry (D_U3) can be kept below 10 mA. The simulation has been performed for positive surges only. The user can expect the negative surge to lead to even lower currents through the internal protection of the DAC. This result is because of the fact that negative transients are to be clamped by D10 to its forward voltages, between –1.5 V to –2 V, which is much less severe than the almost 20 V calculated in Equation 17 for a positive surge at the same absolute application–specific, peak current level of roughly 23.8 A.

From the dual-steering diodes D6 and D7, only one diode per D6 and D7 is visible, which is the diode steering the current to AVDD in the case of a positive surge. D6 and D7 were inserted as a simplified diode (based on an ideal diode) as well as a modified model, which was based on a similar diode. SW1 and SW2 serve as selection switches to run the simulation either with the modified model (switch in position 1) or with the simplified diode (position 2).

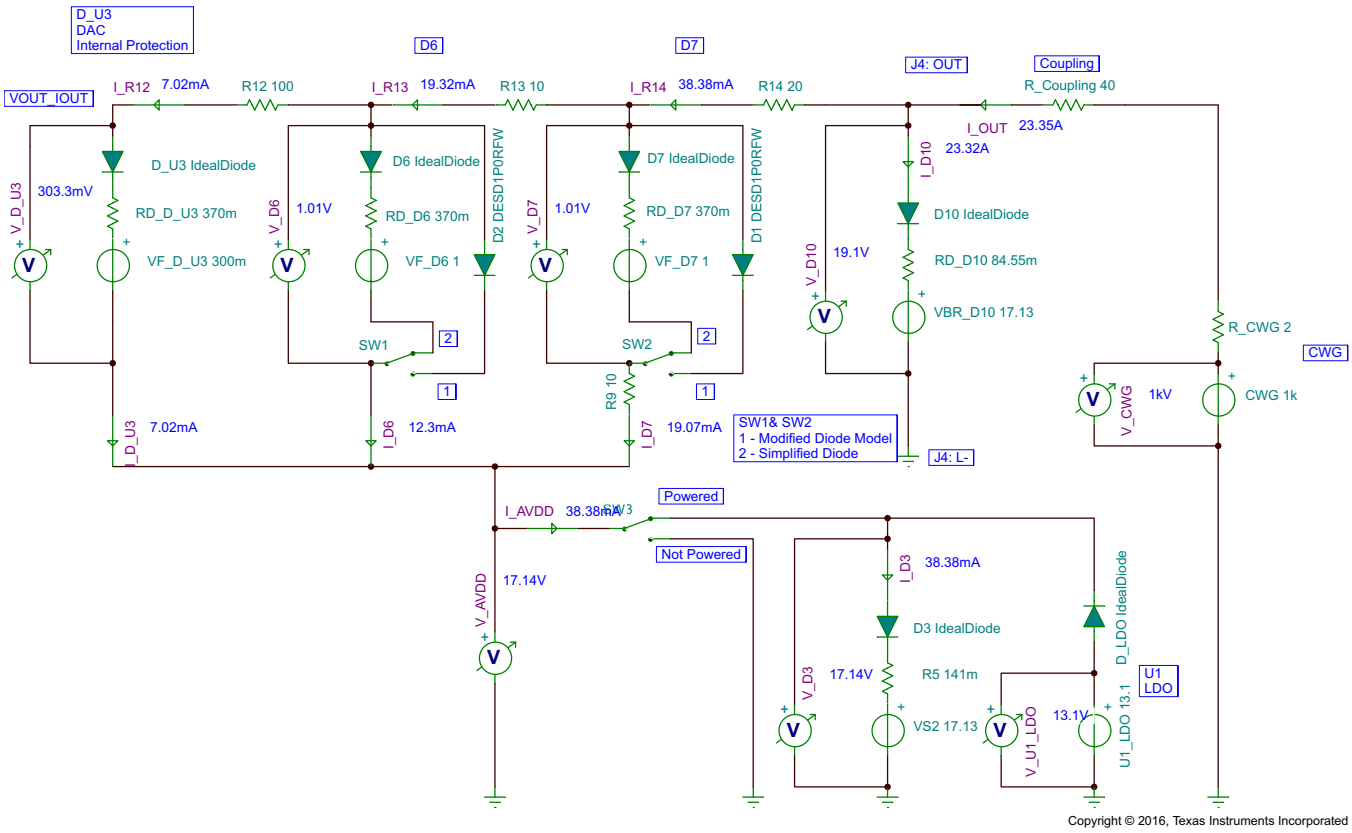


Figure 18. TINA-TI™ Simulation of Current Steering Network Using Simplified Diodes Models—Circuitry Powered

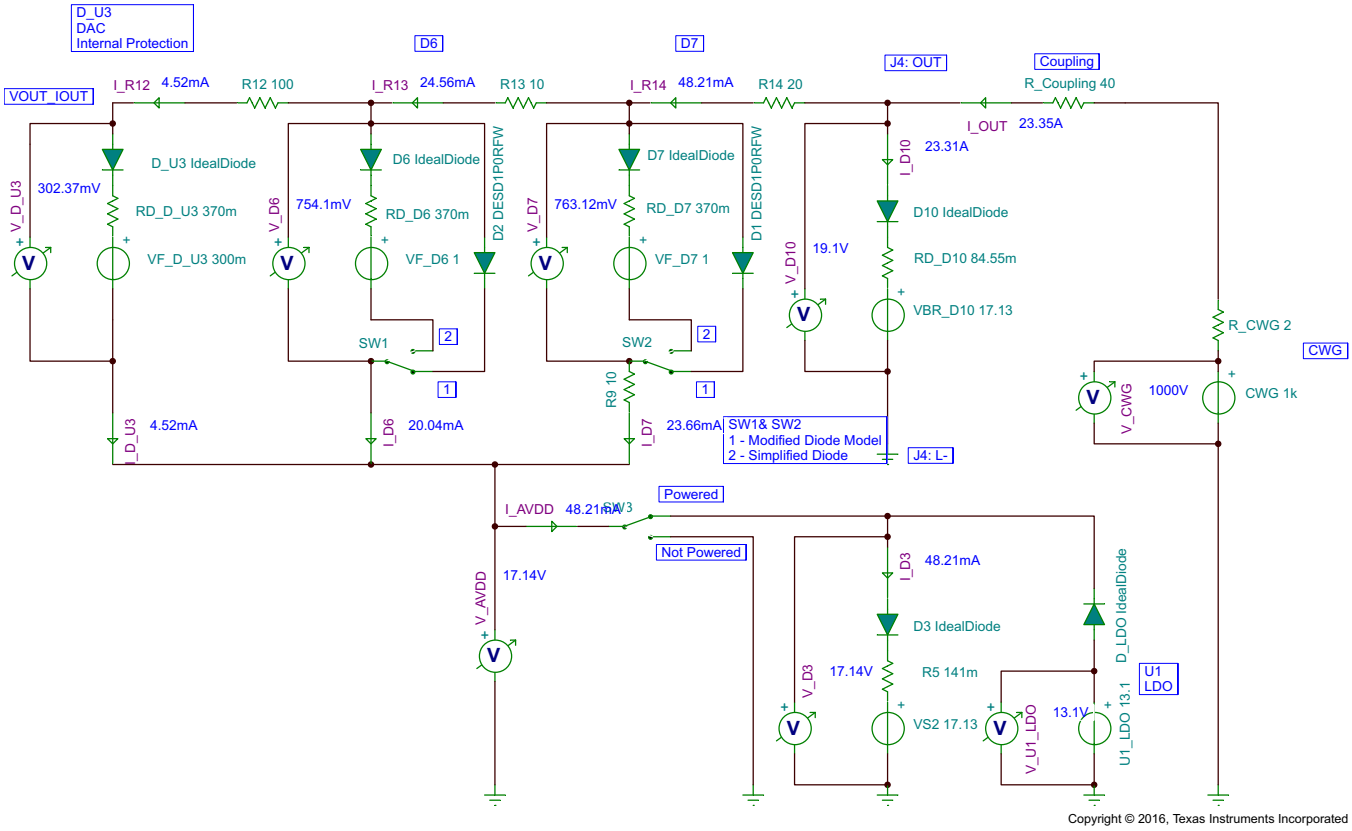


Figure 19. TINA-TI™ Simulation of Current Steering Network Using Modified Diode Models—Circuitry Powered

Both the preceding Figure 18 and Figure 19 are based on the condition that the design has already been powered and that the AVDD is at its nominal voltage of 13.1 V.

Aside from this condition, a much more severe condition is possible when the design has not yet been powered, and all the capacitors are therefore discharged. Any positive surge that hits the design under such a condition leads to the same clamping voltage on D10, but the current through the steering network is not steered to the 13.1-V level on AVDD, but instead to the discharged output capacitors C2 and C3 of the LDO U1.

Figure 20 and Figure 21 show the simulation circuit applicable for the non-powered case and for a positive surge. The non-powered condition of the design is represented by a V_{AVDD} of 0 V which is achieved by switching S3 (in the lower half of the figures) to GND (Not-Powered position of S3). As expected, the current stress in the current-steering network heavily increases under this condition. This increase not only stresses the steering diodes, but also increases the power dissipation in the resistors. R14, for example, must be able to withstand a peak pulse power dissipation of 10.4 W. The selection of the resistor types and sizes accounts for the peak pulse power for any of the resistors in the current-steering network.

The continuous power dissipation must also be considered, which determines the resistor type and size selection. R12 has a relatively high continuous power dissipation –worst-case under a short-circuit condition, where the typical current limit of 30 mA for the output current may increase to more extreme levels. An assumed 50-mA continuous current through R12, for example, results in 250 mW of continuous power dissipation. Therefore, pulse-proof high-power resistors out of the CRCW-HP e3 family[12] in a 1206 size have been selected for the R14 and R12 resistors to address operation at elevated temperatures of 85°C or even at 125°C.

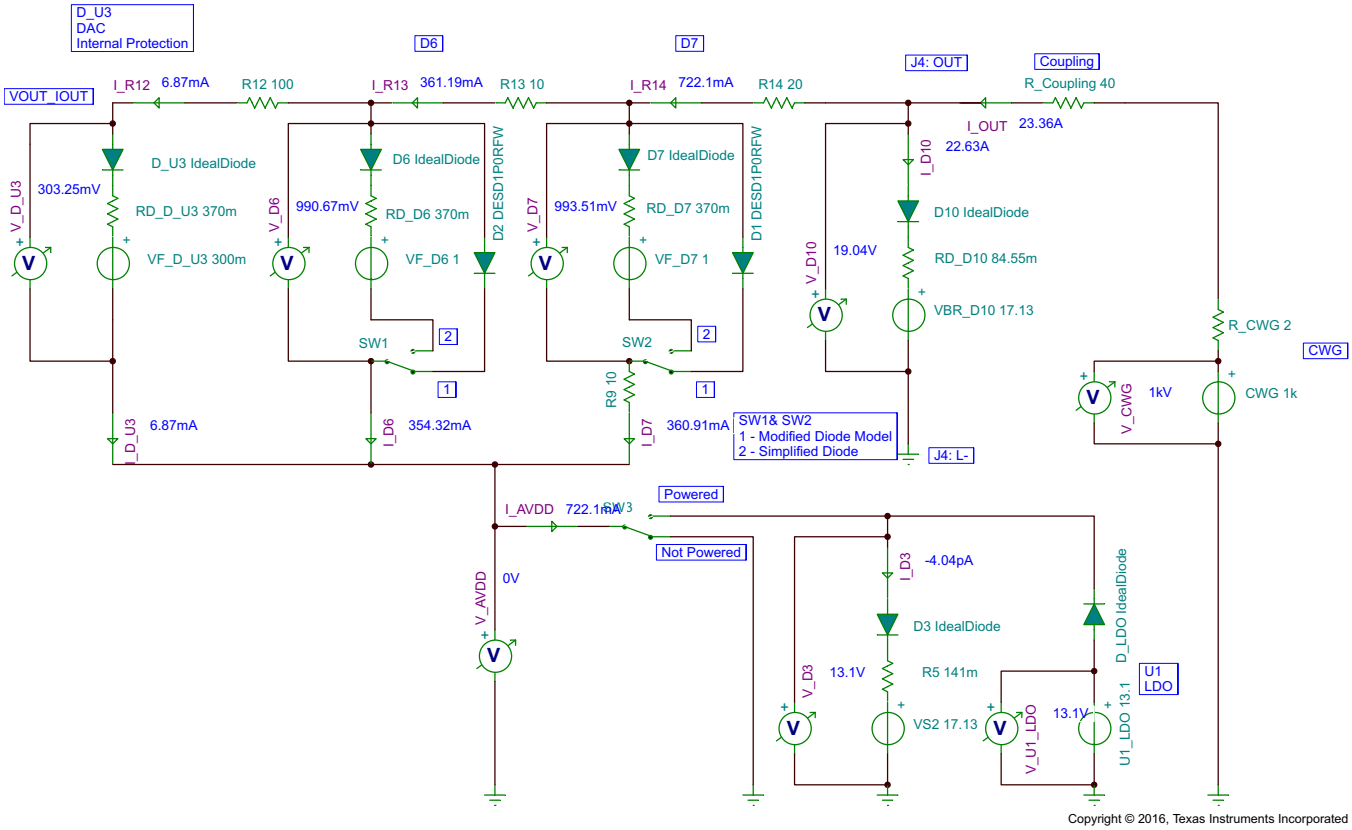


Figure 20. TINA-TI™ Simulation of Current Steering Network Using Modified Diode Models—Circuitry Not Powered

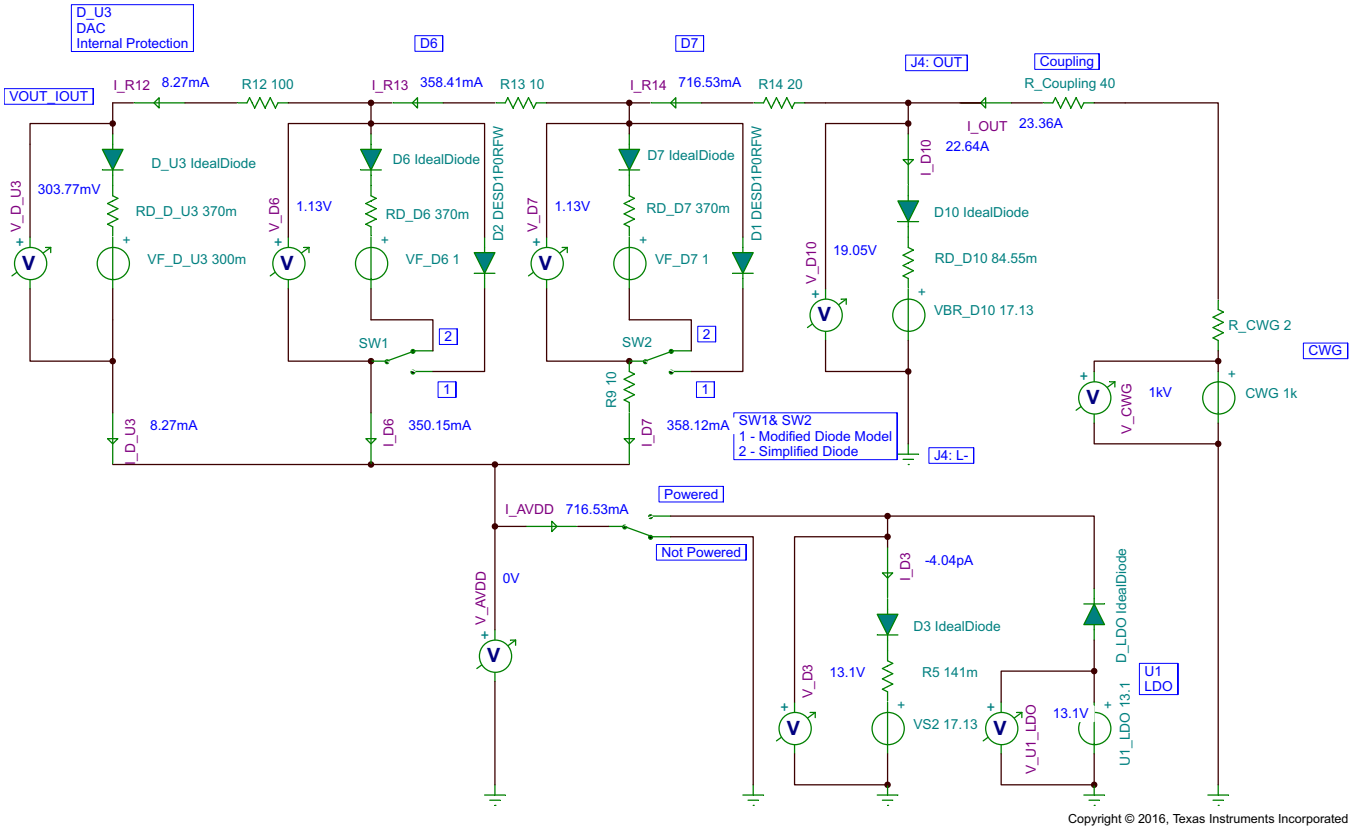


Figure 21. TINA-TI™ Simulation of Current Steering Network Using Simplified Diodes Models—Circuitry Not Powered

1.5.2.8 Protection of Buffer Amplifier U2

The OPA170 op amp used as the U2 buffer U2 is specified with very low bias currents of a maximum 15 pA. Connecting the non-inverting input of U2 through the 10-kΩ resistor R8 to the TVS D10 can be considered as a sufficient protective implement without influencing the accuracy or performance of the design (see Figure 22).

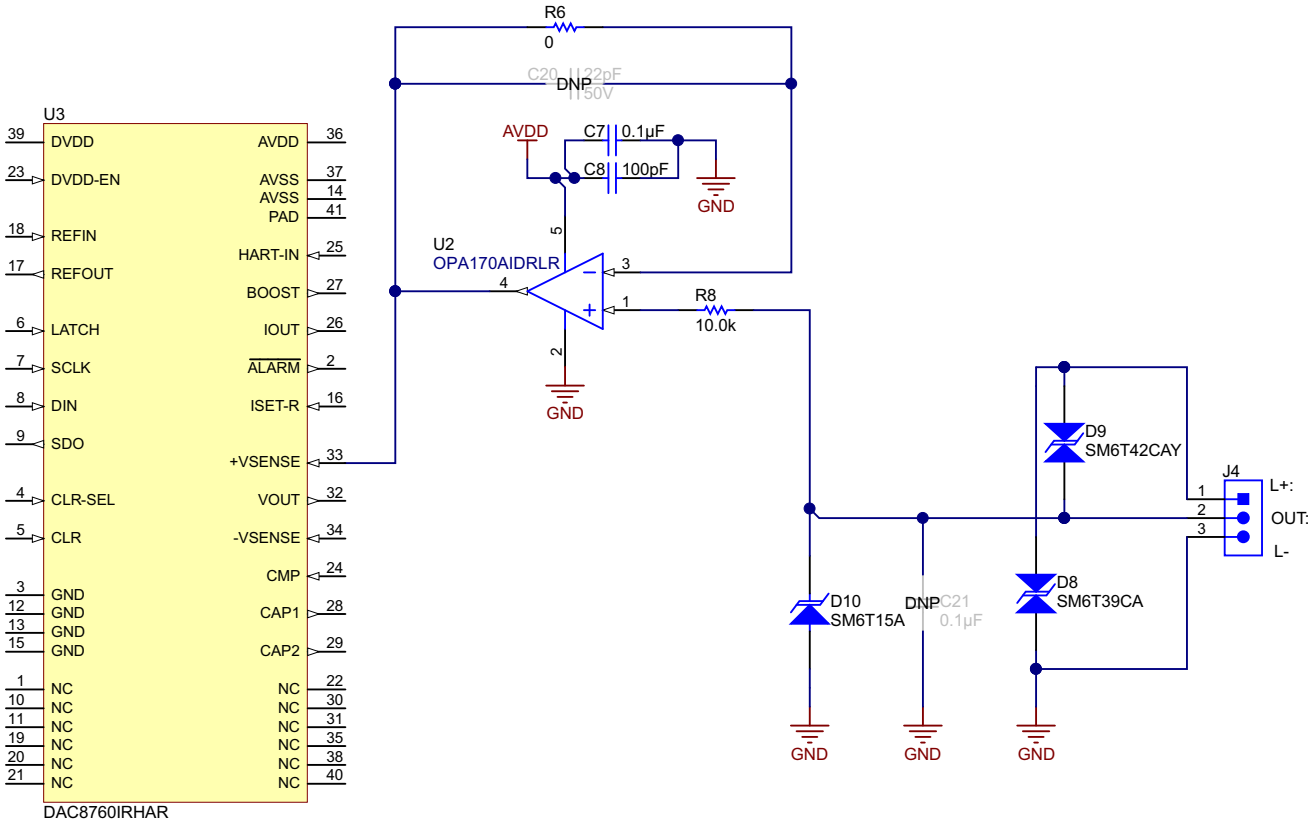


Figure 22. Simple Resistor (R8) Protects U2 Op Amp

The resistor R8 limits the current which flows when the clamping voltage on D10 peaks at almost 20 V (positive surge) or at –1.5 V to –2 V (negative surge). A positive surge under non-powered conditions is the worst-case condition and almost leads to 20 V across resistor R8 and a resulting current of 2 mA through the 10-kΩ resistor R8, as well as through the internal input protection diode of the U2 op amp. The protection diode of U2 has a current rating of ±10 mA, which provides enough margin as compared to the 2-mA current flow.

1.5.2.9 Protection of LDO U1

Several protection concerns exist for the LDO U1, as Figure 23 shows.

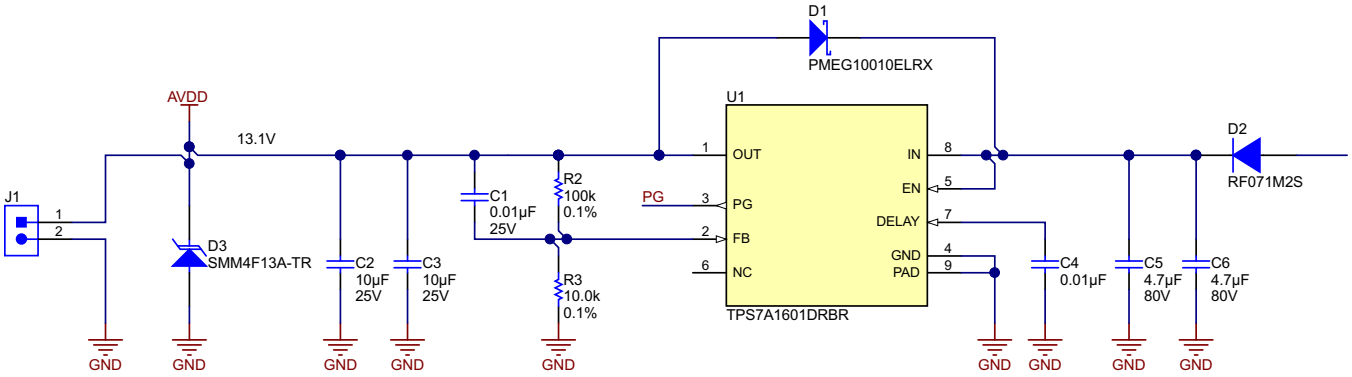


Figure 23. Protection of LDO U1—Diodes in Schematic Provide Protection Against Reverse Input Voltage, Output Overvoltage, and Reverse Output Current

Input voltage: The maximum recommended input voltage is 60 V and the absolute maximum rating is –0.3 V to 62 V. Therefore, the input requires protection against reverse polarity. For this reason, the diode D2 serves as the reverse polarity protection diode. The diode has a low reverse current (typical 120 nA at 35 V and 125°C) that prevents a negative voltage buildup on the input of the LDO under a reverse input condition, as this may happen when alternatively using Schottky diodes at high temperatures.

The reverse voltage of D2 is 200 V, enabling a robust blocking when the input capacitors (C5 and C6) have been fully charged to the maximum voltage (almost 35 V) while a negative surge with an approximate –60-V clamping voltage on D8 occurs. Another advantage of using the reverse polarity protection diodes that the input capacitors C5 and C6 keep their charge (and voltage), even during the short period of a negative surge, which helps to avoid a design reset and the following time-consuming restart.

Output voltage: The maximum recommended output voltage has been provided as 18.5 V and must be kept below this value to avoid any degradation of the performance of the LDO. The protection of the output is given by the unidirectional TVS D3, as the respective Section 1.5.2.6 outlines.

Reverse output current: Reverse current from the output to the input of the LDO may build up in cases when the design has not been powered or has been powered with the lowest possible operating voltage of 15 V. In case of positive surges on the OUT pin of J4, the D10 limits the surge voltage to almost 20 V and charges up the output capacitors C2 and C3 of the LDO. D3 clamps the voltage on the LDOs output capacitors at approximately 18 V. The rising voltage on the LDOs output capacitors also drives a charging current through the parasitic body diode of the LDOs internal FET to charge the input capacitors of the LDO. This body diode has not been designed to withstand currents up to 1 A. Therefore, an external Schottky diode is used in parallel to the internal body diode for bypassing the weak internal body diode. The used PMEG10010ELR Schottky diode has a 1.4-A forward-current rating and a typical 710 mV of forward voltage at 25°C, which safely avoids any conduction of the LDOs internal body diode. The typical reverse current at 35 V and at 125°C is 30 µA, which is low enough to ensure that the output of the LDO always stays in regulation.

1.5.3 16-Bit DAC and Buffer

The general design of the DAC U3 circuitry follows the recommendation given in the data sheet [2].

The DAC is powered unipolar from the positive 13.1-V AVDD only. The intention of this approach is to maintain the simple design. A negative supply voltage does not exist for the DAC in this design; therefore, the AVSS-pins and the thermal pad of U3 are connected to GND.

The DVDD-EN pin of the DAC is left floating to enable the internal 4.6-V linear regulator of U3. The 4.6-V output voltage of this regulator is output on the DAC DVDD pin, which powers the VCC2 rail of the digital isolator U4 through R7, as Section 1.5.1 describes.

The $\overline{\text{ALARM}}$ pin of the DAC is pulled-up via through the super-red LED D4 and R4 in addition to the DVDD rail in addition. The total current draw out of the DVDD rail is expected to be less than 10 mA.

The design uses the internal 5-V reference of the DAC. The DAC REFIN and REFOUT pins are therefore interconnected and bypassed by C13 to GND.

R11, an external 15-kΩ precision resistor is connected to the ISET-R pin of U3. R11 can be enabled by software configuration to be used alternatively to the internal RSET resistor of the DAC.

To combine the voltage output and the current output of the design into a single common output, the VOUT and the IOUT pins of U3 have been interconnected. An additional op amp configured as a buffer amplifier is used to sense the voltage on the OUT pin of J4, which is the single common output pin of this TIDA-00559 design. By using this remote sensing on the interface connector J4, all the errors caused by the voltage drops across the current-limiting resistors (R12, R13, and R14) cancel out. The sensed voltage is buffered by the op amp U2 and fed into the +VSENSE pin of the DAC, which appears with a 60- or 70-kΩ input resistance. View the *Combined Voltage and Current Output With the DACx760* application report for more details [4].

1.5.4 13.1-V LDO

Section 1.5.2.9 already describes the protection circuitry for the LDO U1. Programming the output voltage of the LDO and selecting a fitting LDO are the other important design criteria in addition to the protection. The TPS7A1601 device was carefully selected for U1 and its output voltage was carefully determined to match the required criteria.

Precision resistors with a 0.1% tolerance have been used to match the criteria, as Table 7 shows.

Table 7. Criteria Set for U1 Output Voltage Programming and LDO Selection

PARAMETER	VALUE	COMMENT
U1: $V_{IN\_abs\_max}$	62 V	Data sheet U1 [3]
U1: $V_{IN\_max\_recommended}$	60 V	Data sheet U1 [3]
D8: V_{CL_max} at +125°C and $I_{PP\_appl\_max}$	58.3 V	Section 1.5.2.3
D8 V_{BR_min} at -40°C	34.69 V	Acceptable as Section 1.5.2.3 shows
TIDA-00559 maximum operating voltage	35 V	Section 1.2
U1: $V_{OUT\_max\_recommended}$	18.5 V	Data sheet U1 [3]
D3: V_{CL_max} at +125°C and $I_{PP\_appl\_max}$	17.27 V	Section 1.5.2.6
TIDA-00559: Minimum operating voltage	15 V	Section 1.2
TIDA-00559: $U1_{Min\_VIN}$ at I_{IN} = 30 mA	14.3 V	VF of D2 assumed 0.7 V
D3 V_{BR_min} at -40°C	13.52 V	Section 1.5.2.6
TIDA-00559: $AVDD_{\_max}$ at 0.1% Tol_{R2}, Tol_{R3}, and 2%Tol_{U1}	13.41 V	Data sheet U1 [3]
TIDA-00559: $AVDD_{\_typ}$	13.12 V	Data sheet U1 [3]
TIDA-00559: $AVDD_{\_min}$ at 0.1% Tol_{R2}, Tol_{R3}, and 2%Tol_{U1}	12.84 V	Data sheet U1 [3]
U1: Minimum headroom (V_{IN} – V_{OUT})	0.87 V	—
TIDA-00559: $U3_{\_minV\_IOUT}$: at $V_{Compliance\_max}$ = 2 V U3 in current output mode	10.84 V	Data sheet U3 [2]
TIDA-00559: $J4_{V\_OUT}$: at IOUT = 24 mA U3 in current output mode	7.72 V	Due to (24 mA × 130 Ω) voltage drop across R12 + R13 + R14
TIDA-00559: Maximum R_{Load} U3 in current output mode	320 Ω	7.72 V / 24 mA = 321.7 Ω
TIDA-00559: $J4_{max\_V\_OUT}$: at VOUT = 11 V U3 in voltage output mode	11 V	Data sheet U3 [2]
TIDA-00559: $U3_{max\_V\_VOUT}$: at 11-V $J4_{max\_V\_OUT}$ and 1-kΩ R_{Load} U3 in voltage output mode	12.43 V	Due to (11 mA × 130 Ω) voltage drop across R12 + R13 + R14
TIDA-00559: Desired AVDD at 11-V $J_{4max\_V\_OUT}$ and 1-kΩ R_{Load} U3 in voltage output mode	12.93 V	Due to desired 0.5-V AVDD headroom voltage in voltage output mode, see data sheet U3 [2]

The 12.93-V AVDD required to power the DAC when the DAC is configured as a voltage output with 10% overrange and loaded with 1 kΩ is 90 mV larger than the worst-case minimum 12.84-V AVDD generated by the LDO U1 (see Table 7). For this situation, TI may recommend to slightly increase the LDO output voltage for a real design by modifying the output voltage divider (R2 and R3) of U1.

The AVDD rail generated by the U1 LDO is supervised by the internal power good function of the LDO. The open-drain output of the U1 internal power good comparator is pulled-up to AVDD by R5. A green LED (D5) is used as an indicator, which is ON when the voltage on the LDO FB pin is larger than the threshold V_{IT} of U1s internal power good comparator. Having D5 connected in parallel to the LDO PG pin (to GND) ensures that the LDOs 5.5-V absolute maximum rating for the voltage on the PG-pin is not violated.

2 Getting Started Hardware and Firmware

2.1 Hardware

2.1.1 Board Description

Figure 24 shows the board description for the TIDA-00559.

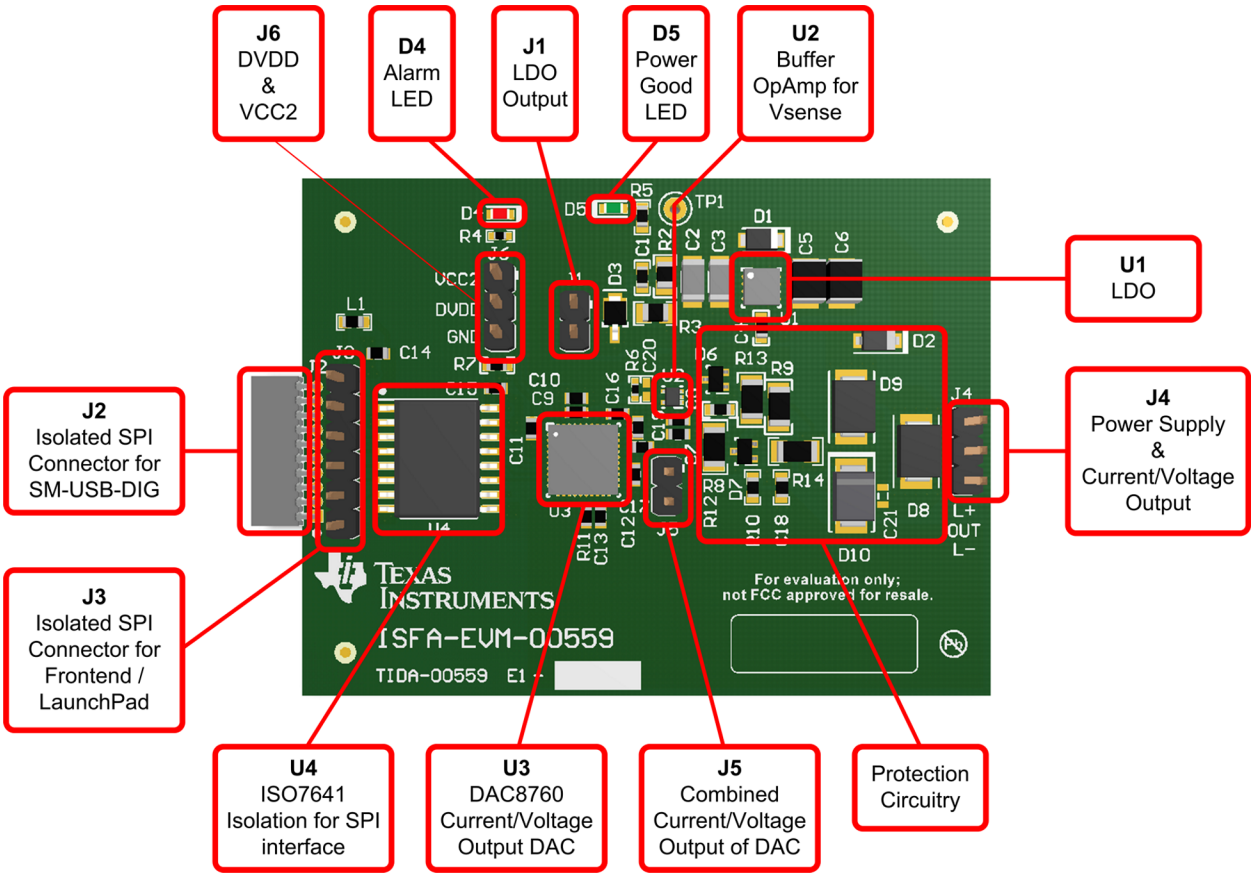


Figure 24. Board Description

2.1.2 Required Equipment

The following equipment is required to test the design:

- TIDA-00559 TI Design
- Digital multimeter (DMM): 6½-digit DMM, or for better accuracy 8½-digit DMM
- Power supply (15 V to 35 V)
- Load Resistor:
  - Current output: ≤ 320 Ω
  - Voltage output: ≥ 1000 Ω
- SM-USB-DIG: TI's USB-to-SPI converter
- PC with installed DAC8760EVM GUI
- Optional: Additional DMMs to measure the voltages at the different connectors (J1, J5, J6) or the power good of the LDO (TP1). See further details in the preceding Figure 24.

2.1.3 Hardware Setup—Current Output

Figure 25 shows the TIDA-00559 in the current output setup, which the following steps outline:

1. Connect SM-USB-DIG to J2. Make sure to connect them with the correct polarity. The text SM-USB-DIG has to be on top.
2. Connect the USB port of the SM-USB-DIG to a PC with the installed DAC8760EVM GUI.
3. Connect the power supply to J4:
   - GND to J4 – PIN3
   - +24V to J4 – PIN1
   - Set the current limit of the power supply to 50 mA.
4. Connect the DMM to J4:
   - Current input of the DMM to J4 – PIN2, with the load resistor R_{Load} in series
   - Common input of the DMM to J4 – PIN3
5. When switching on the power supply, the green LED D5 turns ON.

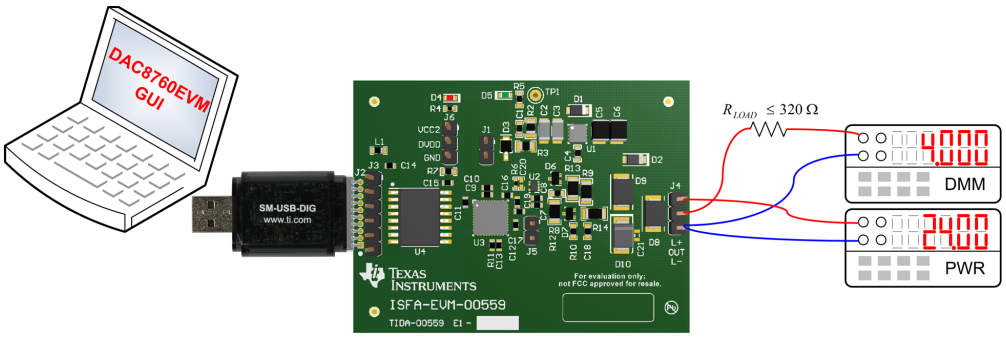


Figure 25. Hardware Setup for Current Output

2.1.4 Hardware Setup—Voltage Output

Figure 26 shows the TIDA-00559 in the voltage output setup, which the following steps outline:

1. Connect the SM-USB-DIG to J2 and make sure to connect them with the correct polarity. The text "SM-USB-DIG" must be on top.
2. Connect the USB port of the SM-USB-DIG to a PC with the installed DAC8760EVM GUI.
3. Connect the power supply to J4:
   - GND to J4 – PIN3
   - +24V to J4 – PIN1
   - Set the current limit of the power supply to 50 mA
4. Connect the DMM to J4:
   - Voltage input of the DMM to J4 – PIN2
   - Common input of the DMM to J4 – PIN3
5. Connect load resistor R_{Load} across J4 – PIN 2 and PIN3.
6. When switching on the power supply, the green LED D5 turns ON.

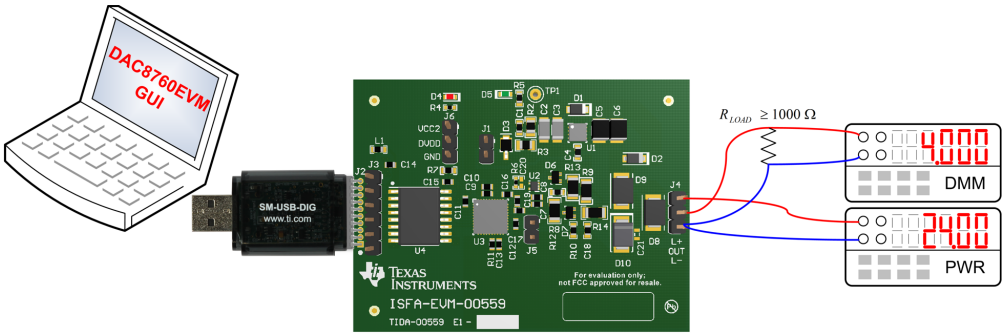


Figure 26. Hardware Setup for Voltage Output

2.1.5 Control of Hardware Through GUI

Refer to the DAC8760EVM user's guide to install the GUI. The same software for use with the DAC8760 device can be used to control the TIDA-00559.

After launching the DAC8760EVM software with connected hardware (as described in Figure 24) the popup interface in Figure 27 appears. For easiest operation, activate Auto-write Changes (see Figure 28). With this function enabled, every change in the GUI immediately writes to the DAC.

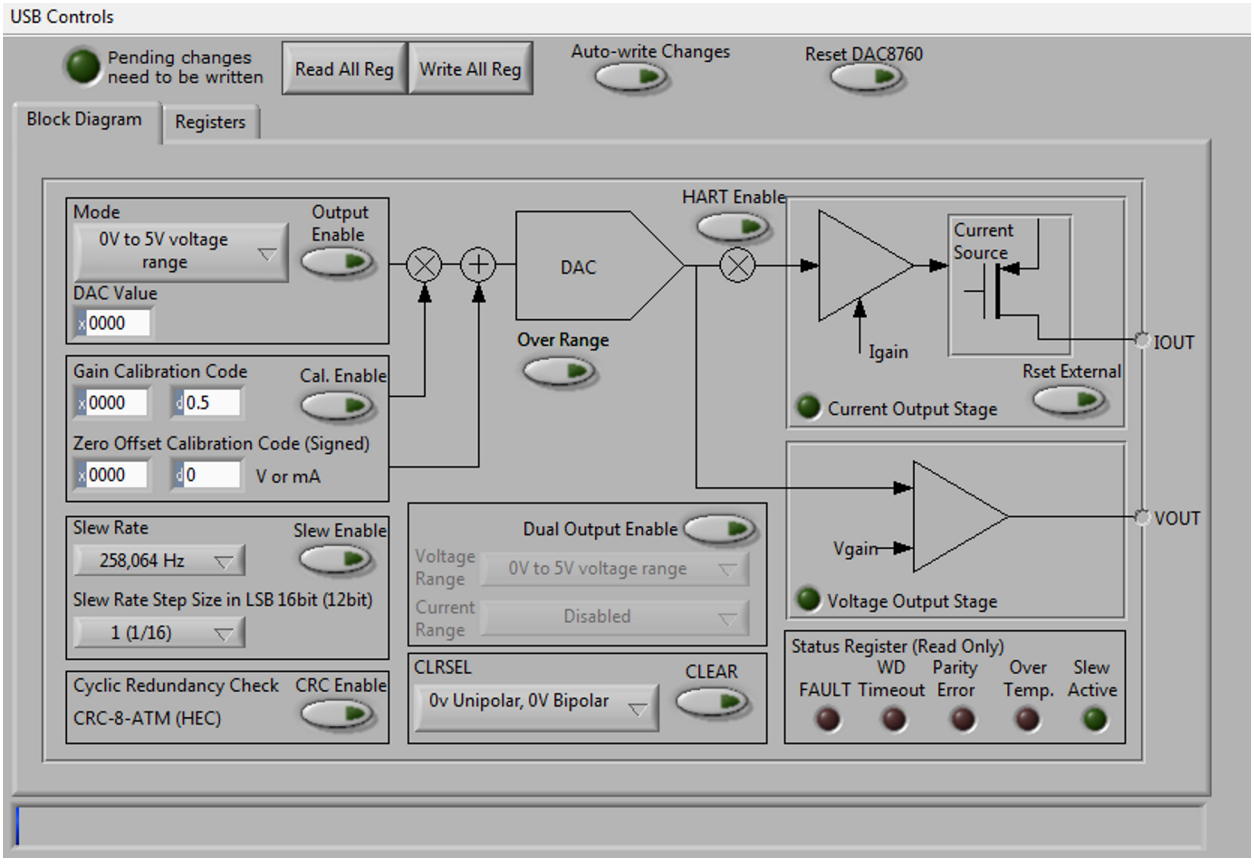


Figure 27. Start Screen of GUI

As Figure 28 shows, in the *Mode* window, select the "0mA to 24mA current range" option and press the *Output Enable* button to activate the DAC output. Because the DAC value is set per default to 0x0000, the current reading on the DMM is 0 mA.

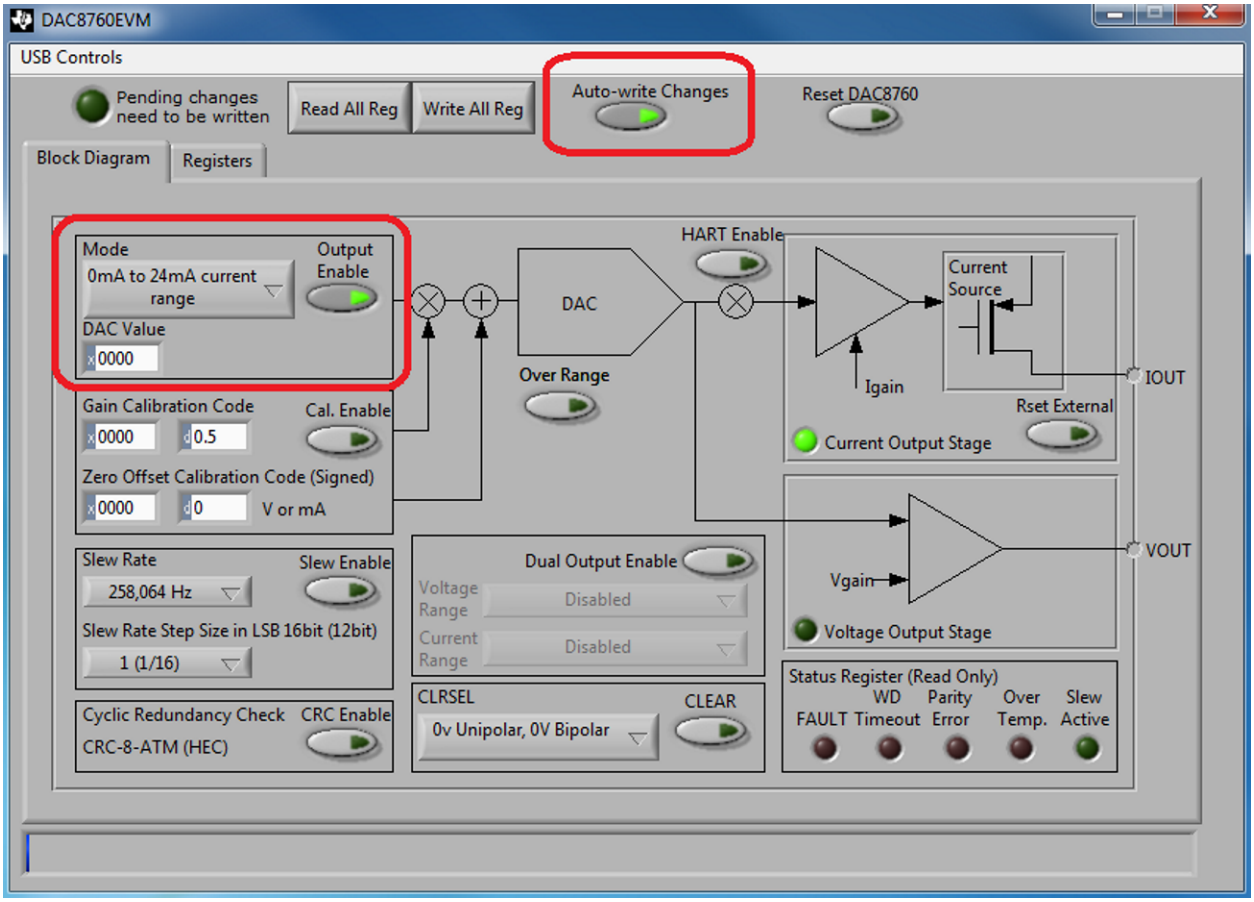


Figure 28. GUI With Current Output Activated

By changing the *DAC Value* in the *Mode* window from 0x0000 to 0xFFFF (see Figure 29) the current changes from 0 mA to 24 mA.

According to the DAC8760 data sheet, the output current in the three different current output modes can be set with the DAC code as follows (given for a 5-V reference):

1. 0- to 20-mA output range

$$I_{OUT} = 20\ mA \times \frac{DAC_{code}}{2^{16}} \quad (27)$$

2. 0- to 24-mA output range

$$I_{OUT} = 24\ mA \times \frac{DAC_{code}}{2^{16}} \quad (28)$$

3. 4- to 20-mA output range

$$I_{OUT} = 16\ mA \times \frac{DAC_{code}}{2^{16}} + 4\ mA \quad (29)$$

In the preceding Equation 27, Equation 28, and Equation 29, the DAC_{code} is the decimal equivalent of the code loaded into the DAC.

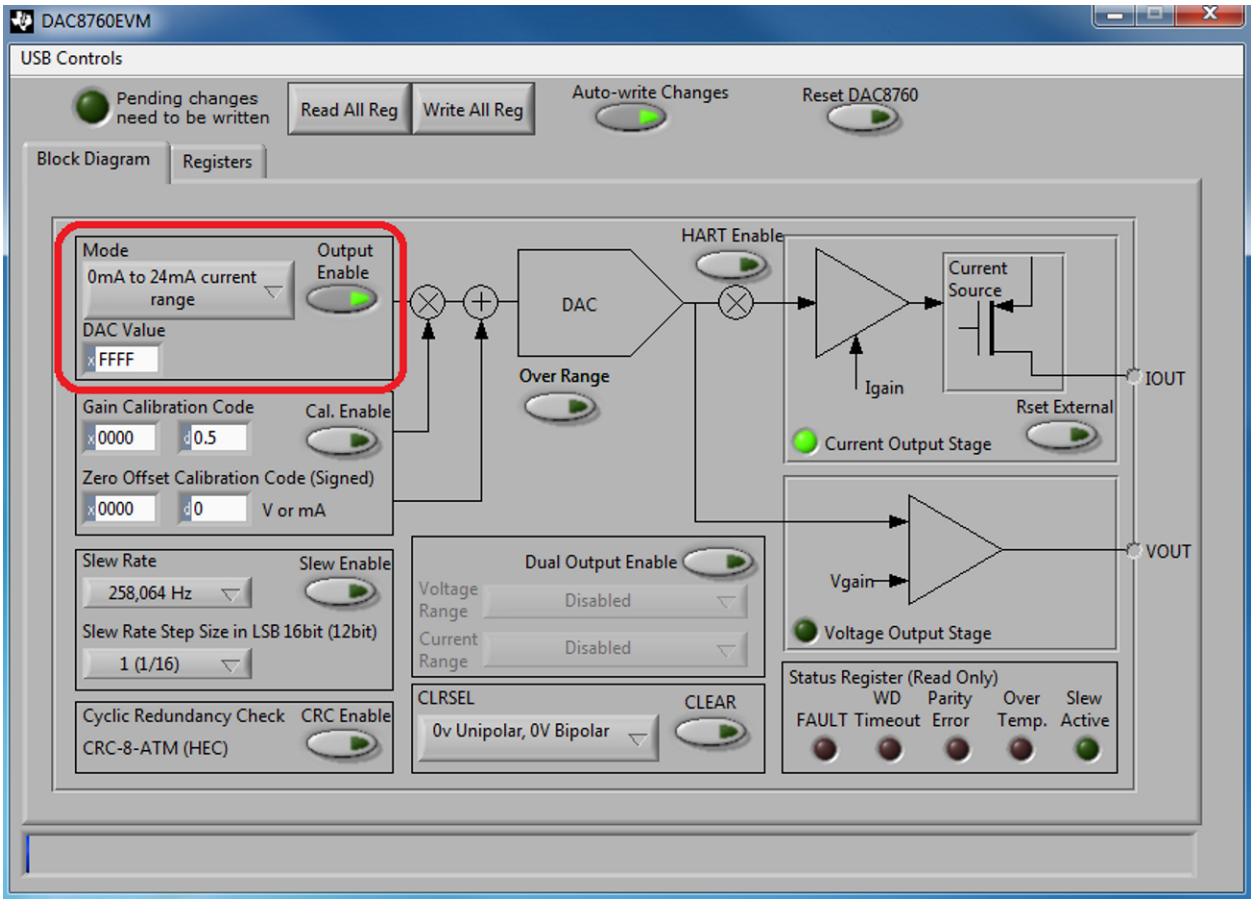


Figure 29. Changing Output Current in GUI

When evaluating the TIDA-00559 design in voltage output mode, change the setup according to Section 2.1.4 and change the settings in the GUI in the *Mode* window to the "0V to 10V voltage range" option (see Figure 30). By setting the DAC Value to 0x0000, the resulting voltage output is 0 V. As Figure 31 shows, by changing the DAC value to 0xFFFF, the maximum value of 10 V is measured with the DMM.

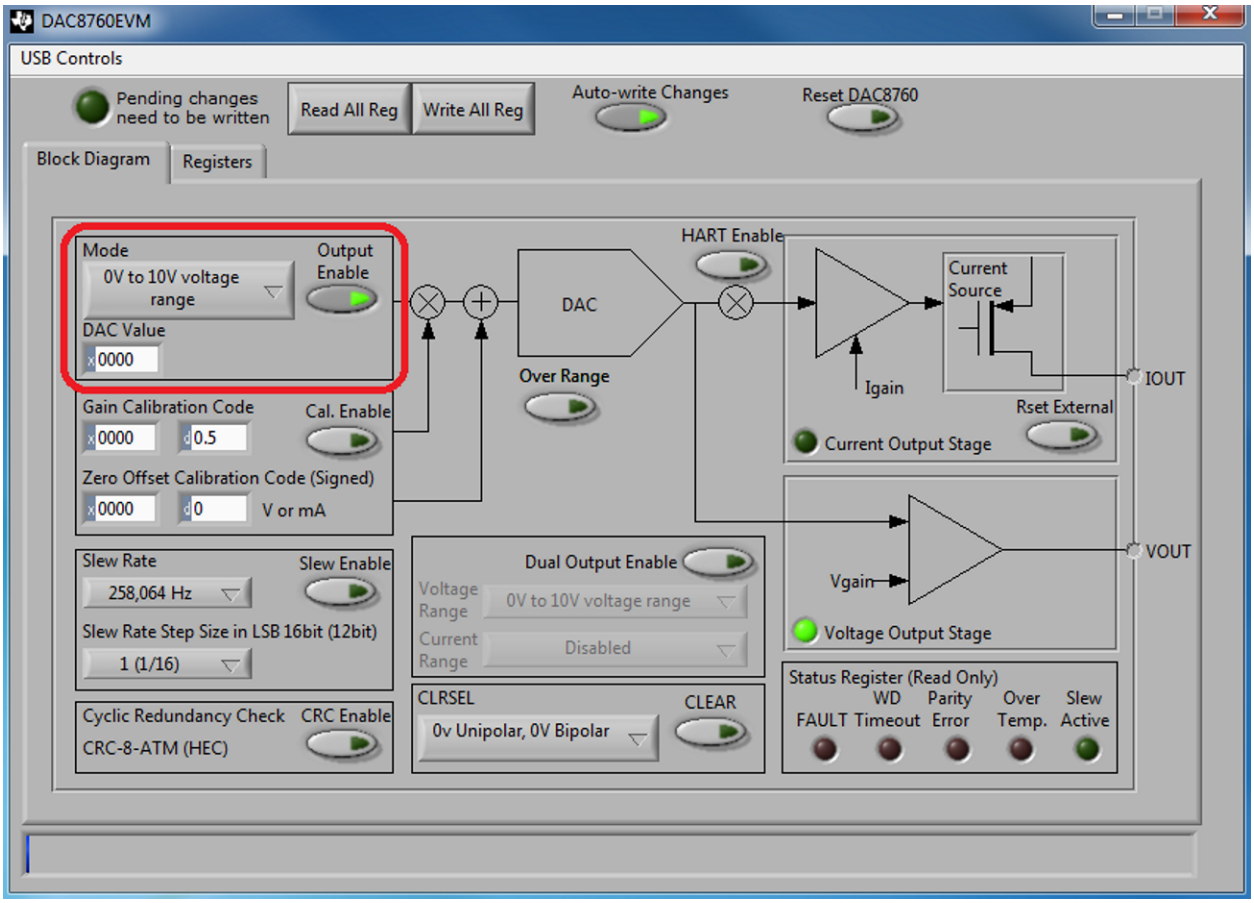


Figure 30. Activating Voltage Output

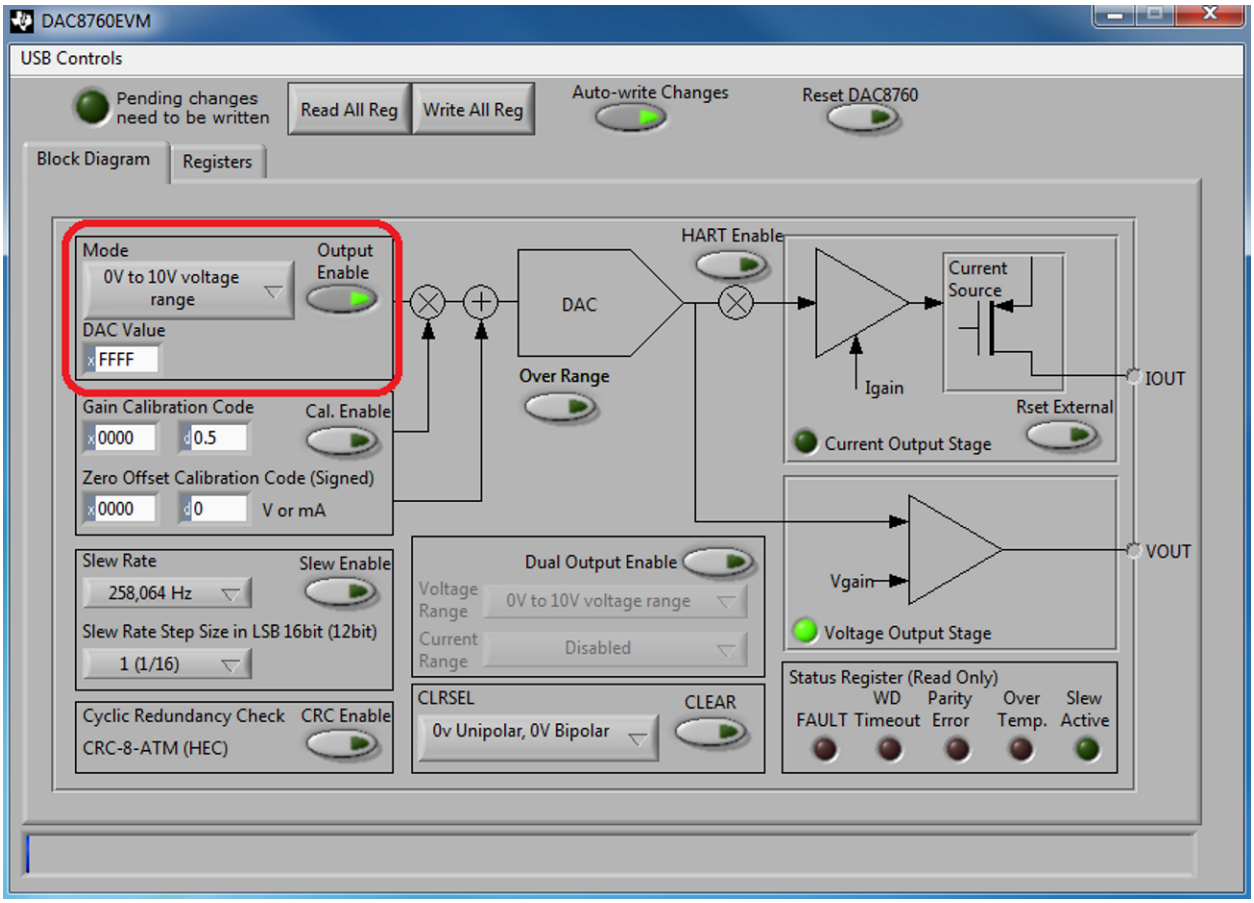


Figure 31. Changing Output Voltage in GUI

Therefore, the output voltage can be set using Equation 30:

$$V_{OUT} = V_{REF} \times Gain \times \frac{DAC_{code}}{2^{16}} \quad (30)$$

where

- DAC_{code} is the decimal equivalent of the code loaded to the DAC.
- V_{REF} is the reference voltage; for internal reference, V_{REF} = 5 V.
- Gain is automatically selected for a desired voltage output range, as Table 8 shows.

Table 8. Voltage Output Range versus Gain Setting (V_{REF} = 5 V)

VOLTAGE OUTPUT RANGE	GAIN
0 V to 5 V	1
0 V to 10 V	2
±5 V(1)	2
±10 V(1)	4

(1) The TIDA-00559 has been designed with a unipolar power supply. For this reason, only the output modes with positive output voltage work.

The DAC8760 has an overrange mode. By enabling this feature, the output voltage range can be extended by 10%. Refer to the DAC8760 data sheet for additional information.

The GUI also enables easy control of all the other features of the DAC8760, such as gain calibration, zero offset calibration, and slew rate settings.

CAUTION

Because the TIDA-00559 design has a combined voltage and current output, as a result of both outputs being tied together, the dual output feature (where both I_{OUT} and V_{OUT} are enabled) must not be enabled.

2.1.6 Control of Hardware Without SM-USB-DIG and GUI

In the case of controlling the TIDA-00559 design with an MCU, the isolated SPI is also available at the 2.54-mm (100-mil) spacing, 6-pin header J3. Table 2 shows a detailed pin assignment.

2.2 Firmware

The TI Design TIDA-00559 does not require firmware without an MCU on the design; however, when using the TIDA-00559 in combination with the USB-to-SPI tool, SM-USB-DIG, the available DAC8760EVM GUI software can be used to easily control the DAC. Refer to Section 2 and the DAC8760EVM user's guide for further information.

3 Testing and Results

3.1 Test Setup

3.1.1 Required Equipment

The following equipment was used for testing the TIDA-00559 TI Design:

- TIDA-00559 TI Design
- DMM: 8½-digit DMM HP3458 (used as DMM5, Figure 32)
- DMM: 6.5-digit DMM Agilent 34980A, including multiplexer unit (used as DMM1 to DMM4, Figure 32)
- Power supply: Agilent E3631A
- PC with installed DAC8760EVM GUI, Python Environment, Energia Environment
- MSP430FR5969 LaunchPad
- Load Resistor: 320R and 1000R

3.1.2 Setup Overview

Figure 32 and Figure 33 show the two basic test setups for testing the TIDA-00559 design in current output mode and voltage output mode. The main differences between these modes are DMM5, which is either set to measure DCV or DCI and the load resistor.

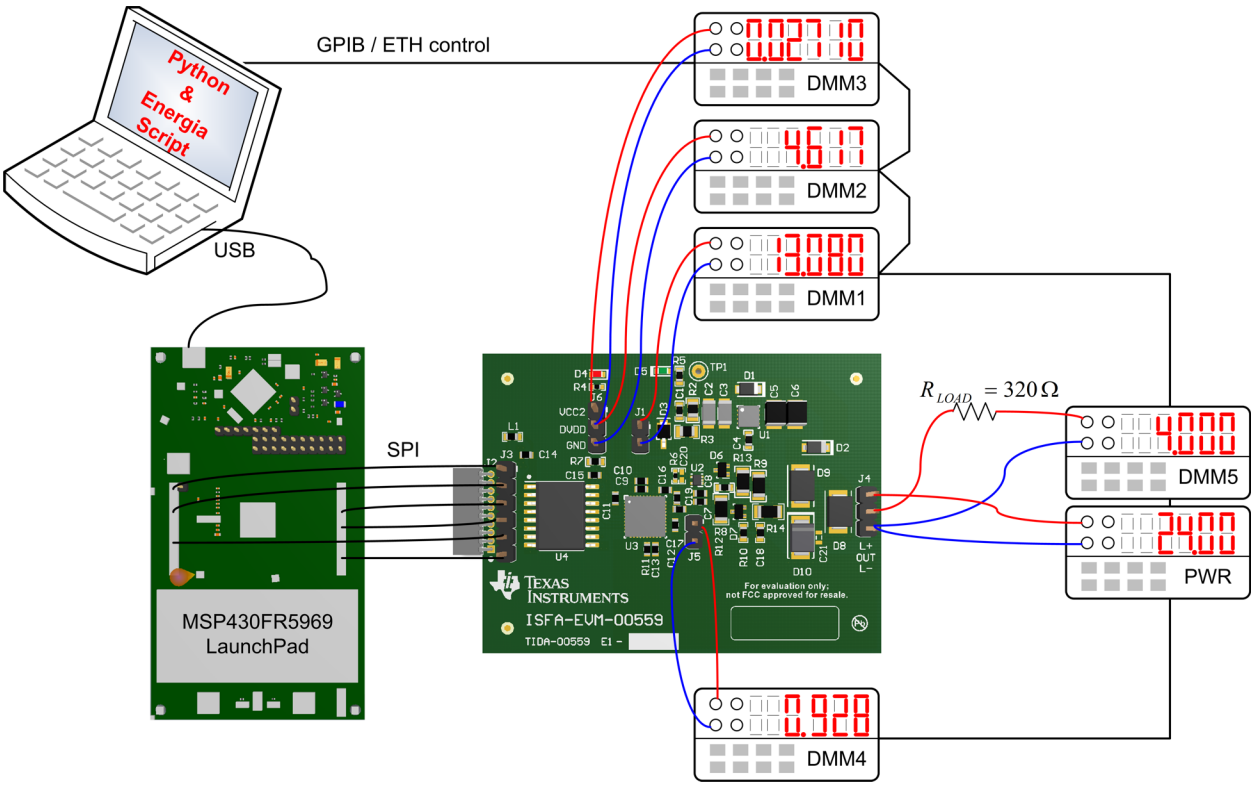


Figure 32. TIDA-00559 Test Setup Current Output

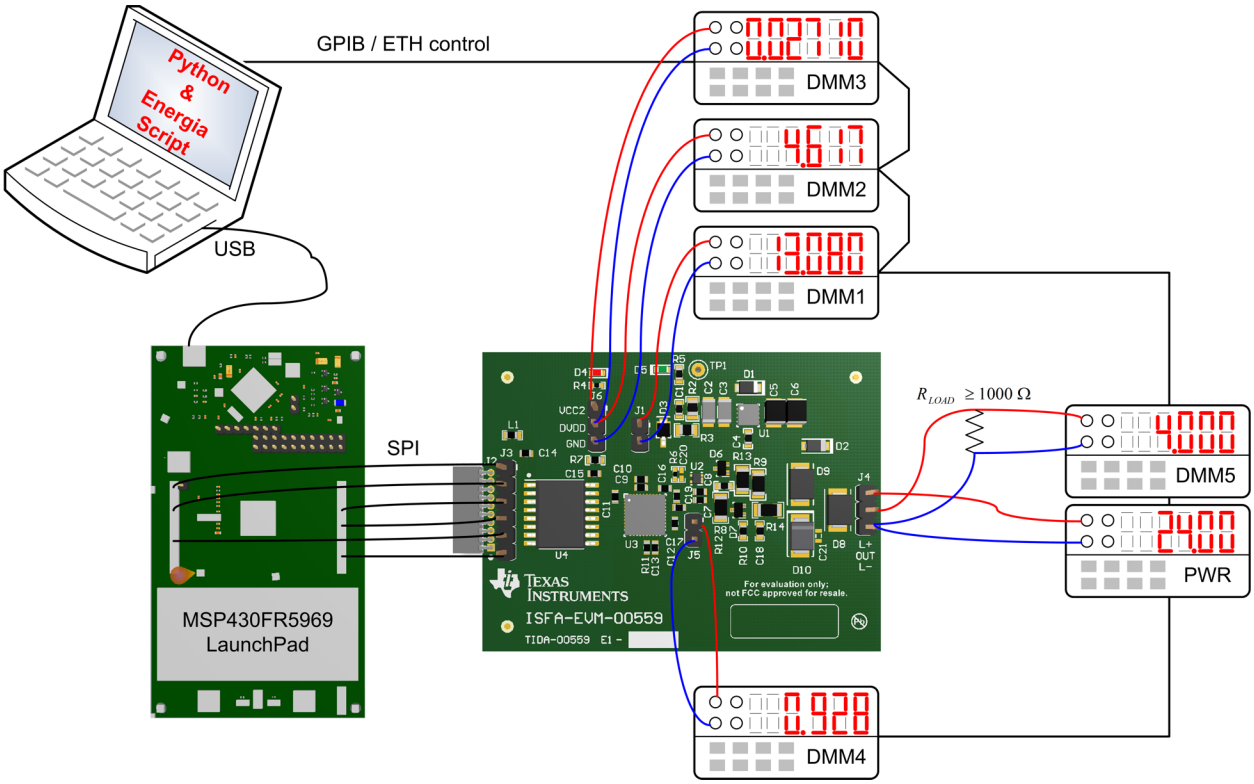


Figure 33. TIDA-00559 Test Setup Voltage Output

3.1.3 Setup Description

To automate the entire test process, an MSP430FR5969 LaunchPad is used to program the DAC. The LaunchPad itself communicates with the PC through a virtual COM port. The LaunchPad works as a UART-to-SPI converter. The code for the MSP430 has been developed in Energia.

The measurement instruments are controlled with GPIB and Ethernet. The overall control of the setup is realized with a Python script.

For the purposes of testing the TI Design, all voltages available at the connectors are measured and stored.

3.2 Test Results

3.2.1 Voltage Output

3.2.1.1 Total Unadjusted Error (TUE)

Figure 34 shows the total unadjusted error (TUE) of the TIDA-00559 testing in voltage output mode.

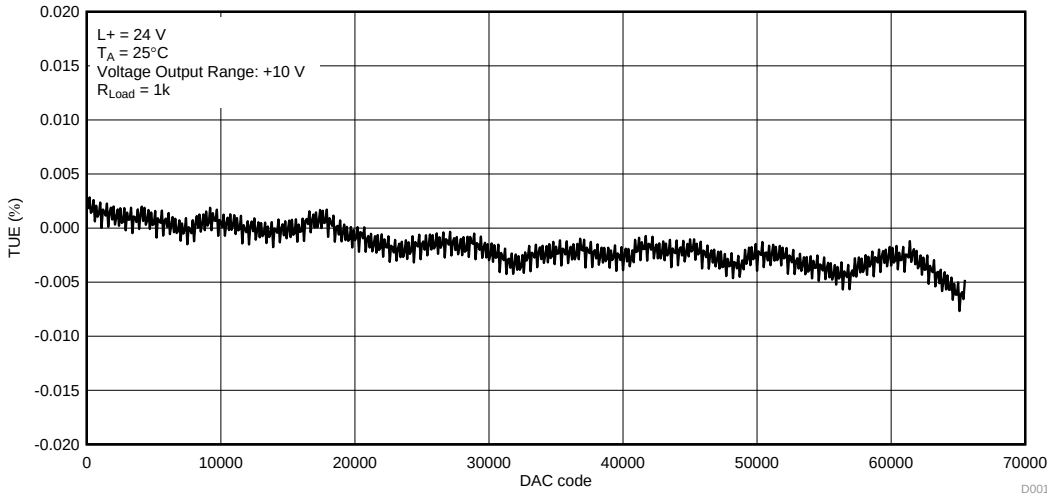


Figure 34. TUE in Voltage Output Mode

For this test, the DAC codes from 0 to 2^{16} have been swept in steps of 100. The TUE in % is calculated as the following Equation 31:

$$\%TUE = \frac{\left(V_{OUT\_MEASURED} - V_{OUT\_SET}\right)}{10\ V} \times 100\% \tag{31}$$

where $V_{OUT\_SET} = V_{REF} \times 2 \times \frac{DAC_{CODE}}{2^{16}}$

3.2.1.2 Absolute Voltage Output Error

Compared to the preceding Figure 34, Figure 35 shows the absolute voltage error (see Equation 32).

$$V_{OUT\_ERROR} = V_{OUT\_MEASURED} - V_{OUT\_SET} \tag{32}$$

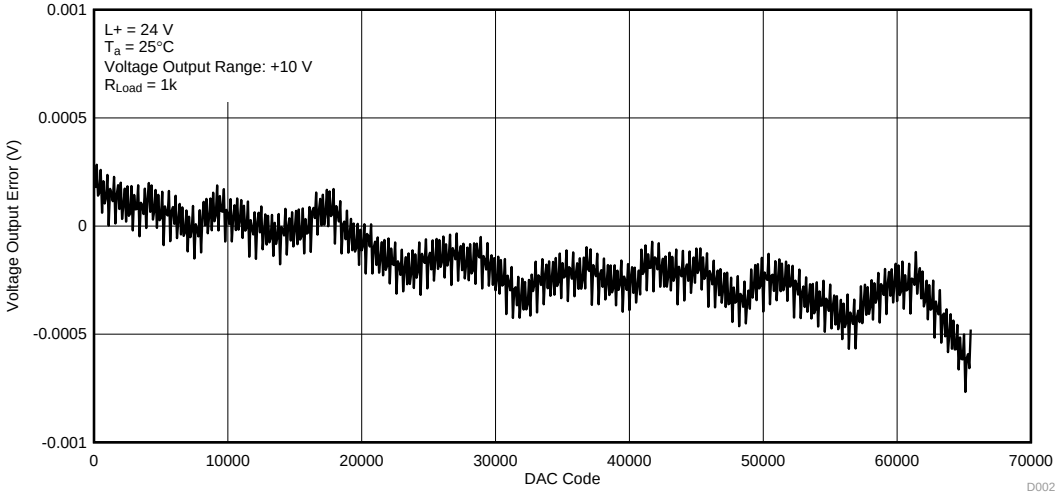


Figure 35. Absolute Voltage Output Error

3.2.1.3 DAC Voltage Footroom

In the voltage output mode and in combination with a single supply (unipolar), the DAC is not able to fully output 0 V because of the footroom. Figure 36 shows the differences between the ideal calculated voltage output for DAC codes from 0 to 160, as compared to the actual measured voltage output. The footroom is approximately 8 mV (DAC code = 52). At this point, the voltage output cannot continue decreasing.

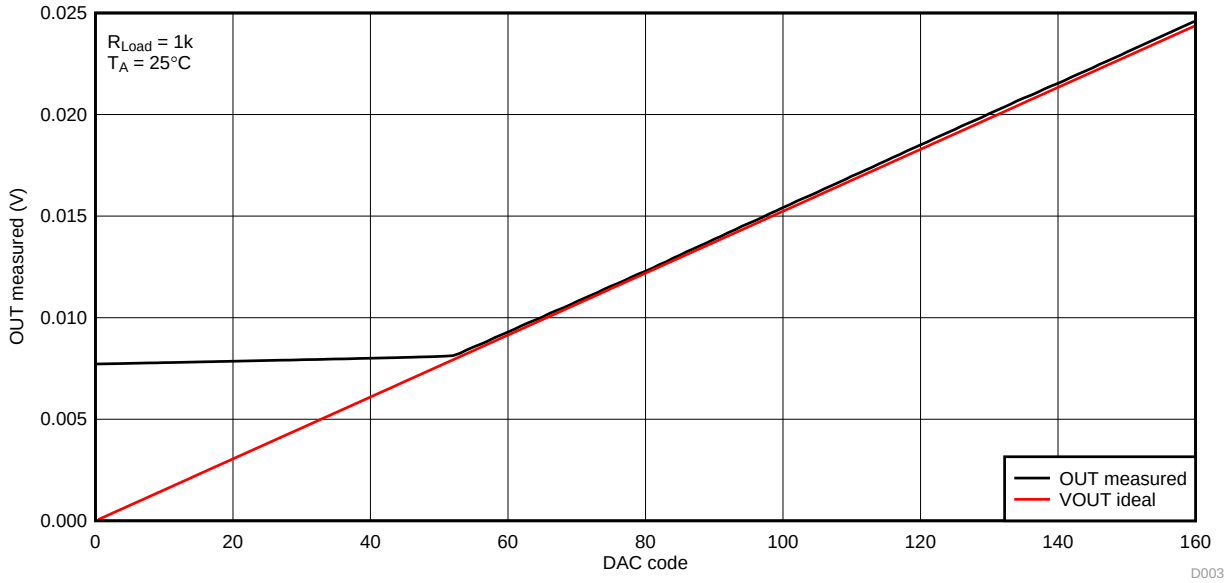


Figure 36. DAC Voltage Footroom

3.2.2 Power Supply and Protection Circuitry

3.2.2.1 LDO Headroom

Figure 37 shows the resulting headroom voltage of the LDO for different values of L+. For further details, see Section 1.3.4).

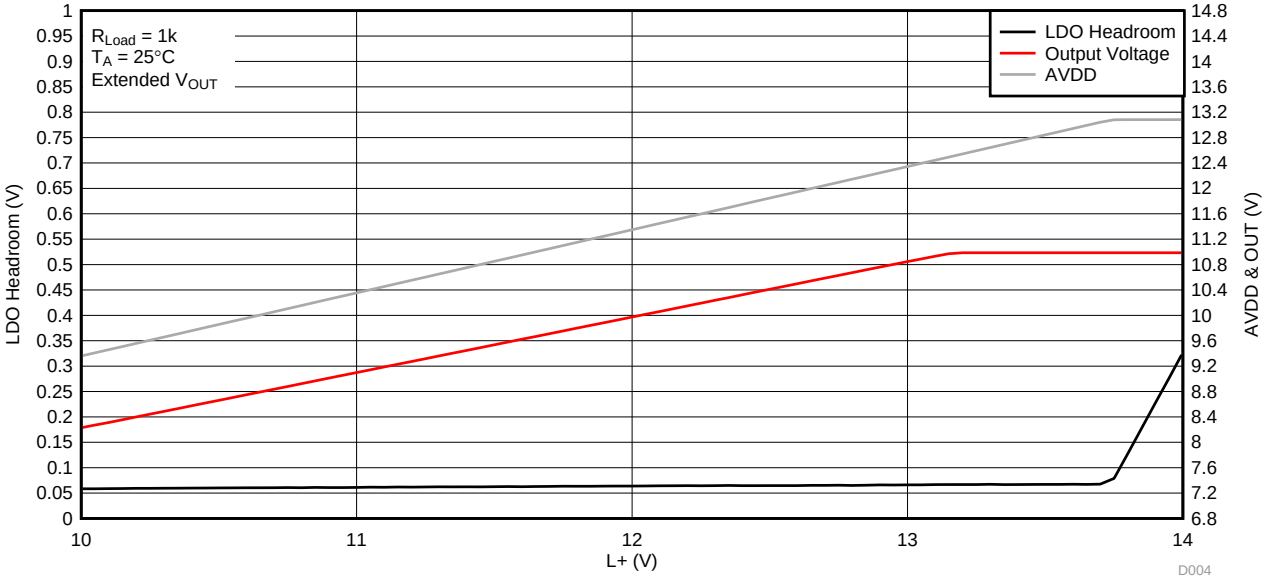


Figure 37. System Performance versus Input Power Voltage (L+)

3.2.2.2 Forward Voltage of Reverse Protection Diode D2

Figure 38 shows the measured forward voltage of the reverse protection diode D2 for different values of L+.

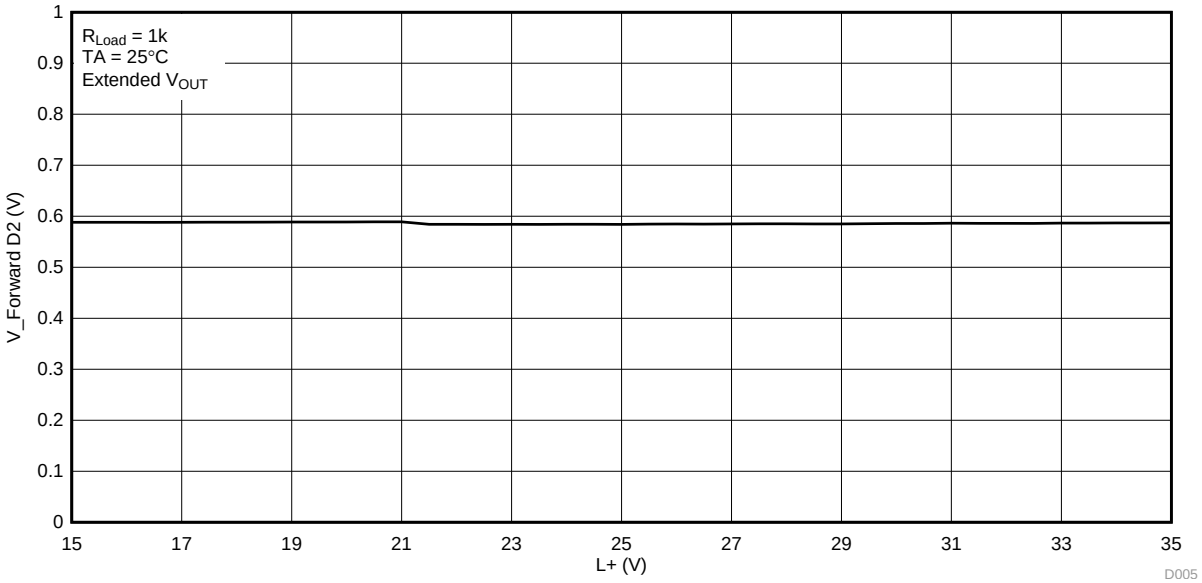


Figure 38. Forward Voltage of Reverse Protection Diode D2

3.2.3 PCB Thermal Images

The following figures show thermal images of the printed-circuit board (PCB) for different conditions

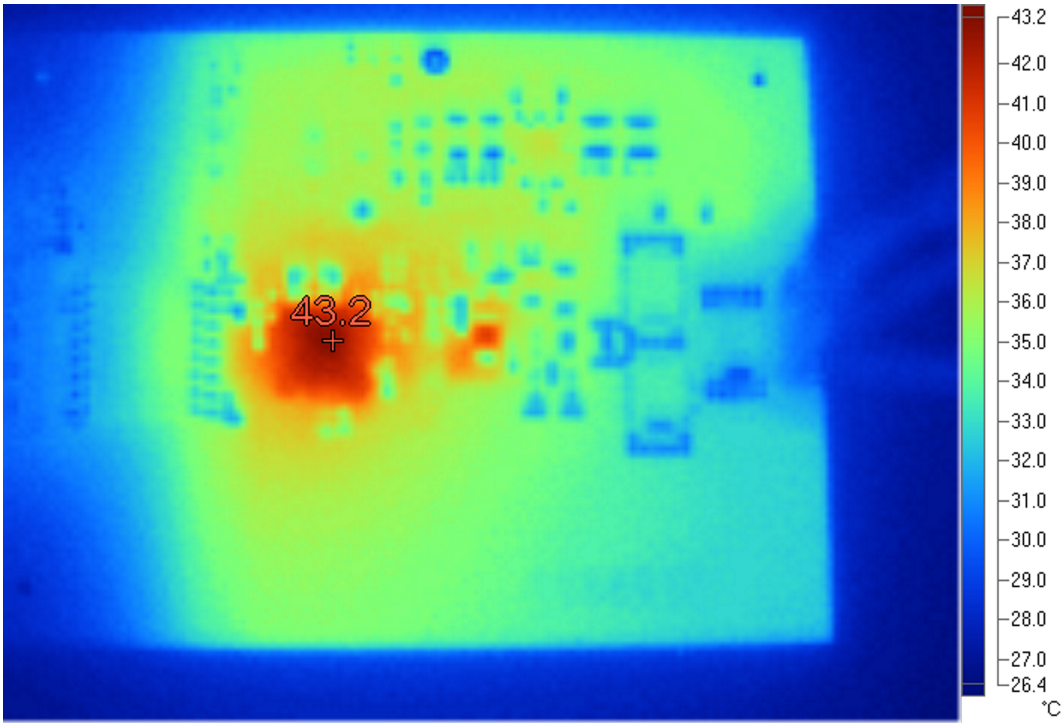


Figure 39. V_{LOOP} = 15 V, I_{OUT} = 24 mA, and R_{Load} = 0R

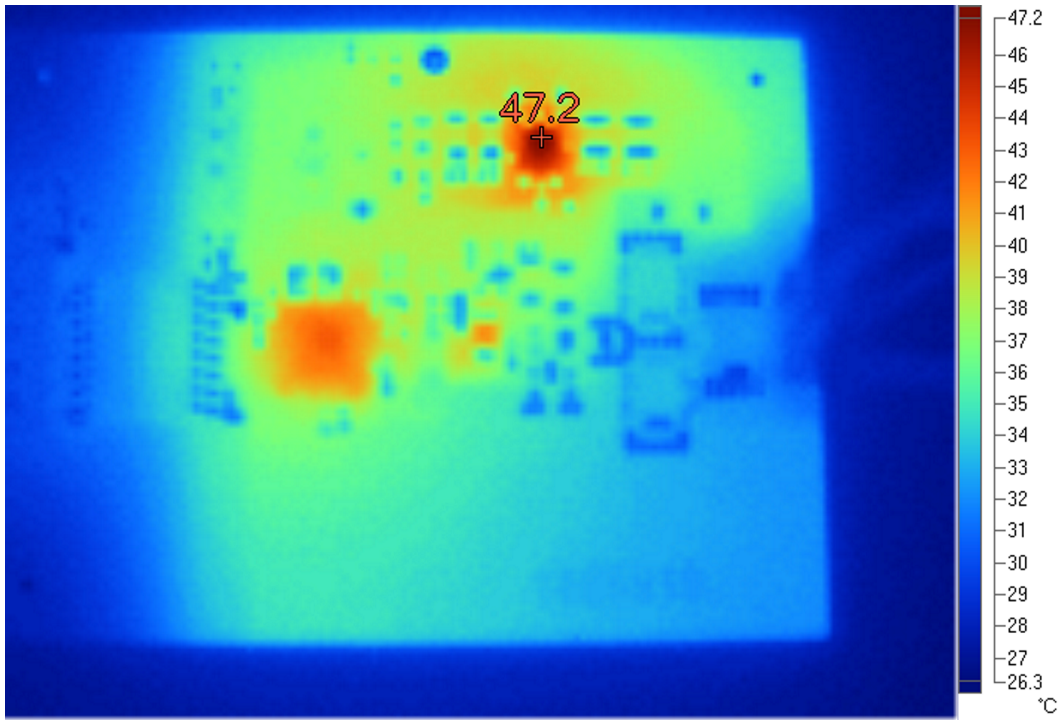


Figure 40. V_{LOOP} = 24 V, I_{OUT} = 24 mA, and R_{Load} = 0R

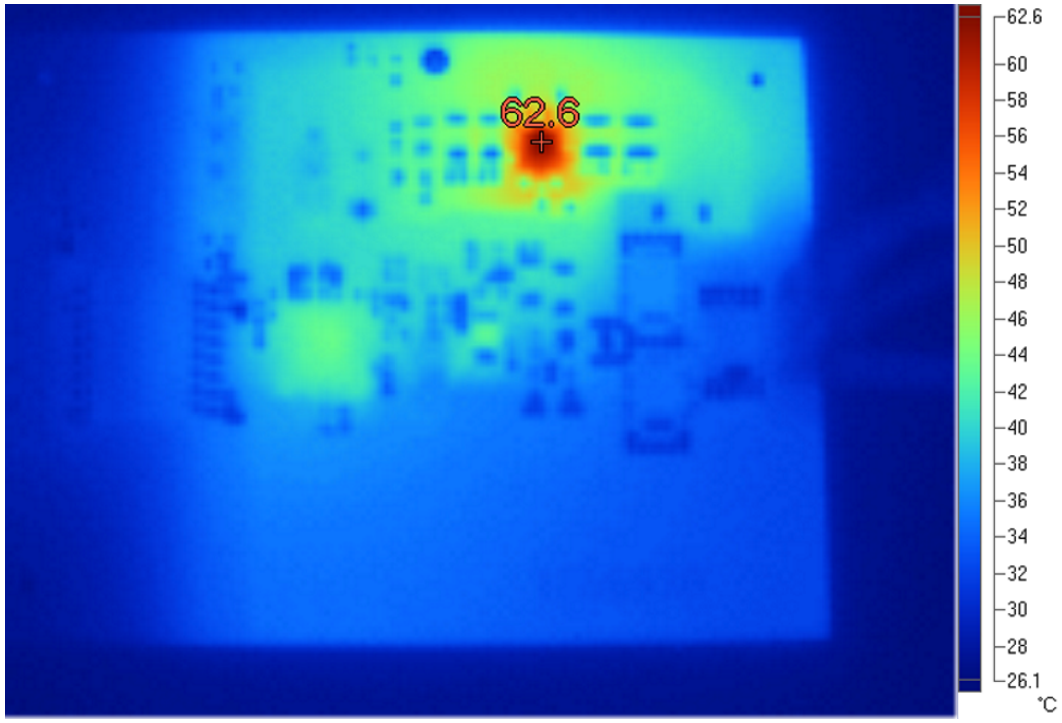


Figure 41. V_{LOOP} = 35 V, I_{OUT} = 24 mA, and R_{Load} = 0R

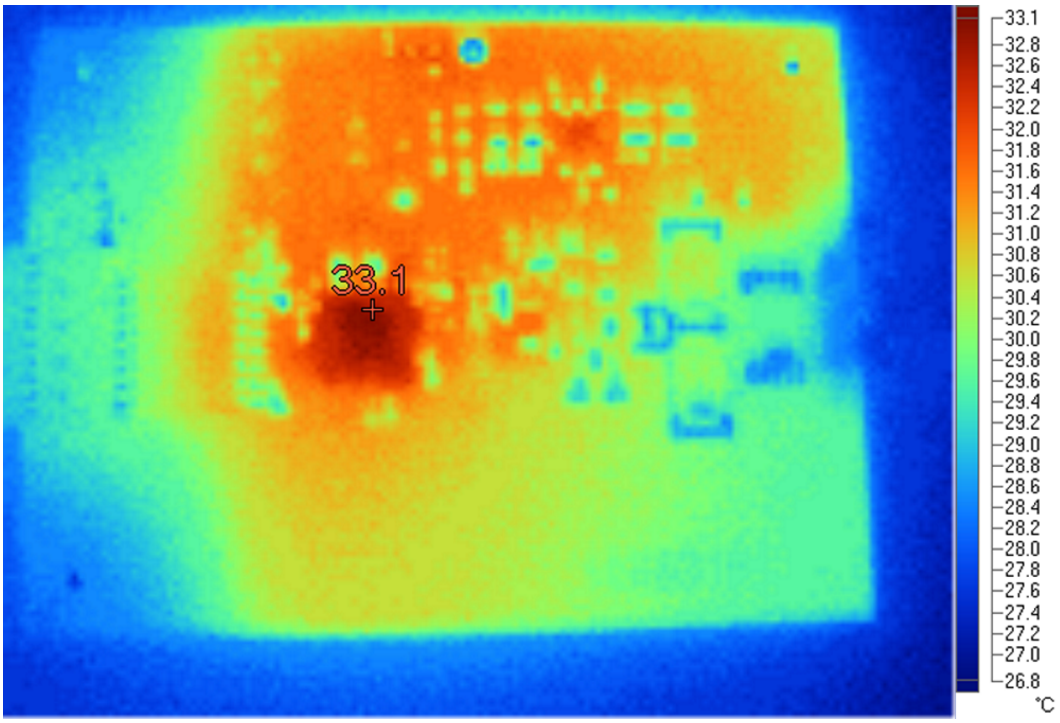


Figure 42. V_{LOOP} = 15 V, V_{OUT} = 10 V, and R_{Load} = 0k

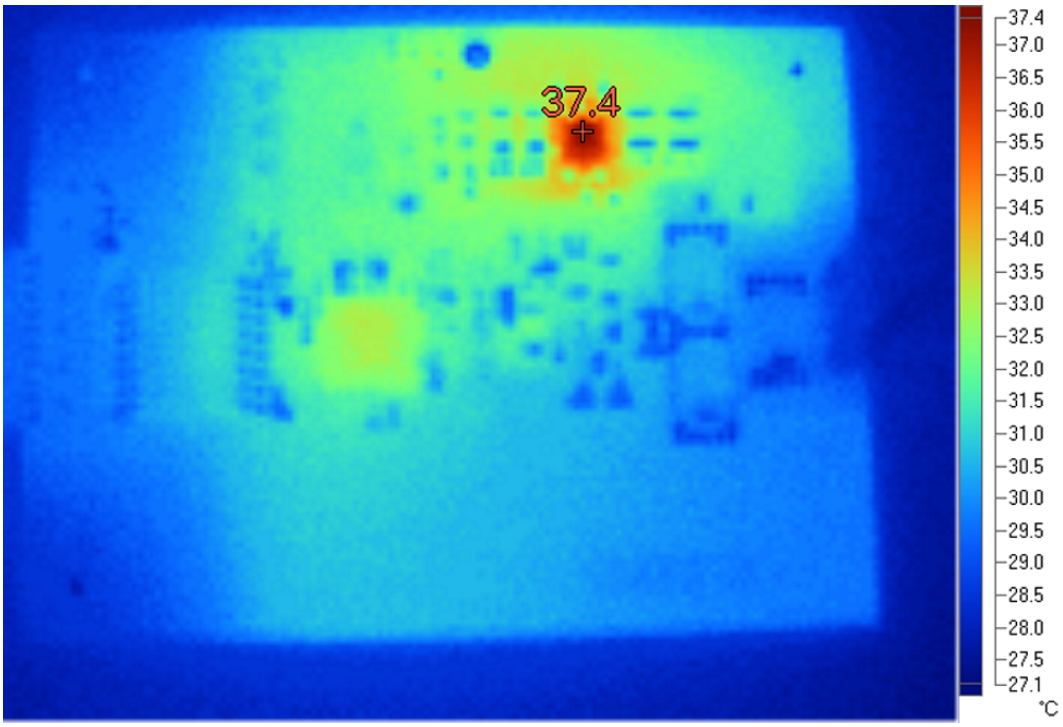


Figure 43. V_{LOOP} = 24 V, V_{OUT} = 10 V, and R_{Load} = 0k

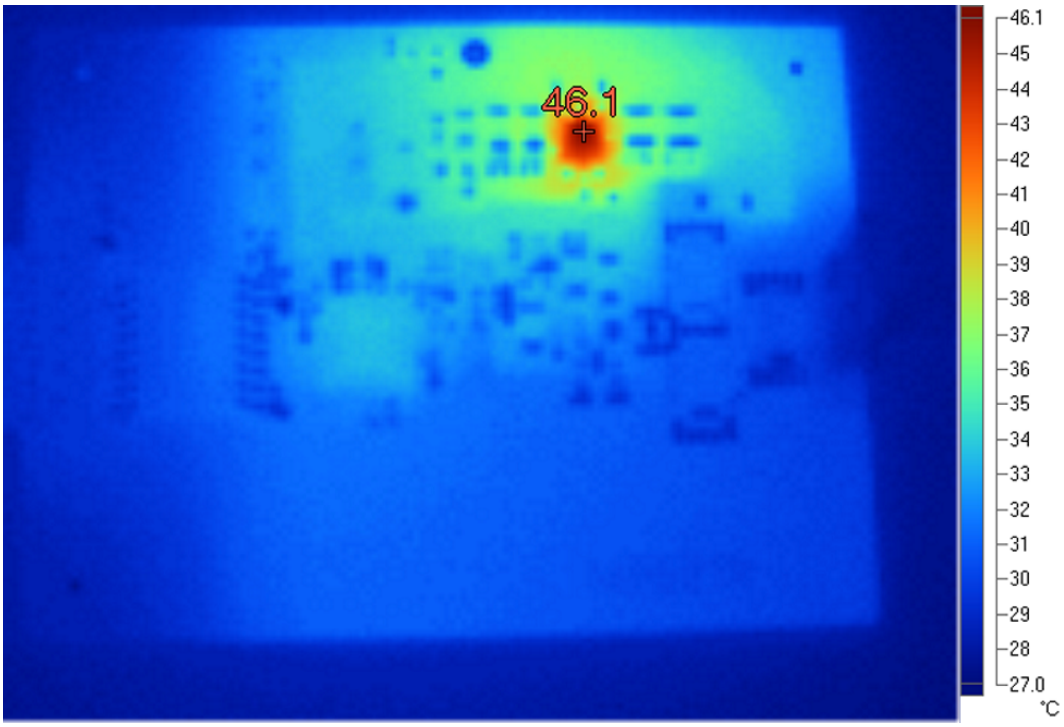


Figure 44. V_{LOOP} = 35 V, V_{OUT} = 10 V, and R_{Load} = 0k

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-00559.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00559.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00559.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-00559.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00559.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00559.

5 Software Files

To download the software files, see the design files at TIDA-00559.

6 Related Documentation

1. Texas Instruments, *ISO76x1 Low-Power Triple and Quad-Channels Digital Isolators*, ISO7631Fx Data Sheet (SLLSEC3)
2. Texas Instruments, *DACx760 Single-Channel, 12- and 16-Bit Programmable Current and Voltage Output Digital-to-Analog Converters for 4-mA to 20-mA Current Loop Applications*, DACx760 Data Sheet (SBAS528)
3. Texas Instruments, *TPS7A16 60-V, 5- μA I_Q, 100-mA, Low-Dropout Voltage Regulator With Enable and Power-Good*, TPS7A16 Data Sheet (SBVS171)
4. Texas Instruments, *Combined Voltage and Current Output Terminal for Analog Outputs (AO) in Industrial Applications*, TIPD119 Reference Guide (SLAU519)
5. Texas Instruments, *SM-USB-DIG Platform*, SM-USB-DIG Platform User's Guide (SBOU098)
6. Texas Instruments, *Combined Voltage and Current Output with the DACx760*, DACx760 Application Report (SBAA199)
7. Texas Instruments, *IEC 61000-4-x Tests for TI's Protection Devices*, Application Report (SLVA711)
8. STMicroelectronics, *SM6T*, SM6T Data Sheet (http://www.st.com/content/ccc/resource/technical/document/datasheet/6f/2d/a6/9e/56/51/48/15/CD00000725.pdf/files/CD00000725.pdf/jcr:content/translations/en.CD00000725.pdf)
9. STMicroelectronics, *SM6TY*, SM6TY Data Sheet (http://www.st.com/content/ccc/resource/technical/document/datasheet/7c/00/1c/38/a4/c1/4b/ae/CD00279657.pdf/files/CD00279657.pdf/jcr:content/translations/en.CD00279657.pdf)
10. STMicroelectronics, *SMM4F*, SMM4F Data Sheet (http://www.st.com/content/ccc/resource/technical/document/datasheet/5d/b3/40/b8/ac/6c/49/a2/CD00178940.pdf/files/CD00178940.pdf/jcr:content/translations/en.CD00178940.pdf)
11. Diodes Incorporated, *LOW CAPACITANCE, ESD PROTECTION DIODE ARRAY*, DESD1P0RFW Data Sheet (http://www.diodes.com/_files/datasheets/DESD1P0RFW.pdf)
12. Vishay, *Pulse Proof, High Power Thick Film Chip Resistors*, CRCW-HP e3 Data Sheet (http://www.vishay.com/docs/20043/crcwhpe3.pdf)

6.1 Trademarks

All trademarks are the property of their respective owners.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ('TI") reference designs are solely intended to assist designers ("Designer(s)") who are developing systems that incorporate TI products. TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.

TI's provision of reference designs and any other technical, applications or design advice, quality characterization, reliability data or other information or services does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such reference designs or other items.

TI reserves the right to make corrections, enhancements, improvements and other changes to its reference designs and other items.

Designer understands and agrees that Designer remains responsible for using its independent analysis, evaluation and judgment in designing Designer's systems and products, and has full and exclusive responsibility to assure the safety of its products and compliance of its products (and of all TI products used in or for such Designer's products) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to its applications, it has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any systems that include TI products, Designer will thoroughly test such systems and the functionality of such TI products as used in such systems. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

Designers are authorized to use, copy and modify any individual TI reference design only in connection with the development of end products that include the TI product(s) identified in that reference design. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of the reference design or other items described above may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS AND OTHER ITEMS DESCRIBED ABOVE ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNERS AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS AS DESCRIBED IN A TI REFERENCE DESIGN OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

TI's standard terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products. Additional terms may apply to the use or sale of other types of TI products and services.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265