TI Designs: TIDA-01053

ADC Driver Reference Design Optimizing THD, Noise, and SNR for High Dynamic Range Instrumentation

Description

The TIDA-01053 is an ADC driver reference design to optimize total harmonic distortion (THD), noise, and the full system signal-to-noise ratio (SNR) for high dynamic range instrumentation. The data acquisition system (DAQ) requirements determine the analog-to-digital converter (ADC) resolution and sampling rate. As a result, the selected input sampling capacitor of the ADC dictates the minimum value of the charge bucket capacitor belonging to the input driver filter, which presents stability and distortion challenges for the driver amplifier. This design explores the tradeoffs between the driver amplifier performance and driver filter performance to optimize the signal chain SNR. Specifically, THD, noise, and stability for both single-ended and fully-differential driver amplifiers have been studied. This reference design describes all the key design theories to guide users through the part selection process and design optimization. This design also presents the schematic, board layout, hardware testing, and results.

Resources

TIDA-01053	Design Folder
THS4551	Product Folder
REF6050	Product Folder
OPA625	Product Folder
OPA376	Product Folder
TIPD115	Design Folder
TINA-TI™	SPICE Simulator

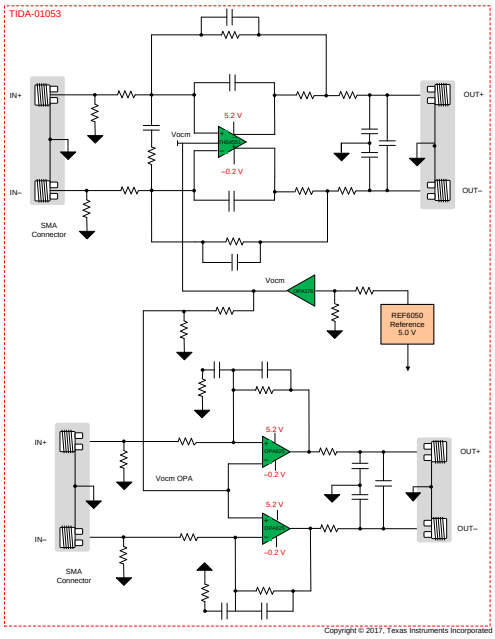
TI E2E™ Community — ASK Our E2E Experts

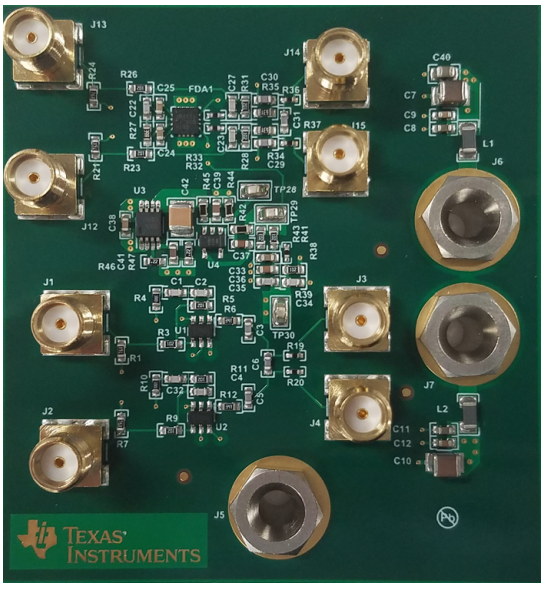
Features

- Noise- and THD-Optimized ADC Driver
- Fully Differential Driver
- Dual Op Amp Configuration
- Noise and THD Measurements
- Design Theory TINA-TI™ simulations

Applications

- Data Acquisition
- Industrial Lab Instrumentation
- Semiconductor Test Equipment
- LCD Test Equipment
- Battery Test Equipment





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1 System Description

System-to-noise ratio (SNR), total harmonic distortion (THD), spurious-free dynamic range (SFDR), and the resulting effective number of bits (ENOB) are the key specifications in any data acquisition (DAQ) system for applications such as semiconductor tests, industrial lab instrumentation, LCD tests, and battery tests. Ensuring that the ADC driver within the analog front end (AFE) is optimized to maximize SNR and ENOB is important (see Figure 1).

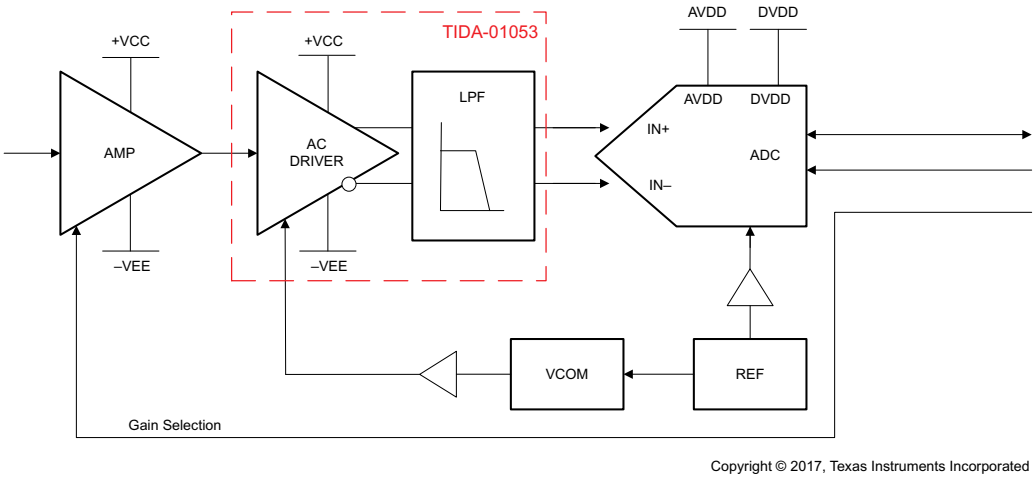

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Figure 1. Generic AFE

Another important step is to ensure that the AFE circuit performance that drives the ADC input does not significantly degrade the performance of the whole system. The power versus noise design tradeoffs for the AFE are fairly well understood and can be simulated in TINA-TI™, which makes the part selection and optimization process a relatively straightforward task; however, the THD performance of the design is more complicated. THD performance cannot be simulated with TINA-TI™ software because it requires the full circuit model, which is proprietary and not available in most cases. The simplified model provided for download is not designed for THD simulations. The designers have to rely on the specification information for their part selection and optimization process, which is also not trivial. The THD performance of the ADC driver varies not only with the input and output voltage amplitude but also with many other parameters including the load conditions and feedback configurations. The THD specification information is usually very limited and most often included for a resistive load condition in one of the gain configurations. Alternatively, the ADC input presents a highly capacitive load for the driver, which is a very different condition compared to the data usually available in the specifications. This realization adds additional challenges to the design and optimization process because designers often have to rely mainly on their intuition and experience, thus making trial and error experiments a common phase of the design. The process of trail and error adds time and uncertainty to the design process and often results in a final product not fully optimized.

While this design does not address the fundamental challenges of the THD optimization for the ADC driver, the objective of this design is to provide the customers with some additional information on the THD performance of different architectures and discuss the common tradeoffs during this design phase. The design is based on the two most-common ADC front-end configurations: fully differential and two single-ended amplifiers. Both configurations have specific applications where they perform better than the other. This design aims to optimize and highlight the performance of ADC front ends utilizing both configurations.

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1.1 Key System Level Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	MEASURED
Number of channels	Dual	Dual
Input type	Differential	Differential
Input range	±2.5-V fully differential	±2.5-V fully differential
Noise (flat-band) at 100 kHz	11 nV/√Hz	10.72 nV/√Hz
HD2/HD3 crossing at –130 dBc (4 V_{PP} V_{OUT})	50 kHz	59.7 kHz
Form factor (L × W)	64 mm × 68 mm	64 mm × 68 mm

2 System Overview

2.1 Block Diagram

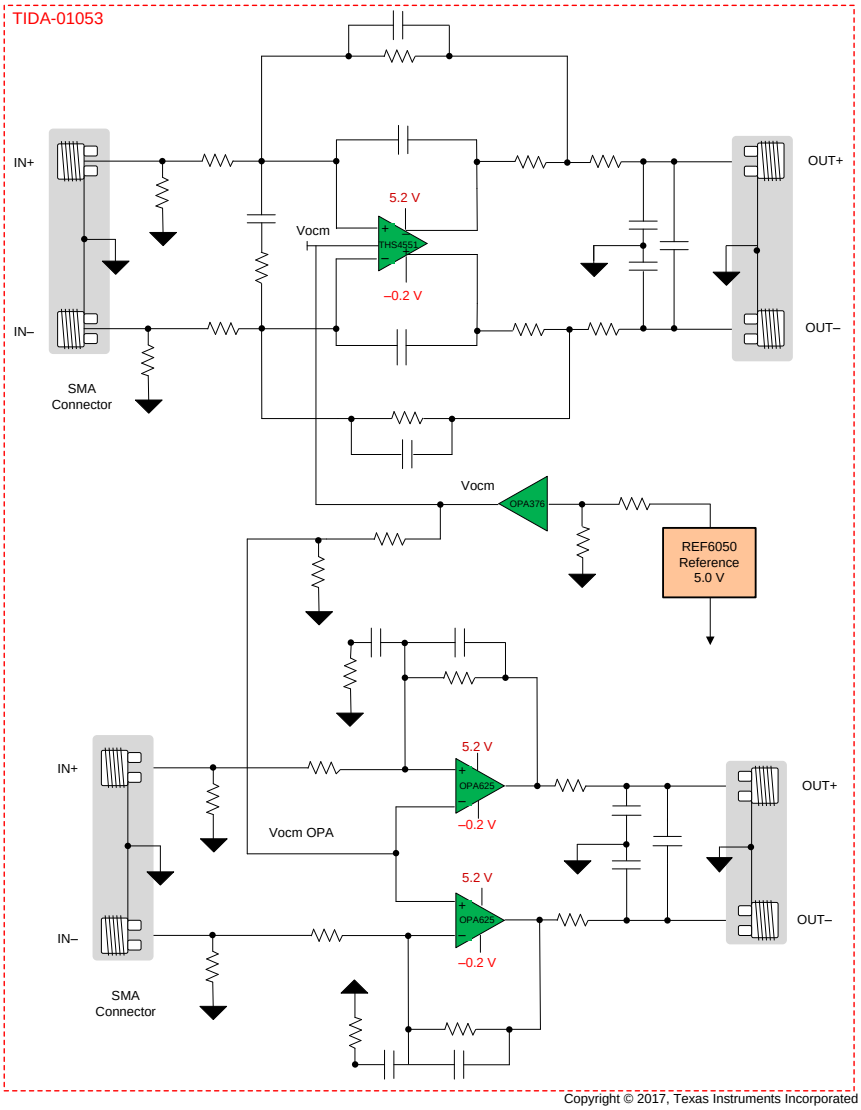

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Figure 2. TIDA-01053 Block Diagram

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2.2 System Design Theory

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a flywheel RC filter. The amplifier is used for input signal conditioning and its low output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the ADC switched capacitor input stage and also assists as an antialiasing filter for band-limiting the front-end circuitry wideband noise. Careful ADC driver circuit design is required to realize the resolution, linearity, and noise performance capabilities of the modern day SAR ADCs. The input driver must support the following key specifications:

1. Rail-to-rail input and output (RRIO)
2. Low noise
3. High small-signal bandwidth with low distortion at high frequencies
4. Fast Settling
5. Low power

The ADC input must settle within the covered specified resolution during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, amplifier datasheets specify output settling performance only up to 0.1% to 0.001%, which may not be sufficient for high-accuracy converters (> 16b). Therefore, the designer must verify the input driver settling behavior with simulators such as TINA-TI to assist amplifier selection.

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum of interest known as aliasing. An analog antialiasing filter must be used to remove the noise and harmonic content from the input signal before ADC sampling. This filter is typically designed as an RC low-pass, where the 3-dB bandwidth is optimized based on specific application requirements.

For DC signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurate settling of the ADC inputs during the small acquisition time window.

For AC signals, keeping the filter bandwidth low is desirable to band-limit the noise fed into the input of the ADC, thereby increasing the system SNR. Besides filtering the noise from the front-end drive circuitry, the filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, C_{FLT}, is connected from each input pin of the ADC to the ground (as shown in Equation 1 and Figure 3).

This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. Generally, the value of this capacitor must be at least 15-20 times the specified sampling capacitor capacitance of the ADC. For example, TI's ADS8910B 18-bit SAR converter specification recommends keeping C_{FLT} greater than 900 pF. However, the THD performance of the ADC driver amplifier typically degrades with high capacitive loads. Higher values of C_{FLT} also degrade the driver phase margin; therefore, TI recommends to select the minimum required value of C_{FLT} and still maintain a good ratio between C_{FLT} and the ADC input sampling capacitance. A 1000-pF capacitor has been used in this design. The capacitor must be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

$$f_{-3dB} = \frac{1}{2\pi \times R_{FLT} \times C_{FLT}} \quad (1)$$

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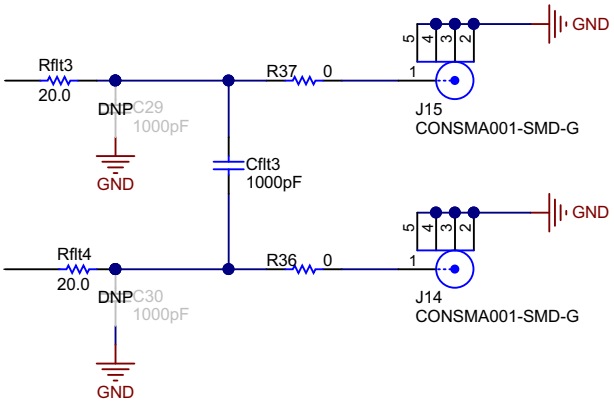

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Figure 3. Antialiasing Filter Configuration Diagram Schematic

Note that driving capacitive loads can degrade the phase margin of their driving amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT} or R_{ISO}) are used at the amplifier outputs. The resistor value is extremely important for many system parameters and these R-C tradeoffs are discussed in the TIPD115 reference design in detail. A higher R_{FLT} value is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear ADC input impedance. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion. For the ADS8910B, limiting the value of R_{FLT} to a maximum of 20 Ω is recommended to avoid any significant degradation in linearity performance. The tolerance of the selected resistors must be kept less than 1% to keep the inputs balanced. The driver amplifier must be selected such that its closed-loop output impedance is at least five times lesser than the R_{FLT}.

The following subsections highlight the design optimization process and ADC driver selection, including comparing fully differential amplifiers (FDA) to operational amplifiers (OPA)

2.2.1 THS4551 Driver

The THS4551 is a fully differential amplifier specifically designed to be used with high performance SAR and ΔΣ ADCs. The TIDA-01053 uses the amplifier in its unity gain configuration and the isolation resistor of the ADC driver filter, R_{FLT}, is selected to be 20 Ω and the C_{FLT} capacitor is selected to be 1000 pF. For more examples of how the THS4551 is used in DAQ systems, refer to the TIDA-01050, TIDA-01051, and TIDA-01052 reference designs where it is used to drive the ADS8910B 18-bit SAR ADC. Refer to the TIDA-01050 reference design to read more about the selection of passive components around the THS4551.

The schematic in Figure 4 shows that the power down pin (pin 12) of the THS4551 is connected to 5 V. The power down pin is logic low, which means that when it is grounded the chip is in power off mode. The chip is in normal operation mode when this pin is high. The amplifier always remains in normal operation mode for this application. Pin 17 is the thermal pad and is connected to ground to ensure that the chip has a proper heat sink. The voltage driven at the common-mode voltage pin is 2.5 V.

TINA-TI was used to verify the stability of this circuit. Figure 5 shows the schematic. When measuring the stability of an amplifier, it is important to look at the closed-loop noise gain, loaded open-loop gain, and loop gain. The phase margin of the circuit must also be sufficient for circuit stability and the required settling. Refer to TI's Precision Labs for more op amp design and stability information.

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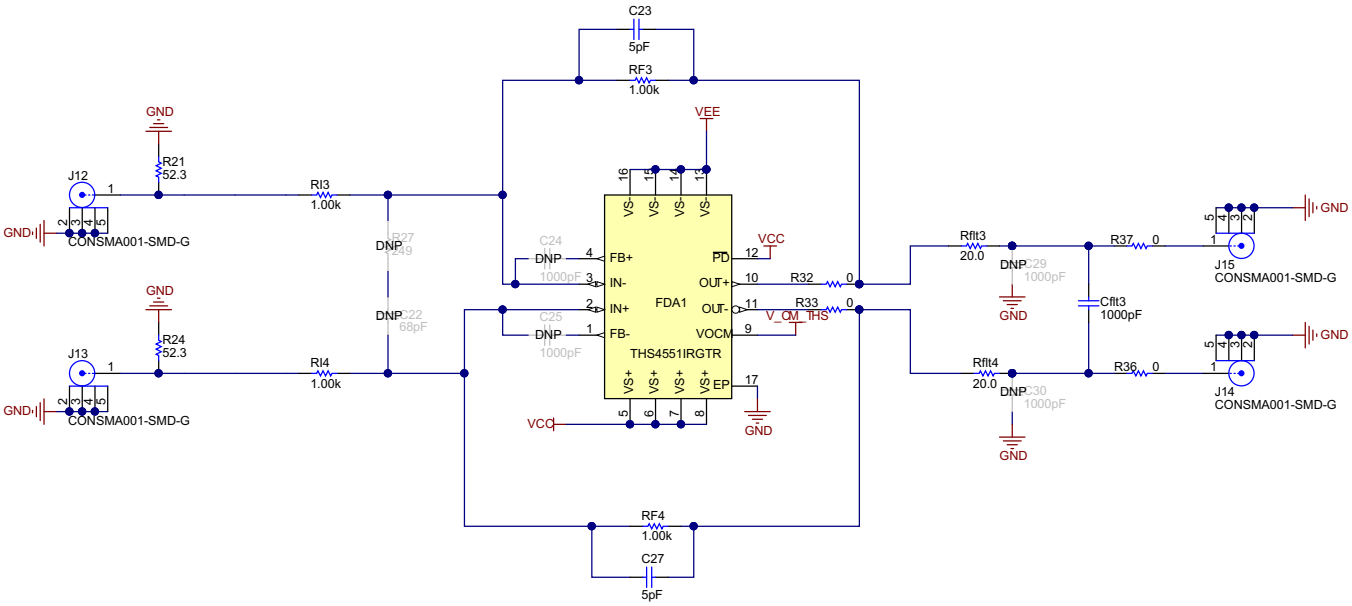

Figure 4. THS4551 Stage Altium Schematic

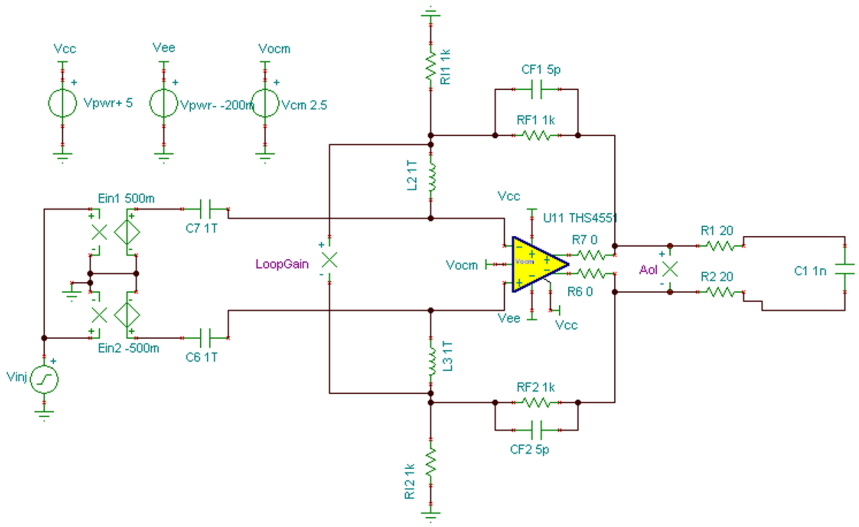

Figure 5. THS4551 Stage TINA-TI Stability Schematic

The TINA-TI schematic in Figure 5 features a 1TF capacitor and 1TH inductor for simulation purposes. These components are used to break the feedback loop because the capacitor is an open at DC while the inductor is a short. At high frequencies, the inductor is an open and the capacitor is a short. The next stage load that the THS4551 must drive is also added (R1, R2, and C1) to properly simulate the stability of the loaded circuit.

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Figure 6 shows the THS4551 stability simulation results demonstrating 44.85º of phase margin.

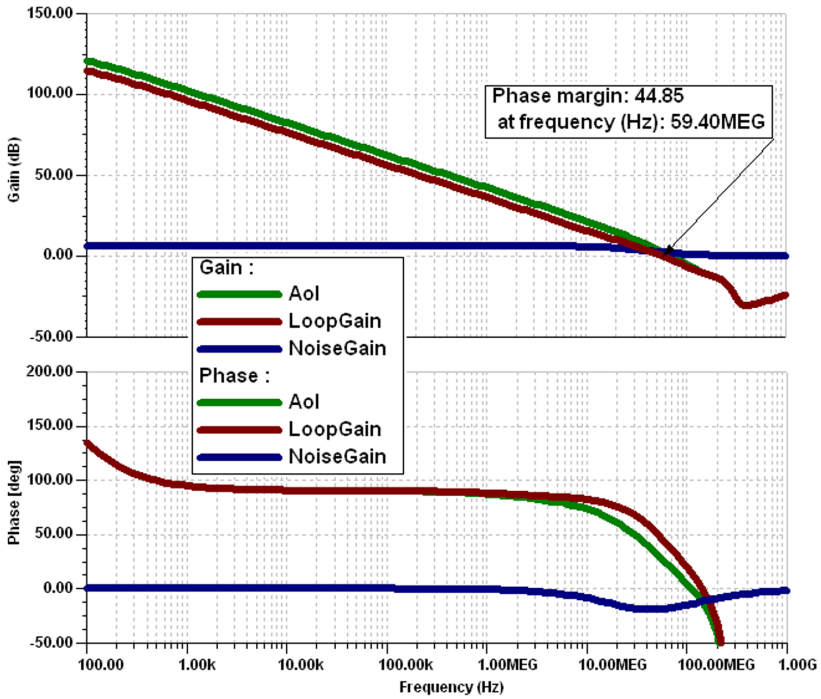

Figure 6. THS4551 TINA-TI™ Stability Simulation Results

To further confirm the driver functionality, transient simulations have been performed to ensure an appropriate response. Figure 7 shows the TINA-TI schematic to simulate the transient response of the THS4551 as an ADC driver. When simulating amplifier transient response, output settling behavior is observed when the input is sharply changed. In this example, a 500-mV amplitude, 50-kHz square wave is applied to the input and the output response is observed over a 100-µS period.

Figure 8 shows the results of the transient simulation. The output of the THS4551 driver shows no ringing and only a slight slew limitation at the beginning and the end of each rising and falling edge. From these results, the designer can conclude that the THS4551 driver is stable and performs as expected.

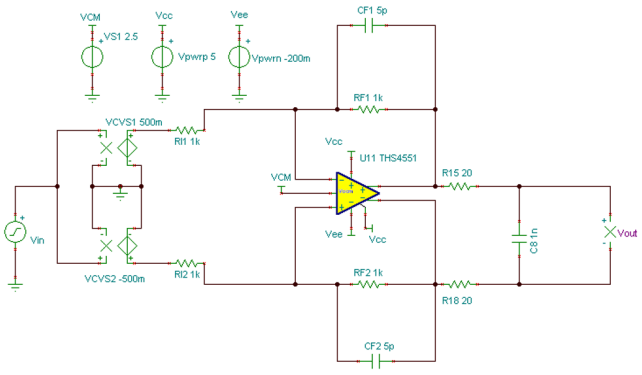

Figure 7. THS4551 TINA-TI™ Transient Schematic

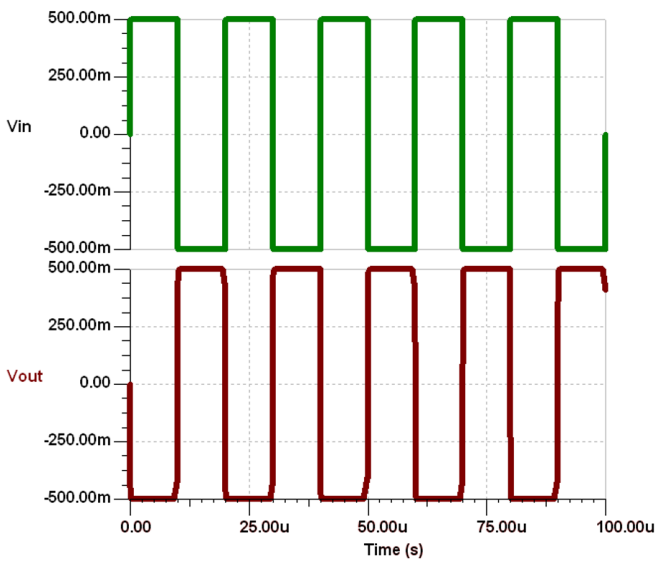

Figure 8. THS4551 TINA-TI™ Transient Results

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2.2.2 Dual OPA625 Driver

Two TI OPA625 operation amplifiers are configured as a fully differential ADC driver. As Figure 9 shows, the non-inverting inputs of the amplifiers are shorted to the common-mode voltage. The gain of this configuration is also set to "1" to highlight the performance of the component. The OPA625 power down pin, pin 5, is connected to VEE. For this application, the amplifier always remains in normal operation mode. Refer to TIDA-01050 to learn about the selection of the passive components.

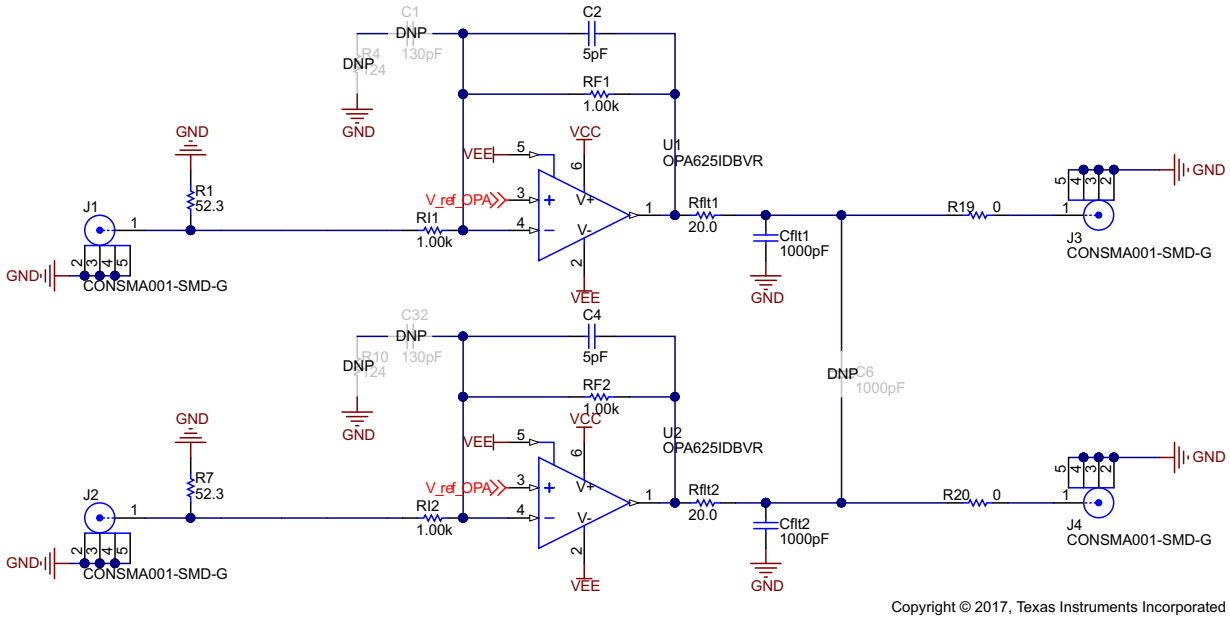

Figure 9. Dual OPA625 Stage Altium Schematic

TINA-TI has been used to verify the circuit stability and the schematic is shown in Figure 10. When measuring amplifier stability, it is important to look at the closed-loop noise gain, loaded open-loop gain, and loop gain. The circuit phase margin must also be sufficient for circuit stability and the required settling. Refer to TI's Precision Labs for more details on op amp design and amplifier stability.

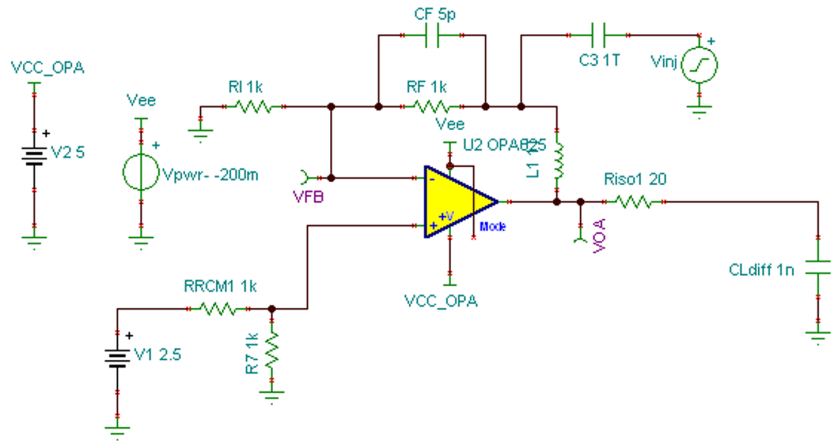

Figure 10. OPA625 Stage TINA-TI™ Stability Schematic

As with the FDA configuration, a 1TF capacitor and 1TH inductor are used for the TINA-TI schematic in Figure 10 for simulation purposes. This configuration is used to break the feedback loop as the capacitor is an open at DC while the inductor is a short. At high frequencies, the inductor is an open and the capacitor is a short. The next stage load that the OPA625 must drive is also added (Rios and CLdiff) to properly simulate the stability of the loaded circuit.

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Figure 11 highlights the stability simulation results from the OPA625 ADC driver configuration resulting in 66.38º of phase margin. Refer to TI's Precision Labs for more information about amplifier stability.

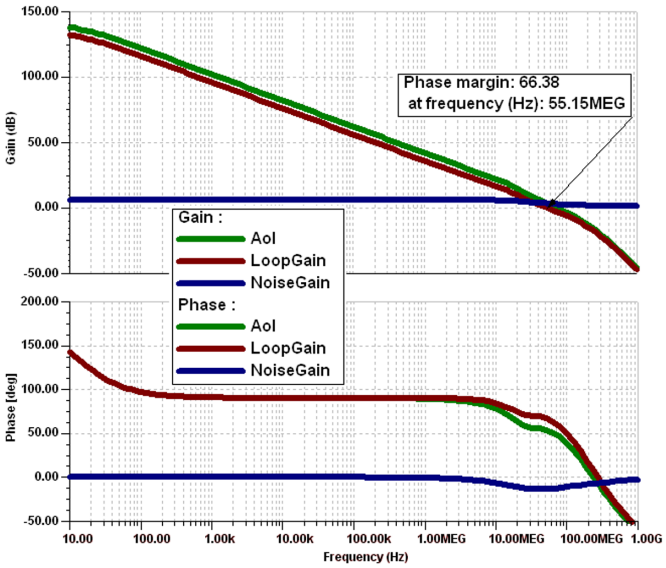

Figure 11. OPA625 TINA-TI™ Stability Simulation Results

To further confirm the functionality of the dual OPA625 ADC driver stage, transient simulations have been performed to ensure an appropriate response. Figure 12 shows the TINA-TI schematic used to simulate the transient response. When simulating an amplifier transient response, output settling behavior is observed when the input is sharply changed. In this example, a 500-mV amplitude, 50-kHz square wave is applied to the input and the output response is observed over a 100-µS period.

Figure 13 shows the results of the transient simulation. The OPA625 output driver shows no ringing and only a slight slew limitation at the beginning and end of each rising and falling edge. From these results, the designer can conclude that the OPA625 driver is stable and performs as expected.

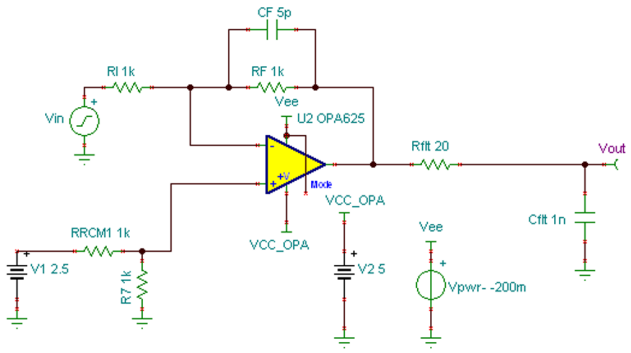

Figure 12. OPA625 TINA-TI™ Transient Schematic

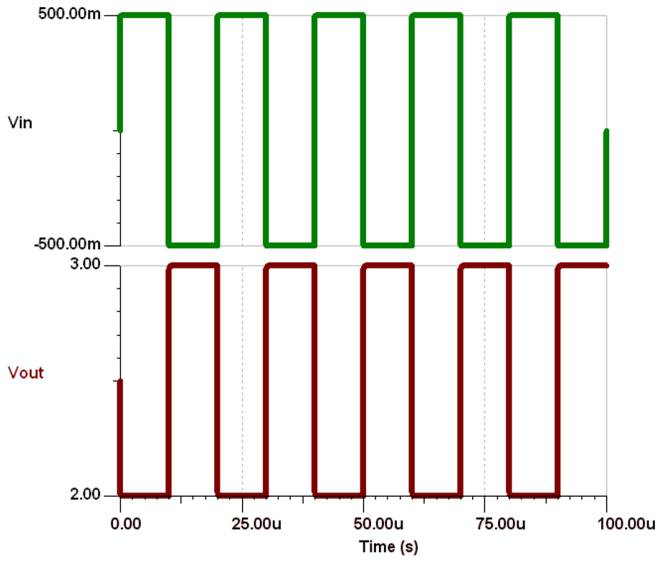

Figure 13. OPA625 TINA-TI™ Transient Results

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2.2.3 Common-Mode Generation

VCC and VEE for both amplifiers are both supplied externally. A high-quality power supply is used to provide 5.2 V and –0.2 V for VCC and VEE, respectively. The negative 200-mV supply is used to ensure true rail-to-rail swing. In practice, such a supply is easily realized using TI's LM7705 LM7705 as described in TIDA-01052. The input common-mode voltage is designed to be 2.5 V, which is exactly half of the expected ADC full-scale reference voltage. The high precision TI REF6050 voltage reference, which is commonly used for high-performance AFEs, is used to generate a stable 5.0-V reference voltage for an ADC. This reference outputs 5.0 V, which means VCC must be 5.2 V. The REF6050 output voltage is divided in half using a resistor divider (R44 and R45) and an OPA376 as the common-mode buffer, as Figure 14 shows. The buffered output at the "V_CM_THS" node then directly goes to pin 9 on the THS4551 FDA. By dividing the reference common-mode by 2, the system supports a 5-V_{pk-pk} output swing.

As Figure 14 shows, the REF6050 is used to generate a very stable 5.0-V reference voltage. The output of the REF6050 then gets divided by R44 and R45 before that voltage is buffered by the OPA376.

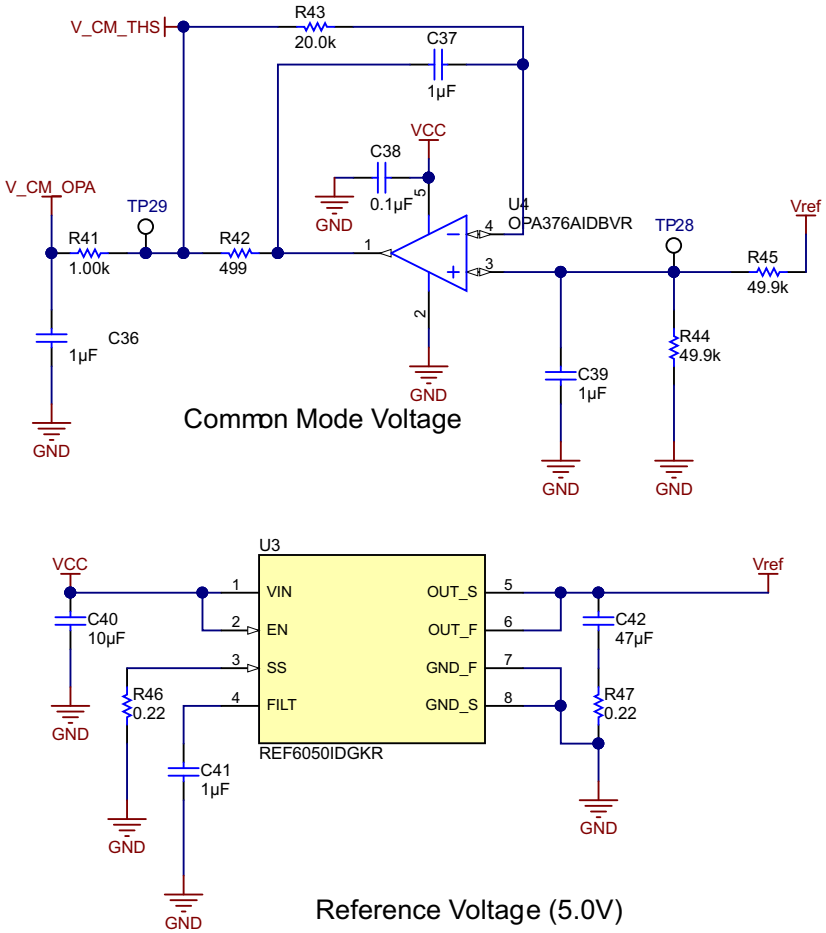

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Figure 14. OPA and THS Common-Mode Generation

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Because the OPA non-inverting input to output gain is $1+\frac{R_f}{R_g}$, its common-mode voltage must further be scaled by $\frac{R_g}{R_f+R_g}$ utilizing another resistor divider (R39 and R41), as Figure 15 shows. Therefore, the OPA common-mode is ½ of the reference voltage, or 1.25 V in this design.

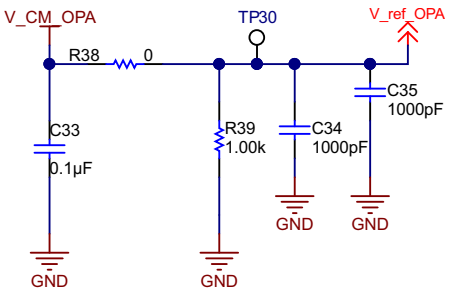

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Figure 15. OPA625 Common-Mode Division

2.2.4 Driver Amplifier Comparison

The ADC driver noise must be minimized, which is crucial for the best performance. Any electronic noise added to the analog signal also becomes digitized, which results in poor data integrity. When comparing the performance of the dual OPA625 driver and the single THS4551 FDA driver, selection of the best driver depends specifically on the final end-use application.

The use of a single FDA has inherent noise advantages simply because more electronics are required for the dual OPA625 architecture. In general, the total output noise is to be $\sqrt{2}$ larger than a single OPA625. The noise levels of both front ends are first compared using TINA-TI to simulate and compare their results. The simulation schematics used to compare the noise performance for both architectures are shown in Figure 16 and Figure 17.

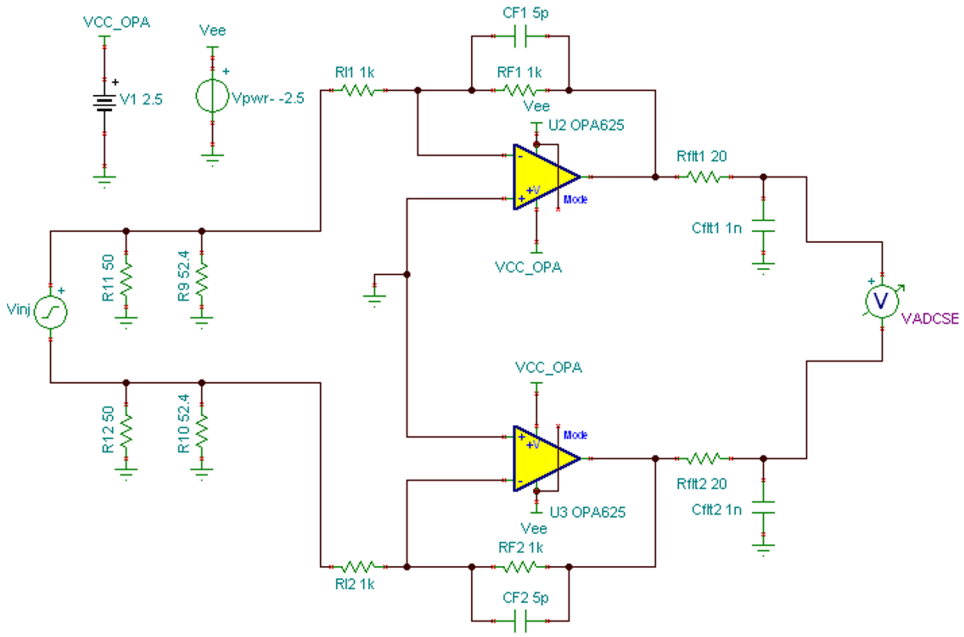

Figure 16. OPA625 TINA-TI™ Schematic for Noise Simulations

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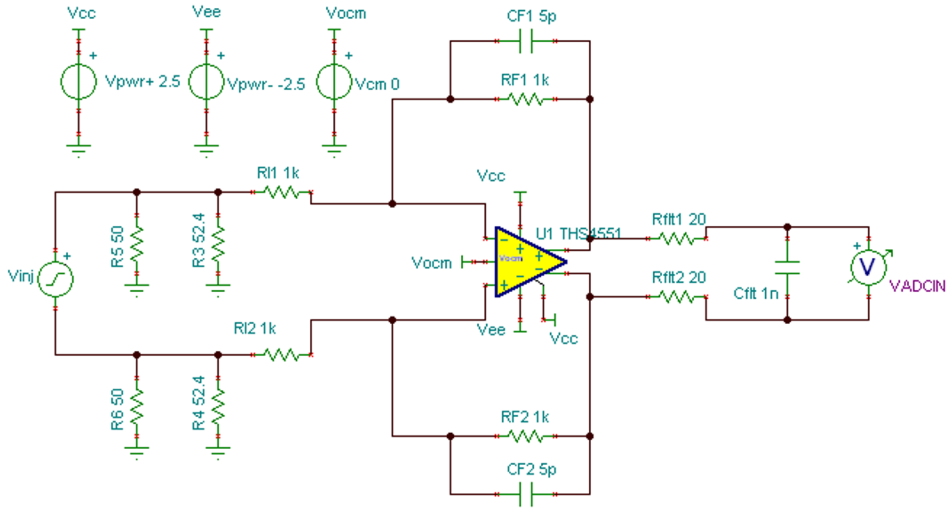

Figure 17. THS4551 TINA-TI™ Schematic for Noise Simulations

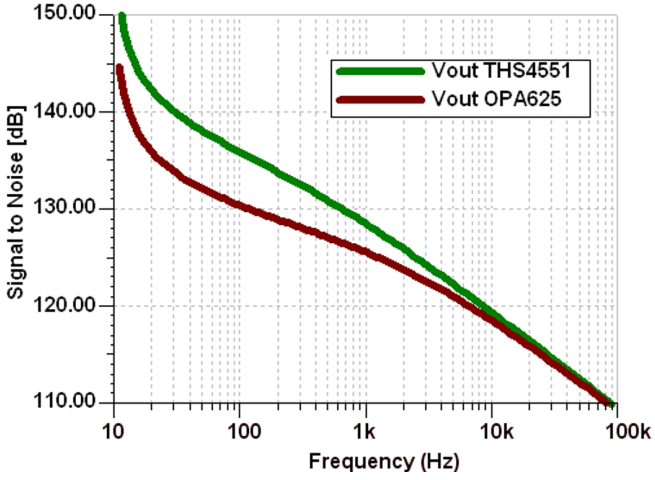

Figure 18. SNR Simulation

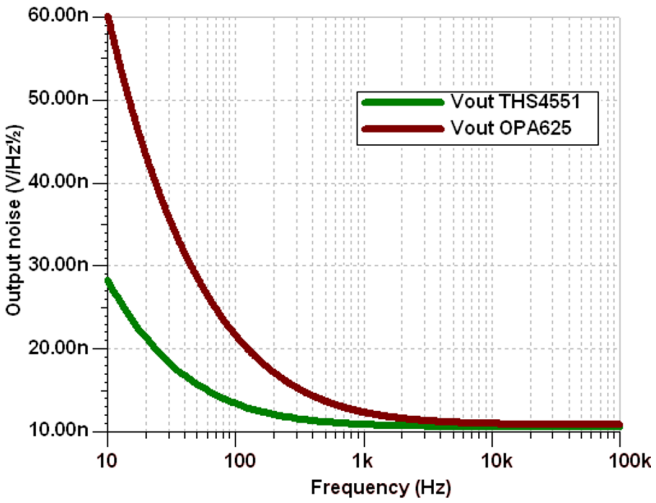

Figure 19. Output Noise Comparison

As the TINA-TI simulations show, output noise and thus the signal-to-noise (SNR) ratio of the FDA architecture gives better results across the whole frequency range. TI's Precision Labs covers amplifier noise in great detail and is highly recommended for understanding noise theory.

In applications where power consumption is crucial, the THS4551 is most likely to be the preferred device. The quiescent current of the THS4551 is just 1.35 mA, which is considerably lower than the 2 mA required per channel in the OPA625 case. When comparing just the devices, the THS4551 also possesses an advantageous slew rate of 220 V/µs vs. The slew rate is 115V/µs for the OPA625; however, when configured as a differential driver, the OPA625 single-channel slew rate is doubled, which results in a differential signal slew rate of 230V/µs.

When comparing THD values of the two amplifiers, it is important to consider the second-order harmonic distortion because the FDA should grant further benefits. The OPA625 specifies a HD2 value of 122 dBc at 100 kHz while the THS4551 specifies an HD2 value of 128 dBc at 100 kHz and at 2 V_{PP} at the output. THD performance of the amplifier varies with the load. Both datasheets are specifying the THD performance for the resistive load, which is not the case for the ADC driver configuration. The ADC input circuit presents a highly capacitive load to the ADC driver and the THD performance of the driver may be quite different from the numbers specified in the datasheet. Typically, THD degrades as load impedance decreases, which reduces the effectiveness of the ADC driver filter. As described in the TIPD115

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reference design, the minimum required C_{FLT} and the maximum R_{FLT} for a specific ADC can be calculated. The designer can obtain the best ADC performance using a very-low impedance filter: one with high C_{FLT} and Low R_{FLT}; however, this configuration puts increased demands on the ADC driver. Therefore, it is important to balance the filter impedance and amplifier drive capability to preserve THD and system-level SNR. Both architectures, OPA and THS, should be considered because of this balance.

Board space and cost are always a significant system design consideration. The THS4551 and OPA625 devices occupy almost the same board space when using a dual-channel OPA package. However, in this TI Design, two single-channel OPA devices are used to match positive and negative signal parasitics. When using two single-channel devices, board layout routing is more symmetrical, which ensures that both the positive and negative signal traces are of equal length. Therefore, the OPA solution is slightly larger. Note that, despite the signal chain requiring the same number of external resistors and capacitors, this design is not fully optimized as it also includes many 0-Ω jumper resistors and “Do not populate” components.

Figure 20 and Figure 21 highlight the differences in layout between the two amplifier options. As the figures show, the OPA625 configuration uses two single-channel devices to ensure a symmetrical layout. As a result, the THS4551 configuration maintains inherent symmetry and requires less printed-circuit board (PCB) space.

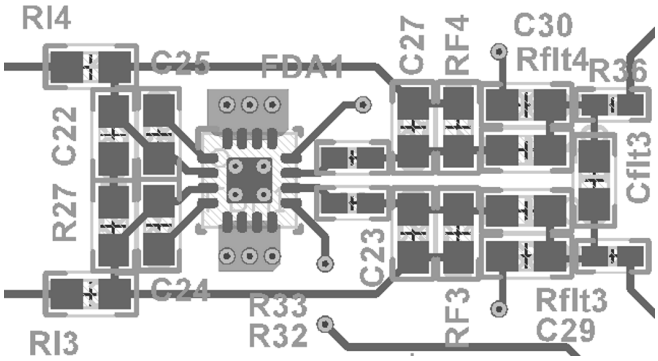

Figure 20. THS4551 Layout

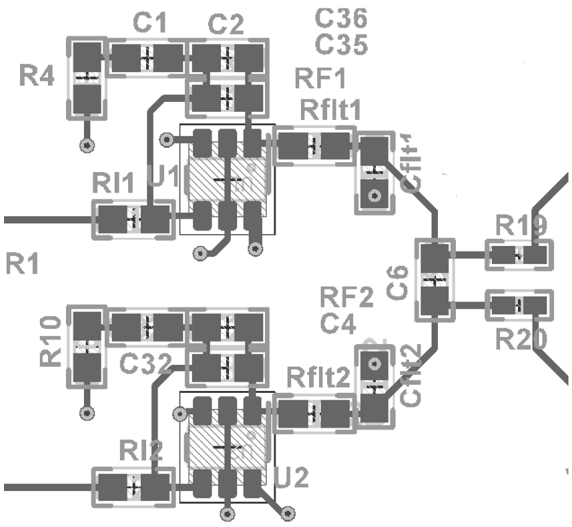

Figure 21. Dual OPA625 Layout

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2.3 Highlighted Products

Key features for selecting the devices for this reference design are highlighted in the following subsections. Find the complete details of the highlighted devices in their respective product datasheets.

2.3.1 OPA625

The OPAx625 family of operational amplifiers are excellent 16-bit and 18-bit, SAR ADC drivers that are high precision with low THD and noise, which allow for a unique power-scalable solution. This family of devices is fully characterized and specified with a 16-bit settling time of 280 ns that enables a true 16-bit effective number of bits (ENOB). Along with a high DC precision of only 100-µV offset voltage, a wide gain-bandwidth product of 120 MHz, and a low wideband noise of 2.5 nV/√Hz, this family is optimized for driving high-throughput, high-resolution SAR ADCs, such as the ADS88xx family of SAR ADCs.

The OPA625 is used in many SAR ADC reference designs. The device is also used in the ADS8910B evaluation model. The OPA625 is often regarded as the best 5-V ADC driver amplifier available today from Texas Instruments.

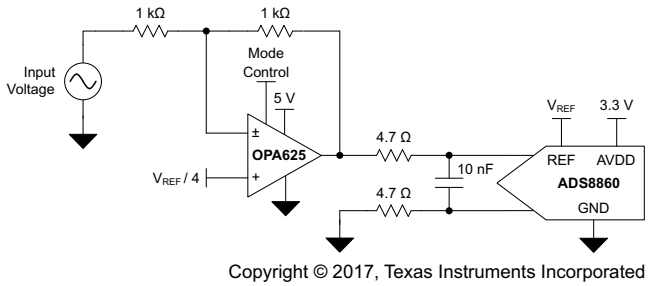

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Figure 22. OPA625 SAR ADC Driver Configuration

2.3.2 THS4551

The THS4551 fully differential amplifier offers an easy interface from single-ended sources to the differential output required by high-precision ADCs. Designed for exceptional DC accuracy, low noise, and robust capacitive load driving, this device is well suited for DAQs where high precision is required along with the best SNR ratio and spurious-free dynamic range (SFDR) through the amplifier and ADC combination.

The THS4551 features the negative rail input required when interfacing a DC-coupled, ground-centered, source signal to a single-supply differential input ADC. Very low DC error and drift terms support the emerging 16- to 20-bit SAR input requirements. A wide-range output common-mode control supports the ADC running from 1.8-V to 5-V supplies with ADC common-mode input requirements from 0.7 V to greater than 3.0 V.

The THS4551 is commonly used in SAR ADC driver circuits; however, it is unclear where using a fully differential amplifier is beneficial over using two precision op amps and vice versa. This design aims to clear up that uncertainty and distinguish benefits to using both configurations.

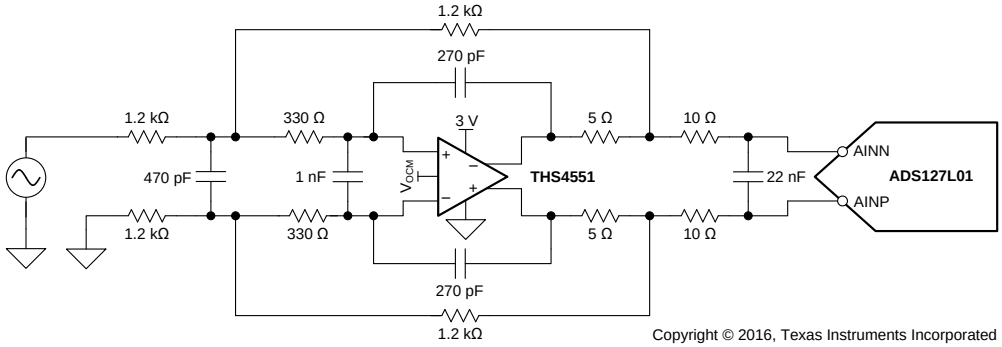

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Figure 23. THS4551 SAR ADC Driver Configuration

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2.3.3 REF6050

The REF6000 family of voltage references have an integrated, low-output impedance buffer that enable the user to directly drive the REF pin of precision data converters while preserving linearity, distortion, and noise performance. Most precision SAR and ΔΣ ADCs switch binary-weighted capacitors onto the REF pin during the conversion process. To support this dynamic load, the output of the voltage reference must be buffered with a low-output impedance (high-bandwidth) buffer. The REF6000 family devices are well suited (but not limited) to drive the REF pin of the ADS88xx family of SAR ADCs, the ADS127xx family of ΔΣ ADCs, as well as other digital-to-analog converters (DACs).

The REF6000 family of voltage references are able to maintain an output voltage within 1LSB (18 bit) with minimal droop, even during the first conversion while driving the REF pin of the ADS8881 device. This feature is useful in burst-mode, event-triggered, equivalent-time sampling, and variable-sampling-rate DAQ systems. The REF60xx variants of the REF6000 family specify a maximum temperature drift of just 5 ppm/°C and an initial accuracy of 0.05% for both the voltage reference and the low-output impedance buffer combined.

A 5-V reference voltage is required to generate the common-mode voltages of this design. The REF6050 also contains an internal buffer enabling multiple ADCs to be driven in parallel.

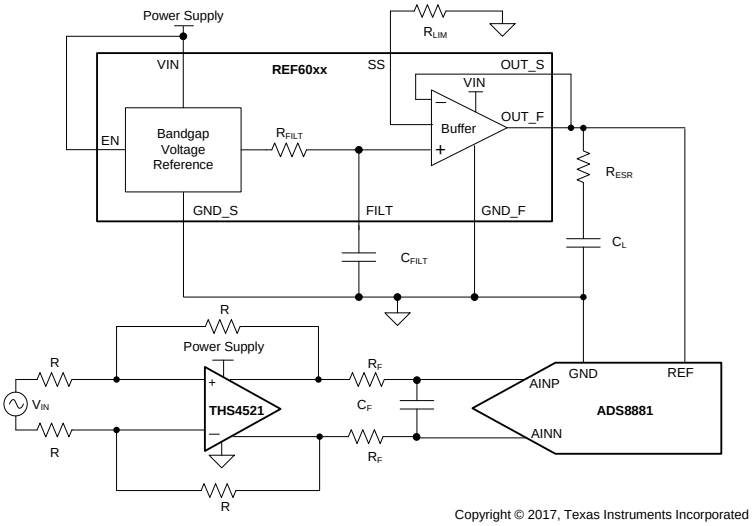

Figure 24. REF6050 Typical Application Circuit

2.3.4 OPA376

The OPA376 family represents a new generation of low-noise operational amplifiers with e-trim™ integrated circuits, offering outstanding DC precision and AC performance. Rail-to-rail input and output, low offset (25 µV, maximum), low noise (7.5 nV/√Hz), quiescent current of 950 µA (maximum), and a 5.5-MHz bandwidth make this part very attractive for a variety of precision and portable applications. In addition, this device has a reasonably wide supply range with excellent power supply rejection ratio (PSRR), which makes it an attractive selection for applications that run directly from batteries without regulation.

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3 Getting Started Hardware

The ensuing section outlines the TIDA-01053 test setup and different measurement configurations. Care should be taken when handling the device under test, equipment and moving jumper pins to avoid possible damage to the components.

3.1 Measuring Performance

To ensure predictable and accurate measurements, a differential high-quality signal generator is required; if not, results are limited by the signal source. The Audio Precision AP-2700 series was selected as the input source. Using SMA cables, attach the signal from the generator to one of the data channels (either the single-ended or fully differential front end).

Likewise, a high-quality spectrum analyzer is required to adequately measure the noise spectrum and distortion characteristics. The HP 3589A Spectrum/Network Analyzer was selected for this task and used by attaching SMA cables to the output connectors on the board. Use the correct high-quality analysis equipment for recording results.

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4 Testing and Results

Figure 25 shows the measured noise performance of both drive configurations.

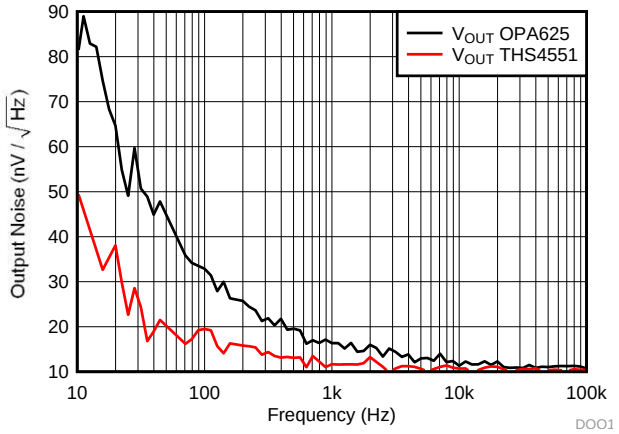

Figure 25. THS4551 versus Dual OPA625 Driver Measured Noise Performance

Several observations can be made when comparing the measured results from Figure 25 to the simulated results shown in Figure 19. Even though the "flat-band" noise performance of both driver configurations correlates fairly well with the simulations, the measured 1/f noise performance is slightly worse compared to simulations. This result can be explained by the inaccuracies of the measurement setup and part-to-part variations. However, the trends and conclusions shown in the simulated results are still confirmed in the measurements. The dual OPA625 configuration has slightly worse noise performance compared to the THS4551 configuration.

The THS4551 ADC driver distortion measured results are shown in Figure 27 and compared to the datasheet shown in Figure 26.

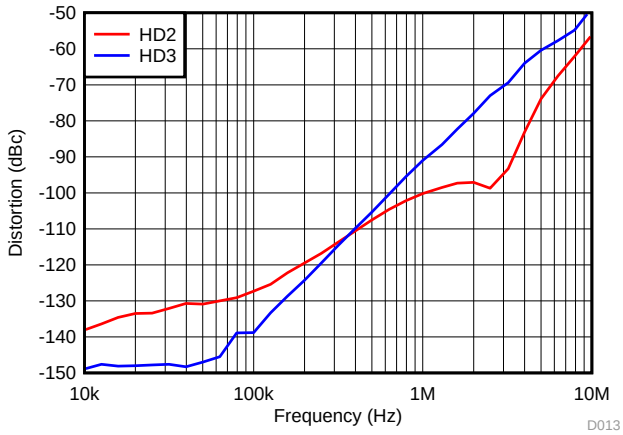

Figure 26. Harmonic Distortion versus Frequency

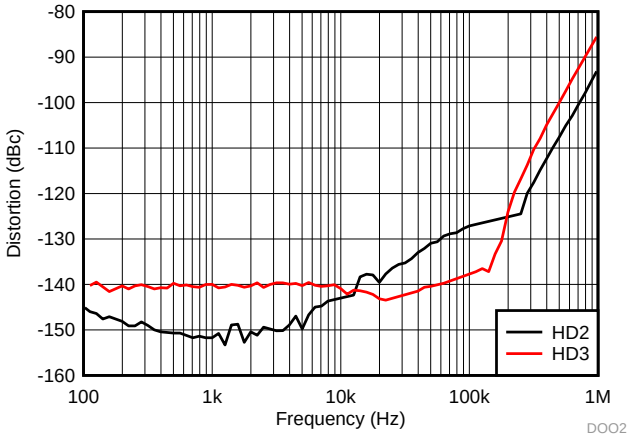

Figure 27. THS4551 ADC Driver

$G = 1\ V/V,\ V_{OUT} = 2\ V_{PP}$

$G = 1\ V/V,\ V_{OUT} = 4\ V_{PP}$

Even though the conditions for the ADC driver configuration measurement are somewhat different compared to the datasheet configuration, the similar distortion trends are observable. The two main differences are the output voltage amplitude, which is 4 V_{PP} for the ADC driver configuration compared to 2 V_{PP} in the datasheet. The second difference is the load, which is a 1-kΩ resistor in the datasheet compared to two 20-Ω resistors in series with a 1-nF capacitor. In both cases, the distortion performance starts do degrade at the relatively-low frequencies compared to the bandwidth of the part in the same configuration. The THD performance is expected to degrade with the larger output voltage and high

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capacitive load, which can be seen in Figure 27. And while the impact of the high capacitive load is pretty significant at higher frequencies the effect at lower frequencies is minimal where the good performance could be achieved if the load capacitor value is kept at the minimum required for the proper ADC operation. Many modern SAR ADCs are able to achieve the THD performance up to –130 dBc. If the goal for the driver design is to provide the performance that is similar or better compared to the ADC performance, then Figure 27 shows that the THS4551 configuration is capable of driving the signals up to approximately 60 kHz.

The dual OPA625 ADC driver distortion measured results are shown in Figure 29 and compared to the datasheet shown in Figure 28.

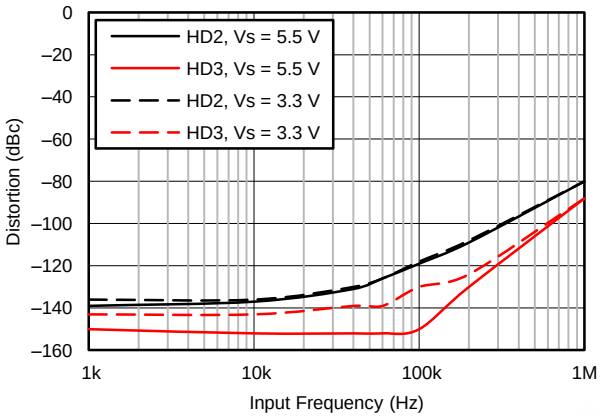

Figure 28. Distortion versus Frequency for Various Power Supplies

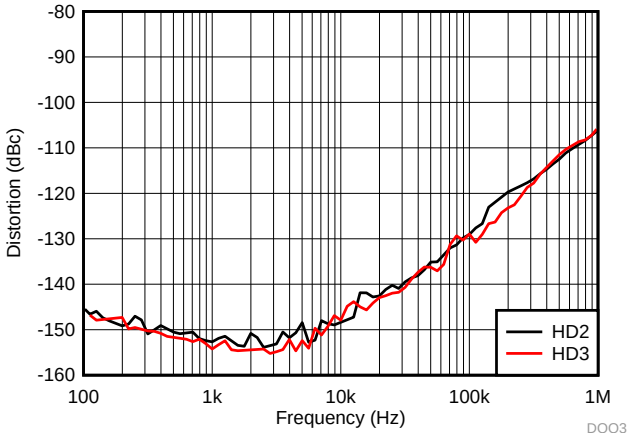

Figure 29. Dual OPA625 ADC Driver

$G = 1\ V/V,\ V_{OUT} = 2\ V_{PP},\ R_{LOAD} = 600\ \Omega$ $G = 1\ V/V,\ V_{OUT} = 4\ V_{PP}$

In this case, the 4-V_{PP} differential output signal amplitude of the dual OPA625 ADC driver configuration is the same as the 2-V_{PP} signal amplitude that is specified for the single OPA625 in the datasheet. The main differences in the measurement configuration derive from the load and the fact that two OPA625 parts are configured to generate a differential signal at the output. A 600-Ω load was used in the datasheet configuration as compared to the 20-Ω resistor in series with a 1-nF capacitor from each output of the dual OPA625 configuration. As with the THS4551 configuration, the good THD performance can be achieved at the lower frequencies if the load capacitor value is kept at the minimum required for proper ADC operation. The additional advantage of this configuration is the improvements in HD2 performance of the dual ADC drive configuration as compared to the value provided in the datasheet for the single part. As Figure 29 shows, HD2 performance of the dual OPA625 configuration almost matches HD3 performance, which is not the case for the single OPA625 configuration from the datasheet shown in Figure 28. In this case, the dual OPA625 configuration provides similar advantages in HD2 performance as the fully differential amplifier. Dual OPA625 configuration is designed to generate a differential signal at the output. If both OPA625 parts have similar asymmetric nonlinearities that create even harmonics, all of them are cancelled out in the dual OPA625 differential configuration. Similar to the THS4551 configuration, the dual OPA625 configuration is capable of driving the signals up to approximately 70 kHz.

In conclusion, many different performance characteristics and design tradeoffs must be taken into account when designing the ADC drivers. Noise and THD are just two key components that affect the design optimization. As this reference guide explains, noise optimization is somewhat easier because it can be simulated with relative accuracy using TINA-TI. Alternatively, the distortion performance is somewhat more difficult to optimize due to model and simulation limitations. Designers must understand the tradeoffs between ADC driver and filter design and how the optimization of each can impact system-level SNR. This reference guide outlines these considerations using two different ADC driver architectures. Primarily, it is important to keep the value of the load capacitor as low as possible while still matching the ADC requirements as described in TIPD115. Another recommendation is to keep the isolation resistor value as close to the maximum allowable value as possible, as this improves the stability of the circuit impacted by the filter capacitor.

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This reference design also shows that, even though the distortion performance of the ADC driver circuit is degraded as compared to the performance provided in the datasheet for a resistive load, it is still possible to use the data from the datasheet and approximate the performance of the driver circuit given that the filter capacitor value is kept close to its minimum required value and the isolation resistor value is close to the maximum allowable value. Moreover, in the case of the dual OPA625 driver, the HD2 performance at lower frequencies is expected to be as good or better as compared to the datasheet due to the differential nature of the ADC driver design.

In case of both driver configurations, distortion performance decreases rapidly at higher frequencies due to a decreased driver amplifier loop gain and decreased effective load impedance. High-speed amplifiers must be used in the driver circuit to provide the adequate levels of THD performance. As this reference design shows, the THS4551 driver configuration is capable of driving the output signals up to 60 kHz while the dual OPA625 configuration is capable of driving the output signals up to 70 kHz. The tradeoffs and design considerations between the two configurations are likely to be dominated by power and board space.

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5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01053.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01053.

5.3 PCB Layout Recommendations

This design is very sensitive to layout. Maintaining the differential input signal traces to the same length to negate any potential propagation loss on these lines is important. Any mismatch between the positive and negative traces in length or parasitic resistances and capacitances to other signals causes an unbalance in the signal path, which results in THD degradation.

Figure 30 highlights the layout for TIDA-01053. The brownish-colored layer is the ground plane. The signal path of the differential inputs is matched as much as possible.

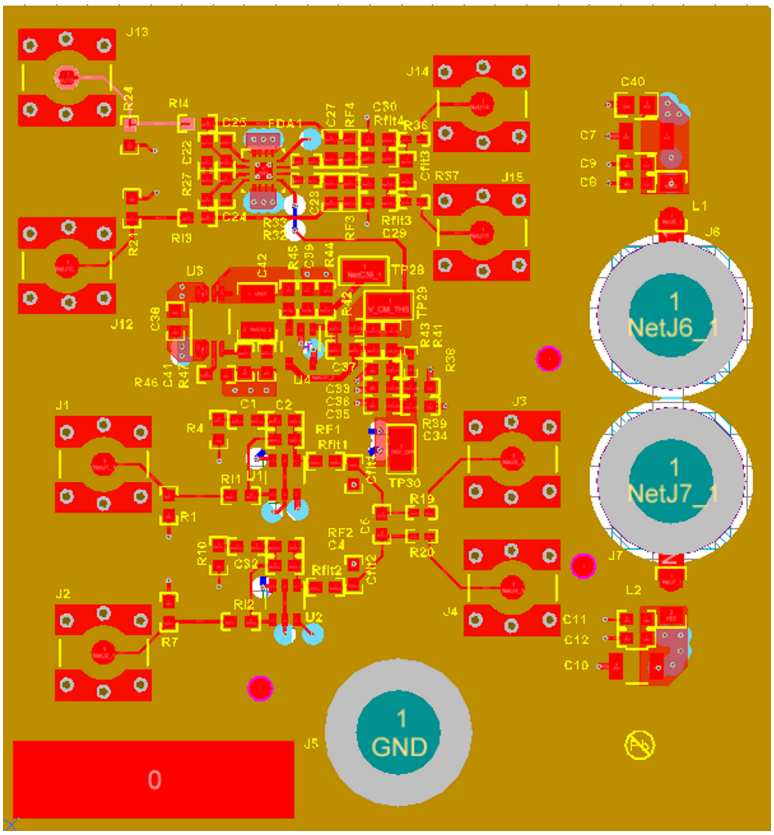

Figure 30. Layout Preview

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01053.

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5.4 Altium Project

To download the Altium project files, see the design files at TIDA-01053.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01053.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01053.

6 Related Documentation

1. Texas Instruments, *Noise Analysis in Operational Amplifier Circuits*, Application Report (SLVA043)
2. Texas Instruments, *Op Amp Noise Theory and Applications*, Application Report (SLOA082)

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