Design Guide: TIDA-010234

Eight Port IO-Link Master Reference Design

Description

This design implements an IO-Link Master with fast and deterministic timing with eight ports. Each port can be operated with independed bit rate and cycle timing. This design can be used to build a remote IO gateway to connect to OPC UA, Profinet, EtherCAT, or Ethernet IP. A PRU based frame handler provides a flexible way to of timing and synchronization.

Resources

TIDA-010234	Design Folder
LP-AM243	Tool Folder
BOOSTXL-IOLINKM-8	Tool Folder
AM243	Product Folder
TIOL112	Product Folder
TPS274160	Product Folder

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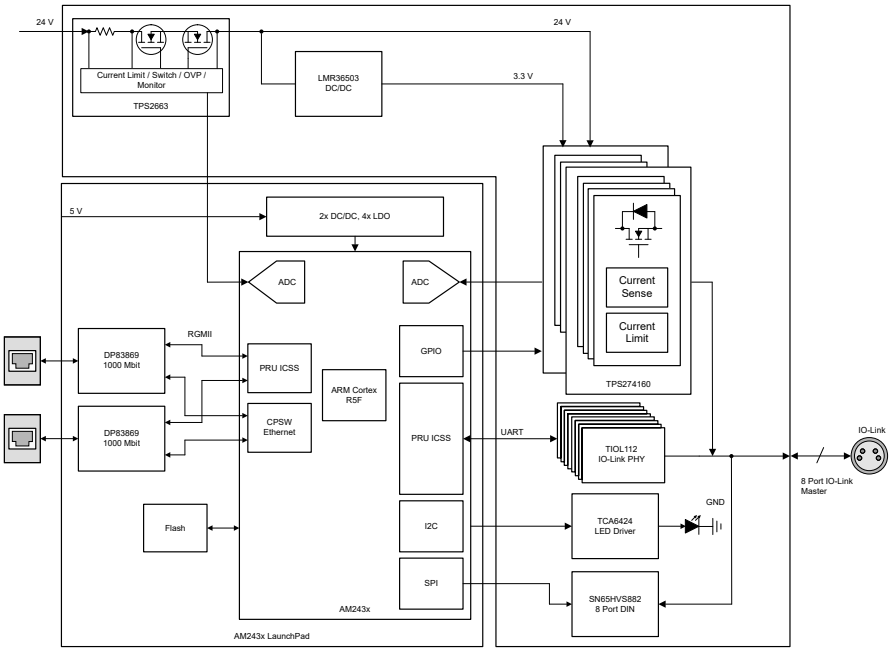
Features

- Eight IO-Link ports
- Supports IO-Link transmission rates COM1, COM2, COM3
- Supports 400-µs cycle time
- 500-mA current per port
- All ports feature overcurrent protection and limiting
- PRU frame handler enables flexible timing

Applications

- Stand-alone remote IO
- Communication module



1 System Description

Sensors and actuators are the most basic units of automation, feeding information into and acting on instructions from networked systems. Traditionally, these devices connect to control units through interfaces that provide little intelligence, and thus exchange little or no configuration and diagnostic information. Installing a new device requires configuration by hand at the point of use, and without diagnostics it is impossible to perform just-in-time preventive maintenance.

IO-Link (International Electrotechnical Commission [IEC] 61131-9) is an open standards protocol that addresses the need for intelligent control of small devices such as sensors and actuators. This standard provides low speed point-to-point serial communication between a device and a master that normally serves as a gateway to a field bus and PLC. The intelligent link established enables ease of communication for data exchange, configuration, and diagnostics.

An unshielded three-wire cable as long as 20 meters, normally equipped with M12 connectors, establishes an IO-Link connection. Data rates range up to 230 kbps with a non-synchronous minimum cycle time of 400 µs, +10%. Four operating modes support bidirectional input/output (I/O), digital input, digital output and deactivation. Security mechanisms and deterministic data delivery are not specified. A profile known as the IO Device Description (IODD) contains communication properties; device parameters; identification, process and diagnostic data; and information specifically about the device and manufacturer.

The many advantages of deploying an IO-Link system include standardized wiring, increased data availability, remote monitoring and configuration, simple replacement of devices and advanced diagnostics. IO-Link permits factory managers to receive sensor updates and plan for upcoming maintenance or replacement. Swapping out a sensing or actuation unit that needs replacement and configuring a new one from the PLC through the IO-Link master eliminates manual setup and reduces downtime. Switching production remotely from one configuration to another without visiting the factory floor facilitates easier product customization. Factories can upgrade production lines readily to IO-Link, since it is backwards-compatible with existing standard I/O installations and cabling. Altogether, these capabilities result in reduced overall costs, more efficient processes, and greater machine availability.

2 System Overview

2.1 Block Diagram

The design consists of two major blocks as it is shown in Figure 2-1.

The first block is the AM243x LaunchPad™, containing the processor, two Ethernet ports as well as the necessary power supply circuitry and flash memory.

The second block is the IO-Link BoosterPack. Here all the analog circuit to build an Io-Link port is included. The main components here are the power supply for each port and the IO-Link transceiver.

The power supply is built with a four port high side switch TPS274160, it offers not only switching power, but also includes a configurable current limit and current monitoring. This helps in case of overloaded outputs due to shorts, defective devices or wiring issues to keep the system running and locate the reason for problems. The power input of the system is protected against over voltage and reverse polarity using a TPS2663 eFuse. This also offers a current monitoring output to observe the total current consumption.

Each of the eight IO-Link ports use the TIOL112 as a transceiver. This devices implements the physical layer and has an integrated current sink on the CQ line as required for an IO-Link Master interface. Also it offers a current limit of about 700 mA, to provide enough current during the wake up pulse, and at the same time limit the current so cables and power supplies are not overloaded in case faults. To minimize overshoots during communication and reduce emissions, the slew rate on the CQ line is limited.

For signaling the port status a simple LED driver with serial interface TCA6424 is added to the board. A SN65HVS883 implements eight digital inputs, one on each of the IO-Link ports.

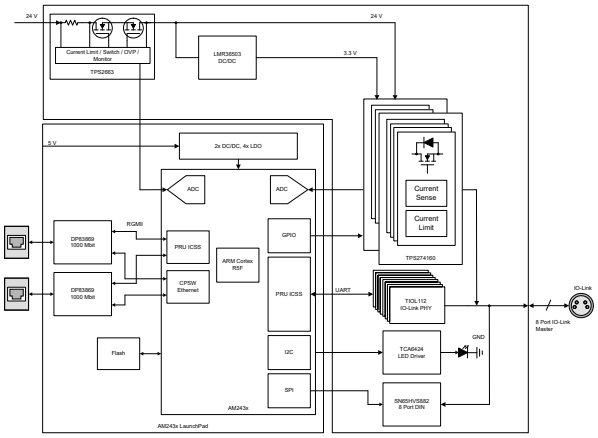


Figure 2-1. TIDA-010234 Block Diagram

2.2 Design Considerations

This reference design implements an IO-Link master using the TIOL112 PHY and surrounding components needed to build a complete IO-Link master design. Therefore, on the physical side in addition to the TIOL112 device, only a power supply for the ports has to be added.

The necessary current sink is already integrated into TIOL112 and automatically activated when using a current limit set resistor below 5 kΩ. The device is in this mode able to directly drive a wake-up pulse. In this mode, the current limit is set to about 700 mA, so enough current to drive a wakeup, but still limited to a safe level, so nothing can be damaged.

On the other side it is necessary to have a hardware as well as frame handler that support all three communication speeds. The TIOL112 device used as PHY here can handle all speeds (COM1, COM2, COM3) the eight port frame handler is implemented in the programmable real-time unit (PRU) of the AM243x.

To realize an eight-port IO-Link capable master gateway, eight TIOL112 devices are necessary. One TPS2724160 supports four IO-Link ports. This results in only eight TIOL112 devices (IO-Link PHY), two TPS2724160 devices (high-side switch), and one TCA6424 device (LED driver).

2.2.1 Framehandler

In Figure 2-2 relation shows how the different cores work together. The complete frame handling is done using one Industrial communication subsystem (ICSS), including the cycle-time generation. The stack itself is implemented in a single Arm® core.

PRU0 implements the framehandler, responsible for sending and receiving frames on all eight ports. After the internal state machine has completed, an interrupt is sent to the second PRU core.

This interrupt is used for generating the cycle timing. PRU1 holds a counting register, and for each port a compare register as well as some status and control bits. Here the cycle time is configured and as soon as it is time for sending the next frame, a trigger is sent to PRU0 to send out a frame.

The Arm core controls both PRUs. During start-up, the cycle timer is not yet used and frames are sent out manually through PRU0 and triggering the Tx from the Arm core. When switching to operational mode and the exchange of process data begins, PRU1 gets configured to the right cycle time and takes over to control the trigger for sending data. The Arm core in this case gets an interrupt after each frame has been sent and the answer from a device is received or a timeout has occurred.

With the scheme, the cycle time is independent from the CPU load on the Arm core. Also the load is reduced as the timing does not need to be generated there.

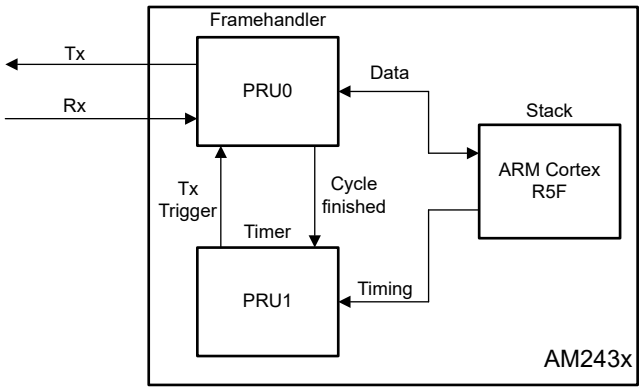


Figure 2-2. Sitara PRU – Arm® Relation

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

3.2 Test Setup

To test the different physical parameters, the IO-Link board, BOOSTXL-IOLINKM-8, is connected to a 24-V supply without the AM243x LaunchPad. The necessary signals for each test are explained in the following sections.

3.3 Test Results

Focus of this section of tests are the physical layer tests as describe by the IO-Link community in *IO-Link Interface and System Specification* publication.

3.3.1 Power Supply Inrush Tests (TCM_PHYL_INTF_ISIRM)

This test case tests the behavior of a master during inrush on the L+ line. A load of at least 1000 mA is to be connected and the charge during inrush has to be observed. For this test a resistive load is used, the current as well as the voltage on the L+ and L- is observed. It is done with PSM = 20 V and PSM = 30 V. The charge going into the load is monitored and must be more or equal to 20 mAs.

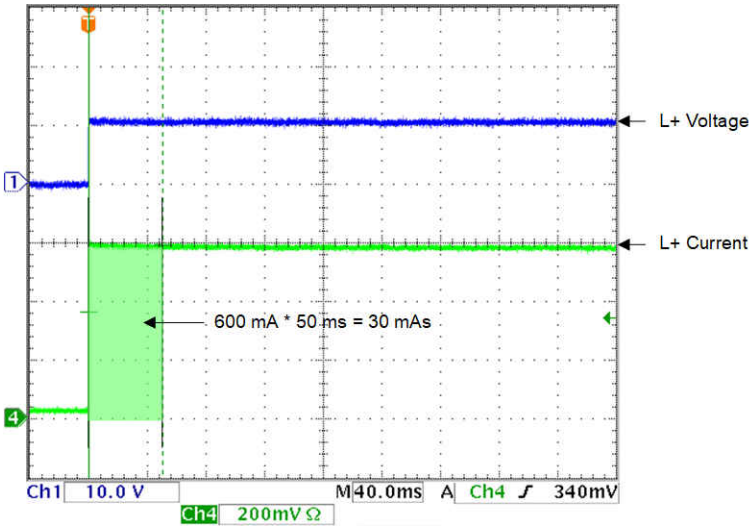


Figure 3-1. TCM_PHYL_INTF_ISIRM with 20 V

Figure 3-1 shows the behavior at a supply voltage of 20 V and a load of about 18 Ω. The current gets limited to 600 mA by the TPS274160 high side switch. Thus the output voltage is limited to 10 V. During the first 50 ms, a charge of 30 mAs is provided by the master.

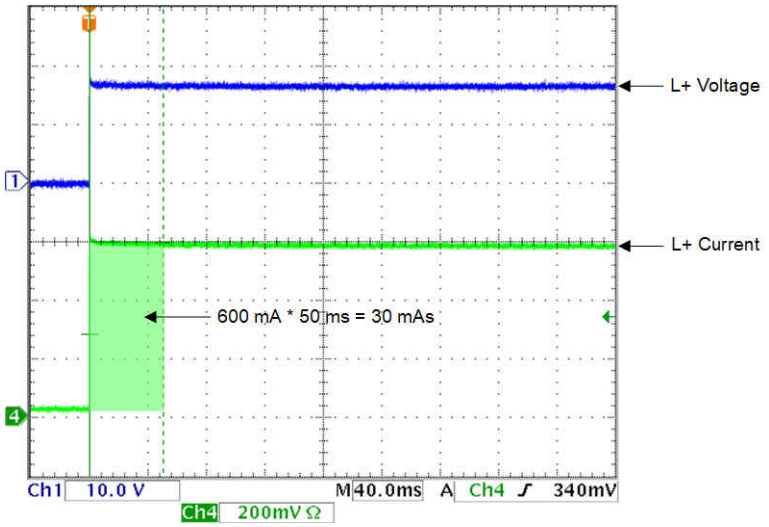


Figure 3-2. TCM_PHYL_INTF_ISIRM with 30 V

Figure 3-2 shows the same test with a supply voltage of 30 V. Therefore a resistive load of 28 Ω is used. The current is still limited to 600 mA, the voltage goes up to about 16 V. Important is the charge in the first 50 ms is here also 30 mAs and fulfills the requirements by the standard.

3.3.2 Interface Wake-Up Voltages (TCM_PHYL_INTF_IQWUH and TCM_PHYL_INTF_IQWUHL)

The next tests verify the behavior of the IO-Link CQ lines driver stage during the generation of a wake-up pulse. The CQ output is loaded with a resistive load resulting in a 500-mA current and the voltage level is observed. The first two tests verify the high-side driver.

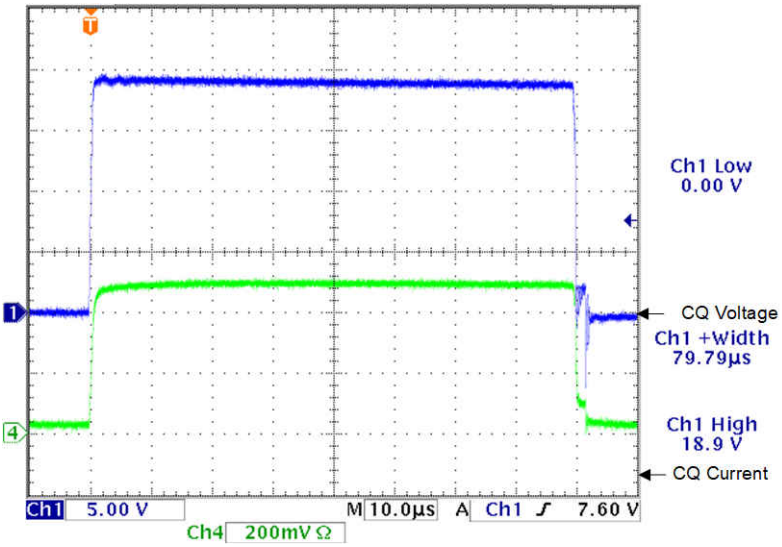


Figure 3-3. TCM_PHYL_INTF_IQWUH With 20 V

The first test is shown in Figure 3-3. Here, the supply voltage is set to 20 V and the line is loaded with 40 Ω, resulting in 500 mA of current. It is observed if the voltage level exceeds VTHHmax which is 13 V. The scope plot shows a measurement of 18.9 V, so this test is passed.

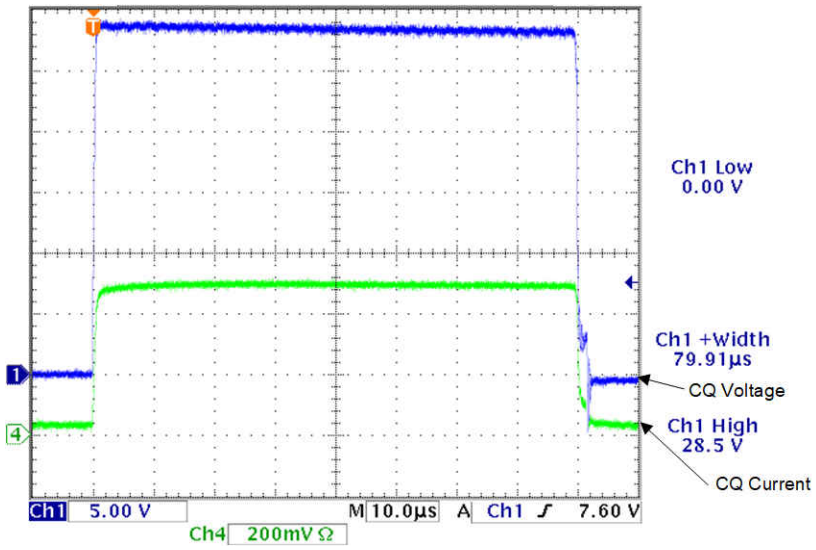


Figure 3-4. TCM_PHYL_INTF_IQWUH With 30 V

Similar measurement has to be done with a supply voltage of 30 V, the scope plot in Figure 3-4 shows this. Here the resistive load has to be changed to 60 Ω, so the resulting current is still 500 mA. A voltage of 28.5 V is measured, so this test is also passed.

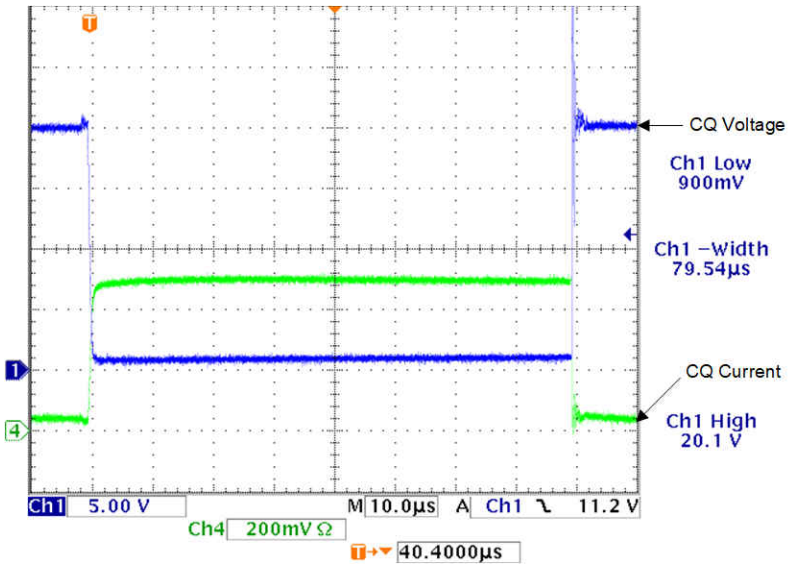


Figure 3-5. TCM_PHYL_INTF_IQWUL With 20 V

The same test is to be done for the low side driver. Figure 3-5 shows the first test with a supply voltage of 20 V. Again the line has to be loaded with a resistive load resulting in 500 mA. In this case, the load is connected to L+. As illustrated, a voltage of 0.9 V is measured, which is a pass for this test.

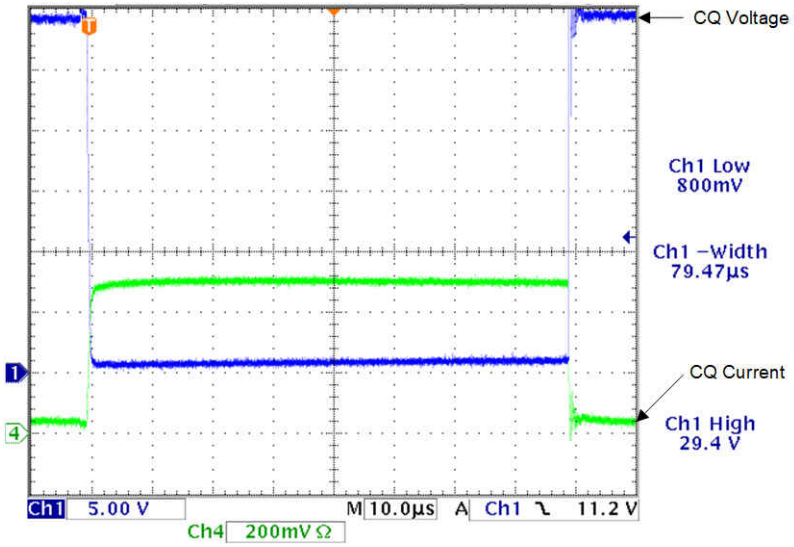


Figure 3-6. TCM_PHYL_INTF_IQWUL With 30 V

The last physical layer test is similar but with 30 V and an equally higher load resistor. The results in Figure 3-6 show again a voltage of 0.9 V. Which is again a pass.

Table 3-1 lists all physical layer tests in summary and the results.

Table 3-1. IO-Link® Physical Layer Test

ID	Name	Configuration	Specification (Clause)	Comment	Result
SDCI_TC_0001	TCM_PHYL_INTF_ISM	The supply current at the Master port is monitored.	See *Section 5.3.2.3*, *Table 6* in *IO-Link Interface and System Specification Version 1.1.3* 4	Test with 500 mA	20 V: Pass 30 V: Pass
SDCI_TC_0002	TCM_PHYL_INTF_ISIRM	The supply current at the Master port is monitored.		Test with 500 mA	20 V: Pass 30 V: Pass
SDCI_TC_0003	TCM_PHYL_INTF_ILLM	The input current at C/Q at the Master port is monitored.			ILLM (VIM = 5 V, VSM = 20 V): 8.56mA Pass ILLM (VIM = 5,1 V, VSM = 20 V): 8.56 mA Pass ILLM (VIM = 15 V, VSM = 20 V): 8.57 mA Pass ILLM (VIM = VSM = 20 V): 8.57 mA Pass ILLM (VIM = 5 V, VSM = 30 V): 8.57 mA Pass ILLM (VIM = 5,1 V, VSM = 30 V): 8.57 mA Pass ILLM (VIM = 15 V, VSM = 30 V): 8.58 mA Pass ILLM (VIM = VSM = 30 V): 8.59 mA Pass
SDCI_TC_0004	TCM_PHYL_INTF_VREShigh	The output level at the Master C/Q output is measured.			VRQHM (VSM = 20 V): 0.23 V VRQHM (VSM = 30 V): 0.228 V Pass
SDCI_TC_0005	TCM_PHYL_INTF_VRESLOW	The output level at the Master C/Q output is measured.			VRQLM (VSM = 20 V): 0.225 V VRQLM (VSM = 30 V): 0.225 V Pass
SDCI_TC_0006	TCM_PHYL_INTF_VTHHM	The digital input signal for C/Q input is monitored	See *Section 5.3.2.2*, *Table 5* in *IO-Link Interface and System Specification Version 1.1.3* 4		VIM@VTHHM (VSM = 20 V): 11.1 V VIM@VTHHM (VSM = 30 V): 11.1 V Pass
SDCI_TC_0007	TCM_PHYL_INTF_VTHLM	The digital input signal for C/Q input is monitored			VIM@VTHLM (VSM = 20 V): 10.35 V VIM@VTHLM (VSM = 30 V): 10.35 V Pass
SDCI_TC_0008	TCM_PHYL_INTF_VHYSM	Comparison of values from SDCI_TC_0006 and SDCI_TC_0007			VHYSM (VSM = 20 V): 0.75 V VHYSM (VSM = 30 V): 0.75 V Pass
SDCI_TC_0299	TCM_PHYL_INTF_VOLTRANGECQ	Test if working after connecting CQ to 0 V and 30 V via 1 Ω	See *Section 5.3.2.2*, *Table 5* - VIL and VIH, in *IO-Link Interface and System Specification Version 1.1.3* 4		Pass

Table 3-1. IO-Link® Physical Layer Test (continued)

ID	Name	Configuration	Specification (Clause)	Comment	Result
SDCI_TC_0021	TCM_PHYL_INTF_IQWUH		See *Section 5.3.3.3*, *Table 9* in *IO-Link Interface and System Specification Version 1.1.3* 4	Wake-up pulse from function generator	VIM@WURQ (VSM = 20 V): 18.9 V VIM@WURQ (VSM = 30 V): 28.5 V Pass
SDCI_TC_0022	TCM_PHYL_INTF_TWUH			Wake-up pulse from function generator	TWUH@WURQ (VSM = 20 V): 80 µs TWUH@WURQ (VSM = 30 V): 80 µs Pass
SDCI_TC_0023	TCM_PHYL_INTF_IQWUL			Wake-up pulse from function generator	VIM@WURQ (VSM = 20 V): 0.9 V VIM@WURQ (VSM = 30 V): 0.9 V Pass
SDCI_TC_0024	TCM_PHYL_INTF_TWUL			Wake-up pulse from function generator	TWUL@WURQ (VSM = 20 V): 80 µs TWUL@WURQ (VSM = 30 V): 80 µs Pass

3.3.3 Current Sink

Other than the IO-Link physical layer tests, also the integrated current sink is tested. Figure 3-7 shows the current into the CQ line, when only the RX together with the current sink is active. With a current of about 8.5 mA it is well within the allowed range of 5 – 15 mA.

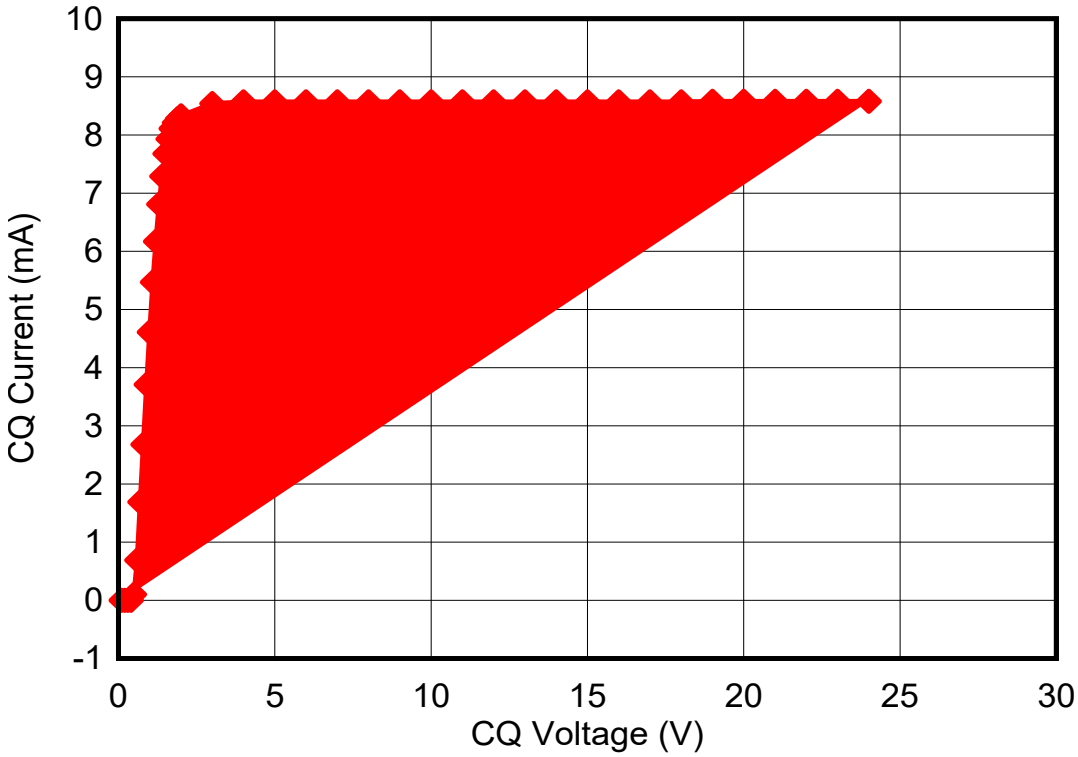


Figure 3-7. Current Sink of TIOL112

3.3.4 Timing Tests

Further testing was done in terms of timing, especially on the capability of a cycle time of 400 µs and the timing jitter during this communication. For this test the BOOSTXL-IOLINKM-8 is combined with the AM243x LaunchPad, and the example from the MCU+ SDK is compiled and loaded. Figure 3-8 with infinite persistence shows a cycle time of about 412 µs and no visible jitter in this configuration.

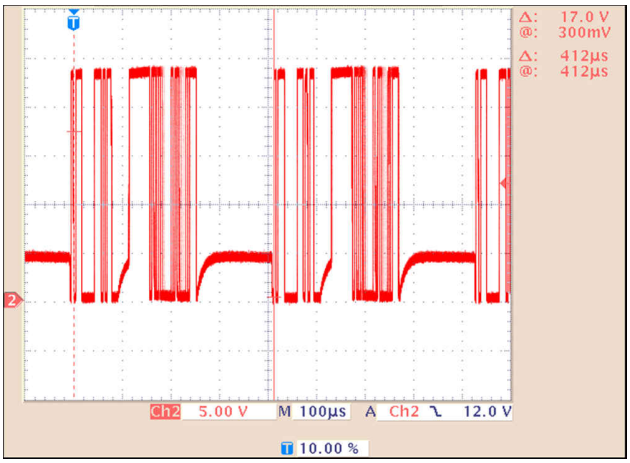


Figure 3-8. CQ Line Communication

Figure 3-9 shows the timing to be about 417 µs, well within the range allowed by the standard. Here also, the answer time of the connected device can be seen.

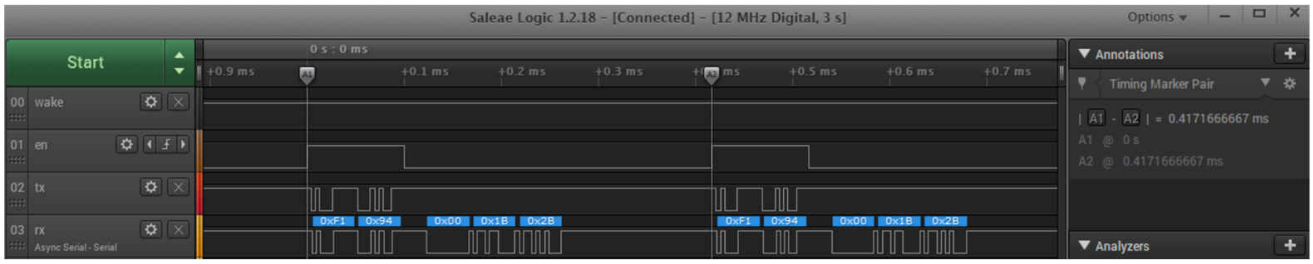


Figure 3-9. Master Cycle Timing

Figure 3-10 shows a zoomed in view of the second communication cycle on the CQ line. Trigger is set to trigger on one cycle and delay until the next one. This allows to look at the cycle to cycle jitter. With infinite persistence a jitter of about 50 ns gets visible. Compared to the rise and fall times, as well as the cycle timing, this is neglectable and does not degrade the system performance.

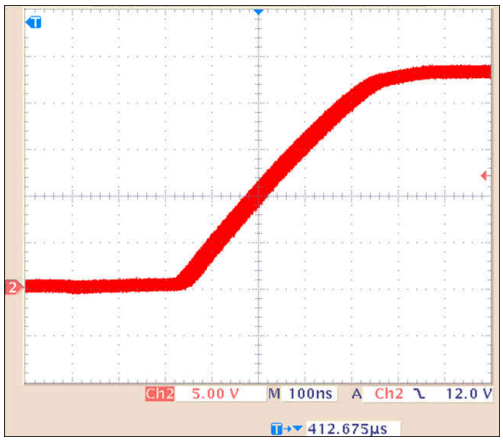


Figure 3-10. Master Cycle Jitter

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010234.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010234.

4.2 Tools and Software

Tools

Eight Port IO-Link Master Reference Design

AM243x Arm-based MCU General Purpose LaunchPad Development Kit

IO-Link Master Booster Pack

Software

Software Development Kit for AM243x Sitara™ Microcontrollers

4.3 Documentation Support

1. Texas Instruments, IO-Link Master Demo
2. Texas Instruments, TIOL112 and TIOL112x IO-Link Device Transceivers with Low Residual Voltage and Integrated Surge Protection in Small Packages data sheet
3. Texas Instruments, AM243x Sitara™ Microcontrollers data sheet
4. IO-Link Interface and System Specification V1.1.3
5. IO-Link Test Specification V1.1.3

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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4.5 Trademarks

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2022) to Revision A (April 2023)	Page
• Fixed many URLs in the Resources section	1
• Fixed URLs in the Schematics and BOM sections	12

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