

TI Designs: TIDA-01435

High Bandwidth, Zero-IF Reference Design for Microwave Backhaul



Description

This reference design describes the method for interfacing the TSW40RF82EVM with the TRF370417EVM. The TSW40RF82EVM reference design provides a platform to interface the DAC38RF82 with the TRF370417EVM, a high-performance modulator. The TRF370417EVM can modulate wideband signals up to 6-GHz. The TRF370417 device can be substituted for a suitable, higher-frequency device. Minimal modification is required to interface the digital-to-analog converter (DAC) with the modulator.

Resources

TIDA-01435	Design Folder
DAC38RF82	Product Folder
TRF370417EVM	Product Folder
TSW40RF82EVM	Product Folder

Features

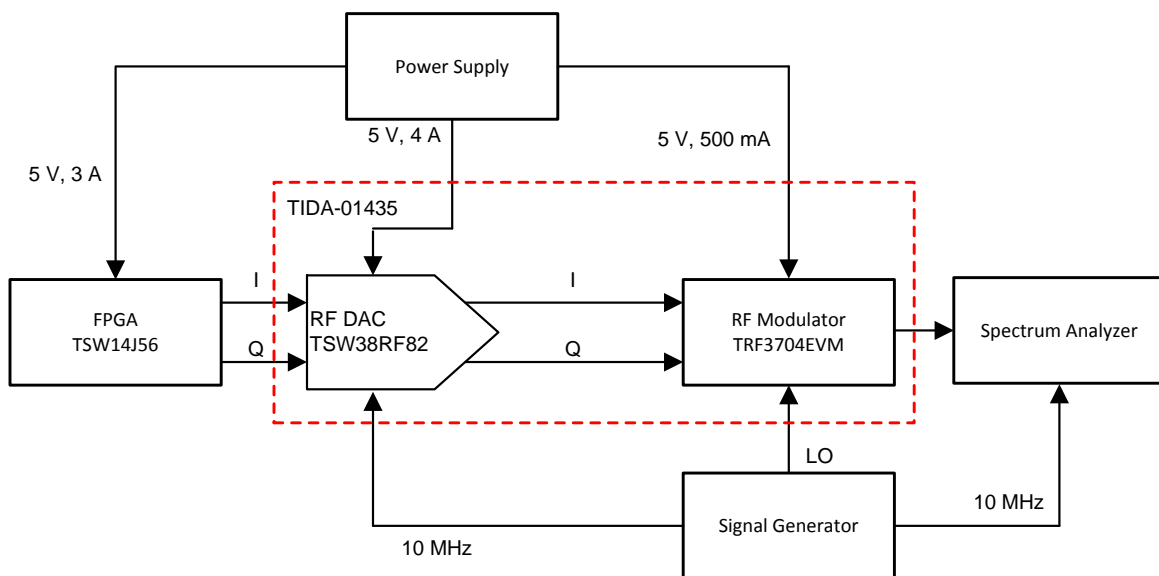
- High-Bandwidth, Zero-Intermediate Frequency (Zero-IF) Transmitter Solution
- DAC Solution With RF Sampling Speed up to 8 GS/PS
- Wideband Modulation With TRF370417EVM up to 6 GHz
- Modulator Interchangeable to Achieve Higher RF Frequencies
- Modulation Error Ratio (MER) Over 40 dB Throughout 5-GHz Frequency Band

Applications

- [Wireless Infrastructure](#)
- [Microwave Backhaul](#)



[ASK Our E2E Experts](#)



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1 System Description

The TSW40RF82EVM reference design demonstrates an RF transmitter solution that supports zero-IF microwave backhaul applications. This reference design includes the DAC38RF82 DAC, which interfaces with the TRF3704 modulator.

Quadrature amplitude modulation (QAM) is commonly used in microwave backhaul applications. Increasing the QAM level produces a higher throughput or capacity, but this method results in diminishing returns (see [Table 1](#)). The improvement in capacity is eventually outweighed by the deteriorating RF performance. Increasing the bandwidth instead of increasing the QAM level is a more efficient way to increase capacity. For example, increasing the level from 512 QAM to 1024 QAM results in a mere 11.11% increase in capacity at an additional cost of increased carrier-to-interference susceptibility; however, doubling the transmission bandwidth results in a 100% capacity increase, regardless of the QAM level, without the cost of increased sensitivity to interference.

Table 1. Diminishing Efficiency With Increased QAM Level

QAM LEVEL	NUMBER OF BITS PER SYMBOL	EFFICIENCY OVER PREVIOUS QAM LEVEL
4 QAM	2	—
8 QAM	3	50.00%
16 QAM	4	33.33%
32 QAM	5	25.00%
64 QAM	6	20.00%
128 QAM	7	16.67%
256 QAM	8	14.29%
512 QAM	9	12.50%
1024 QAM	10	11.11%

The TIDA-01435 reference design allows the utilization of 5-GHz unlicensed bands. The benefits of utilizing 5-GHz bands include [\[1\]](#):

1. Abundance of available channels – 21 non-overlapping 20-MHz channels (or 9 non-overlapping 40-MHz channels)
2. Less interference – Largely available and much less crowded, which translates into less RF interference
3. Improved performance – Improved spectrum efficiency and higher data rates due to lower interference levels and the availability of the channels

For applications operating at higher frequencies, substitute a higher frequency modulator for the TRF370417 device. This substitution may require an interface network that holds the respective common-mode voltages (V_{CM}) of the DAC and modulator to their nominal values. This type of network can be designed and implemented according to [High Bandwidth, High Frequency Transmitter Solution \[2\]](#).

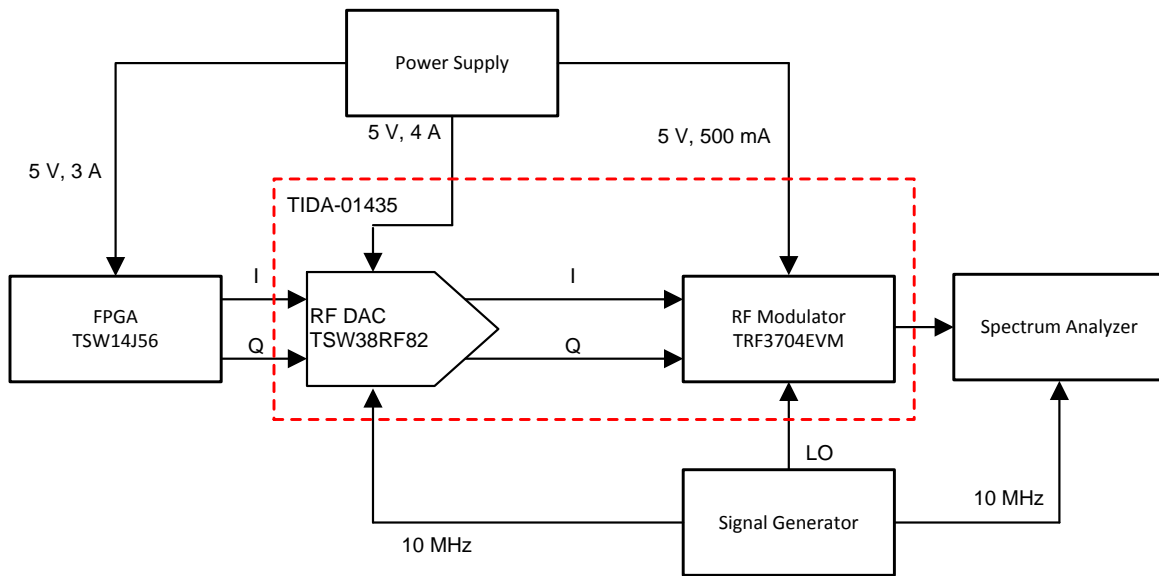
1.1 Key System Specifications

Table 2. Key System Specifications

SPECIFICATIONS	TYPICAL	UNITS
Max frequency	6	GHz
Quadrature amplitude modulation (QAM)	64	Symbols
Bandwidth (BW)	80	MHz
Modulation error ratio (MER)	40	dB

2 System Overview

2.1 Block Diagram



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Figure 1. TIDA-01435 Block Diagram

2.2 Highlighted Products

2.2.1 DAC38RF82

The DAC38RF82 is high performance RF Sampling Digital to Analog Converter (DAC). It is capable of sampling up to 9-GSPS. It is a dual channel device that supports a data rate up to 3.33-GSPS. This device is suited for using each channel as a very wide bandwidth quadrature input to an RF modulator.

2.2.2 TRF370417

The TRF370417 quadrature modulator operates up to 6-GHz. It supports wide bandwidths on the input baseband up to 1-GHz which yields up to 2-GHz RF signal bandwidth. The baseband ports operate at a common mode voltage of 1.7-V which matches the DAC38RF82 requirements.

2.2.3 TSW40RF82

The TSW40RF82 is a reference design that incorporates the DAC38RF82. The normal configuration of the reference design includes a transformer to convert the differential output to a single-ended output for interfacing with 50-ohm test equipment. The TSW40RF82 reference design also provides an option to access to the differential outputs directly. This access interfaces directly to the RF modulator.

3 Getting Started

3.1 Modifications for TSW40RF82EVM and TRF370417EVM Operation

3.1.1 Power Requirement

The TSW40RF82EVM requires a 5-V, 4-A supply, while the TRF370417EVM operates at a 5-V, 1-A supply. An additional external supply is applied at TP16 on the TSW40RF82EVM. This supply sets the common-mode voltage that is required by the DAC output and modulator input. The DAC gain is first set to the desired value and the external supply is then ramped up until the V_{CM} at the input of the modulator is equal to 1.7 V. If the DAC gain is changed, the external supply voltage must be adjusted accordingly. The DAC gain may overdrive the modulator if it is set at an extreme value. TI recommends a coarse DAC gain of 7 to 10 to drive the TRF370417EVM..

3.1.2 TSW40RF82EVM Modifications

- The RF shield near J3 must be removed to gain access to the interconnect components
- Resistors R380, R382, R383, R385, R388, and R390 must be populated with 0- Ω resistors
- Resistors R381, R384, R386, R389, and R391 must be uninstalled
- 50- Ω resistors should be populated in place of L1, L2, L7, and L8

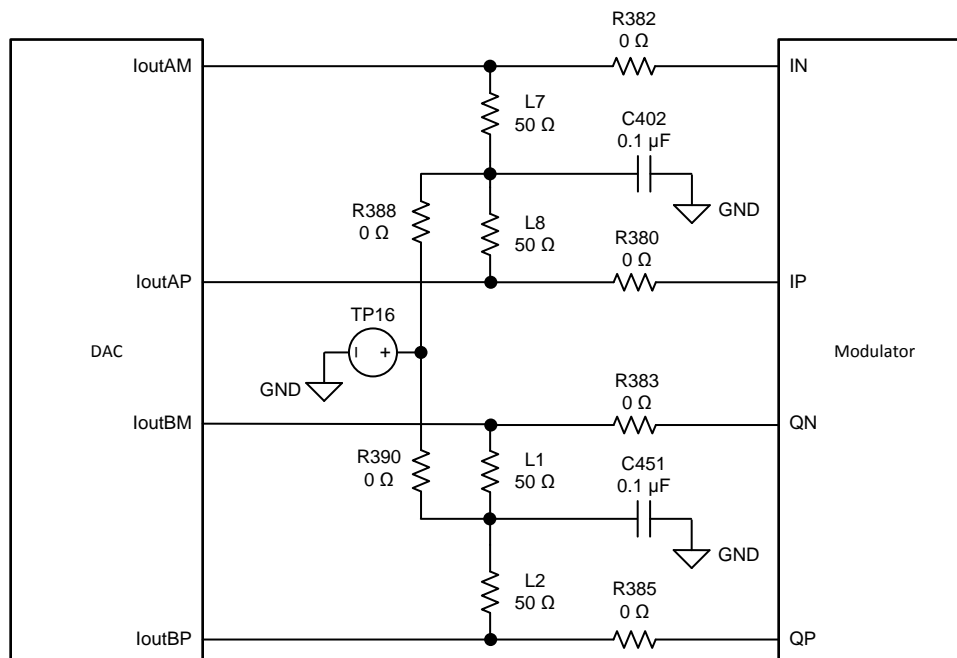


Figure 2. TSW40RF82EVM-to-TRF370417EVM Interface Schematic

4 DAC Configuration

The following restraints require consideration when interfacing the DAC with the modulator:

1. I and Q must be output in differential form because the modulator has two differential inputs.
2. The voltage-controlled oscillator (VCO) of the LMK04828 must be set to a valid frequency. This frequency sets the field-programmable gate array (FPGA) clock frequency and must be compatible with the input data rate, which is determined by the DAC sampling frequency and interpolation factor.
3. The sampling frequency must be within the range of valid frequencies of the DAC VCO.
4. The SerDes lane rate between the FPGA board and the DAC must not exceed the maximum JESD bit rate of 12.5 Gbps.

The DAC is set to dual DAC mode, real input, four lanes per DAC, and 4x interpolation operating at a JESD204B LMF configuration of 821. Setting the DAC to *real input*, despite actually outputting a complex baseband (BB) signal, isolates the DAC channels and preserves I and Q without adding them internally in the DAC.

The LMK04828 VCO is locked to 3072 GHz. This frequency is phase-locked to the on board 122.88-MHz voltage-controlled crystal oscillator (VCXO) through a 1/25 divider ratio. The numerator of the multiplier/divider ratio is set to one to ensure that the phase alignment occurs on every clock cycle of the crystal.

The DAC sampling clock is set to 8192 MHz and the interpolation is set to four, which, in turn, sets the data rate to 2048 MHz. This rate is divided down by a factor of 12 to produce the required FPGA clock of 256 MHz. The LMK04828 VCO must be divided down by an integer to produce the exact clock rate required by the FPGA.

The onboard VCXO can be interchanged with a different crystal or the divider ratio can be adjusted to obtain a different LMK04828 VCO frequency.

The following equations control the relevant frequencies for this design:

$$\text{Input Data Rate} = \left(\frac{f_s}{\text{Interpolation}} \right)$$

$$\text{SerDes Rate} = \left((\text{Input Data Rate}) \times (\text{Number of Channels}) \times \left(\frac{10}{8} \right) \times \left(\frac{1}{\text{Lanes}} \right) \times (\text{DAC}_{\text{RESOLUTION}}) \right)$$

$$\frac{\text{SerDes Rate}}{40} = f_{\text{FPGA}}$$

$$f_{\text{VCO_LMK04828}} = N_{\text{DIV}} \times f_{\text{FPGA}}$$

A data rate of 2048 MHz is used for this design. This data rate allows for an effective bandwidth of approximately 1 GHz ($f_s / 2$). The interpolation is set to four, which fixes the sampling frequency as follows in [Equation 1](#):

$$2048 \times 4 = 8192 \text{ MHz} \quad (1)$$

Use [Equation 2](#) to solve for the SerDes rate.

$$\left(\frac{8192}{4} \right) \times (2) \times \left(\frac{8}{10} \right) \times \left(\frac{1}{8} \right) \times (16) = 10240 \text{ MHz} \quad (2)$$

This rate is under the 12.5-GSPS limit and is a valid SerDes rate. Applying [Equation 2](#) produces the FPGA frequency of the TSW14J56EVM in [Equation 3](#):

$$\left(\frac{10240}{40} \right) = 256 \text{ MHz} \quad (3)$$

The quotient of the LMK04828 VCO frequency and the FPGA clock frequency must be an integer because the FPGA clock is synthesized from this VCO frequency through an integer divider. Any LMK04828 VCO frequency is valid as long as this requirement is satisfied and the selected frequency is confirmed to be within the specified locking range of the VCO. Equation 4 is then applied to obtain the LMK04828 VCO frequency:

$$256 \times 12 = 3072 \text{ MHz} \tag{4}$$

In summary, the frequency of the LMK04828 VCO and FPGA clock is determined and held constant. The system of equations is then solved to determine a valid sampling frequency that is within the range of the DAC phase-locked loop (PLL) and VCO. The previous configuration results in a SerDes lane rate of 10240 MHz, which is under the maximum lane rate of 12.5 GHz. Figure 3 shows the design configuration.

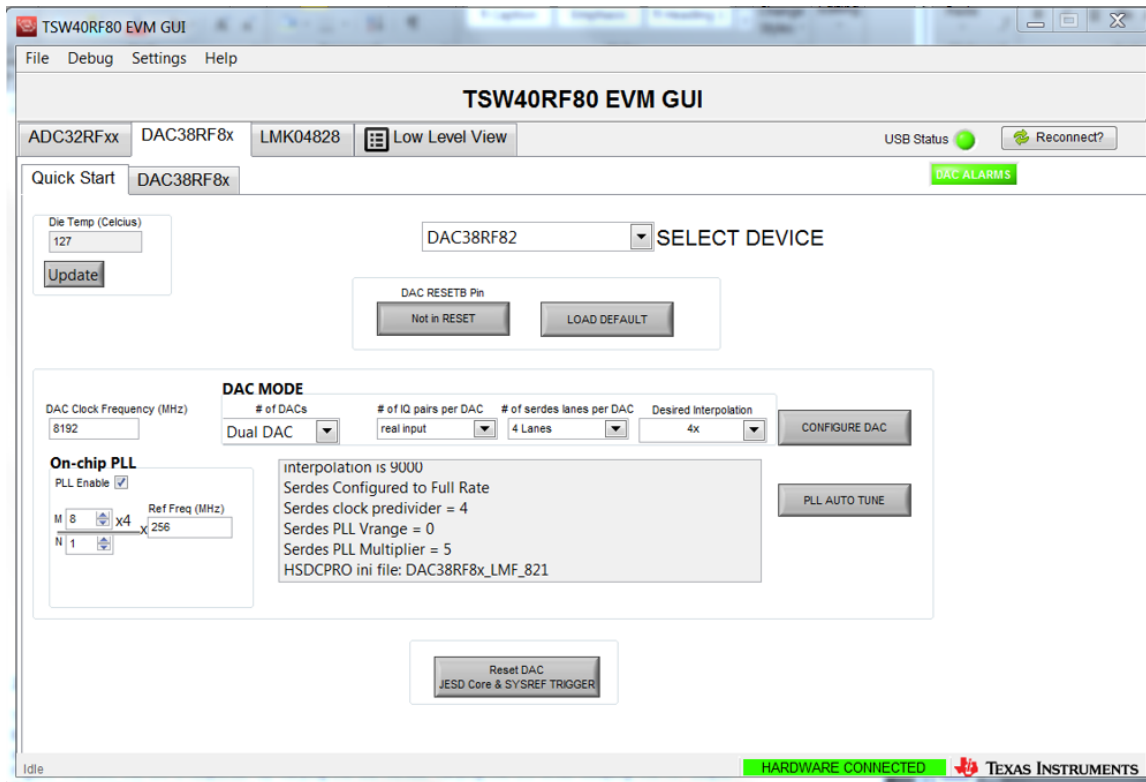


Figure 3. TSW40RF82EVM GUI DAC Configuration—Front Panel

5 Testing and Results

5.1 Measured Performance

The DAC38RF82 is a dual DAC that can sample at a rate of up to 9 GSPS. This DAC supports a maximum complex data rate of 3.33 GSPS. The device is also capable of synthesizing wideband signals up to 2.66-GHz bandwidth. The device is well suited for generating complex wide-bandwidth signals used in QAM schemes, such as the wideband signal shown in Figure 4. The optional PLL/VCO simplifies the DAC clock generation by allowing use of a lower frequency to synthesize the high-frequency sampling clock.

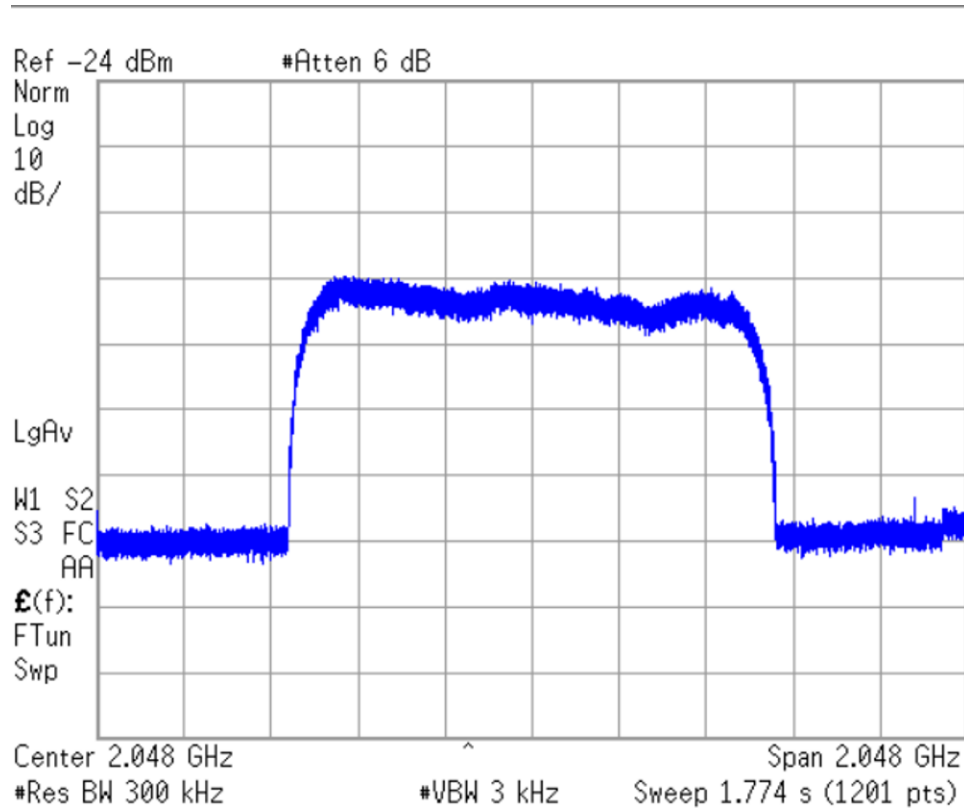


Figure 4. 1024-MHz Wide Signal Generated by RF DAC

5.1.1 OIP3 Response Over BB Frequency

The OIP3 performance over the BB frequency offset is measured with two tones separated by 10 MHz. The OIP3 over frequency is measured in two ways. The first measurement varies the LO across the frequency band while keeping the BB at a fixed 50-MHz offset. The second measurement keeps the LO constant at 5 GHz and varies the BB offset. Figure 5 shows the OIP3 response.

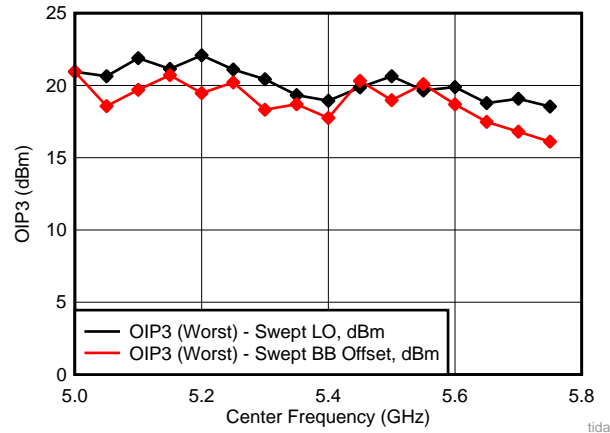


Figure 5. OIP3 Performance With Varying BB Frequency Offset and Varying LO

5.1.2 MER Response Over LO Frequency

Another key concern related to high-bandwidth modulated transmissions is modulation error ratio (MER). This metric indicates the quality of the received signal and is described in the following Equation 5:

$$\text{MER (dB)} = 10 \times \log_{10} \left[\frac{\text{Average Symbol Power}}{\text{Average Error Power}} \right] \tag{5}$$

For QAM transmissions, the higher the MER (dB), the closer the data points align to their ideal locations on the constellation diagram.

This test uses a 64-QAM signal with a bandwidth of 81.92 MHz generated by the DAC and then modulated by the TRF370417EVM. The product of the signal chip rate and interpolation must equal the DAC data rate. As the signal interpolation value must be an integer, and the data rate is already determined, the chip rate must be carefully selected such that it is a rational number. This careful selection reduces the demodulation error because the target demodulation chip rate matches the exact target demodulation chip rate on the receiver end. The signal bandwidth also represents the maximum allowed by the available demodulation equipment.

The first test is performed by offsetting the signal by 100 MHz from DC and sweeping it over the frequency. This test allows the examination of the MER without the sideband suppression limitation imposed by the modulator. The second test sweeps the signal with no offset from DC (Zero-IF). In this case, a number of things affect the MER, including the sideband suppression performance of the modulator, harmonics, and intermodulation products (especially second-order intermodulation products) of the signal itself. The third test is performed at Zero-IF as well; however, the VCM, LO power, and DAC gain are optimized at each data point to produce a more favorable MER. Figure 6 shows how the equalization was applied.

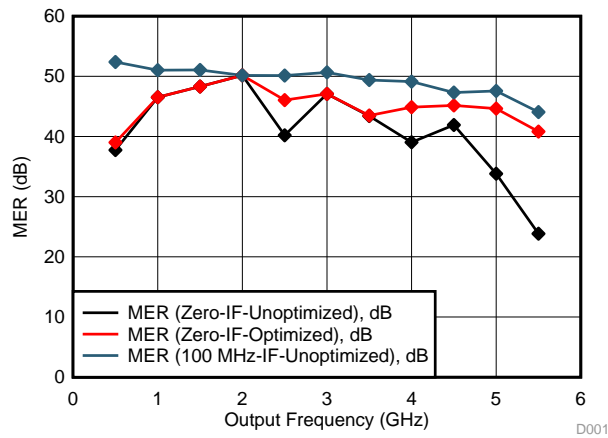


Figure 6. Equalized MER of 64-QAM Signal Over Output Frequency

5.2 Conclusion

The TSW40RF82EVM in conjunction with the TRF370417 device is a suitable platform to operate at output frequencies up to 6 GHz with BB signal bandwidths up to around 2 GHz. A simple network is required to interface the two devices because the DAC common-mode voltage is compatible with the TRF370417EVM common-mode voltage. The demand to increase capacity and improve performance in microwave backhaul applications is rising. Increasing the QAM level to satisfy this demand is neither a viable nor sustainable solution, however, increasing the BB signal bandwidth is a feasible solution.

6 Design Files

6.1 Schematics

To download the schematics, see the design files at [TIDA-01435](#).

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-01435](#).

7 Related Documentation

1. Ho, Quang-Dung; Tweed, Daneil; Le-Ngoc, Tho; *Long Term Evolution In Unlicensed Bands*, 1st Ed. Cham, Switzerland: Springer International Publishing, 2017.
2. Texas Instruments, [High Bandwidth, High Frequency Transmitter Solution](#), TSW38J84EVM Reference Design (TIDU579)

7.1 Trademarks

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8 Terminology

BB— Baseband

DAC— Digital-to-analog converter

FPGA— Field-programmable gate array

GUI— Graphical user interface

LMF— Limited mitigation factor

MER— Modulation error ratio

PLL— Phase-locked loop

QAM— Quadrature amplitude modulation

VCO— Voltage-controlled oscillator

VCXO— Voltage-controlled crystal oscillator

Zero-IF— Zero-intermediate frequency

9 About the Author

ABDALLAH OBIDAT is an Applications Engineer at Texas Instruments. He supports high-speed data converters, discrete RF devices, and integrated transceivers. Abdallah earned his bachelor of science in electrical engineering (BSEE) from the Georgia Institute of Technology.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2017) to A Revision	Page
• Updated Figure 5 : Y-axis changed from "MER (dB)" to "OIP3 (dBm)"	8

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