Test Data
For PMP20852
June 16, 2017

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1. Design Specifications

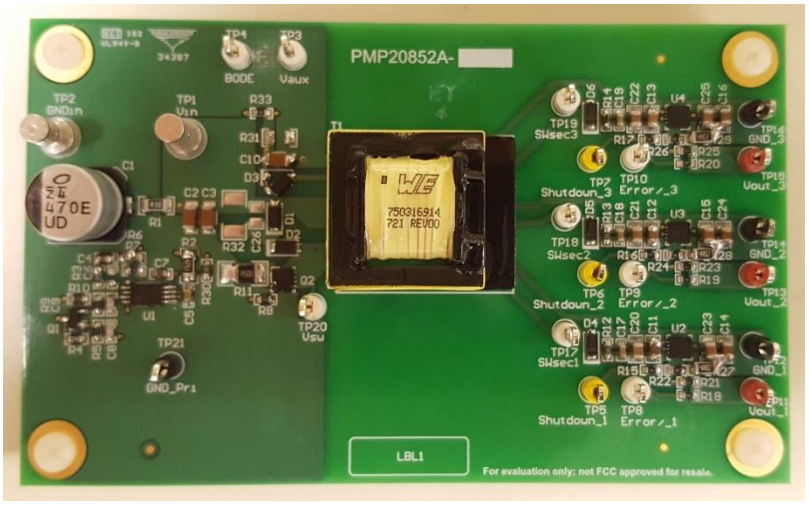
Vin Minimum	**10VDC**
Vin Nominal	**12VDC**
Vin Maximum	**14VDC**
Vout 1	**16VDC**
Iout 1	**65mA**
Vout 2	**16VDC**
Iout 2	**65mA**
Vout 3	**16VDC**
Iout 3	**65mA**
Switching Frequency	**≈ 400KHz**

2. Circuit Description

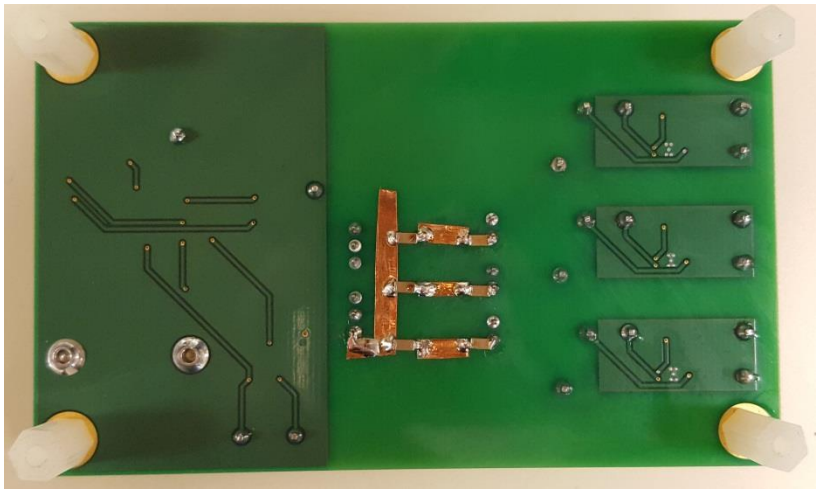
PMP20852 is an Isolated Flyback Converter with primary-side regulation using the UCC2805 controller IC. There are three independently isolated outputs on the secondary side, each of which use LP2951-33 linear regulators to provide a well-regulated 16V output on each of the three rails. The design accepts an input voltage of 10Vin to 14Vin (12Vin Nominal) and provides three isolated 16Voutput rails capable of supplying 65mA each of continuous current to the load. The design is built on a 2-layer PCB with 1oz Copper on each layer.

3. PMP20852 Board Photos

Board Dimensions: 4.2” x 2.55”

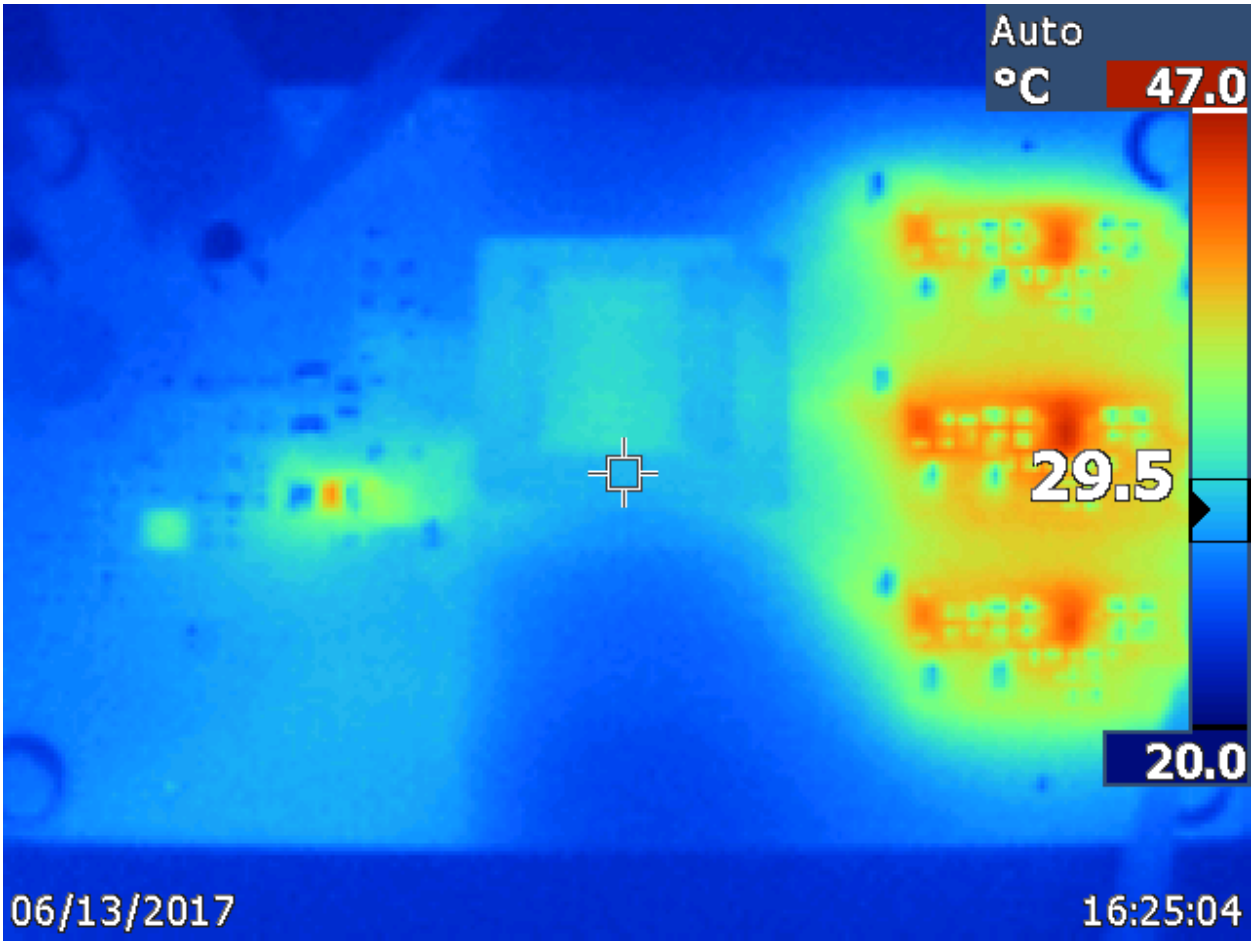


Board Photo (Top)

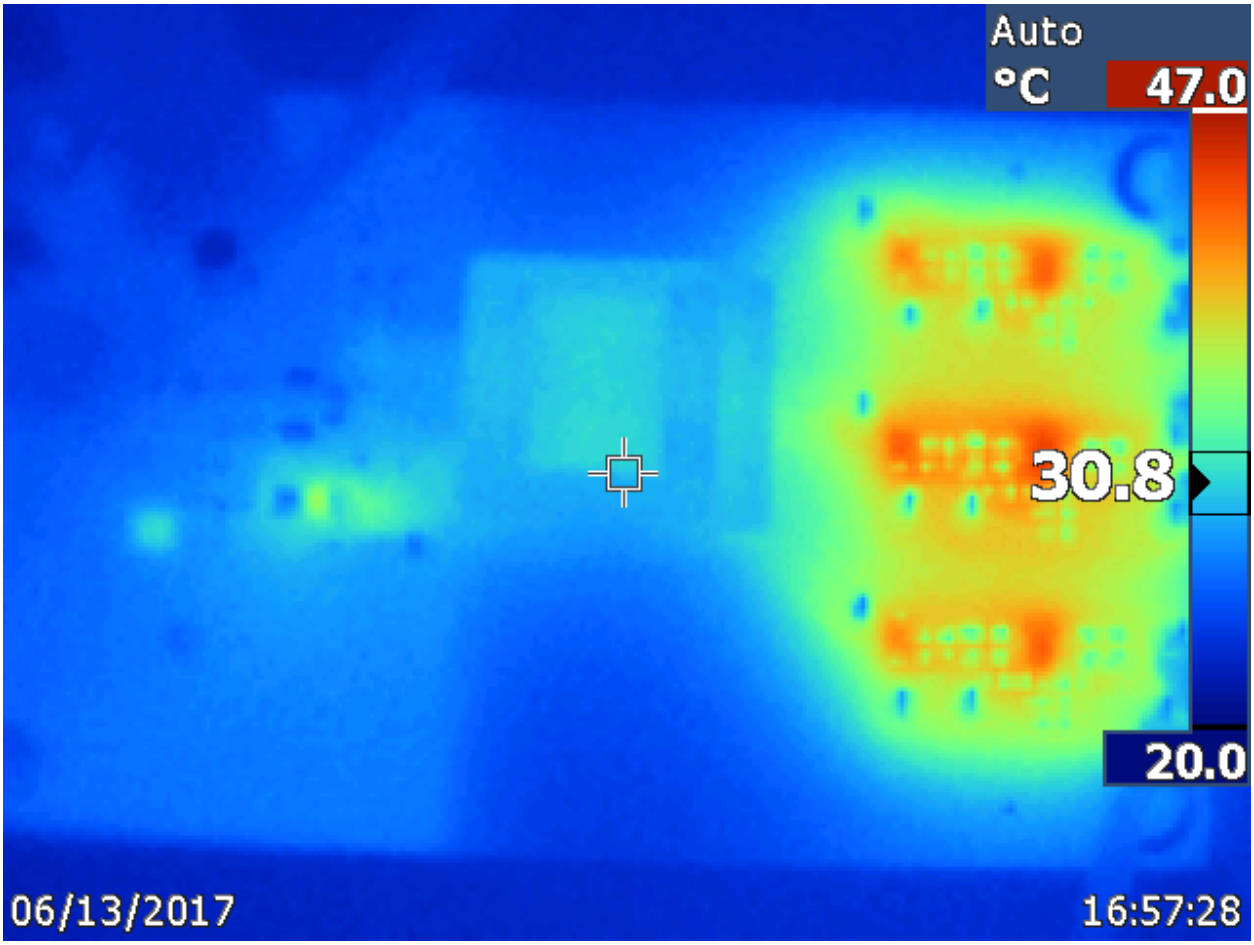


Board Photo (Bottom)

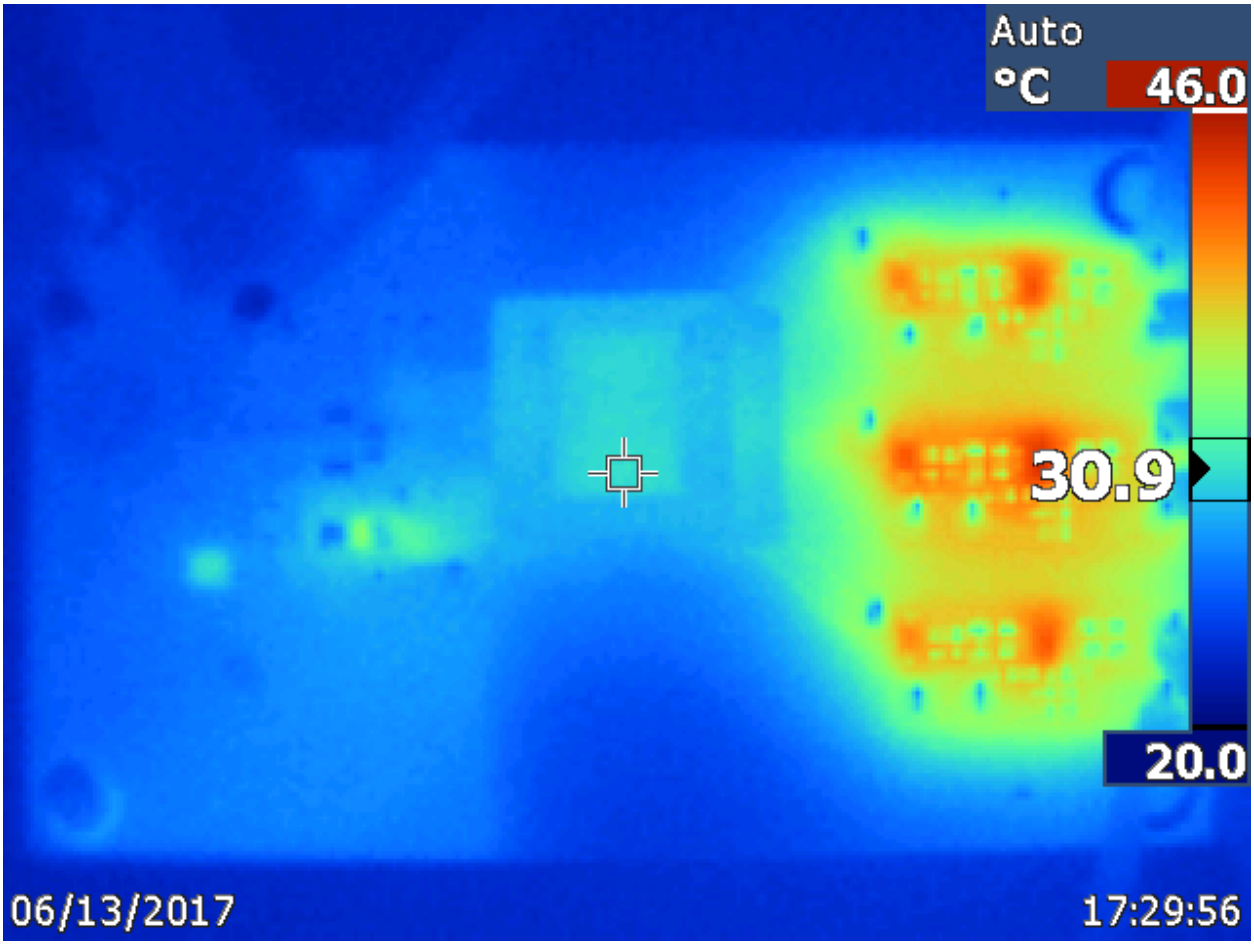
4. Thermal Data



IR thermal image taken at steady state with 10Vin and 65mA load on each of the three output rails (no airflow; ambient at room temp.)



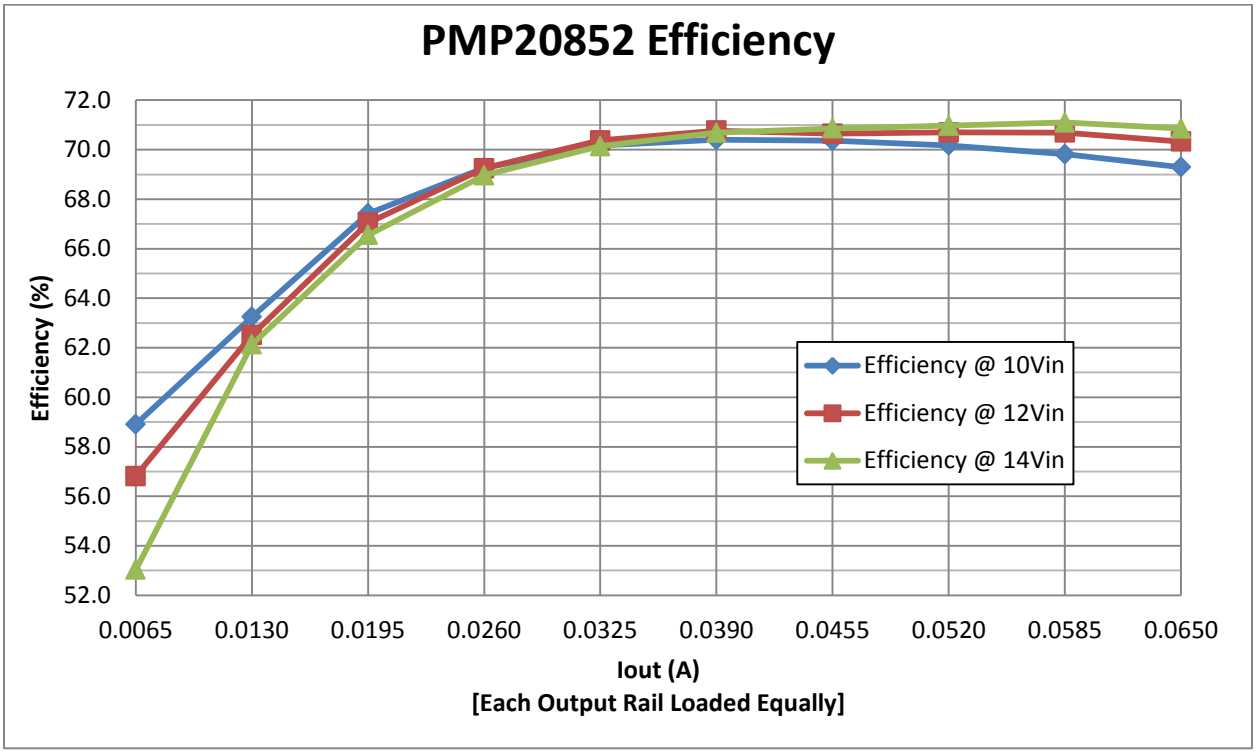
IR thermal image taken at steady state with 12Vin and 65mA load on each of the three output rails (no airflow; ambient at room temp.)



IR thermal image taken at steady state with 14Vin and 65mA load on each of the three output rails (no airflow; ambient at room temp.)

5. Efficiency and Regulation

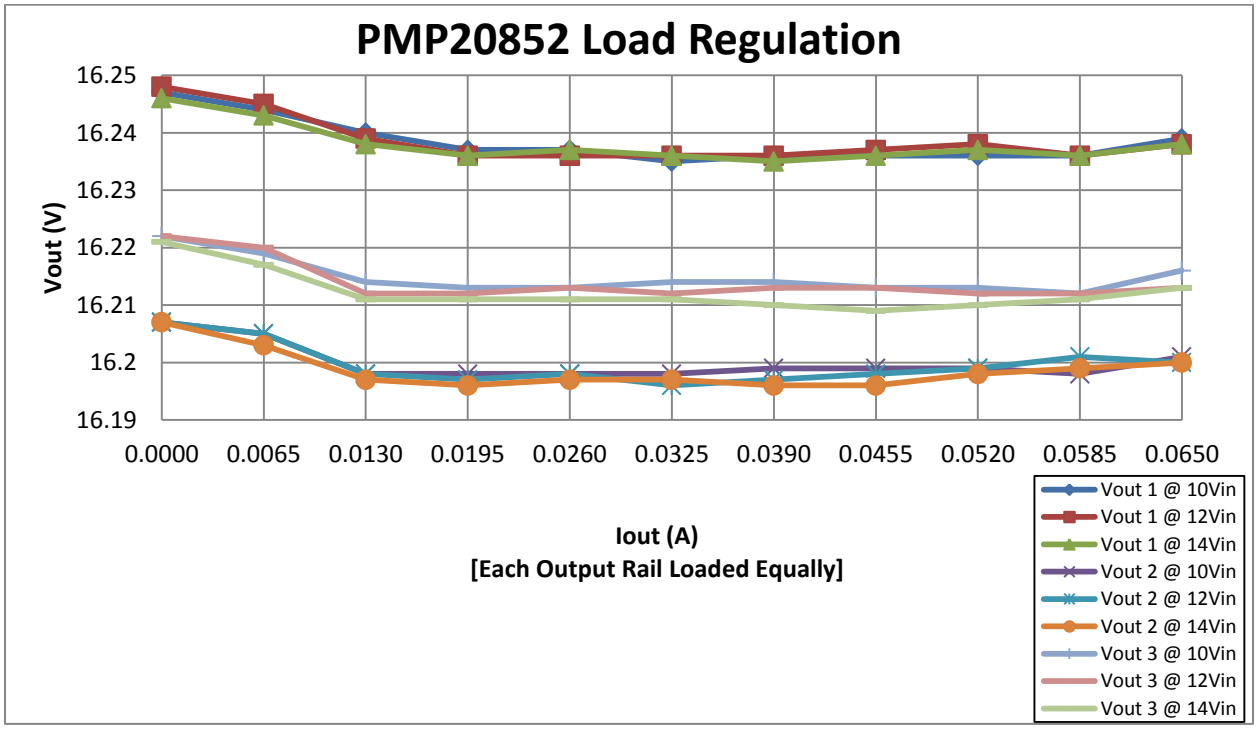
5.1 Efficiency Chart



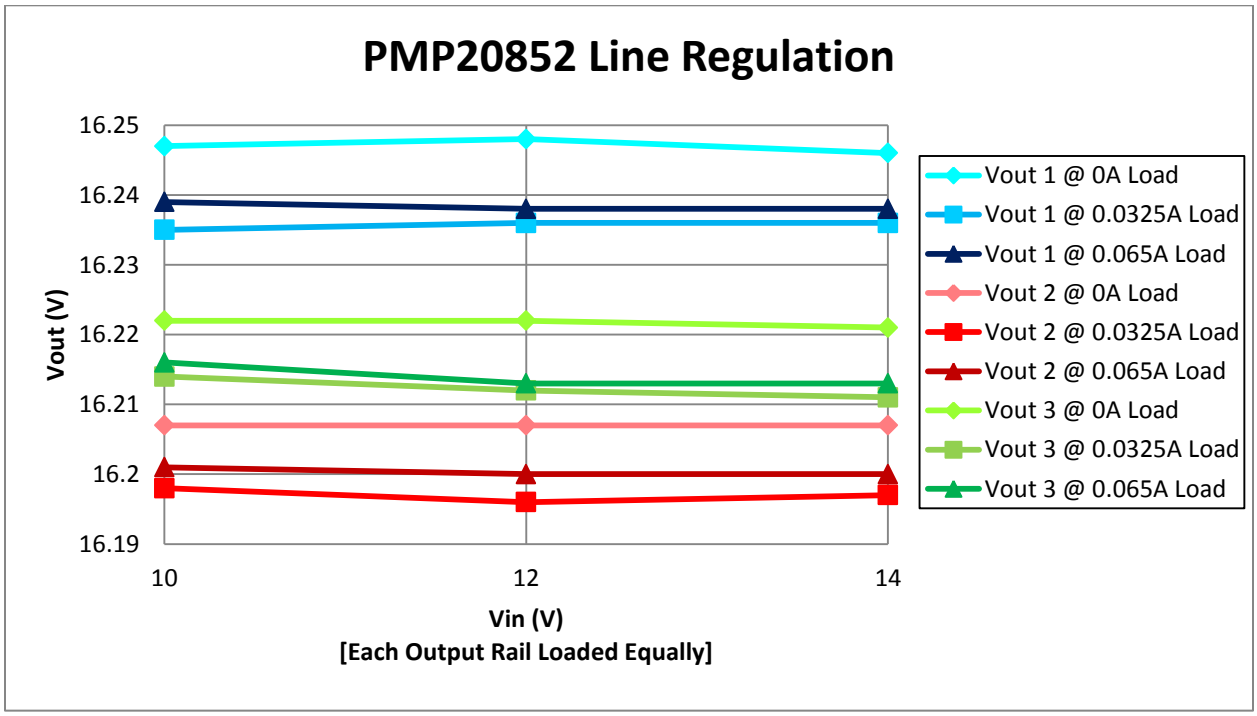
5.2 Efficiency Data

Vin (V)	Iin (A)	Vbias (V)	Vsec 1 (V)	Vout 1 (V)	Iout 1 (A)	Vsec 2 (V)	Vout 2 (V)	Iout 2 (A)	Vsec 3 (V)	Vout 3 (V)	Iout 3 (A)	Pin (W)	Pout 1 (W)	Pout 2 (W)	Pout 3 (W)	Pout Total (W)	Ploss (W)	Efficiency (%)
10	0.0157	9.346	20.224	16.247	0	20.196	16.207	0	20.219	16.222	0	0.157	0.000	0.000	0.000	0.000	0.157	0.0
10	0.0537	9.357	19.442	16.244	0.0065	19.407	16.205	0.0065	19.432	16.219	0.0065	0.537	0.106	0.105	0.105	0.316	0.221	58.9
10	0.1	9.347	19.269	16.24	0.013	19.247	16.198	0.013	19.25	16.214	0.013	1.000	0.211	0.211	0.211	0.632	0.368	63.2
10	0.1407	9.347	19.198	16.237	0.0195	19.177	16.198	0.0195	19.178	16.213	0.0195	1.407	0.317	0.316	0.316	0.949	0.458	67.4
10	0.1826	9.346	19.141	16.237	0.026	19.122	16.198	0.026	19.125	16.213	0.026	1.826	0.422	0.421	0.422	1.265	0.561	69.3
10	0.2253	9.346	19.09	16.235	0.0325	19.077	16.198	0.0325	19.075	16.214	0.0325	2.253	0.528	0.526	0.527	1.581	0.672	70.2
10	0.2695	9.346	19.039	16.236	0.039	19.033	16.199	0.039	19.023	16.214	0.039	2.695	0.633	0.632	0.632	1.897	0.798	70.4
10	0.3146	9.345	18.988	16.236	0.0455	18.99	16.199	0.0455	18.966	16.213	0.0455	3.146	0.739	0.737	0.738	2.213	0.933	70.4
10	0.3605	9.345	18.93	16.236	0.052	18.94	16.199	0.052	18.905	16.213	0.052	3.605	0.844	0.842	0.843	2.530	1.075	70.2
10	0.4076	9.345	18.865	16.236	0.0585	18.885	16.198	0.0585	18.838	16.212	0.0585	4.076	0.950	0.948	0.948	2.846	1.230	69.8
10	0.4564	9.344	18.806	16.239	0.065	18.831	16.201	0.065	18.771	16.216	0.065	4.564	1.056	1.053	1.054	3.163	1.401	69.3
Vin (V)	**Iin (A)**	**Vbias (V)**	**Vsec 1 (V)**	**Vout 1 (V)**	**Iout 1 (A)**	**Vsec 2 (V)**	**Vout 2 (V)**	**Iout 2 (A)**	**Vsec 3 (V)**	**Vout 3 (V)**	**Iout 3 (A)**	**Pin (W)**	**Pout 1 (W)**	**Pout 2 (W)**	**Pout 3 (W)**	**Pout Total (W)**	**Ploss (W)**	**Efficiency (%)**
12	0.0127	9.346	20.116	16.248	0	20.102	16.207	0	20.102	16.222	0	0.152	0.000	0.000	0.000	0.000	0.152	0.0
12	0.0464	9.346	19.404	16.245	0.0065	19.371	16.205	0.0065	19.395	16.22	0.0065	0.557	0.106	0.105	0.105	0.316	0.240	56.8
12	0.0843	9.349	19.237	16.239	0.013	19.211	16.198	0.013	19.22	16.212	0.013	1.012	0.211	0.211	0.211	0.632	0.379	62.5
12	0.1179	9.347	19.152	16.236	0.0195	19.132	16.197	0.0195	19.132	16.212	0.0195	1.415	0.317	0.316	0.316	0.949	0.466	67.0
12	0.1522	9.346	19.094	16.236	0.026	19.075	16.198	0.026	19.078	16.213	0.026	1.826	0.422	0.421	0.422	1.265	0.562	69.3
12	0.1872	9.346	19.047	16.236	0.0325	19.032	16.196	0.0325	19.033	16.212	0.0325	2.246	0.528	0.526	0.527	1.581	0.665	70.4
12	0.2234	9.345	19.004	16.236	0.039	18.995	16.197	0.039	18.99	16.213	0.039	2.681	0.633	0.632	0.632	1.897	0.784	70.8
12	0.2611	9.345	18.96	16.237	0.0455	18.957	16.198	0.0455	18.943	16.213	0.0455	3.133	0.739	0.737	0.738	2.213	0.920	70.6
12	0.2982	9.344	18.913	16.238	0.052	18.918	16.199	0.052	18.894	16.212	0.052	3.578	0.844	0.842	0.843	2.530	1.049	70.7
12	0.3355	9.344	18.864	16.236	0.0585	18.874	16.201	0.0585	19.842	16.212	0.0585	4.026	0.950	0.948	0.948	2.846	1.180	70.7
12	0.3747	9.343	18.811	16.238	0.065	18.825	16.2	0.065	18.783	16.213	0.065	4.496	1.055	1.053	1.054	3.162	1.334	70.3
Vin (V)	**Iin (A)**	**Vbias (V)**	**Vsec 1 (V)**	**Vout 1 (V)**	**Iout 1 (A)**	**Vsec 2 (V)**	**Vout 2 (V)**	**Iout 2 (A)**	**Vsec 3 (V)**	**Vout 3 (V)**	**Iout 3 (A)**	**Pin (W)**	**Pout 1 (W)**	**Pout 2 (W)**	**Pout 3 (W)**	**Pout Total (W)**	**Ploss (W)**	**Efficiency (%)**
14	0.0134	9.346	20.122	16.246	0	20.09	16.207	0	20.159	16.221	0	0.188	0.000	0.000	0.000	0.000	0.188	0.0
14	0.0426	9.346	19.354	16.243	0.0065	19.328	16.203	0.0065	19.344	16.217	0.0065	0.596	0.106	0.105	0.105	0.316	0.280	53.0
14	0.0727	9.348	19.209	16.238	0.013	19.179	16.197	0.013	19.195	16.211	0.013	1.018	0.211	0.211	0.211	0.632	0.385	62.1
14	0.1018	9.346	19.115	16.236	0.0195	19.095	16.196	0.0195	19.097	16.211	0.0195	1.425	0.317	0.316	0.316	0.949	0.477	66.6
14	0.131	9.346	19.054	16.237	0.026	19.036	16.197	0.026	19.036	16.211	0.026	1.834	0.422	0.421	0.421	1.265	0.569	69.0
14	0.161	9.345	19.007	16.236	0.0325	18.99	16.197	0.0325	18.992	16.211	0.0325	2.254	0.528	0.526	0.527	1.581	0.673	70.1
14	0.1917	9.345	18.968	16.235	0.039	18.956	16.196	0.039	18.954	16.21	0.039	2.684	0.633	0.632	0.632	1.897	0.787	70.7
14	0.2231	9.345	18.93	16.236	0.0455	18.923	16.196	0.0455	18.914	16.209	0.0455	3.123	0.739	0.737	0.738	2.213	0.910	70.9
14	0.2546	9.344	18.89	16.237	0.052	18.888	16.198	0.052	18.872	16.21	0.052	3.564	0.844	0.842	0.843	2.530	1.035	71.0
14	0.2859	9.344	18.848	16.236	0.0585	18.856	16.199	0.0585	18.829	16.211	0.0585	4.003	0.950	0.948	0.948	2.846	1.157	71.1
14	0.3188	9.343	18.803	16.238	0.065	18.813	16.2	0.065	18.779	16.213	0.065	4.463	1.055	1.053	1.054	3.162	1.301	70.9

5.3 Load Regulation



5.4 Line Regulation

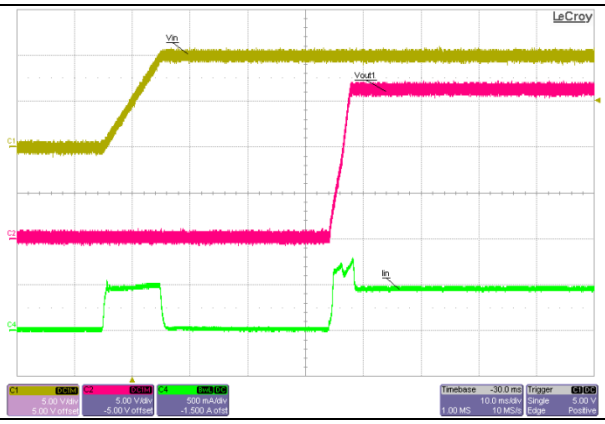


5.5 Regulation Data

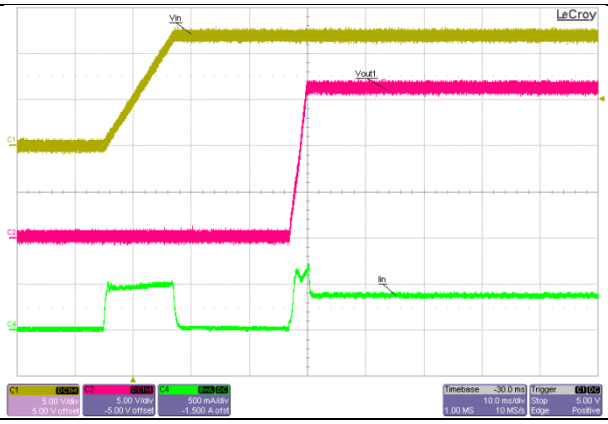
Vin (V)	Iin (A)	Vbias (V)	Iout 1 (A)	Iout 2 (A)	Iout 3 (A)	Vsec 1 (V)	Vout 1 (V)	Vsec 2 (V)	Vout 2 (V)	Vsec 3 (V)	Vout 3 (V)
10	0.0157	9.346	0	0	0	20.224	16.247	20.196	16.207	20.219	16.222
10	0.1589	9.35	0	0	1	20.137	16.243	20.458	16.202	18.94	16.208
10	0.1586	9.348	0	1	0	19.917	16.244	18.951	16.192	19.966	16.219
10	0.3043	9.347	0	1	1	19.973	16.245	18.921	16.197	18.893	16.21
10	0.1591	9.346	1	0	0	18.949	16.231	20.015	16.206	19.725	16.219
10	0.3038	9.346	1	0	1	18.904	16.233	20.809	16.206	18.869	16.209
10	0.3048	9.346	1	1	0	18.917	16.233	18.907	16.195	19.858	16.218
10	0.4564	9.344	1	1	1	18.806	16.239	18.831	16.201	18.771	16.216
Vin (V)	**Iin (A)**	**Vbias (V)**	**Iout 1 (A)**	**Iout 2 (A)**	**Iout 3 (A)**	**Vsec 1 (V)**	**Vout 1 (V)**	**Vsec 2 (V)**	**Vout 2 (V)**	**Vsec 3 (V)**	**Vout 3 (V)**
12	0.0127	9.346	0	0	0	20.116	16.248	20.102	16.207	20.102	16.222
12	0.1327	9.348	0	0	1	20.085	16.243	20.43	16.2	18.905	16.209
12	0.1322	9.347	0	1	0	19.83	16.245	18.917	16.195	19.851	16.217
12	0.2516	9.346	0	1	1	19.872	16.245	18.89	16.198	18.873	16.211
12	0.133	9.346	1	0	0	18.916	16.232	19.98	16.204	19.645	16.216
12	0.2515	9.345	1	0	1	18.878	16.234	20.546	16.205	18.851	16.209
12	0.252	9.345	1	1	0	18.893	16.235	18.88	16.196	19.828	16.217
12	0.3747	9.343	1	1	1	18.811	16.238	18.825	16.2	18.783	16.213
Vin (V)	**Iin (A)**	**Vbias (V)**	**Iout 1 (A)**	**Iout 2 (A)**	**Iout 3 (A)**	**Vsec 1 (V)**	**Vout 1 (V)**	**Vsec 2 (V)**	**Vout 2 (V)**	**Vsec 3 (V)**	**Vout 3 (V)**
14	0.0134	9.346	0	0	0	20.122	16.246	20.09	16.207	20.159	16.221
14	0.1146	9.347	0	0	1	20.061	16.243	20.427	16.202	18.872	16.208
14	0.1143	9.346	0	1	0	19.771	16.244	18.885	16.194	19.771	16.215
14	0.2153	9.346	0	1	1	19.792	16.245	18.857	16.198	18.845	16.209
14	0.1148	9.346	1	0	0	18.885	16.234	19.961	16.203	19.585	16.215
14	0.2151	9.345	1	0	1	18.848	16.233	20.388	16.204	18.825	16.208
14	0.2156	9.345	1	1	0	18.864	16.236	18.849	16.196	19.778	16.215
14	0.3188	9.343	1	1	1	18.803	16.238	18.813	16.2	18.779	16.213
***NOTE: Iout of "0" signifies "No Load"; Iout of "1" signifies "Full Load" of 65mA**					**Min =>**	18.803	16.231	18.813	16.192	18.771	16.208
					Max =>	20.224	16.248	20.809	16.207	20.219	16.222

6 Waveforms

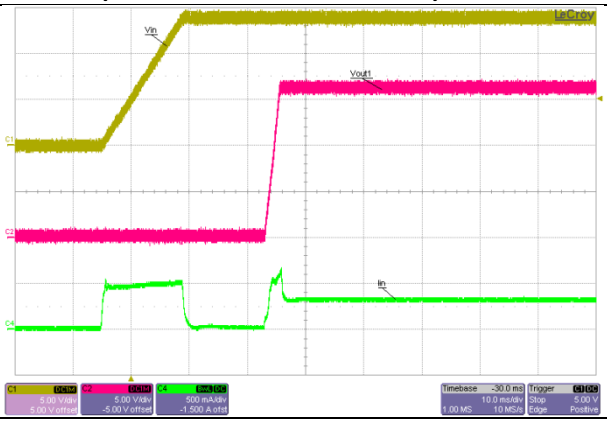
6.1 Startup



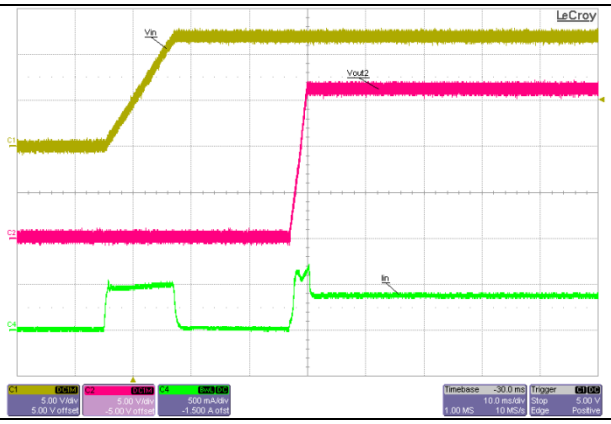
Vo1 Startup at 10Vin with All Outputs at Full (65mA Constant Resistance) Load



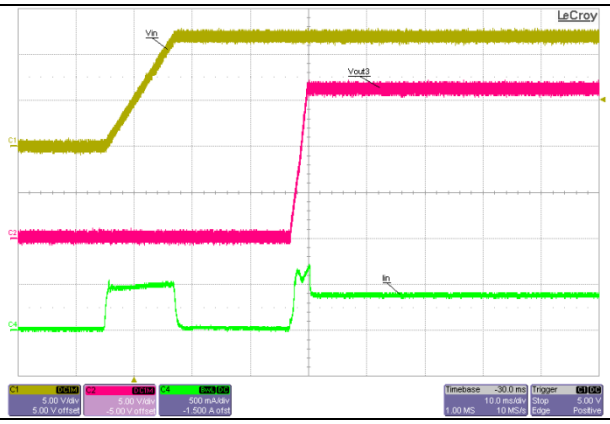
Vo1 Startup at 12Vin with All Outputs at Full (65mA Constant Resistance) Load



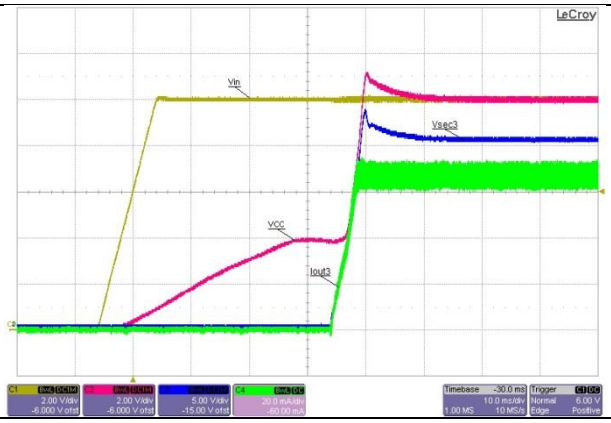
Vo1 Startup at 14Vin with All Outputs at Full (65mA Constant Resistance) Load



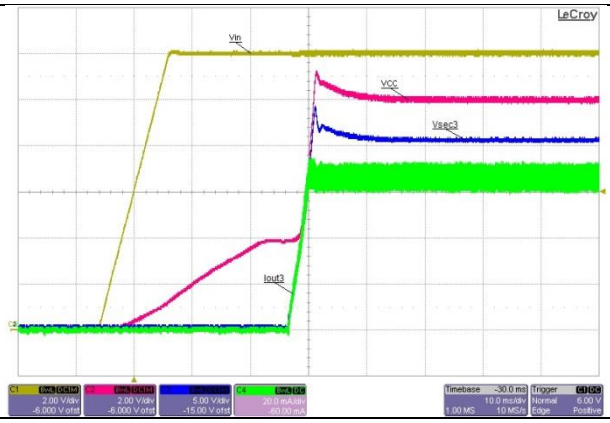
Vo2 Startup at 12Vin with All Outputs at Full (65mA Constant Resistance) Load



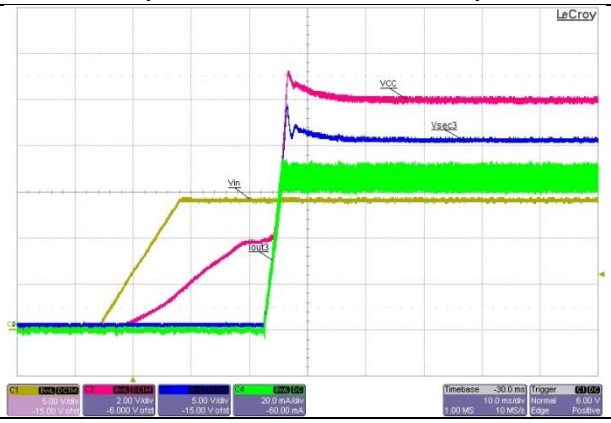
Vo3 Startup at 12Vin with All Outputs at Full (65mA Constant Resistance) Load



Vsec3 and VCC Startup at 10Vin with All Outputs at Full (65mA Constant Resistance) Load

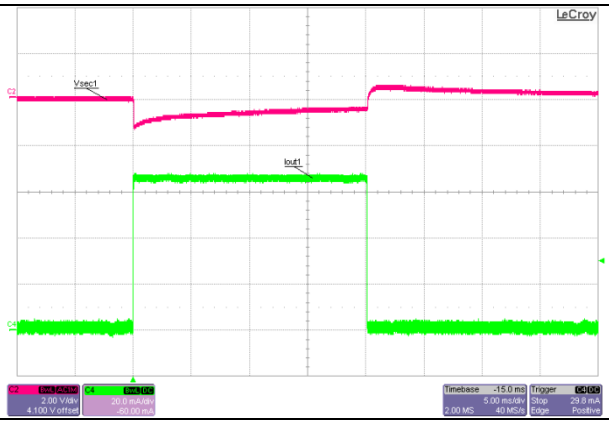


Vsec3 and VCC Startup at 12Vin with All Outputs at Full (65mA Constant Resistance) Load

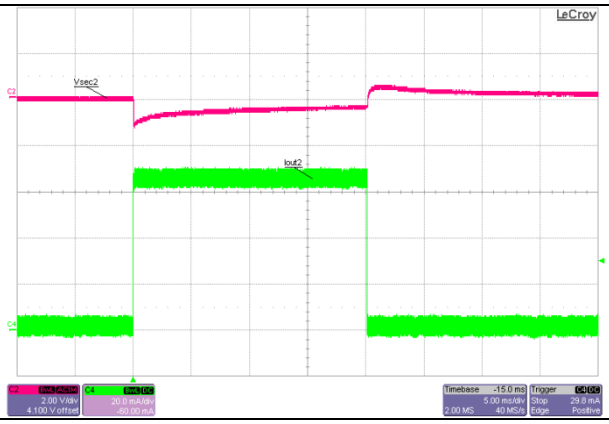


Vsec3 and VCC Startup at 14Vin with All Outputs at Full (65mA Constant Resistance) Load

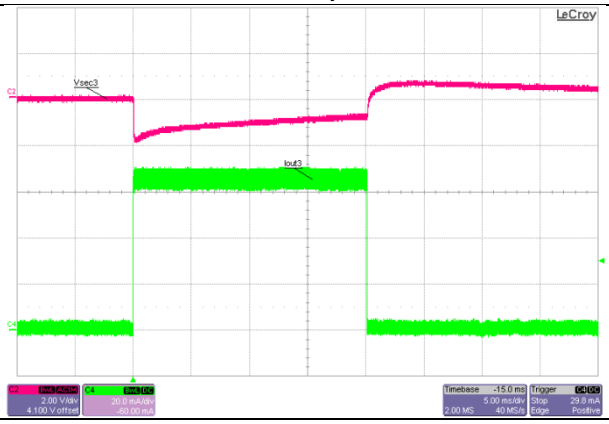
6.2 Load Transient Response



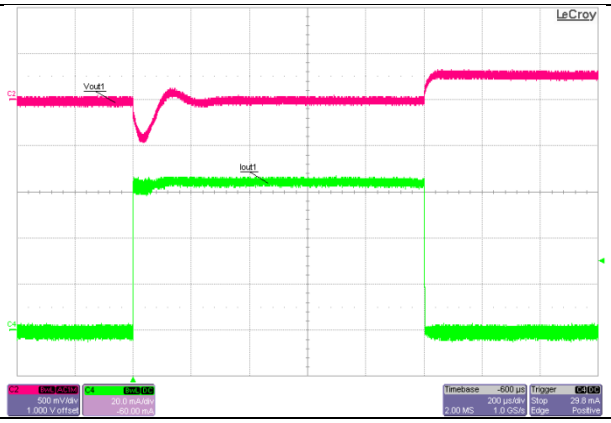
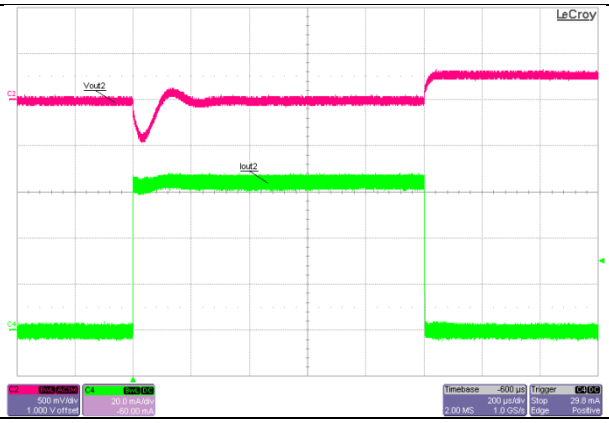
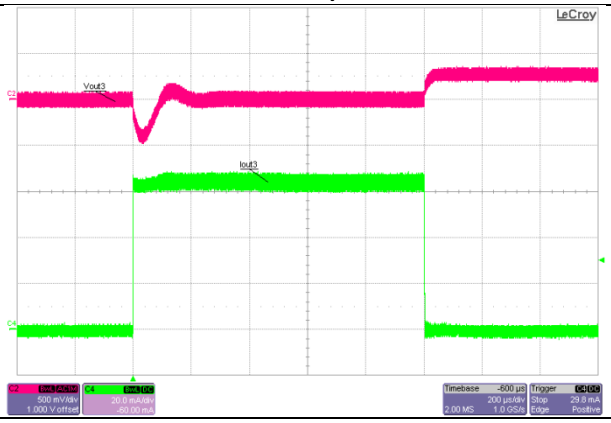
Load Transient Response on Rail 1 at 12Vin and 0mA-to-65mA (0%-to-100%) Load Step (All other outputs loaded at 65mA Constant Resistance Load)

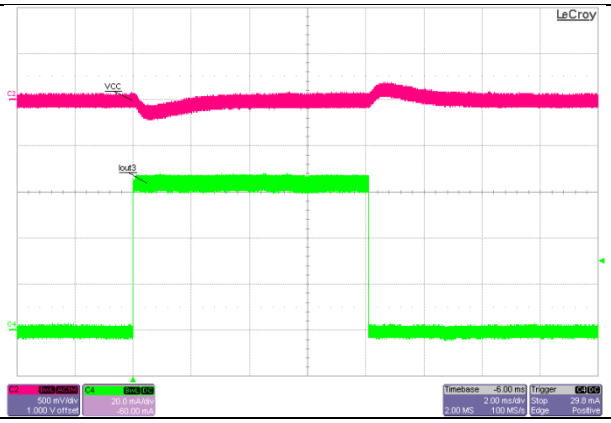


Load Transient Response on Rail 2 at 12Vin and 0mA-to-65mA (0%-to-100%) Load Step (All other outputs loaded at 65mA Constant Resistance Load)

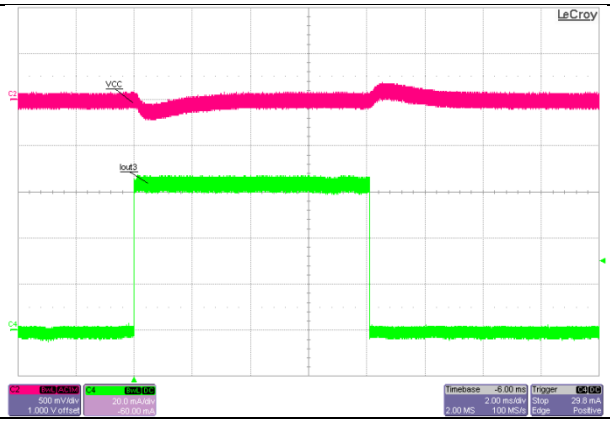


Load Transient Response on Rail 3 at 12Vin and 0mA-to-65mA (0%-to-100%) Load Step (All other outputs loaded at 65mA Constant Resistance Load)

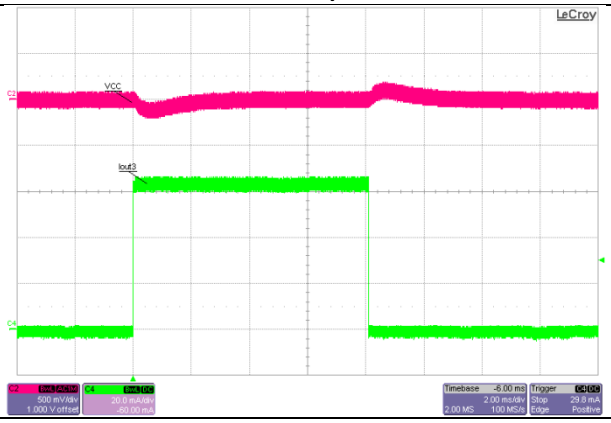
	
Load Transient Response on Vo1 at 12Vin and 0mA-to-65mA (0%-to-100%) Load Step (All other outputs loaded at 65mA Constant Resistance Load)	**Load Transient Response on Vo2 at 12Vin and 0mA-to-65mA (0%-to-100%) Load Step (All other outputs loaded at 65mA Constant Resistance Load)**
	
Load Transient Response on Vo3 at 12Vin and 0mA-to-65mA (0%-to-100%) Load Step (All other outputs loaded at 65mA Constant Resistance Load)	



Load Transient Response on Vo3 at 10Vin and 0mA-to-65mA (0%-to-100%) Load Step (All other outputs loaded at 65mA Constant Resistance Load)

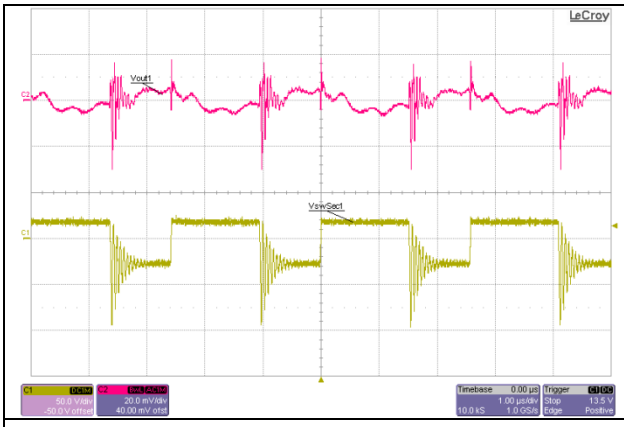


Load Transient Response on Vo3 at 12Vin and 0mA-to-65mA (0%-to-100%) Load Step (All other outputs loaded at 65mA Constant Resistance Load)

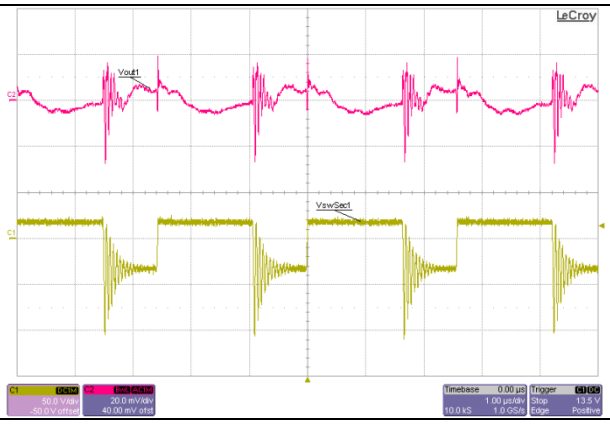


Load Transient Response on Vo3 at 14Vin and 0mA-to-65mA (0%-to-100%) Load Step (All other outputs loaded at 65mA Constant Resistance Load)

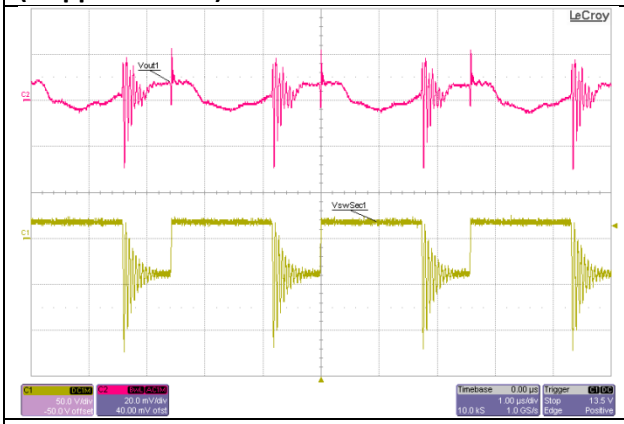
6.3 Output Voltage Ripple and Switch Node Voltage



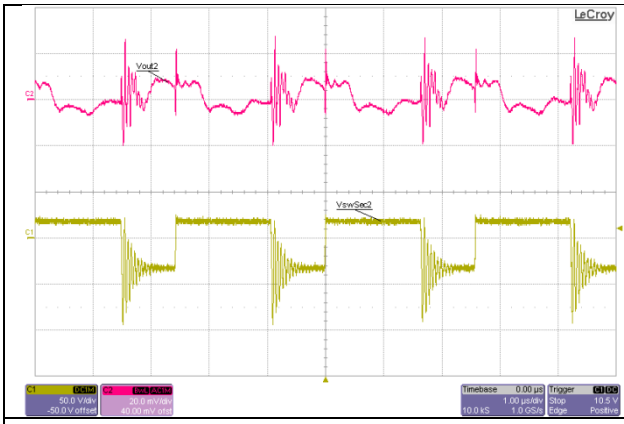
VswSec1 and Vo1 Ripple at 10Vin and All Outputs at Full (65mA Constant Resistance) Load (Vripple ≈ 48mV)



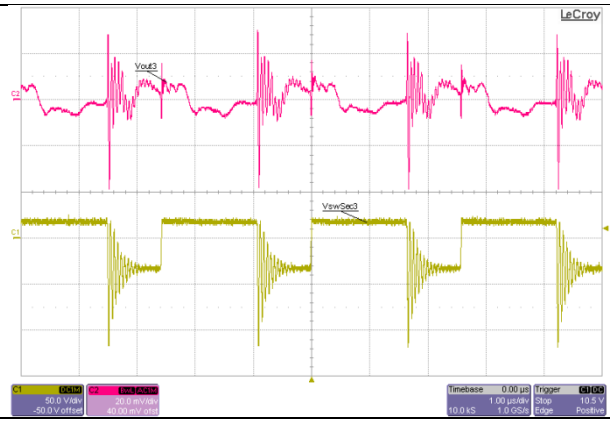
VswSec1 and Vo1 Ripple at 12Vin and All Outputs at Full (65mA Constant Resistance) Load (Vripple ≈ 48mV)



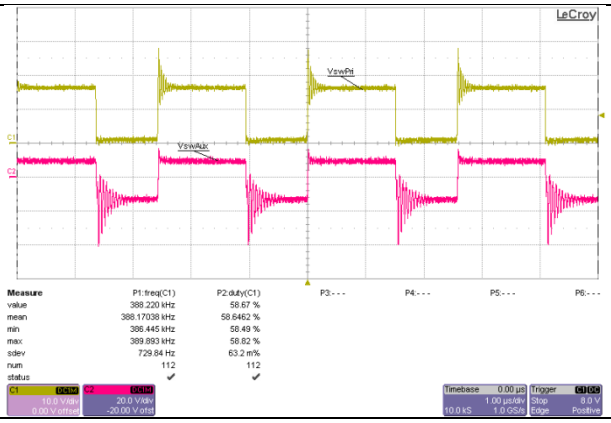
VswSec1 and Vo1 Ripple at 14Vin and All Outputs at Full (65mA Constant Resistance) Load (Vripple ≈ 56mV)



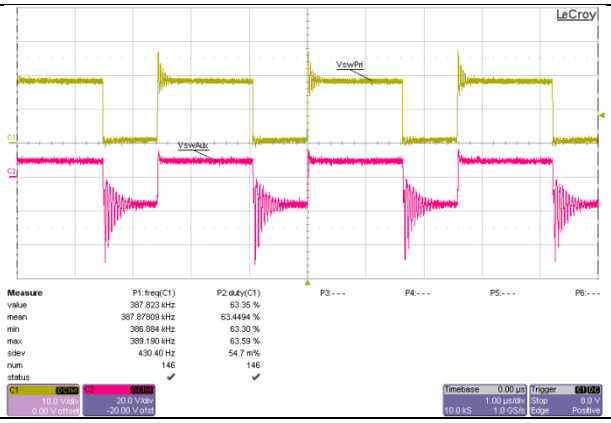
VswSec2 and Vo2 Ripple at 12Vin and All Outputs at Full (65mA Constant Resistance) Load (Vripple ≈ 48mV)



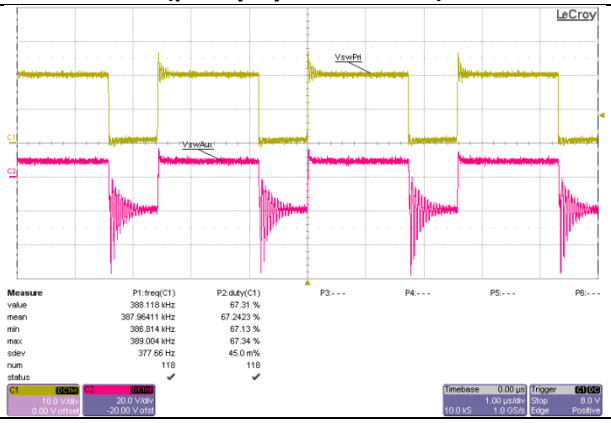
VswSec3 and Vo3 Ripple at 12Vin and All Outputs at Full (65mA Constant Resistance) Load (Vripple ≈ 68mV)



VswPri and VswAux at 10Vin and All Outputs at Full (65mA Constant Resistance) Load (µDuty Cycle ≈ 41.35%)



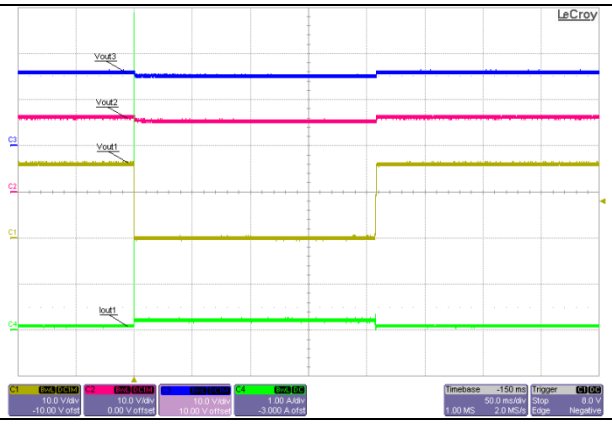
VswPri and VswAux at 12Vin and All Outputs at Full (65mA Constant Resistance) Load (µDuty Cycle ≈ 36.55%)



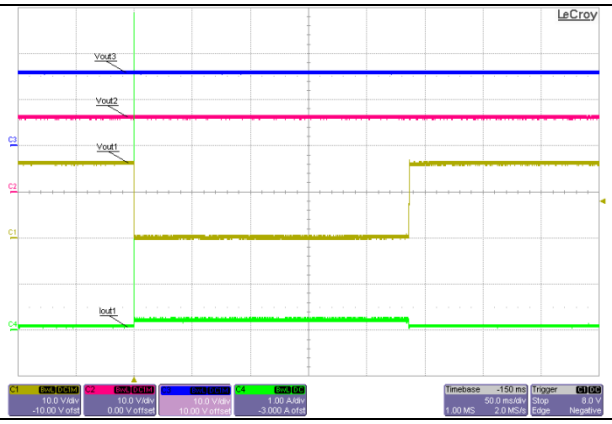
VswPri and VswAux at 14Vin and All Outputs at Full (65mA Constant Resistance) Load (µDuty Cycle ≈ 32.76%)

***NOTE: Due to the topology being a Flyback, the actual duty cycle is 100% subtracted by the duty cycle displayed in the waveforms.**

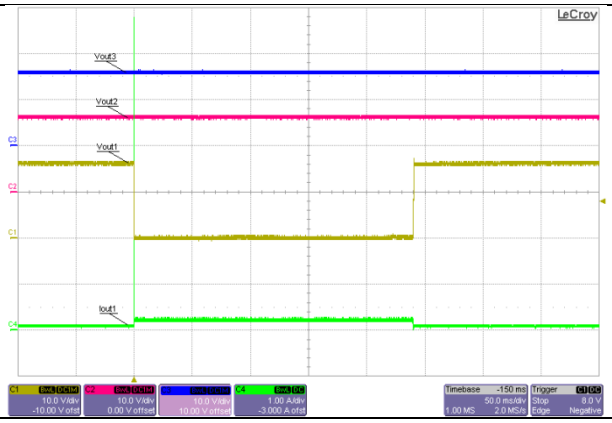
6.4 Short Circuit



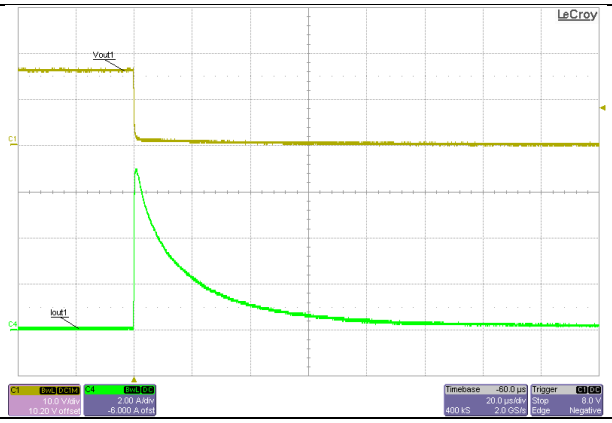
Vo1 Short Circuit Application and Recovery at 10Vin from/into Full (65mA Constant Resistance) Load with All Other Rails Loaded at Full (65mA Constant Resistance) Load*



Vo1 Short Circuit Application and Recovery at 12Vin from/into Full (65mA Constant Resistance) Load with All Other Rails Loaded at Full (65mA Constant Resistance) Load*



Vo1 Short Circuit Application and Recovery at 14Vin from/into Full (65mA Constant Resistance) Load with All Other Rails Loaded at Full (65mA Constant Resistance) Load*

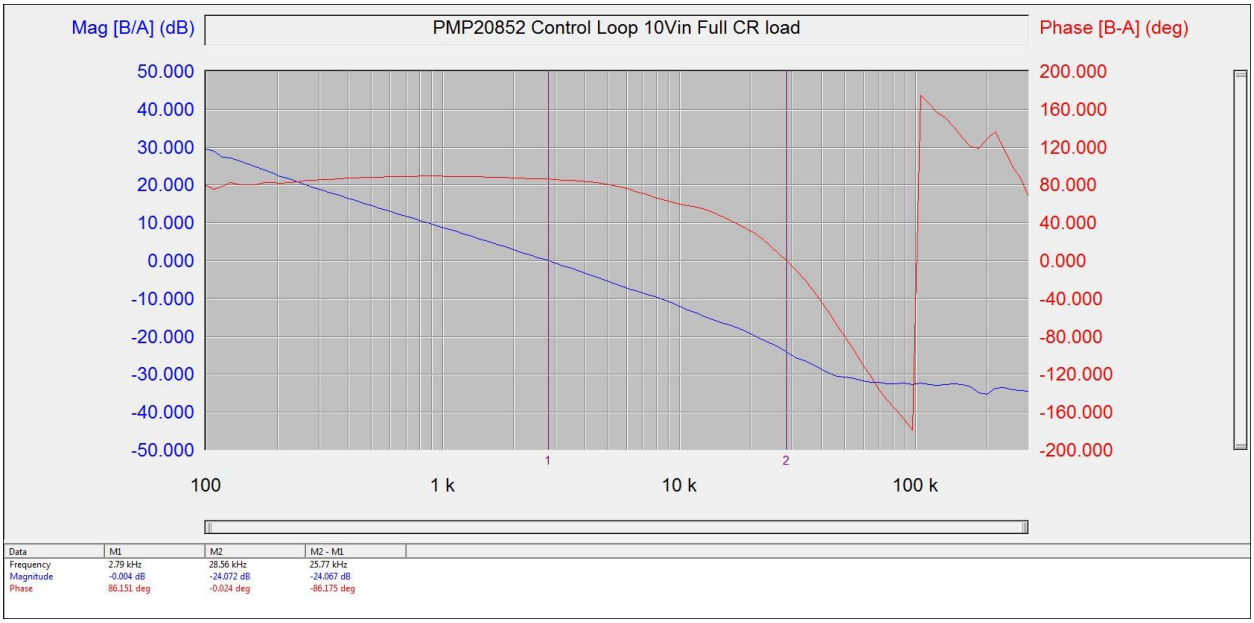


Zoomed-in waveform of output current during short circuit. The output current during the short peaks at about 7A (i.e. peak power is calculated as: $P_{pk} = I^2R = (7A)^2(2\Omega) = 98W$ peak**

***NOTE1: Short circuit/over-current conditions should be transient and not sustained. If overcurrent or short circuit conditions are sustained, the LP2951 LDO temperature will rise very rapidly and the device will go into thermal shutdown.**

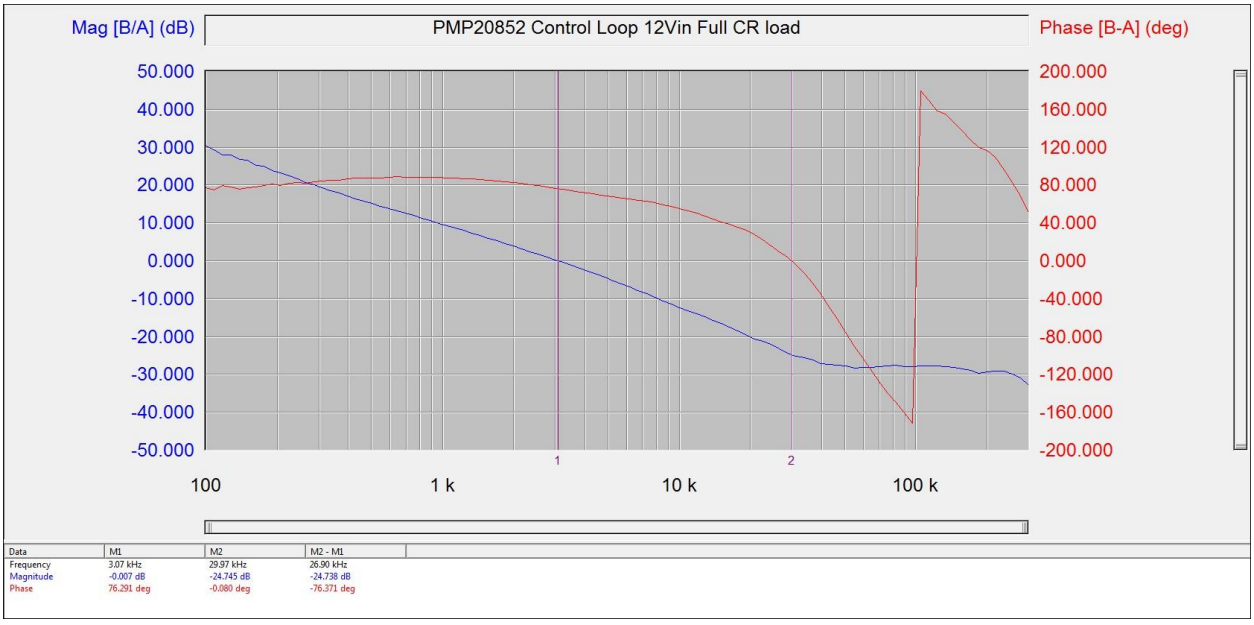
****NOTE2: This is why x2-paralleled 4.02Ω resistors (1206-package; Imperial) were used in the design. The original 0603-package 2Ω resistors were failing due to this peak pulse of power. A single 2Ω resistor with a larger package (i.e. 2010-package; Imperial; check manufacturer's datasheet to confirm) the ratings of which can sustain peak pulses of power reach ≈ 100W for ≈ 4µsec.**

6.5 Loop Response



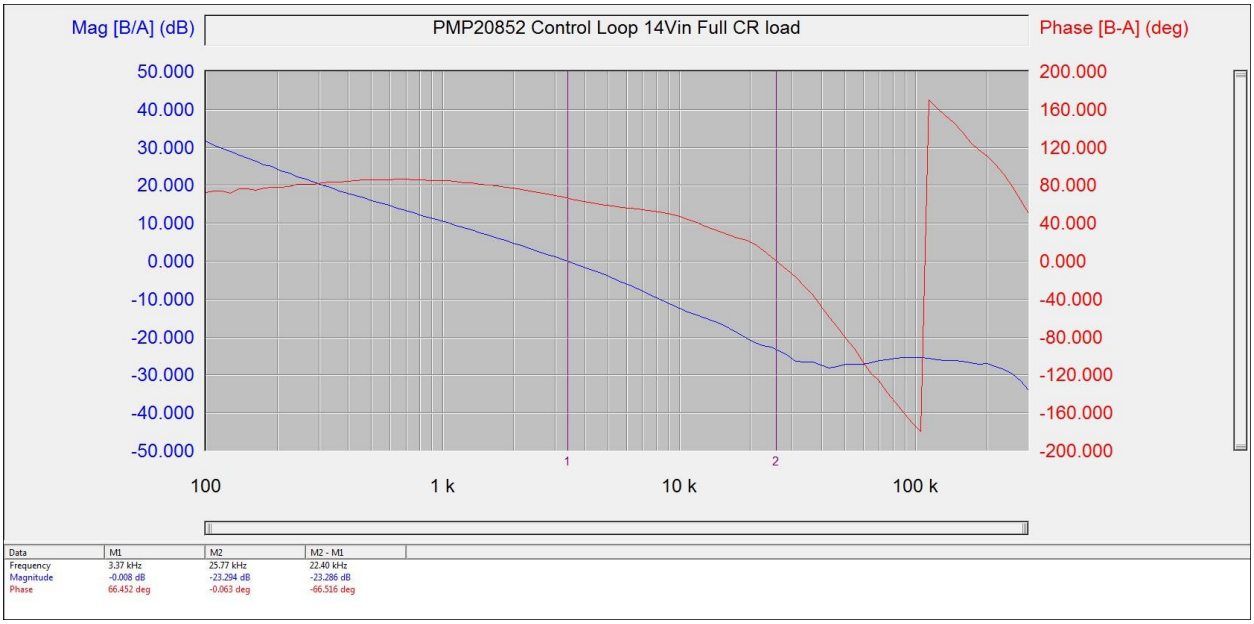
Loop Response at 10Vin and All Outputs Fully Loaded (at 65mA Constant-Resistance Load Each)

Crossover Frequency = 2.79KHz; Phase Margin = 86.2deg.; Gain Margin = -24.1dB



Loop Response at 12Vin and All Outputs Fully Loaded (at 65mA Constant-Resistance Load Each)

Crossover Frequency = 3.07KHz; Phase Margin = 76.3deg.; Gain Margin = -24.7dB



Loop Response at 14Vin and All Outputs Fully Loaded (at 65mA Constant-Resistance Load Each)

Crossover Frequency = 3.37KHz; Phase Margin = 66.5deg.; Gain Margin = -23.3dB

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