Design Guide: TIDA-010231

Analog Front End for Arc Detection in Photovoltaic Applications Reference Design

Description

This reference design implements a 4-channel analog front-end for DC arc detection in photovoltaic systems, supporting DC voltages up to 1000 V and currents up to 10 A. Arcing is detected by analyzing the AC noise present on the DC current between the solar panels and inverter. The signal is acquired by a current transformer, conditioned by an analog filter stage and sampled by an internal 12-bit ADC of the MCU or the 16-bit ADC ADC8363, before the frequency analysis is done with a C2000™ real-time microcontroller. This design is compatible with different C2000 controlCARDs, which allows adjustment to the MCU to the system. The internal ADC of the C2000 MCU can be evaluated by using a bypass option of the ADS8363.

Resources

TIDA-010231	Design Folder
ADS8363, OPA4322	Product Folder
TMDSCNCD280049C	Tool Folder
TPS562202, TPS745, TPS25947	Product Folder
TLV733P, REF5025	Product Folder

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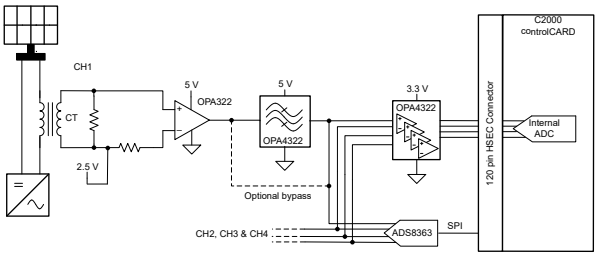
Features

- Four independent channels for arc detection
- DC voltages of 1000 V and DC currents up to 10 A
- Evaluation of external and internal ADC
- Industrial temperature range (–40°C to +85°C)
- Flexible C2000 MCU selection, due to 120-pin HSEC standard connector for multiple C2000 controlCARDs, also compatible with 180-pin HSEC connector controlCARDs
- Adjustable arc detection software for system optimization available in DigitalPower-SDK

Applications

- Solar arc protection
- String inverter
- Micro inverter
- Smart combiner box
- Central inverter



1 System Description

With the increasing amount of solar installations, safety concerns get ever more important. Arcing between high-voltage lines must be detected and the solar string must be de-energized to prevent hazards like electrical shock or fire. Therefore, standards like UL 1699B demand arc-fault protection circuits for all solar systems with rated voltages below 1500 V. This reference design is intended to show a possible implementation for an analog front end for such arc detection purposes. The design does not fulfill the UL 1699B standard by itself.

DC arcing causes an AC noise current in the cabling between a PV string, which is present in a wide spectrum up to several MHz. In this design, a frequency range of 30 kHz to 100 kHz is selected for the arc detection. This range can be restricted further by modifying the band-pass filter or the software, to avoid frequencies with known noise, like the switching frequency of the solar inverter. The signal chain consists of the following parts:

- Isolated current measurement
- Band-pass filter
- Analog-to-digital conversion
- Arc detection algorithm

1.1 Isolated Current Measurement

For the isolated current measurement, a current transformer (CT) is used. This approach has two advantages. First, it provides the necessary isolation from the high DC link voltages and second, it filters out the DC component of the current, which is not of interest for the arc detection. An important point is to consider the saturation behavior of the CT for the high DC current of up to 10 A. To interface the voltage drop on the burden resistor to the voltage level of the filter stage and ADC a first gain stage is implemented, which also introduces a bias to signal to convert the CT output into a unipolar signal. Since the switching frequency of the inverter typically lies inside the pass band of the CT, the gain of this first amplification stage has to be adjusted in a way that the ripple current does not drive the amplifier stage into saturation.

1.2 Band-Pass Filter

To limit the spectrum of the acquired signal, a band-pass filter is implemented. Since a solar inverter system can be a noisy environment, a 4th order low-pass filter and a 4th order high-pass filter is selected. The separate structure is chosen, to easily adjust upper and lower boundaries of the frequency range. Design this filter in a way to filter out the switching frequency as well other noise sources. In this design a frequency band of 30 kHz to 100 kHz is selected, but the frequency band must specifically be adjusted for each application.

1.3 Analog-to-Digital Conversion

This design offers the evaluation of an external ADC and the internal ADC of the C2000 MCU. In general, the ADC has to sample with at least double the frequency of the analyzed frequency range, to fulfill the sampling theorem. With a frequency band of 30 kHz to 100 kHz, a sampling speed of 250 kSPS is selected in this design. Furthermore, up to four independent channels have to be sampled continuously, which means a sampling speed of 1 MSPS is required as a minimum. As an external ADC, the ADS8363 is chosen. This 8-channel 16-bit device allows sampling with up to 2 MSPS and is interfaced via SPI to the C2000 MCU. As an alternative the internal ADC of the C2000 MCU can be used. The specifications on the internal ADC vary between versions. The TMS320F280049C, for example, provides three 3.45 MSPS 12-bit ADCs, which support 7 inputs each.

1.4 Arc Detection Algorithm

The arc detection algorithm is based on a frequency domain analysis. Therefore, the AC noise in a defined frequency range is determined. In case of arcing, this noise increases because of the inflicted arcing noise. In this design a 120-pin HSEC connector is used, because it allows connection to different C2000 controlCARDs. This approach allows connection to a variety of C2000 controlCARDs, to select the best fitting MCU depending on the number of arc detection channels needed and other tasks the MCU might have to perform in the system.

1.5 Key System Specifications

Table 1-1 details the key system specifications.

Table 1-1. Key System Specifications

PARAMETER	SPECIFICATION	COMMENT
Maximum DC voltage	1000 V	
Maximum DC current	10 A	Limited by CT current capability and saturation behavior
Frequency band for arc detection	10 kHz to 100 kHz	Modifiable with analog filter and software
Sampling rate per channel	250 kSPS	Can be modified for higher frequency bands
Number of channels	1 to 4	Depends on C2000 controlCARD used
ADC resolution	16-bit (ADS8363)	Optional a C2000 internal ADC can be used
Auxiliary supply voltage	8 V to 16 V	
Interface ADS8363 to C2000	1 SPI module per 2 active channels	Custom SPI, as described in the *Interfacing to the ADS8363 Pseudo-Differential Operating Mode* application note

CAUTION

Do not leave the design powered when unattended.

WARNING

High voltage! *Accessible high voltages are present on the board.* Electric shock is possible. The board operates at voltages and currents that may cause shock, fire, or injury if not properly handled. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property. For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

TI considers it the user's responsibility to confirm that the voltages and isolation requirements are identified and understood before energizing the board or simulation. *When energized, do not touch the design or components connected to the design*.

WARNING

Hot surface! Contact may cause burns. Do not touch!

Some components may reach high temperatures > 55°C when the board is powered on. Do not touch the board at any point during operation or immediately after operating, as high temperatures may be present.

WARNING

TI intends this reference design to be operated in a ***lab environment only and does not consider it to be a finished product*** for general consumer use. The design is intended to be run at ambient room temperature and is not tested for operation under other ambient temperatures.

TI intends this reference design to be used only by ***qualified engineers and technicians*** familiar with risks associated with handling high-voltage electrical and mechanical components, systems, and subsystems.

There are ***accessible high voltages present on the board***. The board operates at voltages and currents that may cause shock, fire, or injury if not properly handled or applied. Use the equipment with necessary caution and appropriate safeguards to avoid injuring yourself or damaging property.

2 System Overview

2.1 Block Diagram

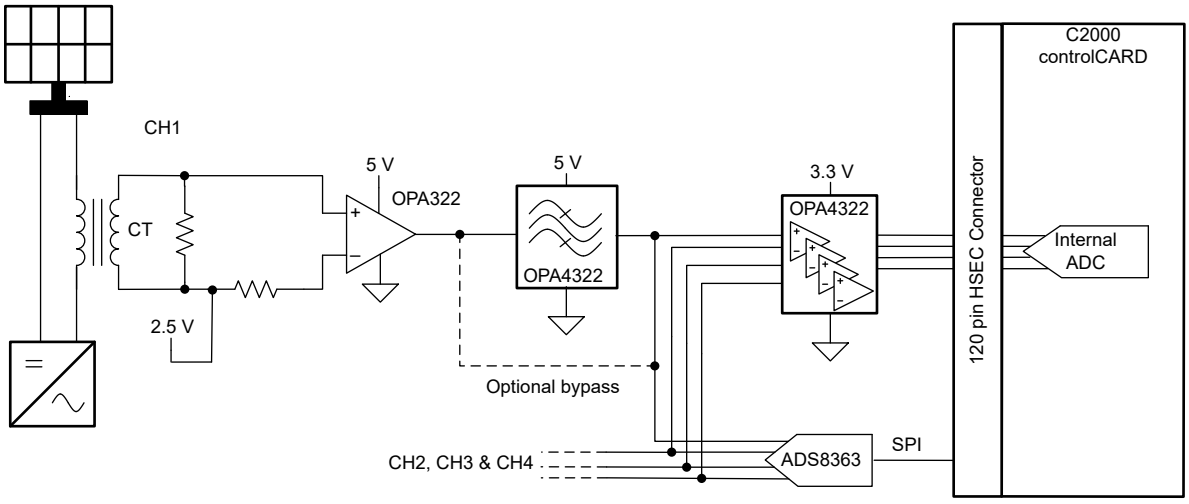


Figure 2-1. System Block Diagram

2.2 Design Considerations

2.2.1 Current Transformer Circuit

For sensing the AC noise on the DC current between solar string and inverter a current transformer (CT) based approach is selected. This has the advantage that the large DC component which is not of interest for the arc detection is filtered out right away. Since a large DC current is fed through the CT, the saturation behavior is very important. For higher DC currents gapped ferrite cores or powdered metal cores with lower permeability might be required. The circuit shown in Figure 2-2, consists of the CT, some passive components, and an amplifier. The burden resistor R5 is selected with 200 Ω according to the data sheet, which leads to a current to voltage ration of 1:1 for the AC components within the frequency band of the CT, which is 10 kHz to 200 kHz. The passives afterward are used for protection of the amplifier and to introduce a bias voltage of 2.5 V. The amplifier circuit introduces a gain of 10, to fit the output signal to the input voltage range of the following filter section. This gain can be reduced in case of bigger AC components present.

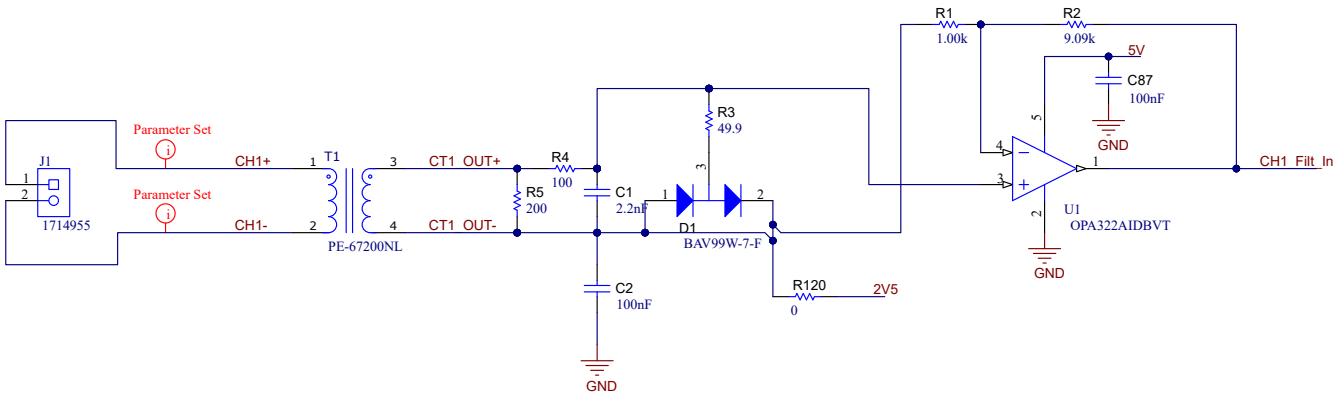


Figure 2-2. Schematic Current Transformer Circuit and Gain Stage

2.2.2 Analog Band-Pass Filter

The filter stage shown in Figure 2-3 consists of an OPA4322, 4-channel operational amplifier. U6A and U6B form a low-pass filter with a cutoff frequency at 100 kHz. U6C and U6D form a high-pass filter with a cutoff frequency of 30 kHz. In combination, this forms a band-pass filter with a pass band of 30 kHz to 100 kHz. The split topology of low-pass plus high-pass filters is selected to make it easy to adjust upper and lower levels of the band-pass filter separately.

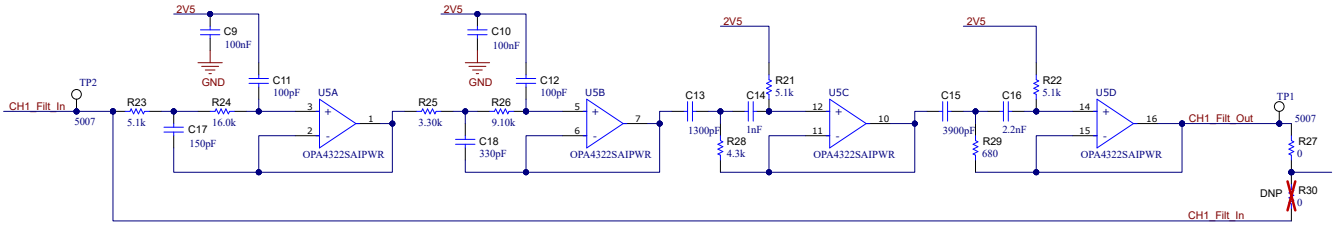


Figure 2-3. Schematic Filter Stage

The two most important specifications of an amplifier in an active filter application are Gain-Bandwidth-Product (GBW) and slew rate (SR).The minimum requirements for GBW and SR are given in Equation 1 and Equation 2.

$$GBW_{min} = 100 \times G \times f_c \quad (1)$$

$$SR_{min} = 2 \times \pi \times f_c \times V_{P-P} \quad (2)$$

where

- G = closed-loop gain
- f_c= cutoff frequency of the low pass filter
- V_{P-P}= peak-to-peak output voltage

With the values of G = 1, f_c = 100 kHz and V_{P-P} = 5 V a minimum GBW of 10 MHz and a minimum slew rate of 3.14 V/µs are calculated. With a GBW of 20 MHz and a slew rate of 10 V/µs the OPA4322 fulfills these criteria and allows for some head room if a higher frequency band is desired. The transfer function of the filter is validated using the PSpice for TI simulation tool. The gain of the filter stage is plotted in Figure 2-4. The output of this filter is connected to the external ADC ADS8363 as well as to the internal ADC, via another amplifier which takes care of the voltage level translation from 5 V to 3.3 V for the C2000 MCU.

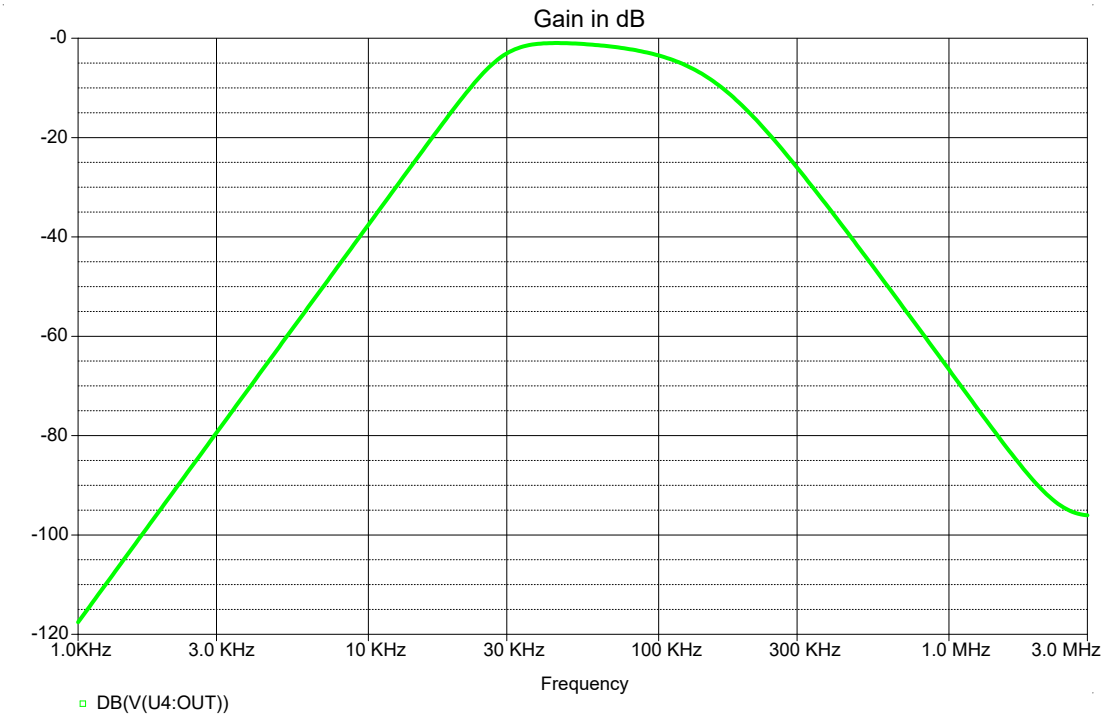


Figure 2-4. Simulated Magnitude of the Frequency Response of the Filter Stage

2.2.3 Analog-to-Digital Conversion

As a next step, the filtered signal is converted to the digital domain. This is done either by the external ADC ADS8363 or by an internal ADC of the C2000 MCU. In case of the ADS8363, only four of the eight channels are used. The outputs of the filters are connected to channel CHA0, CHA1, CHB0, and CHB1 with an additional

anti-aliasing filter. The unused inputs are tied to ground. CMA and CMB are the common-mode inputs for channel A and B and are connected to the 2.5-V reference voltage provided by the REF5025, which is also used as reference for the ADC and for biasing the signal after the CT. The SPI of the ADS8363 allows for two data lines, which is necessary to achieve the required data rate if more than two channels of arc detection are implemented. A guide on how the ADS8363 SPI with two data lines is implemented is found in the *Interfacing to the ADS8363 Pseudo-Differential Operating Mode* application note.

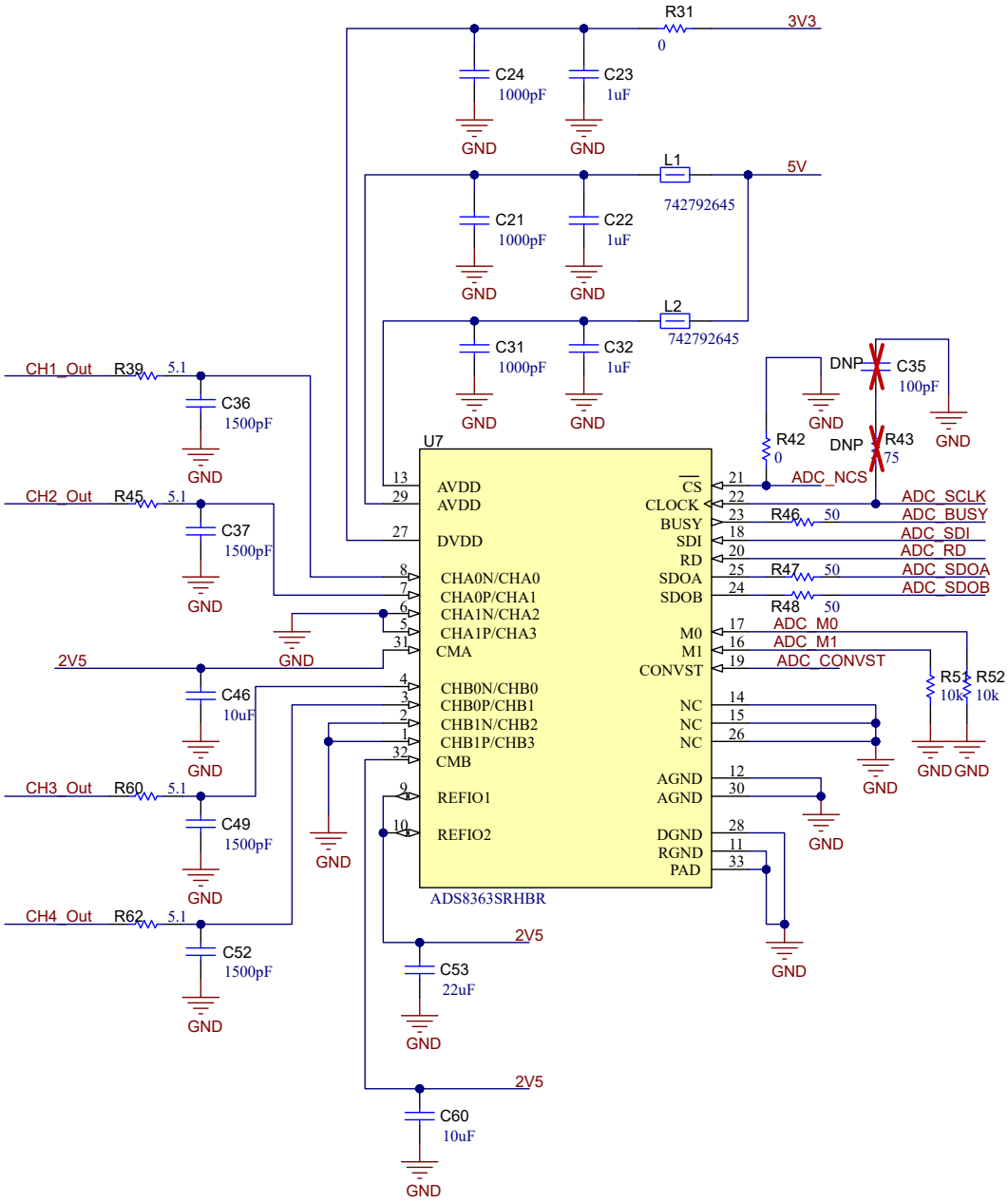


Figure 2-5. Schematic Analog-to-Digital Conversion With ADS8363

The required data rate in this design is calculated with Equation 3.

$$\text{Bitrate}_{\text{min}} = \text{Number of Channels} \times f_s \times \text{Bits per Sample} \quad (3)$$

where

- f_s = sampling rate

With a sampling rate of 250 kSPS, a maximum number of 4 channels and a 22 bits per sample as shown in the previously-mentioned application note, a bit rate of 22 MBit/s is the result. Since the maximum SPI clock frequency f_{SPI} of the ADS8363 is 20 MHz, there are both data lines necessary to achieve the required bit rate for four-channel operation. The easiest way to adjust the bit rate and therefore the sampling rate is to do continuous sampling with the ADS8363 and just modify the SPI clock, since this clock is used for conversion and data transmission. The SPI clock frequency is calculated with Equation 4.

$$f_{SPI} = \frac{\text{Bitrate}}{\text{Number of data lines}} \tag{4}$$

where

- Number of data lines can be either 1 or 2

With the maximum bit rate of 22 MBit/s and 2 data lines used, a SPI clock frequency f_{SPI} of 11 MHz is the result. As another example if only one channel is used a bit rate of 5.5 MBit/s is required which is then implemented only using one data line and f_{SPI} of 5.5 MHz.

For improving signal quality, series termination is implemented for all SPI signals as well as an AC termination for the clock signal. The chip select signal is pulled low permanently, since a continuous sampling is implemented.

In case the internal ADC of the C2000 is used, the filter output signals are connected to a level-shifting stage, which is implemented by another OPA4322. It simply translates the 5-V level to a 3.3-V level before connecting the signals to the analog inputs on the controlCARD connector.

2.2.4 Power Supply

For the power supply an axillary supply voltage between 8 V and 16 V is necessary. Overvoltage and reverse polarity protection are implemented by using the TPS259474 eFuse. By selecting R104, R105, R112, and R113 as shown in Figure 2-6. The undervoltage lockout is set to 7.88 V, the overvoltage lockout is set to 16.15 V and the current limit is set to 0.59 A. For the exact design procedure refer to the device data sheet. A Zener diode is added to the output to protect against fast voltage transients.

There are three voltage rails necessary for this design. The first is a 5.25-V supply which is used to power the C2000 controlCARD. For this, the input voltage is stepped down using the TPS562202 buck converter. With the used values of R107 and R114 the output voltage results in 5.32 V which is slightly higher than the desired 5.25 V. The C2000 controlCARDs allow for maximum input voltage of at least 5.5 V. The 5.25-V rail is also used to generate a 5-V analog supply for the ADC and the filter stage with TPS745 as well as a 3.3-V rail for the digital supply of the ADC with TLV33P. To each supply rail a LED is added to indicate the successful power up.

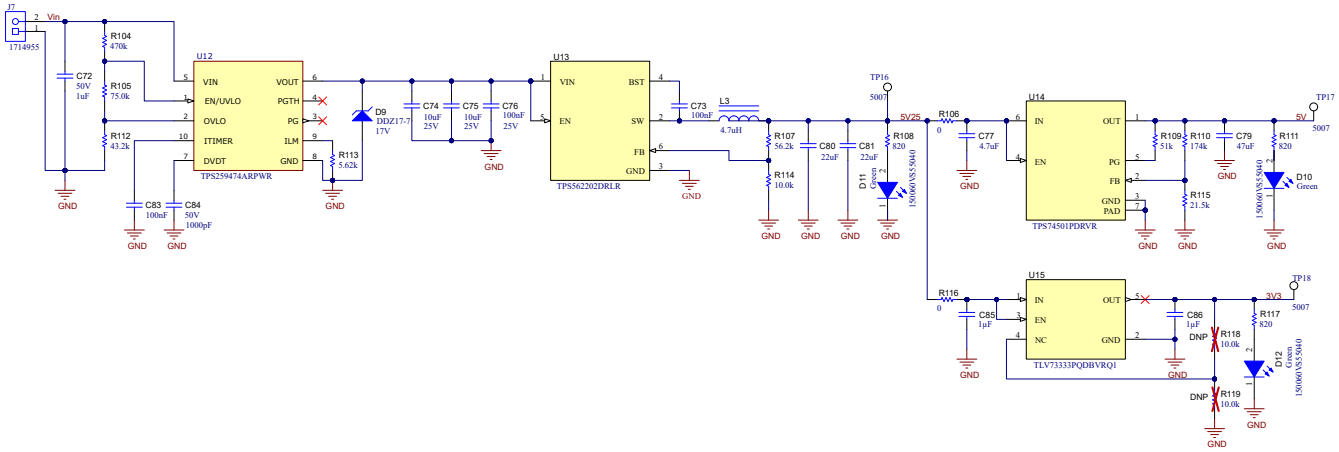


Figure 2-6. Schematic Power Stage

2.2.5 Debugging and Status Indication Options

For debugging and status indication, there are a few different options in this design. First, there are three LEDs for the 5.25-V (D11), 5-V (D10), and 3.3-V (D12) supply voltages and four additional LEDs (D5, D6, D7, and D8) added, which are controlled via GPIOs of the C2000 controlCARD. Additionally, there are two DAC channels routed from the C2000 controlCARD to connector J6, which is used for the indicated different states as well. Additionally, there is one GPIO signal and GND connected to J6, where the GPIO is used for an external interrupt to start the arc detection or as an error output to a different part of the system. Resistors R100, R101, R102, and R103 can be populated in a different way to indicate different versions of the PCB to the software. These debugging and indication options are not implemented in the available software yet. Table 2-1 gives an overview of the debugging options and the related GPIOs and pin numbers they are connected to with a short summery of the function.

Table 2-1. Debugging and Status Indication Overview

PARTS	GPIO NUMBER	HSEC PIN NUMBER	FUNCTION
D11	-	-	Status indication of 5.25-V supply
D10	-	-	Status indication of 5-V analog supply
D12	-	-	Status indication of 3.3-V supply
D5	GPIO37	58	Generic status LED (unused by default)
D6	GPIO35	60	Generic status LED (unused by default)
D7	GPIO39	62	Generic status LED (unused by default)
D8	GPIO23	64	Generic status LED (unused by default)
J6 Pin 1	-	-	GND
J6 Pin 2	-	11	DACA output (unused by default)
J6 Pin 3	-	9	DACB output (unused by default)
J6 Pin 4	GPIO34	86	External input with pulldown (unused by default)
R100, R102	GPIO5	70	Optional board indication. R100 is pullup R102 is pulldown. Both are DNP by default
R101, R103	GPIO4	68	Optional board indication. R101 is pullup R103 is pulldown. Both are DNP by default

2.3 Highlighted Products

2.3.1 TPS259474

The TPS259474 eFuse was selected for this design for overvoltage and reverse polarity protection. The small footprint and programmable overvoltage lockout, undervoltage lockout, and maximum current offer simple and small sized circuit protection.

2.3.2 TPS562202

The TPS562202 is a simple, easy-to-use, 2-A synchronous buck converter in a SOT563 package. The device is optimized to operate with minimum external components and also optimized to achieve low standby current. Its input range up to 17 V covers most laboratory supply options. The switching frequency of 580 kHz does not interfere with the frequency band for arc detection.

2.3.3 TPS745

The TPS745 was selected because of its low drop out voltage, since the 5.25-V supply is only slightly higher than the 5-V analog supply needed for the ADC.

2.3.4 OPAx322

The OPAx422 is used for multiple purposes in this design. The most critical one is the filter stage, where it provides sufficient GBW and slew rate. The 4-channel device allows for a small layout. This device is also used for the gain stage and the 5-V to 3.3-V level translation. In these cases, the specifications are not too critical and the same device was selected to keep the BOM count low.

2.3.5 ADS8363

The ADS8363 offers a high 16-bit resolution in combination with a high channel count and up to 2-MSPS data rate at SPI speeds below 20 MHz. These specifications fit very fell for the arc detection application. The device allows for an accurate and flexible design, the higher data rate at lower SPI speed is helpful in combination with lower-end C2000 models since the SPI clock there is often limited to 25 MHz.

2.3.6 REF5025

The REF5025 is a low-noise, low-drift, very high precision voltage references with excellent line and load regulation.

2.3.7 TMDSCNCD280049C

This controlCARD contains the TMS320F280049C C2000 MCU, which is a mid-tier, single-core C2000 MCU. The device offers sufficient SPI modules and direct memory access (DMA) resources to implement the SPI towards the ADS8363 with a minimum of main CPU run time. This leaves most processing resources to the resource intensive arc detection algorithm. The 120-pin HSEC connector is common with a multiple of other C2000 control cards and also compatible with the 180-pin HSEC connector, which allows evaluation of other C2000 MCUs.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware and Software Requirements

3.1.1 Hardware

For the initial bring-up, one TIDA-010231 board and one TMS320F280049C controlCARD (TMDSCNCD280049C) are necessary.

The controlCARD setup is found in ControlCARD Configuration.

A DC power supply is necessary to provide an auxiliary supply of 8 V to 16 V to the screw terminal J7. If this connector is oriented to the bottom, the left terminal is GND and the right terminal is the supply voltage.

For the initial low-voltage testing, a function generator is used to provide a sinusoidal input to the primary of the CT. With this setup the different parts of the analog front end, like the band-pass filter and the ADC can be tested.

For system testing with arcs, a DC source or a photovoltaic (PV) emulator, a solar inverter, and an arc generator are necessary. This design supports currents up to 10 A and voltages up to 800 V. Since this is a high-voltage test, the necessary safety measures must be in place, to prevent any accidents or injuries.

Table 3-1 lists and describes all test points and connectors.

Table 3-1. Connectors and Test Points

CONNECTOR OR TEST POINT	DESCRIPTION
J1, J2, J3, J4	Inputs CH1, CH2, CH3, and CH4 are for arc detection. Connect these to the primary side of the current transformers. Connect in series with DC line between solar string and inverter. Can handle up to 10-A line current.
J5	120-pin HSEC connector for connecting different C2000 controlCARDs. Also compatible with 180-pin control cards.
J6	Debug connections. Pins 1 to 4 from left to right: GND, DACB, DACA, GPIO (GPIO34 for F280049C). DACA and DACB can be used for some feedback signaling (not implemented) and the GPIO can be used for an external interrupt. The GPIO has external pulldown.
J7	Power supply connection. Connect a voltage between 8 V and 16 V to this terminal. GND is the left pin and VCC is the right pin.
TP1	Filter output and ADC input of CH1
TP2	Filter input of CH1
TP3	Filter output and ADC input of CH2
TP4	Filter input of CH2
TP5	Filter output and ADC input of CH3
TP6	Filter input of CH3
TP7	Filter output and ADC input of CH4
TP8	Filter input of CH4
TP9	2.5-V voltage reference
TP10	DACA
TP11	DACB
TP12, TP13, TP14, TP15	GND
TP16	5.25-V power supply for C2000 controlCARD
TP17	5-V analog power supply
TP18	3.3-V digital supply voltage

3.1.2 Software

Test software for evaluating the internal ADC of the TMS320F280049C controlCARD is part of the DigitalPower-SDK. Request software for evaluating the external ADC via the My Secure Software portal. To run this software, the Code Composer Studio™ integrated development environment (IDE), version 11.0 or later versions as well as the C2000Ware SDK are required. Both are publicly available on ti.com.

A more detailed description of the software is found in the Software Users Guide, which is included with the downloadable software projects.

Find more details on how to use and install the software in Section 3.2.

3.1.2.1 Arc Detection Theory

The arc detection algorithm implemented in this design is an FFT-based arc detection algorithm. Arcing present in a PV system creates random noise current in the cabling used for the PV string. The current noise of the arc itself has a Gaussian distribution with a spectrum extending to several MHz. Because of the geometry of the cabling in a typical PV system, the noise current density above 200 kHz varies significantly with frequency. For this reason, a general frequency band between 10 kHz and 100 kHz is selected for arc detection. This is defined by the analog band-pass on the board. Since there are other noise sources like the inverter switching frequency with in this band, the software allows for further restrictions of this frequency band, by adjusting the ArcTuningParams present in the software. A description of the different tuning parameters is found in Table 3-2. The algorithm performs an FFT of the sampled signal and sums up the noise in the specified frequency band. This computed arc noise can be observed in the variable AD_result. This is performed for every 1024 samples. Since arcing causes noise over the whole frequency band, the AD_result value increases when arcing is present.

Table 3-2. Elements of ArcTuningParams structure and Their Description

NAME	DESCRIPTION
float32 ArcTuningParams.B	Analysis Bandwidth: bandwidth of the analysis frequency.
float32 ArcTuningParams.I	Min Frequency: initial frequency of the band.
float32 ArcTuningParams.F	Filter Weight: weighting for each half of the band.
float32 ArcTuningParams.D	Bin Discard Factor: number of spurious peaks to be discarded.
int16 ArcTuningParams.T	Threshold for arcing: Not used by default
int16 ArcTuningParams.C	Clipping Level: Not used by default
float32 ArcTuningParams.ADSampleRate	Sampling Rate: set to 250000 by default

- I - Min Frequency. The initial frequency of the band for arc-noise computation. The I value specifies the starting frequency of the band where the arc-noise is computed.
- B - Analysis Bandwidth. This bandwidth must be a number greater than 1.0 for proper operation. The computation of arc-noise is carried out till the frequency B + I. For instance, if I is set to 30000, and B is set to 30000, then the arc-noise is computed using the frequency components in the range of 30 kHz to 60 kHz and anything outside this band is not used.

Additional parameters used in the computation of the arc-noise are D and F. These parameters are used to eliminate spurious peaks that may occur that one may sometimes perceive as arc:

- D - Bin Discard Factor. This parameter specifies the number of spurious peaks to be discarded, it controls how aggressive the filtering is and must be a number be between [0.0, 1.0] for proper operation. Peaks within the band of frequencies set by B and I are eliminated for arc-noise computation based on the value set by D stating with the highest peaks. If D is higher more peaks are discarded, and if D is lower fewer peaks are discarded for computation. Note that changing D has an impact on the cycles consumed by the arc-noise computation algorithm. One needs to try different D values probably in the increment of 0.1 and see for real-world arcs how the arc-noise computation varies.
- F - Filter Weight. This parameter specifies the weighting for the first half of the analyzed frequency band and must be a number greater than 0.0 for proper operation. The first half of frequencies set by B and I are weighted by the filter weight while the second half of the band is always weighted by 1.
- T - Threshold. This parameter is currently not used and is a placeholder for a threshold value for AD_result where arcing is detected if this threshold is surpassed. Changing T has no effect.

- C - Clipping Level. This parameter allows a variable for detecting arc, but is not implemented currently. Changing C has no effect.
- ADSampleRate - Sampling Rate. This is the sampling rate of the system. In this design this rate is fixed to 250 kSPS and therefore this is set to 250000.

3.1.2.2 Software Implementation

This section describes the basic functionality of the example software. The example software for the internal ADC implementation is available in the DigitalPower SDK. Request software supporting the ADS8363 from MySecureSoftware. This software is just for evaluation, since it only computes the arc noise in the defined frequency band, but does not implement any conditions or thresholds to indicate if there is arcing or not. The computed arc noise can be observed in the variable AD_result. With correct setup this value increases during an arcing condition.

The software implementation differs between the projects for evaluating the intern or the external ADC, but the general idea is the same. The software reads 1024 samples from the ADC and passes these samples then to the arc detection algorithm. Nearly all the sampling and data manipulation is done using background resources like the Direct Memory Access (DMA), to make sure that the arc detection is running continuously. The sampled data is stored in an array called CH1Data with the size of 1024. As soon as this array is filled up it is passed to the arc detection algorithm, which copies the values into a different memory location, to allow the CH1Data array to be filled up again by the DMA in the background, without corrupting the data used by the arc detection algorithm running in the foreground.

More details on how to control the software and how to observe these variables are found in Section 3.2.

3.2 Test Setup

3.2.1 ControlCARD Configuration

Every controlCARD has switches installed for configuring different pin assignments and other connections on the board. For proper operation these switches have to be configured correctly before inserting the controlCARD to the TIDA-010231 board and powering up. Table 3-3 shows the configurations for the TMS320F280049C controlCARD TMDSCNCD280049C. Up and down and right and left position are referred to the orientation where the HSEC connector of the control card is oriented downwards.

Table 3-3. TMDSCNCD280049C Switch Configuration

SWITCH	SETTING	COMMENT
S1:A	Switch 1 ON, switch 2 OFF	Enable USB JTAG and disable USB UART
S1 (installed with 180-degree rotation)	Switch 1 and switch 2 up position	Select Flash or USB boot mode
S2	Up position	Connect GPIO 10 to HSEC pin 60
S3 (installed with 180-degree rotation)	Down position	Connect GPIO 8 to HSEC pin 58
S4	Down position	Use standard 4-pin JTAG
S5 (installed with 180-degree rotation)	Switch 1 and switch 2 up position	Connect GPIO 25 to HSEC pin 77 and connect GPIO 24 to HSEC pin 75
S6	Switch 1 and switch 2 down position	Connect GPIO 26 to HSEC pin 79 and connect GPIO 27 to HSEC pin 81
S7	All switches in the up position	Connect internal ADC to HSEC Connector
S8 (installed with 90-degree rotation)	Switch 1 and 2 left position	Use internal voltage reference for all internal ADCs. Only applicable for use of internal ADCs.

3.2.2 Setup for Hardware and Software Validation

With the setup developed, the hardware and software can be validated in a low-voltage environment. The following hardware is required:

The hardware setup is illustrated in Figure 3-1.

- One TIDA-010231 board
- C2000 controlCARD TMDSCNCD280049C
- DC power supply to provide 8-V to 16-V auxiliary supply to J2. Limit the current to 0.5 A. Refer to Figure 3-1 for polarity.

- Function generator to provide a sinusoidal signal to the CH1 input J4 with variable frequency up to 100 kHz
- Oscilloscope to observe waveforms at the filter test points
- PC with Code Composer Studio software to observe sampled waveforms and the output of the arc detection algorithm.

The software project can be imported directly from the DigitalPower SDK into the Code Composer Studio IDE. (internal ADC software).

Detailed instructions on how to control the software are found in the User's Guide PDF document included in the downloaded package.

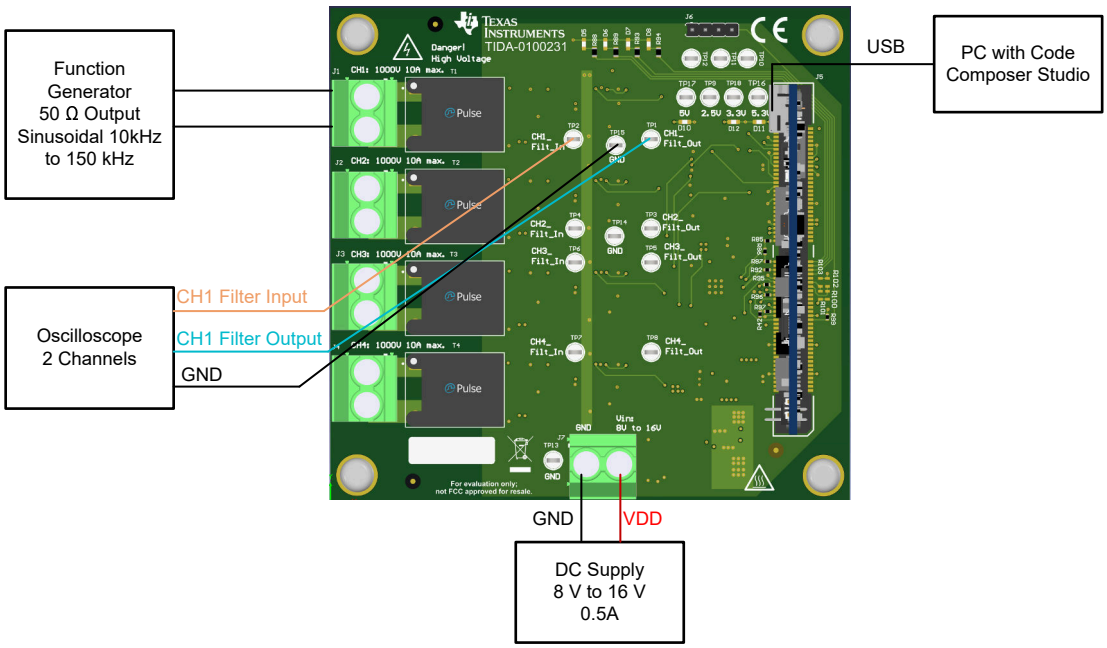


Figure 3-1. Hardware and Software Validation Setup

3.2.3 Setup for Arc Testing

For the actual arc detection setup, the following hardware is necessary:

- One TIDA-010231 board
- C2000 controlCARD TMDSCNCD280049C
- DC power supply to provide 8-V to 16-V auxiliary supply to J2. Limit the current to 0.5 A. For polarity refer to Figure 3-2
- DC source or PV emulator in the role of a solar panel or solar string
- Solar inverter (for which the arc detection is optimized)
- Arc generator, for producing arc faults in a controlled way
- All necessary safety equipment to do these high-voltage arcing experiments in safe environment

WARNING

High voltages and high currents are present in this experiment to produce open arcs. Take all the necessary protective measures to prevent harm. Put the arc generator as well as the arc detection board inside a safety box, to prevent contact to high voltages. Make sure that all conductors carrying high voltages are protected against touch.

Figure 3-2 shows the block diagram of the arc detection test setup.

The software setup is identical to the hardware validation setup.

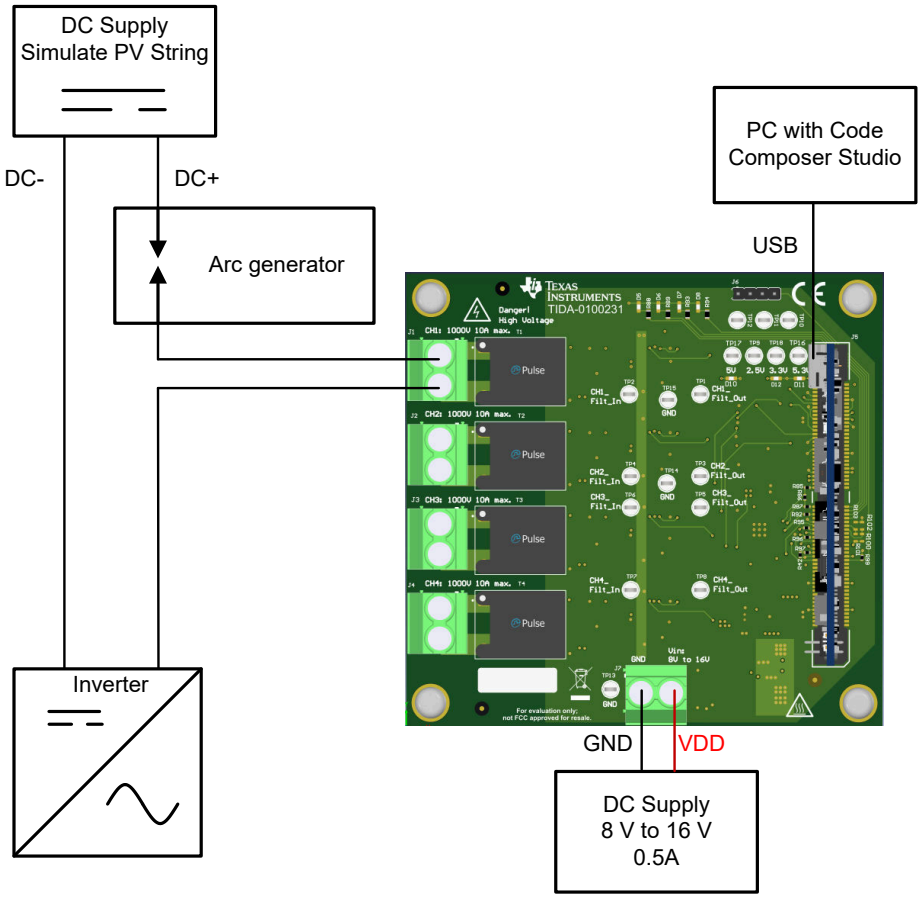


Figure 3-2. Arc Detection Test Setup

3.3 Test Results

3.3.1 Test Results of Hardware and Software Validation

Figure 3-1 shows the setup used for this test. There are sinusoidal input signals with different frequencies applied to the CH1 input and the sampled signal. The computed arc noise is observed within Code Composer Studio. Figure 3-3 and Figure 3-4 show the *Expressions* window for the external ADC version and for the internal ADC version after loading the software to the controlCARD, but before starting the code.

Variables | Expressions | Registers

Expression	Type	Value	Address
CH1Data	int[1024]	[0,0,0,0,0...]	0x0000E000@Data
AD_result	long[1500]	[0,0,0,0,0...]	0x0000B000@Data
BufferFillFlagCH1	unsigned int	0	0x0000BC76@Data
ArcTuningParams	struct <unnamed>	{B=30000.0,I=30000.0,F=64.0,D=0.0,...	0x0000A80A@Data
B	float	30000.0	0x0000A80A@Data
I	float	30000.0	0x0000A80C@Data
F	float	64.0	0x0000A80E@Data
D	float	0.0	0x0000A810@Data
T	int	220	0x0000A812@Data
C	int	55	0x0000A813@Data
ADSampleRate	float	250000.0	0x0000A814@Data
Add new expression			

Figure 3-3. Expressions Window for External ADC

Variables | Expressions | Registers

Expression	Type	Value	Address
CH1Data	int[1024]	[0,0,0,0,0...]	0x0000D400@Data
AD_result	long[1500]	[0,0,0,0,0...]	0x0000B000@Data
ArcTuningParams	struct <unnamed>	{B=30000.0,I=30000.0,F=64.0,D=0.0,...	0x0000A80A@Data
B	float	30000.0	0x0000A80A@Data
I	float	30000.0	0x0000A80C@Data
F	float	64.0	0x0000A80E@Data
D	float	0.0	0x0000A810@Data
T	int	220	0x0000A812@Data
C	int	55	0x0000A813@Data
ADSampleRate	float	250000.0	0x0000A814@Data
Add new expression			

Figure 3-4. Expressions Window for Internal ADC

- **CH1Data:** Array to store 1024 samples of the input signal.
- **AD_result:** Array in which the computed arc noise is stored. Each element represents the outcome of the analysis of 1024 samples.
- **BufferFillFLagCH1 (only for external ADC):** Flag to start the arc detection in case of the external ADC solution. Internal ADC project starts directly after boot up.
- **ArcTunningParams:** See Table 3-2. In this case the frequency band for arc detection is set to 30 kHz to 60 kHz.

After starting the software and enabling the continuous refresh option in the expressions window, the displayed values change, as shown in Figure 3-5. The input signal as well as the AD_result variable can be observed in the graphing tool. Figure 3-6 shows the sampled input signal for a 20-kHz sinusoidal input current.

Variables | Expressions | Registers

Expression	Type	Value	Address
CH1Data	int[1024]	[3231,555,3433,3304,545...]	0x0000D400@Data
AD_result	long[1500]	[35,39,35,39,35...]	0x0000B000@Data
ArcTuningParams	struct <unnamed>	{B=30000.0,I=30000.0,F=64.0,D=0.0,...	0x0000A80A@Data
B	float	30000.0	0x0000A80A@Data
I	float	30000.0	0x0000A80C@Data
F	float	64.0	0x0000A80E@Data
D	float	0.0	0x0000A810@Data
T	int	220	0x0000A812@Data
C	int	55	0x0000A813@Data
ADSampleRate	float	250000.0	0x0000A814@Data
Add new expression			

Figure 3-5. Expressions Window for 20 kHz Sinusoidal Input Current

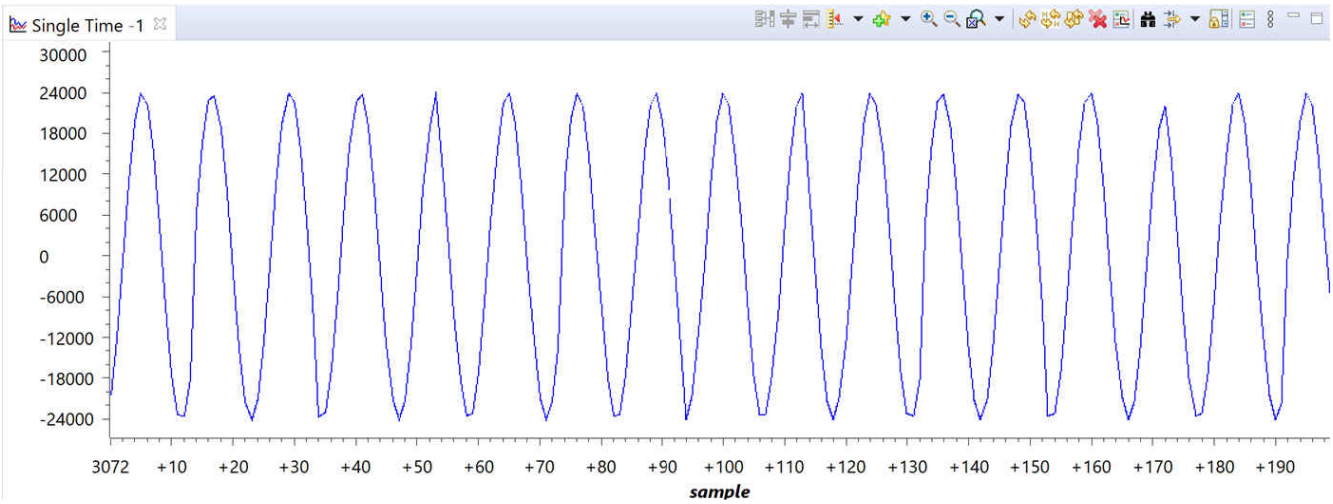


Figure 3-6. Graph of CH1Data at 20-kHz Sinusoidal Input Current

Table 3-4 shows the AD_result value for external and for internal ADC software for different input frequencies. For frequencies inside the arc detection frequency band, higher values are observed for AD_result than expected. In general, the change is more significant for the external ADC solution, which is expected because of the higher resolution of 16 bit versus 12 bit of the internal ADC.

Table 3-4. AD_result Values for Different Sinusoidal Inputs With External ADC and Internal ADC

FREQUENCY IN Hz	AD RESULT WITH EXTERNAL ADC	AD_result WITH INTERNAL ADC
10000	46	23
20000	43	28
30000	**89**	**47**
40000	**98**	**67**
50000	**80**	**49**
60000	**77**	**46**
70000	35	33
80000	12	30
90000	16	29
100000	19	25

3.3.2 Testing With Arcs

Test results under real arcing conditions vary depending on the system. When no arcing is occurring, the values in AD_Result should be stable. During the arcing event there is a significant increase in the AD_Result value, which indicates the arc. The absolute values can differ depending on the already exiting noise in the system, the selected input method of internal or external ADC and the specified ArcTuningParams. As a starting point, the default values shown in Table 3-5 are recommended. Select B and I in a way that the inverter switching frequency is outside the frequency band defined by B and I. In case there are high AD_Result values also during non-arcing, increase parameter D to 0.1 or 0.2 or adjust the cutoff frequencies of the analog band-pass filter. Detailed testing of different parameters allows for identifying the best settings for each system. After defining these parameters, use the AD_Result value to implement a custom algorithm to detect arcing. This can be done in different ways, for example by simply implementing a threshold for AD_Result or applying some filtering to multiple consecutive values of AD_Result before comparing to the threshold.

Table 3-5. Default Values of ArcTuningParams Structure

NAME	VALUE
float32 ArcTuningParams.B	30000
float32 ArcTuningParams.I	30000
float32 ArcTuningParams.F	64
float32 ArcTuningParams.D	0
int16 ArcTuningParams.T	N/A
int16 ArcTuningParams.C	N/A
float32 ArcTuningParams.ADSampleRate	250000

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010231.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010231.

4.2 Tools and Software

Software

C2000 Arc Detection software	Link for secure TI resources (login required).

4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

4.4 Trademarks

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5 About the Author

Andreas Lechner is a Systems Engineer for Grid Infrastructure working in Texas Instruments. Andreas is supporting customers within the Grid Infrastructure sector worldwide. Andreas earned his master's degree from the University of Applied Sciences in Landshut, Germany.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2022) to Revision B (April 2023)	Page
• Changed the content in the SETTING and COMMENT cells on the S7 switch in Table 3-3	13

Changes from Revision * (July 2022) to Revision A (February 2023)	Page
• Added *Digital Power SDK* support for design guide revision A	1

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