

## 3.6-Megapixel 3D Printer Reference Design

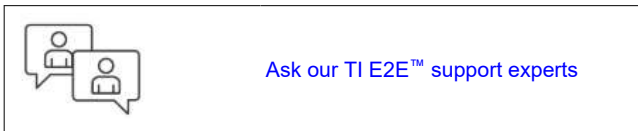


### Description

This reference design features the DLP® Pico® Products 0.3-inch 3.6 megapixel near-UV digital micromirror device (DMD) chipset for 3D printers. The design incorporates the [DLP300S](#) or [DLP301S](#) 2560 x 1440 (WQHD) DMD, [DLPC1438](#) display controller, and the [DLPA2005](#) PMIC/LED driver. The DLPC1438 3D print controller supports reliable operation of the DLP300S and DLP301S digital micromirror devices (DMDs) for DLP 3D Printer applications. The DLPC1438 controller provides a convenient interface between user electronics and the DMD to enable fast, high resolution, reliable DLP 3D printers.

### Resources

<a href="#">TIDA-080010</a>	Design Folder
<a href="#">DLP300S</a>	Product Folder
<a href="#">DLPC1438</a>	Product Folder
<a href="#">DLPA2005</a>	Product Folder

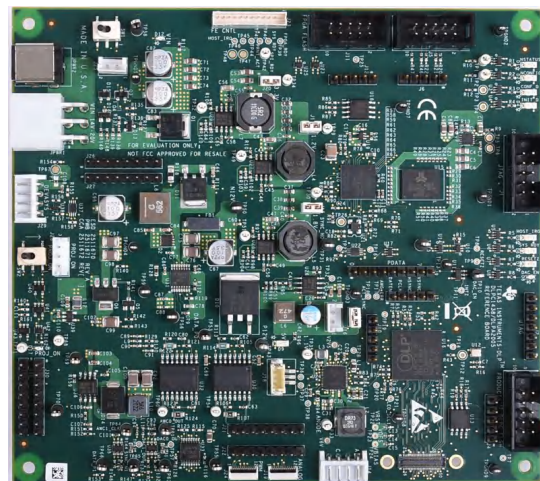
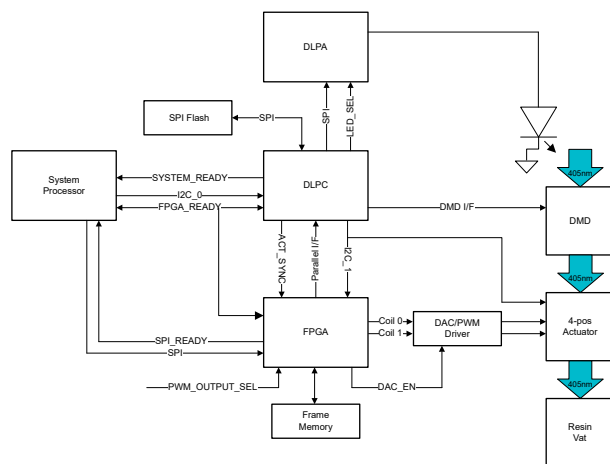


### Features

- Digital controller for DLP300S and DLP301S (0.3-inch 3.6-megapixel) DMDs
- 3D Printing Features:
  - Linear gamma modes optimized for optimizing illumination uniformity and grayscale printing
  - Programmable layer exposure time
  - 8-bit monochrome gray scale output
- System Features:
  - Front-end FPGA with low-cost SPI data input interface
  - Actuator control
  - I<sup>2</sup>C control of device configuration
  - Programmable LED current control
- Operation optimized for reliable performance in DLP 3D printer applications
- Pair with DLPA2000, DLPA2005, DLPA3000 or DLPA3005 PMIC (power management integrated circuit) and LED driver

### Applications

- [TI DLP 3D Printer](#)



## 1 System Description

The DLPC1438 3D print controller supports reliable operation of the DLP300S and DLP301S digital micromirror devices (DMDs) for DLP 3D Printer applications. The DLPC1438 controller provides a convenient interface between user electronics and the DMD to enable fast, high resolution, reliable DLP 3D printers. Get started with TI DLP light-control technology page to learn how to get started with the DLP300S. The DLP advanced light control resources on ti.com accelerate time to market, which include reference designs, optical modules manufactures, and DLP design network partners. This reference design provides developers the ability to quickly implement a compact 3D Printer using DLP300S DMD coupled with the DLPC1438 controller and DLPA2005 PMIC/LED driver.

## 2 System Overview

This reference design features the DLPC1438 display controller for 3D printers and the DLPA2005 PMIC/LED driver. This reference design provides a connection to drive the DLP300S or DLP301S DMD devices. The DLPC1438 chipset requires an FPGA between the DLP display controller and the front-end processor for image processing purposes. The System controller commands the DLPC1438 via an I<sup>2</sup>C bus. Frame data is sent from the System controller to the FPGA via a SPI bus. The System controller commands the DLPC1438 via an I<sup>2</sup>C bus. Frame data is sent from the System controller to the FPGA via a SPI bus.

### 2.1 Block Diagram

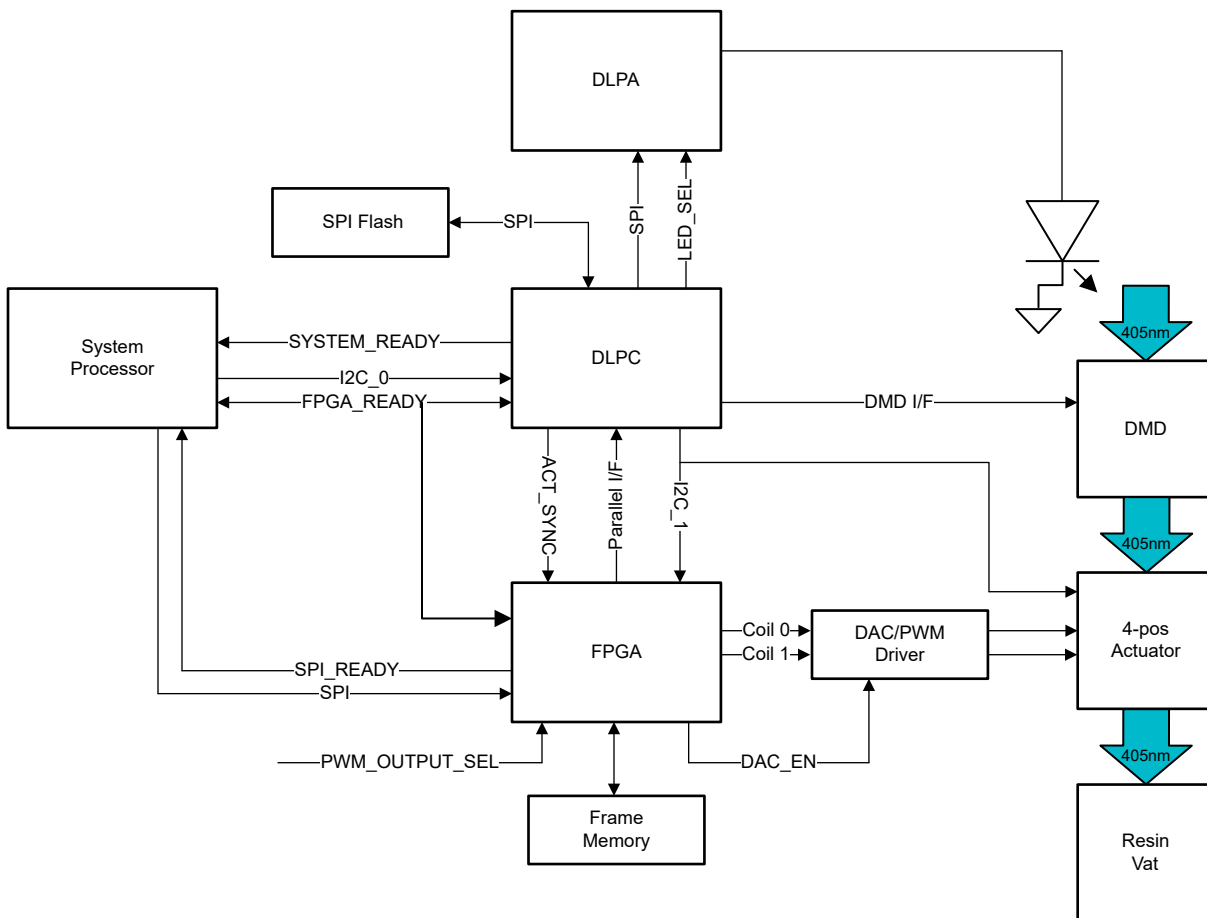


Figure 2-1. DLPC1438 Reference Design Block Diagram

**Table 2-1. Connectors, Jumpers, Headers, Switches**

<b>Jumpers</b>	<b>Connectors, Headers, Switches</b>
J1	FPGA JTAG CONNECTION
J2	DLPC JTAG CONNECTION
J3	DLPC FLASH PROGRAMMING HEADER
J4	SPIO TESTPOINTS
J5	FPGA SPI INPUT
J6	FPGA SPI TESTPOINTS
J7	PDATA CONTROL TESTPOINTS
J8	DMD CONNECTION
J9	PDATA TESTPOINTS
J10	DLPC SPI1 TESTPOINTS
J11	FPGA FLASH PROGRAMMING HEADER
J12	FPGA FLASH PROGRAMMING TESTPOINTS
J13	5V JUMPER
J14	ILLUMINATION POWER
J15	1.8V JUMPER
J16	5V FAN POWER
J17	1.2V JUMPER
J18	THERMISTOR
J19	DAC ACTUATOR CONNECTION
J20	3.3V JUMPER
J21	DAC ACTUATOR SIGNALS
J22	H-BRIDGE ACTUATOR SIGNALS
J23	FPGA/FRONTEND TESTPOINTS
J24	H-BRIDGE ACTUATOR CONNECTION
J25	EXT VIN ON/OFF CONNECTION
J26	FPGA TSTMUX
J27	FPGA TSTMUX
J28	EXT PROJ_ON CONNECTION
J29	IICO EXT CONNECTION
J30	UNUSED DLPC GPIO
J31	DLPC TSTPT ACCESS
JPWR1	PWR IN 14V-20V
JPWR2	ALTERNATE PWR IN 14V-20V
SW1	ENABLES POWER IN
SW2	PROJ_ON (turns system on and off)

## 2.2 Design Considerations

See the following application notes for consideration in DLP system design:

- [TI DLP® PICO™ System Overview: Optical Module Specifications](#)
- [TI DLP® System Design: Brightness Requirements and Tradeoffs](#)

## 2.3 General Layout Recommendations

The layout guidelines listed in this design guide are subsets of the guidelines included in the component data sheets. For more information, refer to the [DLPC1438 Digital Controller](#), [DLP300S DMD](#), and [DLPA2005 PMIC and LED Driver IC Data](#) data sheets.

### 2.3.1 DLPC3436 Layout Guidelines

#### 2.3.1.1 PLL Power Layout

Follow these recommended guidelines to achieve acceptable controller performance for the internal PLL. The DLPC1438 controller contains two internal PLLs which have dedicated analog supplies (VDD\_PLLM, VSS\_PLLM, VDD\_PLLD, and VSS\_PLLD). At a minimum, isolate the VDD\_PLLx power and VSS\_PLLx ground pins using a simple passive filter consisting of two series ferrite beads and two shunt capacitors (to widen the spectrum of noise absorption). TI recommends that one capacitor be 0.1  $\mu$ F and one be 0.01  $\mu$ F. Place all four components as close to the controller as possible. Keep the leads of the high-frequency capacitors as short as possible. Connect both capacitors from VDD\_PLLM to VSS\_PLLM and VDD\_PLLD to VSS\_PLLD on the controller side of the ferrite beads. Select ferrite beads with these characteristics:

- DC resistance less than 0.40  $\Omega$
- Impedance at 10 MHz equal to or greater than 180  $\Omega$
- Impedance at 100 MHz equal to or greater than 600  $\Omega$

The PCB layout is critical to PLL performance. It is vital that the quiet ground and power are treated like analog signals. Therefore, VDD\_PLLM and VDD\_PLLD must be a single trace from the DLPC3436 controller to both capacitors and then through the series ferrites to the power source. Make the power and ground traces as short as possible, parallel to each other, and as close as possible to each other.

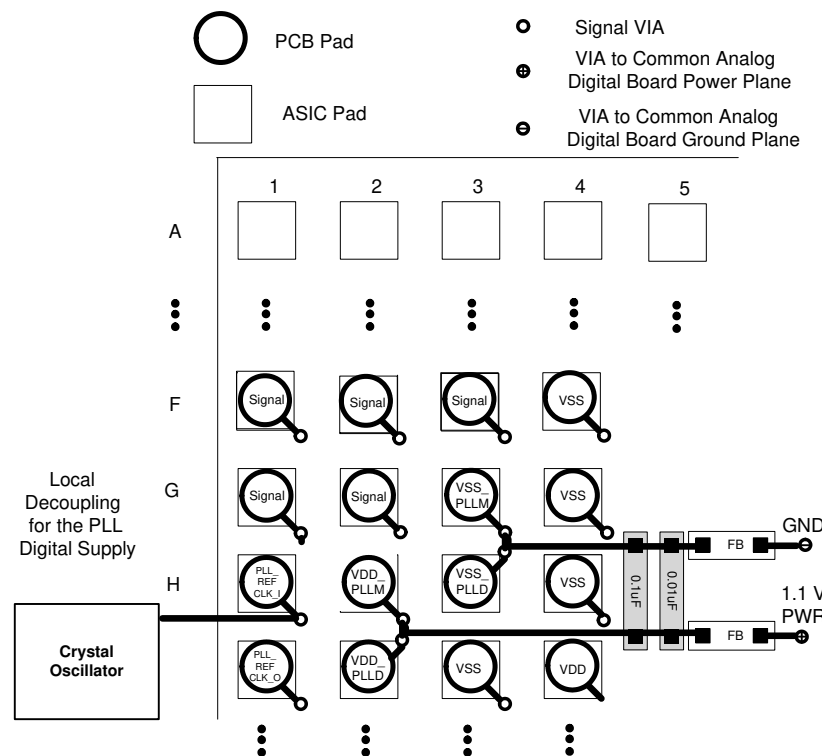


Figure 2-2. PLL Filter Layout

### 2.3.1.2 I2C Interface Performance

Both DLPC3436 I<sup>2</sup>C interface ports support a 100-kHz baud rate. By definition, I<sup>2</sup>C transactions operate at the speed of the slowest device on the bus, thus there is no requirement to match the speed grade of all devices in the system.

### 2.3.1.3 DMD Control and Sub-LVDS Signals

**Table 2-2. Maximum Pin-to-Pin PCB Interconnect Recommendations**

DMD BUS SIGNAL <sup>(1)</sup> <sup>(2)</sup>	SIGNAL INTERCONNECT TOPOLOGY		UNIT
	SINGLE-BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_HS_CLK_P DMD_HS_CLK_N	6.0 (152.4)	See <sup>(3)</sup>	in (mm)
DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	6.0 (152.4)	See <sup>(3)</sup>	in (mm)
DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD_LS_CLK	6.5 (165.1)	See <sup>(3)</sup>	in (mm)
DMD_LS_WDATA	6.5 (165.1)	See <sup>(3)</sup>	in (mm)
DMD_LS_RDATA	6.5 (165.1)	See <sup>(3)</sup>	in (mm)
DMD_DEN_ARSTZ	7.0 (177.8)	See <sup>(3)</sup>	in (mm)

- (1) Maximum signal routing length includes escape routing.
- (2) Multi-board DMD routing length is more restricted due to the impact of the connector.
- (3) Due to PCB variations, these recommendations cannot be defined. The best practice is for any board design to SPICE simulate with the controller IBIS model (found under the *Tools & Software* tab of the controller web page) to make sure routing lengths do not violate signal requirements.

**Table 2-3. High-Speed PCB Signal Routing Matching Requirements**

SIGNAL GROUP LENGTH MATCHING <sup>(1) (2) (3)</sup>				
INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH <sup>(4)</sup>	UNIT
DMD <sup>(5)</sup>	DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	DMD_HS_CLK_P DMD_HS_CLK_N	±1.0 (±25.4)	in (mm)
	DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
	DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
	DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
	DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
	DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
	DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
	DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD	DMD_HS_WDATA_x_P	DMD_HS_WDATA_x_N	±0.025 (±0.635)	in (mm)
DMD	DMD_HS_CLK_P	DMD_HS_CLK_N	±0.025 (±0.635)	in (mm)
DMD	DMD_LS_WDATA DMD_LS_RDATA	DMD_LS_CLK	±0.2 (±5.08)	in (mm)
DMD	DMD_DEN_ARSTZ	N/A	N/A	in (mm)

- (1) The length matching values apply to PCB routing lengths only. Internal package routing mismatch associated with the DLPC34xx controller or the DMD require no additional consideration.
- (2) Training is applied to DMD HS data lines. This is why the defined matching requirements are slightly relaxed compared to the LS data lines.
- (3) DMD LS signals are single ended.
- (4) Mismatch variance for a signal group is always with respect to the reference signal.
- (5) DMD HS data lines are differential, thus these specifications are pair-to-pair.

**Table 2-4. Signal Requirements**

PARAMETER	REFERENCE	REQUIREMENT
Source series termination	DMD_LS_WDATA	Required
	DMD_LS_CLK	Required
	DMD_DEN_ARSTZ	Acceptable
	DMD_LS_RDATA	Required
	DMD_HS_WDATA_x_y	Not acceptable
	DMD_HS_CLK_y	Not acceptable
Endpoint termination	DMD_LS_WDATA	Not acceptable
	DMD_LS_CLK	Not acceptable
	DMD_DEN_ARSTZ	Not acceptable
	DMD_LS_RDATA	Not acceptable
	DMD_HS_WDATA_x_y	Not acceptable
	DMD_HS_CLK_y	Not acceptable
PCB impedance	DMD_LS_WDATA	68 Ω ±10%
	DMD_LS_CLK	68 Ω ±10%
	DMD_DEN_ARSTZ	68 Ω ±10%
	DMD_LS_RDATA	68 Ω ±10%
	DMD_HS_WDATA_x_y	100 Ω ±10%
	DMD_HS_CLK_y	100 Ω ±10%
Signal type	DMD_LS_WDATA	SDR (single data rate) referenced to DMD_LS_DCLK
	DMD_LS_CLK	SDR referenced to DMD_LS_DCLK
	DMD_DEN_ARSTZ	SDR
	DMD_LS_RDATA	SDR referenced to DMD_LS_DCLK
	DMD_HS_WDATA_x_y	sub-LVDS
	DMD_HS_CLK_y	sub-LVDS

### 2.3.1.4 Layout Layer Changes

- Single-ended signals: Minimize the number of layer changes.
- Differential signals: Individual differential pairs can be routed on different layers. Make sure that the signals of a given pair do not change layers.

### 2.3.1.5 Stubs

- Avoid using stubs.

### 2.3.1.6 Terminations

- DMD\_HS differential signals require no external termination resistors.
- Make sure the DMD\_LS\_CLK and DMD\_LS\_WDATA signal paths include a 43-Ω series termination resistor located as close as possible to the corresponding controller pins.
- Make sure the DMD\_LS\_RDATA signal path includes a 43-Ω series termination resistor located as close as possible to the corresponding DMD pin.
- The DMD\_DEN\_ARSTZ pin requires no series resistor.

### 2.3.1.7 Routing Vias

- The number of vias on DMD\_HS signals must be minimized.
- Any and all vias on DMD\_HS signals must be located as close to the controller as possible.
- The number of vias on the DMD\_LS\_CLK and DMD\_LS\_WDATA signals must be minimized and in the best circumstance not exceed two.
- Any and all vias on the DMD\_LS\_CLK and DMD\_LS\_WDATA signals must be located as close to the controller as possible.

### 2.3.2 FPGA DDR2 SDRAM Interface Routing

The FPGA to DDR2 SDRAM interface is based on a 400-MHz DDR clock rate. The Intel® Cyclone® IV E FPGA (EP4CE15M9C7N) to an Alliance DDR2 SDRAM (AS4C64M8D2-25BIN) interface diagram is shown in Figure 2-3 and the recommended interface layout guidelines are defined in Table 2-5.

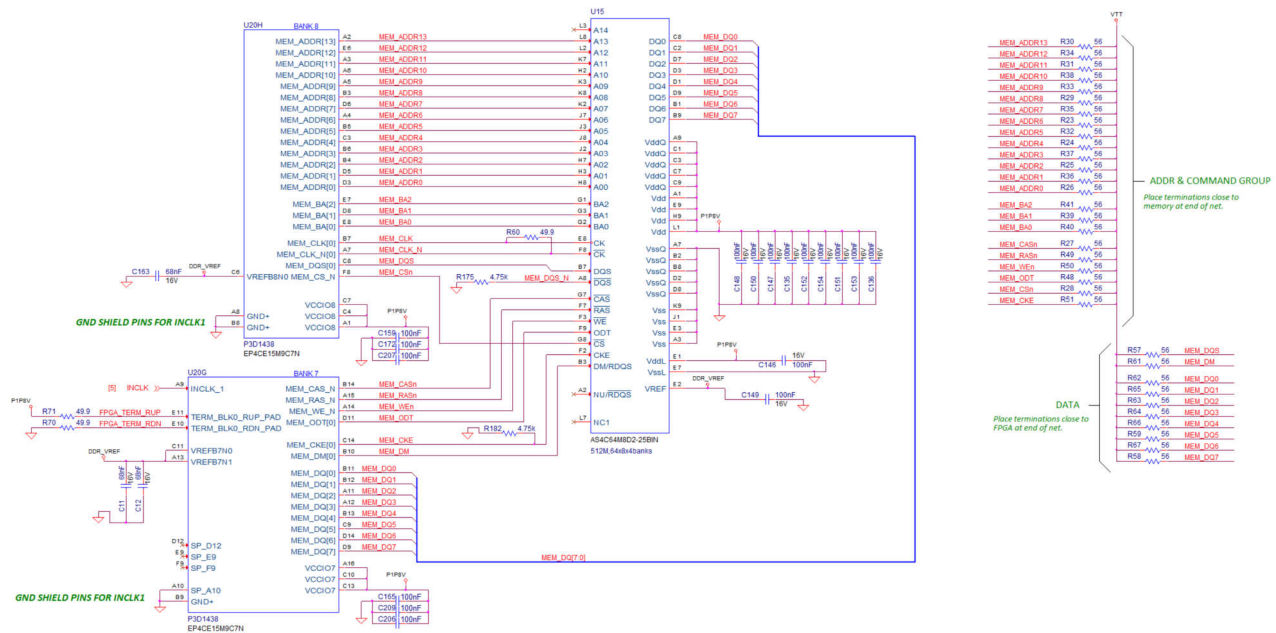


Figure 2-3. FPGA-DDR2 Interface

Table 2-5. Recommended FPGA-DDR2 PCB Matching and Trace Delays

GROUP	GROUP NAME	LENGTH MATCH WITHIN GROUP	LENGTH MATCH TO OTHER SIGNALS	ADDITIONAL ROUTING REQUIREMENTS
MEM_ADDR[13:0], MEM_BA[2:0], MEM_CASn, MEM_RASn, MEM_WEn, MEM_ODT, MEM_CKE, MEM_CSn	Addr/Cntl Group	WITHIN GROUP ±50 ps	0 ps to 15 ps less than MEM_CLK and MEM_CLK_N	50 Ω - place termination at DDR2 end of trace - maximum length 250 ps - minimum length 200 ps
MEM_DQ[7:0], MEM_DM, MEM_DQS	Data Group	WITHIN GROUP ±10 ps	MEM_CLK, MEM_CLK_N ±10 ps	50 Ω - use inner layer - route on same layer - place termination at FPGA end of trace - max length 250 ps - min length 200 ps
MEM_CLK, MEM_CLK_N	CLK Group	WITHIN GROUP ±2 ps	MEM_DQS ±2 ps Must be 0 ps to 15 ps longer than ADDR & CNTL Group	100 differential - minimize trace on outer layer - use inner layer - max length 250 ps - min length 200 ps

PCB routing best practices:

- Use inner PCB layers when possible
- Route DDR\_DQ(7:0), MEM\_DM and DDR\_DQS on the same layers



## 2.3.3 DLPA2005 Layout Recommendations

### 2.3.3.1 Layout Guidelines

As for all chips with switching power supplies, the layout is an important step in the design, especially in the case of high peak currents and high switching frequencies. If the layout is not carefully done, the regulators can show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current paths and for the power ground tracks. Input capacitors, output capacitors, and place inductors as close as possible to the IC.

Figure 2-4 shows an example layout that has critical parts placed as close as possible to the pins. Following are recommendations for the components:

- R1** is RLIM and is connected through a wide trace (low resistance) to the system ground. Star connect the analog ground at pin 5 to the point where RLIM is connected to the system ground. Aim on a wide and low-ohmic trace as well, although this one is less critical (tens of mA).
- L1** is the big inductor for the VLED that is connected through two wide traces to the pins.
- C4** the decoupling capacitors for the VLED. Place C4 as close as possible to the part and directly connect C4 to ground.
- L3/C20** are components used for the VCORE BUCK. L3 is placed close to the pin and connected with a wide trace to the part. C20 is placed directly beside the inductor and connected to the PGND pin.
- L2** This inductor is part of the DMD reset regulators and is also placed as close as possible to the DLPA2005 using wide PCB traces.

### 2.3.3.2 Layout Example

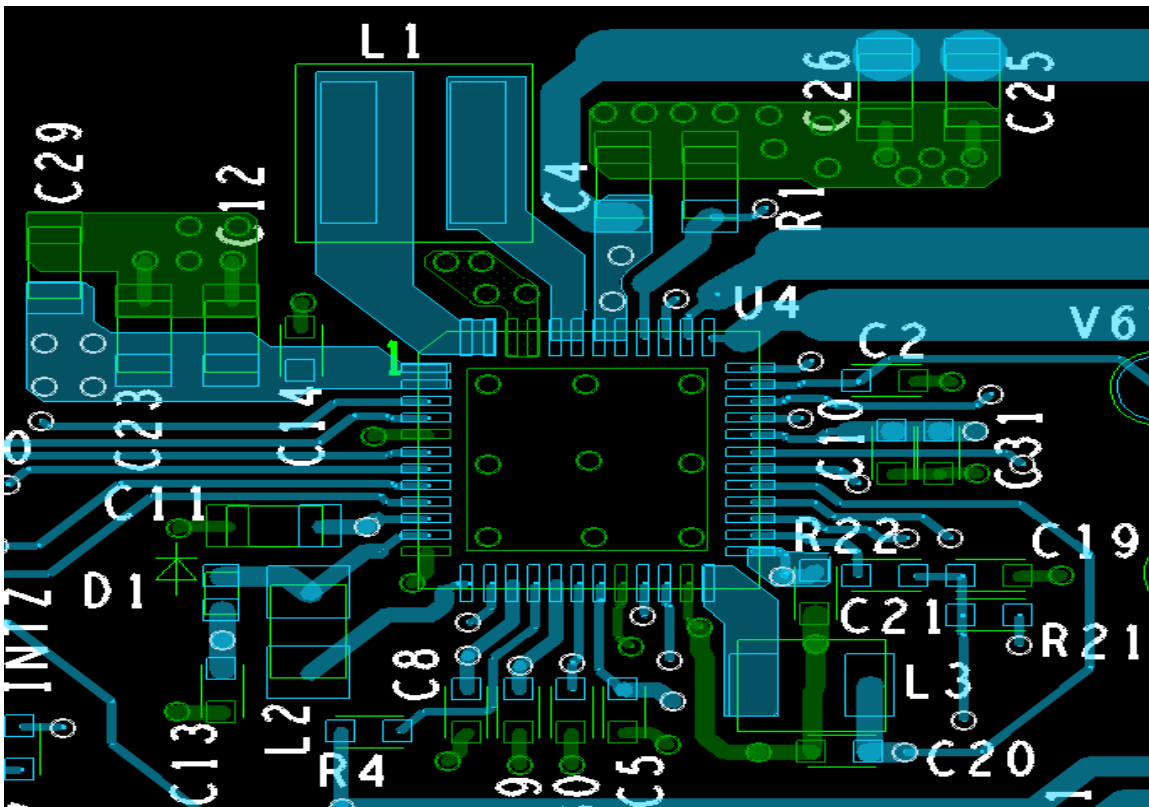
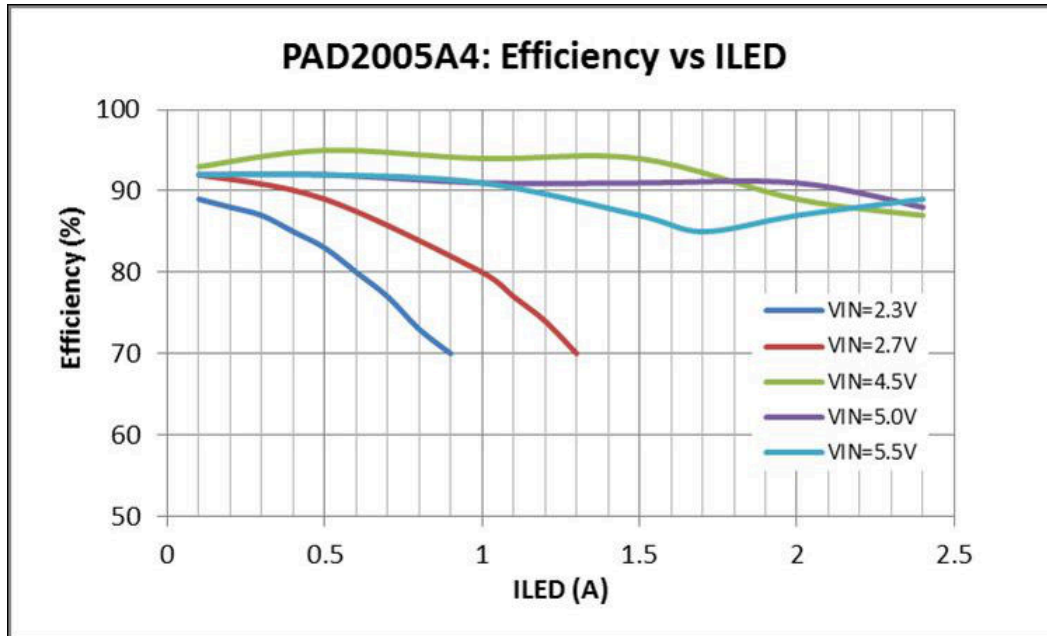


Figure 2-4. Example Layout of DLPA2005

### 2.3.3.3 Thermal Considerations

An important consequence of the efficiency numbers shown in Figure 2-5 is that it enables to perform DLPA2005 thermal calculations. Since the efficiency is not 100%, power is dissipated in the DLPA2005 chip. Due to that dissipation, die temperature rises. For reliability reasons, it is good to aim for as low as possible die temperatures. Using a heat sink and airflow are efficient means to keep die temperature reasonably low. In cases that airflow and or a heat sink are or is not feasible, the system designer must specifically pay attention to the thermal design. The die temperature for regular operation needs to remain below 120°C.



**Figure 2-5. Measured Typical Power Converter Efficiency as a Function of ILED for Several Supply Voltages ( $V_{OUTmax} = 4.8\text{ V}$  for Each Supply)**

In the following, an example is given of such a thermal calculation. The calculation starts with summarizing all blocks in the DLPA2005 that dissipate. The buck-boost converter supplying the LED power is the main source of dissipation. For illustrating purposes, we assume this buck-boost converter to be the only block that dissipates significantly. For the example assume:  $V_{OUT} = 4.8\text{ V}$  (for all three LEDs),  $I_{OUT} = 2.4\text{ A}$  and  $V_{IN} = 5\text{ V}$ . From Figure 2-5 it can be derived that the related efficiency equals about  $\eta_{eff} = 88\%$ .

The power dissipated by the DLPA2005 is then given by:

$$P_{DISS} = P_{IN} - P_{OUT} = P_{OUT} \left( \frac{100\%}{\eta_{eff}} - 1 \right) = 4.8\text{ V} \cdot 2.4\text{ A} \cdot \left( \frac{100\%}{88\%} - 1 \right) = 1.6\text{ W} \quad (1)$$

The rise of die temperature due to this power dissipation can be calculated using the thermal resistance from junction to ambient,  $\theta_{JA} = 27.9^\circ\text{C/W}$ . This calculation yields:

$$T_{JUNCTION} = T_{AMBIENT} + P_{DISS} \cdot \theta_{JA} = 25^\circ\text{C} + 1.6\text{ W} \cdot 27.9^\circ\text{C/W} = 69.6^\circ\text{C} \quad (2)$$

It is also possible to calculate the maximum allowable ambient temperature to prevent surpassing the maximum die temperature. Assume again the dissipation of  $P_{DISS} = 1.6\text{ W}$ . The maximum ambient temperature that is allowed is then given by:

$$T_{AMBIENT-max} = T_{JUNCTION-max} - P_{DISS} \cdot \theta_{JA} = 120^\circ\text{C} - 1.6\text{ W} \cdot 27.9^\circ\text{C/W} = 75.4^\circ\text{C} \quad (3)$$

It is again stressed that for proper calculations, the total power dissipation of the DLPA2005 needs to be taken into account. Also, if components that are close to the DLPA2005 also dissipate a significant amount of power, the (local) ambient temperature can be higher than the ambient temperature of the system.

If calculations show that the die temperature can surpass the maximum specified value, two basic options exist:

- Adding a heat sink with or without airflow. This reduces  $\theta_{JA}$  yielding lower die temperature.
- Lowering the dissipation in the DLPA2005 implying lowering the maximum allowable LED current.

### 2.3.4 DMD Flex Cable Interface Layout Guidelines

The DLP300S DMD is connected to a PCB or a flex circuit using an interposer. For additional layout guidelines regarding length matching, impedance, and so on, see the [DLPC1438 Digital Controller data sheet](#). For layout guidelines for the [DLP300S DMD](#) or [DLP301S](#) see the related data sheet.

Some layout guidelines for routing to the DLP300S or DLP301S DMD include:

- Match lengths for the LS\_WDATA and LS\_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals.
- Minimum of two 100-nF (25 V) capacitors - one close to  $V_{BIAS}$  pin.
- Minimum of two 100-nF (25 V) capacitors - one close to each  $V_{RST}$  pin.
- Minimum of two 220-nF (25 V) capacitors - one close to each  $V_{OFS}$  pin.
- Minimum of four 100-nF (6.3 V) capacitors - two close to each side of the DMD.

## 2.4 Highlighted Products

This chipset reference design guide draws upon figures and content from several other published documents related to the DLP300S and DLP301S DLP chipsets. For a list of these documents, see [Section 4.3](#)

# 3 Hardware

## 3.1 Hardware Requirements

1. Power up the DLPC1438 Reference Design by applying an external DC power supply (14–20 V DC) to the JPWR1 connector.

### External Power Supply Requirements:

- Nominal Output Voltage: 14–20 V DC
- Minimum Output Current: 3 A; Maximum Output Current: 4 A
- Efficiency Level: VI

### Note

TI recommends using an external power supply that complies with applicable regional safety standards such as UL, CSA, VDE, CCC, PSE, and so forth.

2. SW1 enables power into the system. When engaged LED D12 (green) turns on. SW2 drives PROJ\_ON and when engaged turns on LED D17 (green). With SW1 and SW2 in the on positions the system boots (The DLP300S or DLP301S DMD must be connected for system boot to complete.).

There are several indicator LEDs on the DLPC1438 Reference Design, and the LEDs are defined in [Table 3-1](#).

**Table 3-1. LEDs on the DLPC1438 Reference Design**

LED REFERENCE	SIGNAL INDICATION	DESCRIPTION
D5	HOST_IRQ	ON during DLPC1438 boot, OFF when projector is running. Indication of DLPC1438 boot-up completed and ready to receive commands
D17	PROJ_ON	PROJ_ON signal is HIGH
D4	INIT_DONE	ON when FPGA initialization is completed. OFF indicates that the FPGA is in RESET or a configuration error occurred.
D3	CONF_DONE	ON when FPGA configuration is completed.
D9	P5V	Input voltage 5 V applied

## 4 Design and Documentation Support

### 4.1 Design Files

#### 4.1.1 Schematics

To download the schematics, see the design files at [TIDA-080010](#).

#### 4.1.2 BOM

To download the bill of materials (BOM), see the design files at [TIDA-080010](#).

#### 4.1.3 Layout Files

To download the bill of materials (BOM), see the design files at [TIDA-080010](#).

#### 4.1.4 Mechanical Files

To download the bill of materials (BOM), see the design files at [TIDA-080010](#).

### 4.2 Software and FPGA code

[DLPC1438 firmware](#) and [FPGA code](#) can be downloaded from the TI website.

### 4.3 Documentation Support

1. Texas Instruments, [DLPC1438 Digital Controller for TI DLP® 3D Printers Data Sheet](#)
2. Texas Instruments, [DLP300S 0.3-Inch 3.6-Megapixel DMD for Low Cost TI DLP® 3D Printers Data Sheet](#)
3. Texas Instruments, [DLPA2005 Power Management and LED/Lamp Driver IC Data Sheet](#)

### 4.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 4.5 Trademarks

TI E2E™ are trademarks of Texas Instruments.

DLP® and Pico® are registered trademarks of Texas Instruments.

Intel® and Cyclone® are registered trademarks of Intel.

All trademarks are the property of their respective owners.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated