Design Guide: TIDA-060043

56G Retimer QSFP-DD MCB Reference Design

Description

This reference design demonstrates how the 56G PAM-4 retimer DS560DF410 can be used to equalize high-speed signals in active electrical cable applications. The design is a module compliance board (MCB) which routes signals from a QSFP-DD connector through a retimer to SMA and MXP connectors in both ingress and egress directions.

Resources

TIDA-060043	Design Folder
DS560DF410	Product Folder
TPS62867	Product Folder
TPS7A52	Product Folder
TLV702	Product Folder
TXB0108	Product Folder

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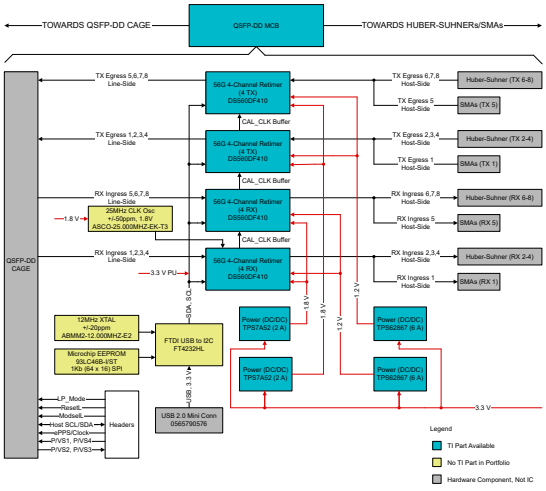
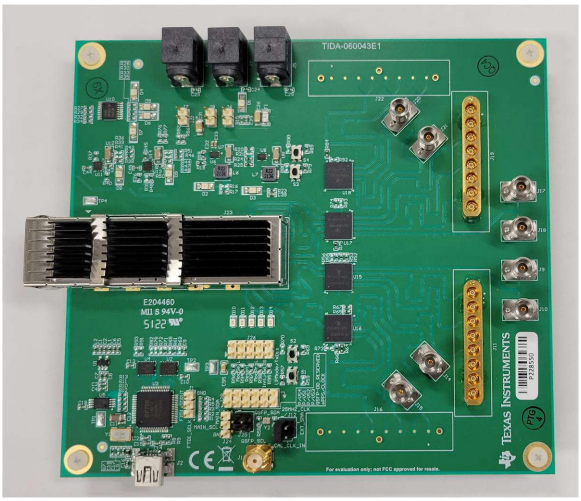
Features

- 8 independent channels for each direction
- QSFP-DD cable compatibility, for both ingress and egress
- Host-side Huber-Suhner and SMA compatibility, for both ingress and egress
- Configurable through electrically erasable programmable read-only memory (EEPROM) or USB-to-I2C communication
- Headers for all relevant debug and configuration pin controls and interrupts
- Onboard power regulation for 3.3 V → {1.8 V, 1.2 V} domains

Applications

- Data center switch
- Campus and branch switches
- Edge router
- Core router





1 System Description

The TIDA-060043 reference design represents a front port application for a 56G retimer. This design provides a reference on how DS560DF410 can be implemented in a front port application and also allows for testing of DS560DF410 in front port applications.

This reference design can be used to test the following IEEE 802.3 specifications:

- Clause 136: Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4
- Clause 92: Physical Medium Dependent (PMD) sublayer and baseband medium type 100GBASE-CR4
- Annex 136A: TP0 and TP5 test point parameters and channel characteristics for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4
- Annex 120E: Chip-to-module 200Gbps four-lane attachment unit interface (200GAUI-4 C2M) and 400Gbps eight-lane attachment unit interface (400GAUI-8 C2M)

2 System Overview

2.1 Block Diagram

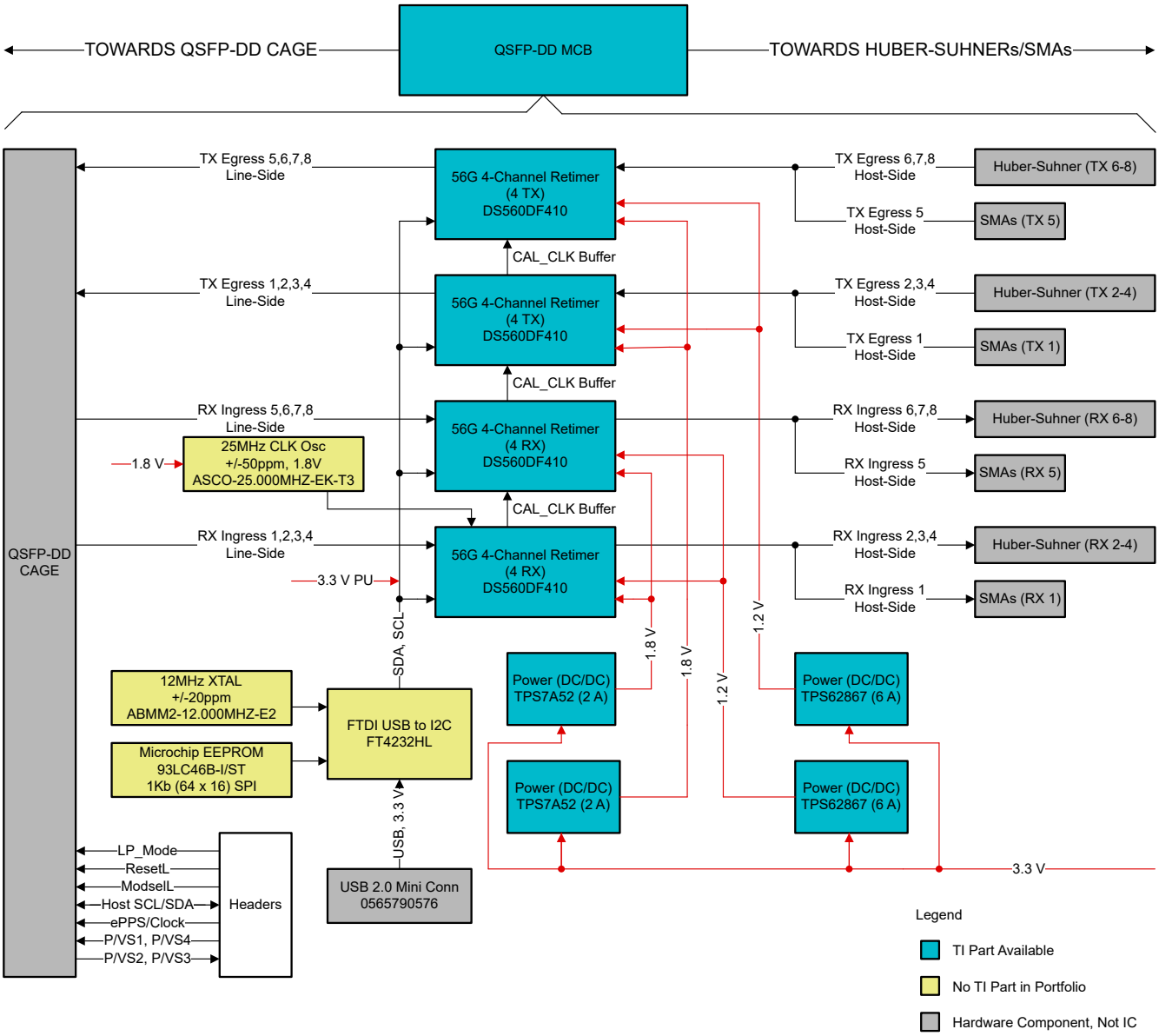


Figure 2-1. TIDA-060043 Block Diagram

2.2 Design Considerations

2.2.1 Connectors

MXP connectors are commonly used on high-speed test and evaluation equipment. TI uses MXP connectors on 25G/28G and 56G Ethernet signal condition device EVMs. Because of this, MXP connecters were also selected to interface with this MCB. There are 4 DS560DF410 devices on each MCB. Two devices handle ingress, and two handle egress. For each device, 3 channels are routed to MXP connectors, and 1 channel is routed to SMA connectors. SMA connectors were added to offer flexibility in case there are challenges acquiring MXP cable assemblies.

2.2.2 High-Speed Traces

High-speed trace layout is an important factor in high-speed design. While designing the MCB, layout recommendations from the *DS560DF410 56Gbps Multi-Rate 4-Channel Retimer with Crosspoint* data sheet were followed. This provides good high-speed performance. Additionally, board-level simulation of the high-speed traces was performed to increase confidence in the performance of the layout prior to manufacturing.

2.2.3 Power Rails

The board is powered with 3.3 V, while the DS560DF410 retimers operate on the 1.8 V and 1.2 V domains. Consistent with DS560DF410EVM design, 3.3 V to 1.8 V conversion is done with TPS7A52, and 3.3 V to 1.2 V conversion is done with TPS62867. Both instances of DC/DC conversion are performed following the design guidelines of each regulator.

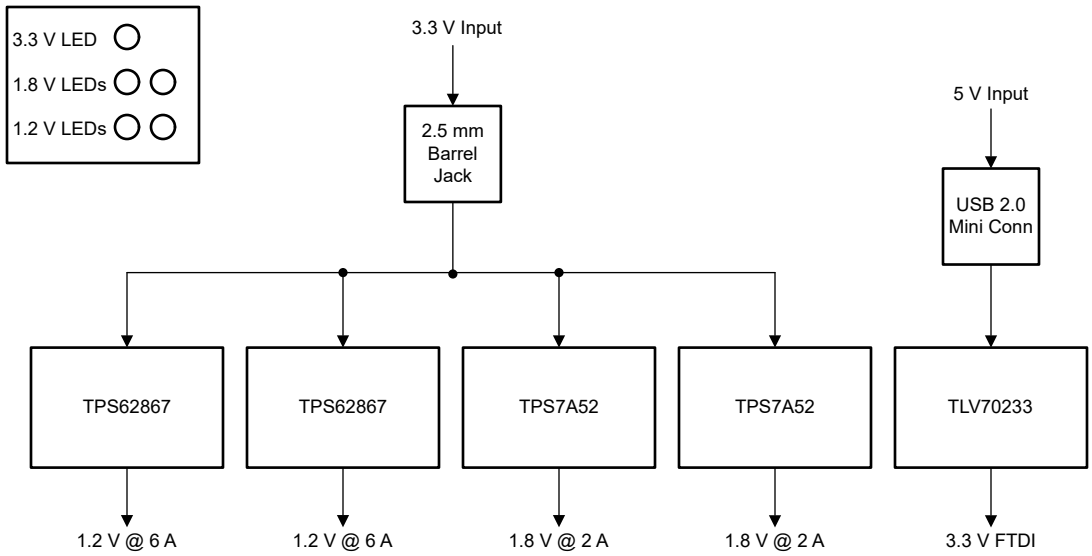


Figure 2-2. TIDA-060043 Power Tree

2.3 Highlighted Products

TIDA-060043	Design Folder
DS560DF410	Product Folder
TPS62867	Product Folder
TPS7A52	Product Folder
TLV702	Product Folder
TXB0108	Product Folder

2.3.1 DS560DF410

The DS560DF410 is a four-channel multi-rate retimer with integrated signal conditioning. The device extends the reach and robustness of long, lossy, crosstalk-impaired high-speed serial links. Each channel in the DS560DF410 independently locks to symbol rates (PAM4 and NRZ) in a continuous range from 19.6 to 28.9GBd or to any supported sub-rate. The integrated CDR function is designed for front-port optical module applications to reset the jitter budget and retime the high-speed serial data. These features allow for individual lane forward error correction (FEC) pass-through. In addition, the DS560DF410 supports automatic lane rate switching for CDR lock up to five different combinations of baud rates and modulation types without host intervention. The advanced equalization features of the DS560DF410 include a continuously adaptive continuous-time linear equalizer (CTLE), RX feedforward equalizer (FFE), decision feedback equalizer (DFE), and a programmable, low-jitter 4-tap TX feedforward equalizer (FFE) filter. These features enable reach extension for lossy interconnects such as direct-attach copper (DAC) cables and backplanes with multiple connectors and crosstalk.

2.3.2 TPS62867

The TPS62865 and TPS62867 devices are high-frequency synchronous step-down converters which provide an efficient, flexible, and high power-density design. At medium to heavy loads, the converters operate in PWM mode and automatically enter Power Save Mode operation at light load to maintain high efficiency over the entire load current range. The devices can also be forced in PWM mode operation to minimize output voltage ripple. Together with the DCS-control architecture, excellent load transient performance and tight output voltage accuracy are achieved. The devices feature a Power Good signal and an internal soft start circuit. The devices are able to operate in 100% mode. For fault protection, the devices incorporate a HICCUP short circuit protection as well as a thermal shutdown

2.3.3 TPS7A52

The TPS7A52 is a low-noise (4.4 μV_{RMS}), ultra-low dropout linear regulator (LDO) capable of sourcing 2 A with only 65 mV of maximum dropout. The device output voltage is adjustable from 0.8 V to 5.2 V using an external resistor divider.

For digital loads [such as application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and digital signal processors (DSPs)] requiring low-input voltage, low-output (LILO) voltage operation, the exceptional accuracy (0.5% over load and temperature), remote sensing, excellent transient performance, and soft-start capabilities of the TPS7A52 provides excellent system performance.

2.3.4 TLV702

The TLV702 series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision band gap and error amplifier provides overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low-dropout voltage make this series of devices an excellent choice for a wide selection of battery-operated handheld equipment. All device versions have thermal shutdown and current limit for safety.

2.3.5 TXB0108

This 8-bit noninverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-, 1.5-, 1.8-, 2.5-, 3.3-, and 5-V voltage nodes. V_{CCA} should not exceed V_{CCB}.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

3.1.1 TX Output Eye Test

The following hardware is required to perform the TX output eye test.

- TIDA-060043 MCB board (qty 1)
- ML4020-MXP or alternate QSFP-to-SMA breakout HCB board (qty 1)
- BERT or alternate PRBS generator (qty 1)
- DCA-X sampling oscilloscope (qty 1)
- PC with Latte software (qty 1)
- 3.3-V capable power supply (qty 1)
- MXP40 1 × 8 connectors (qty 2)
- High-speed SMA cables (qty 4)
- USB2.0 mini high-speed cable (qty 1)
- Banana jack-to-2.5-mm barrel-jack power-supply lead (qty 1)

3.1.2 RX Link Test

The following hardware is required to perform the RX link test.

- TIDA-060043 MCB boards (qty 2)
- BERT or alternate PRBS generator (qty 1)
- PC with Latte software (qty 1)
- 3.3-V capable power supplies (qty 2)
- MXP40 1 × 8 connector (qty 1)
- 1 meter 28 AWG QSFP Molex passive cable or alternate QSFP passive cable (qty 1)
- High-speed SMA cables (qty 2)
- USB2.0 mini high-speed cable (qty 1)
- Banana jack-to-2.5-mm barrel-jack power-supply leads (qty 2)

3.2 Software Requirements

Many of the common device configurations intended for the reference design require configuration through a TI-developed GUI called *Latte*. This software is required to perform the TX output eye test and the RX link test. The latest version of Latte is available for download by request through TI's website. There are two installation files that the user needs to download and execute: the Latte framework installer file and the Latte libraries updater. As of this publication, the latest Latte installation files are the following:

- Main Installer: `TI-DS560-Latte_vXpX.exe`
- Libraries updater: `TI-DS560Lib_vXpX.exe`

For detailed instructions on the software installation sequence, functional overview, and initialization sequence for Latte, refer to the software description sections in the *DS560DF810 EVM User's Guide*. The reference design follows a similar initialization sequence relative to the DS560EVM, with the following key difference:

- In the `devinit.py` file, change the device address to correspond to the target device on the MCB.

3.3 Test Setup

3.3.1 TX Output Eye Test

This procedure specifically explains how to measure a TX output eye of 26.5625GBd PAM-4 PRBS13Q data passing through retimer U15 channel 2 on the TIDA-060043 MCB board.

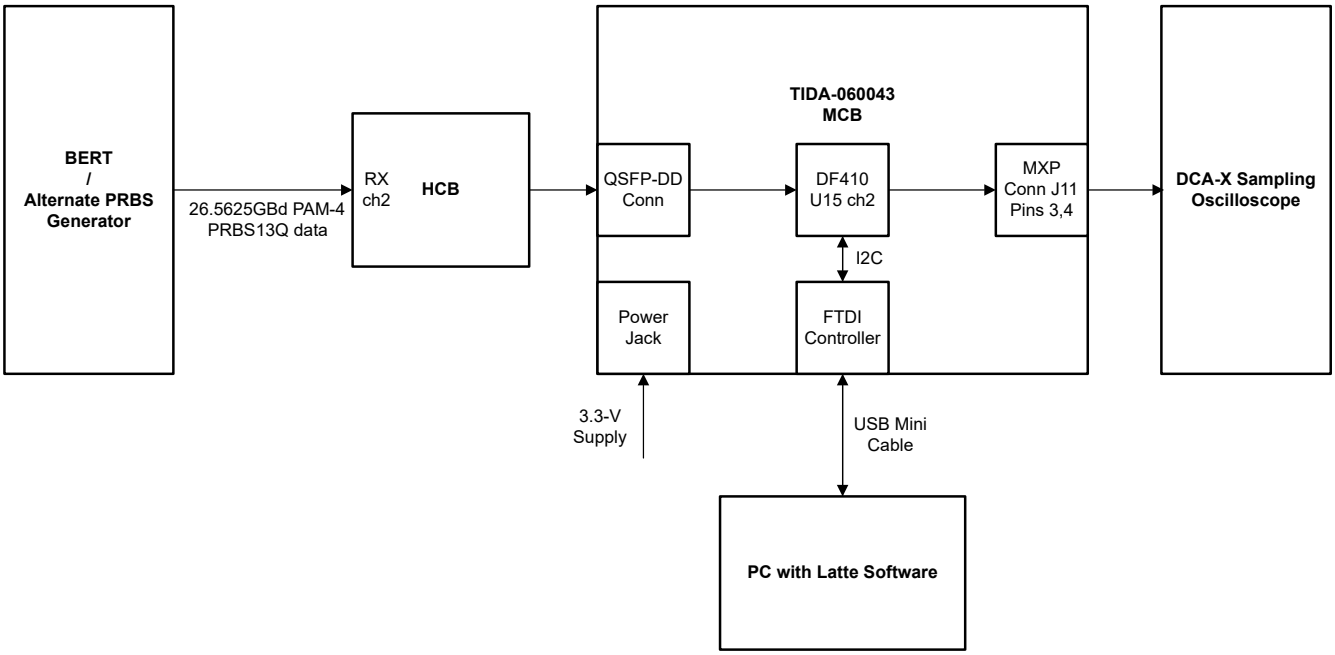


Figure 3-1. TX Output Eye Test Setup

1. Plug the HCB breakout board into the QSFP-DD port on TIDA-060043 (J27). Plug MXP40 connectors onto J11 of TIDA-060043 and the port on the HCB labeled for RX signals.
2. Using SMA cables, connect RX channel 2 of the HCB to the BERT output and J11 pins 3, 4 on TIDA-060043 to the DCA-X sampling oscilloscope input.
3. Connect the PC to the USB port on TIDA-060043 (J2) using the USB2.0 mini cable.
4. Connect the power supply to the +3.3-V barrel jack on TIDA-060043 (J3) using the supply lead. Power the board with 3.3 V.
5. Configure the BERT to output 26.5625GBd PAM-4 PRBS13Q data.
6. Open Latte on the PC and run `setup.py`. Make sure *setupInfo = 0* and *devIdentifier = 1*.
7. Run `devinit.py`. Make sure *device.slaveAddr = 0x18* on line 79 as this address corresponds to retimer U15 on TIDA-060043.
8. Configure `1_bringupParams.py` for 26.5625GBd PAM-4 data enabled on Q0CH2. Run `1_bringupParams.py`.
9. Run `2_bringupLib.py`. Run the "READBACK CHANNEL INIT STATUS / LOCK STATUS" code block of `usefulFunctions.py` and confirm channel 2 has CDR lock.
10. Configure the DCA-X to lock to 26.5625GBD PAM-4 PRBS13Q data and display the output eye.
11. Using the "CHANGE TX-FFE" code block of `usefulFunctions.py`, tune the FFE taps while visually inspecting the output eye to optimize performance. For the results shown in Figure 3-3, settings of *pre=2* and *post=4* were used.
12. Capture the eye diagram and jitter results on the DCA-X.

3.3.2 RX Link Test

This procedure specifically explains how to measure the BER of 26.5625GBd PAM-4 PRBS31Q data passing through retimer U17 channel 2 on the first TIDA-060043 board, a passive QSFP cable, and retimer U15 channel 2 on the second TIDA-060043 board.

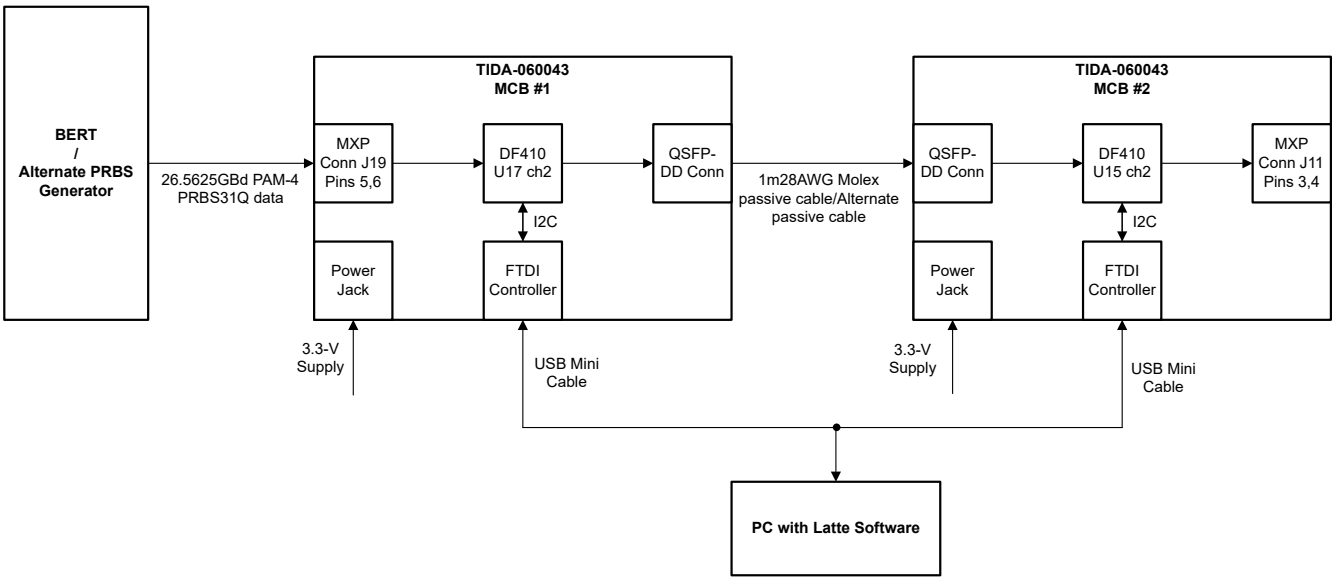


Figure 3-2. RX Link Test Setup

1. Plug the passive QSFP cable into the QSFP-DD port on both TIDA-060043 boards (J27). Plug the MXP40 connector onto J19 of the first TIDA-060043 board.
2. Using SMA cables, connect J19 pins 5, 6 on the first TIDA-060043 board to the BERT output.
3. Connect the PC to the USB port on the first TIDA-060043 board (J2) using the USB2.0 mini cable.
4. Connect the power supplies to the +3.3-V barrel jacks on both TIDA-060043 boards (J3) using the supply leads. Power both boards with 3.3 V.
5. Configure the BERT to output 26.5625GBd PAM-4 PRBS31Q data.
6. Open Latte on the PC and run `setup.py`. Make sure *setupInfo = 0* and *devIdentifier = 1*.
7. Run `devinit.py`. Make sure *device.slaveAddr = 0x19* on line 79 as this address corresponds to retimer U17 on TIDA-060043.
8. Configure *1_bringupParams.py* for 26.5625GBd PAM-4 data enabled on Q0CH2. Run `1_bringupParams.py`.
9. Run `2_bringupLib.py`. Run the "READBACK CHANNEL INIT STATUS / LOCK STATUS" code block of `usefulFunctions.py` and confirm channel 2 has CDR lock.
10. Unplug the USB cable from the first TIDA-060043 board and plug the cable into the USB port of the second TIDA-060043 board (J2).
11. Run `setup.py`. Make sure *setupInfo = 0* and *devIdentifier = 1*.
12. Run `devinit.py`. Make sure *device.slaveAddr = 0x18* on line 79 as this address corresponds to retimer U15 on TIDA-060043.
13. Configure `1_bringupParams.py` for 26.5625GBd PAM-4 data enabled on Q0CH2. Make sure *sysParams.rxPrbsSel = [x,x,5,x,…]* so the device knows it is receiving PRBS31Q data on channel 2. Run `1_bringupParams.py`.
14. Run `2_bringupLib.py`. Run the "READBACK CHANNEL INIT STATUS / LOCK STATUS" code block of `usefulFunctions.py` and confirm channel 2 has CDR lock.
15. Run the "READBACK BER" code block of `usefulFunction.py`. Tune the FFE taps on the BERT to optimize the BER. For the results shown in Table 3-1, BERT FFE settings of *pre1=-8* and *post1=-5* were used.
16. Run "READBACK BER" at least 3 times and record the resulting BER.

3.4 Test Results

3.4.1 TX Output Eye Test

The TX output eye test was performed on the TIDA-060043 board according to the procedure outlined in Section 3.3. The resulting output eye and jitter measurements are shown in Figure 3-3.

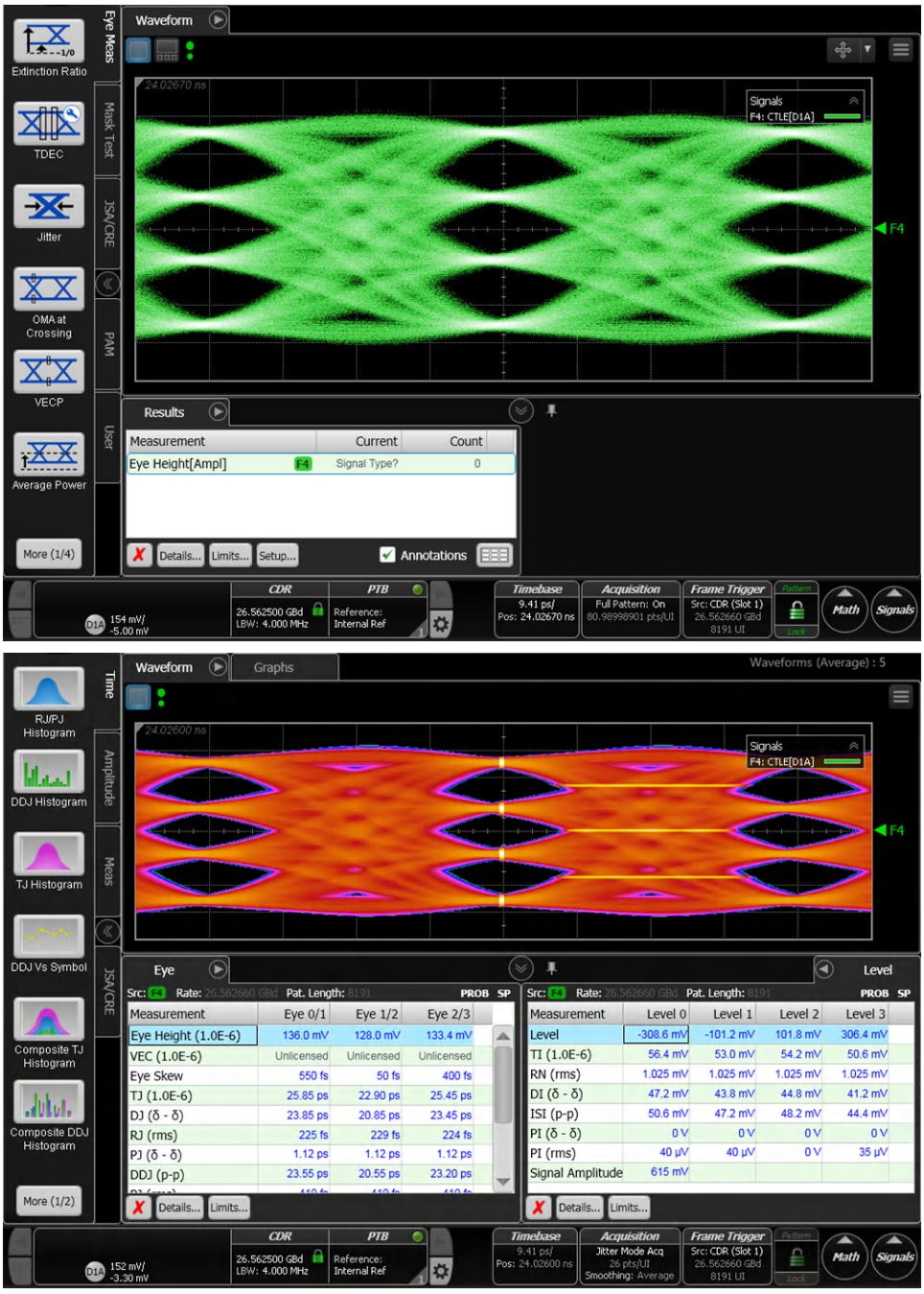


Figure 3-3. TX Output Eye Diagram and Jitter Measurements

3.4.2 RX Link Test

The RX link test was performed on the TIDA-060043 board according to the procedure outlined in Section 3.3. The resulting BER measurements are shown in Table 3-1.

Table 3-1. RX Link Test BER Measurements

TRIAL	BIT ERROR RATE (BER)
1	6.39×10^{-9}
2	3.42×10^{-8}
3	5.75×10^{-9}

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-060043.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-060043.

4.1.3 Altium Project

To download the Altium project, see the design files at TIDA-060043.

4.2 Tools and Software

Tools

DS560DF410EVM	DS560DF410 Evaluation Module

Software

Latte	Latte Software Request Portal

4.3 Documentation Support

1. Texas Instruments, *DS560DF410 56Gbps Multi-Rate 4-Channel Retimer with Crosspoint* data sheet
2. Texas Instruments, *TPS62865/TPS62867 2.4-V to 5.5-V Input, 4-A and 6-A Synchronous Step-Down Converter in 1.5-mm × 2.5-mm QFN Package* data sheet
3. Texas Instruments, TPS7A52 2-A, High-Accuracy (0.5%), Low-Noise (4.4 μV_{RMS}), LDO Voltage Regulator data sheet
4. Texas Instruments, *TLV702 300-mA, Low-I_Q, Low-Dropout Regulator* data sheet
5. Texas Instruments, *TXB0108 8-Bit Bidirectional Voltage-Level Translator with Auto-Direction Sensing and ±15-kV ESD Protection* data sheet

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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