# Design Guide: TIDA-020065 Automotive Smart Fuse Reference Design



# Description

This reference design overcomes challenges commonly associated with replacing the standard melting fuse. By implementing the TPS1213-Q1 high-side switch controller, INA296B-Q1 current sense amplifier, and a microcontroller, this design provides I<sup>2</sup>t overcurrent protection, low-power mode to minimize power consumption, and the capability of driving resistive, capacitive, and inductive loads. The design contains many configuration options, including bidirectional current sense, that allows engineers to run a variety of tests for high-current smart fuse applications.

#### Resources

TIDA-020065	Design Folder
TPS1213-Q1, INA296B-Q1	Product Folder
LM74704-Q1, TPS7B81-Q1	Product Folder
TPS22919-Q1, MSPM0L1306-Q1	Product Folder



Ask the TI E2E<sup>™</sup> support experts

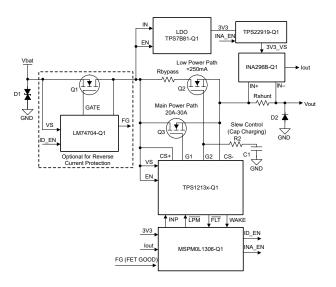
#### Features

- Software-based I<sup>2</sup>t fuse algorithm through MSPM0L1306-Q1
- Prevents uncontrolled inrush current at start-up through gate slew-rate limiting circuit for driving capacitive loads
- 38µA in low-power mode (without MSPM0L1306-Q1)
- Configurable automatic load wakeup
- · Reverse-current and polarity protection
- Unidirectional or bidirectional current sense

## Applications

- 12V, 48V Power distribution box
- Zone control module





1



# **1** System Description

The TIDA-020065 automotive smart fuse design is targeted for power-distribution box and zone-control module systems. As vehicles shift from domain-based architecture to zone-based architecture, these systems aim to replace the standard melting fuse with a semiconductor design to allow for the following:

- 1. Resettable fuses, which allow for optimized cable wiring as fuses no longer need to be in an easily-accesible location.
- 2. Improved time-current characteristics across temperature, which allows for optimized harness cable diameter and reduced cost due to less variability between devices compared to standard melting fuses.

Nevertheless, replacing the melting fuse introduces the following challenges:

- 1. Wire harness protection during overload and short-circuit events while avoiding tripping during peak load transient events
- 2. Protect the FETs from uncontrolled inrush currents while charging load bulk capacitors
- 3. Reducing semiconductor power consumption in key-off state for powered-at-all-times loads

The TIDA-020065 aims to demonstrate how these challenges can be addressed at a system-level for highcurrent loads. This design features the TPS1213-Q1 device for driving a main power path in the drive state, and a low power path for the key-off state. This design also features the INA296B3-Q1 device which is used to sense the load current so the MSPM0L1306-Q1 can run a software-based I<sup>2</sup>t algorithm to replicate fuse behavior.

## 1.1 Terminology

SC	Short-circuit
ECU	Electronic Control Unit
FET	Field-effect transistor
MOSFET	Metal-oxide semiconductor field-effect transistor
l <sup>2</sup> t	Current squared through time
Inom	Nominal current rating
INP	TPS1213-Q1 external FET control input
nLPM	TPS1213-Q1 low-power mode input
WAKE	TPS1213-Q1 automatic load wake up indicator
nFLT	TPS1213-Q1 fault indicator
I <sub>LWU</sub>	Load wakeup threshold current
ADC	Analog-to-digital converter
GPIO	General Purpose Input Output
PWM	Pulse-Width Modulation
EMI	Electromagnetic interference
CE	Conducted Emissions
RE	Radiated Emissions
EUT	Equipment under test



# **1.2 Key System Specifications**

Table 1-1. Key System Specifications				
SYMBOL	PARAMETER	SPECIFICATION	DETAILS	
V <sub>BAT</sub>	Input voltage range	4V-40V	12V DC input. Input and output capacitors must be replaced to make use of the full operating voltage range.	
I <sub>out,max</sub>	ut,max Maximum load current 57A Connectors have a rating of 57A		Connectors have a rating of 57A	
t <sub>charge</sub>	Capacitive precharge time	10ms	_	
I <sub>SC</sub>	Short-circuit threshold	hort-circuit threshold About 100A —		
t <sub>SC</sub>	Short-circuit response time	< 6µs		
I <sub>LWU</sub>	Load wakeup threshold	About 200mA	_	
I <sub>Sense Range</sub>	Current sense range	0A to 66A	Unidirectional current sense configuration. LM74704-Q1 components must be removed to allow for reverse current.	

Tabla 4

1 Kov Svotom Specifications

# 2 System Overview

# 2.1 Block Diagram

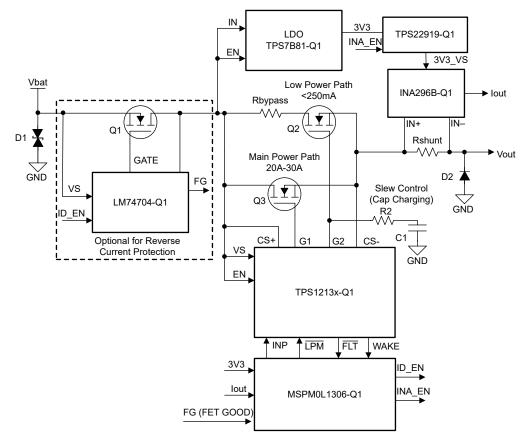


Figure 2-1. TIDA-020065 Block Diagram

# 2.2 Design Considerations

The TPS1213-Q1 high-side switch controller is able to drive an external main power-path FET and an external low power path FET with the use of the nLPM and INP control inputs. See Table 2-1 for information on how nLPM and INP are used to control the low power path and main power path FETs.

PARAMETERS	INP (LOW)	INP (High)
nLPM (Low)	Pulling nLPM low forces the TPS1213-Q1 into low power mode, drives the low power path FET (Q3), and enables automatic load-wakeup.	Pulling nLPM low forces the TPS1213-Q1 into low power mode, drives the low power path FET (Q3), and enables automatic load-wakeup.
nLPM (High)	Pulling nLPM high forces the TPS1213-Q1 into active mode. Pulling INP low turns off the FET of the main power path (Q2).	Pulling INP high turns on the main power path (Q2) if nLPM is high.

#### Table 2-1. TPS1213-Q1 INP and nLPM Truth Table

When discussing vehicle states, using the low power path is analogous to leaving a vehicle in parked (key-off) mode to minimize power consumption. When the vehicle is driving, ECUs need to run at normal operation, so the main path is used to support and protect higher current loads. The TPS1213-Q1 also features automatic load wakeup to quickly transition from low-power mode to active mode when the load current exceeds the configurable load wakeup threshold. All components were selected to minimize the  $I_Q$  during low-power-mode operation. The TPS22919-Q1 load switch was used to disable the INA296B-Q1 in low power mode to further reduce system  $I_Q$ .

For capacitive loads that incur large inrush currents, a gate slew-rate limiting circuit was added on the gate of the low power path so at start-up, the load capacitors can be charged by slowly driving the gate high. Precharging the load capacitors using this method limits the inrush current and prevents false shutdowns from the various time-current characteristics defined for this design.

The INA296B-Q1 and MSPM0L1306-Q1 devices were selected to implement the  $I^{2t}$  Fuse Algorithm. The INA296B-Q1 features precise current sense, which is fed to an ADC peripheral in the MSPM0L1306-Q1. By constantly monitoring the current in active mode, overload events promptly shut down the output according to the software-based I<sup>2</sup>t fuse algorithm to protect the wire harnesses and load. Short-circuit protection is also featured in this design through the TPS1213-Q1; the TPS1213-Q1 monitors the V<sub>DS</sub> of the main FET and signals a fault when V<sub>DS</sub> exceeds a value configurable in hardware.

Finally, the INA296B-Q1 has both unidirectional and bidirectional current sensing capabilities, making this design fit for many kinds of loads including resistive, capacitive, and inductive loads. Reverse current can be monitored through the TPS1213-Q1 but requires removal of the LM74704-Q1 ideal diode control to allow reverse current to the power supply.

4

# 2.3 Highlighted Products

# 2.3.1 TPS1213-Q1 45V, Low I<sub>Q</sub>, Automotive High-Side Switch Controller With Low-Power Mode and Adjustable Load Wakeup Trigger

The TPS1213-Q1 is a 45V, low  $I_Q$  smart high-side driver with protection and diagnostics. With a wide operating voltage range of 3V–40V, the device is an excellent choice for 12V system designs. The device can withstand and protect the loads from negative supply voltages down to –40V.

The device integrates two gate drives with 1.69A source and 2A sink capacity to drive MOSFETs in the main path and 165µA source, 2A sink capacity for the low power path.

In the low power mode with LPM = Low, the low-power path FET is kept ON and the main FETs are turned OFF. The device consumes a low  $I_Q$  of 35µA (typical) in this mode. Auto load wakeup threshold to enter into active state can be adjusted using the ISCP/LWU pin.  $I_Q$  reduces to 1µA (typical) with EN/UVLO low. The device features the WAKE output pin to indicate the mode of operation (Active, Low power mode).

The device provides adjustable short-circuit protection using MOSFET VDS sensing or by using an external RSNS resistor. Auto-retry and latch-off fault behavior can be configured. The device also features diagnosis of the internal short-circuit comparator using external control on the SCP\_TEST input. The device indicates fault (FLT) on open drain output during short circuit, charge pump undervoltage, and input undervoltage conditions.

The TPS1213-Q1 is available in a 19-pin VSSOP package.

# 2.3.2 INA296x-Q1 AEC-Q100, –5V to 110V, Bidirectional, 1.1MHz, 8V/µs, Ultra-Precise Current-Sense Amplifier

The INA296x-Q1 is an ultra-precise, bidirectional current-sense amplifier than can measure voltage drops across shunt resistors over a wide common-mode range from -5V to 110V, independent of the supply voltage. The high-precision current measurement is achieved through a combination of low offset voltage (±10µV, maximum), small gain error (±0.01%, maximum), and a high DC CMRR (typically 166dB). The INA296x-Q1 is not only designed for high-voltage, bidirectional DC current measurements, but also for high-speed applications (such as transient detection and fast overcurrent protection) with a high-signal bandwidth of 1.1MHz and fast settling time.

The INA296x-Q1 operates from a single 2.7V to 20V supply, drawing 2.5mA of supply current. The INA296x-Q1 is available in five gain options: 10V/V, 20V/V, 50V/V, 100V/V, and 200V/V. Multiple gain options allow for optimization between available shunt resistor values and wide output dynamic range requirements.

The INA296x-Q1 is specified over an operating temperature range of -40°C to +125°C.

5

# **3 System Design Theory**

# 3.1 Low-Power Mode Considerations

All components were selected to consume less than  $40\mu$ A in low-power mode. This quiescent current is mostly comprised from the TPS1213-Q1, which consumes a low I<sub>Q</sub> of 35µA when driving the low-power path FET. Since the INA296B-Q1 does not have an enable pin, the TPS22919-Q1 load switch was used to control the state of the INA296B-Q1 in low-power mode. Table 3-1 shows the quiescent current for all devices in low-power mode.

DEVICE	I <sub>Q</sub> (LOW-POWER MODE)	
TPS1213-Q1	35µA	
INA296B-Q1	N/A	
TPS22919-Q1	0.002µA	
TPS7B81-Q1	2.7µA	
LM74704-Q1	1μΑ	
MSPM0L1306-Q1(Standby Mode)	1.4µA	

Table 3-1.	Component	Quiescent	Currents
------------	-----------	-----------	----------

Figure 3-1 shows the TPS1213-Q1 schematic. Because the LM74704-Q1 is disabled in low-power mode, a drop-in output voltage around 0.7V is expected due to the internal FET diode of Q1 conducting.

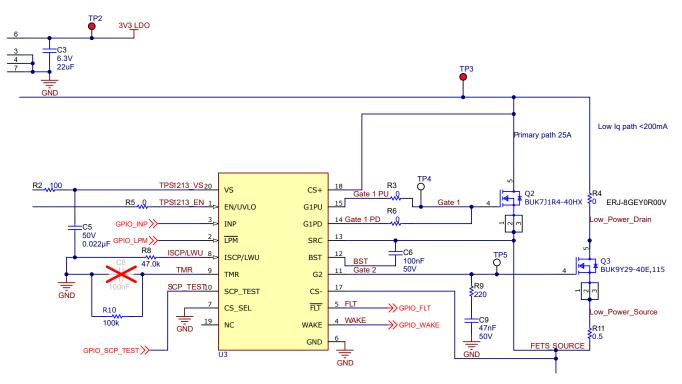


Figure 3-1. TPS1213-Q1 Schematic

(1)

(2)

(4)

When selecting the load wakeup trigger threshold, which is 200mA for this design, use Equation 1:

$$R_{BYPASS}(\Omega) = \frac{(2\mu A \times R_{ISCP} + 19mV)}{I_{LWU}} - R_{DSON\_BYPASS}$$

where

- R<sub>ISCP</sub> (R8) is the resistor selected based on the set short-circuit threshold using Equation 5
- I<sub>LWU</sub> is the desired load current wakeup threshold
- $R_{\text{DSON BYPASS}} = 25.8 \text{m}\Omega$
- R<sub>BYPASS</sub> also helps to limit the current as well as stress on Q3 during power up into short-circuit

Either R4 or R11 can be used for the R<sub>BYPASS</sub> depending if a high-side or low-side resistor is desired.

For pre-release TPS1213-Q1 silicon, use Equation 2 instead of Equation 1.

$$R_{\text{BYPASS}}(\Omega) = \frac{(2\mu A \times R_{\text{ISCP}} + 10mV)}{I_{\text{LWU}}} - R_{\text{DSON}} + R_{\text{DSON}}$$

#### 3.2 Precharge Circuit Considerations

To control excessive inrush current imposed by capacitive loads at start-up, an RC circuit was added on the gate driver (G2) for the low-power path. The external capacitor, C9 ( $C_g$ ), reduces gate turn-on slew rate and controls the inrush current.

Equation 3 and Equation 4 were used to set the 10ms specification of the precharge period:

$$C_{g} = \frac{C_{\text{Load}} \times I(G)}{I_{\text{Inrush}}}$$
(3)

$$I_{Inrush} = \frac{C_{Load} \times V_{BAT}}{T_{Charge}}$$

where

- I<sub>(G)</sub> = 165µA
- $\dot{V}_{BAT}$  represents the input voltage
- I<sub>Inrush</sub> represents the expected peak inrush current
- T<sub>Charge</sub> represents the expected precharge time

The system enters this precharge state through the MSPM0L1306-Q1 control. At start-up, the low power path FET is slowly driven first for 15ms before the system transitions to active state.

**Note** Even though C9 ( $C_g$ ) can be modified to change the precharge time, the MSPM0L1306-Q1 only keeps the system in precharge mode for 15ms.

## **3.3 Short-Circuit Protection**

The TPS1213-Q1 features configurable short-circuit protection. R8 ( $R_{ISCP}$ ) sets the SC protection threshold, whose value can be calculated using Equation 5.

$$R_{\rm ISCP}(\Omega) = \frac{I_{\rm SC} \times R_{\rm DS}(on) - 19mV}{2\mu A}$$

where

R<sub>DS(on)</sub> = 1.06mΩ

(5)



For pre-release TPS1213-Q1 silicon, use Equation 6 instead of Equation 5.

$$R_{ISCP}(\Omega) = \frac{I_{SC} \times R_{DS(on)} - 10mV}{2\mu A}$$
(6)

To set 100A as the SC protection threshold, R8 is calculated to be  $48k\Omega$  using Equation 6. The closest standard value of  $47k\Omega$  was selected.

By leaving C8 ( $C_{TMR}$ ) depopulated, a fast SC response time less than 6µs is selected. Nonetheless, refer to Equation 7 to modify the short-circuit response time.

$$C_{\rm TMR} = \frac{I_{\rm TMR} \times t_{\rm SC}}{1.1} \tag{7}$$

where

- I<sub>TMR</sub> is internal pullup current of 80µA
- t<sub>SC</sub> is the short-circuit response time

R10 ( $R_{TMR}$ ) serves to keep the TMR pin clamped low for latch-off behavior during SC events. nFLT asserts low at the same time, requiring the user to attempt to clear the latch using S2 or S3. To change from latch-off to auto-retry behavior, refer to Equation 8 for automatically recovering from SC events:

$$t_{RETRY} = 22.7 \times 10^6 \times C_{TMR}$$

(8)

#### 3.4 LM74704-Q1 Enable

The LM7404-Q1 enable state can be configured to be always on or controlled by the MSPM0L1306-Q1. Figure 3-2 shows that populating R1 results in the LM74704-Q1 always being enabled. The LM74704-Q1 enable is also tied to a GPIO output of the MSPM0L1306-Q1. Populating R19 allows the MSPM0L1306-Q1 to control the LM74704-Q1 enable state, minimizing  $I_Q$  in low-power mode.

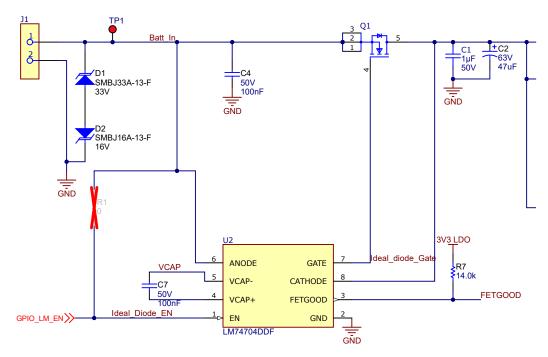


Figure 3-2. LM74704-Q1 Enable Connection

CAUTION Do not populate R1 and R19 at the same time.

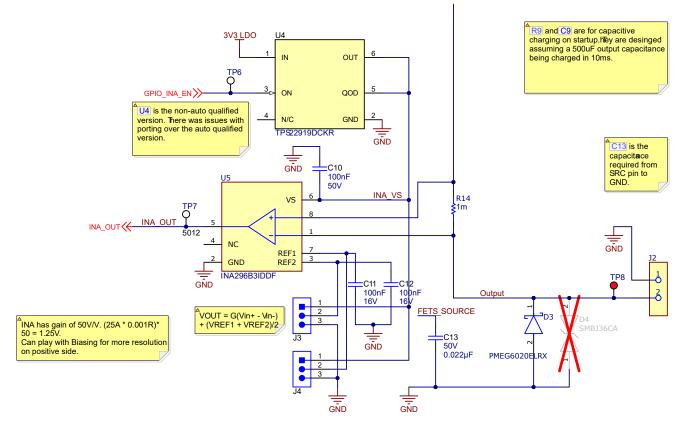
8

# 3.5 Headers

Several configuration options were added to this design to allow for different testing conditions.

#### 3.5.1 Headers for Configuring INA296B-Q1

J3 and J4 both set the reference voltages of the INA296B-Q1. Therefore, the jumpers can be set according to Table 3-2 for different current-sense configurations. Figure 3-3 shows the INA296B-Q1 schematic.



#### Figure 3-3. INA296B-Q1 Schematic

#### Table 3-2. INA296B-Q1 Configuration

J3 SETTING (V <sub>REF1</sub> )	J4 SETTING (V <sub>REF2</sub> )	CONFIGURATION
GND	GND	Unidirectional current sensing (0A to 66A)
GND	3V3	Bidirectional current sensing (-33A to 33A)
3V3	GND	Bidirectional current sensing (-33A to 33A)
3V3	3V3	Unidirectional reverse current sensing (-66A to 0A)

$$V_{\text{OUT, INA}} = G(V_{\text{IN}+} - V_{\text{IN}-}) + \frac{V_{\text{REF1}+}V_{\text{REF2}}}{2}$$

#### where

- V<sub>OUT,INA</sub> is the current sense output
- $V_{IN+} V_{IN-}$  is the voltage drop across the shunt resistor R14
- G is the gain of the current sense amplifier (G = 50)

#### Note

TIDA-020065 software does not have any special logic for reverse-current monitoring. The softwarebased I<sup>2</sup>t algorithm operates correctly only for the forward-current option.

9

# 3.5.2 Headers for Configuring TPS1213-Q1

Headers were added for testing the TPS1213-Q1 independently of the MSPM0L1306-Q1.

Table 5-5. If 61215-& Founder Configurations			
JUMPER	PIN	CONFIGURATION	DESCRIPTION
J5	INP	3V3	Turns on the FET of the main power path (Q2) if LPM = 3V3
12		GND	Turns off the main power FET (Q2) if LPM = 3V3
J6	LPM	3V	Forces the TPS1213-Q1 to Active mode. This disables the FET of the low-power path (Q3) and allows the FET of the main power path (Q2) to be toggled on or off by setting the INP pin (J5)
90	LPINI	GND	Forces the TPS1213-Q1 into low-power mode, turning on the FET of the low-power path (Q3) and disabling the FET of the main power path (Q2)
10		3V3	Used for diagnosing short-circuit protection. This setting forces a short-circuit flag inside the TPS1213-Q1
J8 SCP_TEST		GND	Removes the short-circuit flag inside the TPS1213-Q1

#### Table 3-3. TPS1213-Q1 Jumper Configurations

#### CAUTION

Use of J5, J6, and J8 are not recommended if MSPM0L1306-Q1 is flashed and is on the board. Tie nRST to GND with J7 to prevent damage to the MSPM0L1306-Q1 if use is desired.

#### 3.6 Software Considerations

Figure 3-4 shows a state machine that best describes the TIDA-020065. Initially, the MCU boots up and enters precharge mode to charge the load capacitors for 15ms. After this 15ms period has expired, the system transitions over to active mode by pulling nLPM high.

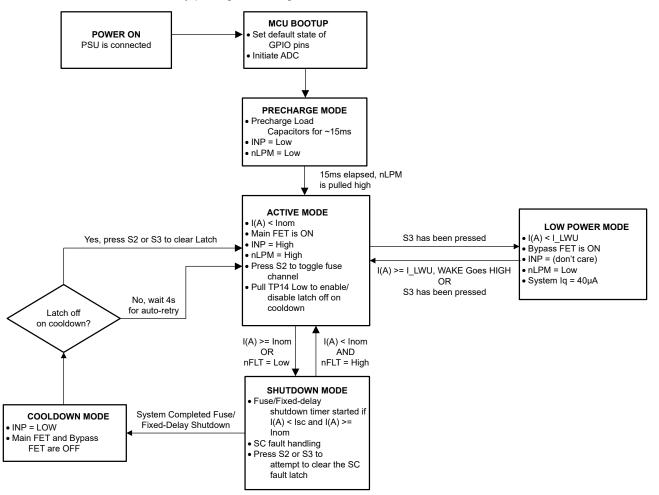


Figure 3-4. TIDA-020065 State Machine



In active state, the main FET is being driven for loads up to 30A. S3 can be pressed to transition the system from active to low power mode. S2 can also be used to switch between the programmed time-current fuse characteristics.

The ADC peripheral of the MSPM01306 collects samples every 100µs to constantly monitor the output current in active mode. When an overload current is detected, the system promptly transitions from active to shutdown mode. Depending on how long the current pulse is active, and how high the pulse is, the software uses the programmed time-current characteristics to protect the wire harnesses and load for the current ranges shown in Figure 3-5.

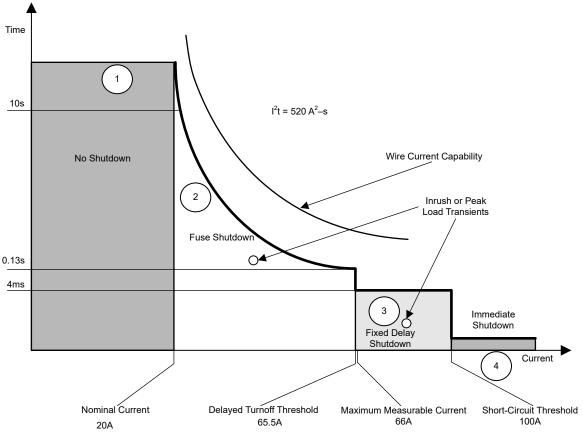


Figure 3-5. TIDA-020065 Time-Current Characteristics

The software  $l^{2}t$  algorithm replicates the behavior of an actual melting fuse; the output is shutdown before peak load transients or other overcurrents cross the wire current capability and damage the vehicle wiring. The  $l^{2}t$  algorithm is best explained by Equation 10.

$$t_{\text{Shutdown}} = \frac{l^2 t}{l_{\text{Load}}^2 - l_{\text{Nom}}^2}$$
(10)

where

- I<sup>2</sup>t is the melting fuse constant
- I<sub>Nom</sub> is the nominal current rating of the fuse channel in use
- t<sub>Shutdown</sub> is the expected shutdown time of the fuse when there is an overcurrent detected



To better simulate a real fuse,  $I_{\text{form}}$  is subtracted from the  $I_{\text{form}}^{\text{coad}}$  measurement every time an ADC sample is taken. This addition allows the smart fuse to operate at the Inom threshold and to avoid falsely shutting down due to normal load transients.

To bypass limitations with only being able to run the  $l^2t$  algorithm up to the maximum monitorable current, which is 66A in this design, a fixed-delay shutdown threshold was added to shutdown the output at a fixed time up until the SC threshold. Although 4ms was chosen for the fixed-delay shutdown time for this design, set this time according to what current pulses are allowed in the system.

When either fuse shutdown or fixed-delay shutdown occurs, the system transitions over to cooldown mode, where INP is pulled low and the system is allowed to recover from the overload event. By default, the MSPM0L1306-Q1 automatically pulls INP high again in 4s to recover the output. Nonetheless, the software can be configured by pulling TP14 low for latch-off behavior in cooldown mode. The output now stays off indefinitely until user input is received by pressing either S2 or S3. Comparing this behavior to a melting fuse shows that melting fuses have to be replaced whereas this design allows for resettable overcurrent protection. In a more realistic application, the software considers the thermals of the vehicle wiring to make sure that enough time has elapsed to cool the wire harnesses down.

For immediate shutdown, the short-circuit protection feature of the TPS1213-Q1 is used. nFLT is pulled low to signal to the MSPM0L1306-Q1 that a hardware fault was detected. In this state, pressing S2 or S3 toggles INP which clears the SC protection latch of the TPS1213-Q1.

#### 3.6.1 Fuse Channel Definition

The TIDA-020065 software implements 4 different fuse channels. Table 3-4 shows the time-current characteristics of these channels.

CHANNEL NUMBER	I <sub>NOM</sub> (A)	l <sup>2</sup> t (A2s)	COOLDOWN AFTER FUSE SHUTDOWN (s)	SOFTWARE CURRENT LIMIT (A)	PULSE WIDTH FOR FIXED-DELAY SHUTDOWN (ms)	COOLDOWN AFTER FIXED-DELAY SHUTDOWN (s)
1	15	340	4	65.5	4	4
2	20	520	4	65.5	4	4
3	25	1000	4	65.5	4	4
4	30	1500	4	65.5	4	4

#### Table 3-4. Fuse Channel Definitions

For all channels, the immediate shutdown threshold is fixed by hardware components at 100A. The TPS1213-Q1 is configured for latch-off and fastest shutdown during SC events (< 6µs).

#### 3.6.2 Software Functions

Table 3-5 shows the descriptions of components tied to a software function.

Table 3-5. Software F	unctions
-----------------------	----------

COMPONENT	FUNCTION	DESCRIPTION
S1	MCU RESET	Press S1 to pull nRST low, which resets the MSPM0L1306-Q1
S2	Toggle Fuse Channel	When pressed, D9 flashes a number of times to indicate which fuse channel is being used. Example: If D9 flashes 2 times, the system is using Fuse Channel 2.
S3	Toggle Power Mode	Transition the system between low power mode and active mode
TP13	SCP_Test Diagnosis	Pull TP13 to GND to toggle the TPS1213-Q1 SCP_Test input pin. SCP_Test is low by default and is used for diagnosing short-circuit protection.
TP14	Enable or Disable Latch Off in Cooldown Mode	Pull TP14 to GND to enable or disable latch off in cooldown. TP14 is disabled by default. If enabled, D9 blinks 2 times to indicate latch off is enabled in cooldown. Press S2 or S3 to clear the latch and restore the output when an overcurrent fault occurs. If disabled, D9 blinks 1 time to indicate latch off is disabled in cooldown. At cooldown, the MSPM0L1306-Q1 automatically restores the output in 4s.

Indicator LEDs are also included in this board as shown in Table 3-6.

LED	NAME	DESCRIPTION
D6	Output On	Indicates the output is on and not shutdown due to any faults. Place a jumper on J9 to enable D6.
D7	LPM On	Indicates the system is in low-power mode. Place a jumper on J10 to enable D7. (When taking current measurements in low-power mode, depopulate jumpers on J9 and J10)
D8	Fault Detected	Indicates that an overcurrent has been detected or that the TPS1213-Q1 nFLT pin has gone low.
D9	Fuse Channel Indicator	Indicates which fuse channel is being used. Example: If D9 flashes 2 times, the system is using Fuse Channel 2.
D5	nFLT Low	Indicates the TPS1213-Q1 nFLT pin has gone low.

#### Table 3-6. LED Indicators and Descriptions

# 3.7 Optional Output TVS Diode

D4 is an optional TVS diode footprint.

TI recommends an SMBJ36CA be used with the TPS1213-Q1 if a TVS diode is needed.

# 4 Hardware, Software, Testing Requirements, and Test Results

#### 4.1 Hardware Requirements

A DC power supply and load are required for evaluating the TIDA-020065.

#### 4.2 Software

The TIDA-020065 software was developed using the MSPM0 SDK 1.10.0.05.

#### 4.3 Test Setup

Figure 4-1 shows the typical setup for the TIDA-020065. The input is tied to a DC power supply and the output is tied to an electronic load.

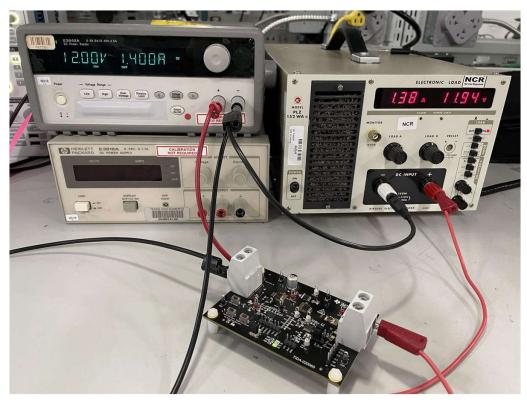


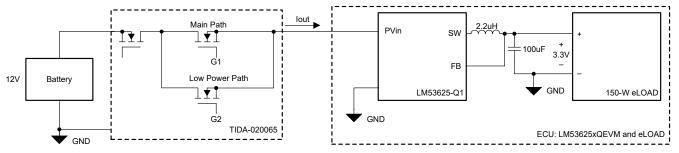
Figure 4-1. Typical TIDA-020065 Setup

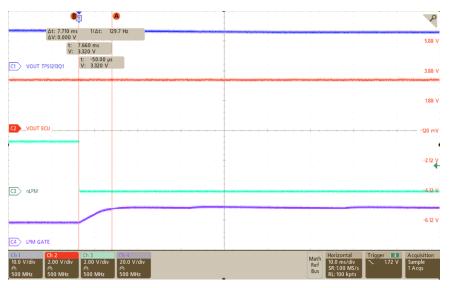


# 4.4 Test Results

#### 4.4.1 State Transition

The test setup for state transitions between low-power mode and active mode involve emulating a simple vehicle ECU with a LM53625xQEVM buck converter and a 150W electronic load configured in constant-current mode.





#### Figure 4-2. State Transition Test Block Diagram

Figure 4-3. Active to Low-Power Mode



In Figure 4-3, the test begins by pressing S3 to trigger the MSPM0L1306-Q1 to transition the system to low-power mode. In this state, nLPM and INP are both pulled low, signaling the TPS1213-Q1 to drive the low power path instead of the main path.

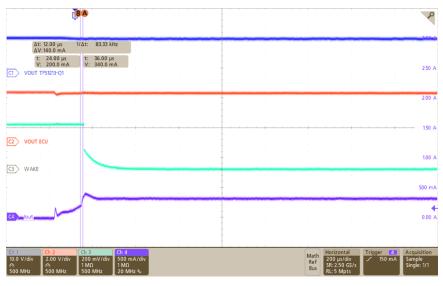


Figure 4-4. Automatic-Load Wakeup

In Figure 4-4, the system is in low-power mode initially, but the electronic load is turned up to cross the automatic load wakeup threshold at 200mA. The TPS1213-Q1 automatically transitions from using the low power path to main path in < 12 $\mu$ s. Concurrently, the WAKE signal asserts low to alert the MSPM0L1306-Q1 to transition the whole system to active mode.

#### 4.4.2 System I<sub>Q</sub> in Low-Power Mode

For this test, an ammeter was connected in series at the  $V_{BAT}$  input to measure the current in low power mode. No load is connected at the output. Figure 4-5 corresponds to the system  $I_Q$  without an MCU, and Figure 4-6 corresponds to the system  $I_Q$  with an MCU.

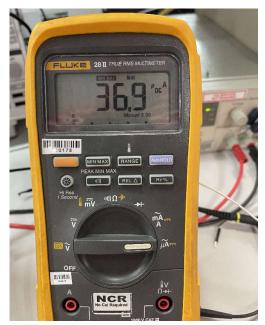


Figure 4-5. System I<sub>Q</sub> Without an MCU

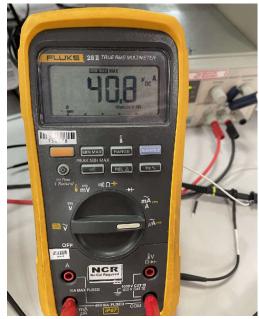


Figure 4-6. System I<sub>Q</sub> With an MCU



## 4.4.3 Precharge Test

This test analyzes the response of the TIDA-020065 to a 1000µF capacitive load.

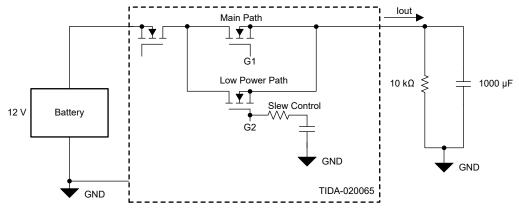


Figure 4-7. Capacitive Charging Test Block Diagram

Figure 4-8 shows the system immediately enters precharge mode upon power up. In hardware, the slew rate control is set to slowly drive the low power path so the load capacitor can be charged in 10ms, which explains why the peak current pulse lasts for about 10ms. After 15ms, the MSPM0L1306-Q1 transitions the system over to active mode by driving the main FET gate (G1). The current probe used in this test is locked to 5A/V, so the actual measured peak current was about 1.3A.

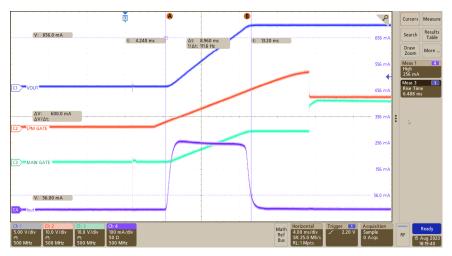


Figure 4-8. Precharging 1000µF Load



#### 4.4.4 Overcurrent Protection

The test setup for verifying the software-based time-current characteristics involves a similar setup as seen in Figure 4-2, except the LM53625xQEVM is removed from the path. A 1000W electronic load is connected directly to the output of the TIDA-020065 and the load is configured in constant resistance mode.

For this test, fuse channel 3 is used, which means  $I_{nom} = 25A$  and  $I^2t = 1000A^2s$ . When the load experiences a constant overcurrent of 36A, a shutdown time of 1.49s is expected. It takes 1.523s for the  $I^2t$  algorithm to pulldown INP and shutdown the output.

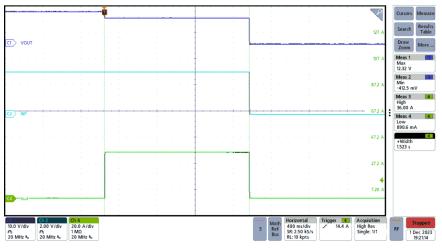


Figure 4-9. Overcurrent Event (I<sub>nom</sub> = 25A, I<sup>2</sup>t = 1000A<sup>2</sup>s)

Figure 4-10 and Figure 4-11 both show results from I<sup>2</sup>t shutdown testing using fuse channel 1 and fuse channel 2, respectively.

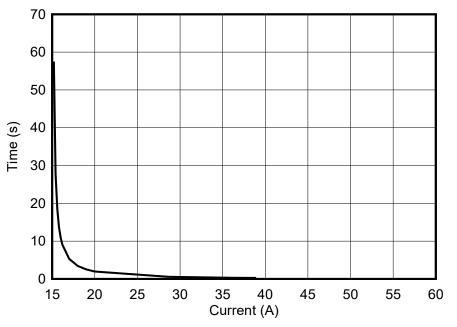


Figure 4-10. I<sup>2</sup>t Tests for Fuse Channel 1 (I<sub>nom</sub> = 15A and I<sup>2</sup>t = 340A<sup>2</sup>s)



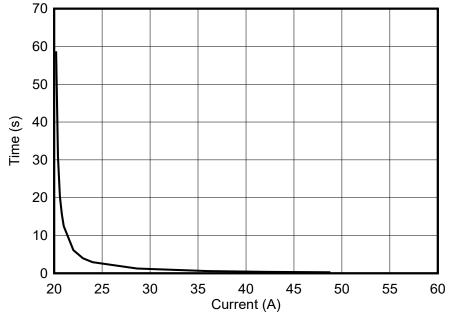


Figure 4-11. I<sup>2</sup>t Tests for Fuse Channel 2 ( $I_{nom}$  = 20A and I<sup>2</sup>t = 520A<sup>2</sup>s)

In addition to fuse I<sup>2</sup>t behavior for overcurrents up to 65.5A, the fixed-delay shutdown behavior was also captured.

For this test, the fixed-delay threshold was set to 65.5A in software. As shown in Figure 4-12, the 65.5A pulse is close to the maximum monitorable current for this design, so the MSPM0L1306-Q1 asserts INP low when the pulse is active for 4ms to shutdown the output.

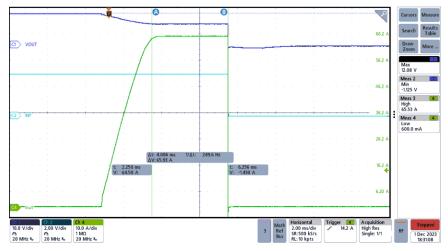


Figure 4-12. Fixed-Delay Shutdown Event



#### 4.4.5 PWM Overcurrent

The purpose of this test is to show the behavior of the TIDA-020065 under various current spikes. For a 20A load with  $I^{2}t$  constant of 340A<sup>2</sup>s and  $I_{nom}$  of 15A, a shutdown is expected in 1.94s. Nonetheless, no  $I^{2}t$  shutdown occurs for the various overcurrent periods which span 1.65s. The period of the PWM load current is 3.3s.

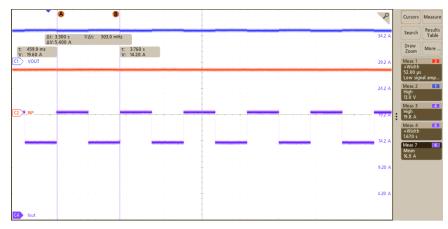


Figure 4-13. PWM Overcurrent Test

#### 4.4.6 Short-Circuit Protection

For this test, the electronic load was turned on initially at 5A and set to constant resistance mode. Then, the "short" option was clicked on the electronic load to initiate a short-circuit event in the TPS1213-Q1. As shown in Figure 4-14, the current spikes up to about 85A before the TPS1213-Q1 turns off the main gate in less than 6µs. In this state, nFLT asserts low and the main gate remains latched off until S2 or S3 are pressed, which signals the MSPM0L1306-Q1 to toggle INP to attempt to clear the latch. If the latch is successfully cleared, nFLT asserts high and alerts the MCU that the fault has been cleared. Figure 4-15 shows an example of successfully recovering from a short-circuit event.

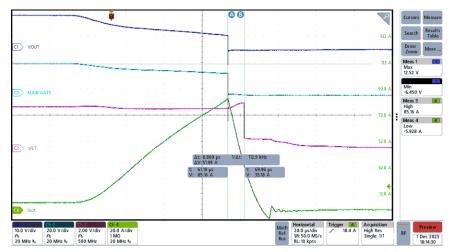


Figure 4-14. Short-Circuit Event





Figure 4-15. Clearing Short-Circuit Latch

#### 4.4.7 Thermal Testing

The TIDA-020065 thermal performance was captured for both 25A and 30A continuous current. For both these tests, the system was allowed to reach thermal equilibrium before capturing a screenshot with a thermal camera. The ambient temperature of the room was 25°C, so for Figure 4-17 a temperature rise of 55.5°C was observed for the FETs.

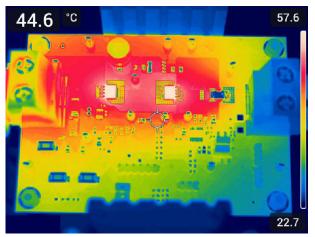


Figure 4-16. 25A Load at Thermal Equilibrium

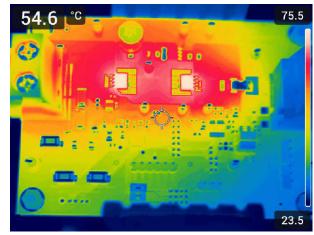


Figure 4-17. 30A Load at Thermal Equilibrium

#### 4.4.8 CISPR-25 Emissions Testing

Section 4.4.8.1 and Section 4.4.8.2 illustrate the EMI performance of the TIDA-020065. These tests show that the TIDA-020065 components pass CISPR-25 requirements without a fully-optimized layout. Tests were conducted for CISPR-25 conducted emissions in the 0.15MHz to 108MHz frequency range, and radiated emissions in the 0.15MHz to 5.925GHz frequency range.

For conducted and radiated emissions testing, emissions were captured under the following test cases:

- Ambient noise floor (EUT power disconnected)
- EUT low power mode (120mA for CE, no load for RE)
- EUT no load
- EUT 3A load

#### where

EUT represents the TIDA-020065

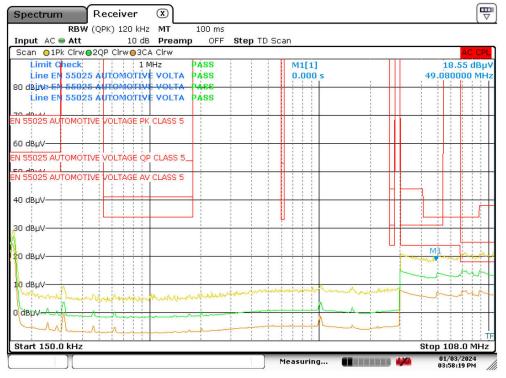


#### 4.4.8.1 Conducted Emissions Testing

Figure 4-18 shows the conducted emissions (CE) test setup. The voltage probe method was used for testing. A 12V car battery is also tied to the LISNs, which are the blue boxes next to the car battery. The EUT is on insulated material with a  $4\Omega$  load connected to the output. The  $4\Omega$  load is locally grounded so the EUT drives 3A in active state.

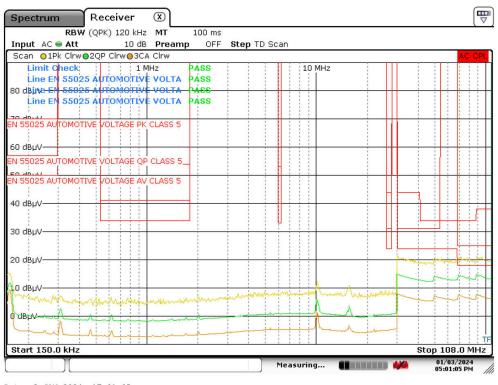


Figure 4-18. Conducted Emissions Test Setup



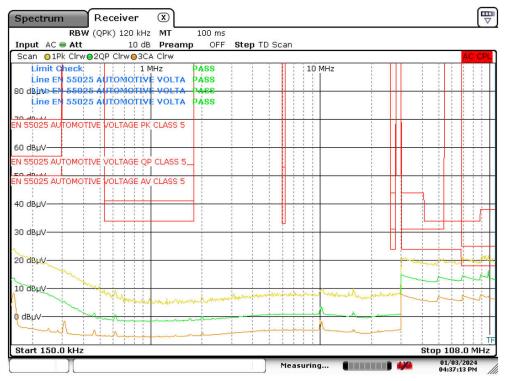
Date: 3.JAN.2024 15:58:18



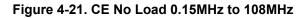


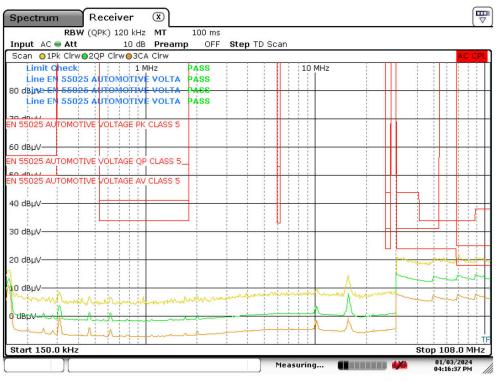
Date: 3.JAN.2024 17:01:05





Date: 3.JAN.2024 16:37:13





Date: 3.JAN.2024 16:16:36



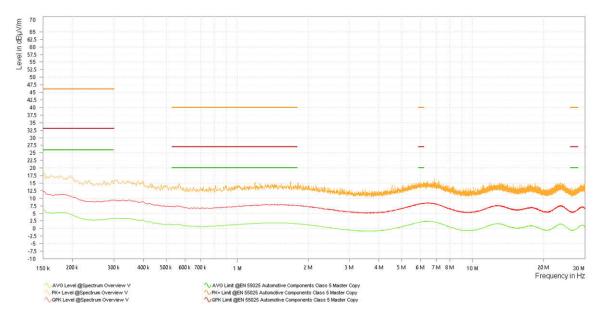


#### 4.4.8.2 Radiated Emissions Testing

Radiated emissions (RE) testing was achieved with 4 different antennas to capture the full frequency range of CISPR-25. A 12V car battery and LISNs are used for these tests. With the EUT tied to the LISNs, the  $4\Omega$  load is wired from the EUT back to the LISN to better replicate an actual application of the EUT. For the tests with monopole, biconical, and horn antenna, tests for low power mode and no load are not shown as these measurements are very similar to the ambient noise floor.

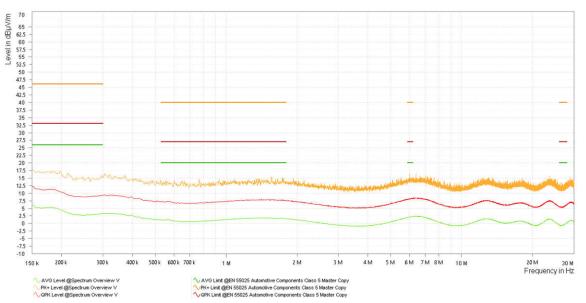


Figure 4-23. RE Setup With a Monopole Antenna: 0.15MHz to 30MHz









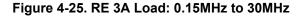
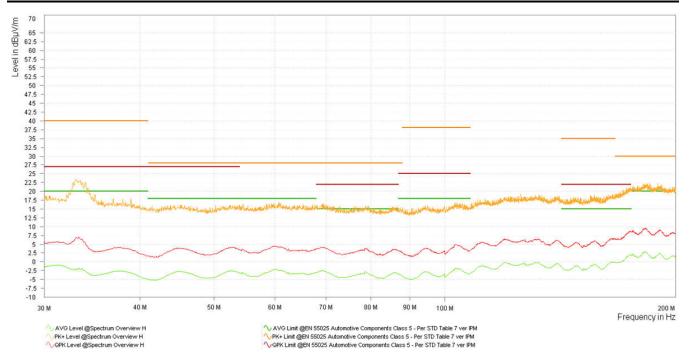




Figure 4-26. RE Setup With a Biconical Antenna: 30MHz to 200MHz





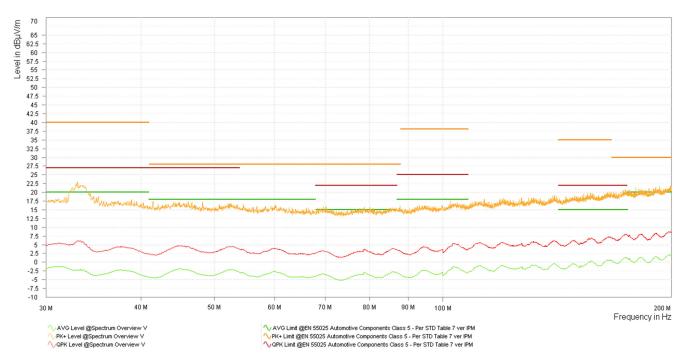


Figure 4-28. RE Ambient Noise Floor Vertical Antenna: 30MHz to 200MHz



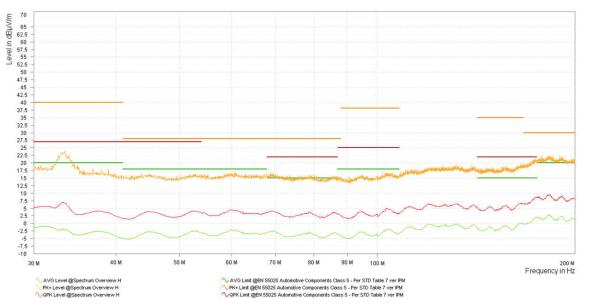


Figure 4-29. RE 3A Load Horizontal Antenna: 30MHz to 200MHz

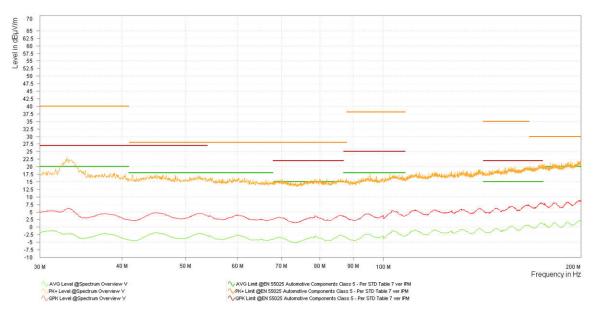


Figure 4-30. RE 3A Load Vertical Antenna: 30MHz to 200MHz



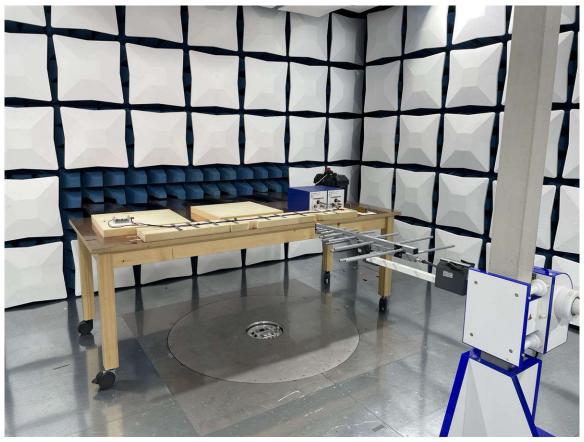


Figure 4-31. RE Setup With a Logarithmic Antenna: 200MHz to 1GHz

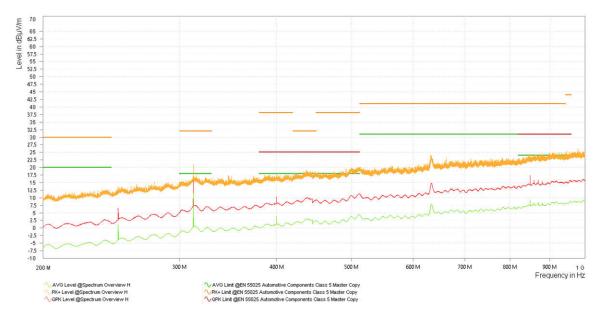


Figure 4-32. RE Ambient Noise Floor Horizontal Antenna: 200MHz to 1GHz



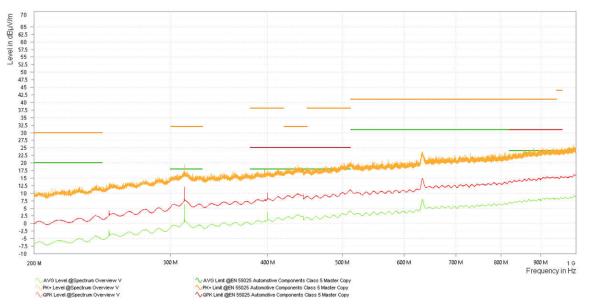


Figure 4-33. RE Ambient Noise Floor Vertical Antenna: 200MHz to 1GHz

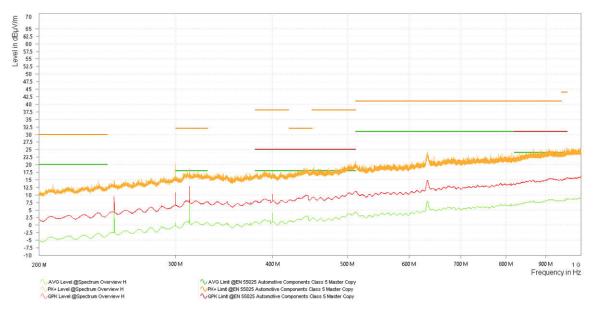
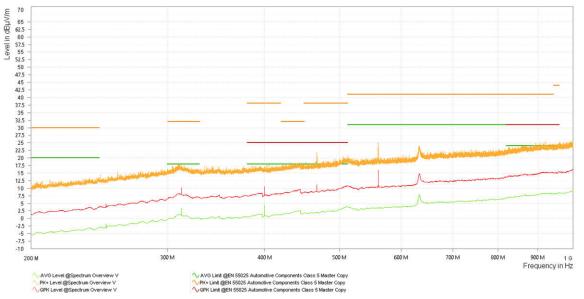


Figure 4-34. RE Low Power Mode Horizontal Antenna: 200MHz to 1GHz







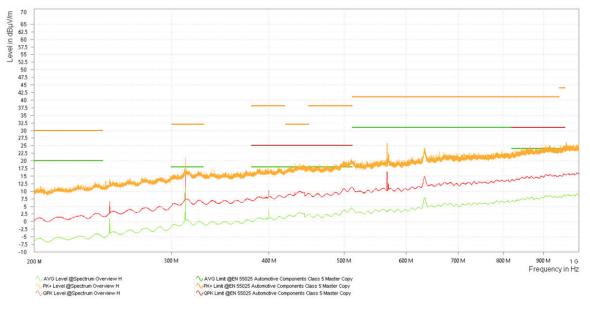


Figure 4-36. RE No Load Horizontal Antenna: 200MHz to 1GHz



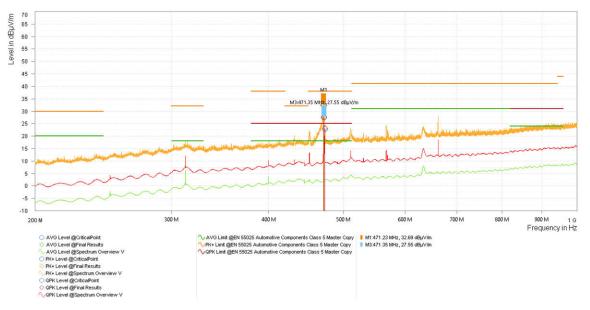


Figure 4-37. RE No Load Vertical Antenna: 200MHz to 1GHz

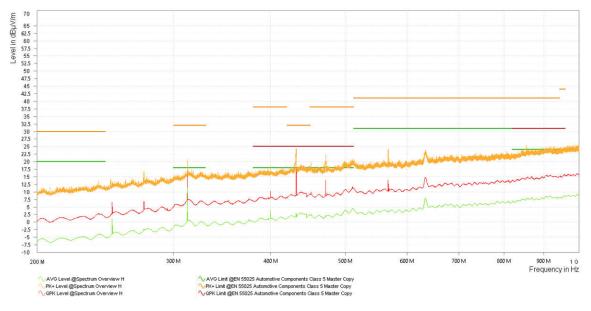


Figure 4-38. RE 3A Load Horizontal Antenna: 200MHz to 1GHz



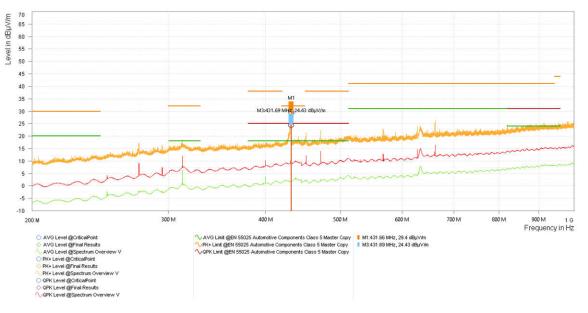


Figure 4-39. RE 3A Load Vertical Antenna: 200MHz to 1GHz

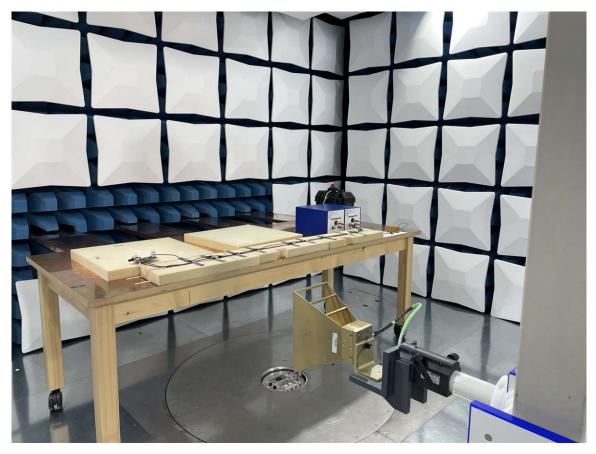


Figure 4-40. RE Setup With a Horn Antenna: 1GHz to 5.925GHz



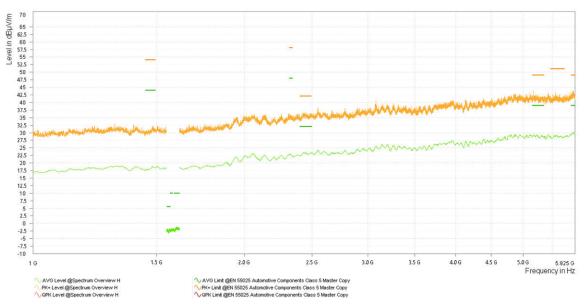


Figure 4-41. RE Ambient Noise Floor Horizontal Antenna: 1GHz to 5.925GHz

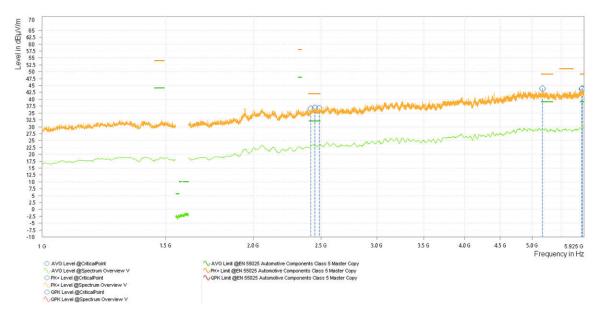


Figure 4-42. RE Ambient Noise Floor Vertical Antenna: 1GHz to 5.925GHz



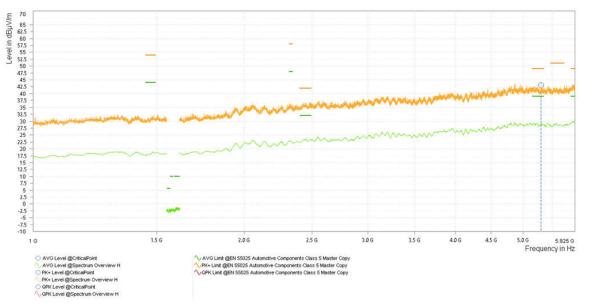
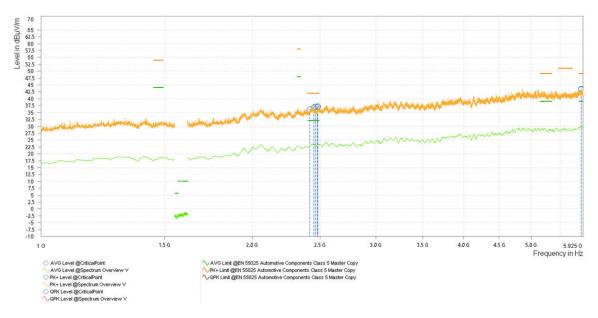
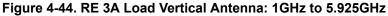


Figure 4-43. RE 3A Load Horizontal Antenna: 1GHz to 5.925GHz





#### 4.4.8.3 Summary of Results

The TIDA-020065 passes all CISPR-25 tests. There are a few critical points observed in Figure 4-37 and Figure 4-39. These are due to the LM74704-Q1 charge pump and these peaks can be improved by increasing the input capacitor (C4) to 220nF and adding a 10nF capacitor in parallel to C4.



# **5** Design and Documentation Support

# 5.1 Design Files

#### 5.1.1 Schematics

To download the schematics, see the design files at TIDA-020065.

#### 5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-020065.

#### 5.1.3 PCB Layout Recommendations

#### 5.1.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-020065.

#### 5.1.4 Altium Project

To download the Altium project files, see the design files at TIDA-020065.

#### 5.1.5 Gerber Files

To download the gerber files, see the design files at TIDA-020065.

#### 5.1.6 Assembly Drawings

To download the assembly drawing files, see the design files at TIDA-020065.

#### 5.2 Documentation Support

- 1. Texas Instruments, *TPS1213-Q1 45-V Low I<sub>Q</sub> Automotive High Side Switch Controller With Low Power Mode and Adjustable Load Wakeup Trigger Data Sheet*
- 2. Texas Instruments, INA296x-Q1 AEC-Q100, –5 V to 110 V, Bidirectional, 1.1 MHz, 8 V/µs, Ultra-Precise Current Sense Amplifier Data Sheet

#### **5.3 Support Resources**

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 5.4 Trademarks

E2E<sup>™</sup> and TI E2E<sup>™</sup> are trademarks of Texas Instruments. All trademarks are the property of their respective owners.

## 6 About the Author

**DAVID MARTINEZ** is a systems engineer at Texas Instruments. As a member of the Automotive Systems Engineering team, David specializes in power distribution boxes, helping create end equipment block diagrams and reference designs for automotive customers. David earned his bachelors of science in electrical engineering from Texas A&M University at College Station, Texas.

**ROBERT SMITH** is part of the Automotive Field Applications team and with a focus on HEV and EV systems. He graduated from Oregon State University with a bachelor's of science in Electrical and Computer engineering. Robert is enamored with all types of analog circuits from large power distribution, to RF circuitry, to sensing circuitry.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2024, Texas Instruments Incorporated