Design Guide: TIDA-010936

48V, 850W Small Form Factor Three-Phase GaN Inverter Reference Design for Motor Integrated Drives

Description

This reference design demonstrates a high-power density 12V to 60V 3-phase power stage using three LMG2100R044 100V, 35A GaN half-bridges with integrated GaN FETs, driver and bootstrap diode specifically for motor-integrated servo drives and robotics applications. Accurate phase-current sensing is achieved through the IN241A current sense amplifier, DC-link and phase voltages are also measured allowing validation of advanced sensorless designs, such as the InstaSPIN-FOC™. The design offers a TI BoosterPack™ compatible 3.3V I/O interface to connect to a C2000™ MCU LaunchPad™ development kit or C2000™ microcontrollers for quick and easy performance evaluation of TI's GaN technology.

Resources

TIDA-010936	Design Folder
LMG2100, INA241A	Product Folder
INA310A, REF3333, LMR38010	Product Folder
TPSM82821, TXU0304	Product Folder
TMP61, LAUNCHXL-F28P65X	Product Folder

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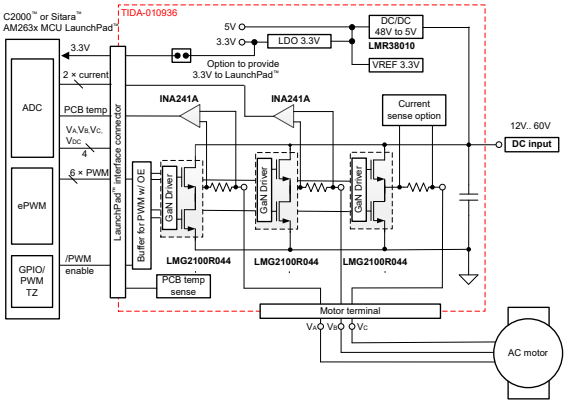
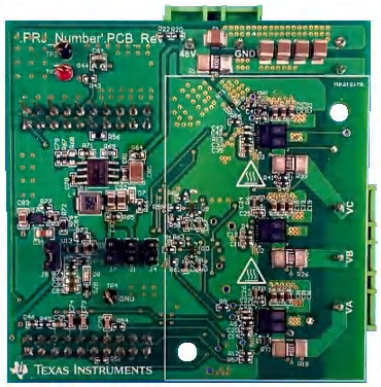
Features

- Small form factor LMG2100R044 GaN half-bridge power stage enables high power density and easy PCB layout
- High efficiency (99.3% peak) at 40kHz PWM enables operation at 25°C ambient up to 16A_{RMS} continuous current without heat sink
- LMG2100R044 enable operation at higher PWM frequencies to help reduce DC-bus capacitor size and height by replacing electrolytic with ceramic capacitors
- Zero reverse recovery losses reduce switch node oscillations
- Low dead time of 16.6ns minimizes phase voltage distortions
- Precision phase current sense with ±33A range using 1mΩ shunt and INA241A amplifier with high PWM rejection

Applications

- Robot servo drive
- Servo drive power stage module
- Linear motor power stage
- Mobile robot motor control
- Drone accessories





1 System Description

Low-voltage 12V to 60V DC-fed three-phase inverters in the power range of 1.5kW are used in many applications such as collaborative robots, automated mobile robots, automated guide vehicles (AGV), servo and non-military drones.

In many of these applications the power electronics is motor integrated and hence has a small form factor. High power efficiency and power density are critical parameters to build smaller and lesser weight collaborative robots with a reduced size and no heat sink.

Higher pulse-width modulation (PWM) switching frequencies up to 100kHz help reduce the DC-bus capacitor; therefore reducing size and height by replacing electrolytic with ceramic capacitors. In addition, higher PWM switching frequencies are desired to reduce the current and hence torque ripple of the motor, especially with low inductance brushless AC motors for more precise control.

Conversely, the inverter losses increase with the switching frequency. With a traditional low-voltage 48V silicon field-effect transistor (Si-FET) inverter, the switching losses at 40kHz PWM can already be significantly higher than the conduction losses and hence dominate the overall power losses. To dissipate the excess heat, a larger heat sink is required. However, the heat sink increases system cost, weight, and space.

The solution to the problem is to use GaN FETs, which have several advantages over Si-FETs. Gallium nitride (GaN) transistors can switch much faster than silicon MOSFETs, thus having the potential to achieve lower switching losses. At high slew rates; however, certain package types can limit GaN FET switching performance. Integrating the GaN FET and driver in the same package reduces parasitic inductances and optimizes switching performance.

The TIDA-010936 reference design has a small form factor, three-phase inverter with three 100V, 35A half-bridge GaN power modules LMG2100R044. The LMG2100R044 integrates the driver and two 80V GaN FETs in a small 5.5mm × 4.5mm QFN package, optimized for extremely low gate loop and power loop impedance. The PCB offers mounting holes for an optional heat sink with the top-side cooled LMG2100R040 GaN-FET power modules. An integrated bootstrap diode helps further reduce space for the high-side GaN-FET bias supply.

For precision and small form factor phase current measurements with high linearity, the reference design employs a low impedance 1mΩ phase current shunt and a differential precision current sense amplifier INA241 with high common mode and high AC common mode transient immunity due to the INA241 integrated PWM rejection. The measurement range is ±33A and is converted into a unipolar output voltage from 0V to 3.3V with a bias voltage of 1.65V for zero current.

The three-phase GaN inverter offers a hardware-based short-circuit projection using high-side DC-link shunt with a high common mode window comparator with a configurable overcurrent threshold, which turns off the PWM buffer. Additional feedback includes the DC-bus voltage as well as the PWM filtered three phase voltages to allow validation of advanced sensorless designs like InstaSPIN-FOC.

The three-phase inverter operates from a wide input voltage range 12V to 60V and offers onboard power management that provides a 5V rail to supply the LMG2100 gate driver and 3.3V band-gap reference well a 3.3V rail for the INA241 current sense amplifiers and temperature switch.

The TIDA-010936 offers a TI BoosterPack compatible 3.3V I/O interface to connect to a C2000 MCU LaunchPad development kit for quick and easy performance evaluation.

1.1 Key System Specifications

The key specifications of the TIDA-010936 small form factor three-phase GaN inverter reference design are provided in Table 1-1. The design can be directly connected to a C2000 MCU LaunchPad development 40-pin instance (J1–J3 and J4–J2). A zero Ohm resistor option is provided on the TIDA-010936 to the power the LaunchPad with 3.3V. Table 1-2 and Table 1-3 introduce the TIDA-010936 pin assignment.

Table 1-1. 3-Phase Inverter Key Specifications

PARAMETER	TYPICAL VALUE	COMMENT
DC input voltage	48V (12V–60V)	80V absolute maximum
Maximum 3-phase continues output current	$16A_{RMS}$	Test condition: No heat sink at 25°C ambient temperature
Maximum output power	825W at 48VDC	At power factor 0.9
Power FET type	GaN technology	Half-bridge power module with integrated high and low side gate drivers (LMG2100)
PWM switching frequency (tested)	20kHz to 80kHz	Higher than 80kHz PWM frequencies supported
PWM dead band	16.66ns	–
Phase currents sense | amplifier	1mΩ shunt | INA241A	Differential, non-isolated current sense amplifier with 50V / V and enhanced PWM rejection (INA241A)
Phase current maximum range	±33A	Scaled to 0V–3.3V, 1.65V bias
PCB layer stack	4-layer, 2oz copper	
GaN-FET PCB area size	16mm × 51mm	3-phase GaN plus shunt
PCB size	68.63mm × 70mm	Dimensions in mil: 2702mil × 2756mil
Temperature range	–40°C to 85°C	
Interface to host processor	TI BoosterPack compatible	See Table 1-2 and Table 1-3 for pin assignment
3.3V or 5V supply option for LaunchPad	Total 600mA (max)	Enable with 0Ω resistor

Table 1-2. Interface Specification Header J2

PIN	SIGNAL	I/O (3.3V)	PIN	SIGNAL	I/O (3.3V)
J2-1	3.3V supply (optional)	O or N/C (R48 not populated)	J2-2	5 supply (optional)	O or N/C (R47 not populated)
J-23	NC		J2-4	GND	GND
J2-5	NC		J2-6	VDC_Bus	O (0-3.3V)(1)
J2-7	NC		J2-8	VA	O (0-3.3V)(1)
J2-9	NC		J2-10	VB	O (0-3.3V)(1)
J2-11	NC		J2-12	VC	O (0-3.3V)(1)
J2-13	NC		J2-14	IA	O (0-3.3V)
J2-15	NC		J2-16	IB	O (0-3.3V)
J2-17	NC		J2-18	Temp	O (0-3.3V)
J2-19	NC		J2-20	NC	

(1) Overvoltage protection with Schottky diodes provides output voltage remains below 3.6V

Table 1-3. Interface Specification Header J3

PIN	SIGNAL	I/O (3.3V)	PIN	SIGNAL	I/O (3.3V)
J3-1	PWM A (high-side)	I (10k PD in buffer)	J3-2	GND	GND
J3-3	PWM A (low-side)	I (10k PD in buffer)	J3-4	NC	
J3-5	PWM B (high-side)	I (10k PD in buffer)	J3-6	NC	
J3-7	PWM B (low-side)	I (10k PD in buffer)	J3-8	NC	
	PWM C (high-side)	I (10k PD in buffer)	J3-10	OC	O
J3-11	PWM C (low-side)	I (10k PD in buffer)	J3-12	NC	
J3-13	NC		J3-14	NC	
J3-15	NC		J3-16	NC	
J3-17	NC		J3-18	NC	
J3-19	NC		J3-20	NC	

2 System Overview

2.1 Block Diagram

Figure 2-1 shows the system block diagram of the three-phase GaN inverter with the TIDA-010936 indicated in the red dotted box.

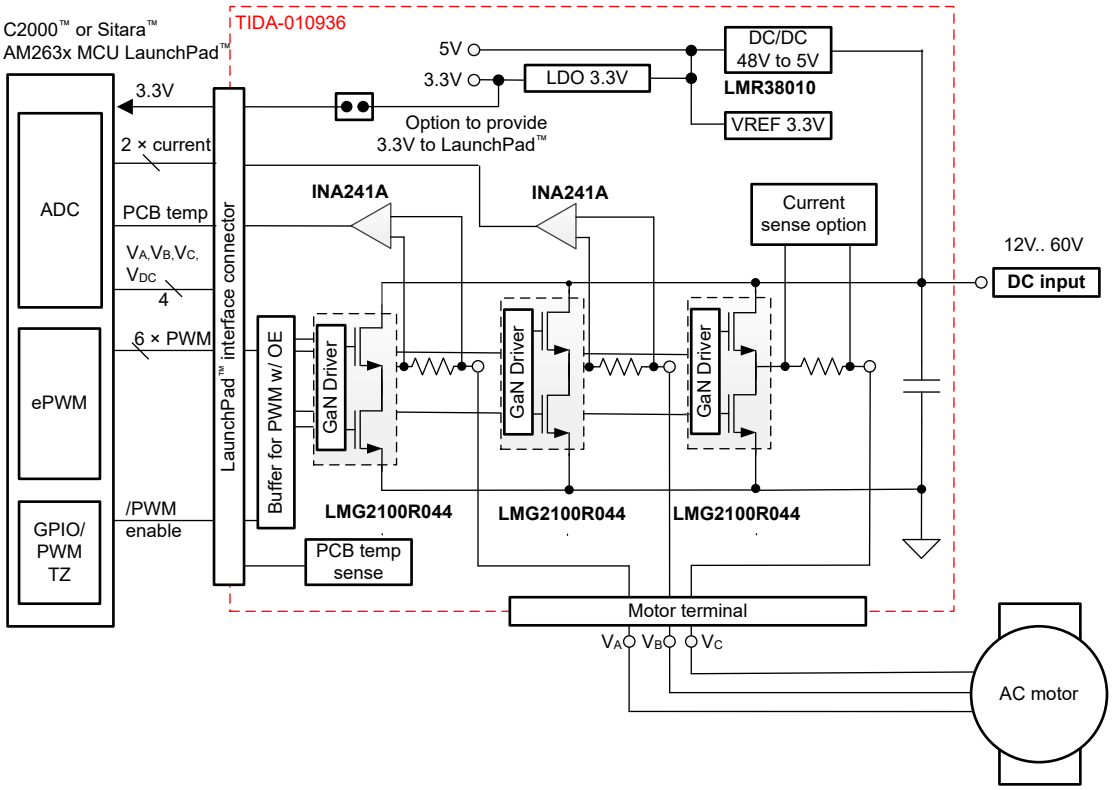


Figure 2-1. TIDA-010936 Block Diagram

2.2 Design Considerations

The design goal was to implement a 3-phase GaN-inverter reference design, which operates from a single DC input voltage from 12V to 60V DC, nominal 48V. A wide input voltage range DC/DC converter LMR38010 generates the 5V rail to supply the GaN-FET power modules and the 3.3V band-gap reference, a 3.3V power modules supplies the current sense amplifiers, input buffer and optional a C2000 MCU LaunchPad development kit.

Each of the three inverter half-bridges employ an integrated 80V, 10A GaN half-bridge module (LMG2100R044) to demonstrate small form factor and high efficiency.

A 1mΩ phase current shunt and a differential current sense amplifier (INA241A) with a gain of 50V / V and a midpoint voltage of 1.65V, set by the 3.3V reference (VREF3333) allows a full-scale current range of ±33A. A thermistor (TP61) monitors the PCB temperature close to the GaN power module.

A high-side DC-link current sense comparator allows hardware-based short-circuit protection, DC-link and phase voltages are also measured and allows validation of advanced sensorless designs like InstaSPIN-FOC™.

The design offers a TI BoosterPack compatible 3.3V I/O interface with to connect to a C2000™ MCU LaunchPad™ development kit or Sitara™ microcontrollers for quick and easy performance evaluation of our GaN technology.

2.3 Highlighted Products

2.3.1 LMG2100

The LMG2100 100V GaN half-bridge power stage provides an integrated power stage design using enhancement-mode Gallium Nitride (GaN) FETs. The device consists of two GaN FETs driven by one high-frequency GaN FET driver in a half-bridge configuration, as shown in Figure 2-2. Key features for this design are summarized in Table 2-1.

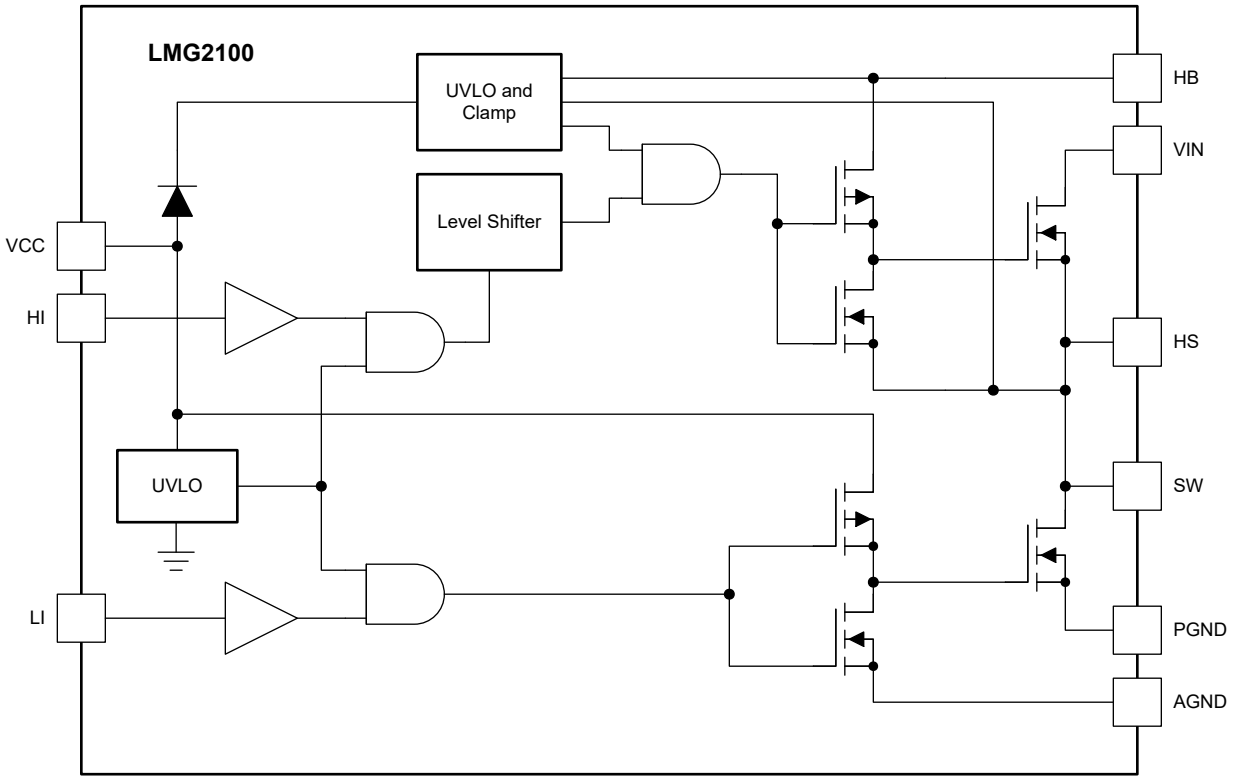


Figure 2-2. LMG2100 Functional Block Diagram

Table 2-1. LMG2100 Features and Benefits

FEATURE	BENEFIT
Integrated high-side and low-side GaN driver and 80V GaN FETs, 4.4mΩ devices for 35A DC operation.	Enables up to $60V_{DC}$, three-phase inverter with $16A_{RMS}$ phase current at 80kHz high-switching frequency for low inductance and high-speed drives.
Integrated 80V, 4.4mΩ, GaN FETs and GaN driver with completely bond-wire-free package.	Minimized package parasitic elements enable ultra-fast switching for reduced switching losses to reduce or eliminate heat sink.
GaN FETs have zero reverse recovery (3^{rd} quadrant operation) and very small input capacitance C_{ISS}.	Reduces or eliminates ringing in hard switching, like in inverters reduce EMI. Very low overshoot and undershoot allows higher nominal DC-link voltage than Si-FET for same maximum rated voltage.
Excellent propagation delay matching (2ns FETs).	Enables ultra-low dead band per half-bridge for major reduction of switching losses in three-phase inverter applications and elimination of dead-time distortions in the phase voltage.
Independent high-side and low-side transistor-transistor logic (TTL) inputs.	Direct PWM interface to 3.3V MCU.
Single 5V gate driver supply with bootstrap voltage clamping and undervoltage lockout.	Ease power management. UVLO provides simultaneous shutdown of high-side and low-side GaN FET in case of gate driver undervoltage
LMG2100 optimized pinout.	Easy PCB layout with minimum inductance for reduced switching losses.
Two exposed GaN dies on top (SW and PGND). Big PGND pad on bottom.	Realize lower top thermal resistance. Accepts both sides cooling.

2.3.2 INA241A

The INA241A is an ultra-precise, bidirectional current sense amplifier than can measure voltage drops across shunt resistors over a wide common-mode range from –5V to 110V, independent of the supply voltage.

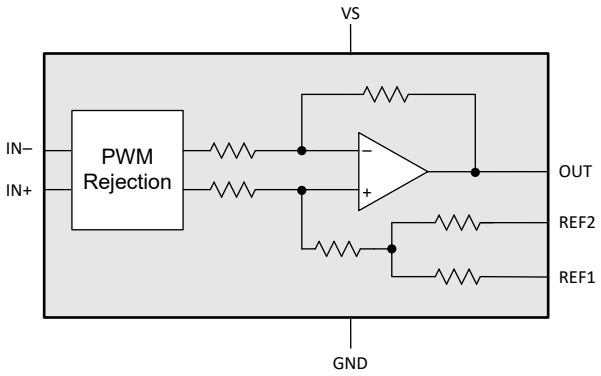


Figure 2-3. INA241A Functional Block Diagram

Table 2-2. INA241A Features and Benefits

FEATURE	BENEFIT
Fast-transient common-mode voltage input filtering (Enhanced PWM Rejection) and high AC common-mode rejection ratio (CMRR): 104dB at 100kHz and 166dB DC CMRR	Enables non-isolated shunt-based precision phase current measurement with three-phase inverters at high switching frequency of 40kHz and above.
Wide common-mode input voltage range: –5V to 110V	Provides sufficient headroom for transient overvoltage and undervoltage in three-phase inverters with 48V to 80V DC link voltage.
Low offset voltage (V_{OS} = ±10µV) and low gain error (0.01%)	Low offset and gain error enables accurate current sensing without calibration.
Low offset voltage drift (0.25µV / °C) and gain error drift (1ppm / °C)	Ultra-low offset and gain error drift allows high accurate current sensing over entire temperature range without temperature-dependent calibration.
1.1MHz signal bandwidth	High signal bandwidth supports low latency phase current measurement of high-speed motors as well as low latency detection of high-current transients such as during a short-circuit event.
Integrated output mid-point voltage reference voltage divider	Allows using an external ADC reference to set the INA241 mid-point voltage to half of the ADC reference voltage. This eliminates any offset generated by the ADC reference voltage drift.

2.3.3 LMR38010

The LMR38010 synchronous buck converter is designed to regulate over a wide input voltage range, minimizing the need for external surge suppression components.

Table 2-3. LMR38010 Features and Benefits

FEATURE	BENEFIT
4.2V to 80V input	Wide input voltage range, fit 12V, 24V, 48V or 60V DC fed drives
Cycle-by-cycle current limit, hiccup mode short-circuit protection, and thermal shutdown	Built-in protections
Spread Spectrum Option Available	Eases EMI mitigation
–40°C to 150°C T_J maximum	Wide temperature operation
HSOIC-8 ease of use package	Compliant to pin spacing request

3 System Design Theory

3.1 Three-Phase GaN Inverter Power Stage

The nominal 48V DC input voltage is buffered with six 10F ceramic capacitors to get a total of 60µF DC-bus capacitance. A 1mΩ, 3W shunt resistor is added in series to provide an option to monitor the DC-bus current for overcurrent protection using a high-common mode input voltage comparator INA310A. The PCB employs two separated ground planes: the power ground (PGND) and the logic or analog ground (GND). Both ground planes are connected in a star configuration through a net tie and two optional 0Ω resistors to minimize the crosstalk of high switching frequency currents in the power ground plane into the logic plane.

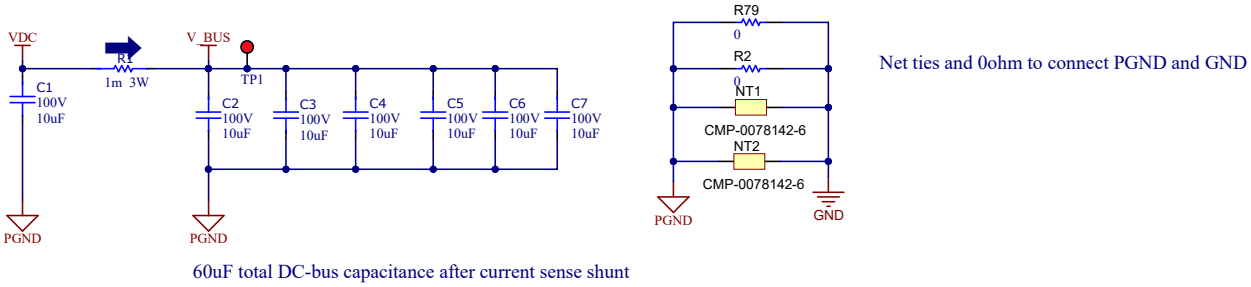


Figure 3-1. DC-Bus Decoupling and GND Scheme

3.1.1 LMG2100 GaN Half-Bridge Power Stage

The LMG2100 100V GaN half-bridge power stage provides an integrated and easy-to-use power stage design using enhancement-mode Gallium Nitride (GaN) FETs. The device consists of two GaN FETs driven by one high-frequency GaN FET driver in a half-bridge configuration. The PCB space is further reduced due to high integration and the fact that only a few additional passive components are required. Figure 3-2 shows the schematic of one half-bridge.

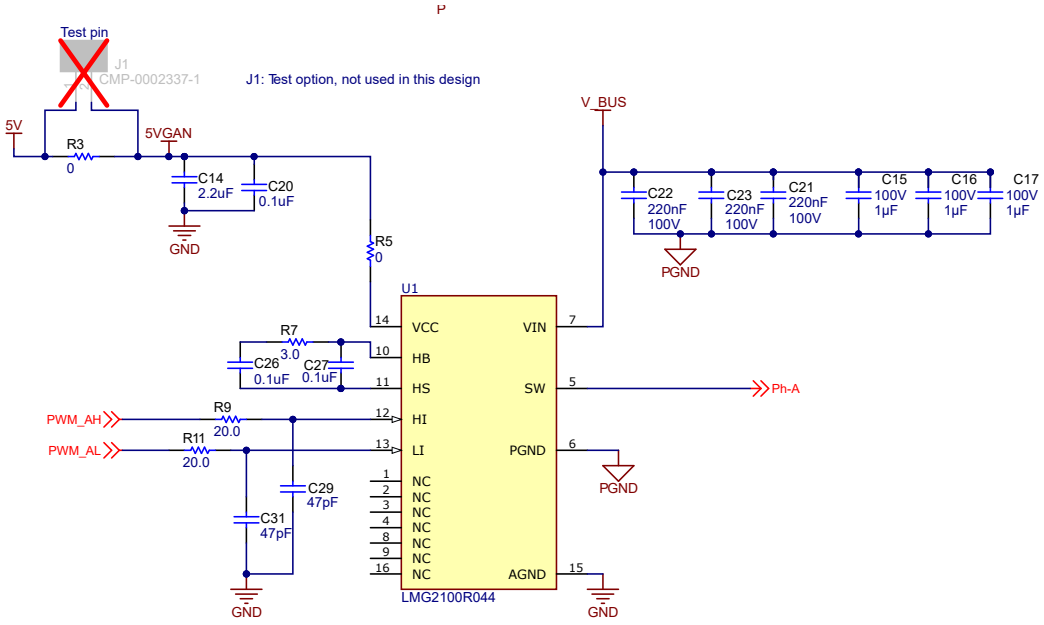


Figure 3-2. Half-Bridge Power Stage Schematic for Phase A

The 48V DC-link voltage is connected to the LMG2100 VIN pin and referenced to the power ground (PGND) pin. Local ceramic bypass capacitors C21, C22, C23 (100nF) and C15, C16, C17 (1µF) are placed in parallel close between the VIN and PGND pins to minimize loop inductance.

The LMG2100 integrated gate driver is supplied with 5V. A 2.2µF and 0.1µF ceramic bypass capacitor (C14, C20) are placed close to the VCC pin and AGND pin, as suggested in the data sheet.

Sequencing is not required for the 5V at VCC and the 48V at VIN, neither during the power up or power down of the input DC voltage.

A 100nF ceramic bootstrap capacitors C26 and C27 is placed close to the HB (high-side gate-driver bootstrap rail) and HS (high-side GaN-FET source connection) pins. R5 and R7 are placed to configure the slew rate of the switch node rising edge and related turn-on time. R5 in VCC path can limit the turn-on slew rate of low side GaN-FET and R7 in bootstrap path is for high side GaN-FET. 3Ω was used for the tests in this design for R5 and R7.

The complementary PWM signals for the high-side and low-side switch from the PWM buffer are low-pass filtered with R9, C29 and R11,C31 to reject high-frequency impulse noise and avoid false switching with a cutoff frequency of around 160MHz and a propagation of around 1ns. The SW (switch node) pin is connected to the motor phase-A terminal through a series inline shunt for phase current sensing, and respectively for the other LMG2100R044 half-bridges to the phase B and the phase C terminal.

3.2 Inline Shunt Precision-Phase Current Sensing With INA241A

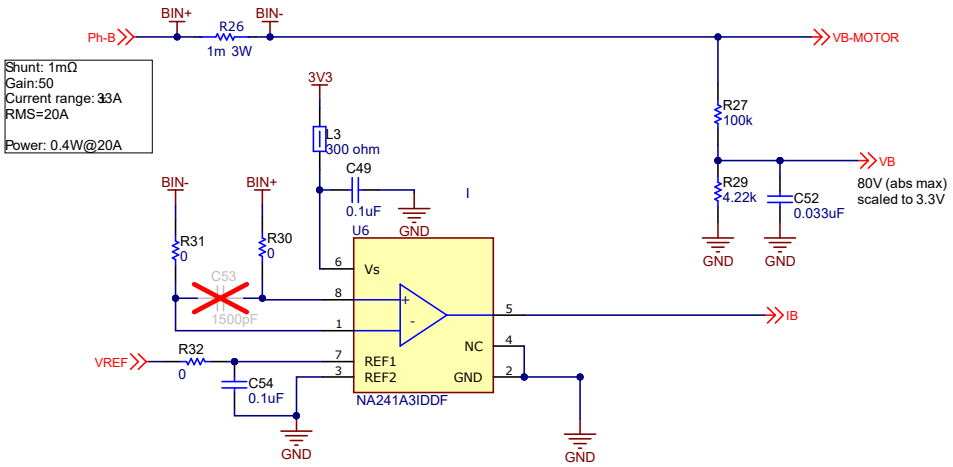


Figure 3-3. Inline Phase-Current Sense Schematic for Phase B

The phase current in phase A and phase B are measured inline through a 1mΩ shunt, for example R26 for phase B, as Figure 3-3 shows. R26 is directly connected to the switch node output (SW pin) of the LMG2100 device. The shunt is connected through a Kelvin connection and optional, differential RC low-pass filter (R30, R31, and C53) to the differential inputs IN+ and IN– of the INA241A3 device. In this design, the low-pass filter is not required and the two series resistors were selected as 0Ω and the capacitor C53 was not populated on all three phases. The INA241A3 device has a fixed gain of 50V / V. To convert the bipolar input voltage across the shunt into a unipolar output voltage that is suitable for an ADC with a 3.3V input voltage range, the mid-voltage of the INA241A3 (U6) is set to 1.65V. To achieve this conversion, a precision, low-drift 3.3V reference REF3333 is connected through an optional RC low-pass filter (R32 and C54) to the REF1 pin. The REF2 pin is connected to GND. In the default setting of this design, the low-pass filter is not used and R32 is set to 0Ω, which is the same on phase A. An internal, precision divide-by-2 function in the INA241 device creates a precision, ultra-low drift, 1.65V bias voltage at the INA241 OUT pin. The transfer function can be calculated as per Equation 1.

$$I_A[V] = (I_A[A] \times 1\,m\,\Omega) \times 50\left[\frac{V}{V}\right] + 1.65V \quad (1)$$

The maximum phase current range is from ±33A. The corresponding output voltage ranges from 0V to 3.3V with 1.65V representing a 0A phase current.

3.3 Phase Voltage and DC Input Voltage Sensing

Figure 3-4. Phase A Voltage Sense Circuit

The phase voltage for each phase and the DC link voltage, which is equal to the input voltage, are sensed through a resistor divider. Figure 3-4 shows an example of this for the DC-Link voltage (R19, R21) with a low-pass filter (C44) to attenuate the PWM carrier frequency. The phase voltage is scaled to 3.3V, assuming an absolute maximum voltage of 80V according to Equation 2.

$$\mathrm{VA[V]} = \mathrm{VA\_MOTOR} \times \frac{\mathrm{R21}}{\mathrm{R21} + \mathrm{R19}} = \mathrm{VA\_MOTOR} \times \frac{1}{24.7} \tag{2}$$

The cutoff frequency (f – 3dB) of the low-pass filter was set to 1kHz, which provides around 32dB of attenuation to reject a 40kHz PWM carrier frequency and 40dB for a 100kHz PWM carrier frequency. The DC-link voltage is sensed through the same resistor divider (see Figure 3-4) and low-pass filtered to make sure all voltages have the same transient response and delay.

3.4 Power-Stage PCB Temperature Monitor

To sense the temperature of the PCB power stage, the TMP61 family of thermistors is selected because these devices offer ±1% from 0°C to +70°C with 0402 and 0603 package options. The TMP6131 device is placed close to the LMG2100 half-bridge module. Based on the design tool, select a 10kΩ resistor as the pullup resistor. The analog output signal of the TMP6131 is low-pass filtered with R57 (20Ω) and C68 (2.2nF) and routed to connector J1-18 to connect to the C2000 MCU integrated ADC. The signal can be used for real-time PCB temperature sensing and overtemperature protection through the C2000 MCU.

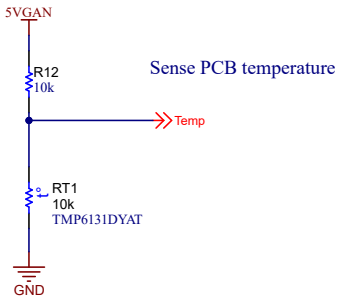


Figure 3-5. PCB Temperature Sense Through Thermistor

3.5 Power Management

Figure 3-6 shows the power supply tree. A wide input voltage DC/DC buck converter to generate the 5V rail. A power module then generates 3.3V from 5V, which supplies 3.3V signal chain such as INA241A and so forth. Optionally the 3.3V supply rail can also power the MCU LaunchPad.

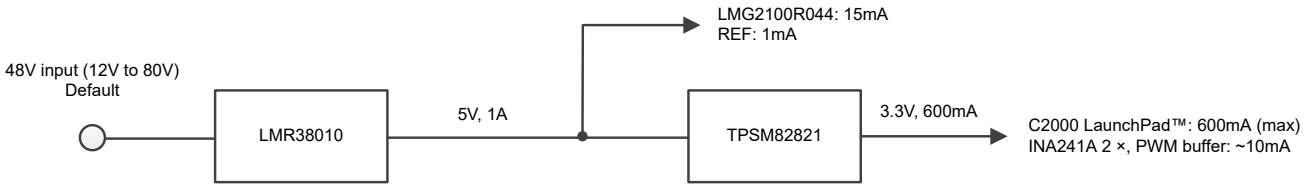


Figure 3-6. Power Supply Tree

3.5.1 48V to 5V DC/DC Converter

The DC/DC buck converter was designed for an input voltage range from 12V to 60V with at least 80V input voltage capability. The output voltage was set to 5V. The DC/DC buck converter feedback circuit was designed for minimum output voltage ripple and at least 1A output current.

The power supply was entirely designed using WEBENCH® circuit design and selection simulation services, using the following parameter specifications:

Table 3-1. Parameter Specifications

PARAMETER	TYPICAL VALUE	MIN, MAX VALUE
DC-link voltage	48V	10V, 80V
Output voltage	5V	±5%
Output voltage ripple	< 50mV$_{PP}$	As low as possible
Output current	500mA	1A
Temperature range	–40°C to 85°C (125°C)	

With these parameters the LMR38010 was the device chosen to fit the design specification. Figure 3-7 shows the WEBENCH recommendation.

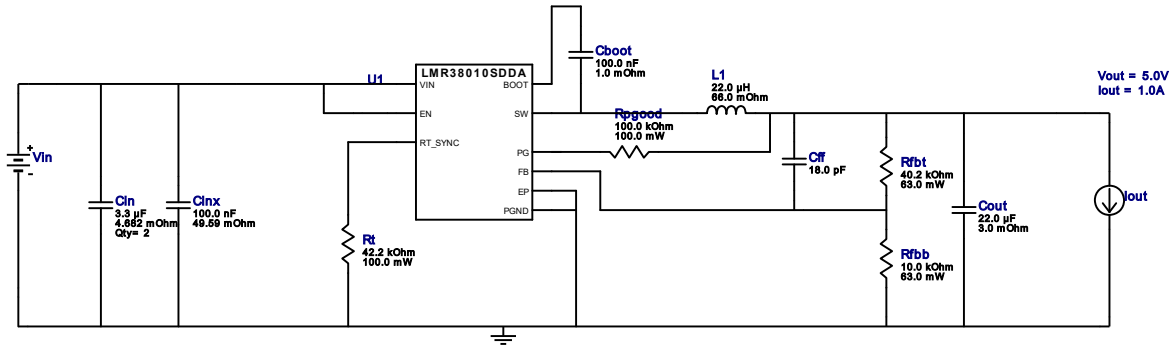


Figure 3-7. LMR38010 WEBENCH Simulation Circuit

To reduce the size as much as possible, the switching frequency is set to 617kHz (R_t = 42.2kHz), which only requires a 22µH inductor. The voltage ripple is shown in Figure 3-8, for 43.5V input. The output ripple is less than 15mV when the current is >0.1A.

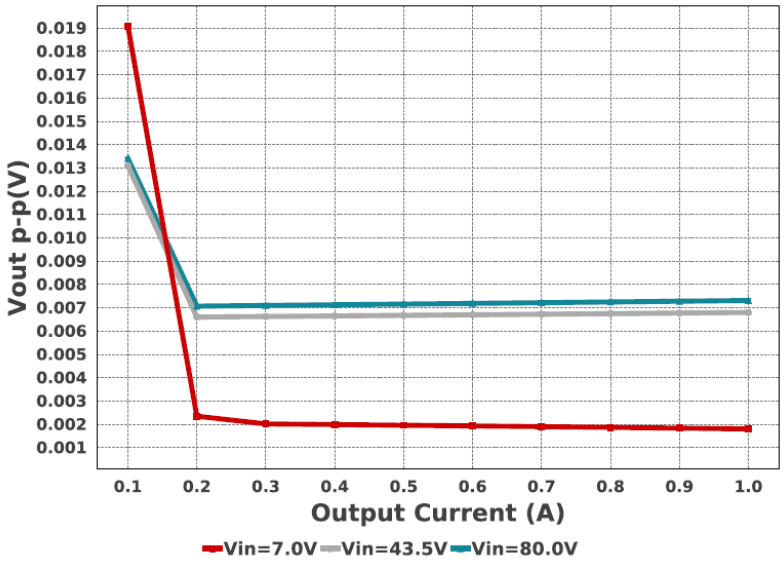


Figure 3-8. 5V Output Voltage Ripple

Based on this simulation, some small changes were made to finish the final schematic of this design. Add an optional resistor R68 parallel to R71 to keep the flexibility for the 5.5V output for LDO to generate a lower ripple 5V. The 5.5V can also be input externally through J7.

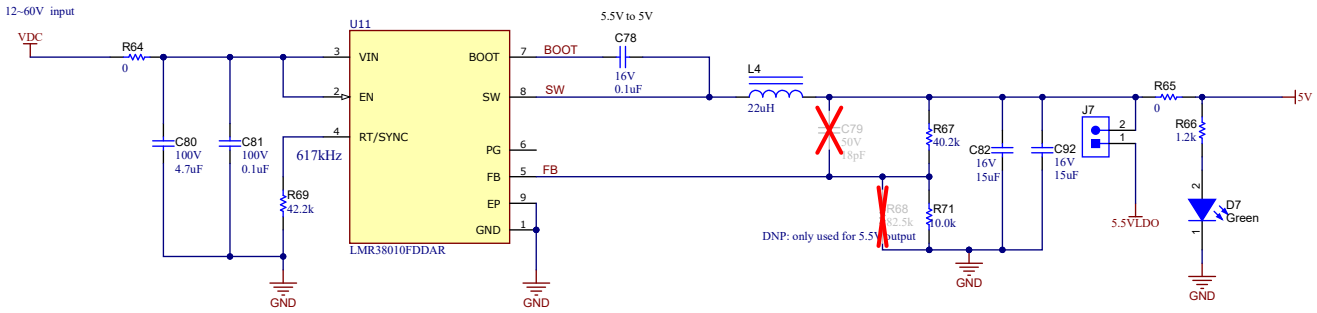


Figure 3-9. 48V to 5V DC/DC Buck Converter

3.5.2 5V to 3.3V Rail

For the 3.3V rail, a power module TPSM82821 with 2mm × 2.5mm super small package meets the 600mA output current requirement. The power modules integrate a synchronous step-down converter and an inductor to simplify design, reduce external components, and save PCB area.

The jumper J8 also keeps the flexibility for an external 3.3V power supply in the board. When R48 is populated, the resistor provides the 3.3V rail from the GaN board to the C2000 MCU LaunchPad development kit.

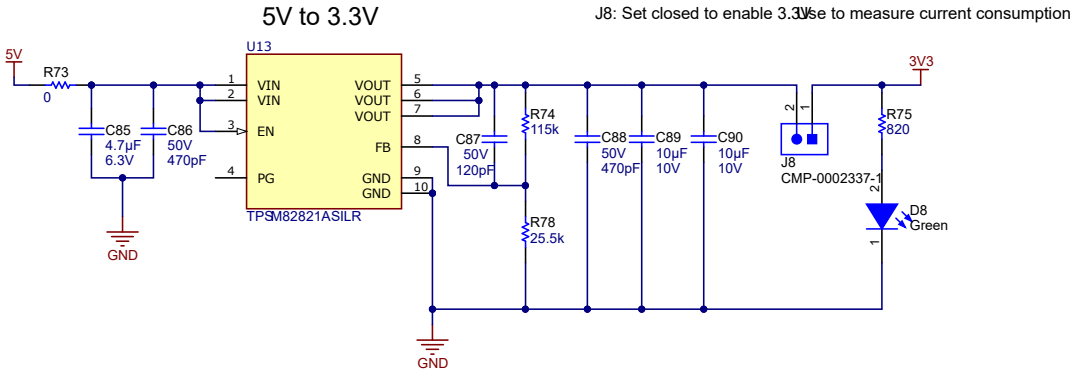


Figure 3-10. 5V–3.3V Power Module

3.6 Interface to Host MCU

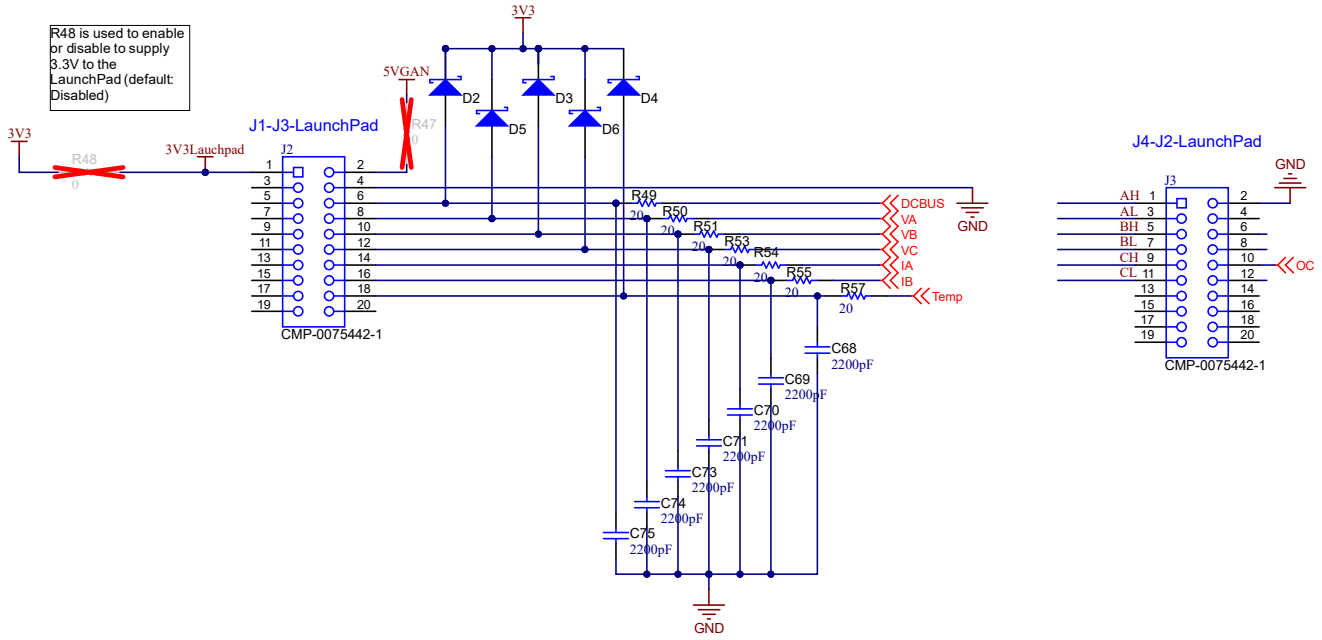


Figure 3-11. Schematic of Host Interface Connectors J1 and J2

The interface-to-host processor, such as the C2000 MCU, is compliant to a 3.3V I/O and provides all the required signals like the complementary PWM signals for phase A, B, and C; a PWM trip and disable signal; as well as accurate phase current, phase voltage, and DC-link voltage feedback to control the three-phase GaN inverter. The analog PCB temperature feedback (temp) further helps to protect the three-phase GaN power stage and adjust the safe operating area (SOA).

Each analog feedback signal is low-pass filtered with an RC filter, for example R57 (20Ω) and C58 (2.2nF) before connecting to the MCU integrated ADC. The 2.2nF capacitor is placed to drive the switched input capacitors of the ADC, which are typically in the range of 5pF to 15pF. The Schottky diodes D2 through D6 clamp the maximum phase voltages to around 3.6V in case the DC bus voltage exceeds the 80V (absolute maximum) value.

The TIDA-010936 fits only upper headers of an 80-pin C2000 MCU LaunchPad, like the LAUNCHXL-F28P65X. Additionally, the TIDA-010936 host interface offers the option to provide the 3.3V rail to power the C2000 LaunchPad. This option provides proper power-up sequencing of the entire system. The details of the pin assignment are outlined in Section 1.1 in Table 1-2 and Table 1-3, respectively.

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware Requirements

4.1.1 TIDA-010936 PCB Overview

Figure 4-1 and Figure 4-2 show labeled photos of the top and bottom of the PCB.

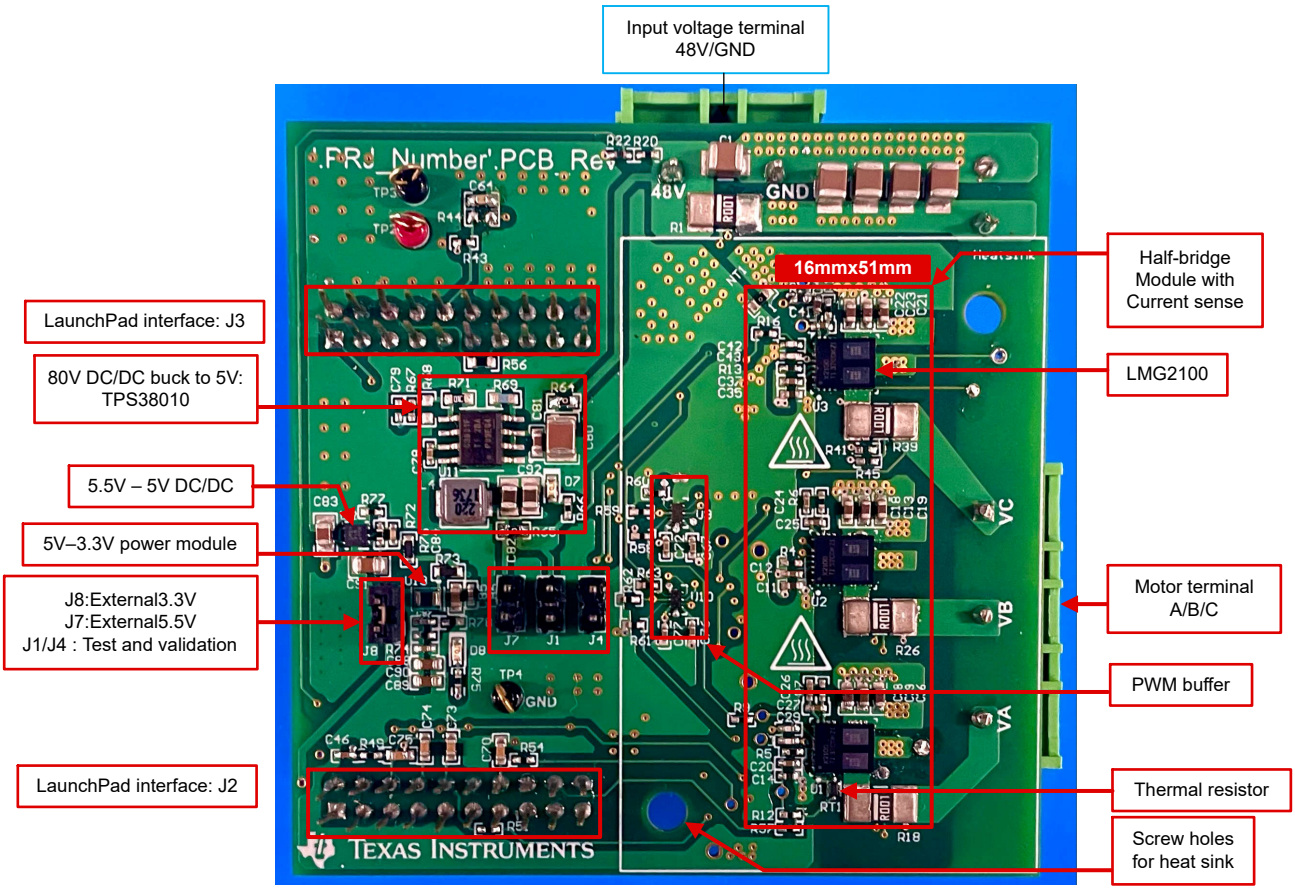


Figure 4-1. TIDA-010936 PCB Top View

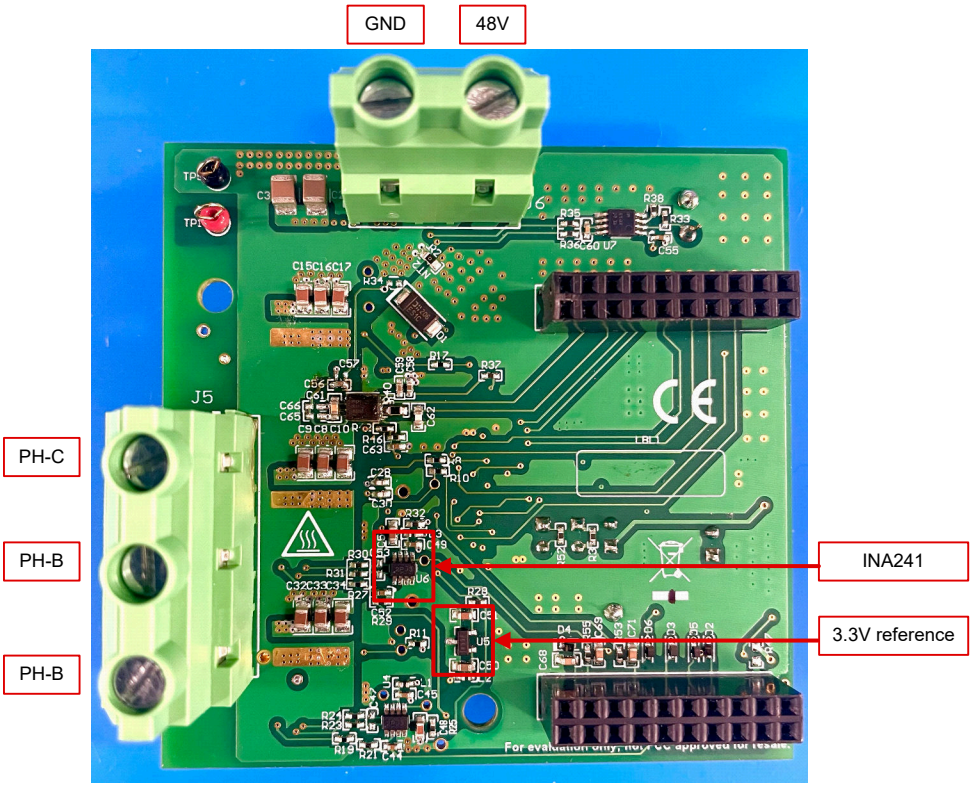


Figure 4-2. TIDA-010936 PCB Bottom View

4.1.2 TIDA-010936 Jumper Settings

The TIDA-010936 employs the four jumpers detailed in Table 4-1.

Table 4-1. TIDA-010936 Jumper Settings

JUMPER	FUNCTION	POPULATED	NOT POPULATED
J1, J4	Test and validation	N/A	Default
J7	5V supply	5.5V to LDO for 5V(1)	Onboard power (default), (2)
J8	3.3V supply	Onboard (default)	External 3.3V
R48, R47	3.3V or 5V for LaunchPad	Supply Launchpad	Not populated (default)LaunchPad uses own USB power

(1) If J7 is populated, 5.5V is supplied to LDO (U12), R68 needs to be populated and R65 needs to be removed.
(2) When J7 (default) is not populated, the board has 5V. If using an external 5.5V to LDO (U12), remove R65 and populated the components related to U12.

CAUTION

Do not populate R48 and R47 at the same time. When R48 or R47 are populated, make sure the C2000 LaunchPad is not powered through USB. To accomplish this setup, remove the jumpers JP1 and J16 on the F28P65X LaunchPad.

4.1.3 Interface to C2000™ MCU LaunchPad™ Development Kit

The TIDA-010936 interface specification is compliant to the TI BoosterPack plug-in module standard. The pin assignments are found in Table 1-2 and Table 1-3 in Section 1.1. The TIDA-010936 board can only be connected to the C2000 LaunchPad headers J1–J4.

Figure 4-3 shows the TIDA-010936 connected to the F28P65X LaunchPad headers J1–J4. The TIDA-010936 does not power the LaunchPad; therefore, TIDA-010936 J8 is populated and the jumpers JP1 and JP2 on the LaunchPad are populated.

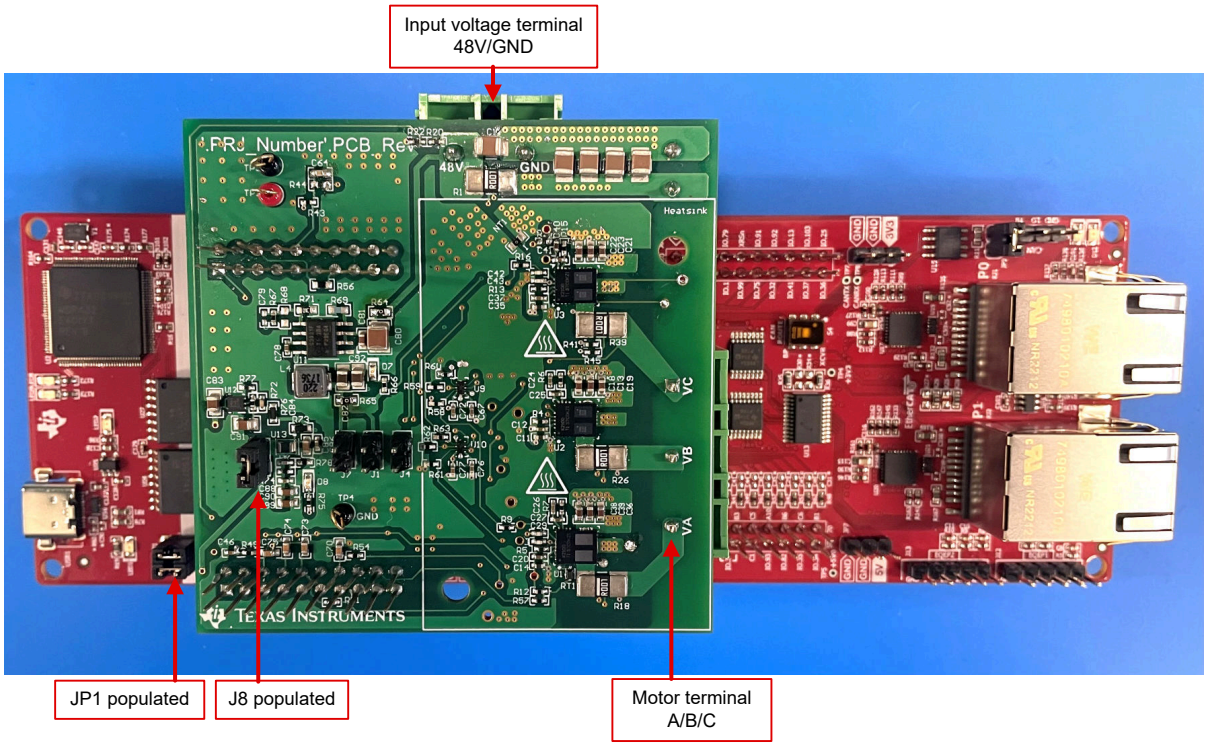


Figure 4-3. TIDA-010936 Connected to C2000™ MCU LaunchPad™ Development Kit

Connect the DC power supply (12V to 60V, 48V nominal) to the DC input voltage connector (J6) and the three-phase motor to the three-phase output voltage connector (J5). Validate the three-phase motor can handle the high slew rates of the phase voltages during PWM switching.

4.2 Software Requirements

To validate the TIDA-010936, a TI internal test software was developed for the TMS320F28P65X and the corresponding LaunchPad development kit was used. This software is not available for public use. For C2000 software support, see the MotorControl software development kit (SDK) for C2000™ and the TI E2E™ design support forum for C2000™ microcontrollers.

4.3 Test Setup

Table 4-2 lists the key test equipment. Description and pictures of the test setup for specific tests are provided in the section of the corresponding test results.

Table 4-2. Key Test Equipment

DESCRIPTION	PART NUMBER
High-speed oscilloscope	Tektronix MSO4104B
Single-ended probes	Tektronix P6139B
Power analyzer	HIOKI PW6001
Isolated current probe	CYBERTEK CP8030H, HIOKI CT6872
Dynamometer	MAGTROL DSP6000
Multimeter	Fluke 17B+
Thermal camera	TESTO 865
Adjustable power supply (10A)	ITECH IT6724H
Adjustable power supply (20A)	ITECH M3902C
C2000 MCU LaunchPad Development Kit	Texas Instruments LAUNCHXL-F28P65X
Low voltage servo motor (48V, 7A)	Teknic M-2310P-LN-04K
Low voltage servo motor (72V, 21A)	7H2207124422

4.4 Test Results

4.4.1 Power Management and System Power Up and Power Down

The focus of this test was to validate the onboard 5V and 3.3V power supplies and measure the typical current consumption of the 3.3V and 5V rail. For these tests, the C2000 MCU LaunchPad development kit was not powered from the TIDA-010936. Due to the high step-down ratio 48:5 (48V input to 5V output), the voltage ripple at the 5V rail was validated too.

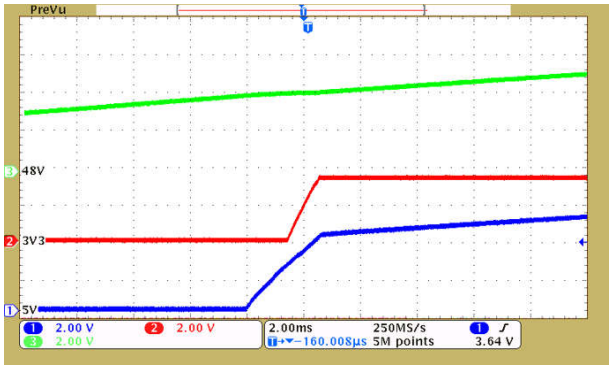


Figure 4-4. TIDA-010936 System Power Up ($48V_{IN}$, 5V Rail, and 3.3V Rail)

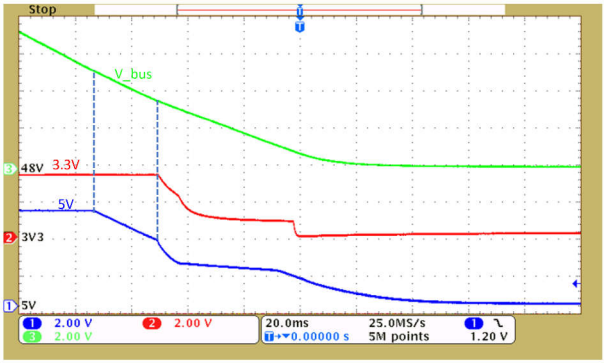


Figure 4-5. TIDA-010936 System Power Down ($48V_{IN}$, 5V Rail, and 3.3V Rail)

For the power-down stage, when the bus voltage drops to about 5V, the output of the LMR38010 drops along with the bus voltage. When the bus is lower than 3.3V, the 3.3V rail also starts to drop.

The AC ripple of the 5V rail remains well below $20mV_{PP}$ in light load. The frequency of ripple is 617kHz, which matches the buck converter switching frequency. The offset of the 5V rail is about 5.07V.

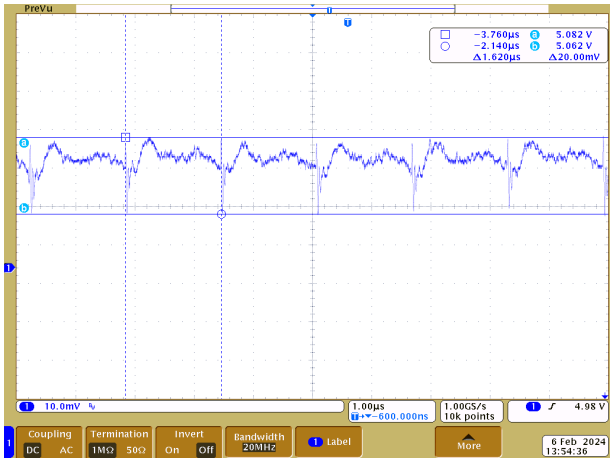


Figure 4-6. 5V Output Ripple at Nominal Load (20mA)

4.5 GaN Inverter Half-Bridge Module Switch Node Voltage

The focus on this test was to validate the transient response of the switch node voltage of the GaN inverter at 48V with low and maximum phase current. The other aim of the test was to validate the capacity or amount of local bypass capacitors at each of the LMG2100 GaN power modules.

The C2000 MCU was configured to generate a three-phase space vector with complementary PWM with 40kHz switching frequency and 16.6ns dead band. The PWM duty cycle per phase was configured to drive the corresponding phase current I_A with $I_B = I_C = –0.5\ I_A$.

The LMG2100 switch node voltage was measured at the LMG2100 SW pin (pin 8), referenced to the PGND via close to the LMG2100 PGND pin (pin 9) as shown in Figure 4-7.

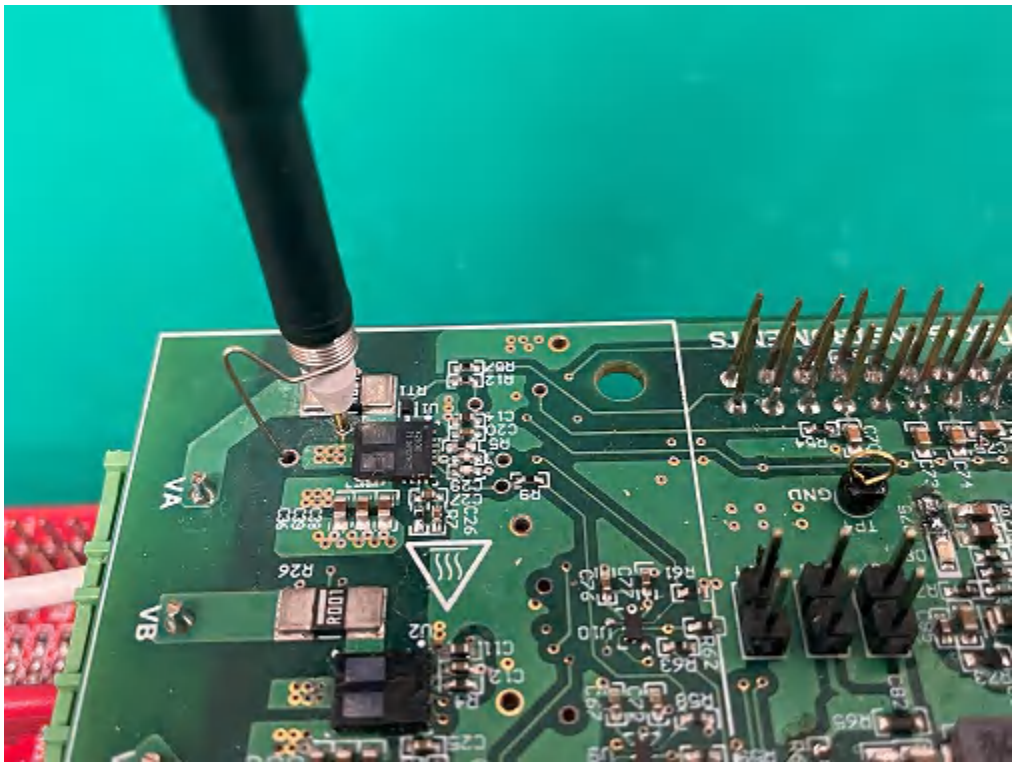


Figure 4-7. Test Setup for LMG2100 Switch-Node Measurement (Pin SW to PGND) With Single-Ended Probe

The pictures below show that the PWM input has a dead time of 16.6ns between the upper and lower bridge arms.

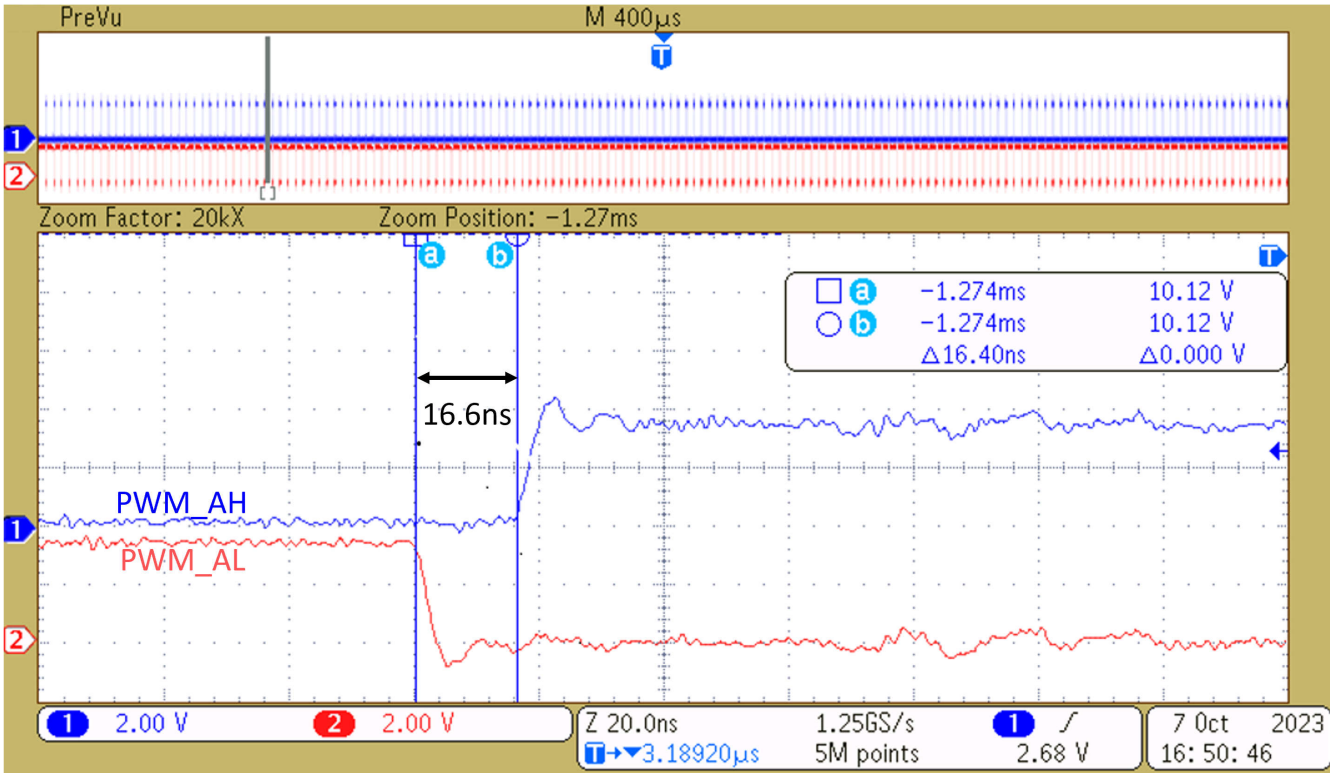


Figure 4-8. Rising Edge PWM A (H and L) at J2

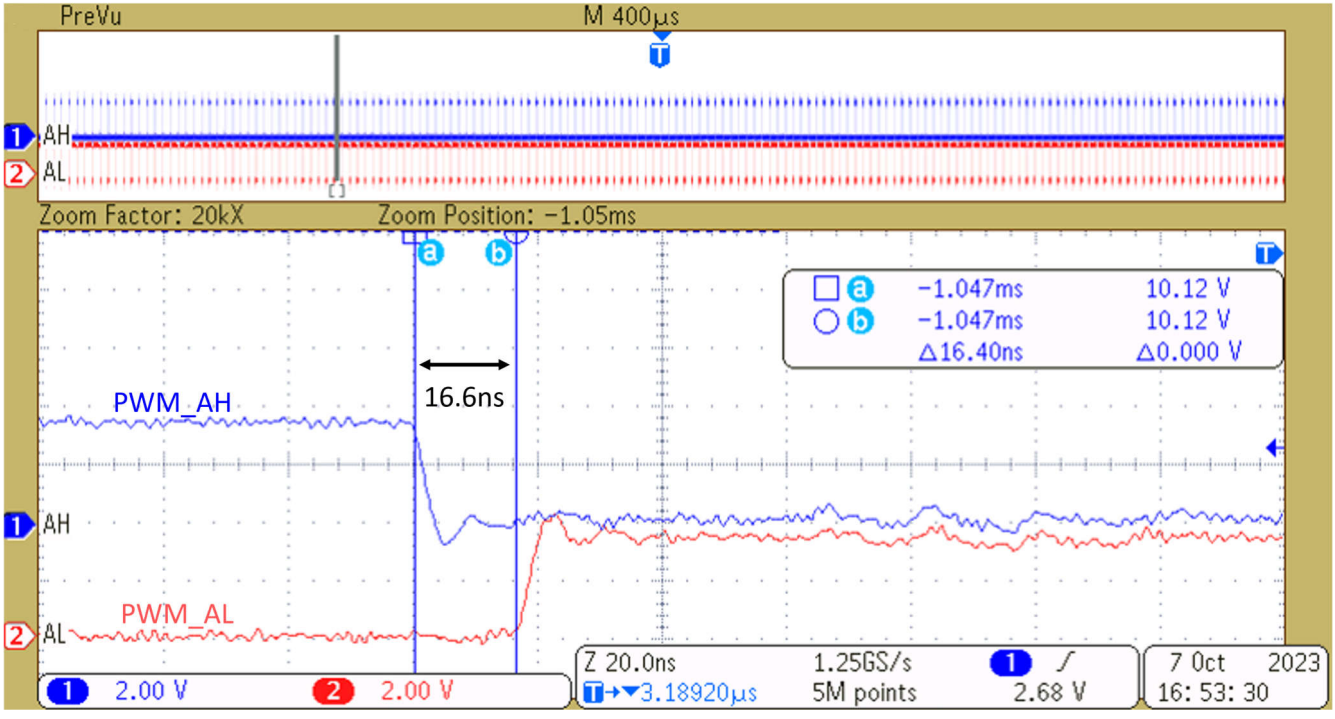


Figure 4-9. TIDA-010936-4-11-Falling Edge PWM A (H/L) at J2

4.5.1 Switch Node Voltage Transient Response at 48V DC Bus

The following figures outline the SW transient voltage at hard-switching and soft-switching. PWM frequency (40kHz), LMG2100 propagation delay, as well as the 16.6ns PWM dead band can be well identified. Due to the low phase current there is hard-switching and a combination of soft- and hard-switching as shown in below figures. The turn-on and turn-off slew rate (20% to 80%) of the GaN-FETs was configured to around 10V/ns to 15V/ns.

4.5.1.1 Output Current at ±1A

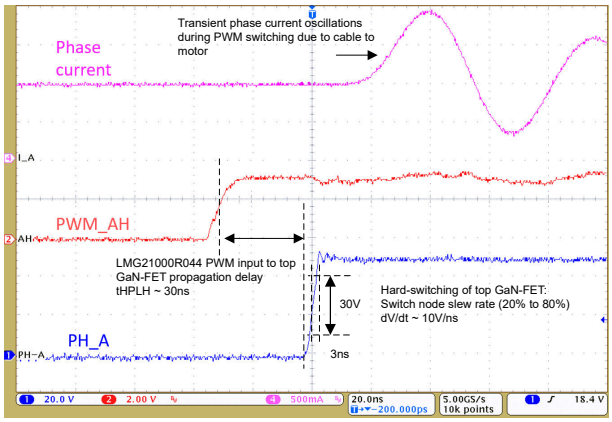


Figure 4-10. Phase A Rising SW, Phase Current and LMG2100 PWM (HI) at 48V, 1A

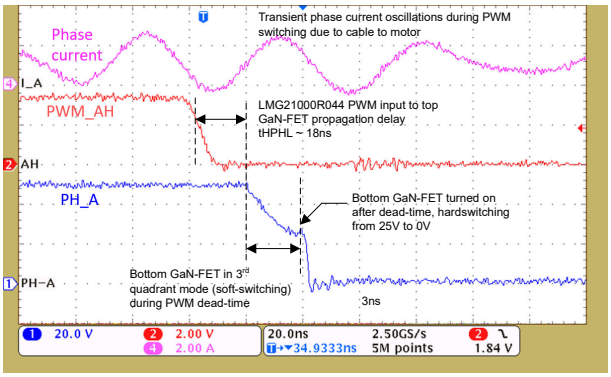


Figure 4-11. Phase A Falling SW, Phase Current and LMG2100 PWM (HI) at 48V, 1A

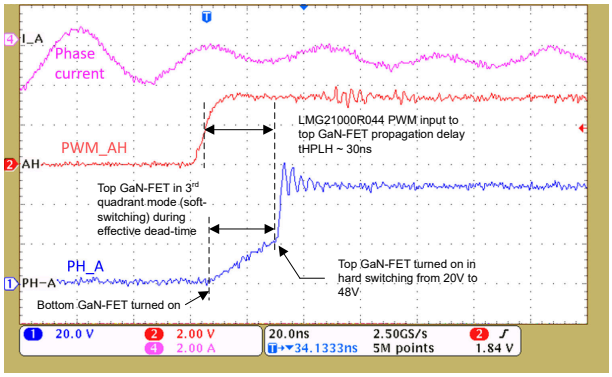


Figure 4-12. Phase A Rising SW, Phase Current and LMG2100 PWM (HI) at 48V, –1A

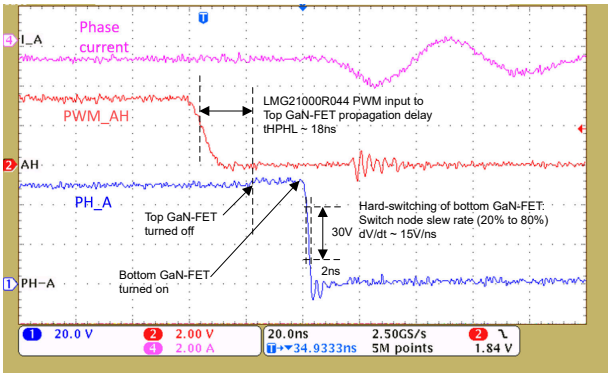


Figure 4-13. Phase A Falling SW, Phase Current and LMG2100 PWM (HI) at 48V, –1A

4.5.1.2 Output Current at ±10A

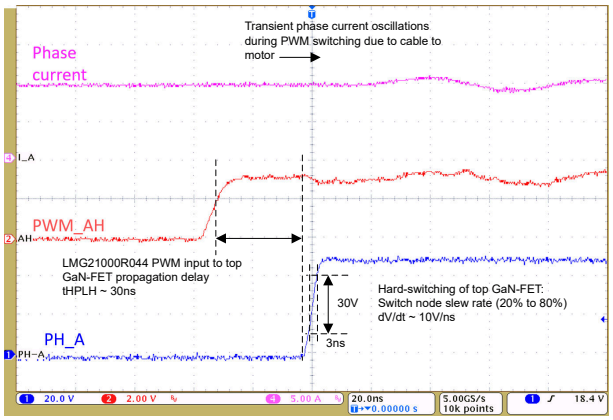


Figure 4-14. Phase A Rising SW, Phase Current and LMG2100 PWM (HI) at 48V, 10A

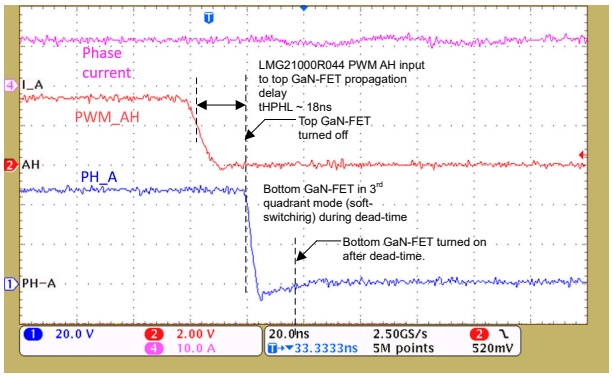


Figure 4-15. Phase A Falling SW, Phase Current and LMG2100 PWM (HI) at 48V, 10A

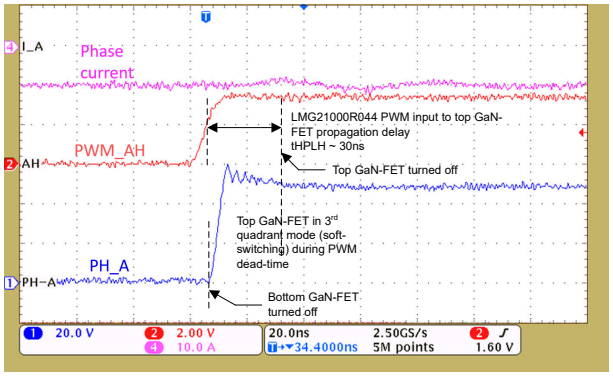


Figure 4-16. Phase A Rising SW, Phase Current and LMG2100 PWM (HI) at 48V, –10A

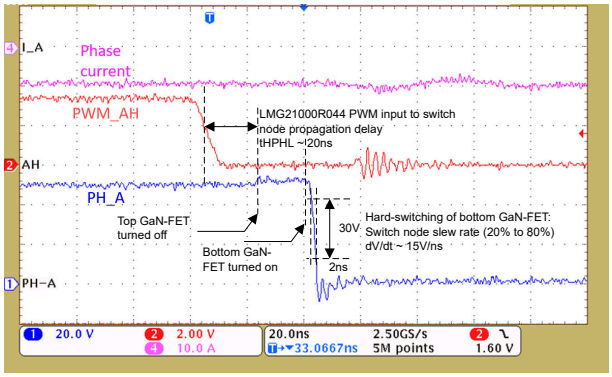


Figure 4-17. Phase A Falling SW, Phase Current and LMG2100 PWM (HI) at 48V, –10A

4.5.2 Impact of PWM Frequency to DC-Bus Voltage Ripple

A key function of the bus capacitor is to smooth the bus voltage and provide transient current at the switching moment to keep the ripple of the bus voltage small enough.

When the PWM switching frequency is increased, the requirements for bus capacitance are reduced. Because the switching time of the FET becomes shorter, the amount of charge required by the capacitor becomes smaller, so using a higher PWM switching frequency can reduce the required bus capacitance value.

Usually, electrolytic capacitors are used as bus capacitors. Electrolytic capacitors can provide sufficient capacitance, but also have disadvantages, such as huge size, short life, poor high-frequency characteristics, and so forth. In comparison, ceramic capacitors are more stable and smaller, but the capacitance ceramic capacitors can provide is limited. The following test attempts to replace electrolytic capacitors with ceramic capacitors by increasing the PWM frequency.

Determine whether smaller ceramic capacitors can be used by testing the bus ripple of electrolytic capacitors and ceramic capacitors at different frequencies. This test used 60µF and 100µF ceramic capacitors (PN: C3225X7R2A106K250AC × 6 or 10) and 100µF electrolytic capacitor (PN: ECA2AM101).

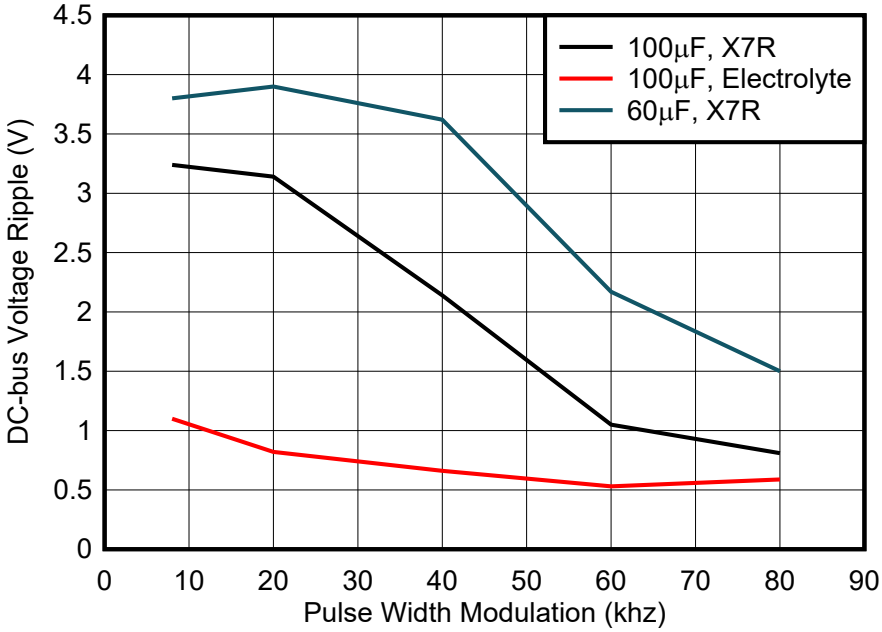


Figure 4-18. DC-Link Voltage AC Ripple at 48VDC, 8kHz–80kHz PWM, PH_I = 5A_{RMS}

As Figure 4-18 shows, as the frequency increases, the ripple on the bus gradually decreases, so capacitors with smaller capacitance can be used. But ceramic capacitors have significantly larger voltage ripple at low frequencies (< 80kHz). Because the actual capacitance of this 10µF ceramic capacitor is only 2.2µF at a voltage of 50V, the actual effective capacitances corresponding to the 60µF and 100µF ceramic capacitors in Figure 4-18 are 13.2µF and 22µF. Therefore, the ripple is larger than that of the 100µF electrolytic capacitor.

When the PWM frequency increases to 80kHz, the voltage ripple of a 100µF ceramic capacitor and an electrolytic capacitor is similar. Therefore, the ultra-low switching loss of GaN can be used to increase the PWM frequency to 80kHz. At the same time, the electrolytic capacitor can be replaced with a ceramic capacitor of the same capacity to achieve a smaller size.

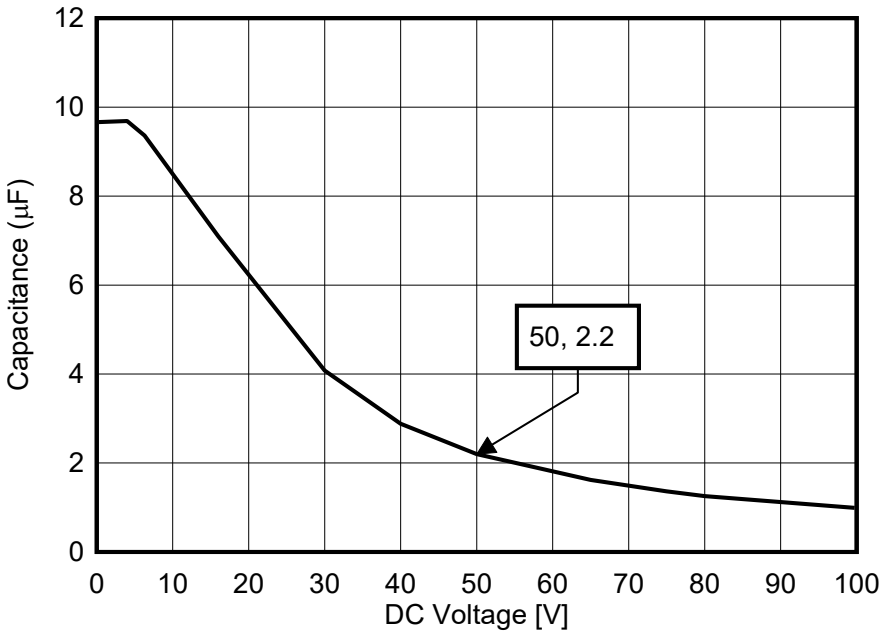


Figure 4-19. Ceramic Capacitor Capacitance vs Voltage Curve

4.5.3 Efficiency Measurements

The efficiency testing was done at 27°C lab temperature using a HIOKI PW6001 Power Analyzer and HIOKI CT6872 current transformer. The TIDA-010936 was powered with 48V DC and a high-power servo motor was used as load (72V, 21A). A dynamometer supplies high load in the motor. The PWM carrier frequency was set from 40Hz to 80kHz. The motor speed is 600RPM. Figure 4-20 shows a picture of the test setup and block diagram for wiring.

For all of these tests neither a heat sink nor a fan were used, hence only natural convection of the TIDA-010936 PCB applied.

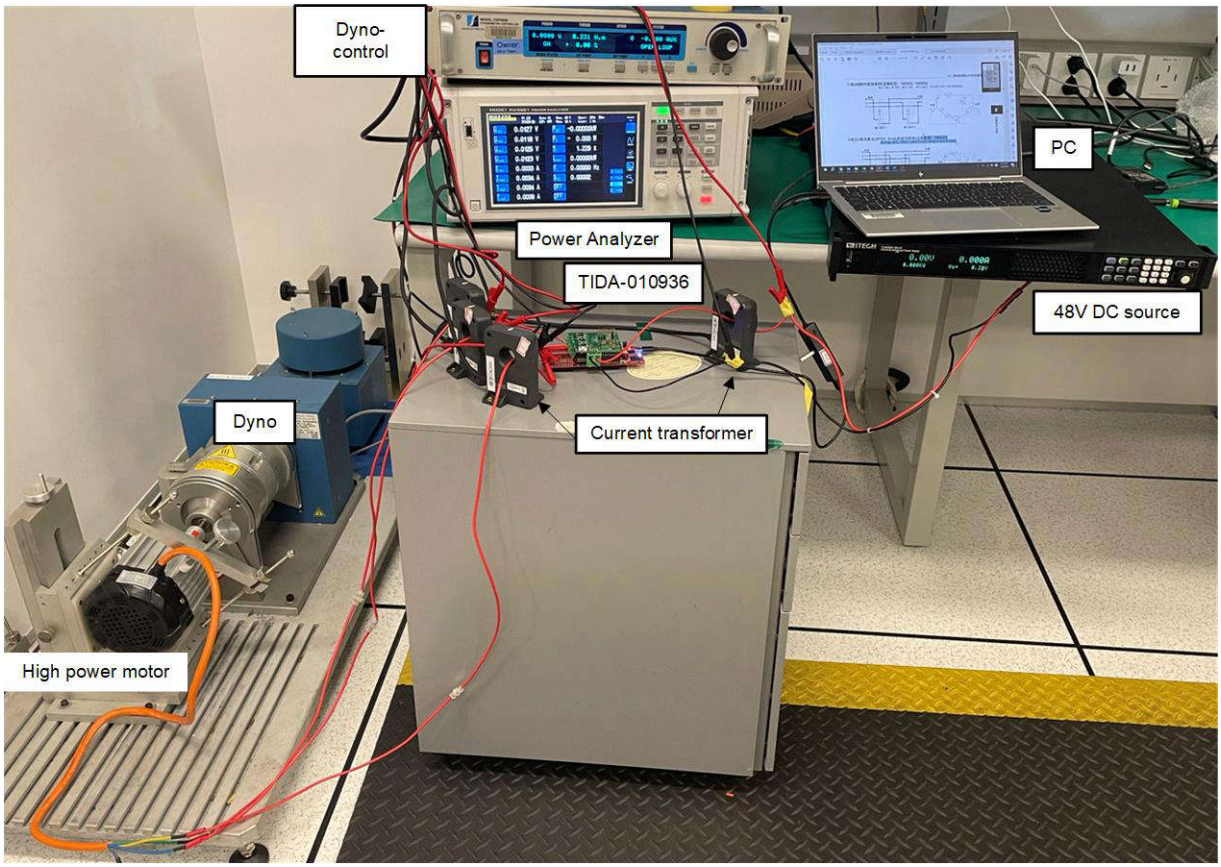


Figure 4-20. TIDA-010936 Test Setup for Inverter Efficiency Analysis

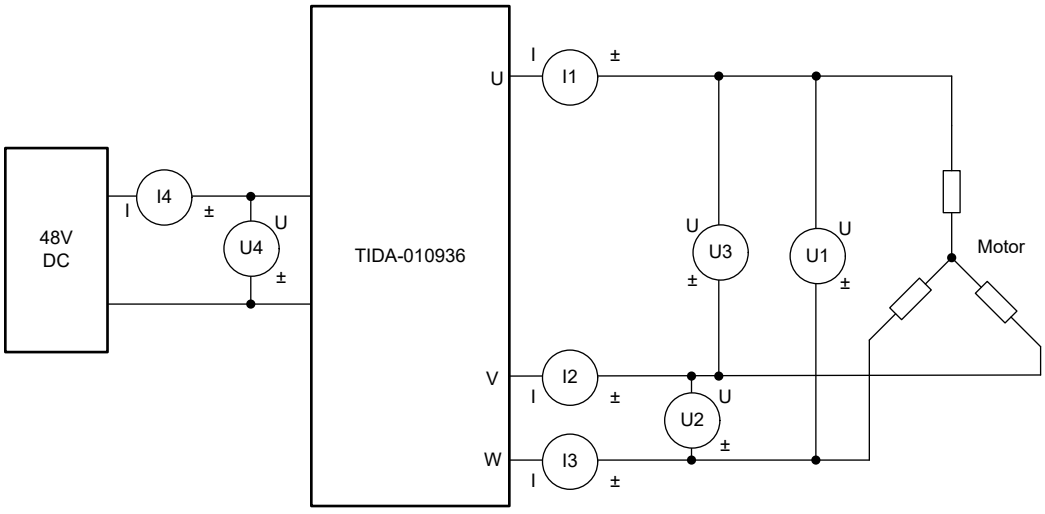


Figure 4-21. TIDA-010936 Wiring Block Diagram for Inverter Efficiency Analysis

Figure 4-22 shows the TIDA-010936 power losses versus the three-phase motor load current in A_{RMS}. These numbers do not include the power losses of the C2000 MCU LaunchPad development kit.

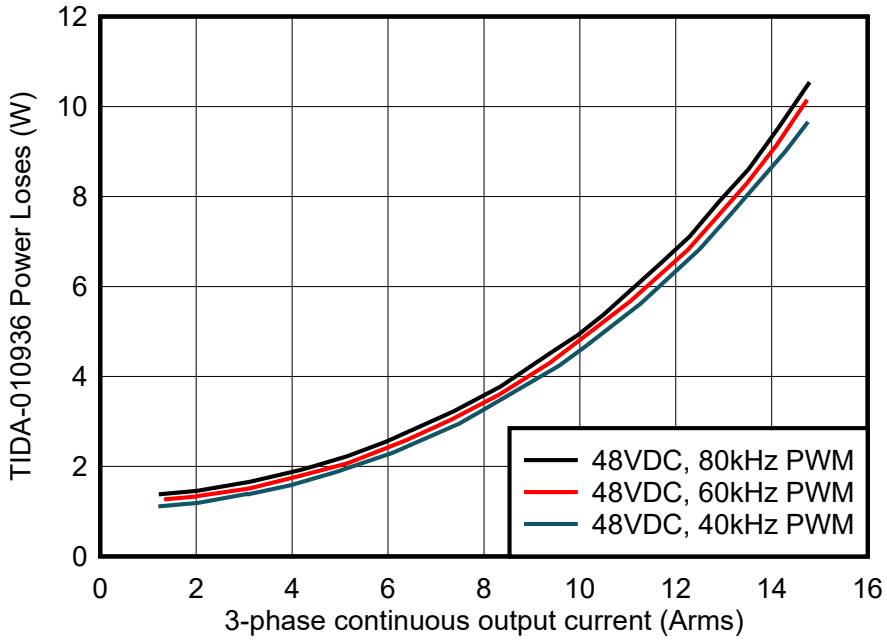


Figure 4-22. TIDA-010936 Board Losses at 48V Input Versus 3-Phase Output Current

The TIDA-010936 board power losses at maximum load current of 14.8A_{RMS} were 9.66W at 40kHz PWM and 10.5W 80kHz PWM. The TIDA-010936 power losses are dominated by the losses in the GaN FETs (LMG2100) and the losses in the 1mΩ shunt resistors.

The theoretical maximum peak efficiency at 48VDC with a maximum phase-to-phase voltage of 19.5V_{RMS} (Space Vector PWM with 3rd harmonics) and a power factor of 0.9 is 99.3% at 40kHz PWM and 99.2% at 80kHz PWM, as shown in Figure 4-23.

Observe that while the PWM switching frequency increases, the power losses of the board do not increase significantly. This also reflects the very low switching losses of the LMG2100R044 GaN-FETs to help to achieve very high efficiency even at higher PWM switching frequencies.

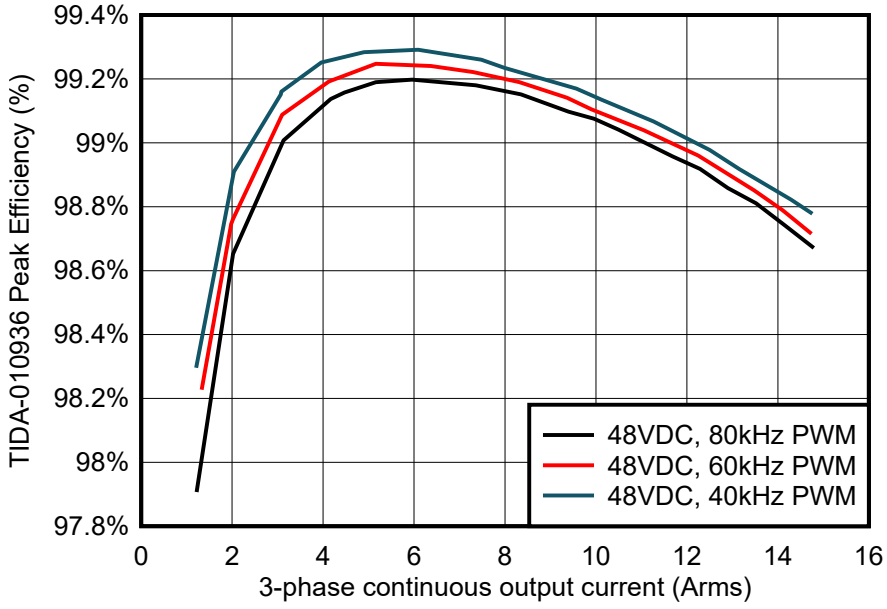


Figure 4-23. Calculated Maximum Peak Efficiency at 48VDC and 40, 60, and 80kHz PWM

4.5.4 Thermal Analysis

The thermal analysis of the design was done at 27°C lab temperature with 48V DC input with 40kHz with the high-power motor driven. For this test neither a heat sink or a fan were used.

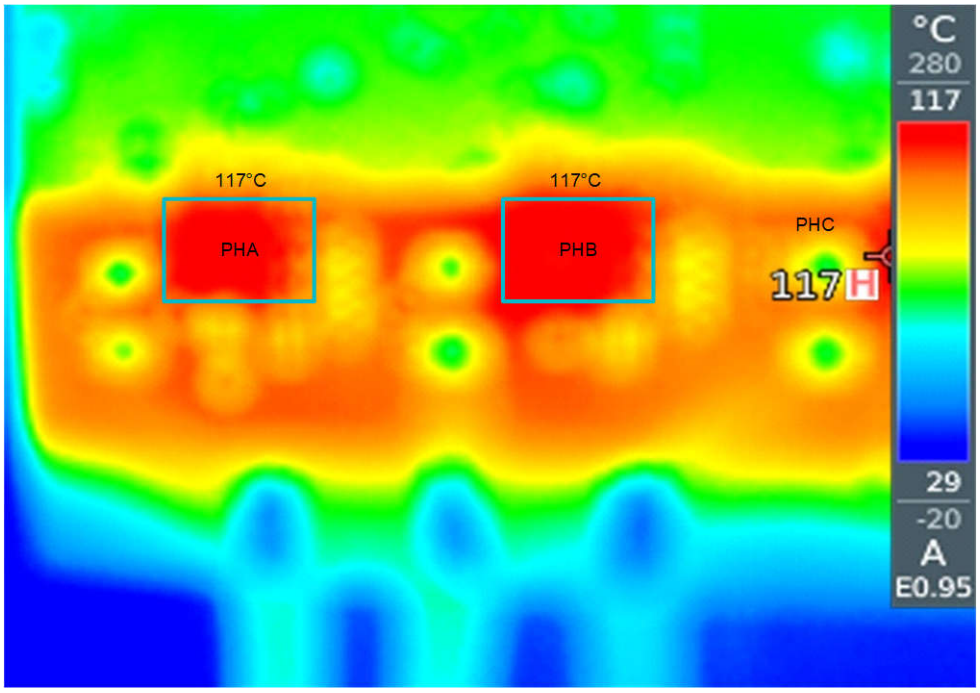
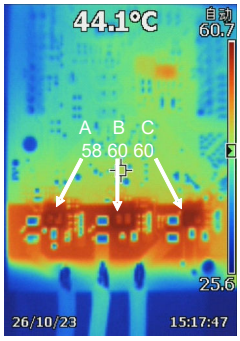


Figure 4-24. Thermal Picture of TIDA-010936 at 15.6A_{RMS} at 40kHz PWM

Since LMG2100 has exposed dies on top, the case temperature of LMG2100 can be very close to the temperature of the die. The recommended junction temperature is up to 125°C. In this test the GaN device achieved 117°C with 15.6A_{RMS} phase current.



PWM	A	B	C	/°C
40k:	56	57	58	
60k:	58	60	60	
80k:	59	60	60	

Figure 4-25. Thermal Picture of TIDA-010936 at 10A_{RMS} at 60kHz PWM and 40kHz and 80kHz

With 60kHz PWM and 10A_{RMS} output current, all three-phase GaN has 60°C case temperature. At 40kHz and 80kHz there is almost no difference of case temperature with 10A output.

4.5.5 No Load Loss Test (C_{OSS} Losses)

To see the effective parasitic capacitive losses, the TIDA-010936 PCB power losses were measured at zero load current with 50% PWM duty cycle and PWM switching frequencies from 8kHz to 80kHz, as shown in Equation 3.

$$P_{COSS_{loss}} = C_{OSS_{FET}} \times V_{DC}{}^{2} \times f_{PWM} \times 2 \quad (3)$$

The simulation was done using $C_{OSS(TR)}$ = 501pF from the LMG2100R044 data sheet, while adding an additional 80pF equivalent board related capacitance due to PCB and cabling parasitic capacitances.

To subtract the supply current offset on the TIDA-010936 at zero PWM switching, a first measurement was done without PWM switching, which yielded power losses of 0.765W at 48V supply without PWM switching. Then incremental increase of the power consumption starting from 8kHz to 80kHz PWM was printed against the simulated C_{OSS} power losses. In addition, the phase voltage resistor divider losses for sensing the three phase voltages (when switching) were subtracted from the measurement too, in order not to add these to the C_{OSS} power losses. The simulation is a good match with the measured C_{OSS} power losses.

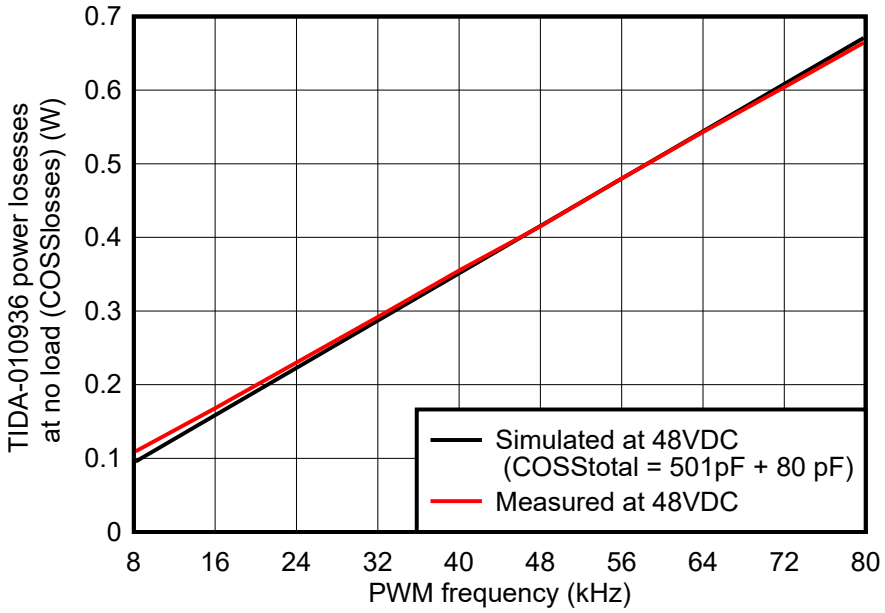


Figure 4-26. No Load (C_{OSS}) Power Losses at 48V_{DC} vs PWM Frequency

5 Design and Documentation Support

5.1 Design Files {Required Topic}

5.1.1 Schematics

To download the schematics, see the design files at TIDA-010936.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010936.

5.1.3 PCB Layout Recommendations

The layout for the LMG2100 in the TIDA-010936 PCB followed the layout examples in the *LMG2100R044 100-V, 35-A GaN Half-Bridge Power Stage* data sheet.

5.1.3.1 Layout Prints

To download the Layout Prints, see the design files at TIDA-010936.

5.1.4 Altium Project

To download the Altium project files, see the design files at TIDA-010936.

5.1.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010936.

5.1.6 Assembly Drawings

To download the Assembly Drawings, see the design files at TIDA-010936.

5.2 Tools and Software

Tools

LAUNCHXL-F28P65X C2000™ Real-Time MCU F28P65x LaunchPad™ Development Kit	LAUNCHXL-F28P65X is a low-cost development board for TI C2000™ real-time microcontrollers series of F28P65x devices. An excellent choice for initial evaluation and prototyping, the board provides a standardized and easy-to-use platform to develop applications. This extended version LaunchPad™ development kit offers extra pins for development and supports the connection of two BoosterPack™ plug-in modules. As part of the vast TI MCU LaunchPad ecosystem, the board is also cross-compatible with a broad range of plug-in modules.

Software

MotorControl Software Development Kit (SDK) for C2000™ MCU	MotorControl SDK for C2000™ microcontrollers (MCU) is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 real-time controller-based motor control system development time targeted for various three-phase motor control applications. The software includes firmware that runs on C2000 motor control evaluation modules (EVMs) and TI reference designs which are targeted for industrial drives, robotics, appliances, and automotive applications. MotorControl SDK provides all the needed resources at every stage of development and evaluation for high performance motor control applications.

5.3 Documentation Support

1. Texas Instruments, *Optimizing GaN Performance With an Integrated Driver White Paper*
2. Texas Instruments, *GaN FET Module Performance Advantage Over Silicon White Paper*
3. Texas Instruments, *LMG2100R044 100-V, 35-A GaN Half-Bridge Power Stage Data Sheet*
4. Texas Instruments, Gallium Nitride (GaN) Solutions
5. Texas Instruments, WEBENCH® Design Center
6. Texas Instruments, MotorWare™ Software
7. Texas Instruments , Low Voltage Servo Motor

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6 About the Author

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7 Recognition

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