Design Guide: TIDA-010259

Cascaded Clock Distribution Reference Design Supports 16 High Frequency Outputs

Description

Large phased array radar and communication systems require many transceiver channels, each with high speed data converters at the core of the analog signal chain. Integrated RF sampling data converters are ideal devices to proliferate the required channels. Each one of those devices requires a high-speed sampling clock with excellent phase noise performance. Since the sampling clock frequency is the same for all the devices, a single high-performance clock signal can be distributed to all of the data converter devices. This reference design showcases a cascaded LMX1204 clock distribution chip to distribute one clock source input to 16 differential clock outputs. The design supports frequencies over 12GHz and introduces negligible degradation to the phase noise performance through the distribution. All clock signals are synchronized to maintain deterministic latency and ensure phase aligned outputs.

Features

- 1-to-16 Clock Distribution Design
- Up to 12.8GHz Operation
- Very Low Phase Noise Performance
- 16 SysRef Outputs for JESD204B Data Converters
- Syncronized Outputs Maintain Deterministic Latency
- Optional Clock Divider or Clock Multiplier

Applications

- Phased Array Radar
- Electronic Warfare
- Communications Payload
- Radar Payload
- Software Defined Radio
- Active Antenna System

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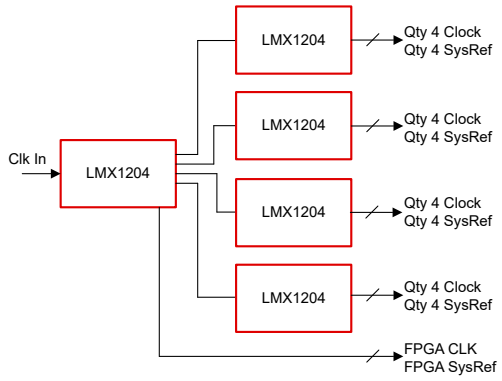
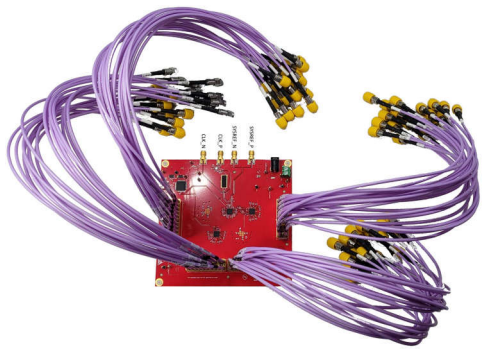
Resources

TIDA-010259	Design Folder
LMX1204	Product Folder
LMX1204EVM	EVM Folder
TPS62913	Product Folder
TPS7A4700	Product Folder





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1 System Description

The Cascaded Clock Distribution Reference Design uses multiple LMX1204 devices to distribute a single clock input to 16 clock outputs. The device operates up to 12.8GHz which supports high frequency clock distribution for high speed data converter applications. The design also provides 16 SysRef signals to data converters using the JESD204B digital interface protocol. There are 4 additional low speed clock outputs suitable for FPGA clocking. The design also incorporates options to divide-down or multiply-up the input clock signal. All outputs are synchronized to maintain deterministic latency within an array of data converter devices.

2 System Overview

2.1 Block Diagram

Figure 2-1 shows the block diagram of the reference design.

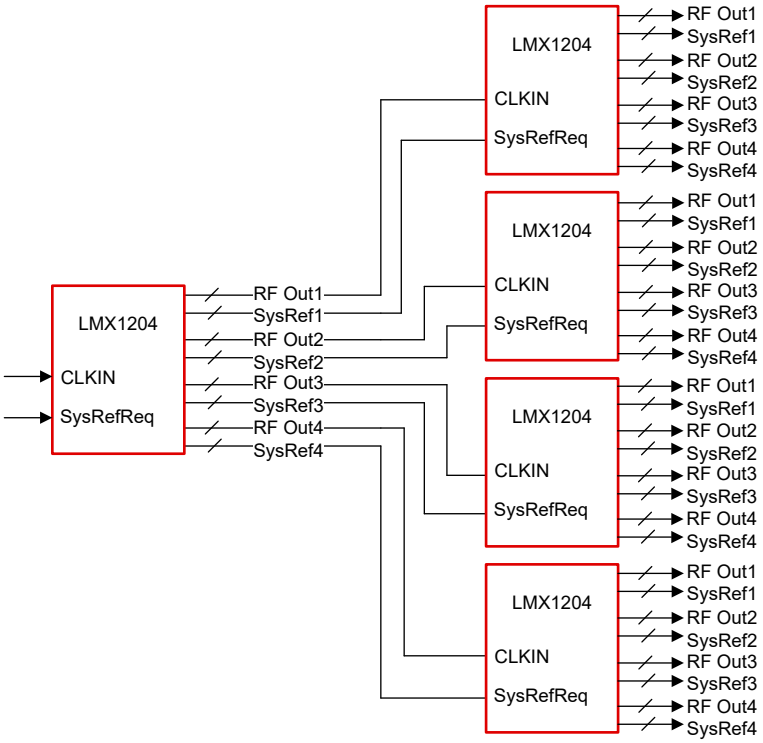

Figure 2-1. Reference Design Block Diagram

2.2 Design Considerations

RF sampling data converters require a low phase noise, high frequency clock signal. In a phased array system that employs many channels, the clock frequency is the same for each data converter device; hence, there is a need for distributing a single clock frequency. For the system to operate properly, all of the clock outputs must be phase aligned. Since phase noise performance is critical, the distribution network should not degrade phase noise performance compared to the original incoming signal.

The reference design demonstrates a cascaded LMX1204 device topology where the first level provides a 1:4 distribution. The second level takes each of those outputs and provides an additional 1:4 distribution, providing 16 outputs in total. The phase noise performance is not degraded within the distribution network. Since each output is independently buffered, all outputs maintain high signal levels negating any distribution losses through the network.

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2.3 Highlighted Products

2.3.1 LMX1204

The LMX1204 is a 1-to-4 clock distribution chip. The LMX1204 supports clock frequencies up to 12.8GHz and has very low additive jitter. All clock outputs are synchronized. In addition to the four high frequency outputs, there is an additional low frequency LOGICLK suitable for clocking FPGAs. Each output has an accompanying low frequency SysRef output for operation with data converters using the JESD204B digital interface. The SysRef signal can be generated internally or passed in as an input and re-clocked to the ouptuts. There is also an option to engage an input divide-down or multiply-up at the clock input.

2.3.2 TPS62913

The TPS62913 device is a high-efficiency, low-noise and low-ripple current mode synchronous buck converter. The TPS62913 is designed for powering noise sensitive data converters and clock devices. The device supports up to a 3A load.

2.3.3 TPS7A4700

The TPS7A4700 is an ultra-low-noise (4μVRMS), low-dropout linear regulator. The TPS7A4700 is capable of sourcing a 1A load. The device is designed for very sensitive clock and data converter power applications.

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3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

Evaluation of the reference design requires the following test equipment.

- 12V power supply
- R&S SMA100B Signal Generator (or equivalent)
- Spectrum Analyzer and or Phase Noise Analyzer

3.2 Test Setup

Figure 3-1 shows the test setup block diagram. Figure 3-2 shows a picture of the board with the RF connector cables for all 16 differential clock outputs and 16 differential SysRef signals.

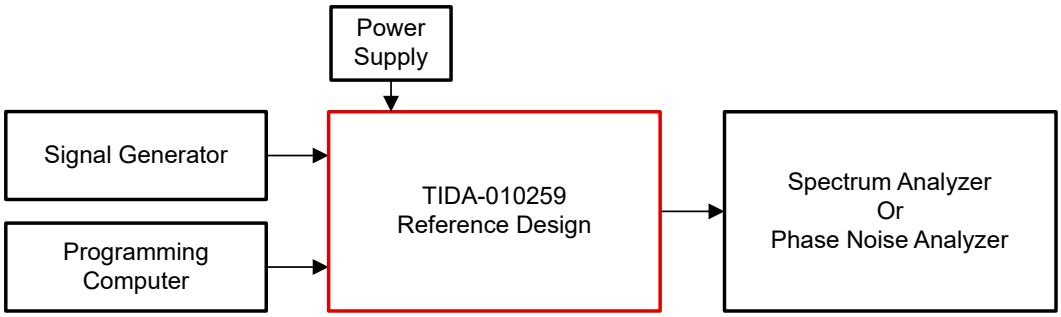

Figure 3-1. Reference Design Test Setup

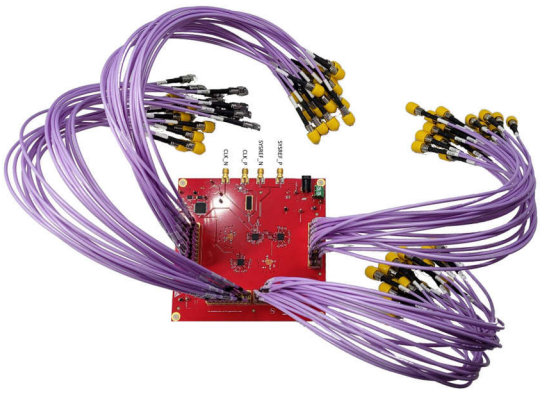

Figure 3-2. Cascaded Clock Distribution Board with RF Cables

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3.3 Test Results

Figure 3-3 shows the clock performance from one output at 12.8GHz compared to a standard SMA100B signal generator. There is no noticeable phase noise degradation due to the cascaded LMX1204 out to 1MHz offset. Afterward, the degradation at the higher frequency offsets is attributed to a higher thermal noise floor of the cascaded devices.

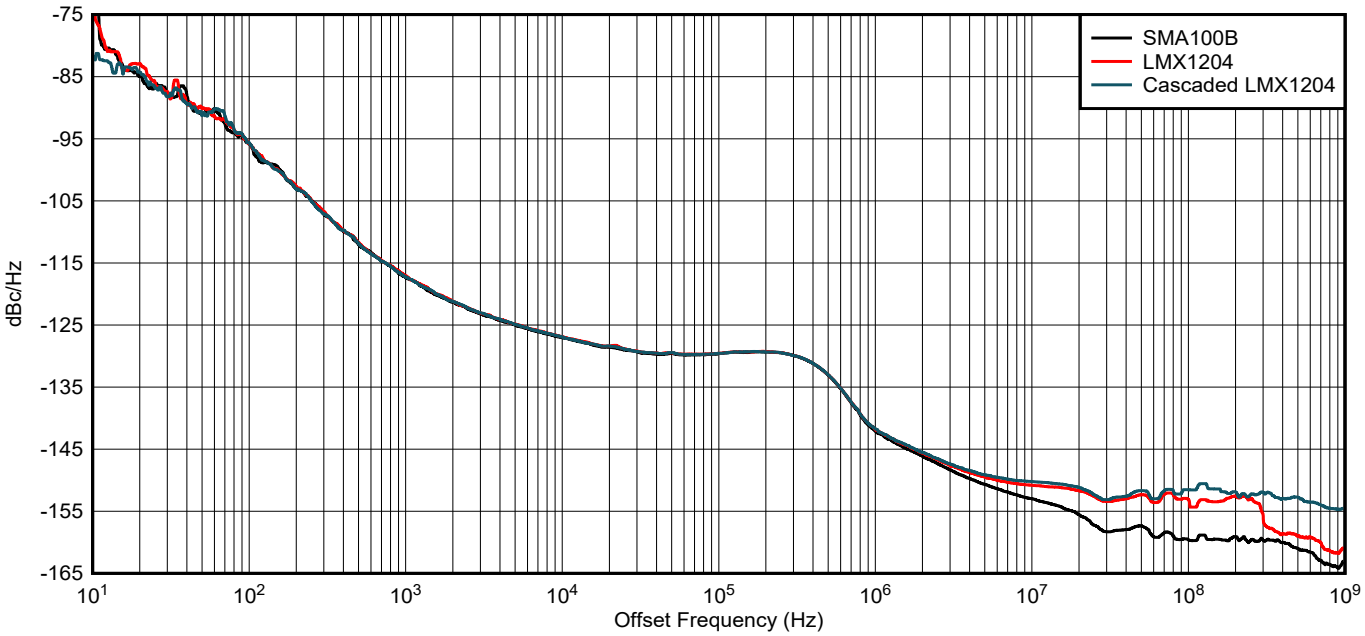

Figure 3-3. Cascaded LMX1204 vs R&S SMA100B Phase Noise Response

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4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010259.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010259.

4.2 Tools and Software

- TICSPRO-SW, LMX1204 Programming Software

4.3 Documentation Support

1. Texas Instruments, *Getting the Most of Your Data Converter Clocking System Using LMX1204 in Cascaded Configuration* application note.
2. Texas Instruments, *Cascaded LMX1204 Phase-Error Analysis* application note.
3. Texas Instruments, *LMX1204 Multiplier Clock Distribution Drives Large Phased-Array Systems* application note.

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

Russell Hoppenstein is a system engineer in the System Engineering Marketing (SEM) group supporting the Aerospace and Defense sector. He has over 20 years of semiconductor experience working with high-performance RF devices and RF sampling data converters for the communication and defense markets. He previously designed RF transceivers, active antenna systems, and linearized power amplifiers for the wireless infrastructure market. Russell earned his BSEE from the University of Texas at Austin and his MSEE from University of Texas at Arlington.

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