Design Guide: TIDA-020071

4 × Automotive Ethernet PHY Expansion for 100/1000Base-T1 Reference Design for Jacinto 7 Processors

Description

This reference design interfaces with Jacinto™ 7 processor EVM boards through the RGMII Ethernet Expansion Connector. Four automotive Ethernet connections are added through TI's automotive Ethernet physical layers (PHY). This design shows an implementation with TI's DP83TC818S-Q1 100Mbps and DP83TG721S-Q1 1000Mbps single-pair Ethernet (SPE) PHY. A coupling network is used to couple in 12V to the data line.

Resources

TIDA-020071	Design Folder
DP83TC817S-Q1, DP83TC818S-Q1	Product Folder
DP83TG720R-Q1, DP83TG721S-Q1	Product Folder
TPS74701-Q1, TPS7B82-Q1	Product Folder
TPS4H160-Q1	Product Folder

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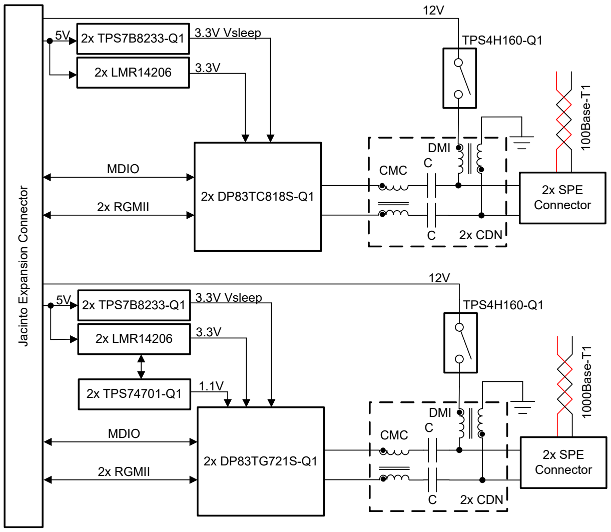
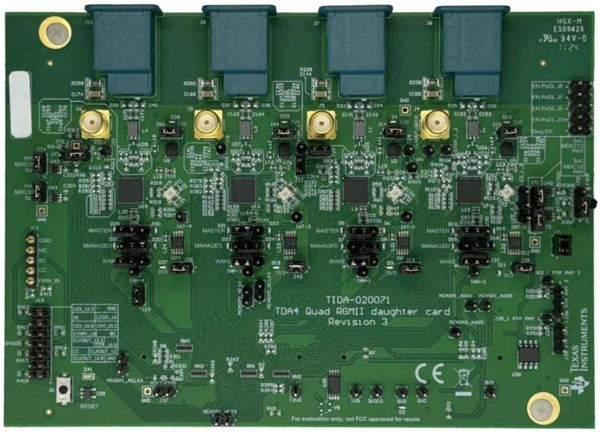
Features

- 100Base-T1 and 1000Base-T1 automotive Ethernet connection through RGMII to Jacinto™ 7 processors
- Option to provide the same clock to all four Ethernet PHYs
- Option to populate TI's BAW oscillator
- Automotive qualified filter network for 12V power coupling
- Board ID EEPROM for identification

Applications

- Advanced driver assistance systems (ADAS)
- Body electronics and lighting
- Infotainment and cluster
- Software-defined vehicle





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1 System Description

The Jacinto™ 7 EVMs are development on evaluation platforms that enable developers to write software and develop hardware around the Jacinto™ 7 family of processors. The main elements of the system are available on the EVM. This gives developers the basic resources needed for most general-purpose type projects that encompass the Jacinto™ 7 processor. Beyond the basic resources provided, additional functionality can be added through expansion cards.

This reference design adds four automotive Ethernet connections through TI's automotive Ethernet PHYs. The DP83TC818S-Q1 automotive Ethernet PHY supports 100Mbps link speed, is IEEE 802.3bw and OA 100BASE-T1 compliant, supports IEEE 1588v2, 802.1AS time synchronization, supports IEEE 1722 CRF packet decoding and Audio Video Bridging (AVB) media clock generation and supports IEEE 802.1AE MACsec. The DP83TG721 automotive Ethernet PHY supports 1000Mbps link speed, is IEEE 802.3bp compliant, IEEE 1588v2, 802.1AS time synchronization and has AVB IEEE 1722 media clock generation capability.

1.1 Key System Specifications

The key features of the TIDA-020071 design include the following:

- 100Base-T1 and 1000Base-T1 automotive Ethernet
- 12V can be coupled on the automotive Ethernet cable
- DP83TC818S-Q1 1.0V supplied by the internal LDO of the PHY
- Option to provide the same clock from TI's BAW oscillator through a clock buffer to all four Ethernet PHYs
- Option to populate TI's BAW oscillator
- Board ID EEPROM for identification

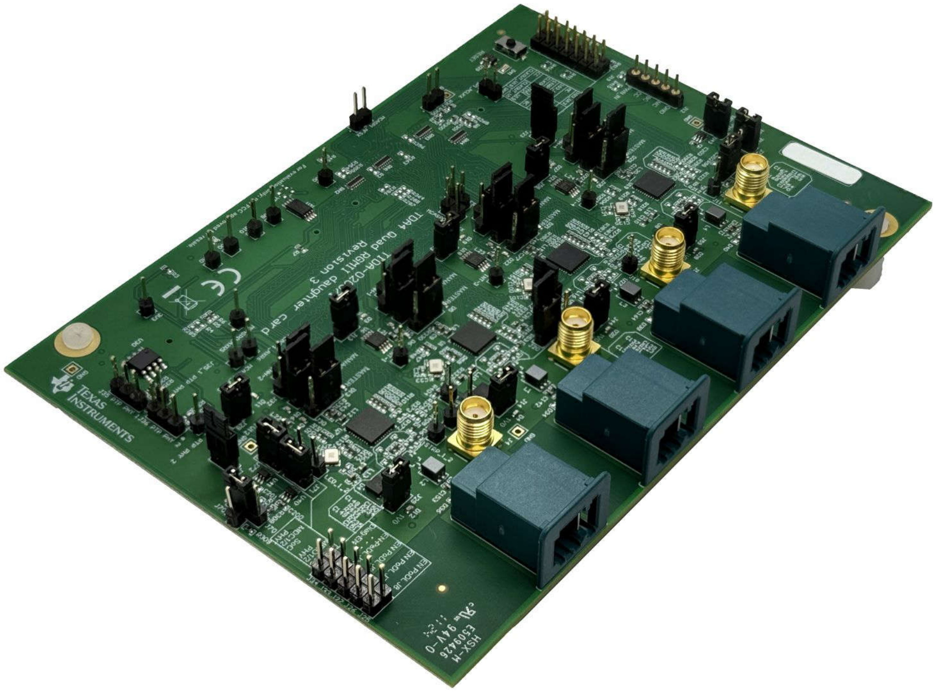

Figure 1-1. TIDA-020071 Board

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2 System Overview

Figure 2-1 illustrates that the system consists of one board, connected on one side through the expansion connector to a Jacinto™ 7 processor EVM and on the other side through twisted-pair cables with up to four link partners.

The Jacinto™ 7 EVM provides 5V power through the expansion connector to the buck converter and the LDO for 3.3V Vsleep. The EVM also provides 12V to the differential mode inductors to couple in power to the automotive Ethernet cable.

2.1 Block Diagram

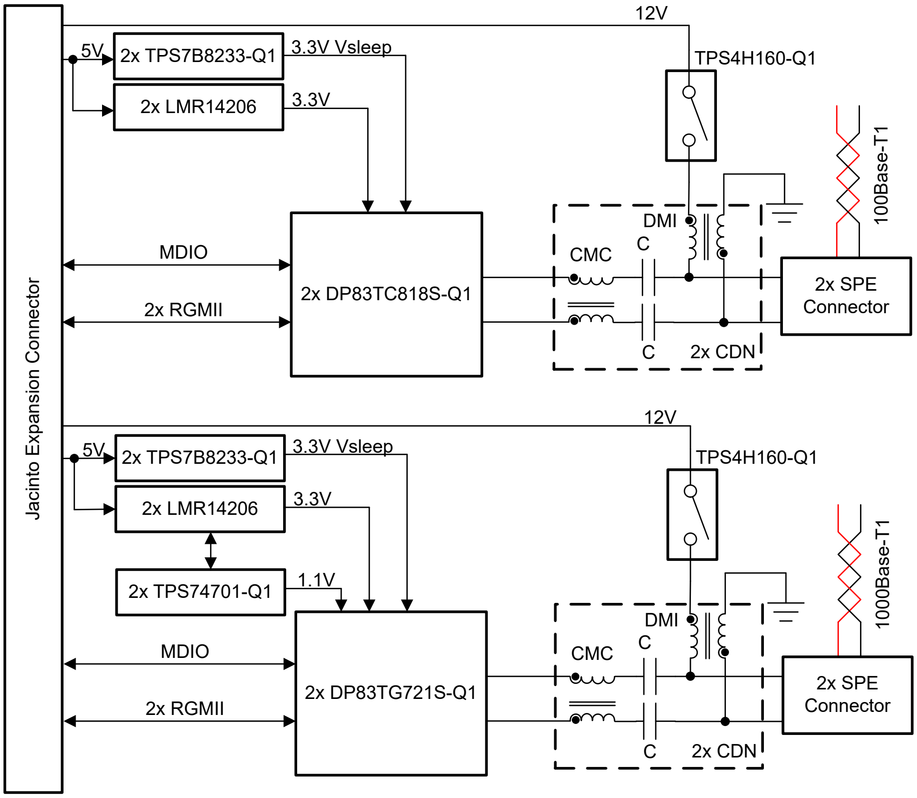

Figure 2-1. TIDA-020071 Block Diagram

2.2 Design Considerations

This reference design shows the implementation of an Ethernet interface consisting of a single-pair Ethernet (SPE) PHY with the option for powering a link partner through the same cable. This is part of Power over Data Lines (PoDL). Although PoDL is standardized in IEEE802.3bu for 100/1000Base-T1, this reference design is not compliant to IEEE802.3bu to address the automotive requirements. In the automotive sector, the car OEM defines which ECUs and sensor modules are used in the system and therefore a detection and classification is not required. This assumption is based on the fact that the network does not change over the lifetime of the vehicle. The boards are designed to fulfill the automotive requirements for a cost- and weight-efficient implementation.

With transmitting the power over the same cable as the data, the use of the classic fuse is no longer applicable, which is why the integration of a high-side switch (HSS) is strongly recommended to protect the link partner from any damage. The 12V supply for power coupling to the data line is generated on the Jacinto™ 7 EVM by a LM5175 buck-boost converter. This device already supports protection features including cycle-by-cycle current limiting, output overvoltage protection (OVP), and thermal shutdown. This reference design includes the TPS4H160-Q1 (High-Side Switch) which includes adjustable current limit, short-to-GND protection, thermal shutdown, and an inductive load negative voltage clamp.

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2.3 Highlighted Products

This section introduces the key devices in this reference design. For comprehensive details, see the product page and data sheet of each respective device.

2.3.1 DP83TC818S-Q1 (Automotive SPE PHY)

The DP83TC818S-Q1 device is an IEEE 802.3bw automotive Ethernet physical layer transceiver. The device provides all physical layer functions needed to transmit and receive data, and xMII interface flexibility. DP83TC818S-Q1 is compliant to Open Alliance EMC and interoperable specifications over unshielded single twisted-pair cable. DP83TC818S-Q1 supports OA TC-10 low-power sleep feature with wake forwarding for reduced system power consumption when communication is not required.

The DP83TC818S-Q1 integrates IEEE 802.1AE line rate security with authentication and optional encryption support, to secure communication over the network. The DP83TC818S-Q1 supports up to 16 secure association (SA) channels with automatic SAK rollover and extended packet numbering support. DP83TC818S-Q1 offers ingress classification to filter the unwanted packets and supports WAN MACsec for end-to-end security.

DP83TC818S-Q1 integrates IEEE 1588v2, 802.1AS hardware time stamping and fractional PLL, enabling highly accurate time synchronization. The fractional PLL enables frequency and phase synchronization of the wall clock (eliminating the need for external VCXO) and generation of a wide range of time synchronized frequencies needed for audio and other ADAS applications. The PHY also integrates IEEE 1722 CRF decode to generate Media clock and Bit Clock for AVB and other audio applications.

2.3.2 TPS7B8233-Q1 (3.3V Vsleep Ultra-Low-IQ Low-Dropout Regulator)

In automotive battery-connected applications, low quiescent current (I_Q) is important to save power and extend battery lifetime. Ultra-low I_Q must be included for always-on systems.

The TPS7B82-Q1 is a low-dropout linear regulator designed to operate with a wide input-voltage range from 3V to 40V (45V load dump protection). Operation down to 3V allows the TPS7B82-Q1 to continue operating during cold-crank and start and stop conditions. With only 2.7µA typical quiescent current at light load, this device is an excellent choice for powering microcontrollers (MCUs) and CAN or LIN transceivers in standby systems.

The device features integrated short-circuit and overcurrent protection. This device operates in ambient temperatures from –40°C to +125°C and with junction temperatures from –40°C to +150°C. Additionally, this device uses a thermally conductive package to enable sustained operation despite significant dissipation across the device. Because of these features, the device is designed as a power supply for various automotive applications.

2.3.3 TPS74701-Q1 (1.0V Rail Low-Dropout Regulator)

The TPS74701-Q1 low-dropout (LDO) linear regulator provides an easy-to-use, robust power management design for a wide variety of applications. The user-programmable soft-start minimizes stress on the input power source by reducing capacitive inrush current and the monotonic start-up is designed for powering many different types of processors and application-specific integrated circuits (ASIC). The enable input and power-good output allow easy sequencing with external regulators, allowing a design to be configured that meets the sequencing requirements for a wide range of applications with special start-up requirements.

A precision reference and error amplifier deliver 0.95% accuracy over load, line, temperature, and process. The device is stable with any type of capacitor greater than or equal to 2.2µF, and is fully specified per AEC-Q100.

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2.3.4 CDC6CE025000-Q1 (BAW Oscillator)

Texas Instruments' Bulk-Acoustic Wave (BAW) is a micro-resonator technology that enables integration of high-precision BAW resonator directly into packages with ultra-low jitter clock circuitry. BAW is fully designed and manufactured at TI factories like other silicon-based fabrication processes.

The CDC6x device is an ultra-low jitter, fixed-frequency oscillator which incorporates the BAW as the resonator source. The device is factory-programmed per specific operation mode, including frequency, voltage, output type, and function pin. With a high-performance fractional frequency divider, the CDC6x is capable of producing any frequency within the specified range providing a single device family for all frequency needs.

The high-performance clocking, mechanical stability, flexibility, and small package options for this device are designed for reference and core clocks in high-speed SERDES used in telecommunications, data and enterprise network, and industrial applications.

2.3.5 TPS4H160-Q1 (High-Side Switch)

The TPS4H160-Q1 device is a fully protected quad-channel, smart, high-side switch with four integrated 160mΩ NMOS power FETs.

The device includes full diagnostics and high-accuracy current sense enabling intelligent control of the load. An external adjustable current limit improves the reliability of whole system by limiting the inrush or overload current.

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3 System Design Theory

This section provides details about different sections on the reference design.

3.1 Ethernet PHY

This board supports a broad range of TI's automotive SPE PHYs. The board supports both 100Base-T1 and 1000Base-T1. By default, the board uses two 100Base-T1 systems with the DP83TC818S-Q1 and two DP83TG721S-Q1 SPE PHYs with the addresses shown in Table 3-1. The automotive Ethernet PHYs DP83TC818S-Q1 and DP83TG721S-Q1 and other TI SPE PHYs are pin-to-pin compatible and thereby can be interchanged with minor BOM changes.

Table 3-1. Ethernet PHY Addresses

ETHERNET PHY	DESIGNATOR	IEEE STANDARD	PHY ADDRESS
DP83TC818S-Q1	U13	100Base-T1	0x5
DP83TC818S-Q1	U19	100Base-T1	0x8
DP83TG721S-Q1	U1	1000Base-T1	0x0
DP83TG721S-Q1	U7	1000Base-T1	0x4

3.1.1 Ethernet PHY Power Supply

The DP83TC818S-Q1 is capable of operating with a wide range of I/O supply voltages (3.3V, 2.5V, or 1.8V). This board features an IO supply voltage of 3.3V to interface with various baseboards capable of 3.3V I/O voltage. The DP83TC818S-Q1 also requires a 1.0V rail. The implemented schematic shown in Figure 3-1 allows use of the DP83TC818S-Q1 integrated LDO to generate the required 1.0V. No power supply sequencing is required. Check and follow the DP83TC818S-Q1 Precise and Secure 100BASE-T1 Automotive Ethernet with TC10, IEEE802.1AS, IEEE802.1AE MACsec and AVB Clock Generation data sheet for the latest power supply device recommendation.

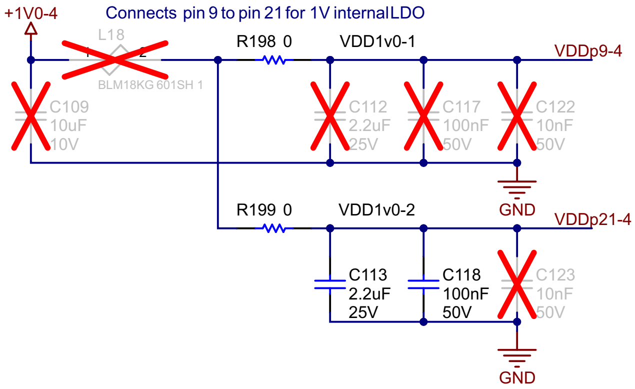

Figure 3-1. Ethernet PHY 1.0V Rail Schematic

3.1.2 Ethernet PHY Clock Source

The schematic shown in Figure 3-2 uses TI's BAW oscillator in conjunction with a clock buffer to be able to provide the same clock source to all four Ethernet PHYs on this reference design. This implementation can help with synchronization where the link partner then can use the recovered clock function of the Ethernet PHY to reduce the jitter of a time-synchronized system.

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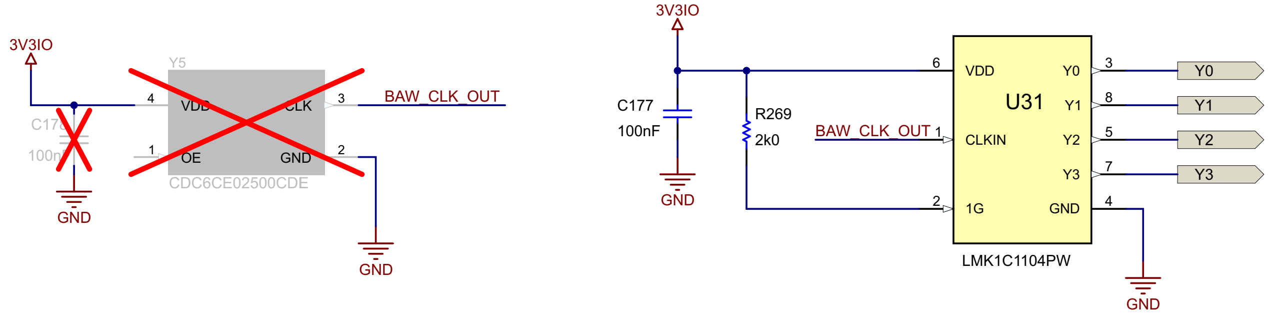

Figure 3-2. Ethernet PHY Clocking Schematic

3.2 Power Coupling Network

There are two main factors to consider when selecting a coupling network: Ethernet data rate and power consumption of the link partner. Table 3-2 shows each Ethernet PHY with the corresponding Ethernet standard and data frequency.

Table 3-2. Ethernet Signal Frequencies

ETHERNET PHY	IEEE STANDARD	DATA RATE	SYMBOL RATE
—	10Base-T1S	10Mbps	12.5MHz
DP83TC812-Q1	100Base-T1	100Mbps	66.6MHz
DP83TC813-Q1			
DP83TC814-Q1			
DP83TC817-Q1			
DP83TC818-Q1			
DP83TG720-Q1	1000Base-T1	1000Mbps	750MHz
DP83TG721-Q1			

There is a maximum current each coupling network can support while maintaining the required impedance based on the saturation characteristics of the components. Inductors do not behave in a ideal manner, the inductors dissipate heat, pass very high frequencies, and saturate when too much current is passed through. All components and cables have parasitic capacities and inductance throughout the entire circuit. Knowing the maximum power, the link partner draws from the power line and selecting a component design that can deliver that power for a given voltage is important. Calculate the maximum power as the worst-case scenario of power consumption on the link partner side.

Table 3-3 provides coupling network design suggestions. TI recommends selecting one of the networks based on the desired frequency range, current rating, and temperature.

Table 3-3. CDN Filter Design for PoDL

VENDOR	ETHERNET SPEED	COMPONENTS	CURRENT RATING	TEMPERATURE RATING
TDK	1000Base-T1	CMC: ACT1210G-800 DMI: ADL32VHR-3R9M	540mA	150°C
Murata	1000Base-T1	CMC: DLW32MH101XK2	—	—
TDK	100Base-T1	CMC: ACT1210L-201 DMI: ADL32VHR-180M	370mA	150°C
Murata	100Base-T1	CMC: DLW32MH201XK2	—	—

3.2.1 High-Side Switch

The TPS4H160-Q1 four channel high-side switch in combination with the jumpers J25, J26, J27, and J33 is used to enable or disable the coupling of 12V to the data line. Populate the jumpers to enable the output. The switch also provides protection against short-to-GND and thermal shutdown.

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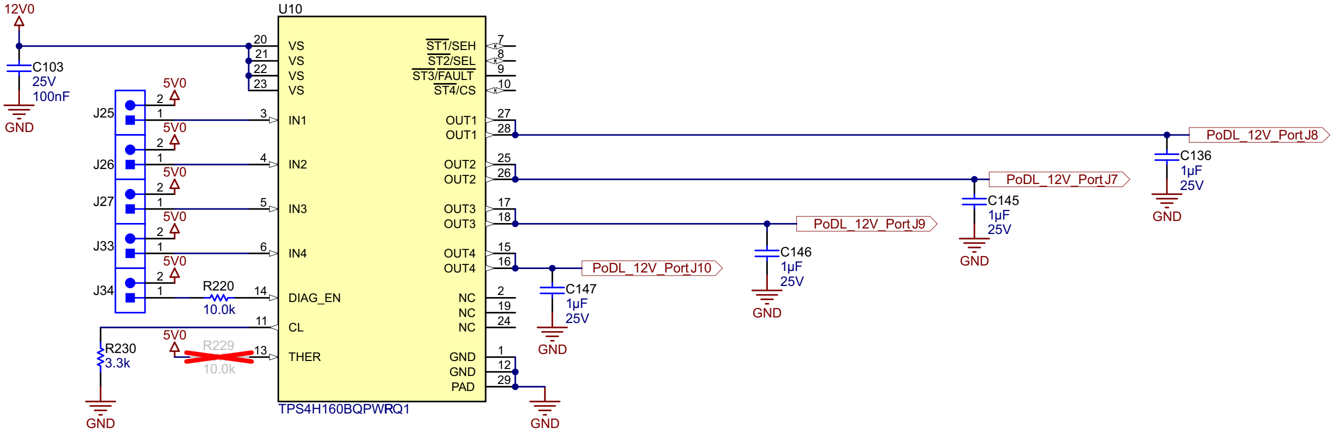

Figure 3-3. High-Side Switch Schematic

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4 Hardware, Software, Testing Requirements, and Test Results

This section describes the fundamental hardware and software requirements to demonstrate the automotive Ethernet functionality in a minimal setup. The setup allows to measurement of the maximum achievable bandwidth on IP networks.

4.1 Hardware Requirements

Table 4-1 lists the required hardware.

Table 4-1. Hardware Required for Minimal Setup

QUANTITY	DEVICE DESCRIPTION	DEVICE NUMBER
1 ×	4 × automotive Ethernet PHY reference design	TIDA-020071
1 ×	Jacinto 7 SoM board	J721EXSOMXEVM
1 ×	Common processor board for Jacinto 7 processors	J721EXCPXEVM
1 ×	Automotive-to-standard Ethernet media converter for 100Mbps	DP83TC812EVM-MC
1 ×	Automotive-to-standard Ethernet media converter for 1000Mbps	DP83TG721EVM-MC
1 ×	TE Connectivity MATEnet SPE cable	—
1 ×	RJ45 Cable	—
1 ×	12V, 5A power supply	—

4.2 Software Requirements

This section describes the software requirements for the minimal setup. The Software development kit (SDK) for Jacinto 7 processors is used to control and monitor the Ethernet PHY on this reference design shown in Figure 4-1 during testing.

Add the automotive Ethernet PHY driver to the Linux SDK so the Jacinto 7 processor can identify the Ethernet PHY. See also, the How to Integrate Linux Driver Into Your System application note.

The Linux Device Tree overlay for this specific board with the PHYs configured for PHY addresses 0x0, 0x4, 0x5 and 0x8 is shown in the following code block for Jacinto 7 SDK v10. For other SDK versions, see the SDK documentation.

```
/dts-v1/;
/plugin/;

#include <dt-bindings/gpio/gpio.h>
#include <dt-bindings/net/ti-dp83867.h>
#include "k3-pinctrl.h"

&{/} {
    aliases {
        ethernet1 = "/bus@100000/ethernet@c000000/ethernet-ports/port@1";
        ethernet2 = "/bus@100000/ethernet@c000000/ethernet-ports/port@2";
        ethernet3 = "/bus@100000/ethernet@c000000/ethernet-ports/port@3";
        ethernet4 = "/bus@100000/ethernet@c000000/ethernet-ports/port@4";
    };
};

&cpsw0 {
    status = "okay";
    pinctrl-names = "default";
    pinctrl-0 = <&rgmii1_pins_default
             &rgmii2_pins_default
             &rgmii3_pins_default
             &rgmii4_pins_default>;
};

&cpsw0_port1 {
    status = "okay";
    phy-handle = <&cpsw9g_phy0>;
    phy-mode = "rgmii-rxid";
```

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```
    mac-address = [00 00 00 00 00 00];
    phys = <&cpsw0_phy_gmii_sel 1>;
};

&cpsw0_port2 {
    status = "okay";
    phy-handle = <&cpsw9g_phy4>;
    phy-mode = "rgmii-rxid";
    mac-address = [00 00 00 00 00 00];
    phys = <&cpsw0_phy_gmii_sel 2>;
};

&cpsw0_port3 {
    status = "okay";
    phy-handle = <&cpsw9g_phy5>;
    phy-mode = "rgmii-rxid";
    mac-address = [00 00 00 00 00 00];
    phys = <&cpsw0_phy_gmii_sel 3>;
};

&cpsw0_port4 {
    status = "okay";
    phy-handle = <&cpsw9g_phy8>;
    phy-mode = "rgmii-rxid";
    mac-address = [00 00 00 00 00 00];
    phys = <&cpsw0_phy_gmii_sel 4>;
};

&cpsw9g_mdio {
    status = "okay";
    pinctrl-names = "default";
    pinctrl-0 = <&mdio0_pins_default>;
    bus_freq = <1000000>;
    #address-cells = <1>;
    #size-cells = <0>;

    cpsw9g_phy0: ethernet-phy@0 {
        reg = <0>;
    };
    cpsw9g_phy4: ethernet-phy@4 {
        reg = <4>;
    };
    cpsw9g_phy5: ethernet-phy@5 {
        reg = <5>;
    };
    cpsw9g_phy8: ethernet-phy@8 {
        reg = <8>;
    };
};


&main_pmx0 {
    mdio0_pins_default: mdio0-pins-default {
        pinctrl-single,pins = <
            J721E_IOPAD(0x1bc, PIN_OUTPUT, 0) /* (V24) MDIO0_MDC */
            J721E_IOPAD(0x1b8, PIN_INPUT, 0) /* (V26) MDIO0_MDIO */
        >;
    };

    rgmii1_pins_default: rgmii1-pins-default {
        pinctrl-single,pins = <
            J721E_IOPAD(0x4, PIN_INPUT, 4) /* (AC23) PRG1_PRU0_GPO0.RGMII1_RD0 */
            J721E_IOPAD(0x8, PIN_INPUT, 4) /* (AG22) PRG1_PRU0_GPO1.RGMII1_RD1 */
            J721E_IOPAD(0xc, PIN_INPUT, 4) /* (AF22) PRG1_PRU0_GPO2.RGMII1_RD2 */
            J721E_IOPAD(0x10, PIN_INPUT, 4) /* (AJ23) PRG1_PRU0_GPO3.RGMII1_RD3 */
            J721E_IOPAD(0x1c, PIN_INPUT, 4) /* (AD22) PRG1_PRU0_GPO6.RGMII1_RXC */
            J721E_IOPAD(0x14, PIN_INPUT, 4) /* (AH23) PRG1_PRU0_GPO4.RGMII1_RX_CTL */
            J721E_IOPAD(0x30, PIN_OUTPUT, 4) /* (AF24) PRG1_PRU0_GPO11.RGMII1_TD0 */
            J721E_IOPAD(0x34, PIN_OUTPUT, 4) /* (AJ24) PRG1_PRU0_GPO12.RGMII1_TD1 */
            J721E_IOPAD(0x38, PIN_OUTPUT, 4) /* (AG24) PRG1_PRU0_GPO13.RGMII1_TD2 */
            J721E_IOPAD(0x3c, PIN_OUTPUT, 4) /* (AD24) PRG1_PRU0_GPO14.RGMII1_TD3 */
            J721E_IOPAD(0x44, PIN_OUTPUT, 4) /* (AE24) PRG1_PRU0_GPO16.RGMII1_TXC */
            J721E_IOPAD(0x40, PIN_OUTPUT, 4) /* (AC24) PRG1_PRU0_GPO15.RGMII1_TX_CTL */
        >;
    };

    rgmii2_pins_default: rgmii2-pins-default {
        pinctrl-single,pins = <
```

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```
            J721E_IOPAD(0x58, PIN_INPUT, 4) /* (AE22) PRG1_PRU1_GPO0.RGMII2_RD0 */
            J721E_IOPAD(0x5c, PIN_INPUT, 4) /* (AG23) PRG1_PRU1_GPO1.RGMII2_RD1 */
            J721E_IOPAD(0x60, PIN_INPUT, 4) /* (AF23) PRG1_PRU1_GPO2.RGMII2_RD2 */
            J721E_IOPAD(0x64, PIN_INPUT, 4) /* (AD23) PRG1_PRU1_GPO3.RGMII2_RD3 */
            J721E_IOPAD(0x70, PIN_INPUT, 4) /* (AE23) PRG1_PRU1_GPO6.RGMII2_RXC */
            J721E_IOPAD(0x68, PIN_INPUT, 4) /* (AH24) PRG1_PRU1_GPO4.RGMII2_RX_CTL */
            J721E_IOPAD(0x84, PIN_OUTPUT, 4) /* (AJ25) PRG1_PRU1_GPO11.RGMII2_TD0 */
            J721E_IOPAD(0x88, PIN_OUTPUT, 4) /* (AH25) PRG1_PRU1_GPO12.RGMII2_TD1 */
            J721E_IOPAD(0x8c, PIN_OUTPUT, 4) /* (AG25) PRG1_PRU1_GPO13.RGMII2_TD2 */
            J721E_IOPAD(0x90, PIN_OUTPUT, 4) /* (AH26) PRG1_PRU1_GPO14.RGMII2_TD3 */
            J721E_IOPAD(0x98, PIN_OUTPUT, 4) /* (AJ26) PRG1_PRU1_GPO16.RGMII2_TXC */
            J721E_IOPAD(0x94, PIN_OUTPUT, 4) /* (AJ27) PRG1_PRU1_GPO15.RGMII2_TX_CTL */
        >;
    };

    rgmii3_pins_default: rgmii3-pins-default {
        pinctrl-single,pins = <
            J721E_IOPAD(0xb0, PIN_INPUT, 4) /* (AF28) PRG0_PRU0_GPO0.RGMII3_RD0 */
            J721E_IOPAD(0xb4, PIN_INPUT, 4) /* (AE28) PRG0_PRU0_GPO1.RGMII3_RD1 */
            J721E_IOPAD(0xb8, PIN_INPUT, 4) /* (AE27) PRG0_PRU0_GPO2.RGMII3_RD2 */
            J721E_IOPAD(0xbc, PIN_INPUT, 4) /* (AD26) PRG0_PRU0_GPO3.RGMII3_RD3 */
            J721E_IOPAD(0xc8, PIN_INPUT, 4) /* (AE26) PRG0_PRU0_GPO6.RGMII3_RXC */
            J721E_IOPAD(0xc0, PIN_INPUT, 4) /* (AD25) PRG0_PRU0_GPO4.RGMII3_RX_CTL */
            J721E_IOPAD(0xdc, PIN_OUTPUT, 4) /* (AJ28) PRG0_PRU0_GPO11.RGMII3_TD0 */
            J721E_IOPAD(0xe0, PIN_OUTPUT, 4) /* (AH27) PRG0_PRU0_GPO12.RGMII3_TD1 */
            J721E_IOPAD(0xe4, PIN_OUTPUT, 4) /* (AH29) PRG0_PRU0_GPO13.RGMII3_TD2 */
            J721E_IOPAD(0xe8, PIN_OUTPUT, 4) /* (AG28) PRG0_PRU0_GPO14.RGMII3_TD3 */
            J721E_IOPAD(0xf0, PIN_OUTPUT, 4) /* (AH28) PRG0_PRU0_GPO16.RGMII3_TXC */
            J721E_IOPAD(0xec, PIN_OUTPUT, 4) /* (AG27) PRG0_PRU0_GPO15.RGMII3_TX_CTL */
        >;
    };

    rgmii4_pins_default: rgmii4-pins-default {
        pinctrl-single,pins = <
            J721E_IOPAD(0x100, PIN_INPUT, 4) /* (AE29) PRG0_PRU1_GPO0.RGMII4_RD0 */
            J721E_IOPAD(0x104, PIN_INPUT, 4) /* (AD28) PRG0_PRU1_GPO1.RGMII4_RD1 */
            J721E_IOPAD(0x108, PIN_INPUT, 4) /* (AD27) PRG0_PRU1_GPO2.RGMII4_RD2 */
            J721E_IOPAD(0x10c, PIN_INPUT, 4) /* (AC25) PRG0_PRU1_GPO3.RGMII4_RD3 */
            J721E_IOPAD(0x118, PIN_INPUT, 4) /* (AC26) PRG0_PRU1_GPO6.RGMII4_RXC */
            J721E_IOPAD(0x110, PIN_INPUT, 4) /* (AD29) PRG0_PRU1_GPO4.RGMII4_RX_CTL */
            J721E_IOPAD(0x12c, PIN_OUTPUT, 4) /* (AG26) PRG0_PRU1_GPO11.RGMII4_TD0 */
            J721E_IOPAD(0x130, PIN_OUTPUT, 4) /* (AF27) PRG0_PRU1_GPO12.RGMII4_TD1 */
            J721E_IOPAD(0x134, PIN_OUTPUT, 4) /* (AF26) PRG0_PRU1_GPO13.RGMII4_TD2 */
            J721E_IOPAD(0x138, PIN_OUTPUT, 4) /* (AE25) PRG0_PRU1_GPO14.RGMII4_TD3 */
            J721E_IOPAD(0x140, PIN_OUTPUT, 4) /* (AG29) PRG0_PRU1_GPO16.RGMII4_TXC */
            J721E_IOPAD(0x13c, PIN_OUTPUT, 4) /* (AF29) PRG0_PRU1_GPO15.RGMII4_TX_CTL */
        >;
    };
};
```

In addition to adding the PHY driver, adjust the following *Device Tree*, to enable the Ethernet interface:

Change the linked firmware (`r5f0_0-fw`) with the following command:

```
ln -sfn /usr/lib/firmware/ti-ipc/j721e/ipc_echo_test_mcu2_0_release_strip.xer5f /lib/firmware/j7-
main-r5f0_0-fw
```

With the board powered up, use the following terminal command to confirm the PHY address (phy[x]) and eth port (eth[y]):

```
dmesg | grep mdio
```

```
davinci_mdio c000f00.mdio: phy[0]: device c000f00.mdio:00, driver TI DP83TG721CS1.0
davinci_mdio c000f00.mdio: phy[4]: device c000f00.mdio:04, driver TI DP83TG721CS1.0
davinci_mdio c000f00.mdio: phy[5]: device c000f00.mdio:05, driver TI DP83TC818CS2.0
davinci_mdio c000f00.mdio: phy[8]: device c000f00.mdio:08, driver TI DP83TC818CS2.0
am65-cpsw-nuss c000000.ethernet eth1: PHY [c000f00.mdio:00] driver [TI DP83TG721CS1.0] (irq=POLL)
am65-cpsw-nuss c000000.ethernet eth2: PHY [c000f00.mdio:04] driver [TI DP83TG721CS1.0] (irq=POLL)
am65-cpsw-nuss c000000.ethernet eth3: PHY [c000f00.mdio:05] driver [TI DP83TC818CS2.0] (irq=POLL)
am65-cpsw-nuss c000000.ethernet eth4: PHY [c000f00.mdio:08] driver [TI DP83TC818CS2.0] (irq=POLL)
```

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4.3 Test Setup

Figure 4-1 shows the block diagram of the test setup. The setup consists of a Jacinto 7 processor EVM, TIDA-020071, DP83TC812EVM-MC, DP83TG721EVM-MC, an Ethernet Switch, a standard PC, and cable assemblies.

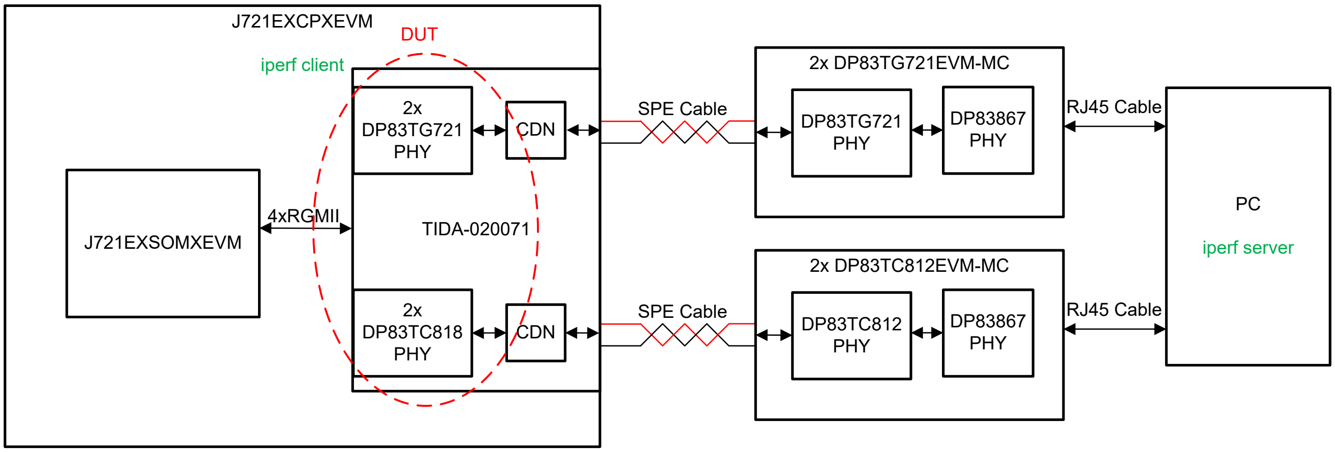

Figure 4-1. IP network bandwidth test setup

iPerf3, an open-source tool used to measure network performance and bandwidth, and is already integrated in TI's SDK. Use iPerf3 with the following commands after an IP address is assigned to the Ethernet port. iPerf3 can be used to test each interface individually or when creating multiple server instances on different ports, multiple client connections can be established to test multiple interfaces simultaneously.

Run the following command on the PC (server):

```
iperf3 -s
```

Additionally, run the following command on the Jacinto 7 (client):

```
iperf3 -c 192.168.1.1 (the IP address of the server)
```

4.4 Test Results

The following code block is captured from the Jacinto 7 EVM. With the 100 Mbits/sec connection, observe that 114 MBytes (112 MBytes) of data successfully transferred and the bandwidth is very close to the advertised speed of the network port (100 Mbit/sec). On the 1000 Mbit/sec setup, observe that 1.10 GBytes of data successfully transferred and the bandwidth is very close to the advertised speed of the network port (1000 Mbit/sec).

The following code block shows the 100Mbit/sec connection:

```
root@j721e-evm:~# iperf3 -c 192.168.1.1
Connecting to host 192.168.1.1, port 5201
[  5] local 192.168.1.237 port 32836 connected to 192.168.1.1 port 5201
[ ID] Interval           Transfer     Bitrate         Retr  Cwnd
[  5]   0.00-1.00   sec  12.6 MBytes   106 Mbits/sec    0    249 KBytes
[  5]   1.00-2.00   sec  10.9 MBytes  91.7 Mbits/sec    0    249 KBytes
[  5]   2.00-3.00   sec  11.4 MBytes  95.9 Mbits/sec    0    249 KBytes
[  5]   3.00-4.00   sec  10.9 MBytes  91.7 Mbits/sec    0    249 KBytes
[  5]   4.00-5.00   sec  11.4 MBytes  95.9 Mbits/sec    0    249 KBytes
[  5]   5.00-6.00   sec  11.4 MBytes  95.9 Mbits/sec    0    249 KBytes
[  5]   6.00-7.00   sec  10.9 MBytes  91.7 Mbits/sec    0    249 KBytes
[  5]   7.00-8.00   sec  11.4 MBytes  95.9 Mbits/sec    0    249 KBytes
[  5]   8.00-9.00   sec  10.9 MBytes  91.7 Mbits/sec    0    249 KBytes
[  5]   9.00-10.00  sec  11.4 MBytes  95.9 Mbits/sec    0    249 KBytes
- - - - - - - - - - - - - - - - - - - - - - - - -
[ ID] Interval           Transfer     Bitrate         Retr
[  5]   0.00-10.00  sec   114 MBytes  95.2 Mbits/sec    0             sender
```

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```
[  5]   0.00-10.05  sec   112 MBytes  93.8 Mbits/sec                  receiver
iperf Done.
```

The following code block shows the 1000Mbit/sec connection:

```
root@j721e-evm:~# iperf3 -c 192.168.1.1
Connecting to host 192.168.1.1, port 5201
[  5] local 192.168.1.81 port 52240 connected to 192.168.1.1 port 5201
[ ID] Interval           Transfer     Bitrate         Retr  Cwnd
[  5]   0.00-1.00   sec   114 MBytes   957 Mbits/sec    0    362 KBytes
[  5]   1.00-2.00   sec   112 MBytes   936 Mbits/sec   10    365 KBytes
[  5]   2.00-3.00   sec   112 MBytes   944 Mbits/sec   10    369 KBytes
[  5]   3.00-4.00   sec   112 MBytes   942 Mbits/sec   20    342 KBytes
[  5]   4.00-5.00   sec   112 MBytes   943 Mbits/sec   10    366 KBytes
[  5]   5.00-6.00   sec   113 MBytes   945 Mbits/sec   20    315 KBytes
[  5]   6.00-7.00   sec   112 MBytes   940 Mbits/sec   10    363 KBytes
[  5]   7.00-8.00   sec   112 MBytes   938 Mbits/sec   20    264 KBytes
[  5]   8.00-9.00   sec   113 MBytes   947 Mbits/sec   10    346 KBytes
[  5]   9.00-10.00  sec   112 MBytes   936 Mbits/sec   10    368 KBytes
- - - - - - - - - - - - - - - - - - - - - - - - -
[ ID] Interval           Transfer     Bitrate         Retr
[  5]   0.00-10.00  sec  1.10 GBytes   943 Mbits/sec  120             sender
[  5]   0.00-10.04  sec  1.10 GBytes   938 Mbits/sec                  receiver
iperf Done.
```

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5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-020071.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-020071.

5.2 Tools and Software

Tools

ETHERNET-SW	Ethernet PHY Linux drivers and tools
J721EXCPXEVM	Common processor board for Jacinto™ 7 processors
J721EXSOMXEVM	TDA4VM and DRA829V system on module (SoM)

Software

PROCESSOR-SDK-J721E	Software development kit for DRA829 and TDA4VM Jacinto™ processors

5.3 Documentation Support

1. Texas Instruments, *How to Integrate Linux Driver Into Your System Application Note*
2. Texas Instruments, *DP83TC818S-Q1 Precise and Secure 100BASE-T1 Automotive Ethernet with TC10, IEEE802.1AS and IEEE802.1AE MACsec and AVB Clock Generation Data Sheet*
3. Texas Instruments, *DP83TG721x-Q1 1000BASE-T1 Automotive Ethernet PHY with Advanced TSN and AVB Data Sheet*
4. Texas Instruments, *DP83TC811, DP83TC812, DP83TC814, DP83TG720 Hardware Rollover Document Application Note*
5. Texas Instruments, *TDA4: Custom Board Bring Up Guide Application Note*
6. Texas Instruments, *High-Speed Interface Layout Guidelines Application Note*

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6 About the Author

YANNIK MUENDLER is a systems engineer at Texas Instruments contributing to the Automotive ADAS Systems Engineering team. In this role, he plays a pivotal part in the development of reference designs within the automotive sector. With a wealth of expertise in areas such as high-performance compute with TI's Jacinto™ 7 processors and communication interfaces such as single-pair Ethernet and FPD-Link™ technology, Yannik brings a depth of knowledge and experience to his responsibilities.

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