

123456789

A

B

C

D

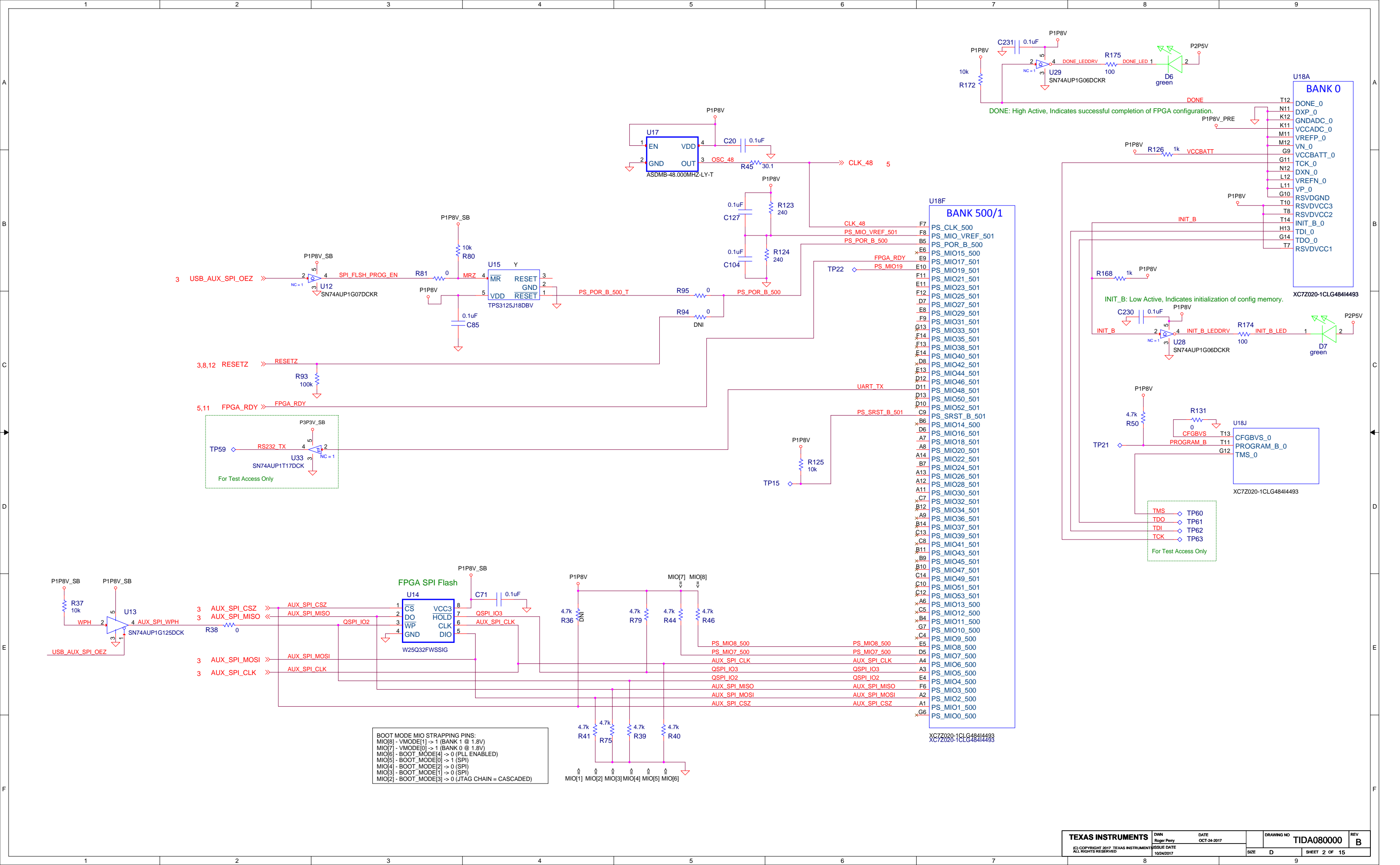
E

F

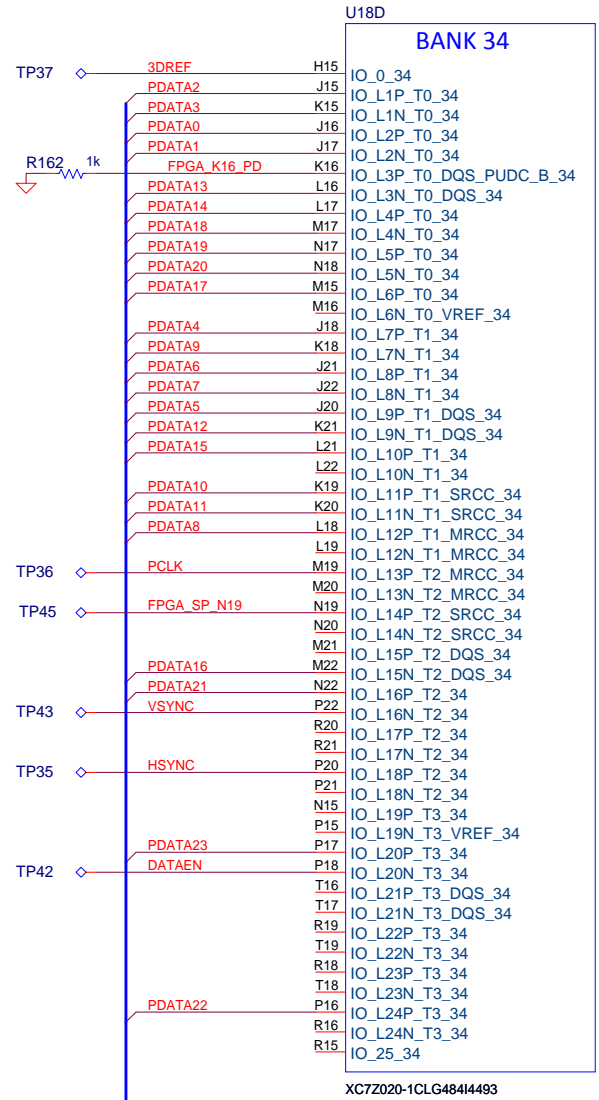
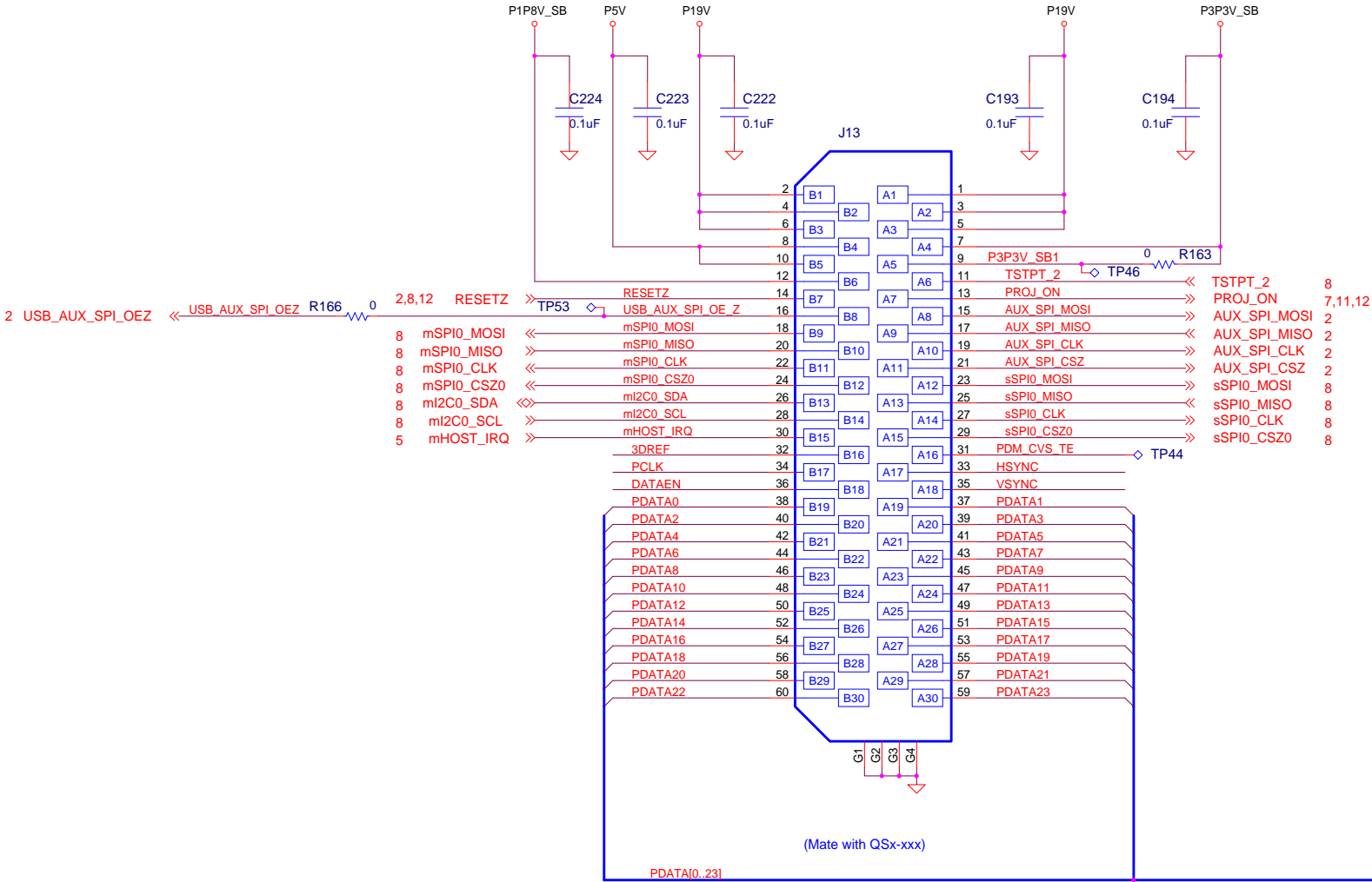
TIDA080000 DISPLAY BOARD

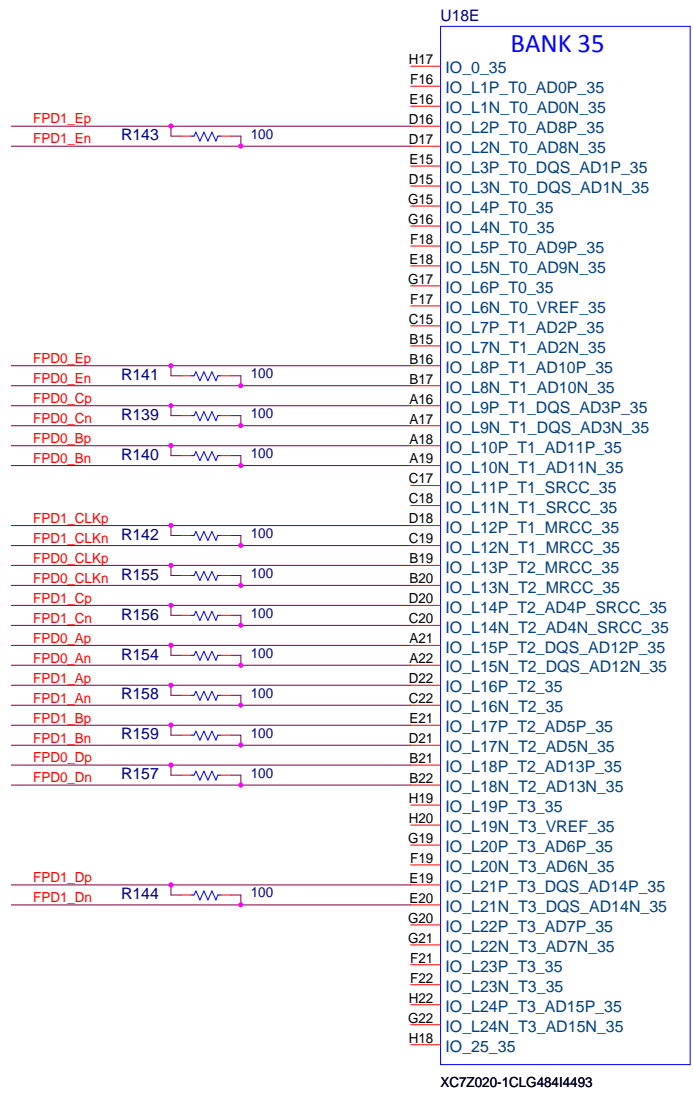
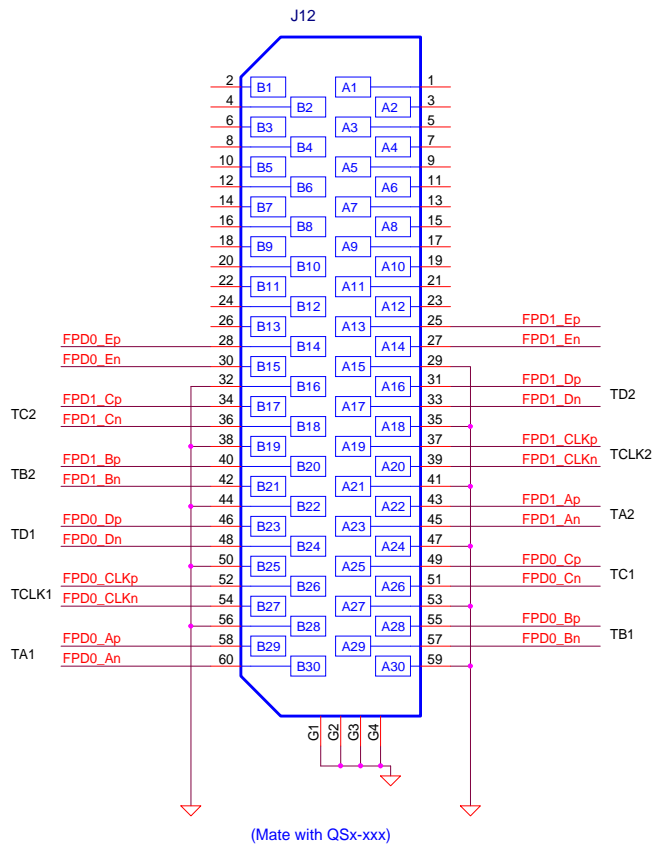
COMPUTER GENERATED DRAWING - DO NOT REVISE MANUALLY				
REVISIONS				
REV	DESCRIPTION		DATE	APPROVED
B	ECO	DDR3 & DLPA3000 updates	08/15/2018	K.LOWDERMAN

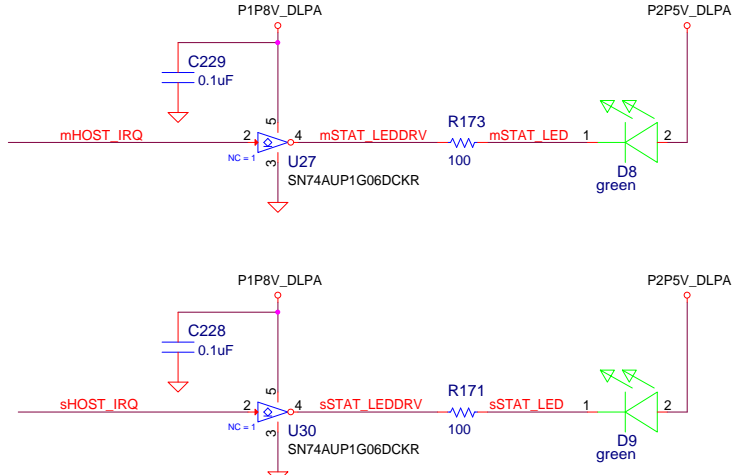
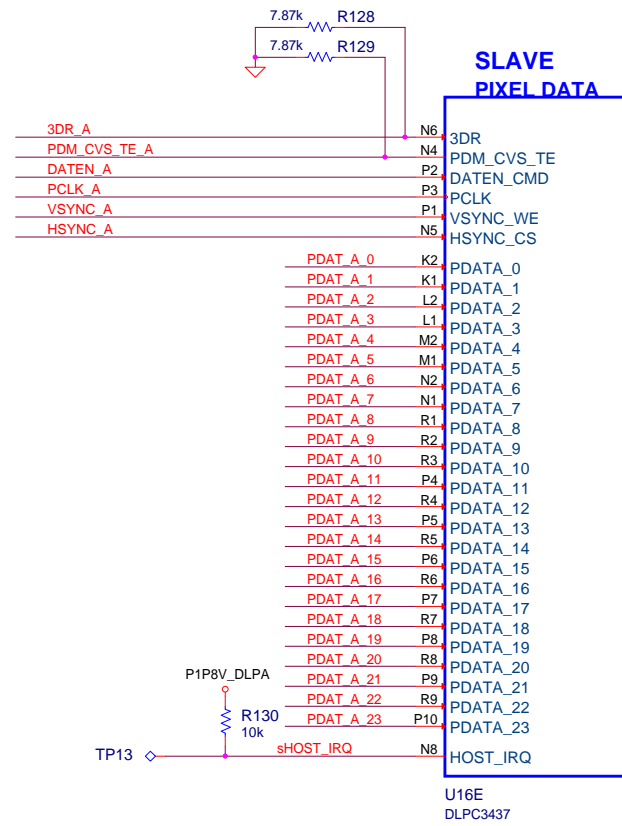
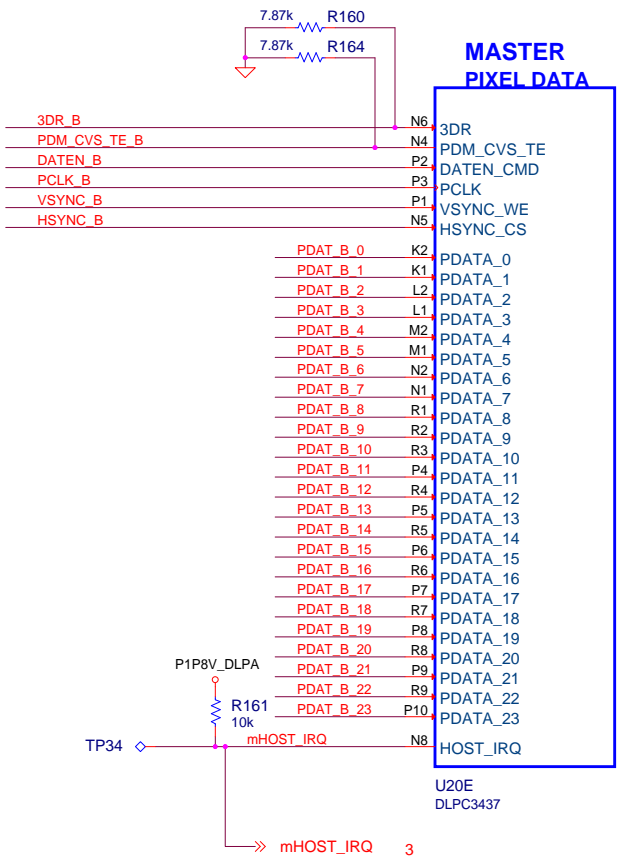
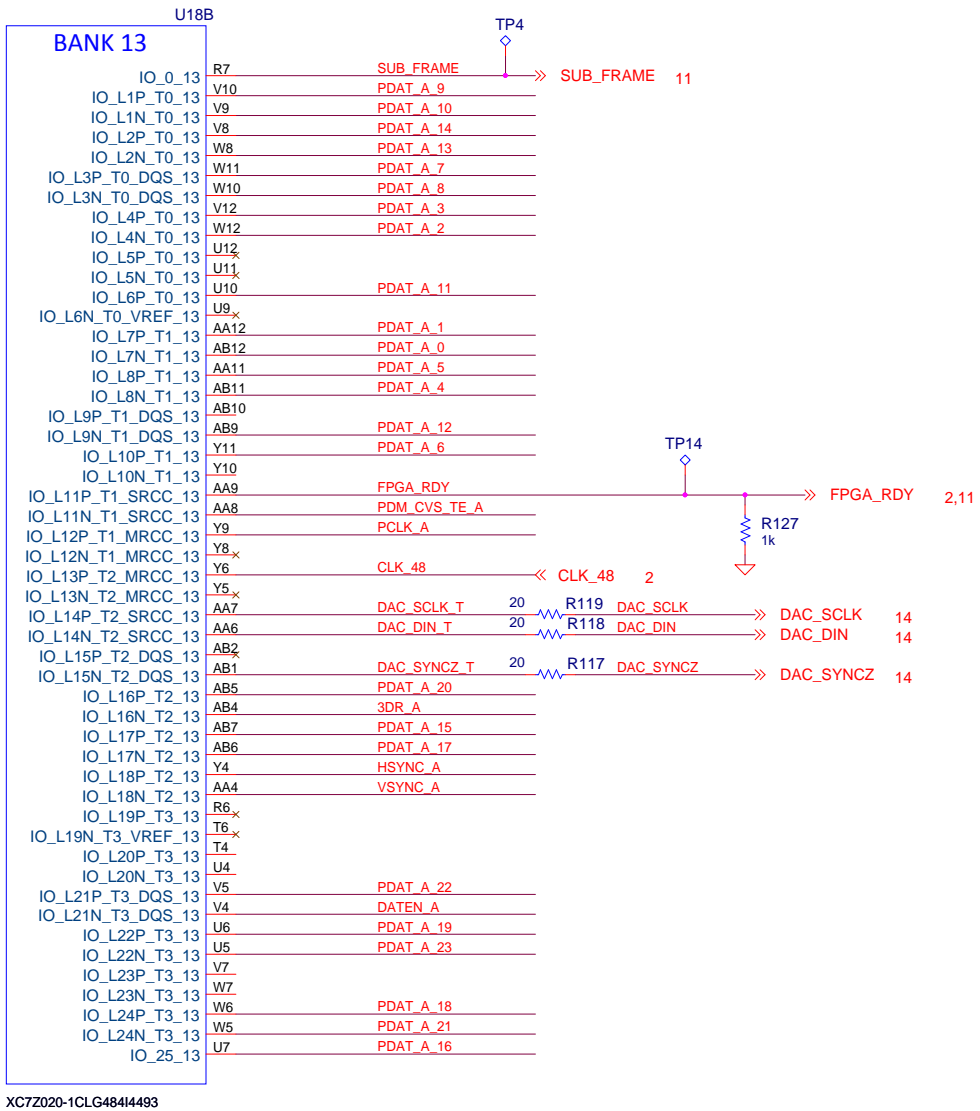
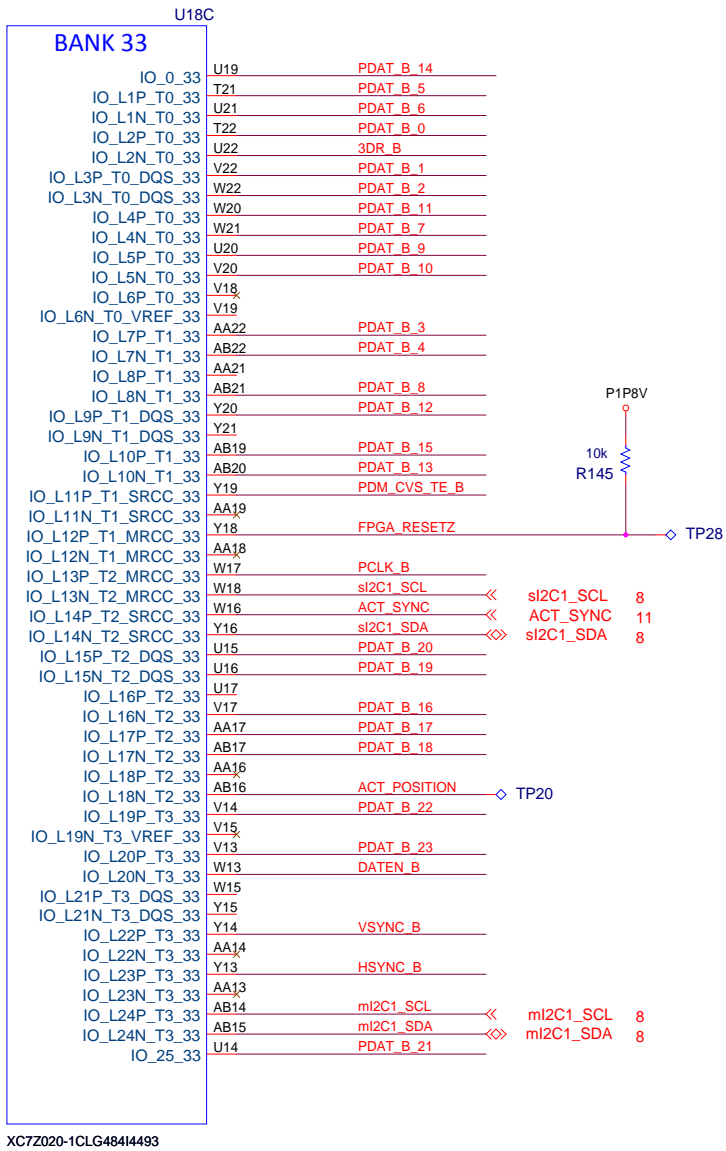
DWN	Roger Perry	DATE	OCT-24-2017	TEXAS INSTRUMENTS - DLP® Products			
ENGR	Roger Perry	DATE	OCT-24-2017	(C) COPYRIGHT 2017 Texas Instruments Inc. All Rights Reserved			
SYS	Paul Rancuret	DATE	OCT-24-2017	TITLE TIDA080000 Display Board			
APVD	Jeff Dennis	DATE	OCT-24-2017	DRAWING NO	TIDA080000	REV	B
QA	---	---	---	11 x 17	Orcad Capture 16.6	SHEET	1 of 15



CONNECTION TO FRONT END PROVIDING PARALLEL RGB VIDEO INPUT  
(PLACE ON TOP SIDE)



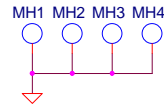




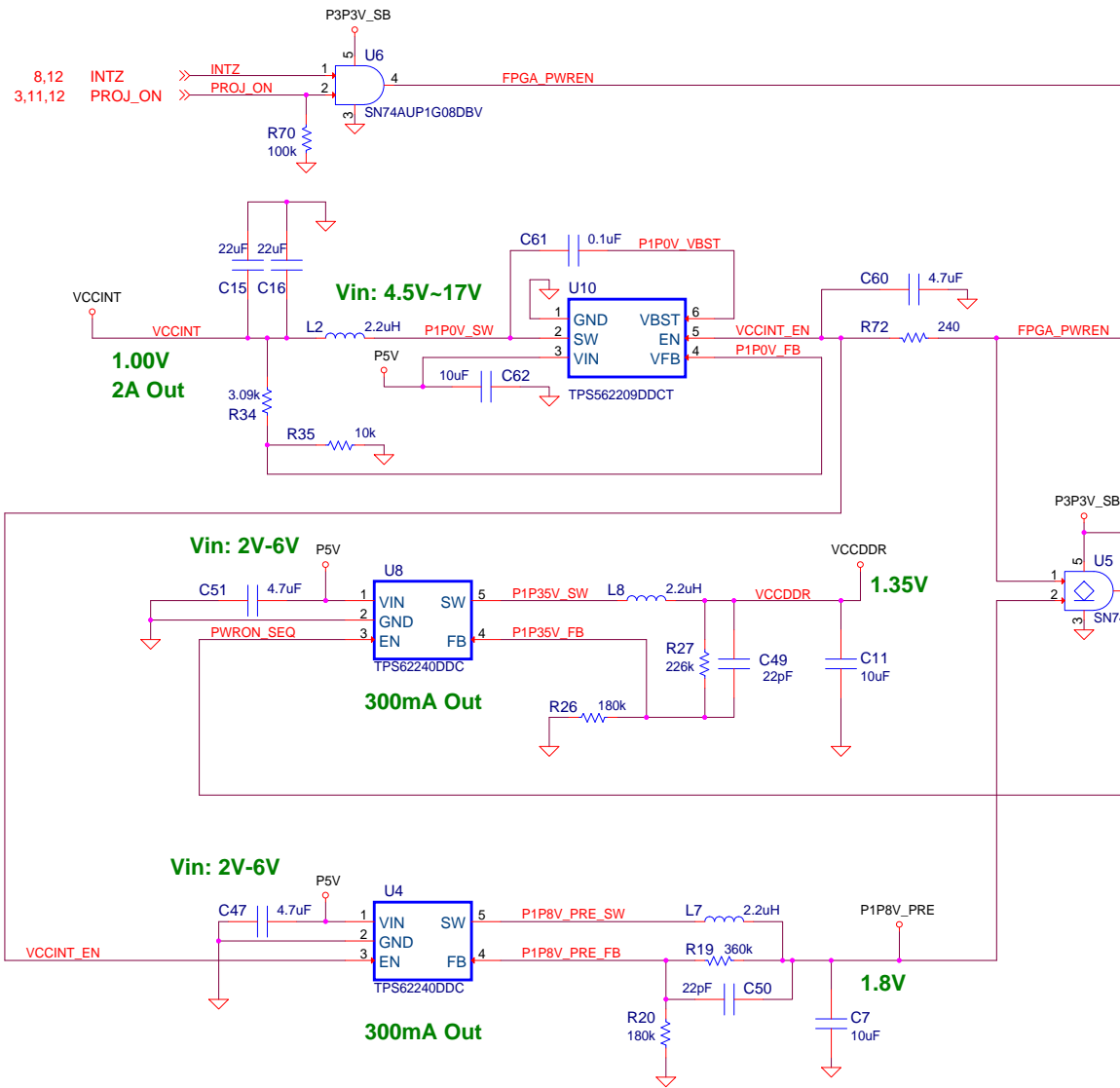
ASIC PDATA Interface



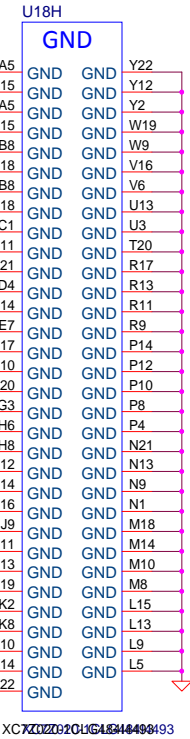
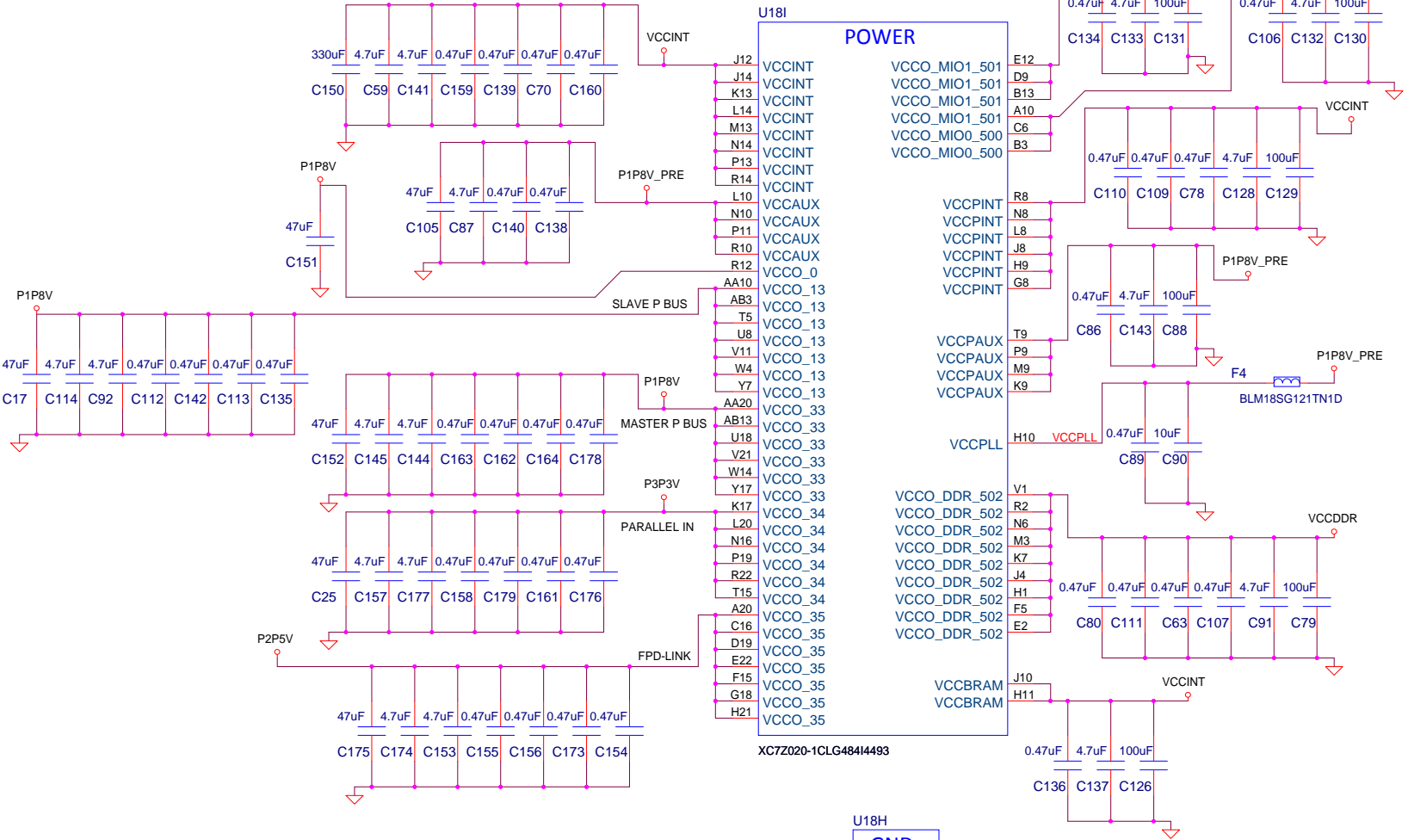
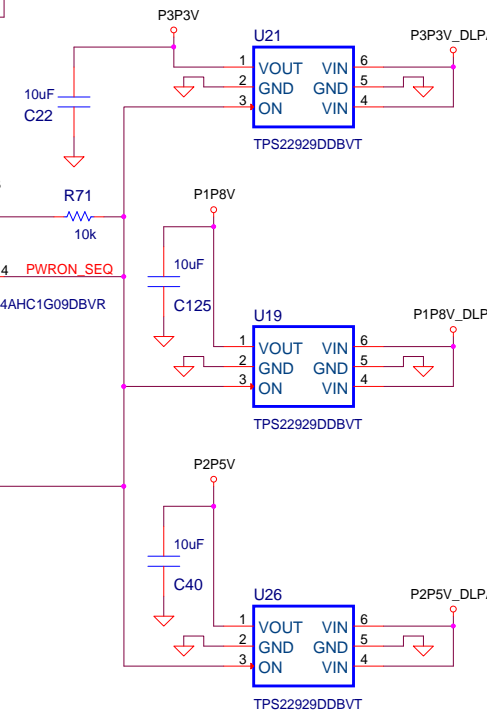
# BOARD MOUNTING HOLES



- SHUTDOWN WHEN FAST PARK DETECTED.
- PROJ\_ON GOING HIGH ENABLES POWER TO FPGA.



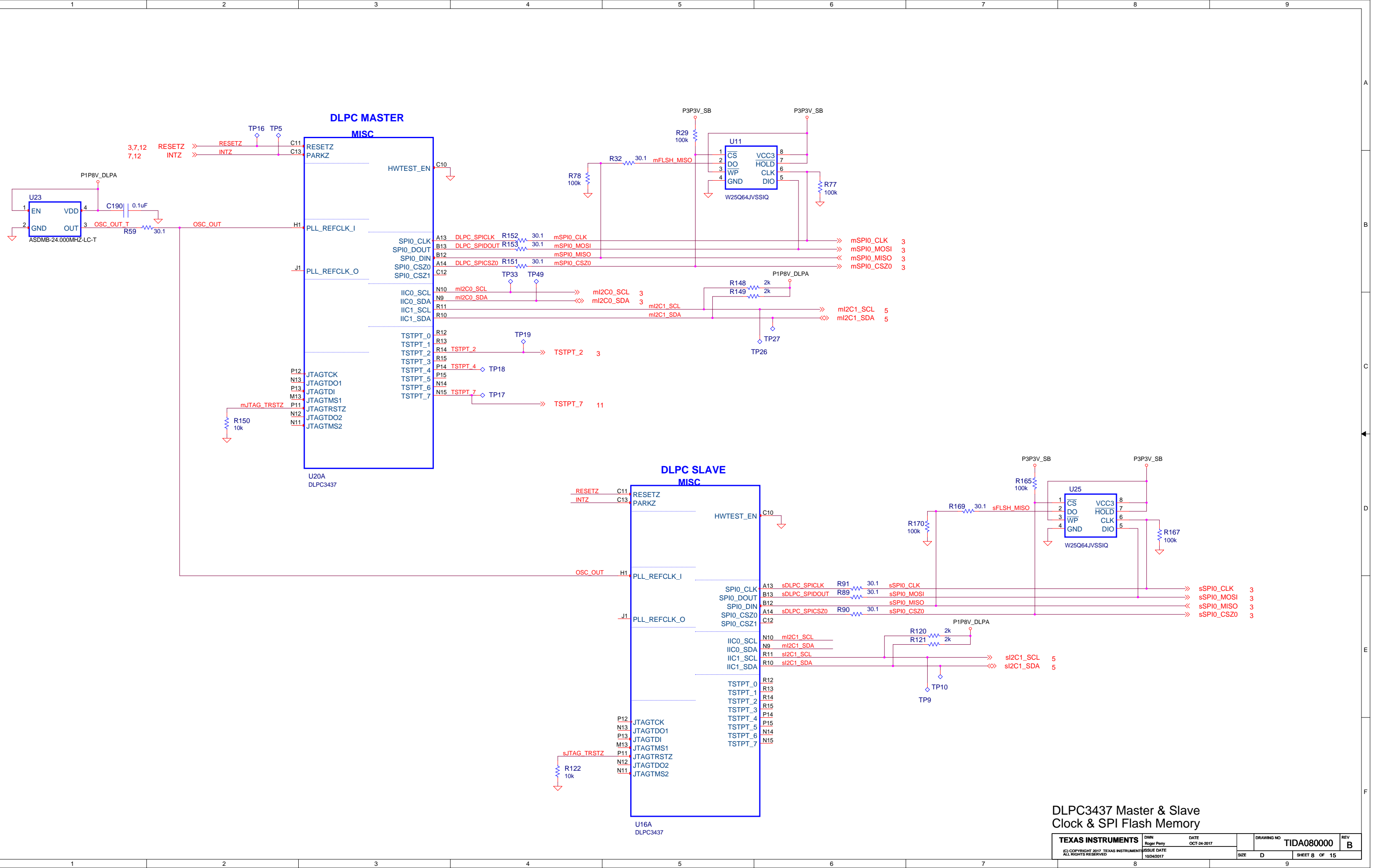
# LOAD SWITCHES FOR I/O POWER



# FPGA POWER

TEXAS INSTRUMENTS		DWN Roger Perry	DATE OCT-24-2017	DRAWING NO TIDA080000	REV B
(C) COPYRIGHT 2017, TEXAS INSTRUMENTS ALL RIGHTS RESERVED		ISSUE DATE 10/24/2017	SIZE D	SHEET 7 OF 15	

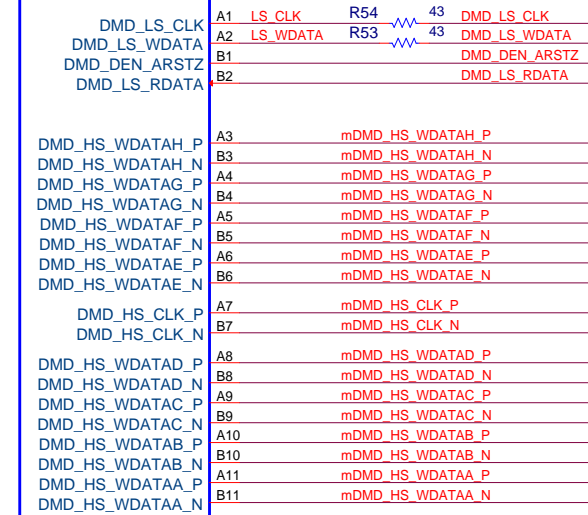




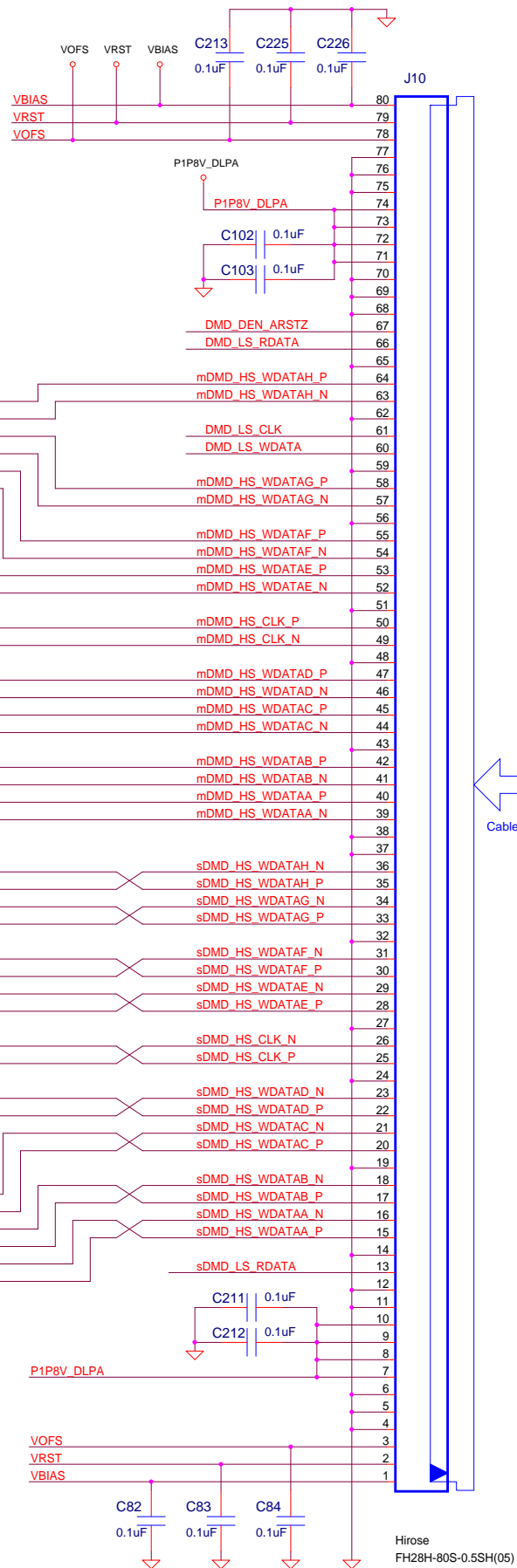
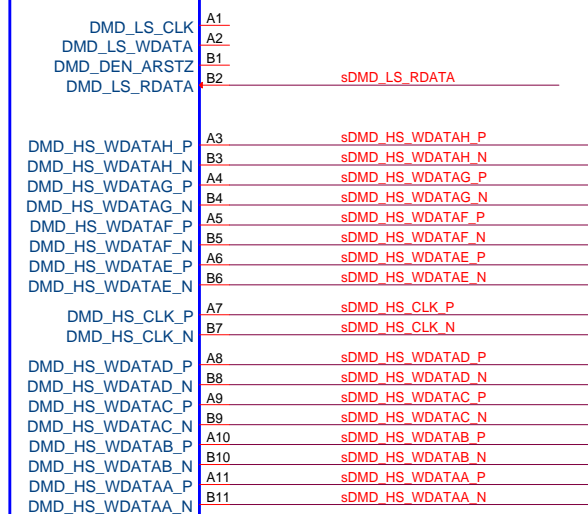




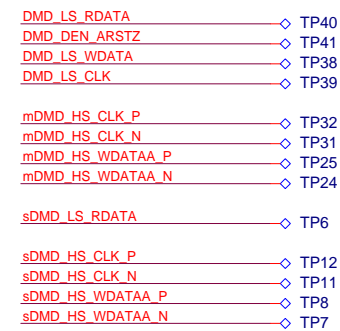
MASTER  
DMD INTERFACE



SLAVE  
DMD INTERFACE



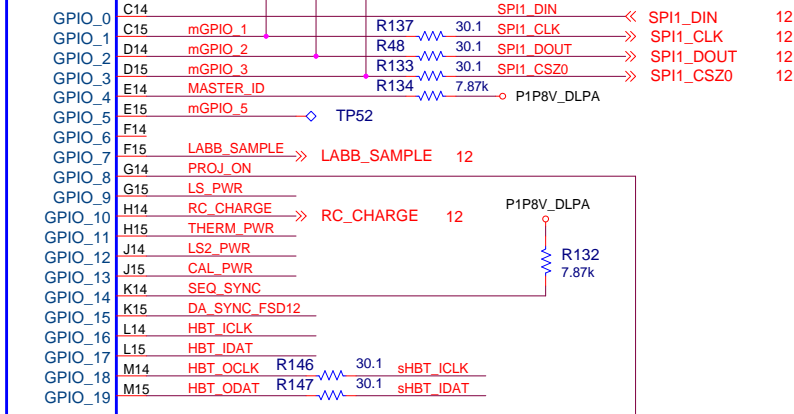
Cable Insert Direction



DMD INTERFACE

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	ISSUE DATE 10/24/2017				
	SIZE D	SHEET 10 OF 15			

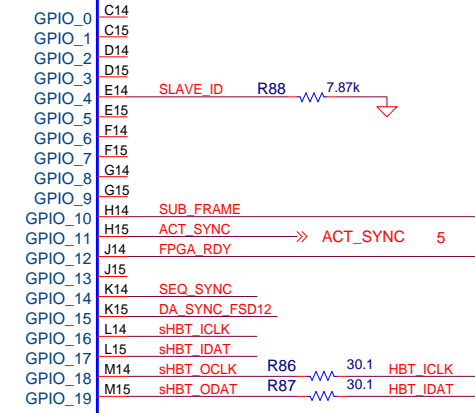
MASTER  
GPIO



U20C  
DLPC3437

3,7,12 PROJ\_ON » PROJ\_ON

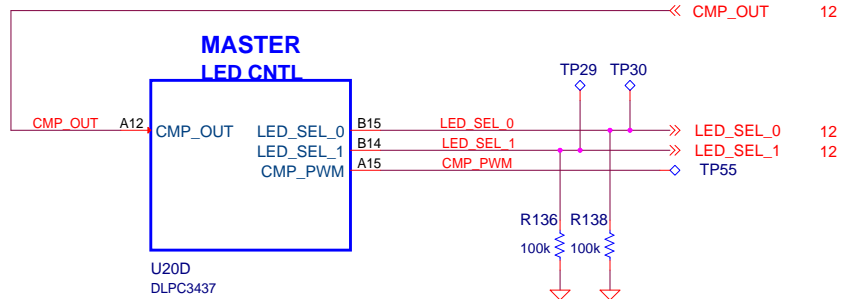
SLAVE  
GPIO



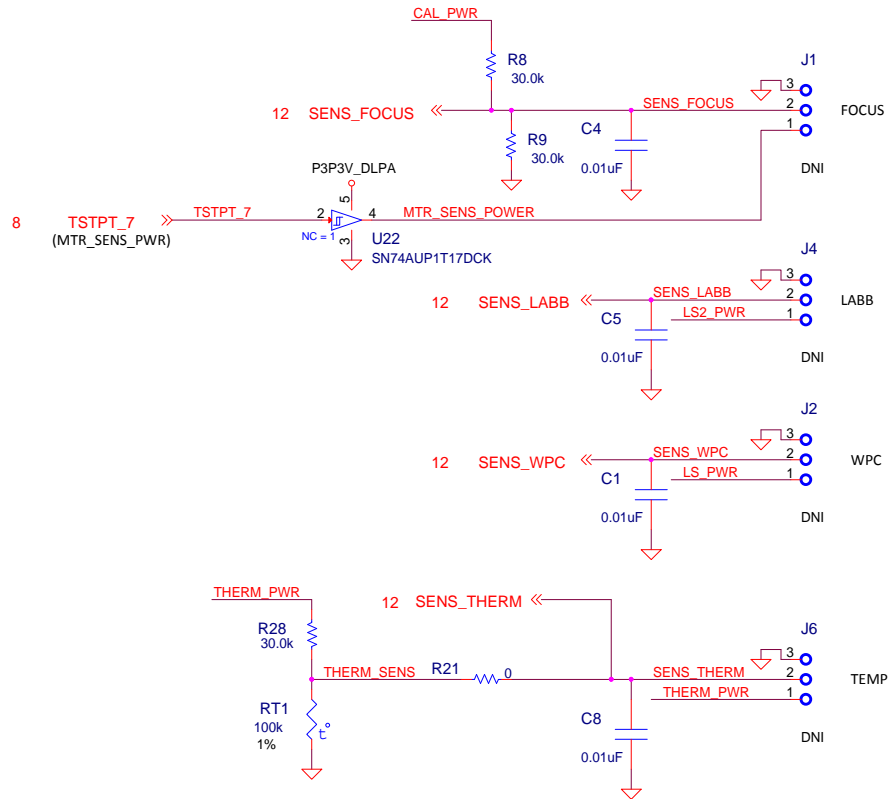
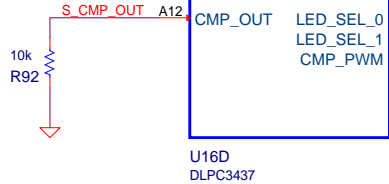
U16C  
DLPC3437

2,5 FPGA\_RDY »  
5 SUB\_FRAME »

MASTER  
LED CNTL



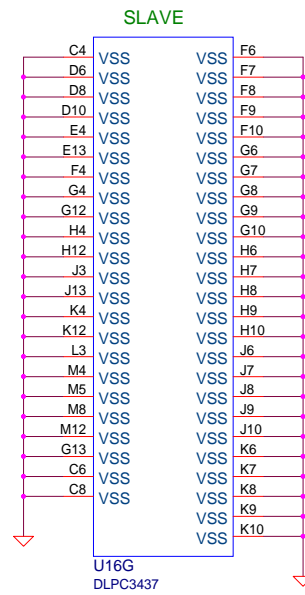
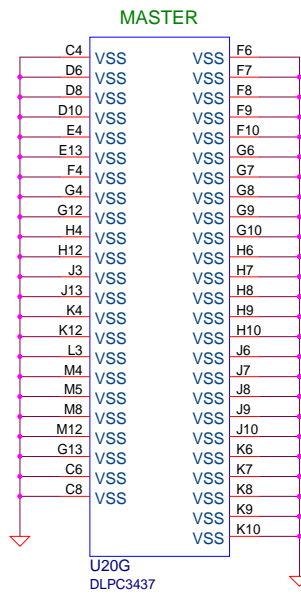
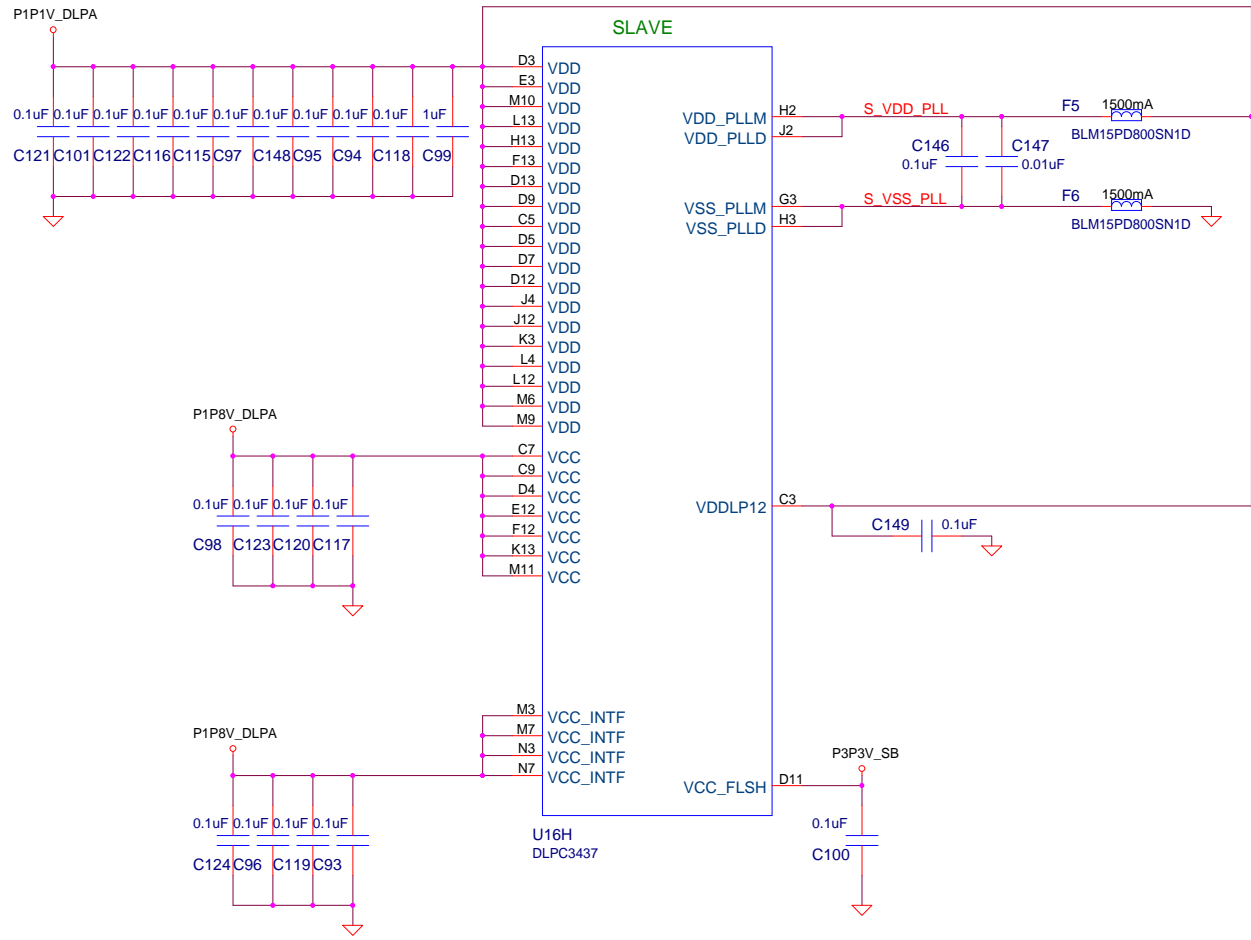
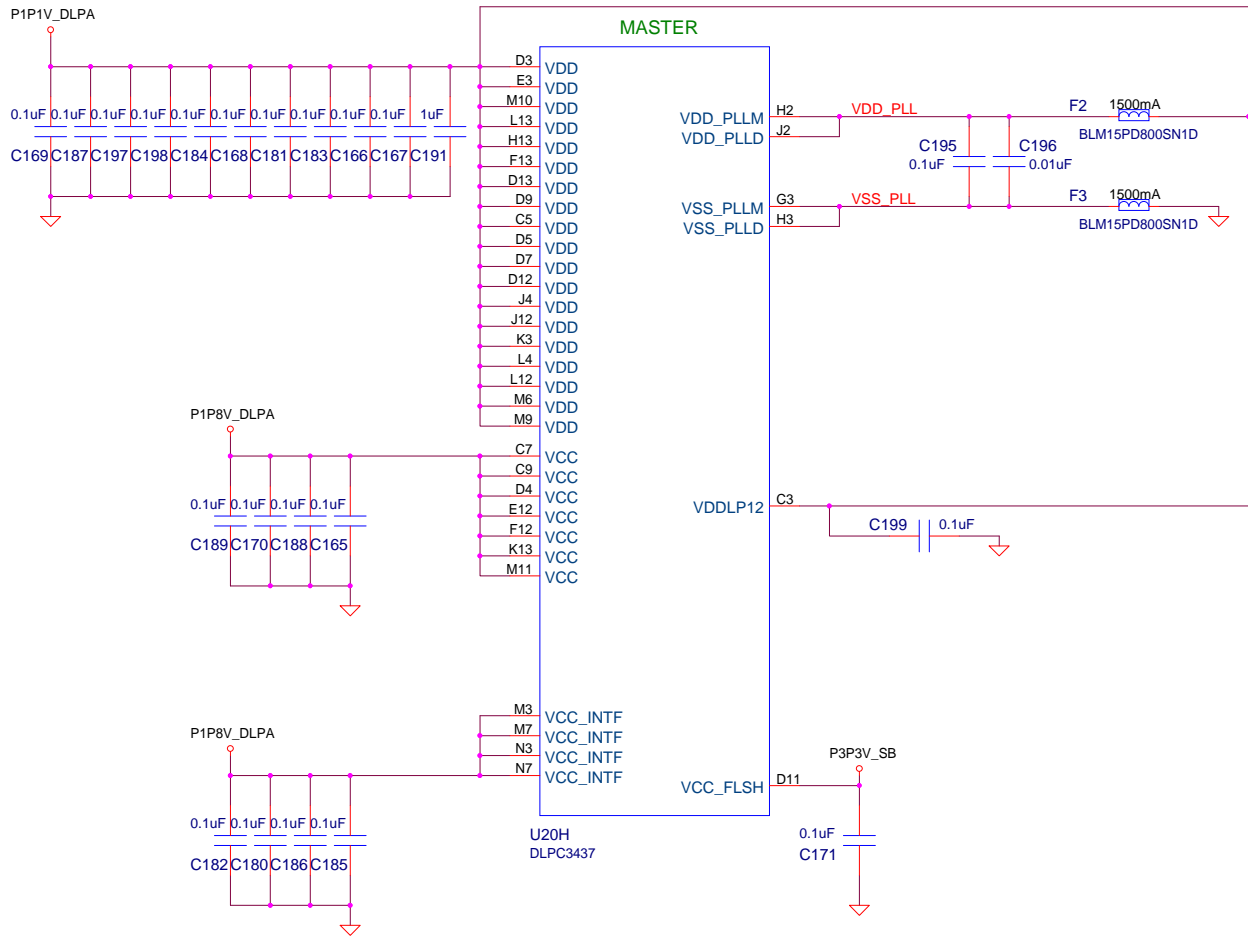
SLAVE  
LED CNTL



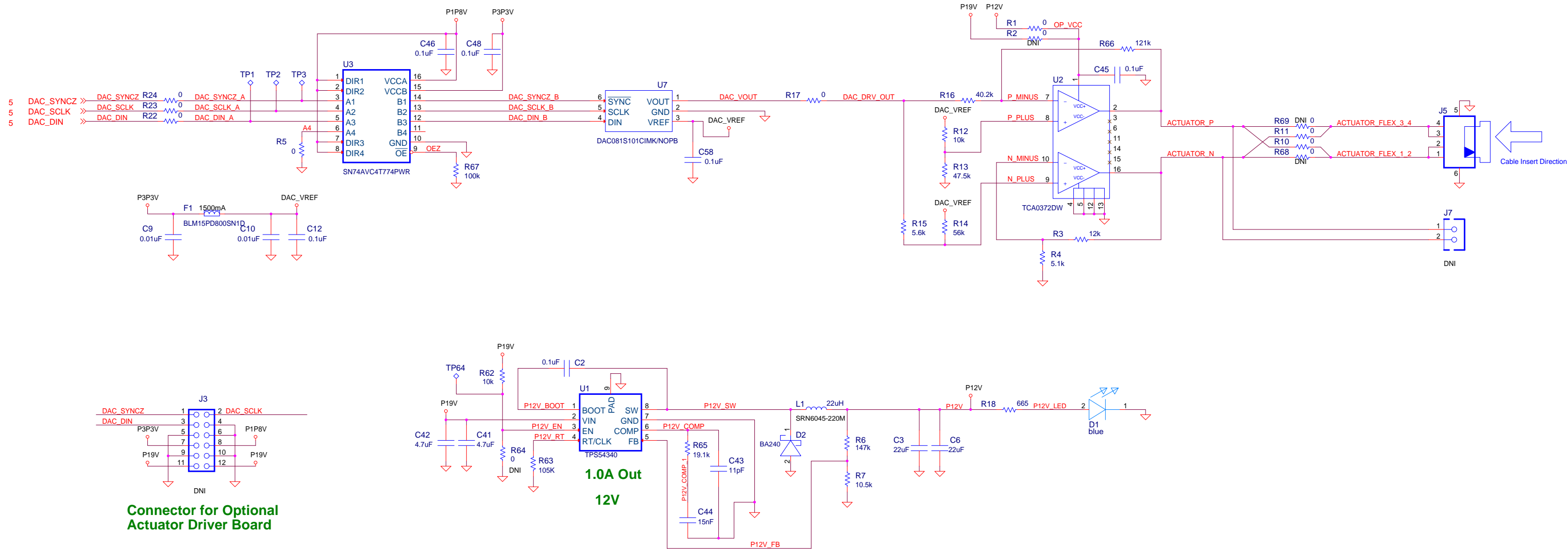
DLPC3437 GPIO & DUAL ASIC CONTROL

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	ISSUE DATE 10/24/2017			
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POWER - MASTER & SLAVE ASIC



Connector for Optional  
Actuator Driver Board

## ACTUATOR DRIVER

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SIZE D SHEET 14 OF 15

# Revisions

Rev. A: Initial Release

- Rev. B:
- Correct DDR3 DQS connections (page 6). PS\_DDR\_DQS\_P/N1 connects to UDQS and PS\_DDR\_P/N0 connects to LDQS.
  - Remove R74 & R76 (page 6).
  - Add RC circuit between LED\_ANODE and RLIM (R176 & C232 on page 12).

## REVISION NOTES

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	ISSUE DATE 10/24/2017		SIZE <b>D</b>	SHEET 15 OF 15